LM139A-MIL クワッド差動コンパレータ

1 特長

- 広い電源電圧範囲
  - 単一電源: 2V～36V
    (30Vでテスト)
  - デュアル電源: ±1V～±18V
    (±15Vでテスト)
- 電源電圧に影響されない低い電源消費電流: 0.8mA (標準値)
- 低い入力バイアス電流: 25nA (標準値)
- 低い入力オフセット電圧: 2mV (標準値)
- 同相入力電圧範囲にグランドが含まれる
- 差動入力電圧範囲が最大定格電源電圧と同じ: ±36V
- 低い出力飽和電圧
- TTL、MOS、CMOS互換出力
- MIL-PRF-38535準拠の製品については、特に記述のない限り、すべてのパラメータはテスト済みです。
  他のすべての製品については、量産プロセスにすべてのパラメータのテストが含まれているとは限りません。

2 アプリケーション

- 産業用
- オートモーティブ（車載）
  - インフォテインメントおよびクラスタ
  - 車体制御モジュール
- 電源監視
- 発振器
- ピーク検出器
- 論理電圧変換

3 概要

LM139A-MILデバイスは4つの独立した電圧コンパレータで構成され、広い電圧範囲の単一電源で動作するよう設計されています。デュアル電源での動作も可能です。この場合、2つの電源の差が2V～36Vで、V_{CC}が入力同相電圧よりも1.5V以上高いことが条件です。消費電流は、電源電圧に依存しません。出力を他のオープン・コレクタ出力に接続し、ワイヤードAND関係を構築できます。

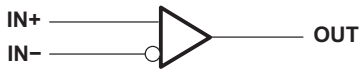
LM139A-MILデバイスは、軍事用温度範囲-55℃～+125℃全体での動作が規定されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
LM139A-MIL	CDIP (14)	21.30mm×7.60mm
	LCCC (20)	8.90mm×8.90mm
	CFP (14)	9.20mm×6.29mm
	SOIC (14)	8.70mm×3.90mm
	PDIP (14)	19.30mm×6.40mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

概略回路図



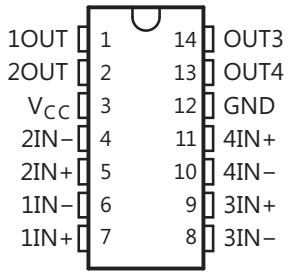
目次

4 改訂履歴

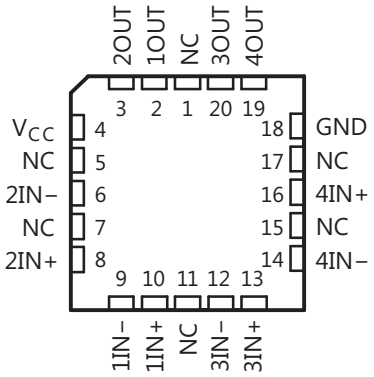
日付	改訂内容	注
2017年6月	*	初版

5 Pin Configuration and Functions

D, N, J, or W Package
SOIC, PDIP, CDIP, or CFP
Top View



FK Package
20-Pin LCCC
Top View



NC = no internal connection.

Pin Functions

PIN			I/O[1]	DESCRIPTION
NAME	D, J, W, N	FK		
1IN+	7	10	I	Positive input pin of the comparator 1
1IN–	6	9	I	Negative input pin of the comparator 1
1OUT	1	2	O	Output pin of the comparator 1
2IN+	5	8	I	Positive input pin of the comparator 2
2IN–	4	6	I	Negative input pin of the comparator 2
2OUT	2	3	O	Output pin of the comparator 2
3IN+	9	13	I	Positive input pin of the comparator 3
3IN–	8	12	I	Negative input pin of the comparator 3
3OUT	14	20	O	Output pin of the comparator 3
4IN+	11	16	I	Positive input pin of the comparator 4
4IN–	10	14	I	Negative input pin of the comparator 4
4OUT	13	19	O	Output pin of the comparator 4
GND	12	18	—	Ground
V_{CC}	3	4	—	Supply pin
NC	—	1	—	No connect (no internal connection)
		5		
		7		
		11		
		15		
		17		

(1) I = Input, O = Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)			36	V
V_{ID}	Differential input voltage(3)			±36	V
V_I	Input voltage range (either input)		–0.3	36	V
I_K	Input current(4)			–50	mA
V_O	Output voltage			36	V
I_O	Output current			20	mA
	Duration of output short circuit to ground(5)		Unlimited		
T_J	Operating virtual-junction temperature			150	°C
	Case temperature for 60 s	FK package		260	°C
	Lead temperature 1.6 mm (1/16 in) from case for 60 s	J package		300	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground.
(3) Differential voltages are at xIN+ with respect to xIN–.
(4) Input current flows through parasitic diode to ground and will turn on parasitic transistors that will increase I_{CC} and may cause output to be incorrect. Normal operation resumes when input is removed.
(5) Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2	30	V
T_J	Junction temperature	–55	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LM139A-MIL					UNIT
		D (SOIC)	N (PDIP)	J (CDIP)	W (CFP)	FK (LCCC)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	98.8	79	89.5	156.2	82.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	64.3	73.4	46.1	86.7	60.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	59.7	58.7	78.7	154.6	59.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	25.7	48.3	3	56.5	53	°C/W
ψ_{JB}	Junction-to-board characterization parameter	59.3	58.5	71.8	133.5	58.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	24.2	14.3	9.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]			MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{CC} = 5 V to 30 V, V_{IC} = V_{ICR} min, V_O = 1.4 V		T_A = 25°C		1	2	mV
				T_A = –55°C to +125°C			4	
I_{IO}	Input offset current	V_O = 1.4 V		T_A = 82.5		3	25	nA
				T_A = 60.7			100	
I_{IB}	Input bias current	V_O = 1.4 V		T_A = 59.4		–25	–100	nA
				T_A = 53			–300	
V_{ICR}	Common-mode input-voltage range[2]			T_A = 58.4	0 to V_{CC} – 1.5			V
				T_A = 9.7	0 to V_{CC} – 2			
A_{VD}	Large-signal differential-voltage amplification	V_{CC+} = ±7.5 V, V_O = –5 V to 5 V		T_A = 25°C	50	200		V/mV
I_{OH}	High-level output current	V_{ID} = 1 V	V_{OH} = 5 V	T_A = 25°C		0.1		nA
			V_{OH} = 30 V	T_A = –55°C to +125°C			1	µA
V_{OL}	Low-level output voltage	V_{ID} = –1 V,	I_{OL} = 4 mA	T_A = 25°C		150	400	mV
				T_A = –55°C to +125°C			700	
I_{OL}	Low-level output current	V_{ID} = –1 V,	V_{OL} = 1.5 V	T_A = 25°C	6	16		mA
I_{CC}	Supply current (four comparators)	V_O = 2.5 V,	No load	T_A = 25°C		0.8	2	mA

(1) All characteristics are measured with zero common-mode input voltage, unless otherwise specified.
(2) The voltage at either input or common-mode must not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V_{CC+} – 1.5 V; however, one input can exceed V_{CC}, and the comparator will provide a proper output state as long as the other input remains in the common-mode range. Either or both inputs can go to 30 V without damage.

6.6 Switching Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		TYP	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF[1][2]	100-mV input step with 5-mV overdrive	1.3	µs
		TTL-level input step	0.3	

(1) C_L includes probe and jig capacitance.
(2) The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

6.7 Typical Characteristics

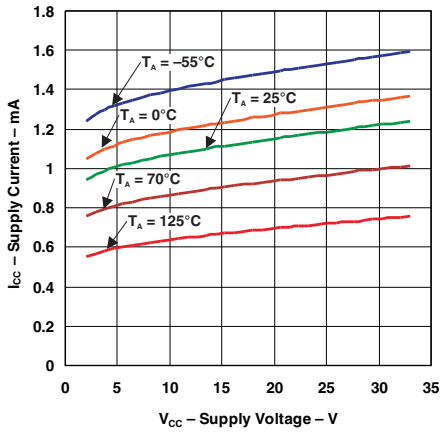


Figure 1. Supply Current vs Supply Voltage

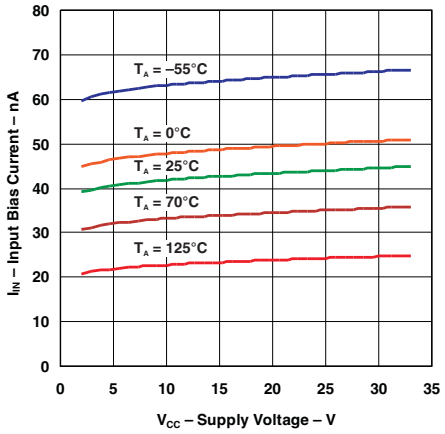


Figure 2. Input Bias Current vs Supply Voltage

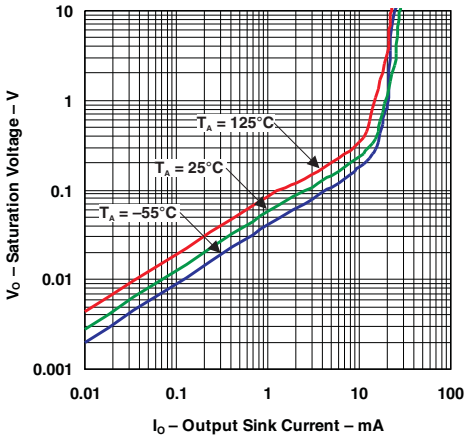


Figure 3. Output Saturation Voltage

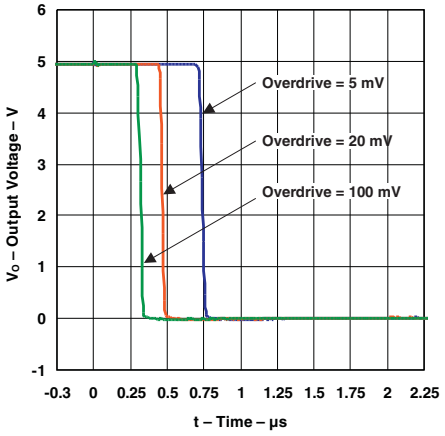


Figure 4. Response Time for Various Overdrives Negative Transition

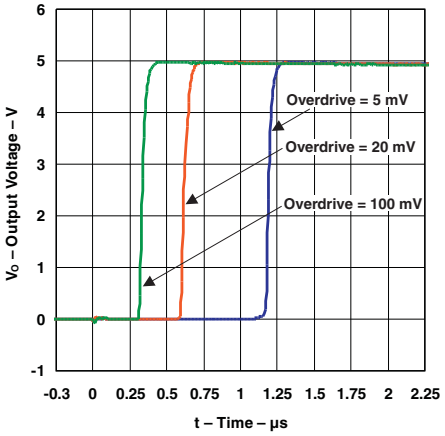


Figure 5. Response Time for Various Overdrives Positive Transition

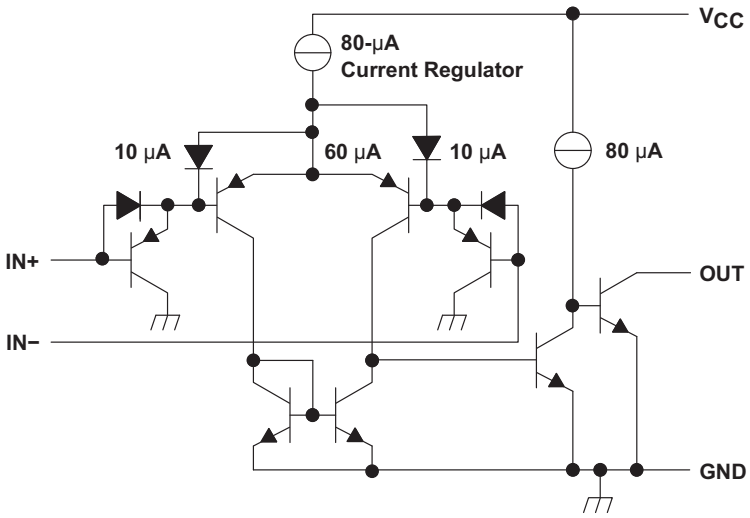
7 Detailed Description

7.1 Overview

The LM139A-MIL is a quad comparator with the ability to operate up to an absolute maximum of 36 V on the supply pin. This standard device has proven ubiquity and versatility across a wide range of applications. This is due to very wide supply voltages range (2 V up to 32 V), low Iq, and fast response of the device.

The open-drain output allows the user to configure the output logic low voltage (V_{OL}) and allows the comparator to be used in AND functionality.

7.2 Functional Block Diagram



COMPONENT COUNT	
Epi-FET	1
Diodes	2
Resistors	2
Transistors	30

Figure 6. Schematic (Each Comparator)

7.3 Feature Description

The comparator consists of a PNP Darlington pair input, allowing the device to operate with very high gain and fast response with minimal input bias current. The input Darlington pair creates a limit on the input common-mode voltage capability, allowing the comparator to accurately function from ground to (V_{CC} – 1.5 V) differential input. Allow for (V_{CC} – 2 V) at cold temperature.

The output consists of an open-collector NPN (pulldown or low-side) transistor. The output NPN sinks current when the negative input voltage is higher than the positive input voltage and the offset voltage. The VOL is resistive and scales with the output current. See the *Specifications* section for V_{OL} values with respect to the output current.

7.4 Device Functional Modes

7.4.1 Voltage Comparison

The comparator operates solely as a voltage comparator, comparing the differential voltage between the positive and negative pins and outputting a logic low or high impedance (logic high with pullup) based on the input differential polarity.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Validate and test the design implementation to confirm system functionality.

8.1 Application Information

Typically, a comparator compares either a single signal to a reference, or to two differnt signals. Many users take advantage of the open-drain output to drive the comparison logic output to a logic voltage level to an MCU or logic device. The wide supply range and high voltage capability makes LM139A-MIL optimal for level shifting to a higher or lower voltage.

8.2 Typical Application

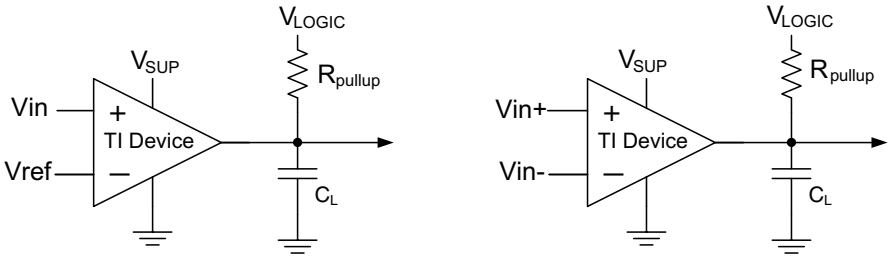


Figure 7. Single-ended and Differential Comparator Configurations

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	0 V to Vsup-1.5 V
Supply Voltage	4.5 V to V_{CC} maximum
Logic Supply Voltage	0 V to V_{CC} maximum
Output Current (R_{PULLUP})	1 µA to 4 mA
Input Overdrive Voltage	100 mV
Reference Voltage	2.5 V
Load Capacitance (C_L)	15 pF

8.2.2 Detailed Design Procedure

When using the LM139A-MIL in a general comparator application, determine the following:

- Input voltage range
- Minimum overdrive voltage
- Output and drive current
- Response time

8.2.2.1 Input Voltage Range

When choosing the input voltage range, the input common-mode voltage range (V_{ICR}) must be taken in to account. If temperature operation is above or below 25°C the V_{ICR} can range from 0 V to V_{CC}– 2 V. This limits the input voltage range to as high as V_{CC}– 2 V and as low as 0 V. Operation outside of this range can yield incorrect comparisons.

The following list describes the outcomes of some input voltage situations.

- When both IN– and IN+ are both within the common-mode range:
  - If IN– is higher than IN+ and the offset voltage, the output is low and the output transistor is sinking current
  - If IN– is lower than IN+ and the offset voltage, the output is high impedance and the output transistor is not conducting
- When IN– is higher than common mode and IN+ is within common mode, the output is low and the output transistor is sinking current
- When IN+ is higher than common mode and IN– is within common mode, the output is high impedance and the output transistor is not conducting
- When IN– and IN+ are both higher than common mode, the output is low and the output transistor is sinking current

8.2.2.2 Minimum Overdrive Voltage

Overdrive voltage is the differential voltage produced between the positive and negative inputs of the comparator over the offset voltage (V_{IO}). To make an accurate comparison, the overdrive voltage (V_{OD}) must be higher than the input offset voltage (V_{IO}). Overdrive voltage can also determine the response time of the comparator, with the response time decreasing with increasing overdrive. Figure 8 and Figure 9 show positive and negative response times with respect to overdrive voltage.

8.2.2.3 Output and Drive Current

Output current is determined by the load and pullup resistance and logic and pullup voltage. The output current produces a low-level output voltage (V_{OL}) from the comparator, where V_{OL} is proportional to the output current.

The output current can also effect the transient response.

8.2.2.4 Response Time

Response time is a function of input over-drive. See the *Typical Characteristics* graphs for typical response times. The rise and fall times can be determined by the load capacitance (C_L), load/pull-up resistance (R_{PULLUP}) and equivalent collector-emitter resistance (R_{CE}).

- The rise time (τ_R) is approximately $\tau_R \sim R_{PULLUP} \times C_L$
- The fall time (τ_F) is approximately $\tau_F \sim R_{CE} \times C_L$
  - R_{CE} can be determined by taking the slope of Figure 3 in its linear region at the desired temperature, or by dividing the V_{OL} by I_{OUT}

8.2.3 Application Curves

Figure 8 and Figure 9 were generated with scope probe parasitic capacitance of 50 pF.

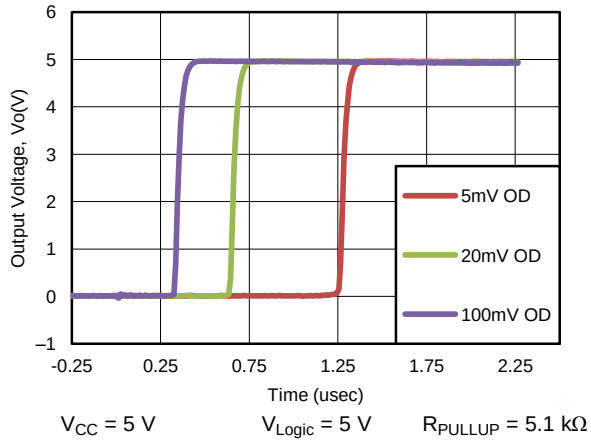


Figure 8. Response Time vs Output Voltage (Positive Transition)

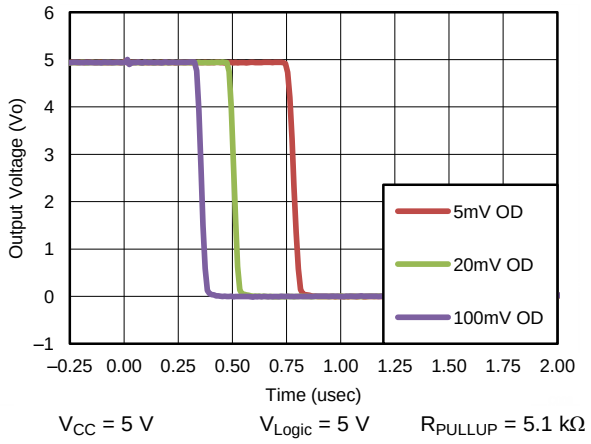


Figure 9. Response Time vs Output Voltage (Negative Transition)

9 Power Supply Recommendations

For fast response and comparison applications with noisy or AC inputs, use a bypass capacitor on the supply pin to reject any variation on the supply voltage. This variation can affect the common-mode range of the comparator input and create an inaccurate comparison.

10 Layout

10.1 Layout Guidelines

To create an accurate comparator application without hysteresis, maintain a stable power supply with minimized noise and glitches, which can affect the high level input common-mode voltage range. To achieve this accuracy, add a bypass capacitor between the supply voltage and ground. Place a bypass capacitor on the positive power supply and negative supply (if available).

NOTE

If a negative supply is not being used, do not place a capacitor between the GND pin of the device and system ground.

10.2 Layout Example

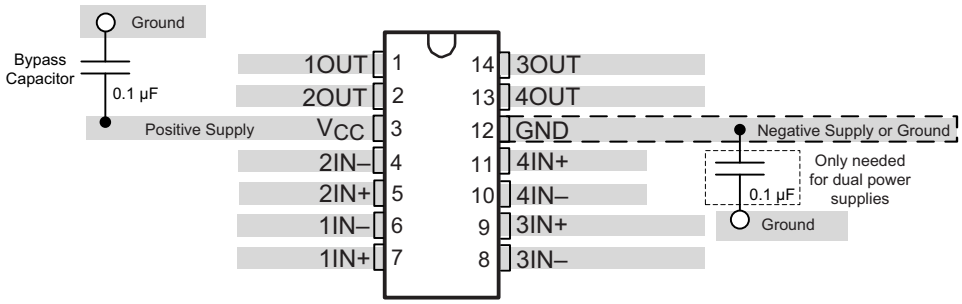


Figure 10. LMx39 Layout Example

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。このデータシートのブラウザ対応版については、左側にあるナビゲーションを参照してください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-87739012A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-87739012A LM139AFKB	Samples
5962-8773901CA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8773901CA LM139AJB	Samples
5962-8773901DA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8773901DA LM139AWB	Samples
LM139AFKB	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-87739012A LM139AFKB	Samples
LM139AJ	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	LM139AJ	Samples
LM139AJB	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8773901CA LM139AJB	Samples
LM139AW	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	LM139AW	Samples
LM139AWB	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8773901DA LM139AWB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

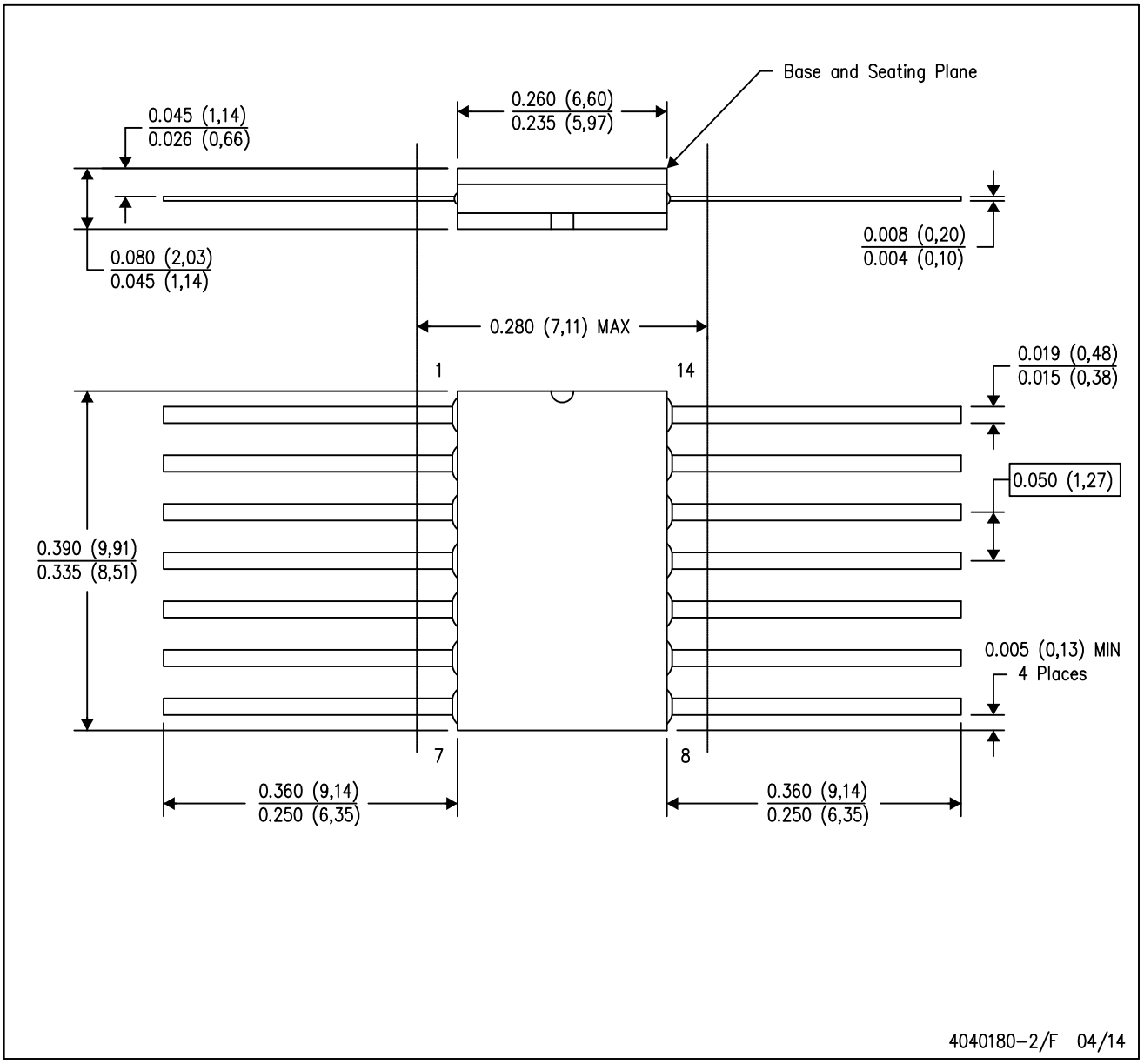
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

W (R–GDFP–F14) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

GENERIC PACKAGE VIEW

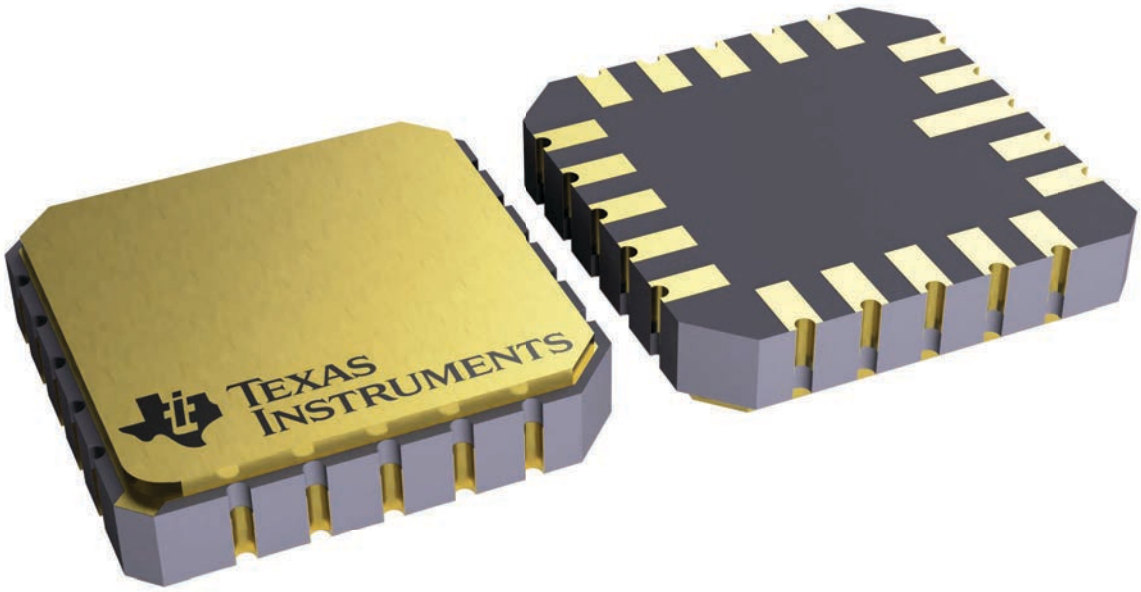
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

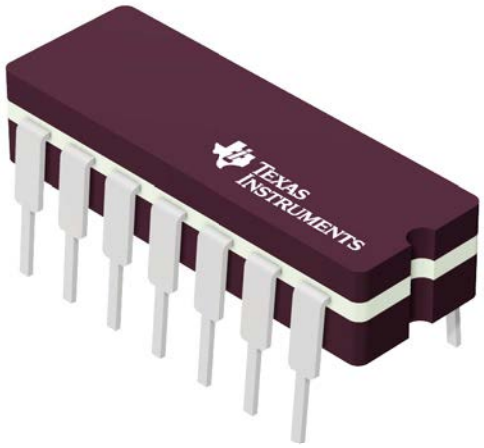


4229370VA\

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

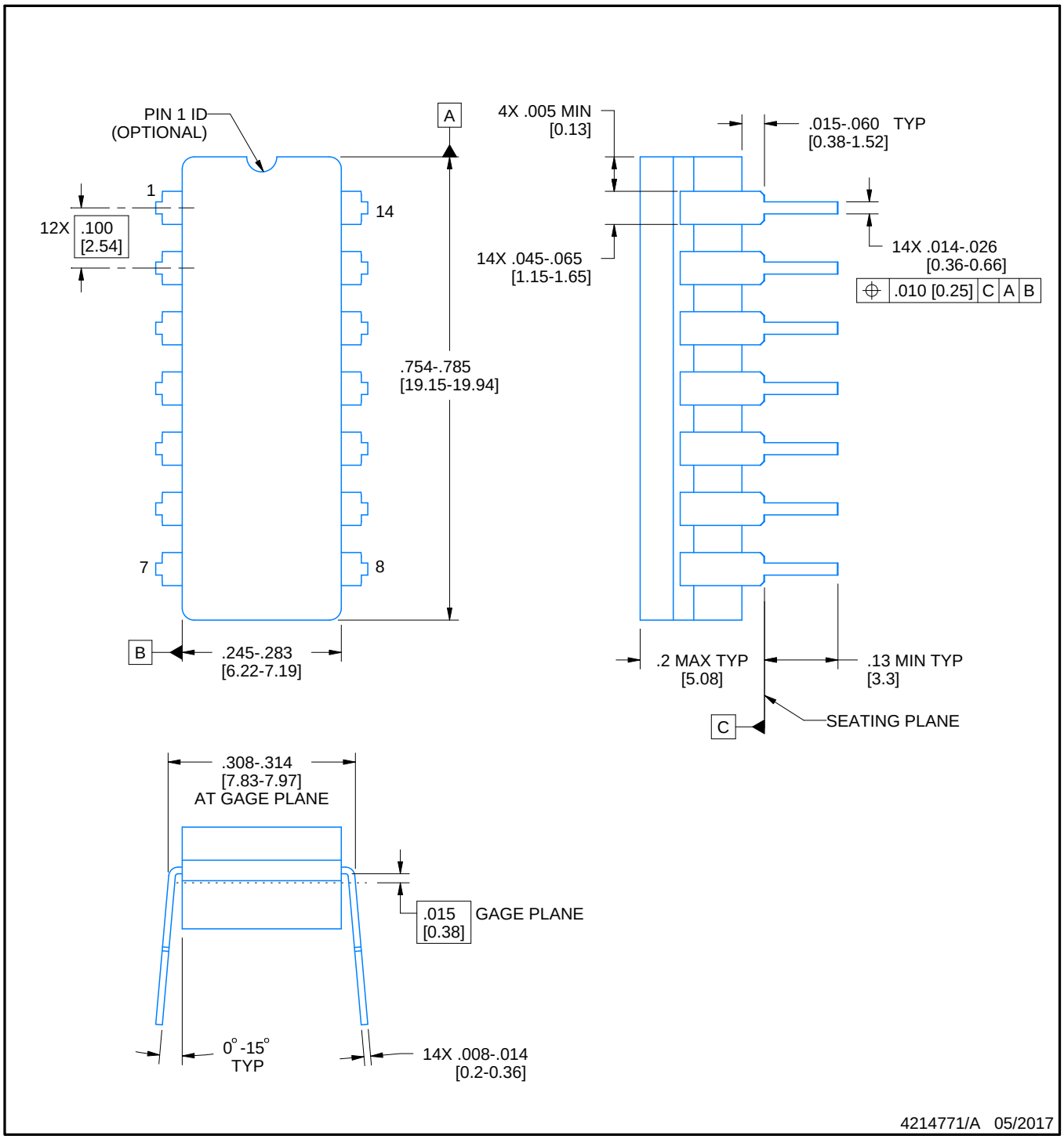
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

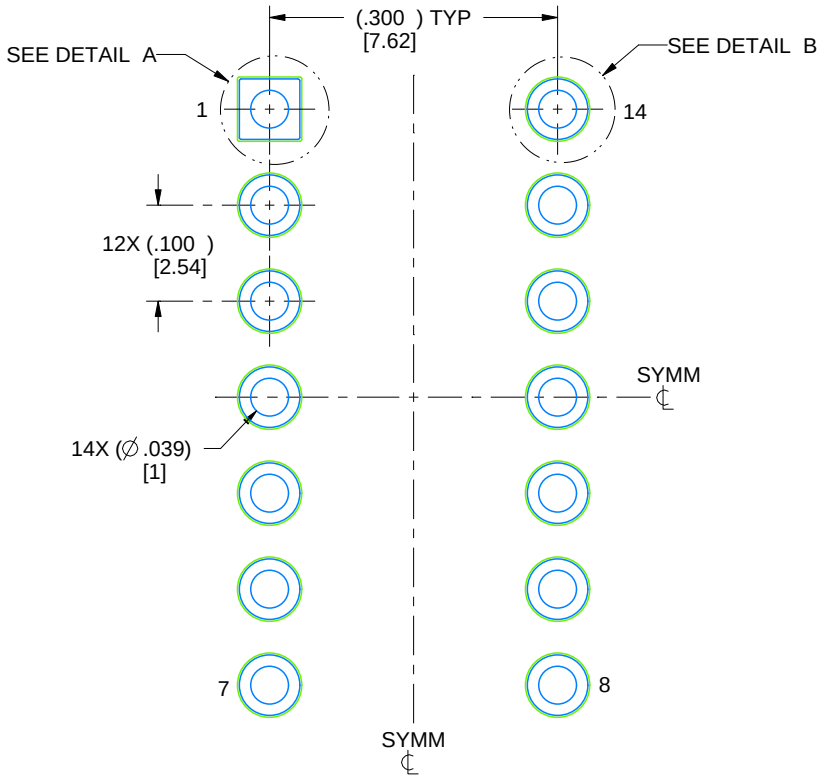
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

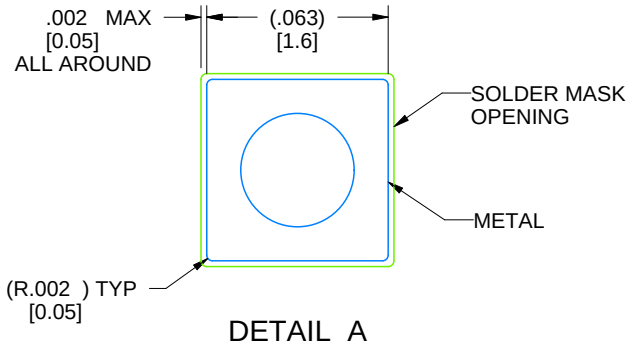
J0014A

CDIP - 5.08 mm max height

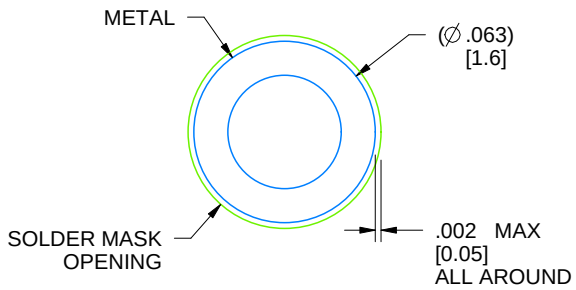
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

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