

# LM3410/LM3410-Q1 525kHz/1.6MHz、内部補償回路搭載、定電流昇圧型 およびSEPIC型LEDドライバ

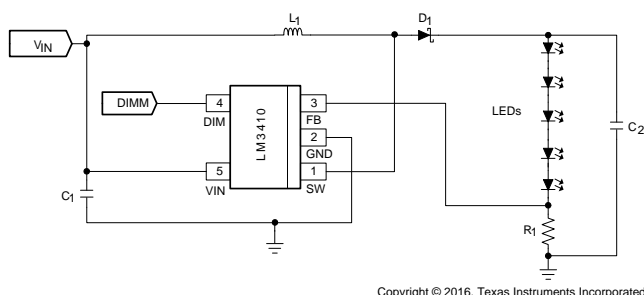
## 1 特長

- 車載アプリケーション用に認定済み
- 以下のAEC-Q100試験ガイドンス:
  - デバイス温度グレード1: -40°C~125°C動作時周囲温度範囲
  - デバイスHBM ESD分類レベル2
  - デバイスCDM ESD分類レベルC6
- 省スペースのSOT-23およびWSONパッケージ
- 入力電圧範囲: 2.7V~5.5V
- 出力電圧範囲: 3V~24V
- スイッチ電流制限: 2.8A (標準値)
- 高いスイッチング周波数
  - 525kHz (LM3410Y)
  - 1.6MHz (LM3410X)
- 170mΩのNMOSスイッチ
- 190mVの内部基準電圧
- 内部的なソフトスタート
- 電流モード、PWMの動作
- サーマル・シャットダウン

## 2 アプリケーション

- LEDバックライトの電流ソース
- リチウムイオン・バックライトOLEDおよびHB LEDドライバ
- ハンドヘルド機器
- LEDフラッシュ・ドライバ
- 車載用アプリケーション

代表的な昇圧アプリケーションの回路



## 3 概要

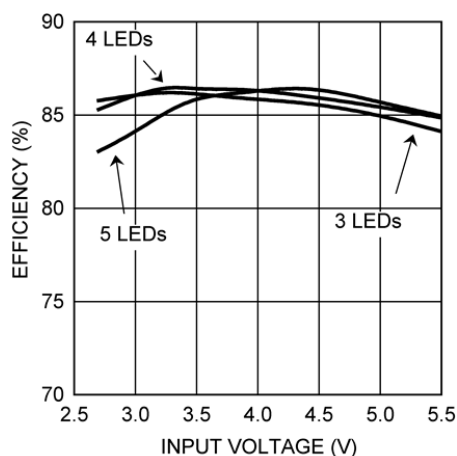
LM3410およびLM3410-Q1は定電流のLEDドライバであり、モノリシック、高周波数のPWM DC/DCコンバータとして、6ピンのWSON、8ピンのMSOP- PowerPad™、および5ピンのSOT-23パッケージで供給されます。LM3410およびLM3410-Q1は、最小限の外付け部品だけで簡単に使用できます。内部の170mΩ NMOSスイッチにより、2.8A (標準値)のピーク電流を駆動できます。スイッチング周波数は内部で525kHzまたは1.6MHzに設定されており、超小型の表面実装インダクタとチップ・コンデンサが使用できます。動作周波数が高いにもかかわらず、88%までの高い効率を簡単に実現できます。外部からのシャットダウン機能を備えており、スタンバイ電流が80nAと非常に低くなっています。LM3410およびLM3410-Q1は電流モード制御と内部的な補償によって、広範な動作条件において高い性能を実現します。追加機能として、PWM調光、サイクル単位の電流制限、サーマル・シャットダウンが搭載されています。

製品情報<sup>(1)</sup>

型番	パッケージ	本体サイズ(公称)
LM3410、 LM3410Q	WSON (6)	3.00mmx3.00mm
	MSOP-PowerPAD (8)	2.90mmx1.60mm
	SOT-23 (5)	3.00mmx3.00mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

標準的な効率(LM3410X)



## 目次

<b>1</b>	<b>特長</b> .....	<b>1</b>	<b>8</b>	<b>Application and Implementation</b> .....	<b>11</b>
<b>2</b>	<b>アプリケーション</b> .....	<b>1</b>	8.1	Application Information.....	11
<b>3</b>	<b>概要</b> .....	<b>1</b>	8.2	Typical Applications.....	19
<b>4</b>	<b>改訂履歴</b> .....	<b>2</b>	<b>9</b>	<b>Power Supply Recommendations</b> .....	<b>31</b>
<b>5</b>	<b>Pin Configuration and Functions</b> .....	<b>3</b>	<b>10</b>	<b>Layout</b> .....	<b>32</b>
<b>6</b>	<b>Specifications</b> .....	<b>4</b>	10.1	Layout Guidelines.....	32
6.1	Absolute Maximum Ratings.....	4	10.2	Layout Examples.....	32
6.2	ESD Ratings.....	4	10.3	Thermal Considerations.....	33
6.3	Recommended Operating Conditions.....	4	<b>11</b>	<b>デバイスおよびドキュメントのサポート</b> .....	<b>40</b>
6.4	Thermal Information.....	4	11.1	デバイス・サポート.....	40
6.5	Electrical Characteristics.....	5	11.2	ドキュメントのサポート.....	41
6.6	Typical Characteristics.....	6	11.3	関連リンク.....	41
<b>7</b>	<b>Detailed Description</b> .....	<b>8</b>	11.4	ドキュメントの更新通知を受け取る方法.....	41
7.1	Overview.....	8	11.5	コミュニティ・リソース.....	41
7.2	Functional Block Diagram.....	10	11.6	商標.....	41
7.3	Feature Description.....	10	11.7	静電気放電に関する注意事項.....	41
7.4	Device Functional Modes.....	10	11.8	Glossary.....	41
			<b>12</b>	<b>メカニカル、パッケージ、および注文情報</b> .....	<b>41</b>

## 4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

### Revision G (April 2013) から Revision H に変更

**Page**

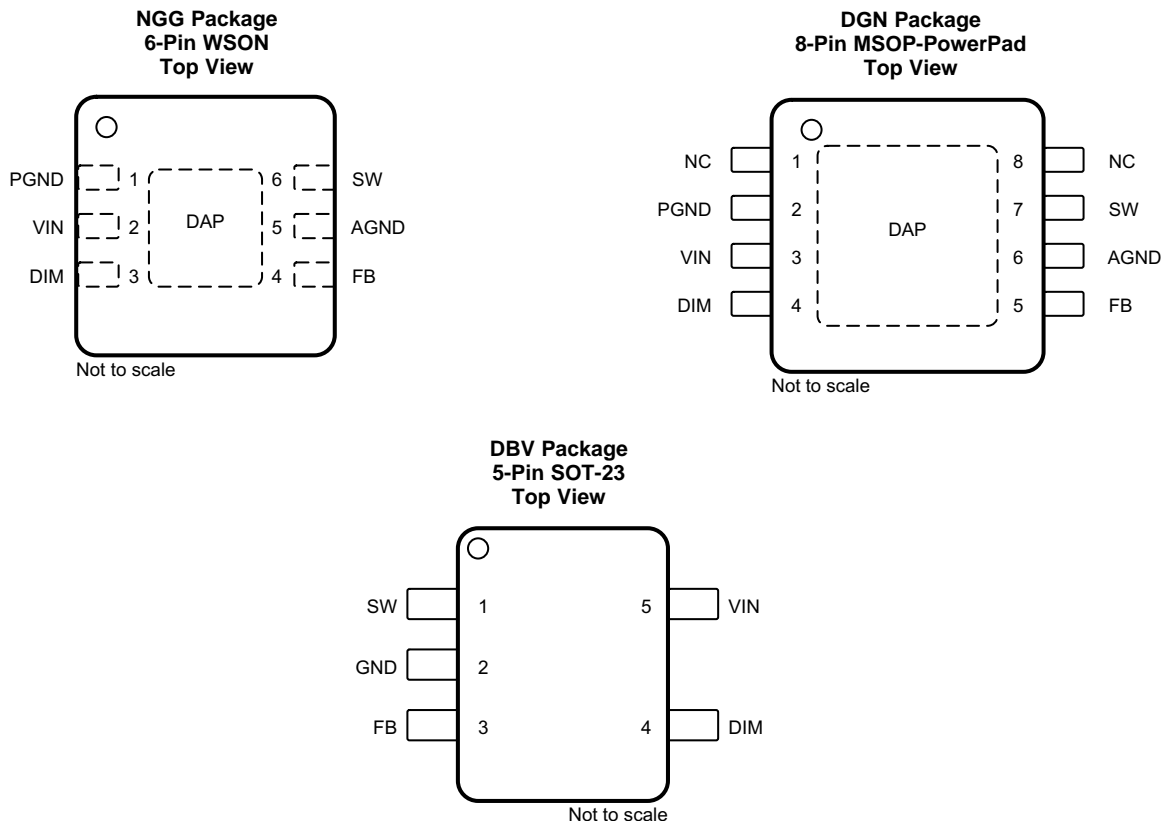
• 「製品情報」表、「ESD定格」表、「熱に関する情報」表、「詳細説明」セクション、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「代表的なアプリケーション」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクション 追加.....	<b>1</b>
• 「特徴」の箇条書きにAEC-Q100試験ガイダンスを追加.....	<b>1</b>
• Changed $R_{\theta JA}$ value for NGG package from 80°C/W : to 55.3°C/W.....	<b>4</b>
• Changed $R_{\theta JA}$ value for DGN package from 80°C/W : to 53.7°C/W.....	<b>4</b>
• Changed $R_{\theta JA}$ value for DBV package from 118°C/W : to 164.2°C/W.....	<b>4</b>
• Changed $R_{\theta JC(top)}$ value for NGG package from 18°C/W : to 65.9°C/W.....	<b>4</b>
• Changed $R_{\theta JC(top)}$ value for DGN package from 18°C/W : to 61.4°C/W.....	<b>4</b>
• Changed $R_{\theta JC(top)}$ value for DBV package from 60°C/W : to 115.3°C/W.....	<b>4</b>

### Revision F (May 2013) から Revision G に変更

**Page**

• ナショナル・セミコンダクターのデータシートのレイアウトをTIフォーマットに変更.....	<b>1</b>
--	----------

## 5 Pin Configuration and Functions



### Pin Functions

NAME	PIN			I/O	DESCRIPTION
	WSON	MSOP-PowerPAD	SOT-23		
AGND	5	6	—	—	Signal ground pin. Place the bottom resistor of the feedback network as close as possible to this pin and FB.
DIM	3	4	4	I	Dimming and shutdown control input. Logic high enables operation. Duty Cycle from 0% to 100%. Do not allow this pin to float or be greater than $V_{IN} + 0.3\text{ V}$ .
FB	4	5	3	I	Feedback pin. Connect FB to external resistor to set output current.
GND	DAP	DAP	—	—	Die attach pad. Signal and Power ground. Connect to PGND and AGND on top layer. Place 4 to 6 vias from DAP to bottom layer GND plane.
	—	—	2	—	Signal and power ground pin. Place the bottom resistor of the feedback network as close as possible to this pin.
NC	—	1, 8	—	—	No connection
PGND	1	2	—	—	Power ground pin. Place PGND and output capacitor GND close together.
SW	6	7	1	O	Output switch. Connect to the inductor, output diode.
VIN	2	3	5	I	Supply voltage pin for power stage, and input supply voltage.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)<sup>(1)(2)</sup>

		MIN	MAX	UNIT
Input voltage	V <sub>IN</sub>	-0.5	7	V
	SW	-0.5	26.5	
	FB	-0.5	3	
	DIM	-0.5	7	
Operating junction temperature <sup>(3)</sup> , T <sub>J</sub>			150	°C
Storage temperature, T <sub>stg</sub>		-65	150	°C

- Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- Thermal shutdown occurs if the junction temperature exceeds the maximum junction temperature of the device.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	

- JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>IN</sub>	Input voltage	2.7	5.5	V
V <sub>DIM</sub>	DIM control input <sup>(1)</sup>	0	V <sub>IN</sub>	V
V <sub>SW</sub>	Switch output	3	24	V
T <sub>J</sub>	Operating junction temperature	-40	125	°C
	Power dissipation (Internal)		400	mW
				SOT-23

- Do not allow this pin to float or be greater than V<sub>IN</sub> + 0.3 V.

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		LM3410, LM3410-Q1			UNIT		
		NGG (WSON)	DGN (MSOP-PowerPAD)	DBV (SOT-23)			
		6 PINS	8 PINS	5 PINS			
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	0 LFPM Air Flow		55.3	53.7	164.2	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	65.9	61.4	115.3	°C/W		
R <sub>θJB</sub>	Junction-to-board thermal resistance	29.6	37.3	27	°C/W		
ψ <sub>JT</sub>	Junction-to-top characterization parameter	1.1	7.1	12.8	°C/W		
ψ <sub>JB</sub>	Junction-to-board characterization parameter	29.7	37	26.5	°C/W		
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	9.3	6.8	—	°C/W		

- For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics

Typical values apply for  $T_J = 25^\circ\text{C}$ ; Minimum and maximum limits apply for  $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$  and  $V_{IN} = 5\text{ V}$  (unless otherwise noted). Typical values represent the most likely parametric norm at  $T_J = 25^\circ\text{C}$ , and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{FB}$	Feedback voltage		178	190	202	mV
$\Delta V_{FB}/V_{IN}$	Feedback voltage line regulation	$V_{IN} = 2.7\text{ V to }5.5\text{ V}$		0.06		%/V
$I_{FB}$	Feedback input bias current			0.1	1	$\mu\text{A}$
$f_{SW}$	Switching frequency	LM3410X	1200	1600	2000	kHz
		LM3410Y	360	525	680	
$D_{MAX}$	Maximum duty cycle	LM3410X	88%	92%		
		LM3410Y	90%	95%		
$D_{MIN}$	Minimum duty cycle	LM3410X		5%		
		LM3410Y		2%		
$R_{DS(ON)}$	Switch on resistance	MSOP and SOT-23		170	330	$\text{m}\Omega$
		WSON		190	350	
$I_{CL}$	Switch current limit		2.1	2.8		A
SU	Start-up time			20		$\mu\text{s}$
$I_Q$	Quiescent current (switching)	LM3410X, $V_{FB} = 0.25\text{ V}$		7	11	mA
		LM3410Y, $V_{FB} = 0.25\text{ V}$		3.4	7	
	Quiescent current (shutdown)	All versions, $V_{DIM} = 0\text{ V}$		80		nA
UVLO	Undervoltage lockout	$V_{IN}$ rising		2.3	2.65	V
		$V_{IN}$ falling	1.7	1.9		
$V_{DIM\_H}$	Shutdown threshold voltage				0.4	V
	Enable threshold voltage		1.8			
$I_{SW}$	Switch leakage	$V_{SW} = 24\text{ V}$		1		$\mu\text{A}$
$I_{DIM}$	Dimming pin current	Sink and source		100		nA
$T_{SD}$	Thermal shutdown temperature <sup>(1)</sup>			165		$^\circ\text{C}$

(1) Thermal shutdown occurs if the junction temperature exceeds the maximum junction temperature of the device.

## 6.6 Typical Characteristics

All curves taken at  $V_{IN} = 5\text{ V}$  with the 50-mA boost configuration shown in Figure 18.  $T_J = 25^\circ\text{C}$ , unless otherwise specified.

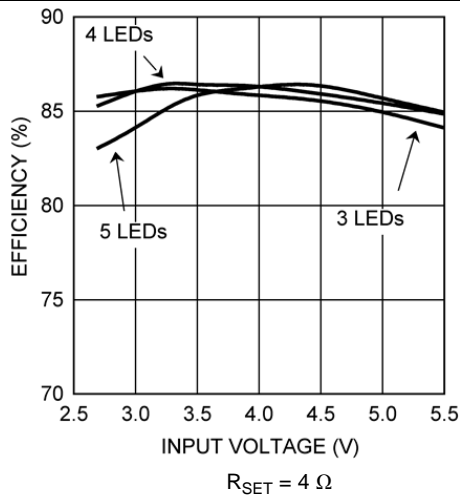


Figure 1. LM3410X Efficiency vs  $V_{IN}$

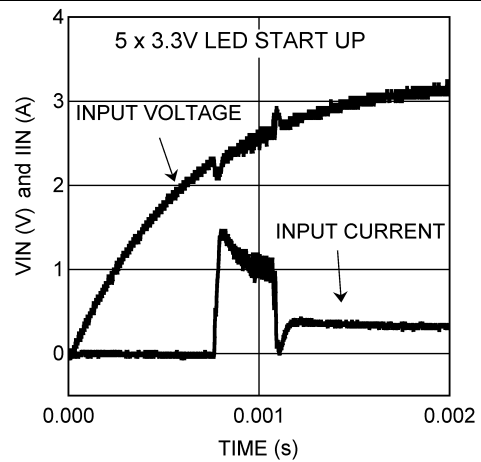


Figure 2. LM3410X Start-Up Signature

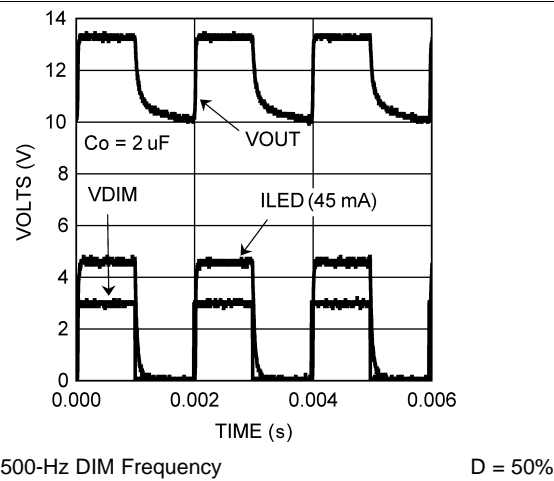


Figure 3. Four 3.3-V LEDs

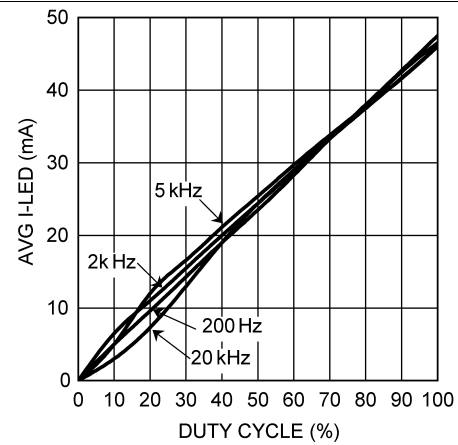


Figure 4. DIM Frequency and Duty Cycle vs Average  $I_{LED}$

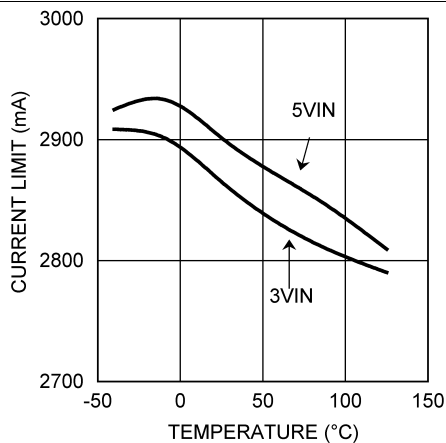


Figure 5. Current Limit vs Temperature

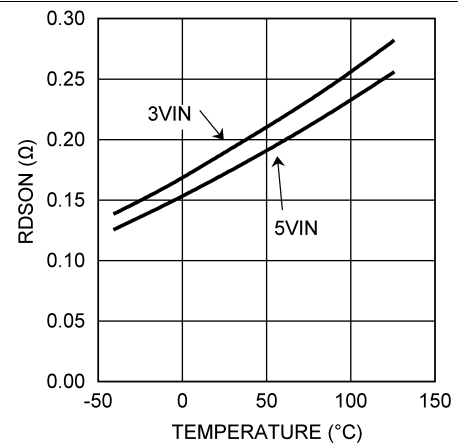
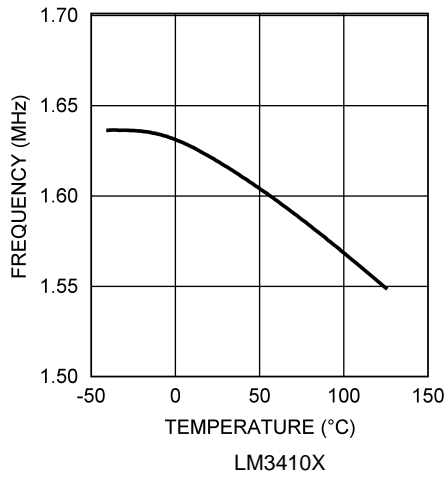


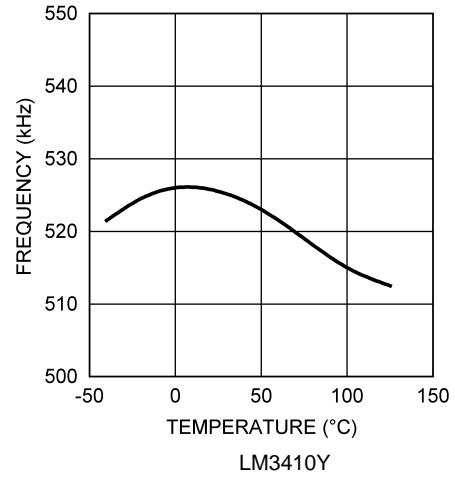
Figure 6.  $R_{DS(ON)}$  vs Temperature

**Typical Characteristics (continued)**

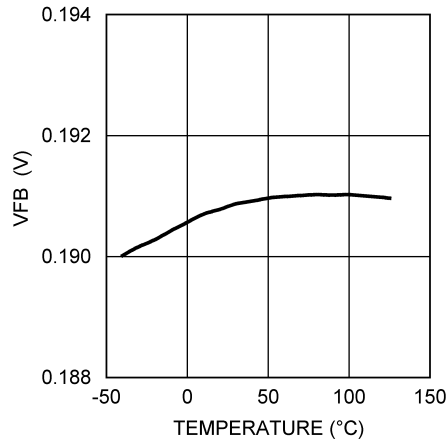
All curves taken at  $V_{IN} = 5\text{ V}$  with the 50-mA boost configuration shown in Figure 18.  $T_J = 25^\circ\text{C}$ , unless otherwise specified.



**Figure 7. Oscillator Frequency vs Temperature**



**Figure 8. Oscillator Frequency vs Temperature**



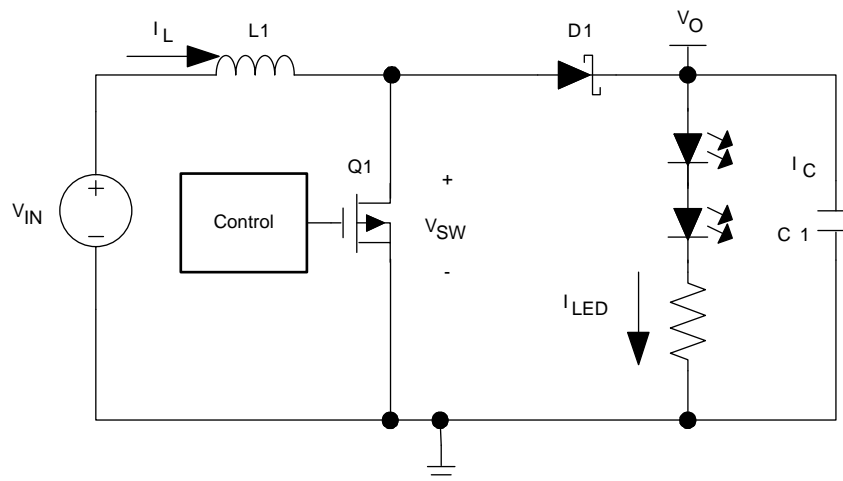
**Figure 9. V<sub>FB</sub> vs Temperature**

## 7 Detailed Description

### 7.1 Overview

The LM3410 and LM3410-Q1 are a constant frequency PWM, boost regulator IC. It delivers a minimum of 2.1-A peak switch current. The device operates very similar to a voltage regulated boost converter except that the device regulates the output current that passes through LEDs. The current magnitude is set with a series resistor. The converter regulates to the feedback voltage (190 mV) created by the multiplication of the series resistor and the LED current. The regulator has a preset switching frequency of either 525 kHz or 1.6 MHz. This high frequency allows the LM3410 or LM3410-Q1 to operate with small surface mount capacitors and inductors, resulting in a DC-DC converter that requires a minimum amount of board space. The LM3410 and LM3410-Q1 are internally compensated and requires few external components, making usage simple. The LM3410 and LM3410-Q1 use current-mode control to regulate the LED current.

The LM3410 and LM3410-Q1 supply a regulated LED current by switching the internal NMOS control switch at constant frequency and variable duty cycle. A switching cycle begins at the falling edge of the reset pulse generated by the internal oscillator. When this pulse goes low, the output control logic turns on the internal NMOS control switch. During this ON time, the SW pin voltage ( $V_{SW}$ ) decreases to approximately GND, and the inductor current ( $I_L$ ) increases with a linear slope.  $I_L$  is measured by the current sense amplifier, which generates an output proportional to the switch current. The sensed signal is summed with the regulator's corrective ramp and compared to the error amplifier's output, which is proportional to the difference between the feedback voltage and reference voltage ( $V_{REF}$ ). When the PWM comparator output goes high, the output switch turns off until the next switching cycle begins. During the switch OFF time, inductor current discharges through diode D1, which forces the SW pin to swing to the output voltage plus the forward voltage ( $V_D$ ) of the diode. The regulator loop adjusts the duty cycle (D) to maintain a regulated LED current.



**Figure 10. Simplified Boost Topology Schematic**



Overview (continued)

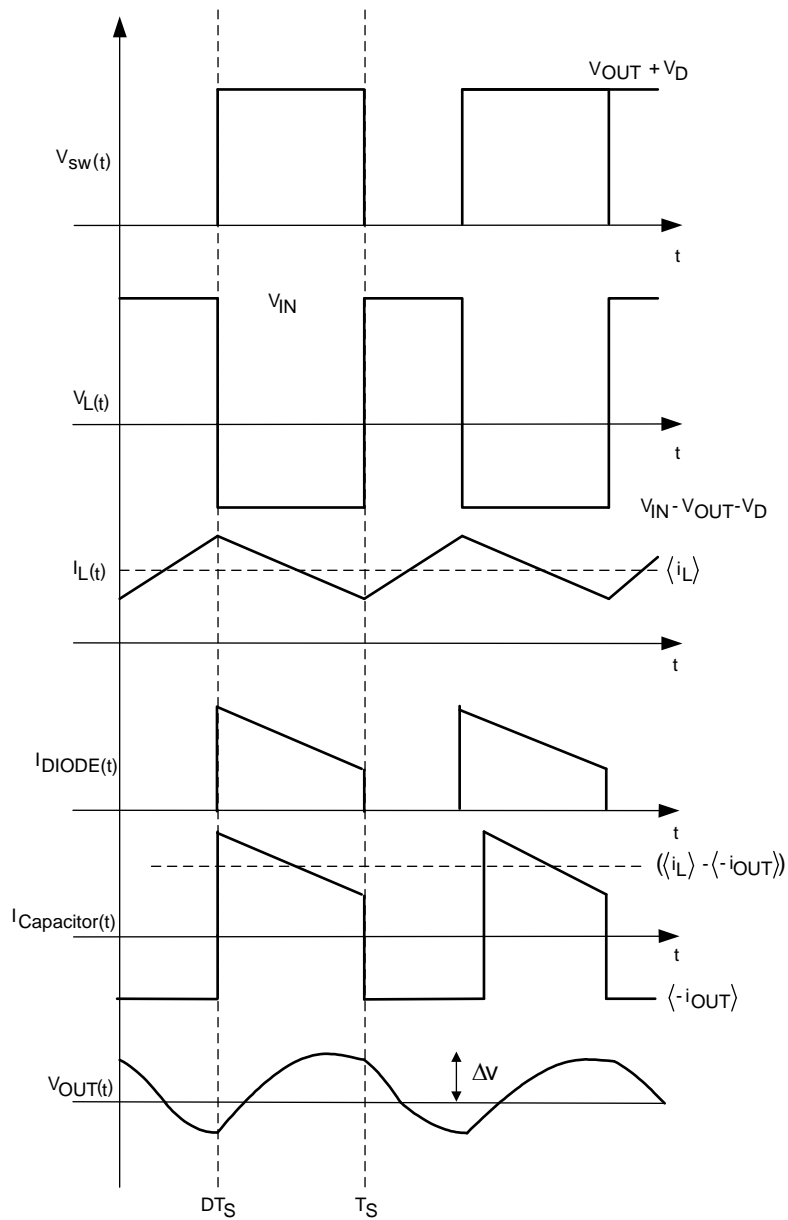
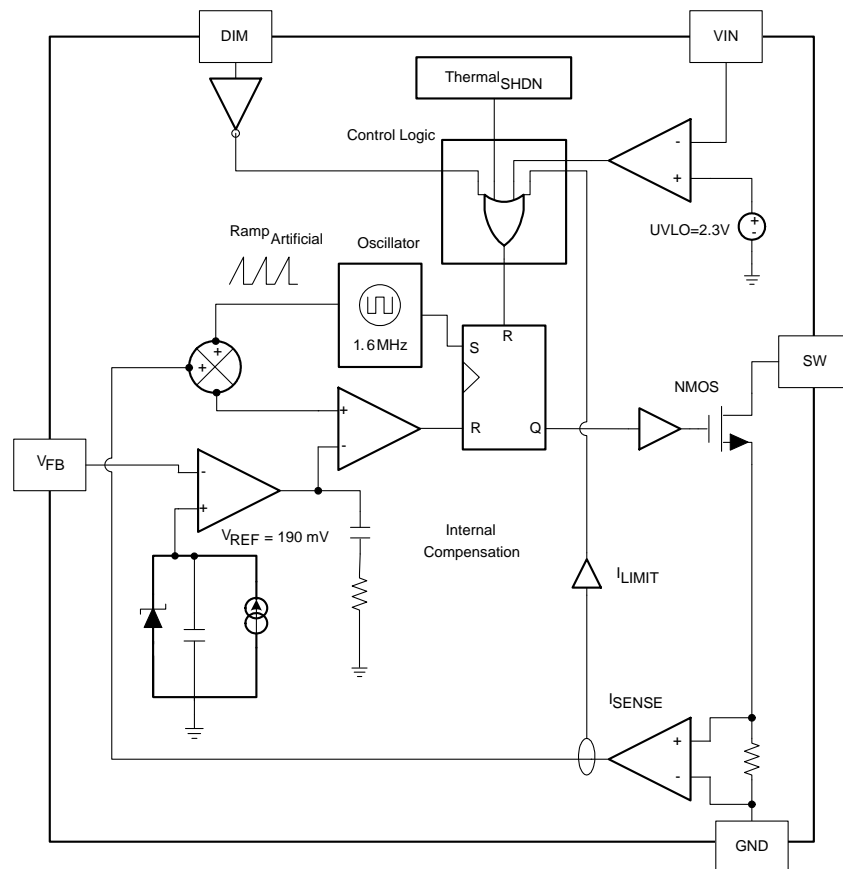


Figure 11. Typical Waveforms

## 7.2 Functional Block Diagram



Copyright © 2016, Texas Instruments Incorporated

## 7.3 Feature Description

### 7.3.1 Current Limit

The LM3410 and LM3410-Q1 use cycle-by-cycle current limiting to protect the internal NMOS switch. This current limit does not protect the output from excessive current during an output short circuit. The input supply is connected to the output by the series connection of an inductor and a diode. If a short circuit is placed on the output, excessive current can damage both the inductor and diode.

### 7.3.2 DIM Pin and Shutdown Mode

The average LED current can be controlled using a PWM signal on the DIM pin. The duty cycle can be varied from 0 to 100%, to either increase or decrease LED brightness. PWM frequencies from 1 Hz to 25 kHz can be used. For controlling LED currents down to the  $\mu\text{A}$  levels, it is best to use a PWM signal frequency from 200 to 1 kHz. The maximum LED current would be achieved using a 100% duty cycle, that is the DIM pin always high.

## 7.4 Device Functional Modes

### 7.4.1 Thermal Shutdown

Thermal shutdown limits total power dissipation by turning off the output switch when the IC junction temperature exceeds 165°C. After thermal shutdown occurs, the output switch does not turn on until the junction temperature drops to approximately 150°C.

## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

#### 8.1.1 Boost Converter

##### 8.1.1.1 Setting the LED Current

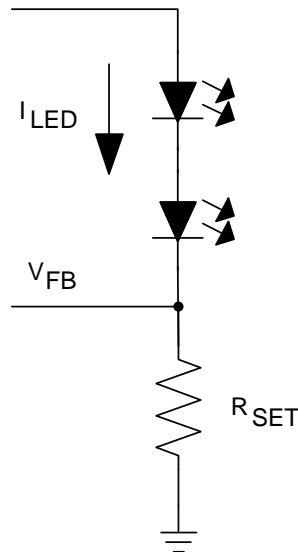


Figure 12. Setting I<sub>LED</sub>

The LED current is set using the following equation:

$$\frac{V_{FB}}{R_{SET}} = I_{LED}$$

where

- R<sub>SET</sub> is connected between the FB pin and GND. (1)

##### 8.1.1.2 LED-Drive Capability

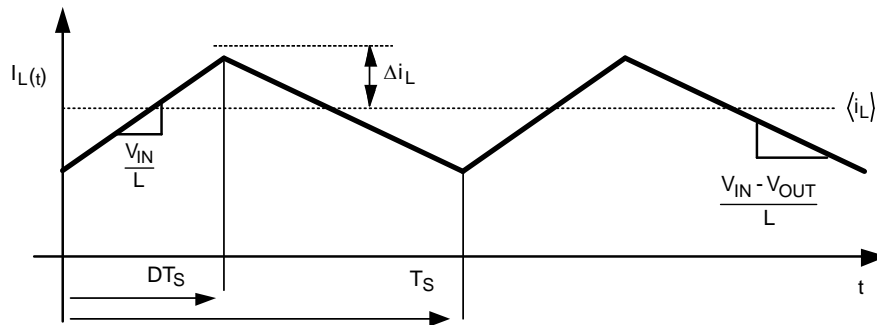
When using the LM3410 or LM3410-Q1 in the typical application configuration, with LEDs stacked in series between the V<sub>OUT</sub> and FB pin, the maximum number of LEDs that can be placed in series is dependent on the maximum LED forward voltage (V<sub>FMAX</sub>).

$$(V_{FMAX} \times N_{LEDS}) + 190 \text{ mV} < 24 \text{ V} \quad (2)$$

When inserting a value for maximum V<sub>FMAX</sub> the LED forward voltage variation over the operating temperature range must be considered.

##### 8.1.1.3 Inductor Selection

The inductor value determines the input ripple current. Lower inductor values decrease the physical size of the inductor, but increase the input ripple current. An increase in the inductor value decreases the input ripple current.

**Application Information (continued)**

**Figure 13. Inductor Current**

$$\frac{2\Delta i_L}{DT_S} = \left( \frac{V_{IN}}{L} \right)$$

$$\Delta i_L = \left( \frac{V_{IN}}{2L} \right) \times DT_S \tag{3}$$

The Duty Cycle (D) for a Boost converter can be approximated by using the ratio of output voltage ( $V_{OUT}$ ) to input voltage ( $V_{IN}$ ).

$$\frac{V_{OUT}}{V_{IN}} = \left( \frac{1}{1 - D} \right) = \frac{1}{D'} \tag{4}$$

Therefore:

$$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \tag{5}$$

Power losses due to the diode (D1) forward voltage drop, the voltage drop across the internal NMOS switch, the voltage drop across the inductor resistance ( $R_{DCR}$ ) and switching losses must be included to calculate a more accurate duty cycle (see [Calculating Efficiency and Junction Temperature](#) for a detailed explanation). A more accurate formula for calculating the conversion ratio is:

$$\frac{V_{OUT}}{V_{IN}} = \frac{\eta}{D'}$$

where

- $\eta$  equals the efficiency of the device application. (6)

Or:

$$\eta = \frac{V_{OUT} \times I_{LED}}{V_{IN} \times I_{IN}} \tag{7}$$

## Application Information (continued)

Therefore:

$$D = \frac{V_{OUT} - \eta V_{IN}}{V_{OUT}} \quad (8)$$

Inductor ripple in a LED driver circuit can be greater than what would normally be allowed in a voltage regulator Boost and Sepic design. A good design practice is to allow the inductor to produce 20% to 50% ripple of maximum load. The increased ripple is unlikely to be a problem when illuminating LEDs.

From the previous equations, the inductor value is then obtained.

$$L = \left( \frac{V_{IN}}{2\Delta I_L} \right) \times DT_S$$

where

- $1 / T_S = f_{SW}$  (9)

Ensure that the minimum current limit (2.1 A) is not exceeded, so the peak current in the inductor must be calculated. The peak current ( $I_{Lpk}$ ) in the inductor is calculated by [Equation 10](#):

$$I_{Lpk} = I_{IN} + \Delta I_L \text{ or } I_{Lpk} = I_{OUT} / D' + \Delta I_L \quad (10)$$

When selecting an inductor, make sure that it is capable of supporting the peak input current without saturating. Inductor saturation results in a sudden reduction in inductance and prevent the regulator from operating correctly. Because of the speed of the internal current limit, the peak current of the inductor only needs to be specified for the required maximum input current. For example, if the designed maximum input current is 1.5 A and the peak current is 1.75 A, then the inductor must be specified with a saturation current limit of >1.75 A. There is no need to specify the saturation or peak current of the inductor at the 2.8-A typical switch current limit.

Because of the operating frequency of the LM3410 and LM3410-Q1, ferrite based inductors are preferred to minimize core losses. This presents little restriction because the variety of ferrite-based inductors is huge. Lastly, inductors with lower series resistance (DCR) provides better operating efficiency. For recommended inductor value examples, see [Typical Applications](#).

### 8.1.1.4 Input Capacitor

An input capacitor is necessary to ensure that  $V_{IN}$  does not drop excessively during switching transients. The primary specifications of the input capacitor are capacitance, voltage, RMS current rating, and ESL (Equivalent Series Inductance). TI recommends an input capacitance from 2.2  $\mu$ F to 22  $\mu$ F depending on the application. The capacitor manufacturer specifically states the input voltage rating. Make sure to check any recommended deratings and also verify if there is any significant change in capacitance at the operating input voltage and the operating temperature. The ESL of an input capacitor is usually determined by the effective cross sectional area of the current path. At the operating frequencies of the LM3410 and LM3410-Q1, certain capacitors may have an ESL so large that the resulting impedance ( $2\pi fL$ ) is higher than that required to provide stable operation. As a result, TI recommends surface mount capacitors. Multilayer ceramic capacitors (MLCC) are good choices for both input and output capacitors and have very low ESL. For MLCCs TI recommends use of X7R or X5R dielectrics. Consult the capacitor manufacturer's datasheet for rated capacitance variation over operating conditions.

### 8.1.1.5 Output Capacitor

The LM3410 and LM3410-Q1 operate at frequencies allowing the use of ceramic output capacitors without compromising transient response. Ceramic capacitors allow higher inductor ripple without significantly increasing output ripple. The output capacitor is selected based upon the desired output ripple and transient response. The initial current of a load transient is provided mainly by the output capacitor. The output impedance therefore determines the maximum voltage perturbation. The output ripple of the converter is a function of the capacitor's reactance and its equivalent series resistance (ESR) (see [Equation 11](#)).

## Application Information (continued)

$$\Delta V_{OUT} = \Delta i_L \times R_{ESR} + \left( \frac{V_{OUT} \times D}{2 \times f_{SW} \times R_{OUT} \times C_{OUT}} \right) \quad (11)$$

When using MLCCs, the ESR is typically so low that the capacitive ripple may dominate. When this occurs, the output ripple is approximately sinusoidal and 90° phase shifted from the switching action.

Given the availability and quality of MLCCs and the expected output voltage of designs using the LM3410 or LM3410-Q1, there no need to review any other capacitor technologies. Another benefit of ceramic capacitors is their ability to bypass high frequency noise. A certain amount of switching edge noise couples through parasitic capacitances in the inductor to the output. A ceramic capacitor bypasses this noise while a tantalum does not. Because the output capacitor is one of the two external components that control the stability of the regulator control loop, most applications requires a minimum at 0.47 μF of output capacitance. Like the input capacitor, TI recommends X7R or X5R as multilayer ceramic capacitors. Again, verify actual capacitance at the desired operating voltage and temperature.

### 8.1.1.6 Diode

The diode (D1) conducts during the switch off time. TI recommends Schottky diode for its fast switching times and low forward voltage drop. The diode must be chosen so that its current rating is greater than:

$$I_{D1} \geq I_{OUT} \quad (12)$$

The reverse breakdown rating of the diode must be at least the maximum output voltage plus appropriate margin.

### 8.1.1.7 Output Overvoltage Protection

A simple circuit consisting of an external Zener diode can be implemented to protect the output and the LM3410 or LM3410-Q1 device from an overvoltage fault condition. If an LED fails open, or is connected backwards, an output open circuit condition occurs. No current is conducted through the LEDs, and the feedback node equals zero volts. The LM3410 or LM3410-Q1 reacts to this fault by increasing the duty cycle, thinking the LED current has dropped. A simple circuit that protects the device is shown in [Figure 14](#).

Zener diode D2 and resistor R3 is placed from  $V_{OUT}$  in parallel with the string of LEDs. If the output voltage exceeds the breakdown voltage of the Zener diode, current is drawn through the Zener diode, R3 and sense resistor R1. Once the voltage across R1 and R3 equals the feedback voltage of 190 mV, the LM3410 and LM3410-Q1 limits their duty cycle. No damage occurs to the device, the LEDs, or the Zener diode. Once the fault is corrected, the application will work as intended.

Application Information (continued)

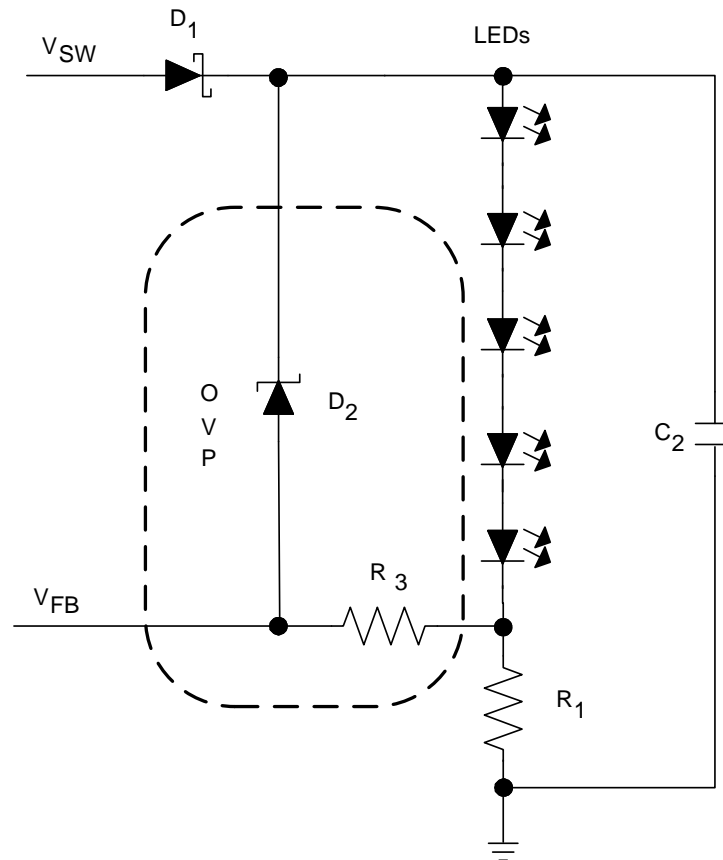
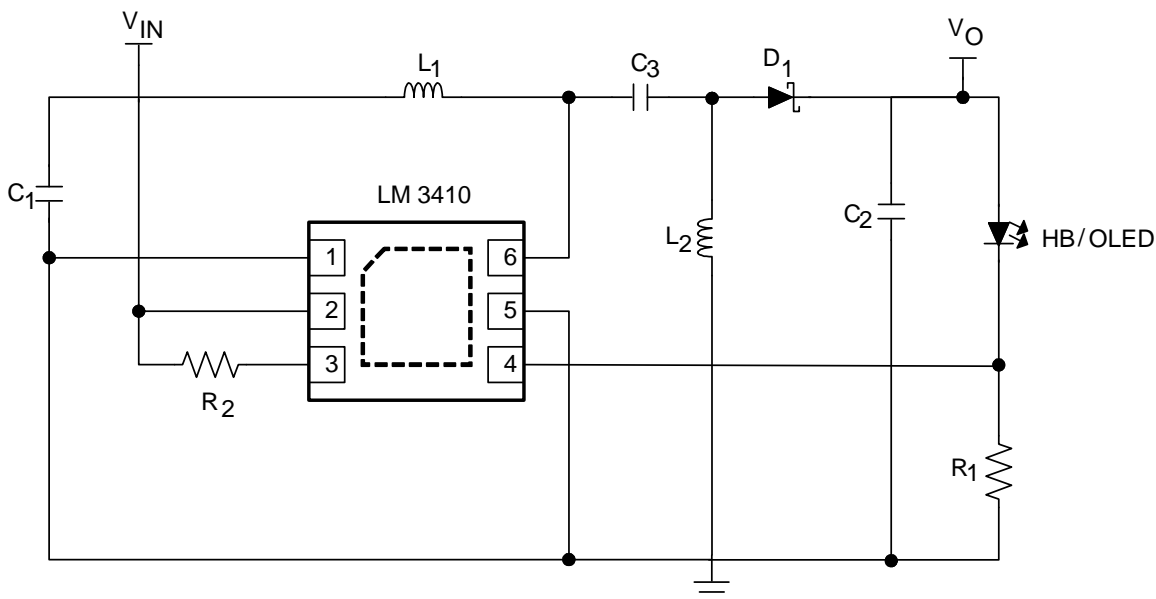


Figure 14. Overvoltage Protection Circuit

8.1.2 SEPIC Converter

The LM3410 or LM3410-Q1 can easily be converted into a SEPIC converter. A SEPIC converter has the ability to regulate an output voltage that is either larger or smaller in magnitude than the input voltage. Other converters have this ability as well (CUK and Buck-Boost), but usually create an output voltage that is opposite in polarity to the input voltage. This topology is a perfect fit for Lithium Ion battery applications where the input voltage for a single cell Li-Ion battery varies from 2.7 V to 4.5 V and the output voltage is somewhere in between. Most of the analysis of the LM3410 Boost Converter is applicable to the LM3410 SEPIC Converter.

**Application Information (continued)**


Copyright © 2016, Texas Instruments Incorporated

**Figure 15. HB or OLED SEPIC Converter Schematic**
**8.1.2.1 SEPIC Equations**

SEPIC Conversion ratio without loss elements:

$$\frac{V_{OUT}}{V_{IN}} = \frac{D}{D'} \quad (13)$$

Therefore:

$$D = \frac{V_{OUT}}{V_{OUT} + V_{IN}} \quad (14)$$

**Small ripple approximation:**

In a well-designed SEPIC converter, the output voltage, and input voltage ripple, the inductor ripple  $I_{L1}$  and  $I_{L2}$  is small in comparison to the DC magnitude. Therefore it is a safe approximation to assume a DC value for these components. The main objective of the Steady State Analysis is to determine the steady state duty cycle, voltage and current stresses on all components, and proper values for all components.

In a steady-state converter, the net volt-seconds across an inductor after one cycle equals zero. Also, the charge into a capacitor equals the charge out of a capacitor in one cycle.

Therefore:

$$I_{L2} = \left(\frac{D'}{D}\right) \times I_{L1}$$

and

$$I_{L2} = \left(\frac{D}{D'}\right) \times I_{LED} \quad (15)$$

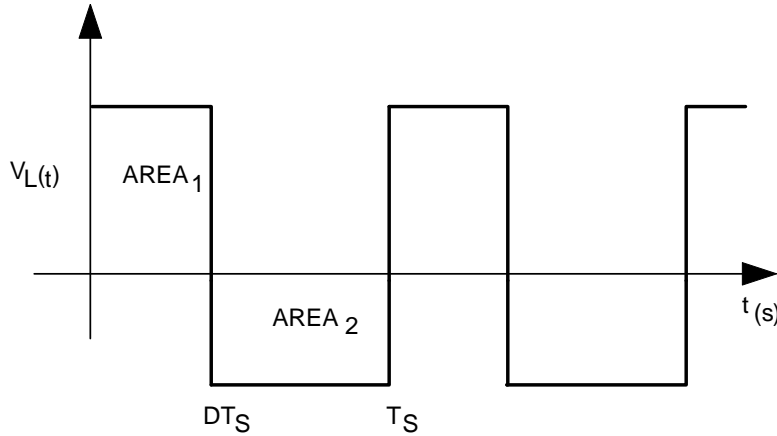


**Application Information (continued)**

Substituting  $I_{L1}$  into  $I_{L2}$

$$I_{L2} = I_{LED} \tag{16}$$

The average inductor current of L2 is the average output load.



**Figure 16. Inductor Volt-Second Balance Waveform**

Applying Charge balance on C1:

$$V_{C3} = \frac{D'(V_{OUT})}{D} \tag{17}$$

Because there are no DC voltages across either inductor, and capacitor C3 is connected to  $V_{IN}$  through L1 at one end, or to ground through L2 on the other end, we can say that

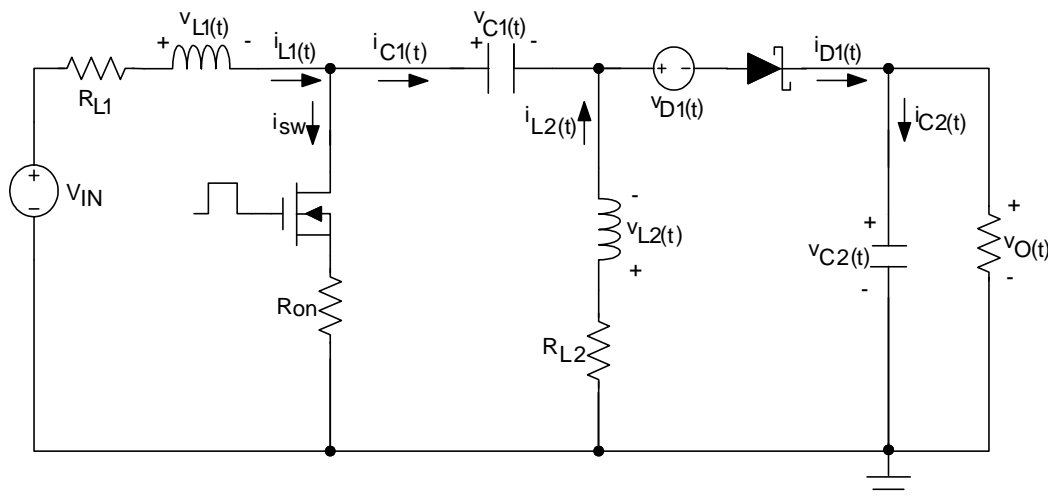
$$V_{C3} = V_{IN} \tag{18}$$

Therefore:

$$V_{IN} = \frac{D'(V_{OUT})}{D} \tag{19}$$

This verifies the original conversion ratio equation.

It is important to remember that the internal switch current is equal to  $I_{L1}$  and  $I_{L2}$  during the D interval. Design the converter so that the minimum ensured peak switch current limit (2.1 A) is not exceeded.

**Application Information (continued)**
**8.1.2.2 Steady State Analysis with Loss Elements**


Copyright © 2016, Texas Instruments Incorporated

**Figure 17. SEPIC Simplified Schematic**
**8.1.2.2.1 Details**

Using inductor volt-second balance and capacitor charge balance, the following equations are derived:

$$I_{L2} = (I_{LED}) \quad (20)$$

and

$$I_{L1} = (I_{LED}) \times (D/D') \quad (21)$$

$$\frac{V_{OUT}}{V_{IN}} = \left( \frac{D}{D'} \right) \left( \frac{1}{\left( 1 + \frac{V_D}{V_{OUT}} + \frac{R_{L2}}{R} \right) + \left( \frac{D}{D'^2} \right) \left( \frac{R_{ON}}{R} \right) + \left( \frac{D^2}{D'^2} \right) \left( \frac{R_{L1}}{R} \right)} \right) \quad (22)$$

$$R_{OUT} = \frac{V_{OUT}}{I_{LED}} \quad (23)$$

Therefore:

$$\eta = \left( \frac{1}{\left( 1 + \frac{V_D}{V_{OUT}} + \frac{R_{L2}}{R_{OUT}} \right) + \left( \frac{D}{D'^2} \right) \left( \frac{R_{ON}}{R_{OUT}} \right) + \left( \frac{D^2}{D'^2} \right) \left( \frac{R_{L1}}{R_{OUT}} \right)} \right) \quad (24)$$

All variables are known except for the duty cycle (D). A quadratic equation is needed to solve for D. A less accurate method of determining the duty cycle is to assume efficiency, and calculate the duty cycle.

$$\frac{V_{OUT}}{V_{IN}} = \left( \frac{D}{1 - D} \right) \times \eta \quad (25)$$

## Application Information (continued)

$$D = \left( \frac{V_{OUT}}{(V_{IN} \times \eta) + V_{OUT}} \right)$$

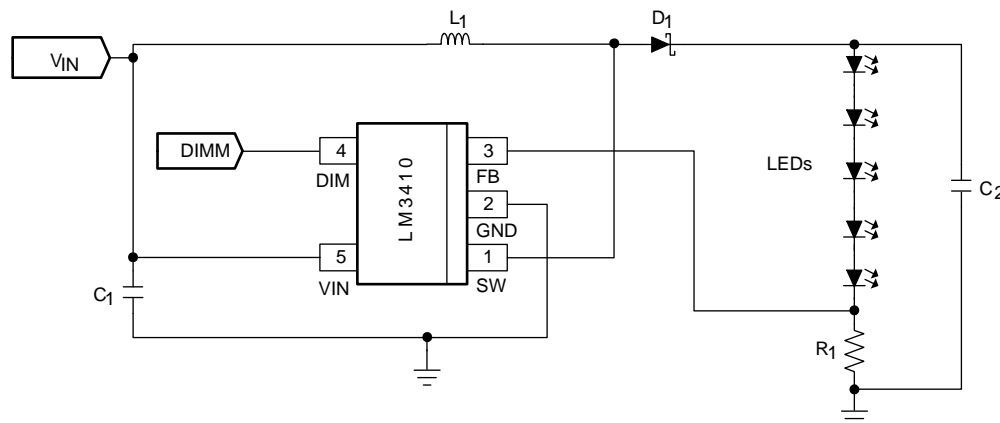
(26)

Table 1. Efficiencies for Typical SEPIC Applications

EXAMPLE 1		EXAMPLE 2		EXAMPLE 3	
V <sub>IN</sub>	2.7 V	V <sub>IN</sub>	3.3 V	V <sub>IN</sub>	5 V
V <sub>OUT</sub>	3.1 V	V <sub>OUT</sub>	3.1 V	V <sub>OUT</sub>	3.1 V
I <sub>IN</sub>	770 mA	I <sub>IN</sub>	600 mA	I <sub>IN</sub>	375 mA
I <sub>LED</sub>	500 mA	I <sub>LED</sub>	500 mA	I <sub>LED</sub>	500 mA
η	75%	η	80%	η	83%

## 8.2 Typical Applications

### 8.2.1 Low Input Voltage, 1.6-MHz, 3 to 5 White LED Output at 50-mA Boost Converter



Copyright © 2016, Texas Instruments Incorporated

Figure 18. Boost Schematic

#### 8.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 2 as the input parameters.

Table 2. Design Parameters

PARAMETER	EXAMPLE VALUE
V <sub>IN</sub>	2.7 V to 5.5 V
I <sub>LED</sub>	50 mA
V <sub>OUT</sub>	14.6 V (four 3.6-V LEDs in series plus 190 mV)
R <sub>D</sub>	8 Ω (dynamic resistance of 4 LEDs in series)
ΔI <sub>LP-P</sub>	100 mA (maximum)
ΔV <sub>OUTP-P</sub>	250 mV (maximum)

#### 8.2.1.2 Detailed Design Procedure

This design procedure uses the worst-case minimum input voltage and a nominal 4 LED series load for calculations.

##### 8.2.1.2.1 Set the LED Current (R<sub>1</sub>)

Rearranging the LED current equation the current sense resistor R<sub>1</sub> can be found using Equation 27.

$$R_1 = \frac{V_{FB}}{I_{LED}} = \frac{190\text{mV}}{50\text{mA}} = 3.8\Omega \quad (27)$$

3.8  $\Omega$  is not a standard value so a standard value of  $R_1 = 3.83 \Omega$  is chosen.

#### 8.2.1.2.2 Calculate Maximum Duty Cycle ( $D_{MAX}$ )

The maximum duty cycle is required for calculating the inductor value and the minimum output capacitance. Assuming an approximate conversion efficiency ( $\eta$ ) of 90%  $D_{MAX}$  is calculated using Equation 28.

$$D_{MAX} = \frac{V_{OUT} - \eta \times V_{IN(min)}}{V_{OUT}} = \frac{14.6\text{V} - 0.9 \times 2.7\text{V}}{14.6\text{V}} = 0.834 \quad (28)$$

#### 8.2.1.2.3 Calculate the Inductor Value ( $L_1$ )

Using the maximum duty cycle, the minimum input voltage, and the maximum inductor ripple current ( $\Delta i_{L-P}$ ) the minimum inductor value to achieve the maximum ripple current is calculated using Equation 29.

$$L_1 = \left( \frac{V_{IN(min)} \times D_{MAX} \times T_S}{2 \times \Delta i_{L-PP}} \right) = \left( \frac{2.7\text{V} \times 0.834 \times 625\text{ns}}{2 \times 100\text{mA}} \right) = 7.04\mu\text{H} \quad (29)$$

To ensure the maximum inductor ripple current requirement is met with a 20% inductor tolerance an inductor value of  $L_1 = 10 \mu\text{H}$  is selected.

#### 8.2.1.2.4 Calculate the Output Capacitor ( $C_2$ )

To maintain a maximum of 250-mV output voltage ripple the dynamic resistance of the LED stack ( $R_D$ ) must be used. Assuming a ceramic capacitor is used so the ESR can be neglected this minimum amount of capacitance can be found using Equation 30.

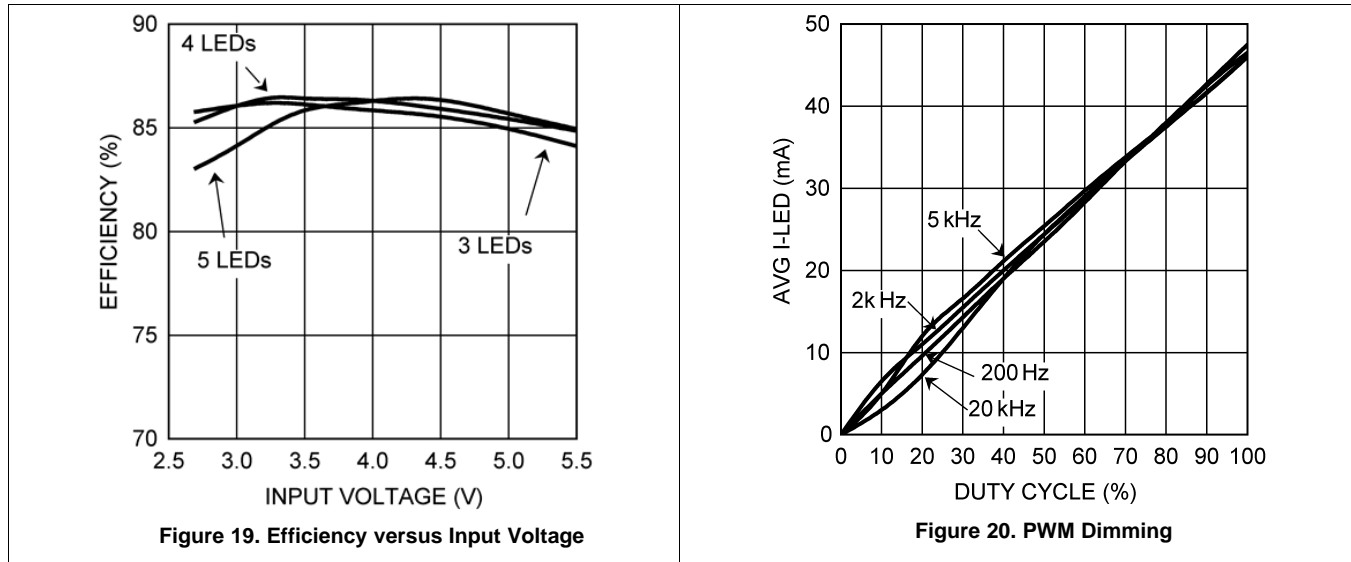
$$C_2 \geq \frac{V_{OUT} \times D_{MAX}}{2 \times f_{SW} \times R_D \times V_{OUT}} = \frac{14.6\text{V} \times 0.834}{2 \times 1.6\text{MHz} \times 8\Omega \times 14.6\text{V}} = 1.9\mu\text{F} \quad (30)$$

1.9  $\mu\text{F}$  is not a standard value so a value of  $C_2 = 2.2 \mu\text{F}$  is selected.

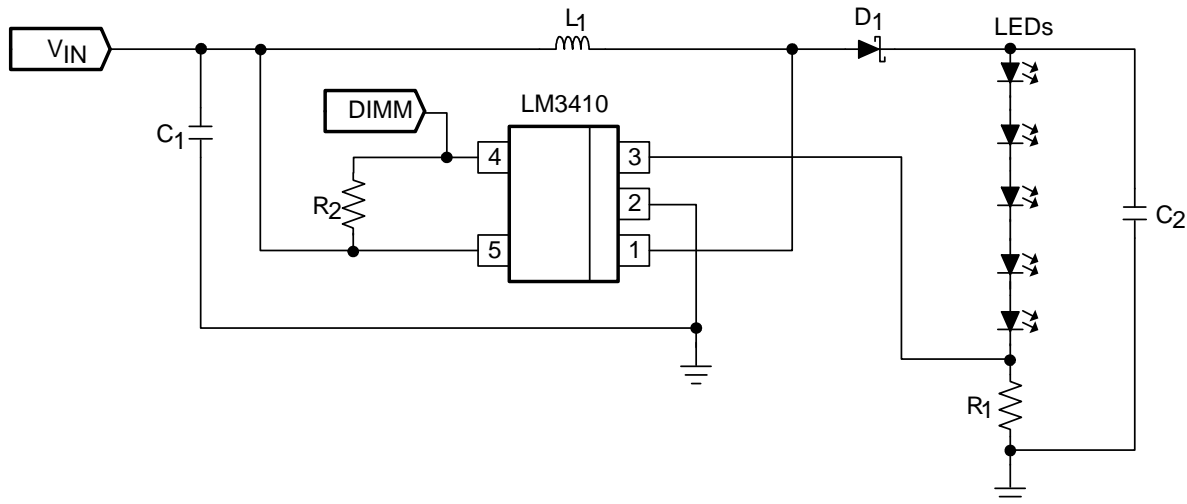
#### 8.2.1.2.5 Input Capacitor ( $C_1$ ) and Schottky Diode ( $D_1$ )

TI recommends an input capacitor from 2.2  $\mu\text{F}$  to 22  $\mu\text{F}$ . This is a relatively low power design optimized for a small footprint. For a good balance of input filtering and small size a 6.3-V capacitor with a value of  $C_1 = 10 \mu\text{F}$  is selected. The output voltage with a 5 LED load is over 18 V and the reverse voltage of the schottky diode must be greater than this voltage. To give some headroom to avoid reverse breakdown and to maintain small size and reliability the diode selected is  $D_1 = 30 \text{ V}, 500 \text{ mA}$ .

### 8.2.1.3 Application Curves



### 8.2.2 LM3410X SOT-23: 5 × 1206 Series LED String Application



Copyright © 2016, Texas Instruments Incorporated

**Figure 21. LM3410X (1.6 MHz) 5 × 3.3-V LED String Application Diagram**

#### 8.2.2.1 Design Requirements

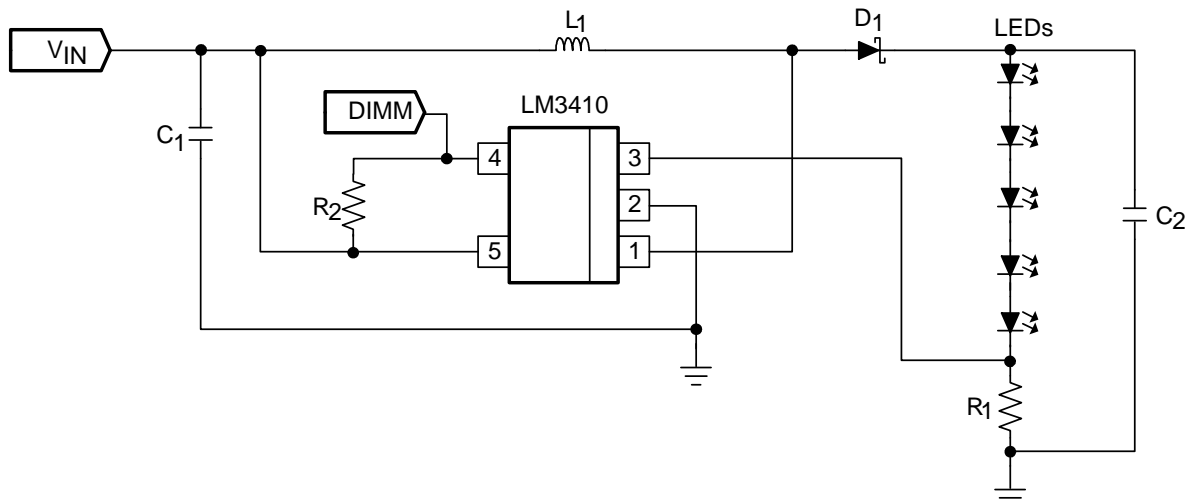
For this design example, use the parameters listed in [Table 3](#) as the input parameters.

**Table 3. Design Parameters**

PARAMETER	EXAMPLE VALUE
$V_{IN}$	2.7 V to 5.5 V
$I_{LED}$	≈50 mA
$V_{OUT}$	≈16.5 V (five 3.3-V LEDs in series)

**Table 4. Part Values**

PART	VALUE
U1	2.8-A $I_{SW}$ LED Driver
C1, Input capacitor	10 $\mu$ F, 6.3 V, X5R
C2, Output capacitor	2.2 $\mu$ F, 25 V, X5R
D1, Catch diode	0.4- $V_f$ Schottky 500 mA, 30 $V_R$
L1	10 $\mu$ H, 1.2 A
R1	4.02 $\Omega$ , 1%
R2	100 k $\Omega$ , 1%
LEDs	SMD-1206, 50 mA, $V_f \approx 3.6$ V

**8.2.3 LM3410Y SOT-23: 5 × 1206 Series LED String Application**


Copyright © 2016, Texas Instruments Incorporated

**Figure 22. LM3410Y (525 kHz) 5 × 3.3-V LED String Application Diagram**
**8.2.3.1 Design Requirements**

 For this design example, use the parameters listed in [Table 5](#) as the input parameters.

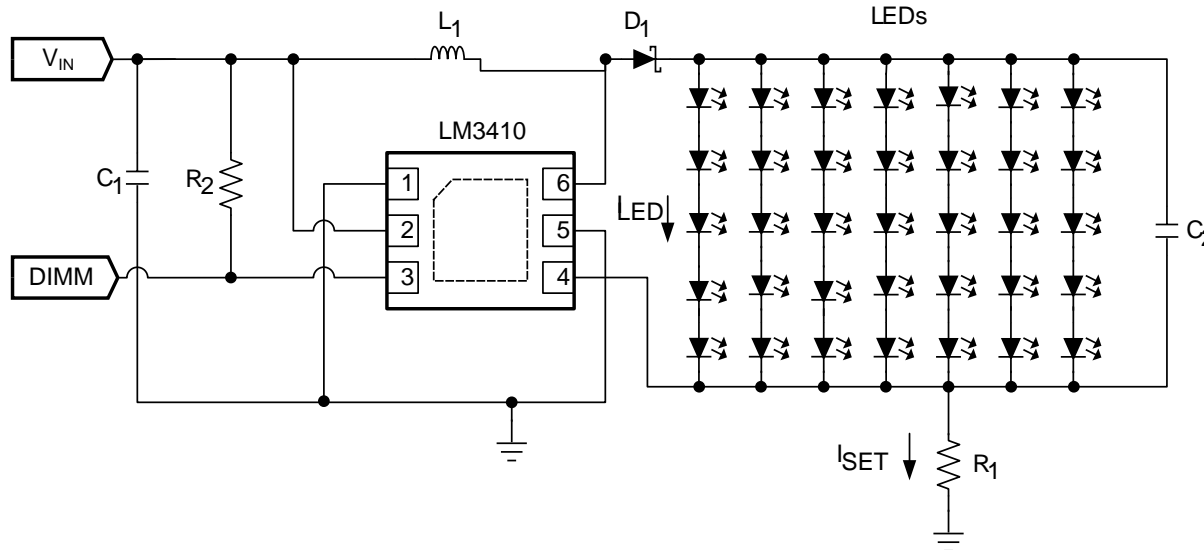
**Table 5. Design Parameters**

PARAMETER	EXAMPLE VALUE
$V_{IN}$	2.7 V to 5.5 V
$I_{LED}$	$\approx 50$ mA
$V_{OUT}$	$\approx 16.5$ V (five 3.3-V LEDs in series)

**Table 6. Part Values**

PART	VALUE
U1	2.8-A $I_{SW}$ LED Driver
C1, Input capacitor	10 $\mu$ F, 6.3 V, X5R
C2, Output capacitor	2.2 $\mu$ F, 25 V, X5R
D1, Catch diode	0.4- $V_f$ Schottky 500 mA, 30 $V_R$
L1	15 $\mu$ H, 1.2 A
R1	4.02 $\Omega$ , 1%
R2	100 k $\Omega$ , 1%
LEDs	SMD-1206, 50 mA, $V_f \approx 3.6$ V

### 8.2.4 LM3410X WSON: 7 × 5 LED Strings Backlighting Application



Copyright © 2016, Texas Instruments Incorporated

Figure 23. LM3410X (1.6 MHz) 7 × 5 × 3.3-V LEDs Backlighting Application Diagram

#### 8.2.4.1 Design Requirements

For this design example, use the parameters listed in Table 7 as the input parameters.

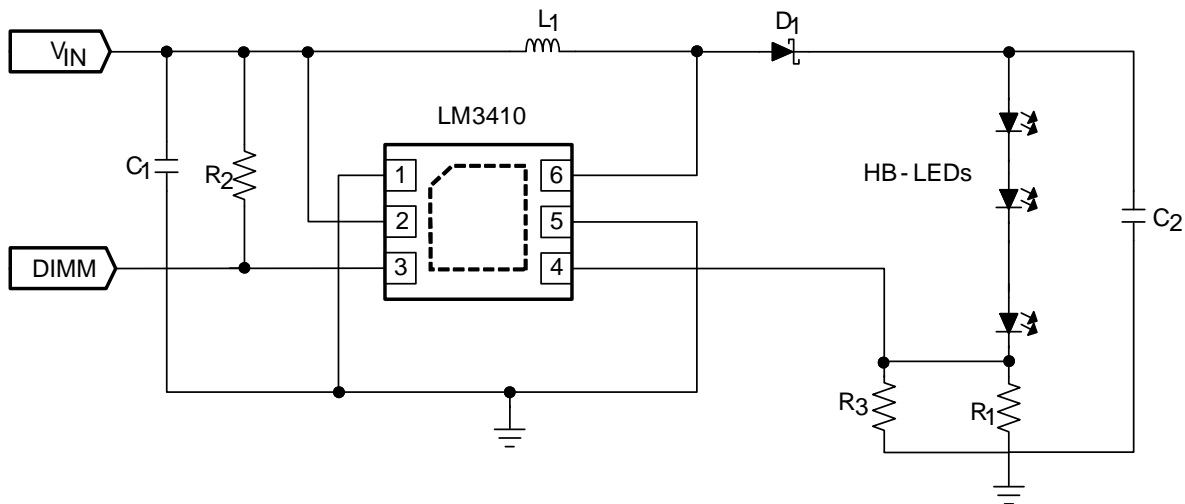
Table 7. Design Parameters

PARAMETER	EXAMPLE VALUE
$V_{IN}$	2.7 V to 5.5 V
$I_{LED}$	≈25 mA
$V_{OUT}$	≈16.7 V (seven strings of five 3.3-V LEDs in series)

Table 8. Part Values

PART	VALUE
U1	2.8-A $I_{SW}$ LED Driver
C1, Input capacitor	10 $\mu$ F, 6.3 V, X5R
C2, Output capacitor	4.7 $\mu$ F, 25 V, X5R
D1, Catch Diode	0.4- $V_f$ Schottky 500 mA, 30 $V_R$
L1	8.2 $\mu$ H, 2 A
R1	1.15 $\Omega$ , 1%
R2	100 k $\Omega$ , 1%
LEDs	SMD-1206, 50 mA, $V_f$ ≈ 3.6 V

## 8.2.5 LM3410X WSON: 3 × HB LED String Application



Copyright © 2016, Texas Instruments Incorporated

**Figure 24. LM3410X (1.6 MHz) 3 × 3.4-V LED String Application Diagram**

### 8.2.5.1 Design Requirements

For this design example, use the parameters listed in [Table 9](#) as the input parameters.

**Table 9. Design Parameters**

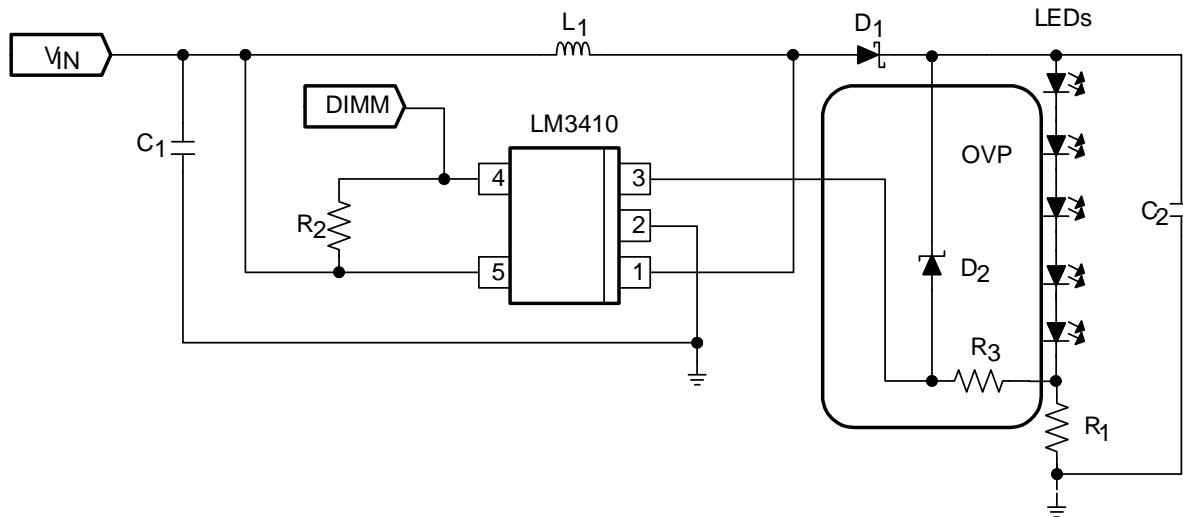
PARAMETER	EXAMPLE VALUE
$V_{IN}$	2.7 V to 5.5 V
$I_{LED}$	≈340 mA
$V_{OUT}$	≈11 V (three 3.4-V LEDs in series)

**Table 10. Part Values**

PART	VALUE
U1	2.8-A $I_{SW}$ LED Driver
C1, Input capacitor	10 $\mu$ F, 6.3 V, X5R
C2, Output capacitor	2.2 $\mu$ F, 25 V, X5R
D1, Catch diode	0.4- $V_f$ Schottky 500 mA, 30 $V_R$
L1	10 $\mu$ H, 1.2 A
R1	1 $\Omega$ , 1%
R2	100 k $\Omega$ , 1%
R3	1.5 $\Omega$ , 1%
HB – LEDs	340 mA, $V_f$ ≈ 3.6 V



### 8.2.6 LM3410Y SOT-23: 5 × 1206 Series LED String Application With OVP



Copyright © 2016, Texas Instruments Incorporated

Figure 25. LM3410Y (525 kHz) 5 × 3.3-V LED String Application With OVP Diagram

#### 8.2.6.1 Design Requirements

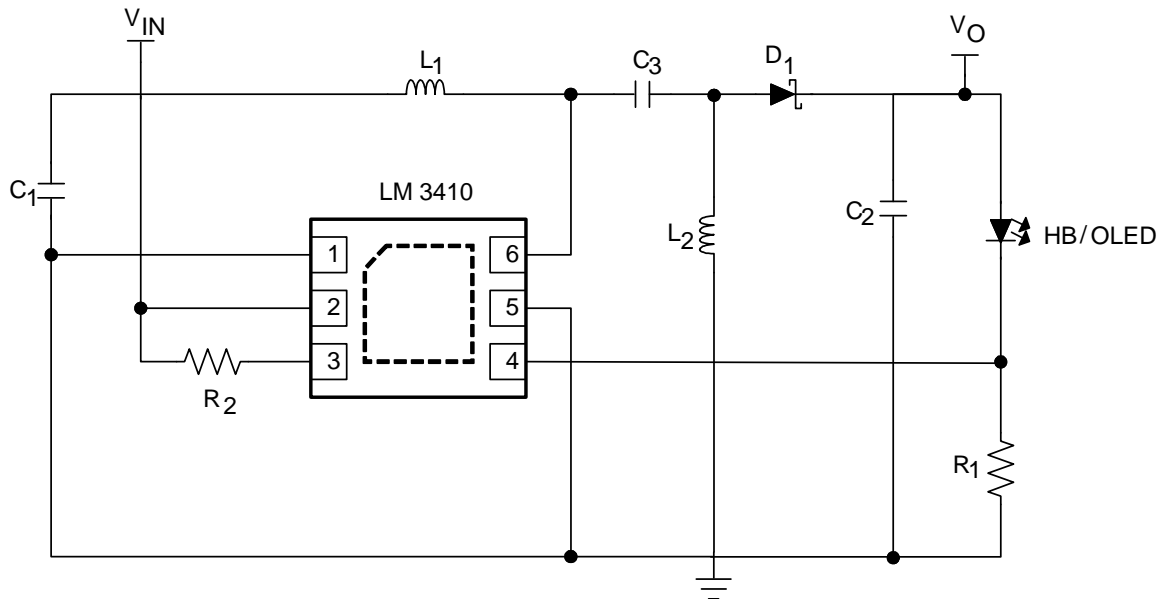
For this design example, use the parameters listed in Table 11 as the input parameters.

Table 11. Design Parameters

PARAMETER	EXAMPLE VALUE
$V_{IN}$	2.7 V to 5.5 V
$I_{LED}$	≈50 mA
$V_{OUT}$	≈16.5 V (five 3.3-V LEDs in series)

Table 12. Part Values

PART	VALUE
U1	2.8-A $I_{SW}$ LED Driver
C1, Input capacitor	10 $\mu$ F, 6.3 V, X5R
C2, Output capacitor	2.2 $\mu$ F, 25 V, X5R
D1, Catch diode	0.4- $V_f$ Schottky 500 mA, 30 $V_R$
D2	18 V Zener diode
L1	15 $\mu$ H, 0.7 A
R1	4.02 $\Omega$ , 1%
R2	100 k $\Omega$ , 1%
R3	100 $\Omega$ , 1%
LEDs	SMD-1206, 50 mA, $V_f$ ≈ 3.6 V

**8.2.7 LM3410X SEPIC WSON: HB or OLED Illumination Application**


Copyright © 2016, Texas Instruments Incorporated

**Figure 26. LM3410X (1.6 MHz) HB or OLED Illumination Application Diagram**
**8.2.7.1 Design Requirements**

 For this design example, use the parameters listed in [Table 13](#) as the input parameters.

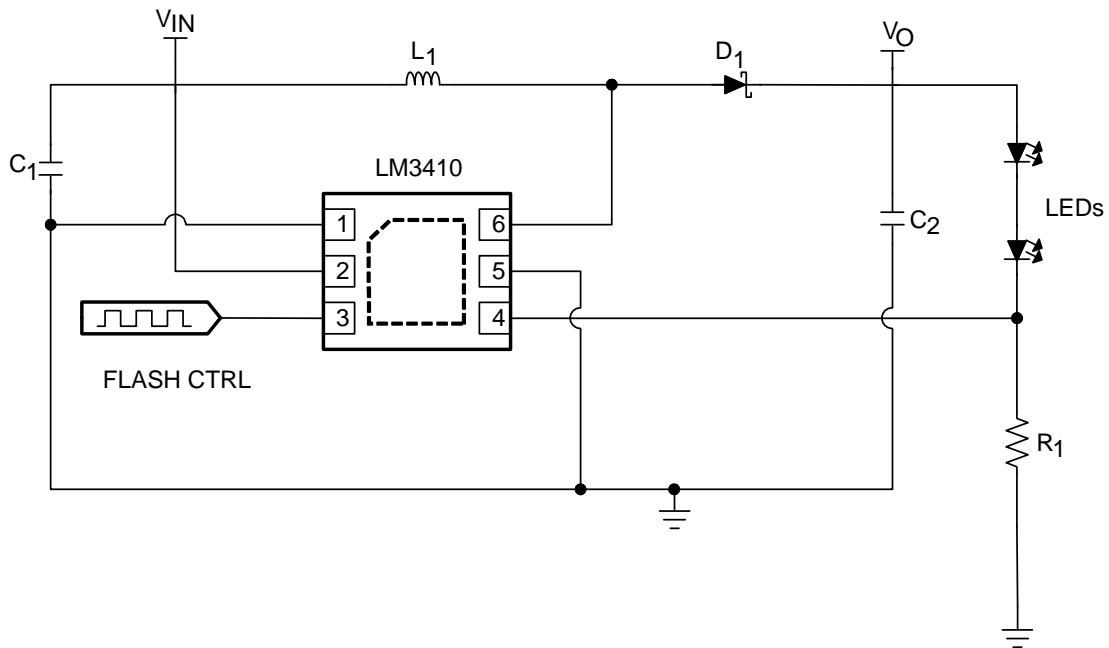
**Table 13. Design Parameters**

PARAMETER	EXAMPLE VALUE
$V_{IN}$	2.7 V to 5.5 V
$I_{LED}$	≈300 mA
$V_{OUT}$	≈3.8 V

**Table 14. Part Values**

PART	VALUE
U1	2.8-A $I_{SW}$ LED Driver
C1, Input capacitor	10 $\mu$ F, 6.3 V, X5R
C2, Output capacitor	10 $\mu$ F, 6.3 V, X5R
C3	2.2 $\mu$ F, 25 V, X5R
D1, Catch diode	0.4- $V_f$ Schottky 1 A, 20 $V_R$
L1 and L2	4.7 $\mu$ H, 3 A
R1	665 m $\Omega$ , 1%
R2	100 k $\Omega$ , 1%
HB – LEDs	350 mA, $V_f \approx 3.6$ V

### 8.2.8 LM3410X WSON: Boost Flash Application



Copyright © 2016, Texas Instruments Incorporated

Figure 27. LM3410X (1.6 MHz) Boost Flash Application Diagram

#### 8.2.8.1 Design Requirements

For this design example, use the parameters listed in Table 15 as the input parameters.

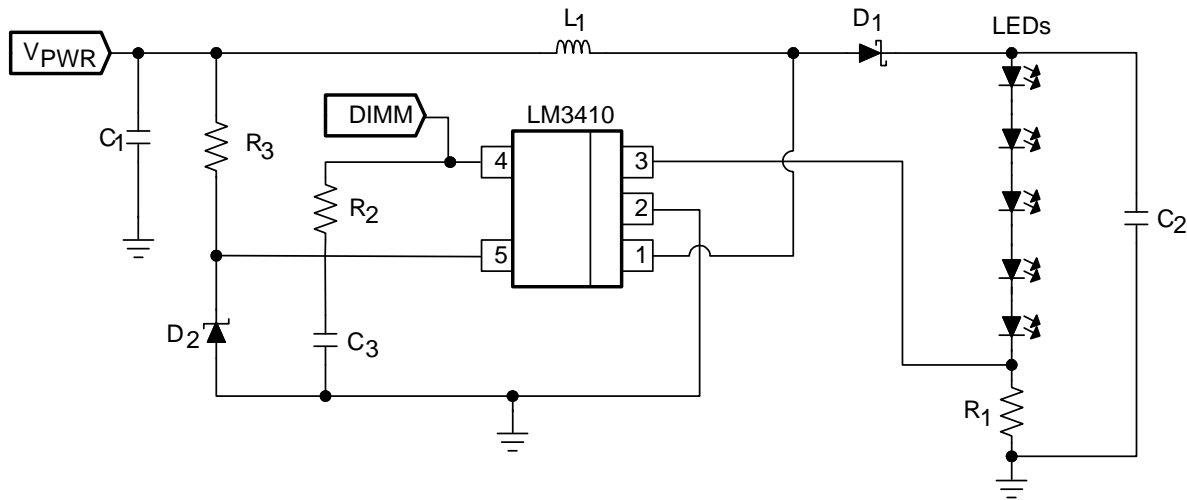
Table 15. Design Parameters

PARAMETER	EXAMPLE VALUE
$V_{IN}$	2.7 V to 5.5 V
$I_{LED}$	$\approx 1$ A (pulse)
$V_{OUT}$	$\approx 8$ V

Table 16. Part Values

PART	VALUE
U1	2.8-A $I_{SW}$ LED Driver
C1, Input capacitor	10 $\mu$ F, 6.3 V, X5R
C2, Output capacitor	10 $\mu$ F, 16 V, X5R
D1, Catch diode	0.4- $V_f$ Schottky 500 mA, 30 $V_R$
L1	4.7 $\mu$ H, 3 A
R1	200 m $\Omega$ , 1%
LEDs	500 mA, $V_f \approx 3.6$ V, $I_{PULSE} = 1$ A

8.2.9 LM3410X SOT-23: 5 × 1206 Series LED String Application With  $V_{IN} > 5.5\text{ V}$



Copyright © 2016, Texas Instruments Incorporated

Figure 28. LM3410X (1.6 MHz) 5 × 1206 Series LED String Application With  $V_{IN} > 5.5\text{ V}$  Diagram

8.2.9.1 Design Requirements

For this design example, use the parameters listed in Table 17 as the input parameters.

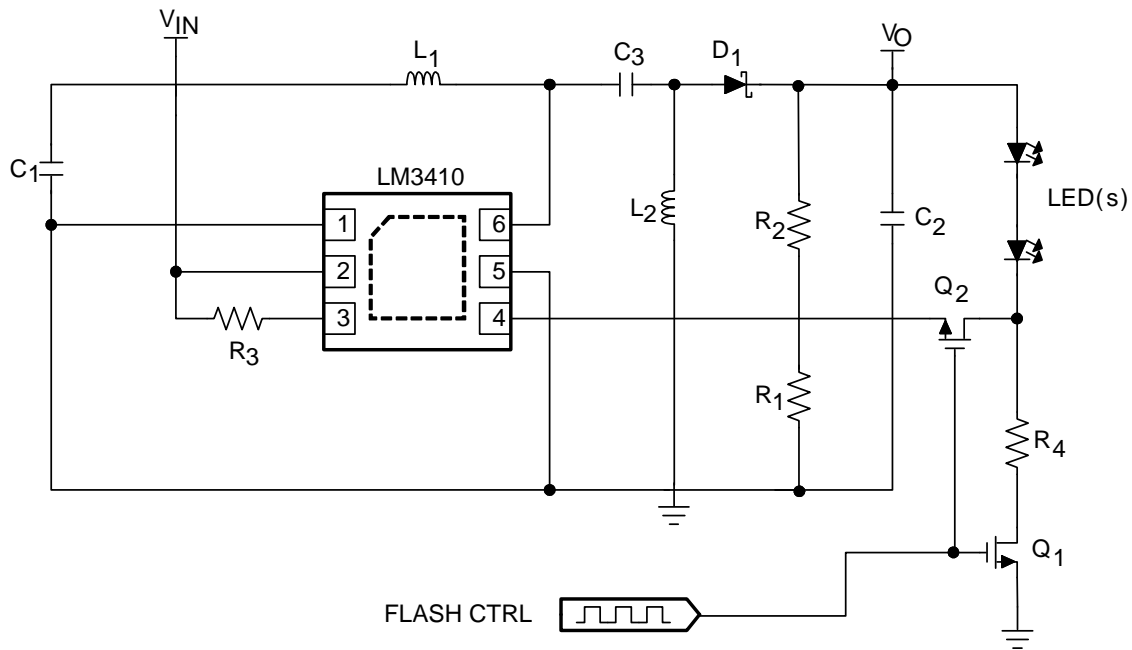
Table 17. Design Parameters

PARAMETER	EXAMPLE VALUE
$V_{PWR}$	9 V to 14 V
$I_{LED}$	≈50 mA
$V_{OUT}$	≈16.5 V (five 3.3-V LEDs in series)

Table 18. Part Values

PART	VALUE
U1	2.8-A $I_{SW}$ LED Driver
C1, Input $V_{PWR}$ capacitor	10 $\mu\text{F}$ , 6.3 V, X5R
C2, Output capacitor	2.2 $\mu\text{F}$ , 25 V, X5R
C3, Input $V_{IN}$ capacitor	0.1 $\mu\text{F}$ , 6.3 V, X5R
D1, Catch diode	0.43- $V_f$ Schottky 500 mA, 30 $V_R$
D2	3.3 V Zener, SOT-23
L1	10 $\mu\text{H}$ , 1.2 A
R1	4.02 $\Omega$ , 1%
R2	100 k $\Omega$ , 1%
R3	576 $\Omega$ , 1%
LEDs	SMD-1206, 50 mA, $V_f \approx 3.6\text{ V}$

8.2.10 LM3410X WSON: Camera Flash or Strobe Circuit Application



Copyright © 2016, Texas Instruments Incorporated

Figure 29. LM3410X (1.6 MHz) Camera Flash or Strobe Circuit Application Diagram

8.2.10.1 Design Requirements

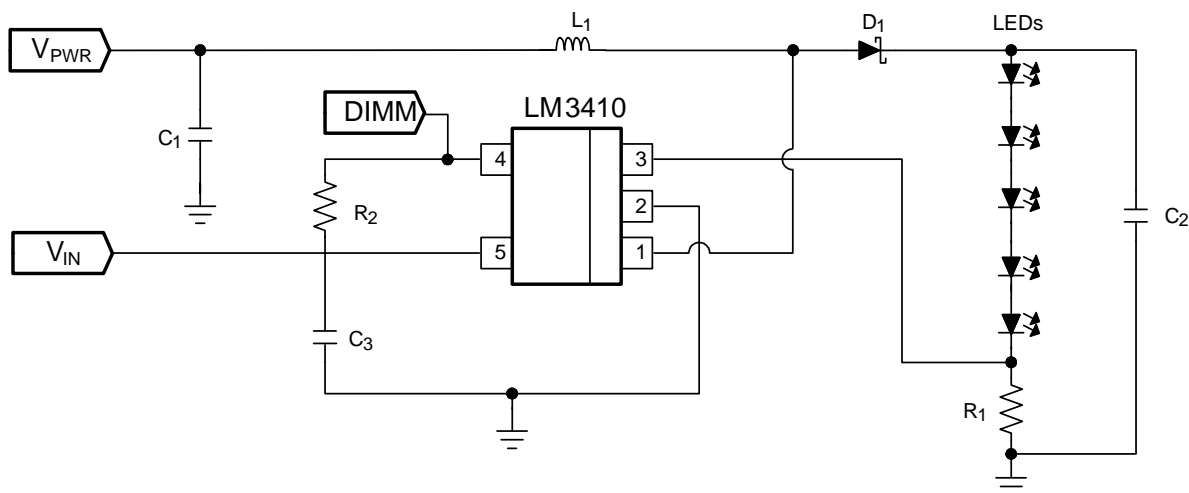
For this design example, use the parameters listed in Table 19 as the input parameters.

Table 19. Design Parameters

PARAMETER	EXAMPLE VALUE
$V_{IN}$	2.7 V to 5.5 V
$I_{LED}$	≈1.5 A (flash)
$V_{OUT}$	≈7.5 V

Table 20. Part Values

PART	VALUE
U1	2.8-A $I_{SW}$ LED Driver
C1, Input capacitor	10 $\mu$ F, 6.3 V, X5R
C2, Output capacitor	220 $\mu$ F, 10 V, tantalum
C3 capacitor	10 $\mu$ F, 16 V, X5R
D1, Catch diode	0.43- $V_f$ Schottky 1 A, 20 $V_R$
L1	3.3 $\mu$ H, 2.7 A
R1	1 $\Omega$ , 1%
R2	37.4 k $\Omega$ , 1%
R3	100 k $\Omega$ , 1%
R4	0.15 $\Omega$ , 1%
Q1 and Q2	30 V, $I_D = 3.9$ A
LEDs	SMD-1206, 50 mA, $V_f \approx 3.6$ V, $I_{PULSE} = 1.5$ A

**8.2.11 LM3410X SOT-23: 5 × 1206 Series LED String Application With  $V_{IN}$  and  $V_{PWR}$  Rail > 5.5 V**


Copyright © 2016, Texas Instruments Incorporated

**Figure 30. LM3410X (1.6 MHz) 5 × 1206 Series LED String Application With  $V_{IN}$  and  $V_{PWR}$  Rail > 5.5 V Diagram**
**8.2.11.1 Design Requirements**

 For this design example, use the parameters listed in [Table 21](#) as the input parameters.

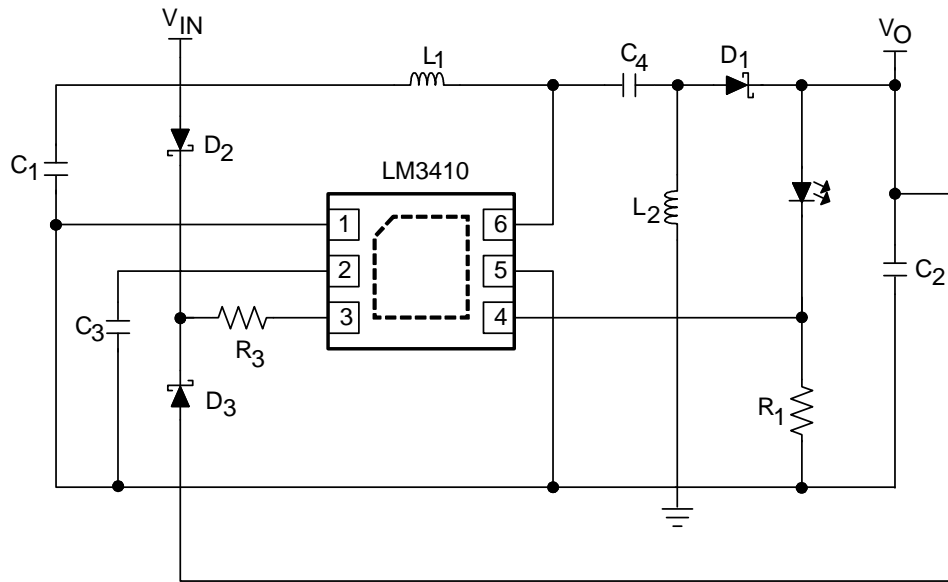
**Table 21. Design Parameters**

PARAMETER	EXAMPLE VALUE
$V_{PWR}$	9 V to 14 V
$V_{IN}$	2.7 V to 5.5 V
$I_{LED}$	≈50 mA
$V_{OUT}$	≈16.5 V (five 3.3-V LEDs in series)

**Table 22. Part Values**

PART	VALUE
U1	2.8-A $I_{SW}$ LED Driver
C1, Input $V_{PWR}$ capacitor	10 $\mu$ F, 6.3 V, X5R
C2, Output capacitor	2.2 $\mu$ F, 25 V, X5R
C3, Input $V_{IN}$ capacitor	0.1 $\mu$ F, 6.3 V, X5R
D1, Catch diode	0.43- $V_f$ Schottky 500 mA, 30 $V_R$
L1	10 $\mu$ H, 1.2 A
R1	4.02 $\Omega$ , 1%
R2	100 k $\Omega$ , 1%
LEDs	SMD-1206, 50 mA, $V_f$ ≈ 3.6 V

### 8.2.12 LM3410X WSON: Boot-Strap Circuit to Extend Battery Life



Copyright © 2016, Texas Instruments Incorporated

Figure 31. LM3410X (1.6 MHz) Boot-Strap Circuit to Extend Battery Life

#### 8.2.12.1 Design Requirements

For this design example, use the parameters listed in Table 3 as the input parameters.

Table 23. Design Parameters

PARAMETER	EXAMPLE VALUE
$V_{IN}$	1.9 V to 5.5 V
	>2.3 V (typical) for start-up
$I_{LED}$	≈300 mA

Table 24. Part Values

PART	VALUE
U1	2.8-A $I_{SW}$ LED Driver
C1, Input $V_{PWR}$ capacitor	10 $\mu$ F, 6.3 V, X5R
C2, Output capacitor	10 $\mu$ F, 6.3 V, X5R
C3, Input $V_{IN}$ capacitor	0.1 $\mu$ F, 6.3 V, X5R
D1, Catch diode	0.43- $V_f$ Schottky 1 A, 20 $V_R$
D2 and D3	Dual small signal Schottky
L1 and L2	3.3 $\mu$ H, 3 A
R1	665 m $\Omega$ , 1%
R3	100 k $\Omega$ , 1%
HB – LEDs	350 mA, $V_f \approx 3.4$ V

## 9 Power Supply Recommendations

Any DC output power supply may be used provided it has a high enough voltage and current range for the particular application required.

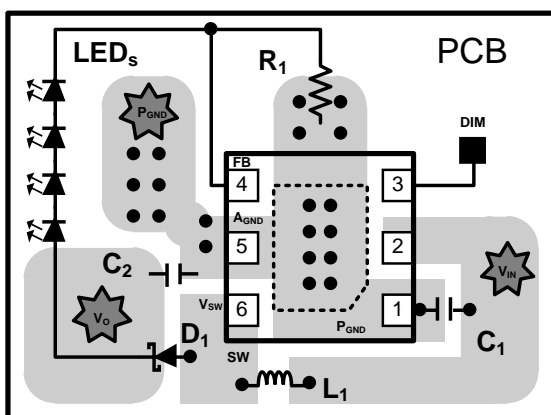
## 10 Layout

### 10.1 Layout Guidelines

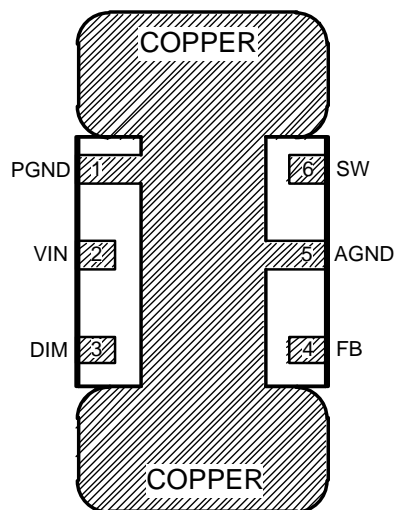
When planning layout there are a few things to consider when trying to achieve a clean, regulated output. The most important consideration when completing a boost converter layout is the close coupling of the GND connections of the  $C_{OUT}$  capacitor and the PGND pin. The GND ends must be close to one another and be connected to the GND plane with at least two vias. There must be a continuous ground plane on the bottom layer of a two-layer board except under the switching node island. The FB pin is a high impedance node and the FB trace must be kept short to avoid noise pickup and inaccurate regulation. The  $R_{SET}$  feedback resistor must be placed as close as possible to the IC, with the AGND of  $R_{SET}$  (R1) placed as close as possible to the AGND of the IC. Radiated noise can be decreased by choosing a shielded inductor. The remaining components must also be placed as close as possible to the IC. See [AN-1229 SIMPLE SWITCHER® PCB Layout Guidelines](#) (SNVA054) for further considerations and the LM3410 demo board as an example of a four-layer layout.

For certain high power applications, the PCB land may be modified to a *dog bone* shape (see [Figure 33](#)). Increasing the size of ground plane and adding thermal vias can reduce the  $R_{\theta JA}$  for the application.

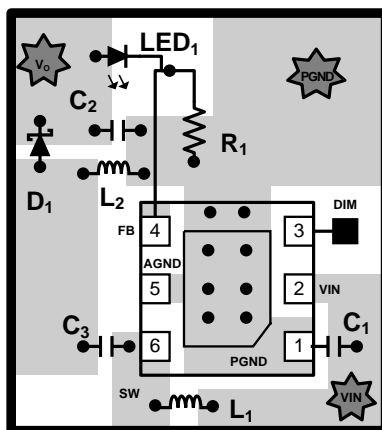
### 10.2 Layout Examples



**Figure 32. Boost PCB Layout Guidelines**



**Figure 33. PCB Dog Bone Layout**



The layout guidelines described for the LM3410 boost-converter are applicable to the SEPIC OLED Converter. This is a proper PCB layout for a SEPIC Converter.

**Figure 34. HB or OLED SEPIC PCB Layout**



## 10.3 Thermal Considerations

### 10.3.1 Design

When designing for thermal performance, many variables must be considered, such as ambient temperature, airflow, external components, and PCB design.

The surrounding maximum air temperature is fairly explanatory. As the temperature increases, the junction temperature increases. This may not be linear though. As the surrounding air temperature increases, resistances of semiconductors, wires and traces increase. This decreases the efficiency of the application, and more power is converted into heat, and increases the silicon junction temperatures further.

Forced air can drastically reduce the device junction temperature. Air flow reduces the hot spots within a design. Warm airflow is often much better than a lower ambient temperature with no airflow.

Choose components that are efficient, and the mutual heating between devices can be reduced.

The PCB design is a very important step in the thermal design procedure. The LM3410 and LM3410-Q1 are available in three package options (6-pin WSON, 8-pin MSOP, and 5-pin SOT-23). The options are electrically the same, but there are differences between the package sizes and thermal performances. The WSON and MSOP have thermal die attach pads (DAP) attached to the bottom of the packages, and are therefore capable of dissipating more heat than the SOT-23 package. It is important that the customer choose the correct package for the application. A detailed thermal design procedure has been included in this data sheet. This procedure helps determine which package is correct, and common applications are analyzed.

There is one significant thermal PCB layout design consideration that contradicts a proper electrical PCB layout design consideration. This contradiction is the placement of external components that dissipate heat. The greatest external heat contributor is the external Schottky diode. Increasing the distance between the LM3410 or LM3410-Q1 and the Schottky diode may reduce the mutual heating effect. This, however, creates electrical performance issues. It is important to keep the device, the output capacitor, and Schottky diode physically close to each other (see [Layout Guidelines](#)). The electrical design considerations outweigh the thermal considerations. Other factors that influence thermal performance are thermal vias, copper weight, and number of board layers.

Heat energy is transferred from regions of high temperature to regions of low temperature via three basic mechanisms: radiation, conduction and convection. *Conduction* and *convection* are the dominant heat transfer mechanism in most applications.

The data sheet values for each packages thermal impedances are given to allow comparison of the thermal performance of one package against another. To achieve a comparison between packages, all other variables must be held constant in the comparison (PCB size, copper weight, thermal vias, power dissipation,  $V_{IN}$ ,  $V_{OUT}$ , load current, and others). This provides indication of package performance, but it would be a mistake to use these values to calculate the actual junction temperature in an application.

### 10.3.2 LM3410 and LM3410-Q1 Thermal Models

Heat is dissipated from the LM3410, LM3410-Q1, and other devices. The external loss elements include the Schottky diode, inductor, and loads. All loss elements mutually increase the heat on the PCB, and therefore increase each other's temperatures.

Thermal Considerations (continued)

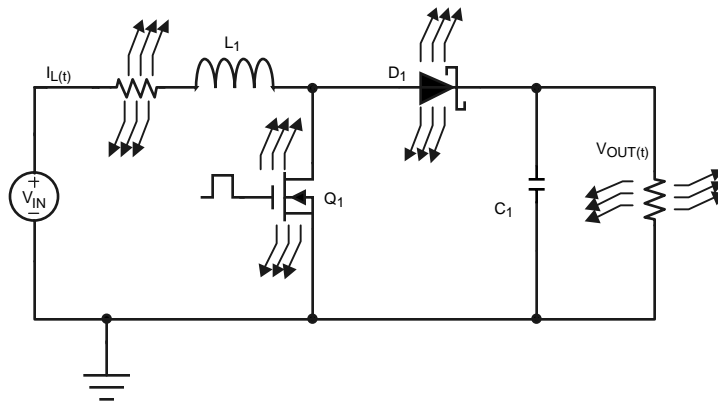


Figure 35. Thermal Schematic

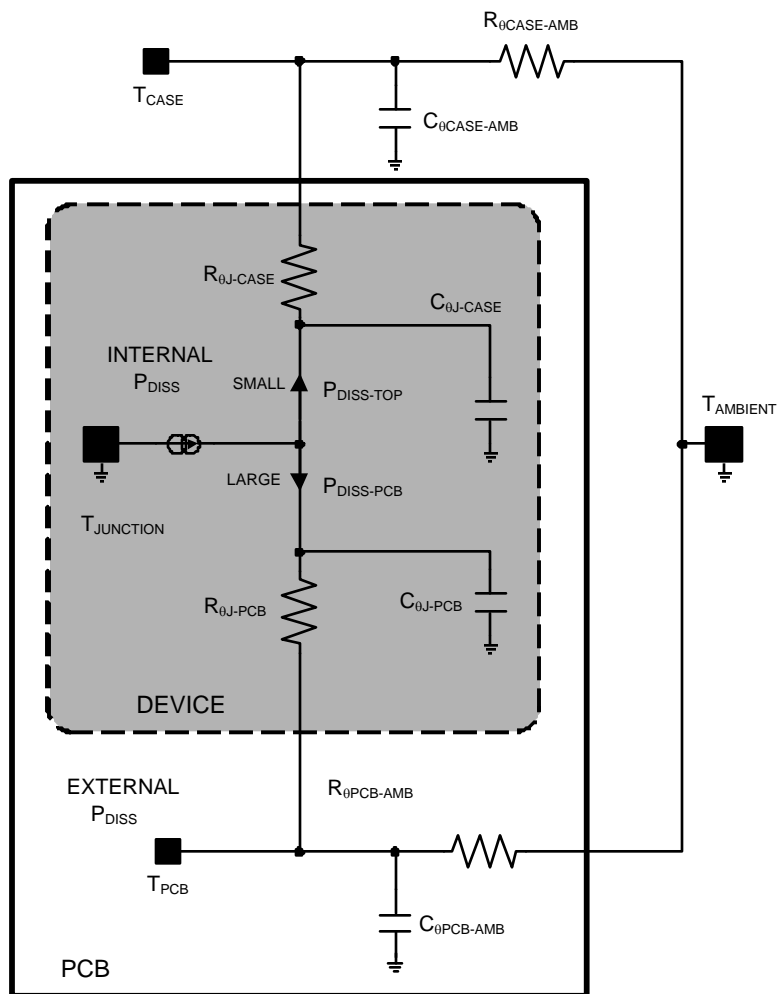


Figure 36. Associated Thermal Model

## Thermal Considerations (continued)

### 10.3.3 Calculating Efficiency and Junction Temperature

Use [Equation 31](#) to calculate  $R_{\theta JA}$ .

$$R_{\theta JA} = \frac{T_J - T_A}{P_{\text{Dissipation}}} \quad (31)$$

A common error when calculating  $R_{\theta JA}$  is to assume that the package is the only variable to consider.

Other variables are:

- Input voltage, output voltage, output current,  $R_{DS(ON)}$
- Ambient temperature and air flow
- Internal and external components' power dissipation
- Package thermal limitations
- PCB variables (copper weight, thermal vias, and component placement)

Another common error when calculating junction temperature is to assume that the top case temperature is the proper temperature when calculating  $R_{\theta JC}$ .  $R_{\theta JC}$  represents the thermal impedance of all six sides of a package, not just the top side. This document refers to a thermal impedance called  $R_{\psi JC}$ .  $R_{\psi JC}$  represents a thermal impedance associated with just the top case temperature. This allows for the calculation of the junction temperature with a thermal sensor connected to the top case.

The complete LM3410 and LM3410-Q1 boost converter efficiency can be calculated using [Equation 32](#).

$$\eta = \frac{P_{OUT}}{P_{IN}}$$

or

$$\eta = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}}$$

where

- $P_{LOSS}$  is the sum of two types of losses in the converter, switching and conduction (32)

Conduction losses usually dominate at higher output loads, where as switching losses remain relatively fixed and dominate at lower output loads.

To calculate losses in the LM3410 or LM3410-Q1 device, use [Equation 33](#).

$$P_{LOSS} = P_{COND} + P_{SW} + P_Q$$

where

- $P_Q$  = quiescent operating power loss (33)

Conversion ratio of the boost converter with conduction loss elements inserted is calculated with [Equation 34](#).

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{D'} \left( 1 - \frac{D' \times V_D}{V_{IN}} \right) \left( \frac{1}{1 + \frac{R_{DCR} + (D \times R_{DSON})}{D'^2 R_{OUT}}} \right)$$

where

- $R_{DCR}$  is the Inductor series resistance (34)

**Thermal Considerations (continued)**

$$R_{OUT} = \frac{V_{OUT}}{I_{LED}} \quad (35)$$

If the loss elements are reduced to zero, the conversion ratio simplifies to [Equation 36](#).

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{D'} \quad (36)$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{\eta}{D'} \quad (37)$$

Therefore:

$$\eta = D' \frac{V_{OUT}}{V_{IN}} = \left( \frac{1 - \frac{D' \times V_D}{V_{IN}}}{1 + \frac{R_{DCR} + (D \times R_{DSON})}{D'^2 R_{OUT}}} \right) \quad (38)$$

Only calculations for determining the most significant power losses are discussed. Other losses totaling less than 2% are not discussed.

A simple efficiency calculation that takes into account the conduction losses is [Equation 39](#).

$$\eta \approx \left( \frac{1 - \frac{D' \times V_D}{V_{IN}}}{1 + \frac{R_{DCR} + (D \times R_{DSON})}{D'^2 R_{OUT}}} \right) \quad (39)$$

The diode, NMOS switch, and inductor (DCR) losses are included in this calculation. Setting any loss element to zero simplifies the equation.

$V_D$  is the forward voltage drop across the Schottky diode. It can be obtained from [Electrical Characteristics](#).

Conduction losses in the diode are calculated with [Equation 40](#).

$$P_{DIODE} = V_D \times I_{LED} \quad (40)$$

Depending on the duty cycle, this can be the single most significant power loss in the circuit. Choose a diode that has a low forward voltage drop. Another concern with diode selection is reverse leakage current. Depending on the ambient temperature and the reverse voltage across the diode, the current being drawn from the output to the NMOS switch during time (D) could be significant, this may increase losses internal to the LM3410 or LM3410-Q1 and reduce the overall efficiency of the application. See the Schottky diode manufacturer's data sheets for reverse leakage specifications.

Another significant external power loss is the conduction loss in the input inductor. The power loss within the inductor can be simplified to [Equation 41](#),

$$P_{IND} = I_{IN}^2 R_{DCR} \quad (41)$$

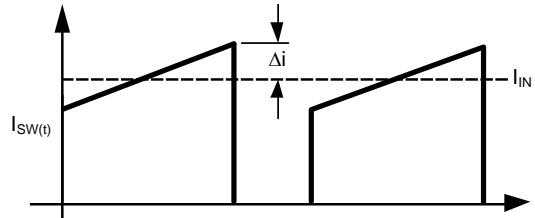
Or [Equation 42](#).

**Thermal Considerations (continued)**

$$P_{IND} = \left( \frac{I_O^2 R_{DCR}}{D'} \right) \tag{42}$$

The LM3410 and LM3410-Q1 conduction loss is mainly associated with the internal power switch.

$$P_{COND-NFET} = I_{SW-rms}^2 \times R_{DS(ON)} \times D \tag{43}$$



**Figure 37. LM3410 and LM3410-Q1 Switch Current**

$$I_{SW-rms} = I_{IND} \sqrt{D} \times \sqrt{1 + \frac{1}{3} \left( \frac{\Delta i}{I_{IND}} \right)^2} \approx I_{IND} \sqrt{D} \tag{44}$$

(small ripple approximation)

$$P_{COND-NFET} = I_{IN}^2 \times R_{DS(ON)} \times D \tag{45}$$

Or

$$P_{COND-NFET} = \left( \frac{I_{LED}}{D'} \right)^2 \times R_{DSON} \times D \tag{46}$$

The value for  $R_{DS(ON)}$  must be equal to the resistance at the desired junction temperature for analyzation. As an example, at 125°C and  $R_{DS(ON)} = 250 \text{ m}\Omega$  (See *Typical Characteristics* for value).

Switching losses are also associated with the internal power switch. They occur during the switch ON and OFF transition periods, where voltages and currents overlap resulting in power loss.

The simplest means to determine this loss is empirically measuring the rise and fall times (10% to 90%) of the switch at the switch node.

$$P_{SWR} = 1/2 (V_{OUT} \times I_{IN} \times f_{SW} \times t_{RISE}) \tag{47}$$

$$P_{SWF} = 1/2 (V_{OUT} \times I_{IN} \times f_{SW} \times t_{FALL}) \tag{48}$$

$$P_{SW} = P_{SWR} + P_{SWF} \tag{49}$$

**Table 25. Typical Switch-Node Rise and Fall Times**

$V_{IN}$ (V)	$V_{OUT}$ (V)	$t_{RISE}$ (ns)	$t_{FALL}$ (ns)
3	5	6	4
5	12	6	5
3	12	8	7
5	18	10	8

### 10.3.3.1 Quiescent Power Losses

$I_Q$  is the quiescent operating current, and is typically around 1.5 mA.

$$P_Q = I_Q \times V_{IN} \quad (50)$$

### 10.3.3.2 $R_{SET}$ Power Losses

$R_{SET}$  power loss is calculated with [Equation 51](#).

$$P_{RSET} = \frac{V_{FB}^2}{R_{SET}} \quad (51)$$

### 10.3.4 Example Efficiency Calculation

Operating Conditions: 5 × 3.3-V LEDs + 190 mV<sub>REF</sub> ≈ 16.7 V

**Table 26. Operating Conditions**

PARAMETER	VALUE
$V_{IN}$	3.3 V
$V_{OUT}$	16.7 V
$I_{LED}$	50 mA
$V_D$	0.45 V
$f_{SW}$	1.6 MHz
$I_Q$	3 mA
$t_{RISE}$	10 ns
$t_{FALL}$	10 ns
$R_{DS(ON)}$	225 mΩ
$L_{DCR}$	75 mΩ
D	0.82
$I_{IN}$	0.31 A

$$\Sigma P_{COND} + P_{SW} + P_{DIODE} + P_{IND} + P_Q = P_{LOSS} \quad (52)$$

#### Quiescent Power Loss:

$$P_Q = I_Q \times V_{IN} = 10 \text{ mW} \quad (53)$$

#### Switching Power Loss:

$$P_{SWR} = 1/2(V_{OUT} \times I_{IN} \times f_{SW} \times t_{RISE}) \approx 40 \text{ mW} \quad (54)$$

$$P_{SWF} = 1/2(V_{OUT} \times I_{IN} \times f_{SW} \times t_{FALL}) \approx 40 \text{ mW} \quad (55)$$

$$P_{SW} = P_{SWR} + P_{SWF} = 80 \text{ mW} \quad (56)$$

#### Internal NFET Power Loss:

$$R_{DS(ON)} = 225 \text{ m}\Omega \quad (57)$$

$$P_{CONDUCTION} = I_{IN}^2 \times D \times R_{DS(ON)} = 17 \text{ mW} \quad (58)$$

$$I_{IN} = 310 \text{ mA} \quad (59)$$

#### Diode Loss:

$$V_D = 0.45 \text{ V} \quad (60)$$

$$P_{DIODE} = V_D \times I_{LED} = 23 \text{ mW} \quad (61)$$

#### Inductor Power Loss:

$$R_{DCR} = 75 \text{ m}\Omega \quad (62)$$

$$P_{IND} = I_{IN}^2 \times R_{DCR} = 7 \text{ mW} \quad (63)$$

**Table 27. Total Power Losses**

PARAMETER	VALUE	LOSS PARAMETER	LOSS VALUE
V <sub>IN</sub>	3.3 V	—	—
V <sub>OUT</sub>	16.7 V	—	—
I <sub>LED</sub>	50 mA	P <sub>OUT</sub>	825 W
V <sub>D</sub>	0.45 V	P <sub>DIODE</sub>	23 mW
f <sub>SW</sub>	1.6 MHz	—	—
I <sub>Q</sub>	10 ns	P <sub>SWR</sub>	40 mW
t <sub>RISE</sub>	10 ns	P <sub>SWF</sub>	40 mW
I <sub>Q</sub>	3 mA	P <sub>Q</sub>	10 mW
R <sub>DS(ON)</sub>	225 mΩ	P <sub>COND</sub>	17 mW
L <sub>DCR</sub>	75 mΩ	P <sub>IND</sub>	7 mW
D	0.82	—	—
η	85%	P <sub>LOSS</sub>	137 mW

$$P_{\text{INTERNAL}} = P_{\text{COND}} + P_{\text{SW}} = 107 \text{ mW} \quad (64)$$

### 10.3.5 Calculating R<sub>θJA</sub> and R<sub>ψJC</sub>

$$R_{\theta JA} = \frac{T_J - T_A}{P_{\text{Dissipation}}} : R_{\psi JC} = \frac{T_J - T_{\text{Case}}}{P_{\text{Dissipation}}} \quad (65)$$

We now know the internal power dissipation, and we are trying to keep the junction temperature at or below 125°C. The next step is to calculate the value for R<sub>θJA</sub> or R<sub>ψJC</sub>. This is actually very simple to accomplish, and necessary for determining the correct package option for a given application.

The LM3410 and LM3410-Q1 have a thermal shutdown comparator. When the silicon reaches a temperature of 165°C, the device shuts down until the temperature drops to 150°C. From this, it is possible calculate the R<sub>θJA</sub> or the R<sub>ψJC</sub> of a specific application. Because the junction to top case thermal impedance is much lower than the thermal impedance of junction to ambient air, the error in calculating R<sub>ψJC</sub> is lower than for R<sub>θJA</sub>. However, a small thermocouple needs to be attached onto the top case of the device to obtain the R<sub>ψJC</sub> value.

Knowing the temperature of the silicon when the device shuts down provides three of the four variables. After calculating the thermal impedance, working backwards with the junction temperature set to 125°C, the maximum ambient air temperature to keep the silicon below 125°C can be calculated.

#### Procedure:

Place the application into a thermal chamber. Dissipate enough power in the device to obtain an accurate thermal impedance value.

Raise the ambient air temperature until the device goes into thermal shutdown. Record the temperatures of the ambient air and the top case temperature of the device. Calculate the thermal impedances.

Example from previous calculations (SOT-23 Package):

$$P_{\text{INTERNAL}} = 107 \text{ mW} \quad (66)$$

$$T_A \text{ at shutdown} = 155^\circ\text{C} \quad (67)$$

$$T_C \text{ at shutdown} = 159^\circ\text{C} \quad (68)$$

$$R_{\theta JA} = \frac{T_J - T_A}{P_{\text{Dissipation}}} : R_{\psi JC} = \frac{T_J - T_{\text{Case-Top}}}{P_{\text{Dissipation}}} \quad (69)$$

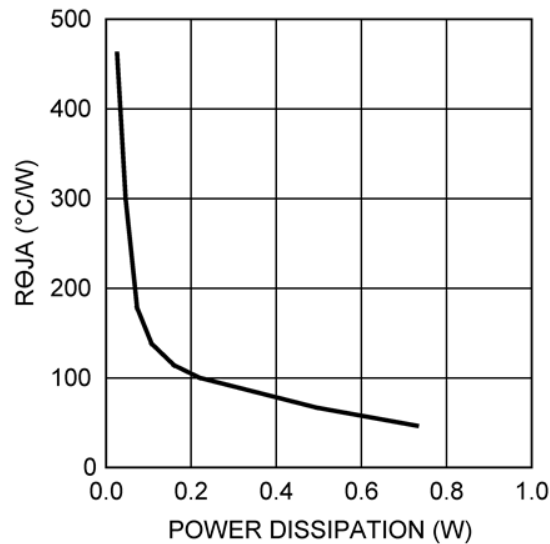
$$R_{\theta JA} \text{ SOT-23} = 93^\circ\text{C/W} \quad (70)$$

$$R_{\psi JC} \text{ SOT-23} = 56^\circ\text{C/W} \quad (71)$$

Typical WSON and MSOP typical applications produces  $R_{\theta JA}$  numbers from 53.7°C/W to 55.3°C/W, and  $R_{\theta JC}$  varies from 61.4°C/W to 65.9°C/W. These values are for PCBs with two and four layer boards with 0.5 oz copper, and four to six thermal vias to bottom side ground plane under the DAP. The thermal impedances calculated above are higher due to the small amount of power being dissipated within the device.

**NOTE**

To use these procedures it is important to dissipate an amount of power within the device that indicates a true thermal impedance value. If a very small internal dissipated value is used, the resulting thermal impedance calculated is abnormally high, and subject to error. [Figure 38](#) shows the nonlinear relationship of internal power dissipation vs  $R_{\theta JA}$ .



**Figure 38.  $R_{\theta JA}$  vs Internal Dissipation**

For 5-pin SOT-23 package typical applications,  $R_{\theta JA}$  numbers range from 164.2°C/W, and  $R_{\theta JC}$  varies from 115.3°C/W. These values are for PCBs with two and four layer boards with 0.5 oz copper, with two to four thermal vias from GND pin to bottom layer.

Using typical thermal impedances and an ambient temperature maximum of 75°C, if the design requires more dissipation than 400 mW internal to the device, or there is 750 mW of total power loss in the application, TI recommends using the 6-pin WSON or the 8-pin MSOP-PowerPad package with the exposed DAP.

## 11 デバイスおよびドキュメントのサポート

### 11.1 デバイス・サポート

#### 11.1.1 デバイスの関連用語

**放射** 温度が異なる物体間の、電磁気的な熱の移動。

**伝導** 固体の媒体を通した熱の移動。

**対流** 流体の媒体、通常は空気を通した熱の移動。

**$R_{\theta JA}$**  シリコン接合部から周囲の空気温度への熱インピーダンス。

$R_{\theta JA}$ は、小さな熱インピーダンスの合計です([Figure 35](#)および[Figure 36](#)を参照)。モデル内のコンデンサは、ある媒体において電力およびそれに関連する熱が定常状態から増大または減少した時点から、別の媒体において熱の増大または減少が定常状態に到達する時点までの遅延時間を表します。

**$R_{\theta JC}$**  シリコン接合部からデバイスのパッケージ温度への熱インピーダンス。

**$C_{\theta JC}$**  シリコン接合部からデバイスのパッケージ温度への熱遅延。



## デバイス・サポート (continued)

**C<sub>0</sub>CA** デバイスのパッケージから周囲の空気温度への熱遅延。

### 11.2 ドキュメントのサポート

#### 11.2.1 関連資料

関連資料については、以下を参照してください。

『[AN-1229 SIMPLE SWITCHER® PCBレイアウト・ガイドライン](#)』(SNVA054)

### 11.3 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 28. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
LM3410	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>
LM3410-Q1	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>

### 11.4 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](#)のデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

### 11.5 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.6 商標

PowerPad, E2E are trademarks of Texas Instruments.  
SIMPLE SWITCHER is a registered trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 11.7 静電気放電に関する注意事項



すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

### 11.8 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3410XMF/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SSVB	<a href="#">Samples</a>
LM3410XMF/NOPB	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SSVB	<a href="#">Samples</a>
LM3410XMF/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SSVB	<a href="#">Samples</a>
LM3410XMY/NOPB	ACTIVE	HVSSOP	DGN	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SSXB	<a href="#">Samples</a>
LM3410XMY/NOPB	ACTIVE	HVSSOP	DGN	8	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SSXB	<a href="#">Samples</a>
LM3410XMY/NOPB	ACTIVE	HVSSOP	DGN	8	3500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SSXB	<a href="#">Samples</a>
LM3410XQMF/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SXUB	<a href="#">Samples</a>
LM3410XSD/NOPB	ACTIVE	WSON	NGG	6	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	3410X	<a href="#">Samples</a>
LM3410XSD/NOPB	ACTIVE	WSON	NGG	6	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	3410X	<a href="#">Samples</a>
LM3410XSD/NOPB	ACTIVE	WSON	NGG	6	4500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	3410X	<a href="#">Samples</a>
LM3410YMF/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SSZB	<a href="#">Samples</a>
LM3410YMF/NOPB	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SSZB	<a href="#">Samples</a>
LM3410YMF/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SSZB	<a href="#">Samples</a>
LM3410YMY/NOPB	ACTIVE	HVSSOP	DGN	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	STAB	<a href="#">Samples</a>
LM3410YMY/NOPB	ACTIVE	HVSSOP	DGN	8	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	STAB	<a href="#">Samples</a>
LM3410YMY/NOPB	ACTIVE	HVSSOP	DGN	8	3500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	STAB	<a href="#">Samples</a>
LM3410YQMF/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SXXB	<a href="#">Samples</a>
LM3410YQMF/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SXXB	<a href="#">Samples</a>
LM3410YSD/NOPB	ACTIVE	WSON	NGG	6	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	3410Y	<a href="#">Samples</a>
LM3410YSD/NOPB	ACTIVE	WSON	NGG	6	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	3410Y	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3410XMF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3410XMF/NOPB	SOT-23	DBV	5	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3410XMF/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3410XMY/NOPB	HVSSOP	DGN	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3410XMY/NOPB	HVSSOP	DGN	8	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3410XMY/NOPB	HVSSOP	DGN	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3410XQMF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3410XSD/NOPB	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM3410XSD/NOPB	WSON	NGG	6	250	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM3410XSD/NOPB	WSON	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM3410YMF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3410YMF/NOPB	SOT-23	DBV	5	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3410YMF/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3410YMY/NOPB	HVSSOP	DGN	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3410YMY/NOPB	HVSSOP	DGN	8	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3410YMY/NOPB	HVSSOP	DGN	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3410YQMF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3410YQMF/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3410YSD/NOPB	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM3410YSDE/NOPB	WSON	NGG	6	250	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

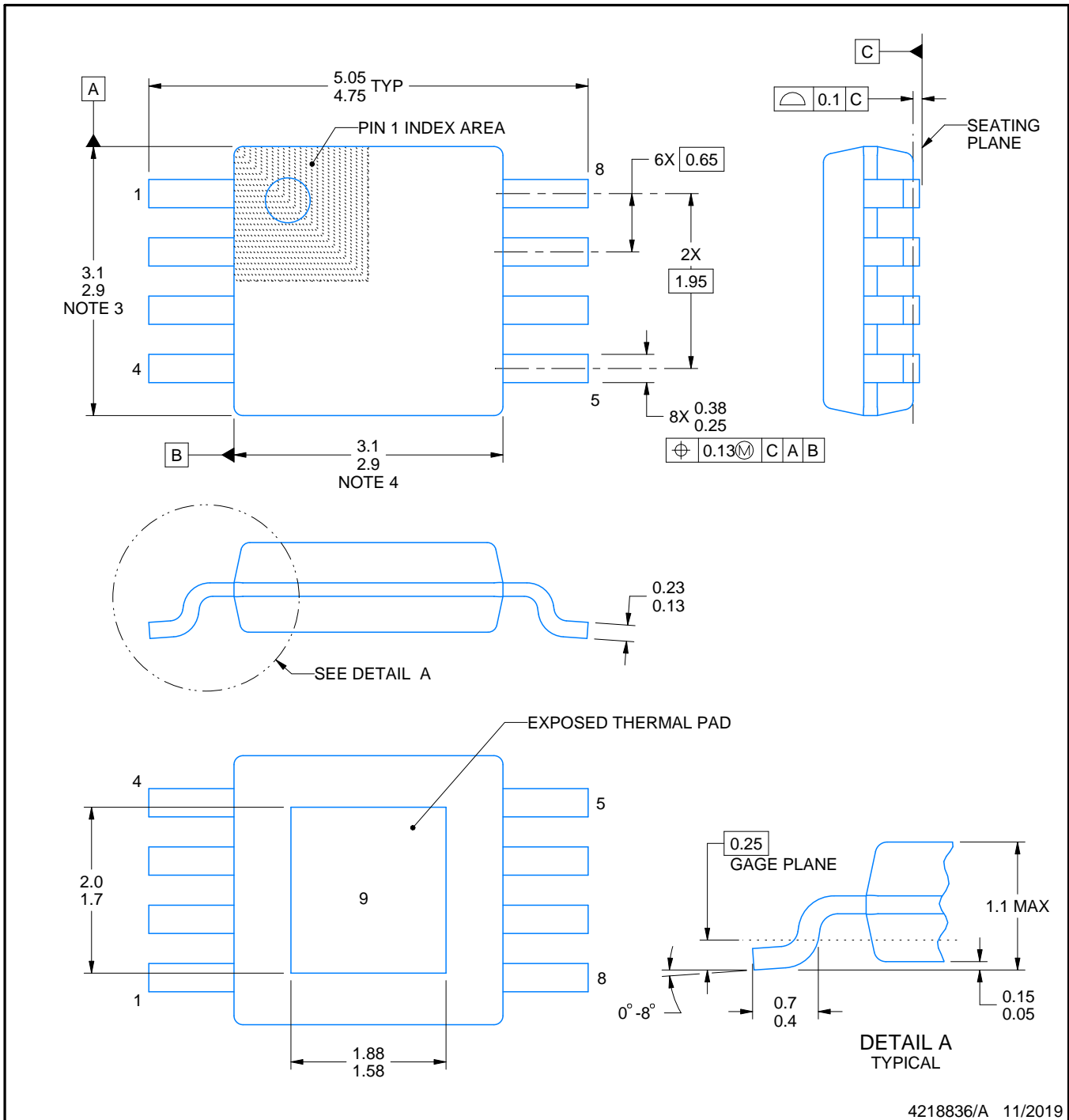
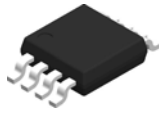
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3410XMF/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LM3410XMF/NOPB	SOT-23	DBV	5	250	208.0	191.0	35.0
LM3410XMF/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LM3410XMY/NOPB	HVSSOP	DGN	8	1000	208.0	191.0	35.0
LM3410XMY/NOPB	HVSSOP	DGN	8	250	208.0	191.0	35.0
LM3410XMY/NOPB	HVSSOP	DGN	8	3500	367.0	367.0	35.0
LM3410XQMF/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LM3410XSD/NOPB	WSON	NGG	6	1000	208.0	191.0	35.0
LM3410XSD/NOPB	WSON	NGG	6	250	208.0	191.0	35.0
LM3410XSD/NOPB	WSON	NGG	6	4500	367.0	367.0	35.0
LM3410YMF/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LM3410YMF/NOPB	SOT-23	DBV	5	250	208.0	191.0	35.0
LM3410YMF/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LM3410YMY/NOPB	HVSSOP	DGN	8	1000	208.0	191.0	35.0
LM3410YMY/NOPB	HVSSOP	DGN	8	250	208.0	191.0	35.0
LM3410YMY/NOPB	HVSSOP	DGN	8	3500	367.0	367.0	35.0
LM3410YQMF/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LM3410YQMF/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0

---

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3410YSD/NOPB	WSON	NGG	6	1000	208.0	191.0	35.0
LM3410YSDE/NOPB	WSON	NGG	6	250	208.0	191.0	35.0



4218836/A 11/2019

NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

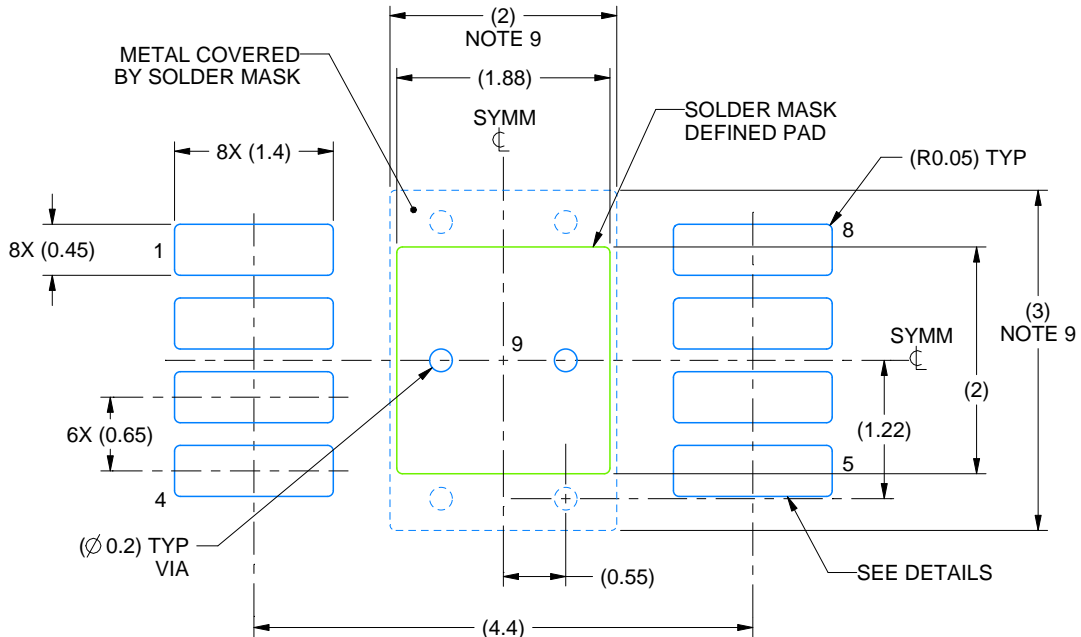


# EXAMPLE BOARD LAYOUT

DGN0008A

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



SOLDER MASK DETAILS

4218836/A 11/2019

NOTES: (continued)

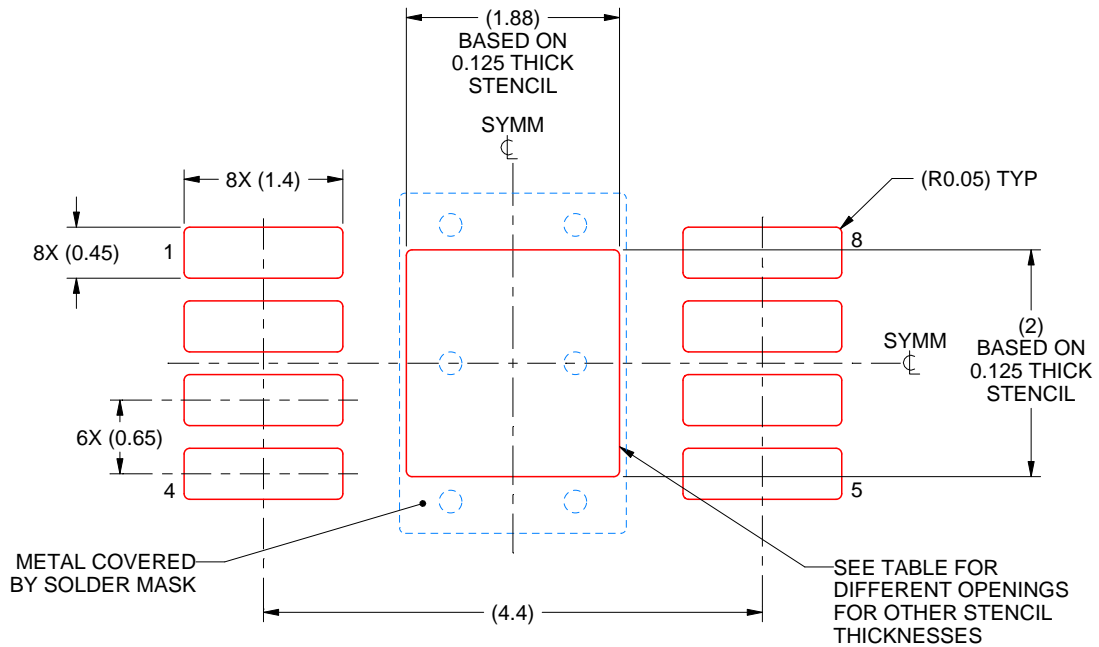
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DGN0008A

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



**SOLDER PASTE EXAMPLE**  
EXPOSED PAD 9:  
100% PRINTED SOLDER COVERAGE BY AREA  
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.10 X 2.24
0.125	1.88 X 2.00 (SHOWN)
0.15	1.72 X 1.83
0.175	1.59 X 1.69

4218836/A 11/2019

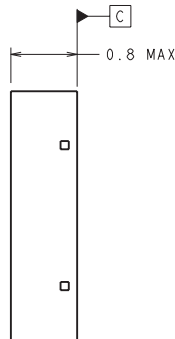
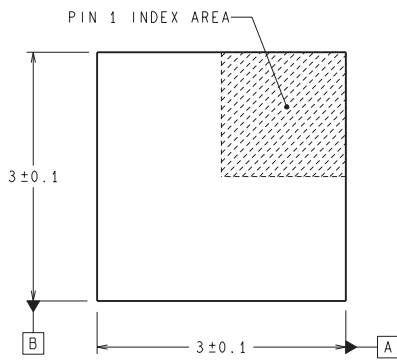
NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

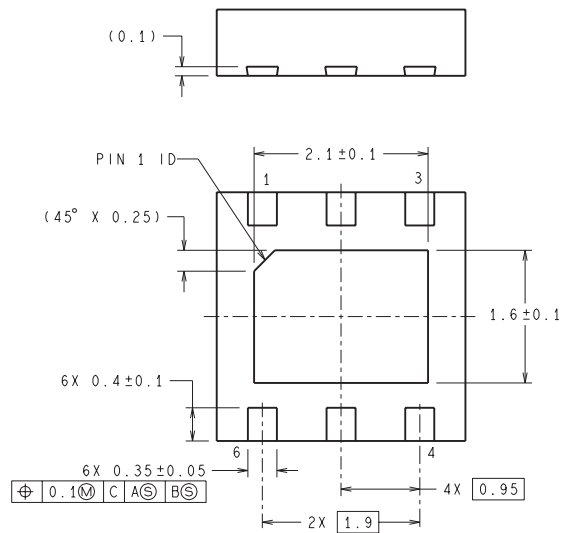
NGG0006A



RECOMMENDED LAND PATTERN



DIMENSIONS ARE IN MILLIMETERS  
DIMENSION IN ( ) FOR REFERENCE ONLY



SDE06A (Rev A)

# DBV0005A



# PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/K 08/2024

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

# EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## 重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス・デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、または [ti.com](#) やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所 : Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2024, Texas Instruments Incorporated