

MAX232 デュアル EIA-232 ドライバ/レシーバ

1 特長

- TIA/EIA-232-F および ITU 勧告 V.28 適合またはそれを上回る性能
- 1 μ F チャージポンプコンデンサを使用して 5V 単一電源で動作
- 最大 120kbit/s で動作
- 2 つのドライバと 2 つのレシーバ
- ± 30 V の入力レベル
- 低い消費電流: 8mA (代表値)
- JESD 22 を上回る ESD 保護
 - 2000V、人体モデル (A114-A)
- MAX202 デバイスを使用すれば、ESD (15kV HBM) の改善および 0.1 μ F チャージポンプコンデンサによるアップグレードが可能です。

2 アプリケーション

- TIA/EIA-232-F
- [バッテリー駆動システム](#)
- 端末
- モデム
- コンピュータ

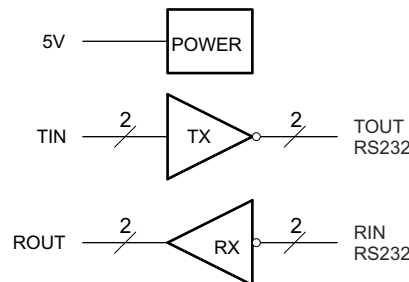
3 概要

MAX232 デバイスは、5V 単一電源から TIA/EIA-232-F の電圧レベルを供給する容量性電圧発生器を内蔵したデュアル ドライバ / レシーバです。各レシーバは、TIA/EIA-232-F の入力を 5V の TTL/CMOS レベルに変換します。これらのレシーバは、標準スレッショルドが 1.3V、標準ヒステリシスが 0.5V で、 ± 30 V の入力を受け入れます。各ドライバは、TTL/CMOS 入力レベルを TIA/EIA-232-F レベルに変換します。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ (2)
MAX232	SOIC (16)	9.9mm \times 6mm
	SOIC (16)	10.4mm \times 10.3mm
	PDIP (16)	19.3mm \times 9mm
	SOP (16)	10.2mm \times 7.8 mm

- (1) 詳細については、[セクション 11](#) を参照してください。
- (2) パッケージ サイズ (長さ \times 幅) は公称値であり、該当する場合はピンも含まれます。



概略回路図



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4 Pin Configuration and Functions

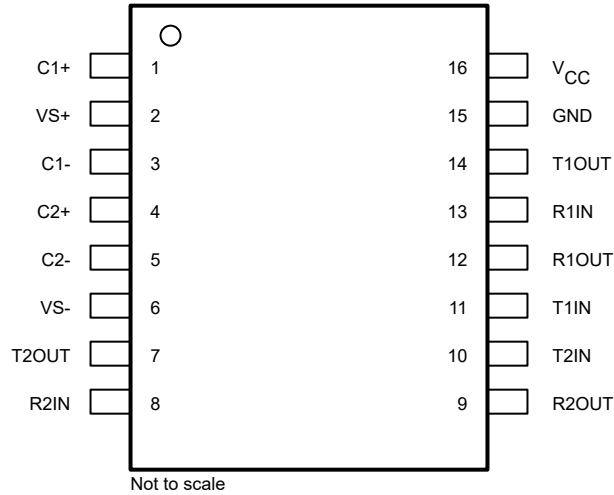


図 4-1. MAX232: D, DW, N or NS Package
MAX232I: D, DW, or N Package
(Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
C1+	1	—	Positive lead of C1 capacitor
VS+	2	O	Positive charge pump output for storage capacitor only
C1-	3	—	Negative lead of C1 capacitor
C2+	4	—	Positive lead of C2 capacitor
C2-	5	—	Negative lead of C2 capacitor
VS-	6	O	Negative charge pump output for storage capacitor only
T2OUT	7	O	RS232 line data output (to remote RS232 system)
R2IN	8	I	RS232 line data input (from remote RS232 system)
R2OUT	9	O	Logic data output (to UART)
T2IN	10	I	Logic data input (from UART)
T1IN	11	I	Logic data input (from UART)
R1IN	13	I	RS232 line data input (from remote RS232 system)
T1OUT	14	O	RS232 line data output (to remote RS232 system)
GND	15	—	Ground
V _{CC}	16	—	Supply Voltage, Connect to external 5V power supply

5 Specifications

5.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Input Supply voltage range ⁽²⁾	-0.3	6	V
V _{S+}	Positive output supply voltage range	V _{CC} - 0.3	15	V
V _{S-}	Negative output supply voltage range	-0.3	-15	V
V _I	Input voltage range	T1IN, T2IN	V _{CC} + 0.3	V
		R1IN, R2IN	±30	
V _O	Output voltage range	T1OUT, T2OUT	V _{S-} - 0.3 V _{S+} + 0.3	V
		R1OUT, R2OUT	-0.3 V _{CC} + 0.3	
Short-circuit duration		T1OUT, T2OUT		
		Unlimited		
T _J	Operating virtual junction temperature	150		°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network GND.

5.2 ESD Ratings

		MIN	MAX	UNIT
T _{stg}	Storage temperature range	-65	150	°C
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins ⁽¹⁾	0 2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	0 1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	4.5	5	5.5	V
V _{IH}	High-level input voltage (T1IN, T2IN)	2			V
V _{IL}	Low-level input voltage (T1IN, T2IN)	0.8			V
R1IN, R2IN	Receiver input voltage	±30			V
T _A	Operating free-air temperature	MAX232	0	70	°C
		MAX232I	-40	85	

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SOIC (D)	SOIC wide (DW)	PDIP (N)	SOP (NS)	UNIT
		16 PINS	16 PINS	16 PINS	16 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	84.6	71.7	60.6	88.5	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	43.5	37.6	48.1	46.2	°C/W
R _{θJB}	Junction-to-board thermal resistance	43.2	36.8	40.6	50.7	°C/W
ψ _{JT}	Junction-to-top characterization parameter	10.4	13.3	27.5	13.5	°C/W
ψ _{JB}	Junction-to-board characterization parameter	42.8	36.4	40.3	50.3	°C/W

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

5.5 Electrical Characteristics, Device

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [8-1](#))

PARAMETER		TEST CONDITIONS ⁽²⁾	MIN	TYP ⁽¹⁾	MAX	UNIT
I_{CC}	Supply current	$V_{CC} = 5.5V$, all outputs open, $T_A = 25^\circ C$		8	10	mA

- (1) All typical values are at $V_{CC} = 5V$, and $T_A = 25^\circ C$.
(2) Test conditions are C1–C4 = 1 μ F at $V_{CC} = 5V \pm 0.5V$

5.6 Electrical Characteristics, Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽²⁾	MIN	TYP ⁽¹⁾	MAX	UNIT
V_{OH}	High-level output voltage	T1OUT, T2OUT $R_L = 3k\Omega$ to GND	5	7		V
V_{OL}	Low-level output voltage ⁽²⁾	T1OUT, T2OUT $R_L = 3k\Omega$ to GND		–7	–5	V
r_O	Output resistance	T1OUT, T2OUT $V_{S+} = V_{S-} = 0$, $V_O = \pm 2V$	300			Ω
I_{OS} ⁽³⁾	Short-circuit output current	T1OUT, T2OUT $V_{CC} = 5.5V$, $V_O = 0V$		± 10		mA
I_{IS}	Short-circuit input current	T1IN, T2IN $V_I = 0$			200	μA

- (1) All typical values are at $V_{CC} = 5V$, $T_A = 25^\circ C$.
(2) The algebraic convention, in which the least-positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.
(3) Not more than one output should be shorted at a time.

5.7 Electrical Characteristics, Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽³⁾	MIN	TYP ⁽¹⁾	MAX	UNIT
V_{OH}	High-level output voltage	R1OUT, R2OUT $I_{OH} = -1mA$	3.5			V
V_{OL}	Low-level output voltage ⁽²⁾	R1OUT, R2OUT $I_{OL} = 3.2mA$			0.4	V
V_{IT+}	Receiver positive-going input threshold voltage	R1IN, R2IN $V_{CC} = 5V$, $T_A = 25^\circ C$		1.7	2.4	V
V_{IT-}	Receiver negative-going input threshold voltage	R1IN, R2IN $V_{CC} = 5V$, $T_A = 25^\circ C$	0.8	1.2		V
V_{hys}	Input hysteresis voltage	R1IN, R2IN $V_{CC} = 5V$	0.2	0.5	1	V
r_I	Receiver input resistance	R1IN, R2IN $V_{CC} = 5V$, $T_A = 25^\circ C$	3	5	7	k Ω

- (1) All typical values are at $V_{CC} = 5V$, $T_A = 25^\circ C$.
(2) The algebraic convention, in which the least-positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.
(3) Test conditions are C1–C4 = 1 μ F at $V_{CC} = 5V \pm 0.5V$.

5.8 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽¹⁾	MIN	TYP ⁽¹⁾	MAX	UNIT
SR	Driver slew rate	$R_L = 3k\Omega$ to $7k\Omega$, see 6-2			30	V/ μ s
SR(t)	Driver transition region slew rate	see 6-3		3		V/ μ s
	Data rate	One TOUT switching		120		kbit/s
t_{PLH} ®	Receiver propagation delay time, low- to high-level output	TTL load, see 6-1		500		ns
t_{PHL} ®	Receiver propagation delay time, high- to low-level output	TTL load, see 6-1		500		ns

- (1) Test conditions are C1–C4 = 1 μ F at $V_{CC} = 5V \pm 0.5V$.

5.9 Typical Characteristics

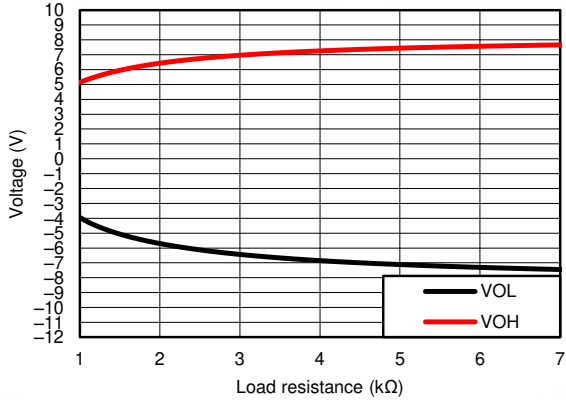


图 5-1. TOUT VOH & VOL vs Load Resistance, Both Drivers Loaded

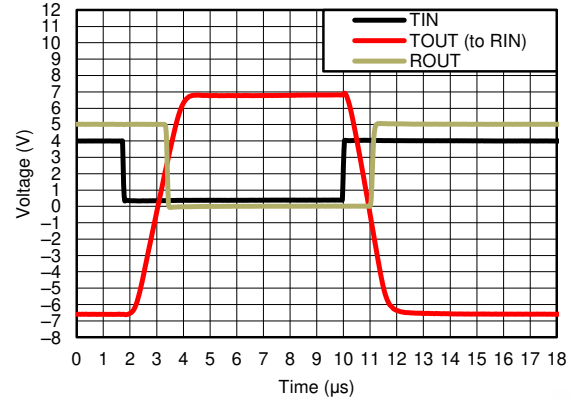
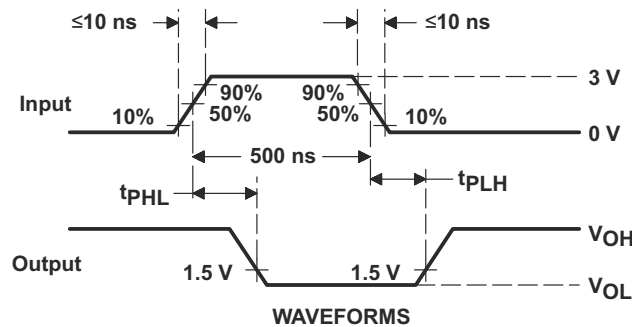
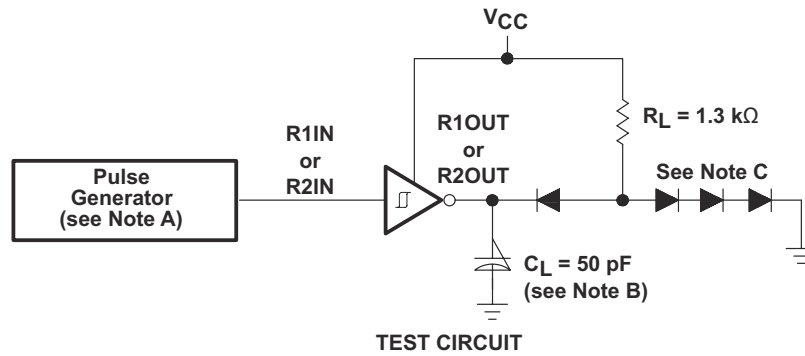


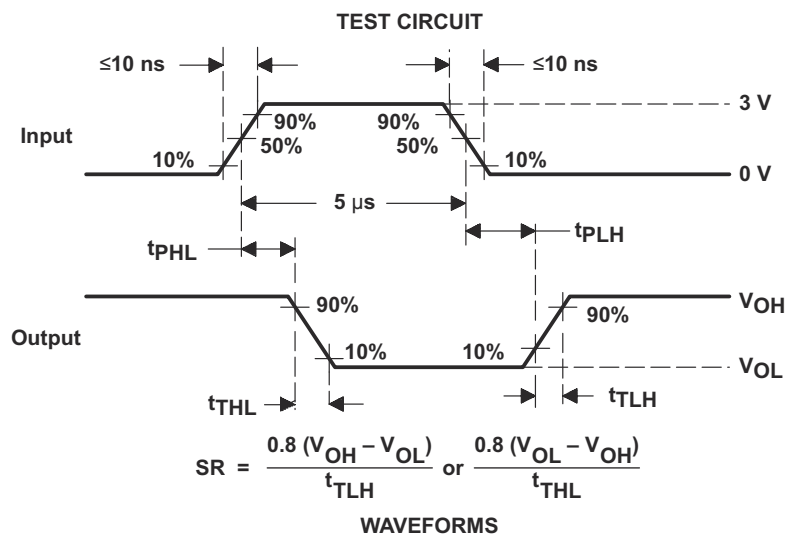
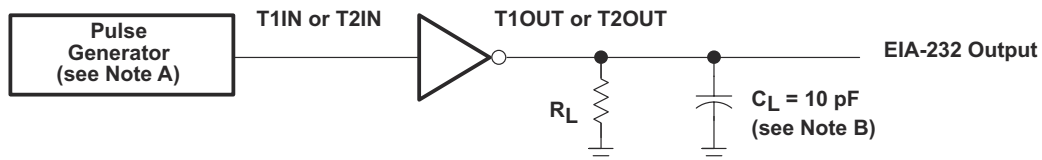
图 5-2. Driver to Receiver Loopback Timing Waveform

6 Parameter Measurement Information



- A. The pulse generator has the following characteristics: $Z_O = 50\Omega$, duty cycle $\leq 50\%$.
- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N3064 or equivalent.

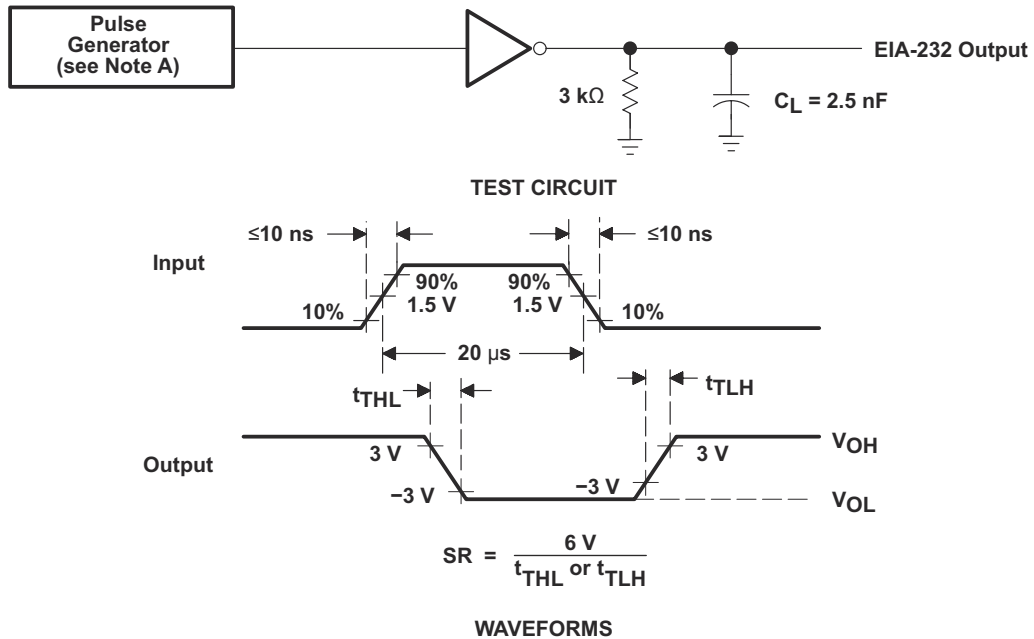
图 6-1. Receiver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurements



- A. The pulse generator has the following characteristics: $Z_O = 50\Omega$, duty cycle $\leq 50\%$.

B. C_L includes probe and jig capacitance.

图 6-2. Driver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurements (5 μ s Input)



A. The pulse generator has the following characteristics: $Z_O = 50\Omega$, duty cycle $\leq 50\%$.

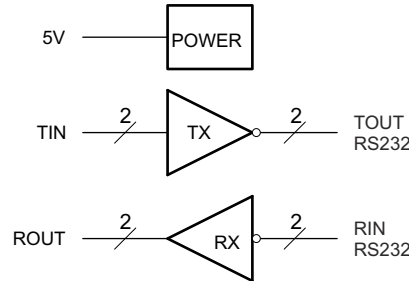
图 6-3. Test Circuit and Waveforms for t_{THL} and t_{TLH} Measurements (20 μ s Input)

7 Detailed Description

7.1 Overview

The MAX232 device is a dual driver/receiver that includes a capacitive voltage generator using four capacitors to supply TIA/EIA-232-F voltage levels from a single 5-V supply. Each receiver converts TIA/EIA-232-F inputs to 5-V TTL/CMOS levels. These receivers have a typical threshold of 1.3 V, a typical hysteresis of 0.5 V, and can accept ± 30 -V inputs. Each driver converts TTL/CMOS input levels into TIA/EIA-232-F levels. The driver, receiver, and voltage-generator functions are available as cells in the Texas Instruments LinASIC™ library. Outputs are protected against shorts to ground.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power

The power block increases and inverts the 5V supply for the RS232 driver using a charge pump that requires four 1 μ F external capacitors.

7.3.2 RS232 Driver

Two drivers interface standard logic level to RS232 levels. Internal pull up resistors on TIN inputs ensures a high input when the line is high impedance.

7.3.3 RS232 Receiver

Two receivers interface RS232 levels to standard logic levels. An open input will result in a high output on ROUT.

7.4 Device Functional Modes

7.4.1 V_{CC} powered by 5V

The device will be in normal operation.

7.4.2 V_{CC} unpowered

When MAX232 is unpowered, it can be safely connected to an active remote RS232 device.

7.4.3 Function Tables

表 7-1. Each Driver

INPUT ⁽¹⁾	OUTPUT
T _{IN}	T _{OUT}
L	H
H	L

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

表 7-2. Each Receiver

INPUTS ⁽¹⁾		OUTPUT	
R _{IN}		R _{OUT}	
L		H	
H		L	
Open		H	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = disconnected input or connected driver off

8 Application and Implementation

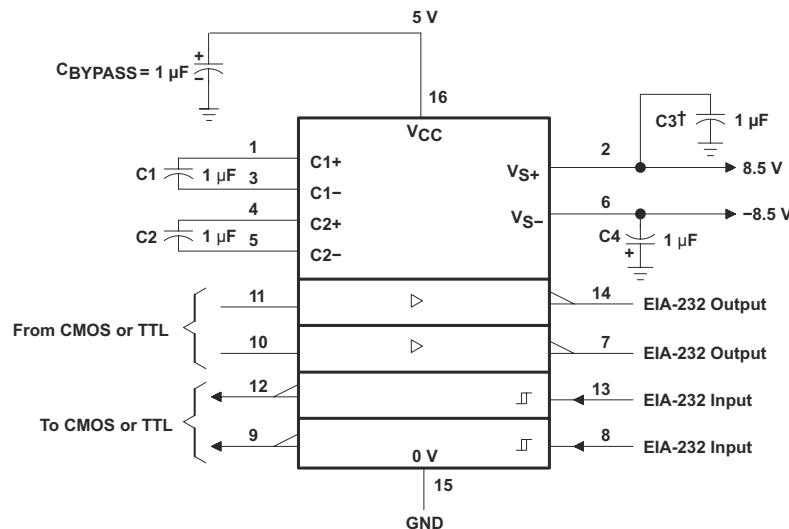
注

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8.1 Application Information

For proper operation add capacitors as shown in [図 8-1](#). Pins 9 through 12 connect to UART or general purpose logic lines. EIA-232 lines will connect to a connector or cable.

8.2 Typical Application



† C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown. In addition to the 1-µF capacitors shown, the MAX202 can operate with 0.1-µF capacitors.

図 8-1. Typical Operating Circuit

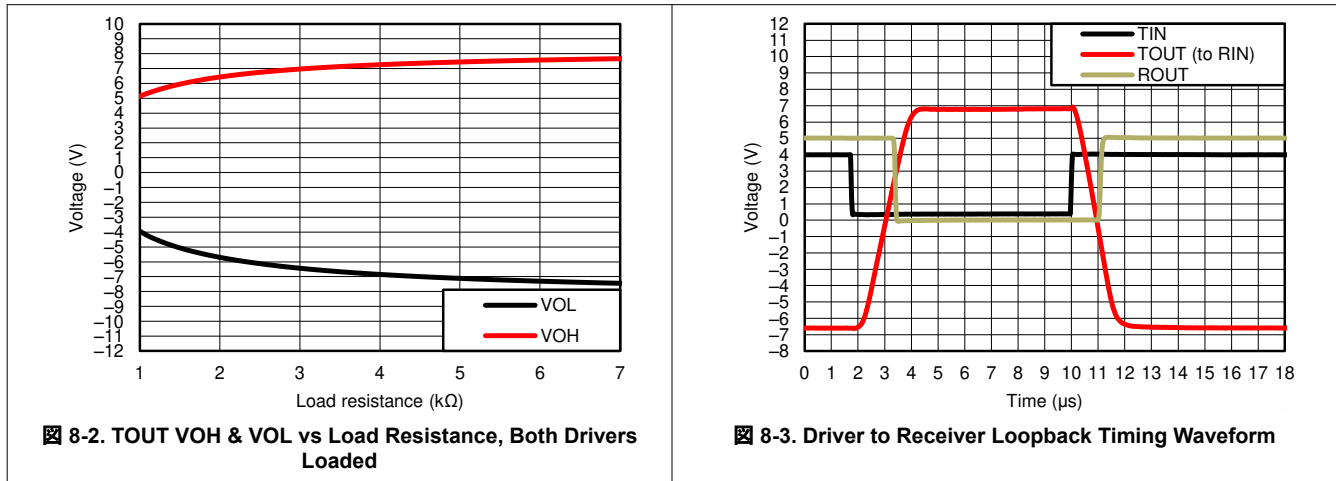
8.2.1 Design Requirements

- V_{CC} minimum is 4.5V and maximum is 5.5V.
- Maximum recommended bit rate is 120kbps.

8.2.2 Detailed Design Procedure

Use 1µF tantalum or ceramic capacitors.

8.2.3 Application Curves



8.3 Power Supply Recommendations

The V_{CC} voltage should be connected to the same power source used for logic device connected to TIN pins. V_{CC} should be between 4.5V and 5.5V.

8.4 Layout

8.4.1 Layout Guidelines

Keep the external capacitor traces short. This is more important on C1 and C2 nodes that have the fastest rise and fall times.

8.4.2 Layout Example

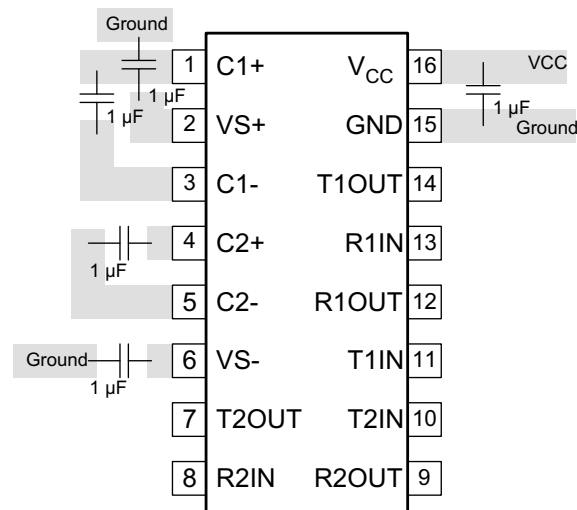


Figure 8-4. Layout Schematic

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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9.3 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

9.4 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい ESD 対策をとらないと、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.5 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

Changes from Revision M (November 2004) to Revision N (February 2024)	Page
• Changed the Handling Ratings table to the <i>ESD Ratings</i> table.....	4
• Changed the <i>Thermal Information</i> table.....	4

Changes from Revision L (March 2004) to Revision M (November 2014)	Page
• 「注文情報」表を削除.....	1
• 「取り扱い定格」の表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加.....	1
• 「製品情報」表を「パッケージ情報」表に変更.....	1
• Moved T_{stg} to Handling Ratings table.....	4

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MAX232DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	0 to 70	MAX232	Samples
MAX232IDR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX232I	Samples
MAX232IDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX232I	Samples
MAX232N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	MAX232N	Samples
MAX232NE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	MAX232N	Samples
MAX232NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX232	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX232DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MAX232DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MAX232IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MAX232IDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
MAX232NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MAX232DR	SOIC	D	16	2500	356.0	356.0	35.0
MAX232DR	SOIC	D	16	2500	333.2	345.9	28.6
MAX232IDR	SOIC	D	16	2500	340.5	336.1	32.0
MAX232IDWR	SOIC	DW	16	2000	350.0	350.0	43.0
MAX232NSR	SO	NS	16	2000	367.0	367.0	38.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
MAX232N	N	PDIP	16	25	506	13.97	11230	4.32
MAX232N	N	PDIP	16	25	506	13.97	11230	4.32
MAX232NE4	N	PDIP	16	25	506	13.97	11230	4.32
MAX232NE4	N	PDIP	16	25	506	13.97	11230	4.32

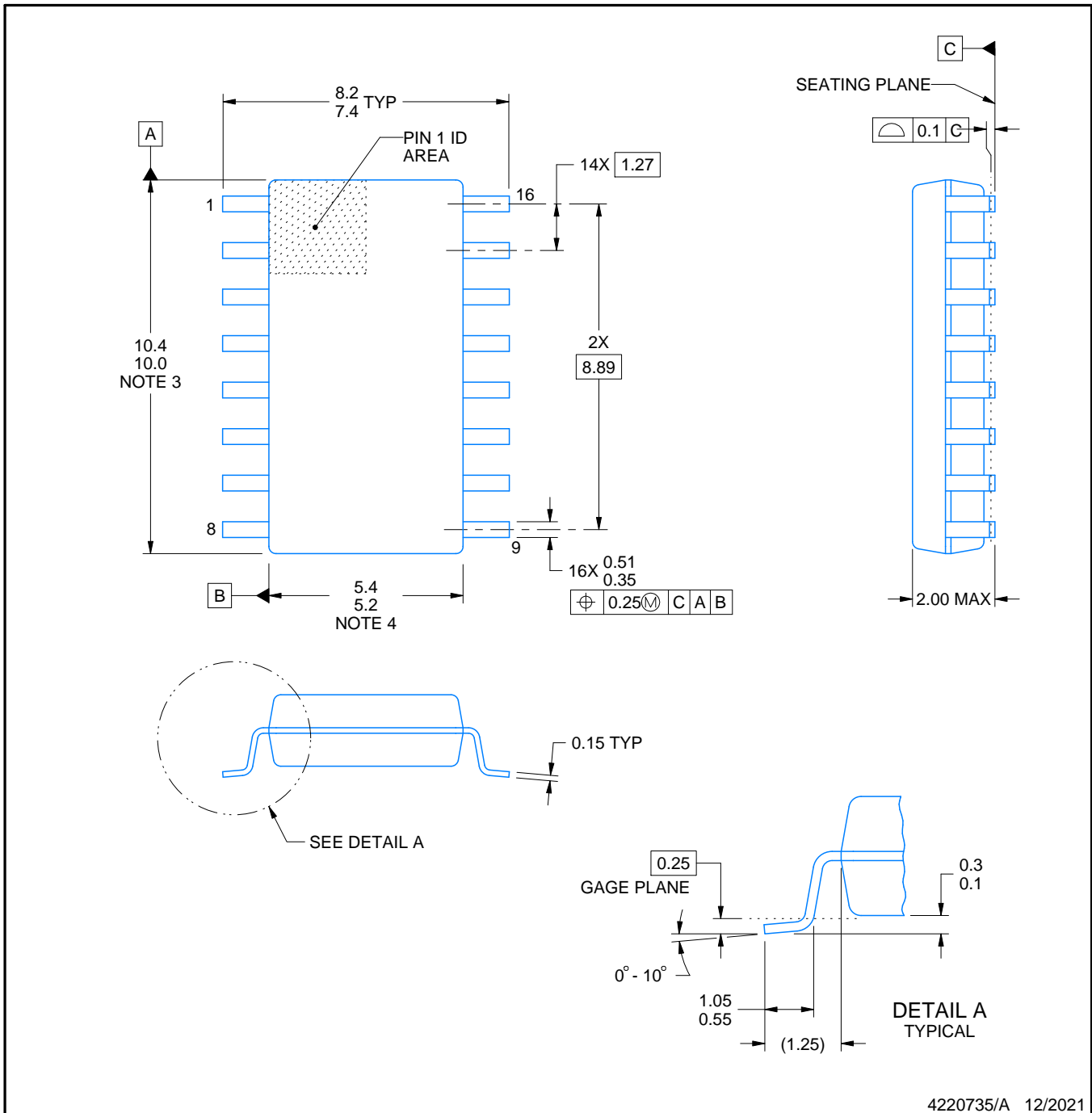


PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

GENERIC PACKAGE VIEW

DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

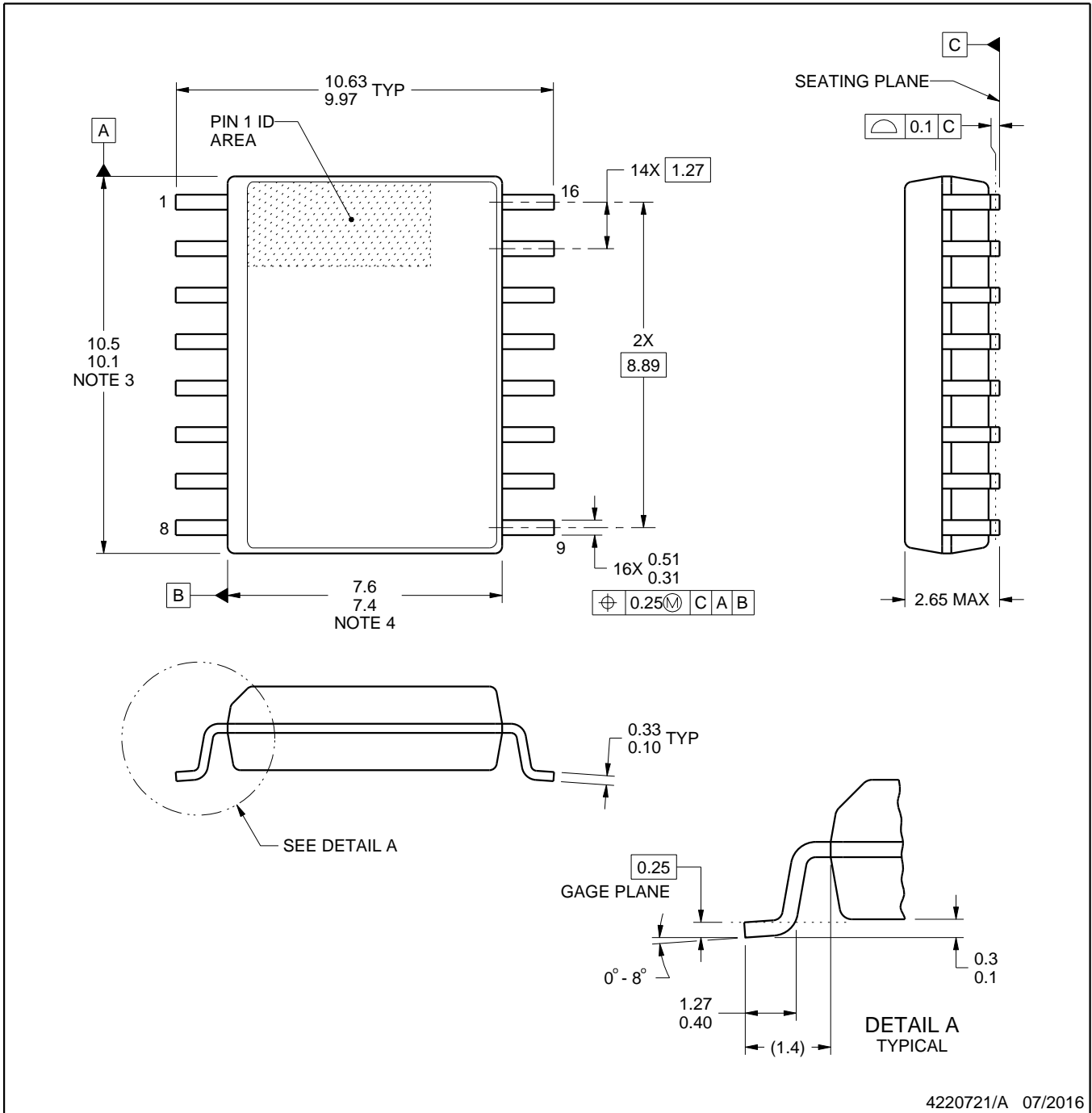


DW0016A

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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