

MAX232E デュアル RS-232 ドライバ/レシーバ、IEC61000-4-2 保護機能搭載

1 特長

- TIA/RS-232-F および ITU 勧告 V.28 適合またはそれを上回る性能
- RS-232 バスピン用 ESD 保護機能
 - ±15kV 人体モデル (HBM)
 - ±8kV IEC61000-4-2、接触放電
 - ±15kV IEC61000-4-2、気中放電
- 1µF チャージポンプコンデンサを使用して 5V 単一電源で動作
- 最大 250kbit/s で動作
- 2つのドライバと2つのレシーバ
- 低い消費電流: 8mA (代表値)

2 アプリケーション

- TIA/RS-232-F
- [バッテリー駆動システム](#)
- 端末
- モデム
- コンピュータ

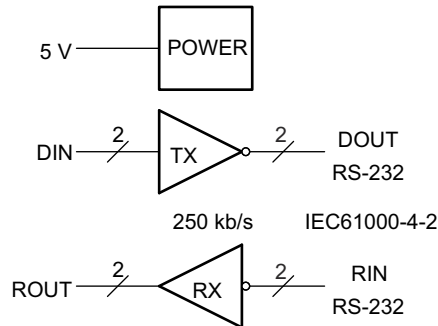
3 概要

MAX232E は、5V 単一電源から RS-232-F 準拠の電圧レベルを供給する容量性電圧発生器を内蔵したデュアルドライバ/レシーバです。各レシーバは、RS-232 の入力を 5V の TTL/CMOS レベルに変換します。このレシーバは、標準スレッショルドが 1.3V、標準ヒステリシスが 0.5V で、±30V の入力を受け入れます。各ドライバは、TTL/CMOS 入力レベルを TIA/RS-232-F レベルに変換します。

パッケージ情報

部品番号	パッケージ (1)	パッケージサイズ (2)
MAX232	SOIC (16)	9.9mm × 6mm
	SOIC (16)	10.4mm × 10.3mm
	PDIP (16)	19.3mm × 9mm
	SOP (16)	10.2mm × 7.8 mm

- (1) 詳細については、[セクション 10](#) を参照してください。
- (2) パッケージサイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



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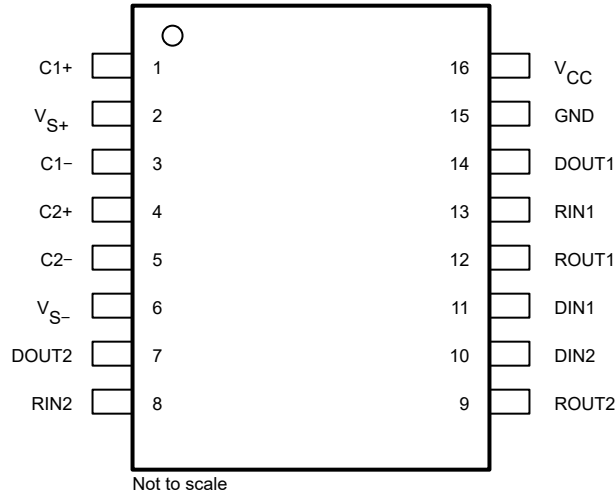
論理図 (正論理)



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4 Pin Configuration and Functions




4-1. D (SOIC), DW (SOIC), N (PDIP), or PW (TSSOP) 16-Pin Package (Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	C1+	—	Positive lead of C1 capacitor
2	VS+	O	Positive charge pump output for storage capacitor only
3	C1-	—	Negative lead of C1 capacitor
4	C2+	—	Positive lead of C2 capacitor
5	C2-	—	Negative lead of C2 capacitor
6	VS-	O	Negative charge pump output for storage capacitor only
7	DOUT2	O	RS-232 line data output (to remote RS-232 system)
8	RIN2	I	RS-232 line data input (from remote RS-232 system)
9	ROUT2	O	Logic data output (to UART)
10	DIN2	I	Logic data input (from UART)
11	DIN1	I	Logic data input (from UART)
12	ROUT1	O	Logic data output (to UART)
13	RIN1	I	RS-232 line data input (from remote RS-232 system)
14	DOUT1	O	RS-232 line data output (to remote RS-232 system)
15	GND	—	Ground
16	VCC	—	Supply voltage, connect to external 5V power supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Input supply voltage ⁽²⁾	-0.3	6	V
V _{S+}	Positive output supply voltage	V _{CC} - 0.3	15	V
V _{S-}	Negative output supply voltage	-0.3	-15	V
V _I	Input voltage	Driver	V _{CC} + 0.3	V
		Receiver	±30	
V _O	Output voltage	DOUT	V _{S-} - 0.3 V _{S+} + 0.3	V
		ROUT	-0.3 V _{CC} + 0.3	
	Short-circuit duration	DOUT		Unlimited
T _J	Operating virtual junction temperature		150	°C
T _{stg}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network GND.

5.2 ESD Ratings

			VALUE	UNIT	
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	Pins 7, 8, 13, and 14	±15000	V
			Other pins	±3000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	All pins	±1500	
		IEC61000-4-2, air-gap discharge	Pins 7, 8, 13, and 14	±15000	
	IEC61000-4-2, contact discharge			±8000	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	4.5	5	5.5	V
V _{IH}	High-level input voltage (DIN1, DIN2)	2			V
V _{IL}	Low-level input voltage (DIN1, DIN2)			0.8	V
	Receiver input voltage (RIN1, RIN2)	±3		±30	V
T _A	Operating free-air temperature	MAX232EC	0	70	°C
		MAX232EI	-40	85	

5.4 Thermal Information

THERMAL METRIC ^{(1) (2) (3)}		D (SOIC)	DW (SOIC)	N (PDIP)	PW (TSSOP)	UNIT
		16 PINS	16 PINS	16 PINS	16 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	84.6	73.4	60.6	107.5	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	43.5	35.1	48.1	38.4	°C/W
R _{θJB}	Junction-to-board thermal resistance	43.2	38.3	40.6	53.7	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	10.4	9.4	27.5	3.2	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	42.8	37.7	40.3	53.1	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.
- (2) Maximum power dissipation is a function of T_{J(max)}, R_{θJA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is P_D = (T_{J(max)} – T_A)/R_{θJA}. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

5.5 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [7-1](#))

PARAMETER		TEST CONDITIONS ⁽¹⁾		MIN	TYP ⁽²⁾	MAX	UNIT
I _{CC}	Supply current	V _{CC} = 5.5 V	All outputs open, T _A = 25°C		8	10	mA

- (1) Test conditions are C1 – C4 = 1μF at V_{CC} = 5V ± 0.5V.
- (2) All typical values are at V_{CC} = 5 V and T_A = 25°C.

5.6 Electrical Characteristics: Driver

over recommended ranges of supply voltage and operating free-air temperature range

PARAMETER		TEST CONDITIONS ⁽¹⁾		MIN	TYP ⁽²⁾	MAX	UNIT
V _{OH}	High-level output voltage	DOUT	R _L = 3 kΩ to GND	5	7		V
V _{OL}	Low-level output voltage ⁽³⁾	DOUT	R _L = 3 kΩ to GND		–7	–5	V
r _o	Output resistance	DOUT	V _{S+} = V _{S–} = 0, V _O = ±2 V	300			Ω
I _{OS} ⁽⁴⁾	Short-circuit output current	DOUT	V _{CC} = 5.5 V, V _O = 0		±10		mA
I _{IS}	Short-circuit input current	DIN	V _I = 0			200	μA

- (1) Test conditions are C1 – C4 = 1μF at V_{CC} = 5V ± 0.5V.
- (2) All typical values are at V_{CC} = 5V and T_A = 25°C.
- (3) The algebraic convention, in which the least-positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.
- (4) Not more than one output should be shorted at a time.

5.7 Electrical Characteristics: Receiver

over recommended ranges of supply voltage and operating free-air temperature range

PARAMETER		TEST CONDITIONS ⁽¹⁾		MIN	TYP ⁽²⁾	MAX	UNIT
V _{OH}	High-level output voltage	ROUT	I _{OH} = –1mA	3.5			V
V _{OL}	Low-level output voltage	ROUT	I _{OL} = 3.2mA			0.4	V
V _{IT+}	Receiver positive-going input threshold voltage	RIN	V _{CC} = 5V T _A = 25°C		1.7	2.4	V
V _{IT–}	Receiver negative-going input threshold voltage	RIN	V _{CC} = 5V T _A = 25°C	0.8	1.2		V
V _{hys}	Input hysteresis voltage	RIN	V _{CC} = 5V	0.2	0.5	1	V
r _i	Receiver input resistance	RIN	V _{CC} = 5V T _A = 25°C	3	5	7	kΩ

- (1) Test conditions are C1 – C4 = 1μF at V_{CC} = 5V ± 0.5V.
- (2) All typical values are at V_{CC} = 5V and T_A = 25°C.

5.8 Switching Characteristics: Driver

$V_{CC} = 5V$, $T_A = 25^\circ C$

PARAMETER		TEST CONDITIONS ⁽¹⁾	MIN	TYP	MAX	UNIT
SR	Driver slew rate	$R_L = 3k\Omega$ to $7k\Omega$, See 6-2			30	V/ μ s
SR(t)	Driver transition region slew rate	$R_L = 3k\Omega$, $C_L = 2.5nF$ See 6-3		3		V/ μ s
	Data rate	One DOUT switching		250		kbit/s

(1) Test conditions are $C1 - C4 = 1\mu F$ at $V_{CC} = 5V \pm 0.5V$.

5.9 Switching Characteristics: Receiver

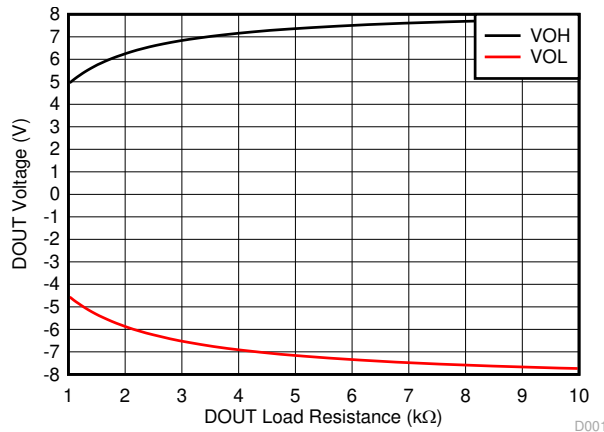
$V_{CC} = 5V$, $T_A = 25^\circ C$ (see [6-1](#))

PARAMETER		TEST CONDITIONS ⁽¹⁾	TYP	UNIT
$t_{PLH(R)}$	Receiver propagation delay time, low- to high-level output	$C_L = 50pF$	500	ns
$t_{PHL(R)}$	Receiver propagation delay time, high- to low-level output	$C_L = 50pF$	500	ns

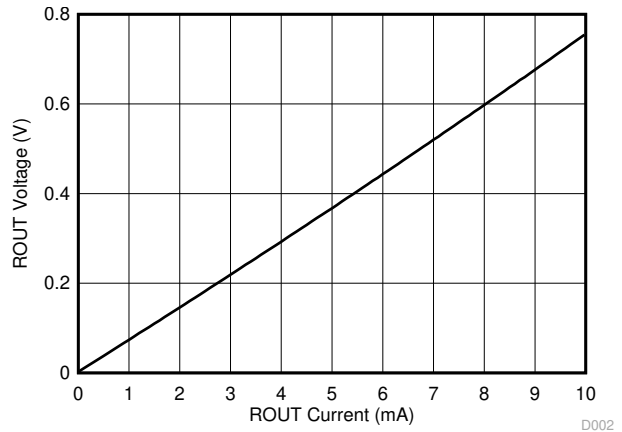
(1) Test conditions are $C1 - C4 = 1\mu F$ at $V_{CC} = 5V \pm 0.5V$.

5.10 Typical Characteristics

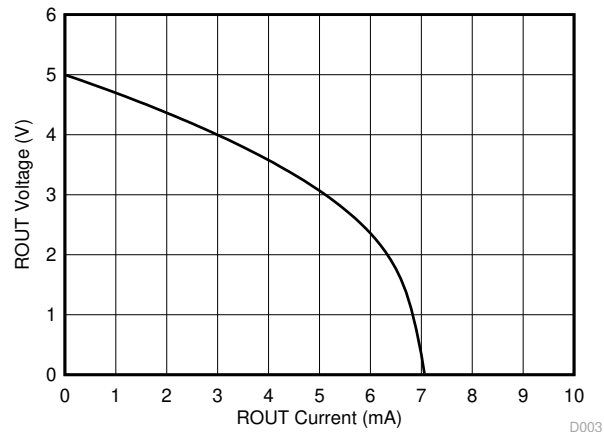
T_A = 25 °C



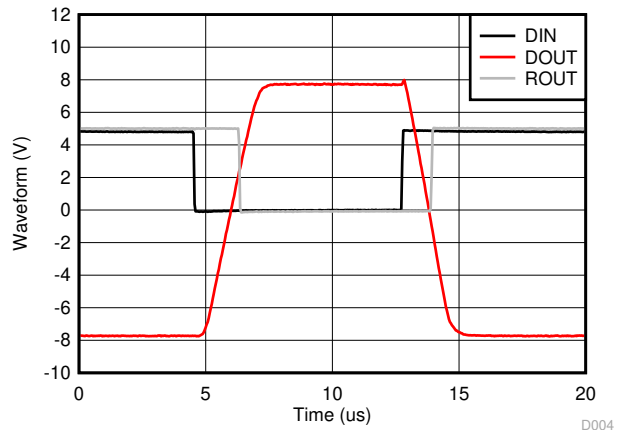
5-1. Driver Output Voltage vs Load Resistance



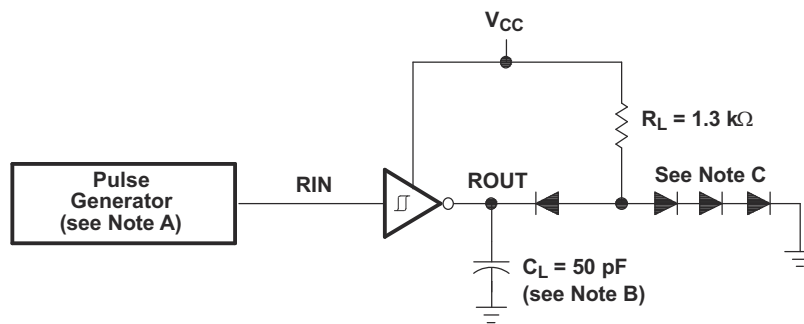
5-2. Receiver Low Output Voltage vs Load Current



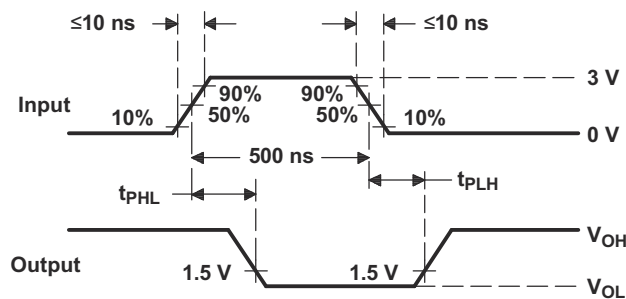
5-3. Receiver High Output Voltage vs Load Current



5-4. Loopback Waveforms Data Rate 120 kbit/s



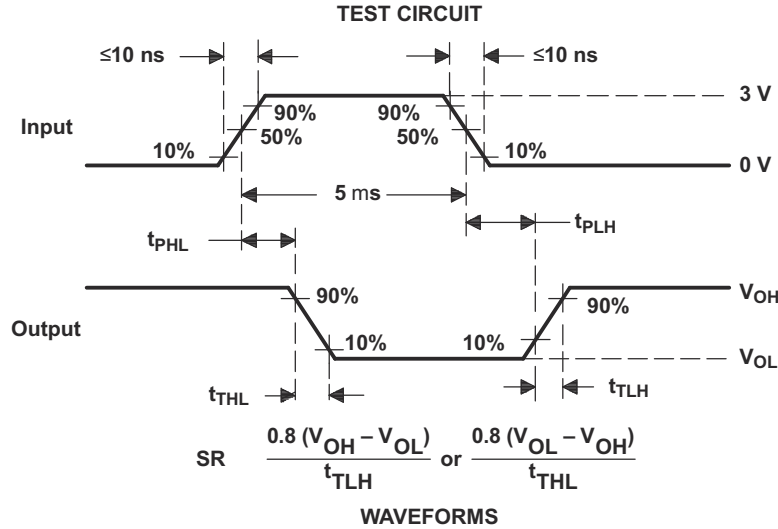
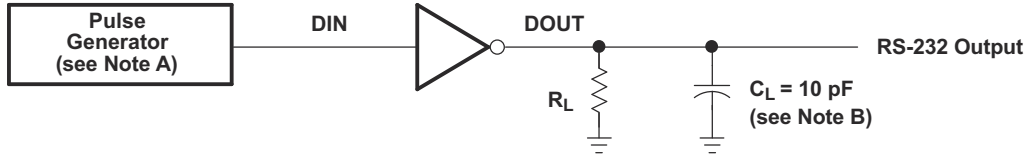
TEST CIRCUIT



WAVEFORMS

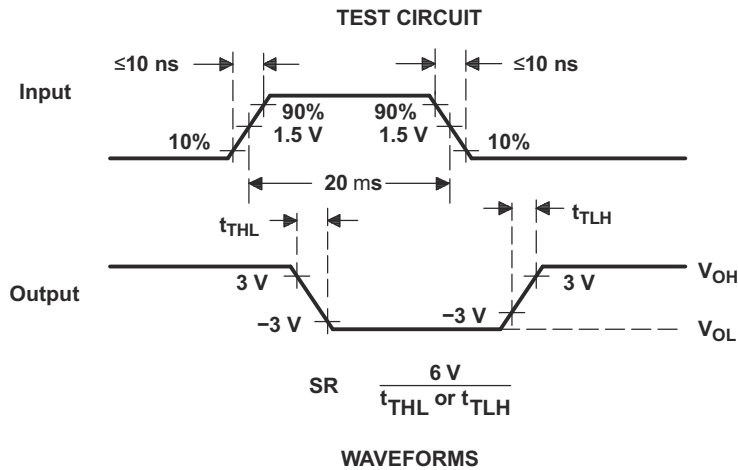
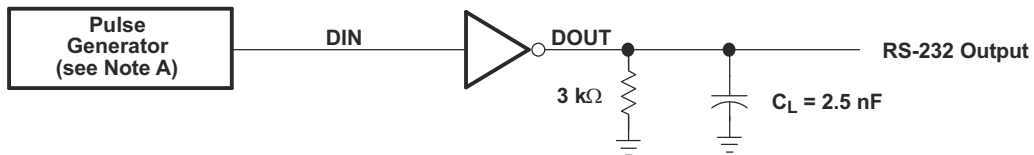
- A. The pulse generator has the following characteristics: $Z_O = 50\Omega$, duty cycle $\leq 50\%$.
- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N3064 or equivalent.

图 6-1. Receiver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurements



- A. The pulse generator has the following characteristics: $Z_O = 50\Omega$, duty cycle $\leq 50\%$.
- B. C_L includes probe and jig capacitance.

6-2. Driver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurements (5- μ s Input)



- A. The pulse generator has the following characteristics: $Z_O = 50\Omega$, duty cycle $\leq 50\%$.

6-3. Test Circuit and Waveforms for t_{THL} and t_{TLH} Measurements (20- μ s Input)

6 Detailed Description

6.1 Overview

The MAX232E is a dual driver and receiver that includes a capacitive voltage generator using four capacitors to supply TIA/EIA-232-F voltage levels from a single 5V supply. All RS-232 pins have 15kV HBM and IEC61000-4-2 Air-Gap discharge protection. RS-232 pins also have 8kV IEC61000-4-2 contact discharge protection. Each receiver converts TIA/EIA-232-F inputs to 5V TTL/CMOS levels. These receivers have shorted and open fail safe. The receiver can accept up to $\pm 30\text{V}$ inputs and decode inputs as low as $\pm 3\text{V}$. Each driver converts TTL/CMOS input levels into TIA/EIA-232-F levels. Outputs are protected against shorts to ground.

6.2 Functional Block Diagram

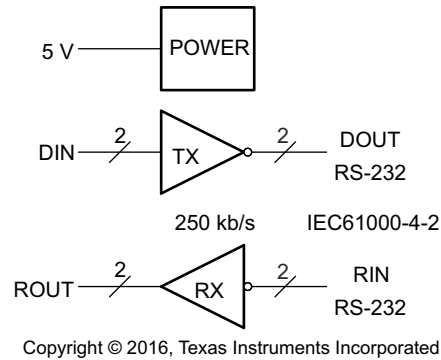


图 6-1. Logic Diagram (Positive Logic)

6.3 Feature Description

6.3.1 Power

The power block increases and inverts the 5V supply for the RS-232 driver using a charge pump that requires four $1\mu\text{F}$ external capacitors.

6.3.2 RS-232 Driver

Two drivers interface standard logic level to RS-232 levels. Internal pullup resistors on DIN inputs ensures a high input when the line is high impedance.

6.3.3 RS-232 Receiver

Two receivers interface RS-232 levels to standard logic levels. An open or shorted to ground input results in a high output on ROUT.

6.4 Device Functional Modes

6.4.1 V_{CC} Powered by 5V

The device is in normal operation.

6.4.2 V_{CC} Unpowered

When MAX232E is unpowered, it can be safely connected to an active remote RS-232 device.

6.4.3 Truth Tables

表 6-1 and 表 6-2 list the functions of this device.

表 6-1. Function Table for Each Driver

INPUT DIN ⁽¹⁾	OUTPUT DOUT
L	H
H	L

(1) H = high level, L = low level

表 6-2. Function Table for Each Receiver

INPUT RIN ⁽¹⁾	OUTPUT ROUT
L	H
H	L
Open	H

(1) H = high level, L = low level, Open = input disconnected or connected driver off

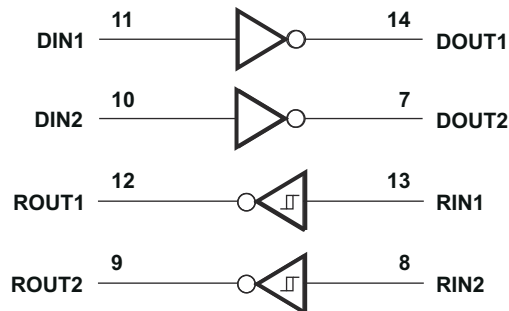


図 6-2. Logic Diagram (Positive Logic)

7 Applications and Implementation

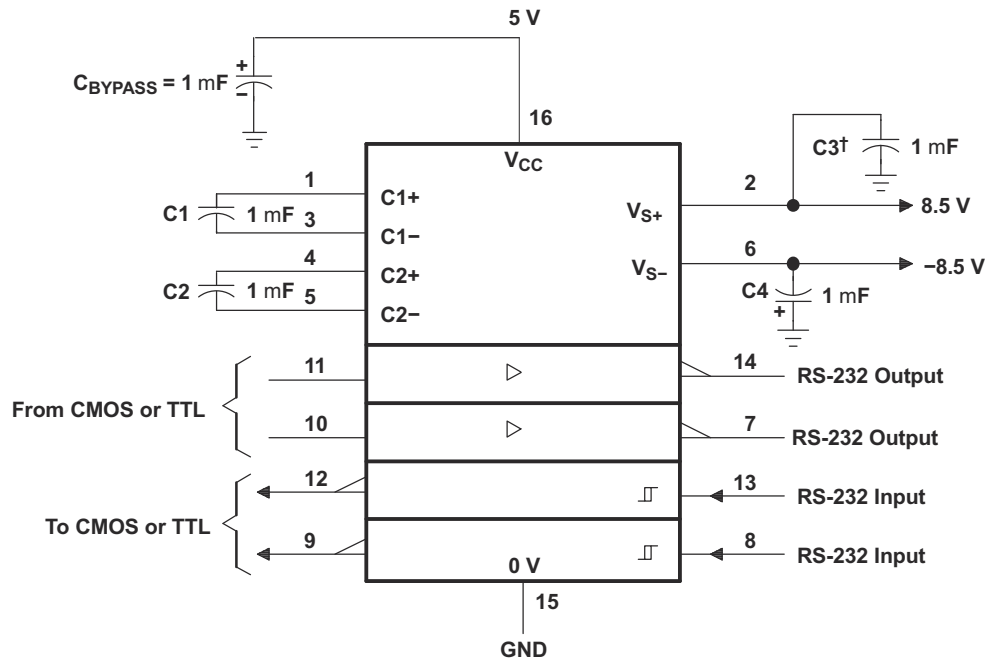
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7.1 Application Information

For proper operation add capacitors as shown in [図 7-1](#). Pins 9 through 12 connect to UART or general purpose logic lines. RS-232 lines on pins 7, 8, 13, and 14 connect to a connector or cable.

7.2 Typical Application



† C3 can be connected to V_{CC} or GND.

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Resistor values shown are nominal.

Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

図 7-1. Typical Operating Circuit

7.2.1 Design Requirements

- V_{CC} minimum is 4.5V and maximum is 5.5V.
- Maximum recommended bit rate is 250kbit/s.

7.2.2 Detailed Design Procedure

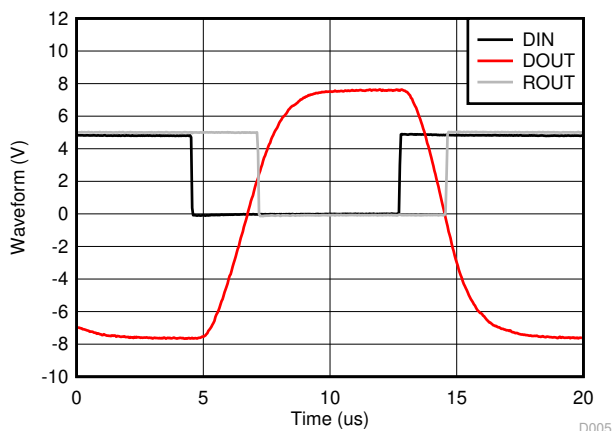
The capacitor type used for C1–C4 is not critical for proper operation. The MAX232E requires 1 μ F capacitors, although capacitors up to 10 μ F can be used without harm. Ceramic dielectrics are suggested for capacitors. When using the minimum recommended capacitor values, make sure the capacitance value does not degrade excessively as the operating temperature varies. If in doubt, use capacitors with a larger (for example, 2 \times) nominal value. The capacitors' effective series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on V+ and V–.

Use larger capacitors (up to 10 μ F) to reduce the output impedance at V_{S+} and V_{S–}.

Bypass V_{CC} to ground with at least 1 μ F. In applications sensitive to power-supply noise generated by the charge pumps, decouple V_{CC} to ground with a capacitor the same size as (or larger than) the charge-pump capacitors (C1–C4).

7.2.3 Application Curve

Loopback waveform connects DOUT to RIN.



Date Rate = 120 kbit/s, C_L = 1 nF

图 7-2. Loopback Waveforms

7.3 Power Supply Recommendations

The V_{CC} voltage should be connected to the same power source used for logic device connected to DIN and ROUT pins. V_{CC} should be between 4.5V and 5.5V.

7.4 Layout

7.4.1 Layout Guidelines

Keep the external capacitor traces short. This is more important on C1 and C2 nodes that have the fastest rise and fall times. Make the impedance from MAX232E ground pin and circuit board ground plane as low as possible for best ESD performance. Use wide metal and multiple vias on both sides of ground pin.

7.4.2 Layout Example

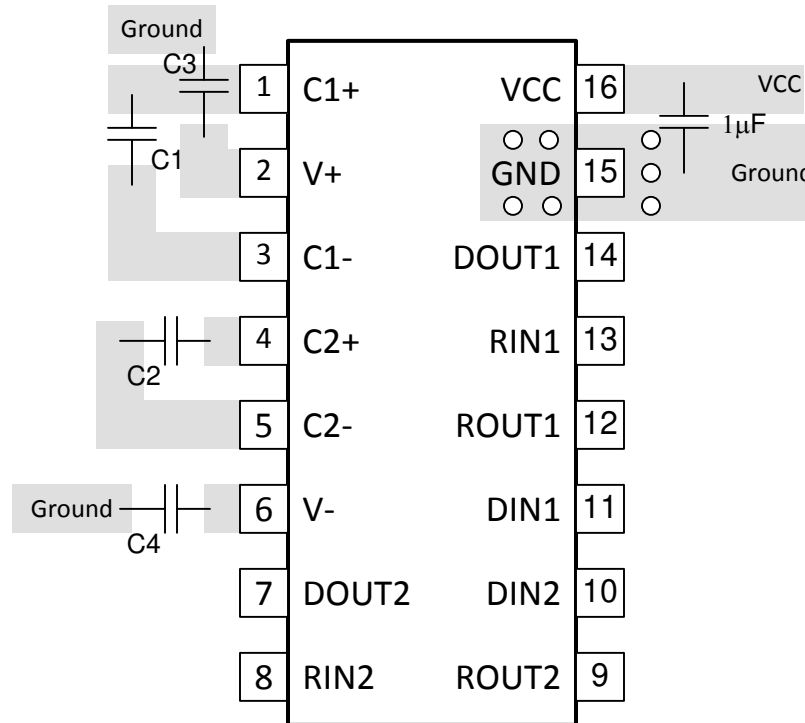


図 7-3. MAX232E Layout

8 Device and Documentation Support

8.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

8.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

8.4 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい ESD 対策をとらないと、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.5 用語集

TI 用語集 この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (August 2016) to Revision D (February 2024)	Page
• 「製品情報」表を「パッケージ情報」表に変更.....	1
• Changed the <i>Thermal Information</i> table.....	5

Changes from Revision B (November 2009) to Revision C (August 2016)	Page
• 「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加。.....	1
• 「特長」から「±30V 入力レベル」を削除.....	1
• 「注文情報」表を削除 (データシートの末尾にある POA を参照).....	1
• Added MIN value ±3 to "Receiver input voltage (RIN1, RIN2) row in <i>Recommended Operating Conditions</i> ...	4
• Changed R _{θJA} values in <i>Thermal Information</i>	5
• Deleted table note 3 from <i>Receiver Section Electrical Characteristics</i>	5
• Added a new row to the <i>Function Table for Each Receiver</i>	11

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MAX232ECD	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	0 to 70	MAX232EC	
MAX232ECDR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX232EC	Samples
MAX232ECDW	OBSOLETE	SOIC	DW	16		TBD	Call TI	Call TI	0 to 70	MAX232EC	
MAX232ECDWR	OBSOLETE	SOIC	DW	16		TBD	Call TI	Call TI	0 to 70	MAX232EC	
MAX232ECDWRG4	OBSOLETE	SOIC	DW	16		TBD	Call TI	Call TI	0 to 70	MAX232EC	
MAX232ECPW	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	0 to 70	MA232EC	
MAX232ECPWR	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	0 to 70	MA232EC	
MAX232ECPWRG4	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	0 to 70	MA232EC	
MAX232EID	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 85	MAX232EI	
MAX232EIDR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX232EI	Samples
MAX232EIDW	OBSOLETE	SOIC	DW	16		TBD	Call TI	Call TI	-40 to 85	MAX232EI	
MAX232EIDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX232EI	Samples
MAX232EIN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	MAX232EIN	Samples
MAX232EINE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	MAX232EIN	Samples
MAX232EIPW	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-40 to 85	MB232EI	
MAX232EIPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB232EI	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX232ECDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MAX232ECDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MAX232EIDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MAX232EIDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
MAX232EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MAX232EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MAX232ECDR	SOIC	D	16	2500	340.5	336.1	32.0
MAX232ECDR	SOIC	D	16	2500	333.2	345.9	28.6
MAX232EIDR	SOIC	D	16	2500	353.0	353.0	32.0
MAX232EIDWR	SOIC	DW	16	2000	350.0	350.0	43.0
MAX232EIPWR	TSSOP	PW	16	2000	353.0	353.0	32.0
MAX232EIPWR	TSSOP	PW	16	2000	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
MAX232EIN	N	PDIP	16	25	506	13.97	11230	4.32
MAX232EINE4	N	PDIP	16	25	506	13.97	11230	4.32

GENERIC PACKAGE VIEW

DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

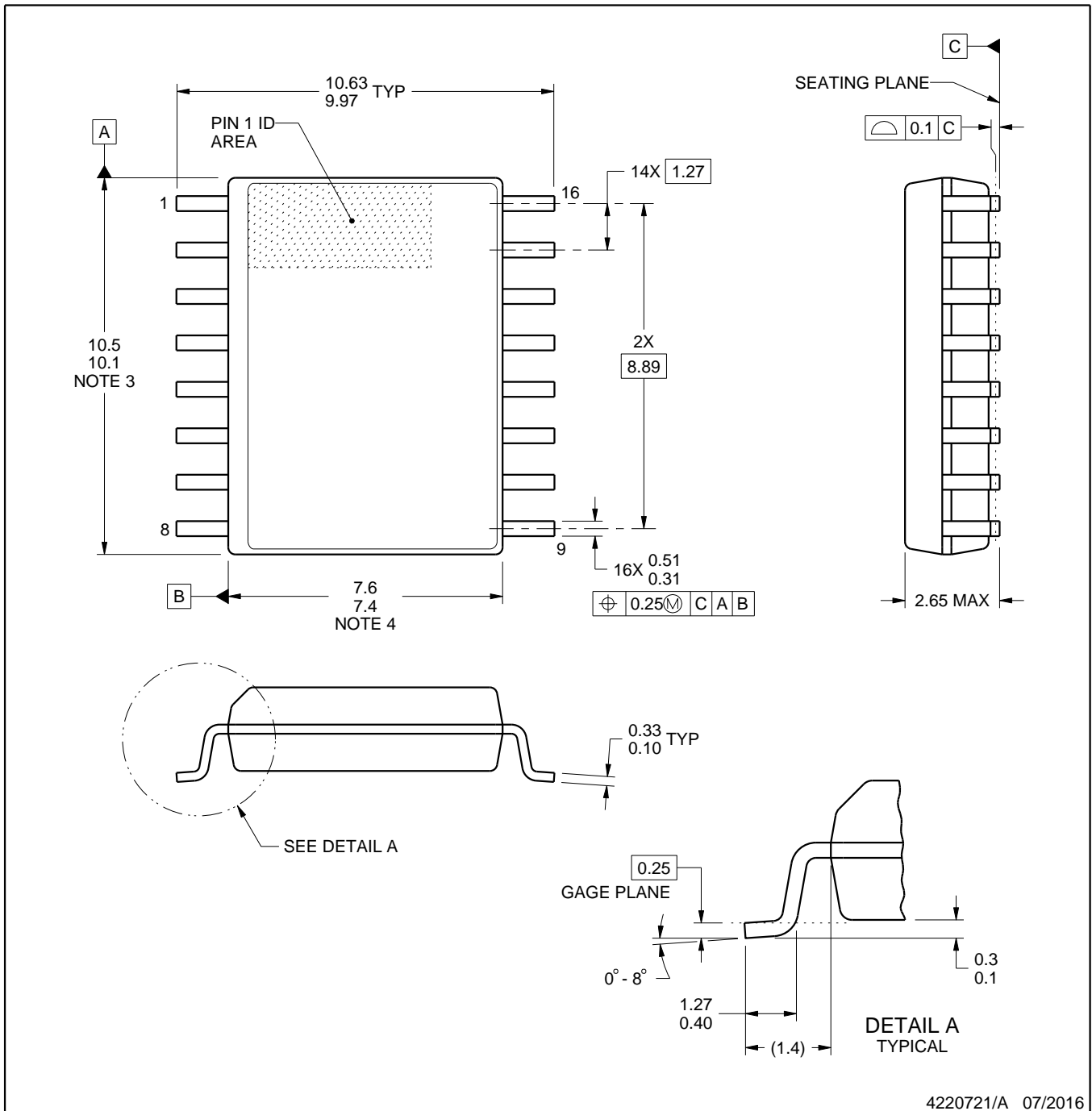


DW0016A

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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