OPA1632 高性能、完全差動オーディオ・オペアンプ

1 特長

- 優れた音質
- 超低歪:0.000028%
- 低ノイズ:1.25nV/√Hz
- 高速:
  - スルーレート:72V/μs
  - ゲイン帯域幅積:180MHz
- 完全差動アーキテクチャ:
  - シングルエンド入力を平衡型の差動出力に変換する平衡型入力および出力
- 広い電源電圧範囲:±2.5V～±15V
- シャットダウン電流:0.85mA (V_S = ±5V)
- 温度範囲:–40℃～+85℃

2 アプリケーション

- 業務用オーディオ・ミキサまたは制御卓
- 業務用マイク / ワイヤレス・システム
- 業務用スピーカ・システム
- 業務用オーディオ・アンプ
- サウンドバー
- ターンテーブル
- 業務用ビデオ・カメラ
- ギターおよびその他楽器用アンプ
- データ・アクイジション (DAQ)

3 概要

OPA1632 は、高性能オーディオ A/D コンバータ (ADC) を駆動するために、または D 級アンプ用プリドライバとして設計された完全差動アンプ (FDA) です。

OPA1632 は優れた音質、超低ノイズ、大きな出力電圧振幅、大電流駆動を実現します。OPA1632 は、180MHz の優れたゲイン帯域幅と、超低歪みの実現に役立つ 72V/μs の超高速スルーレートを備えています。さらに、1.25nV/√Hz の非常に小さい入力電圧ノイズにより、最大限の信号対雑音比とダイナミック・レンジを確保できます。

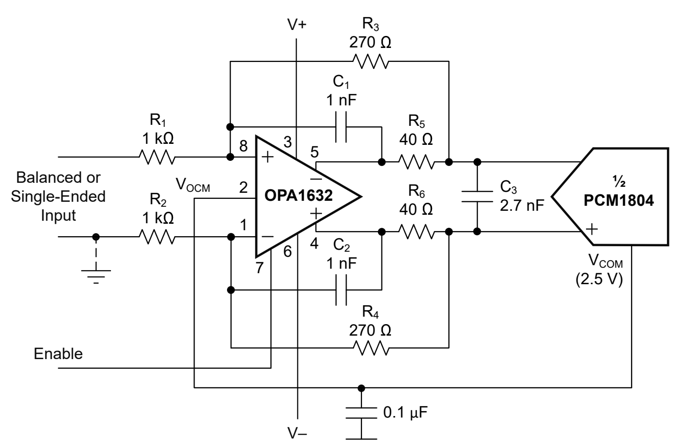
完全差動アーキテクチャの柔軟性を利用すると、シングルエンドから完全差動への出力変換を簡単に実装できます。差動出力は、偶数次の高調波を低減し、同相モード・ノイズによる干渉を最小化します。PCM1804 などの高性能オーディオ ADC を駆動するために使用する際、OPA1632 は優れた性能を発揮します。待機時の電力を節約するため、シャットダウン機能が備わっています。

OPA1632 は、−40℃～+85℃で動作し、SO-8 パッケージと放熱特性の優れた HVSSOP-8 PowerPAD™ IC パッケージで供給されます。

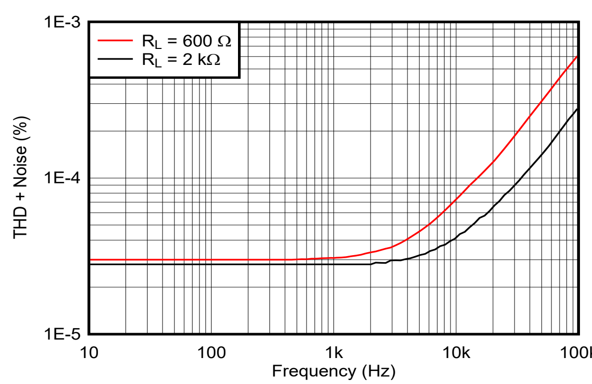
パッケージ情報

部品番号	パッケージ (1)	パッケージ・サイズ (2)
OPA1632	D (SOIC、8)	4.9mm × 6mm
	DGN (HVSSOP、8)	3mm × 4.9mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ・サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



アプリケーション図



THD + ノイズと周波数との関係

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (March 2022) to Revision E (August 2023) — **Page**

- MSOP パッケージのすべてのインスタンスを VSSOP パッケージに変更、MSOP PowerPAD のすべてのインスタンスを HVSSOP に変更.......... 1
- Changed ambient temperature in Recommended Operating Conditions to show only −40°C to +85°C.......... 6
- Changed thermal specifications for DGN package in Thermal Information table.......... 6
- Changed Electrical Characteristics (EC) to combine both tables in to one table for both packages.......... 8
- Changed PSRR minimum limit of 316 μV/V to maximum limit in EC table for DGN package.......... 8
- Changed input offset drift, input voltage noise, small and large signal bandwidth, slew rate, rise and fall time, settling time, output voltage swing, and closed-loop output impedance to show improved values.......... 8
- Changed typical and maximum input bias current from 2 μA to 7.9 μA and 6 μA to 14 μA, respectively for DGN package.......... 8
- Changed input current noise from 0.4 pA/√Hz to 1.7 pA/√Hz in EC table for DGN package.......... 8
- Changed input impedance spec to show both common-mode and differential impedances in EC table for DGN package.......... 8
- Changed typical THD+N with differential input/output and R_L = 2 kΩ from 0.000022% to 0.000028% in EC table for DGN package.......... 8
- Changed IMD of differential input/output and R_L = 2 kΩ from 0.00005% to 0.000061% in EC table for DGN package.......... 8
- Changed voltage output swing low and high to a typical only for a load of 2 kΩ in the EC table for DGN package.......... 8
- Changed the enable and disable voltage threshold from (V−) + 2 V and (V−) 0.8 V to (V−) + 1.45 V and (V−) 1.4 V, respectively, for DGN package.......... 8
- Changed one Turn-on delay specification to Turn-off delay in Electrical Characteristics table.......... 8
- Deleted the DGN Typical Characteristics section and combined all plots into one section.......... 10

Changes from Revision C (September 2015) to Revision D (March 2022) — **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新.......... 1
- 「特長」セクションを更新.......... 1
- 「アプリケーション」セクションを更新.......... 1
- 「概要」セクションを更新.......... 1
- 「概要」セクションの SOIC および MSOP-PowerPAD パッケージ両方の本体サイズの公称値を変更.......... 1

- Updated *Pin Configuration and Functions* section....5
- Added Supply turn-on/off dV/dT specification to Absolute Maximum Ratings table....6
- Added continuous input current specification to Absolute Maximum Ratings table....6
- Changed differential input voltage in Absolute Maximum Ratings table from ±3V to ±1.5V 6
- Changed charged-device model (CDM) reference from JESD22-C101 to JS-002 in ESD Ratings table....6
- Changed minimum temperature range from 0.4℃ to -40℃ in Recommended Operating Conditions table....6
- Changedthermal specifications for D package in Thermal Information table....6
- Changed RθJA from 114.5°C/W to 126.3°C/W for D Package in Thermal Information table....6
- Changed RθJC(top) from 60.3°C/W to 67.3°C/W for D package in Thermal Information table....6
- Changed RθJB from 54.8°C/W to 69.8°C/W for D package in Thermal Information table....6
- Changed ψJT from 14°C/W to 19.5°C/W for D package in Thermal Information table....6
- Changed ψJT from 54.3°C/W to 69.0°C/W for D package in Thermal Information table....6
- Changed typical offset voltage vs temperature from ±5 µV°C to ± 2.5 µV°C in *Electrical Characteristics: OPA1632D* table....8
- Changed PSRR minimum limit of 316 µV/V to maximum limit in *Electrical Characteristics: OPA1632D table* 8
- Changed typical input bias current limit from 2 µA to 7.9 µA in *Electrical Characteristics: OPA1632D* table....8
- Changed Max input bias current limit from 6µA to 14µA in *Electrical Characteristics: OPA1632D* table....8
- Changed typical input voltage noise from 1.3nV/√Hz to 1.25nV/√Hz in Electrical Characteristics: OPA1632D table....8
- Changed typical input current noise from 0.4 pA/√Hz to 1.7 pA/√Hz in *Electrical Characteristics: OPA1632D* table....8
- Changed input impedance spec to show both common-mode and differential impedances in *Electrical Characteristics: OPA1632D* table....8
- Changed SSBW at G = +2, R_F = 602 Ω from 90 MHz to 104 MHz in *Electrical Characteristics: OPA1632D* table....8
- Changed SSBW at G = +5, R_F = 1.5 kΩ from 36 MHz to 46 MHz in *Electrical Characteristics: OPA1632D* table....8
- Changed SSBW at G = +10, R_F = 3.01 kΩ from 18 MHz to 24 MHz in *Electrical Characteristics: OPA1632D* table....8
- Changed typical Large-Signal Bandwidth from 800 kHz to 1.8 MHz in *Electrical Characteristics: OPA1632D* table....8
- Changed typical slew rate from 50 V/µs to 72 V/µs in *Electrical Characteristics: OPA1632D* table 8
- Changed typical rise/fall time from 100 ns to 69 ns in *Electrical Characteristics: OPA1632D* table....8
- Changed typical settling time to 0.1% from 75 ns to 36 ns in *Electrical Characteristics: OPA1632D* table....8
- Changed typical settling time to 0.01% from 200 ns to 49ns in *Electrical Characteristics: OPA1632D* table 8
- Changed typical THD+N with Differential Input/Output and R_L = 600 Ω from 0.0003% to 0.00003% in *Electrical Characteristics: OPA1632D* table....8
- Changed typical THD+N with Differential Input/Output and RL = 2 kΩ from 0.000022% to 0.000028% in Electrical Characteristics: OPA1632D table 8
- Changed typical THD+N with single-ended Input/Output and RL = 600Ω from 0.000059% to 0.000036% in *Electrical Characteristics: OPA1632D* table 8
- Changed typical THD+N with single-ended Input/Output and RL = 2 kΩ from 0.000043% to 0.000031% in Electrical Characteristics: OPA1632D table....8
- Changed IMD at diferrential input/output and R_L= 600Ω from 0.00008% to 0.000061% in *Electrical Characteristics: OPA1632D* table....8
- Changed IMD at diferrential input/output and RL= 2 kΩ from 0.00005% to 0.000061% in Electrical Characteristics: OPA1632D table 8
- Changed IMD at single-ended input/output and R_L= 600Ω from 0.0001% to 0.00007% in *Electrical Characteristics: OPA1632D* table 8

- Changed IMD at single-ended input/output and RL= 2kΩ from 0.0007% to 0.000073% in Electrical Characteristics: OPA1632D table 8
- Removed specified operating voltage specifications from *Electrical Characteristics: OPA1632D* table 8
- Changed typical I_Q from 14mA to 13mA in *Electrical Characteristics: OPA1632D* table.......... 8
- Added new Typical Characteristics section for D package.......... 10
- Updated *Feature Description* section.......... 13
- Updated *Output Common-Mode Voltage* section.......... 14
- Updated *Resistor Matching* section.......... 14
- Updated *Application Curves* section.......... 16
- Updated *Power Supply Recommendations* section.......... 16
- Updated the *Power Dissipation and Thermal Considerations* section.......... 18
- Updated *Layout Example* section.......... 19
- Changed list of documentation in *Related Documentation* section.......... 20

Changes from Revision B (January 2010) to Revision C (September 2015) **Page**

- 「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加。.......... 1

5 Pin Configuration and Functions

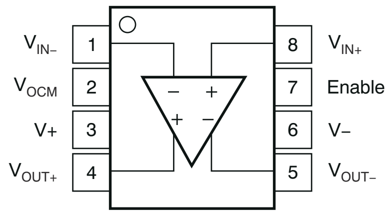


図 5-1. D Package, 8-Pin SOIC or DGN Package[(1)], 8-Pin HVSSOP (Top View)

表 5-1. Pin Functions

PIN		TYPE[(2)]	DESCRIPTION
NAME	NO.		
Enable	7	I	Active high enable pin
V+	3	I/O	Positive supply voltage pin
V–	6	I/O	Negative supply voltage pin
V_{IN+}	8	I	Positive input voltage pin
$V_{IN–}$	1	I	Negative input voltage pin
V_{OCM}	2	I	Output common-mode control voltage pin
V_{OUT+}	4	O	Positive output voltage pin
$V_{OUT–}$	5	O	Negative output voltage pin

(1) Solder the exposed DGN (HVSSOP) package thermal pad to a heat-spreading power or ground plane. This pad is electrically isolated from the die, but must be connected to a power or ground plane and not floated.
(2) I = input, O = output.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)] [(2)]

		MIN	MAX	UNIT
V_S	Supply voltage		±16.5	V
	Supply turn on and turn off dV/dT[(3)]		1.7	V/μs
V_I	Input voltage		$\pm V_S$	V
I_O	Output current		150	mA
I_{IN}	Continuous input current		10	mA
V_{ID}	Differential input voltage		±1.5	V
T_J	Junction temperature		150	°C
T_A	Ambient temperature	–40	85	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The OPA1632 HVSSOP PowerPAD integrated circuit package incorporates a thermal pad on the underside of the chip. This thermal pad acts as a heat sink and must be connected to a thermally-dissipative plane for proper power dissipation. Failure to do so can result in exceeding the maximum junction temperature, which can permanently damage the device. See TI technical brief SLMA002 for more information about using the thermally-enhanced PowerPAD integrated circuit package.
(3) Stay below this specification to make sure that the edge-triggered ESD absorption devices across the supply pins remain off.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±1000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[(2)]	±500	
		Machine model	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_S	Supply voltage	Dual	±2.5	±15	V
		Single	5	30	
T_A	Ambient temperature		−40	85	°C

6.4 Thermal Information

THERMAL METRIC[(1)]		OPA1632		UNIT
		D (SOIC)	DGN (HVSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	126.3	57.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.3	76.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	69.8	30.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	19.5	4.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	69.0	29.9	°C/W

THERMAL METRIC[1]		OPA1632		UNIT
		D (SOIC)	DGN (HVSSOP)	
		8 PINS	8 PINS	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	14.3	°C/W

(1) For information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

at V_S = ±15 V, R_F = 390 Ω, R_L = 800 Ω, and G = +1 (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE					
Input offset voltage			±0.5	±3	mV
Input offset voltage, vs temperature, dc, dV_{OS}/dT			±2.5		µV/°C
Input offset voltage, vs power supply, dc, PSRR			13	316	µV/V
INPUT BIAS CURRENT					
Input bias current, I_B			7.9	14	µA
Input offset current, I_{OS}			±100	±500	nA
NOISE					
Input voltage noise	f = 10 kHz		1.25		nV/√Hz
Input current noise	f = 10 kHz		1.7		pA/√Hz
INPUT VOLTAGE					
Common-mode input voltage		(V−) + 1.5		(V+) − 1	V
Common-mode rejection ratio, dc		74	90		dB
INPUT IMPEDANCE					
Input impedance	Measured into each input pin, common-mode		215 || 1.4		MΩ || pF
Input impedance	Measured into each input pin, differential		10 || 3.1		kΩ || pF
OPEN-LOOP GAIN					
Open-loop gain, dc		66	78		dB
FREQUENCY RESPONSE					
Small-signal bandwidth	G = +1, R_F= 348 Ω		180		MHz
Small-signal bandwidth	V_O = 100 mV_{PP}, peaking < 0.5 dB, G = +2, R_F = 602 Ω		104		MHz
Small-signal bandwidth	V_O = 100 mV_{PP}, peaking < 0.5 dB, G = +5, R_F = 1.5 kΩ		46		MHz
Small-signal bandwidth	V_O = 100 mV_{PP}, peaking < 0.5 dB, G = +10, R_F = 3.01 kΩ		24		MHz
Bandwidth for 0.1-dB flatness	G = +1, V_O = 100 mV_{PP}		40		MHz
Peaking at a gain of 1	V_O = 100 mV_{PP}		0.5		dB
Large-signal bandwidth	G = +2, V_O = 20 V_{PP}		1.8		MHz
Slew rate (25% to 75%)	G = +1		72		V/µs
Rise and fall time	G = +1, V_O = 5-V step		69		ns
Settling time, To 0.1%	G = +1, V_O = 2-V step		36		ns
Settling time, To 0.01%	G = +1, V_O = 2-V step		49		ns
Total harmonic distortion + noise, Differential input/output	G = +1, f = 1 kHz, V_O = 3 V_{RMS}, R_L = 600 Ω		0.00003%		
Total harmonic distortion + noise, Differential input/output	G = +1, f = 1 kHz, V_O = 3 V_{RMS}, R_L = 2 kΩ		0.000028%		
Total harmonic distortion + noise, Single-ended in/differential out	G = +1, f = 1 kHz, V_O = 3 V_{RMS}, R_L = 600 Ω		0.000036%		
Total harmonic distortion + noise, Single-ended in/differential out	G = +1, f = 1 kHz, V_O = 3 V_{RMS}, R_L = 2 kΩ		0.000031%		
Intermodulation distortion, Differential input/output	G = +1, SMPTE/DIN, V_O = 2 V_{PP}, R_L = 600 Ω		0.000061%		
Intermodulation distortion, Differential input/output	G = +1, SMPTE/DIN, V_O = 2 V_{PP}, R_L = 2 kΩ		0.000061%		
Intermodulation distortion, Single-ended in/differential out	G = +1, SMPTE/DIN, V_O = 2 V_{PP}, R_L = 600 Ω		0.000073%		
Intermodulation distortion, Single-ended in/differential out	G = +1, SMPTE/DIN, V_O = 2 V_{PP}, R_L = 2 kΩ		0.00007%		
Headroom	THD < 0.01%, R_L = 2 kΩ		20		V_{PP}

6.5 Electrical Characteristics (続き)

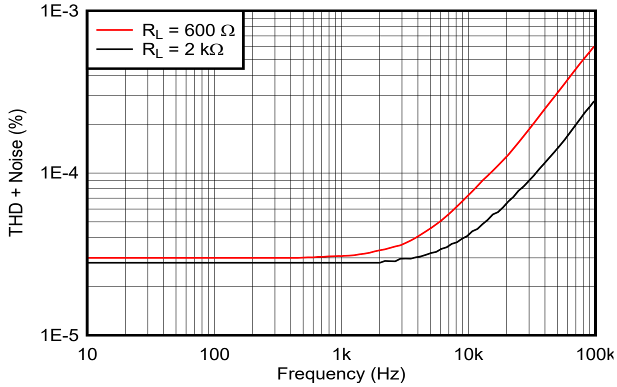
at V_S = ±15 V, R_F = 390 Ω, R_L = 800 Ω, and G = +1 (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT					
Voltage output swing low	R_L = 2 kΩ		(V−) + 1.6		V
	R_L = 1 kΩ			(V−) + 3.5	
Voltage output swing high	R_L = 2 kΩ		(V+) – 1.6		V
	R_L = 1 kΩ	(V+) – 3.5			
Short-circuit current, I_{SC}	Sourcing	50	85		mA
	Sinking	−60	–85		
Closed-loop output impedance	G = +1, f = 100 kHz		0.22		Ω
POWER DOWN					
Enable voltage threshold			(V−) + 1.45		V
Disable voltage threshold			(V−) + 1.4		V
Shutdown current(1)	V_S = ±5 V, V_{ENABLE} = −5 V		0.85		mA
	V_{ENABLE} = −15 V		1.7		
Turn-on delay	Time for I_Q to reach 50%		2		μs
Turn-off delay	Time for I_Q to reach 50%		2		μs
POWER SUPPLY					
Quiescent current, I_Q			13	17.1	mA

(1) Amplifier has internal 250-kΩ pullup resistor to V+ pin. This pullup resistor enables the amplifier with no connection to shutdown pin.

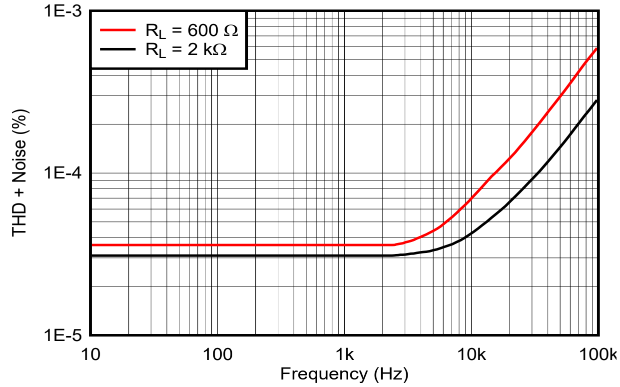
6.6 Typical Characteristics

at T_A = 25°C, V_S = ±15 V, R_F = 348 Ω, G = +1 and R_L = 2 kΩ (unless otherwise noted)



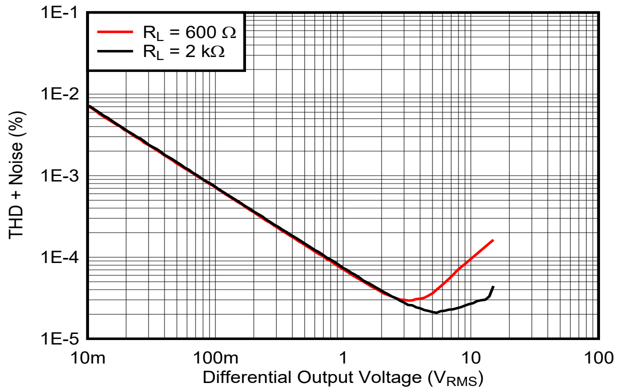
V_O = 3 V_{RMS}, differential input and output

図 6-1. THD + Noise vs Frequency



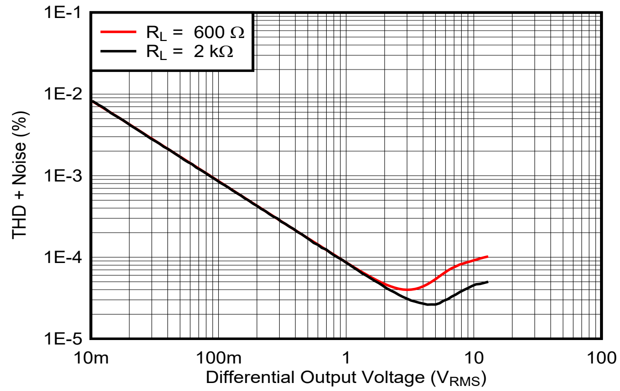
V_O = 3 V_{RMS}, single-ended input to differential output

図 6-2. THD + Noise vs Frequency



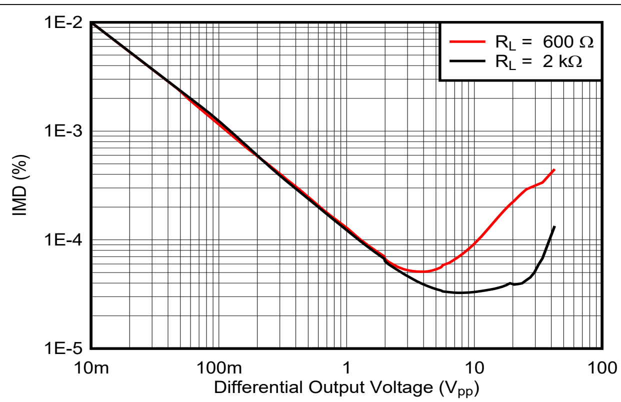
f = 1 kHz, differential input and output

図 6-3. THD + Noise vs Output Voltage



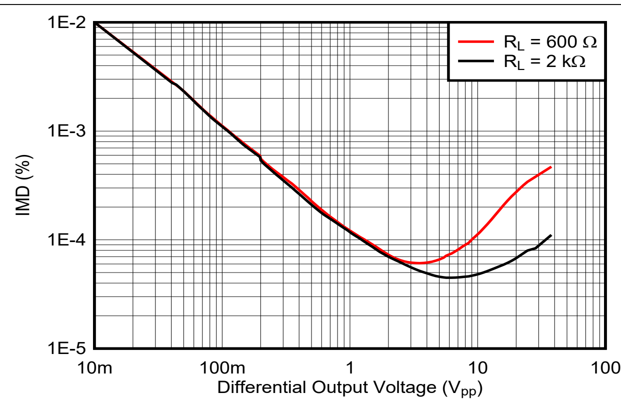
f = 1 kHz; single-ended input to differential output

図 6-4. THD + Noise vs Output Voltage



SMPTE 4:1: 60 Hz, 7 kHz; DIN 4:1: 250 Hz, 8 kHz, differential input and output

図 6-5. Intermodulation Distortion vs Output Voltage



SMPTE 4:1: 60 Hz, 7 kHz; DIN 4:1: 250 Hz, 8 kHz, differential input and output

図 6-6. Intermodulation Distortion vs Output Voltage

6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_F = 348 Ω, G = +1 and R_L = 2 kΩ (unless otherwise noted)

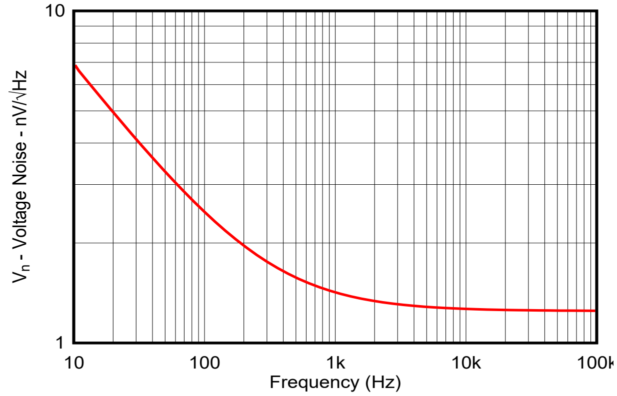


図 6-7. Voltage Noise vs Frequency

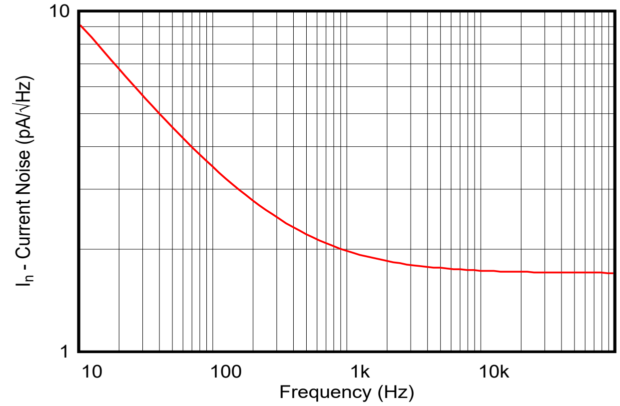
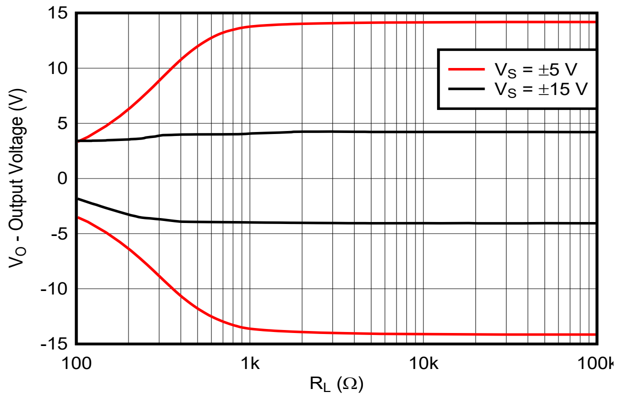


図 6-8. Current Noise vs Frequency



R_F= 1 kΩ, G = +2

図 6-9. Output Voltage vs Differential Load Resistance

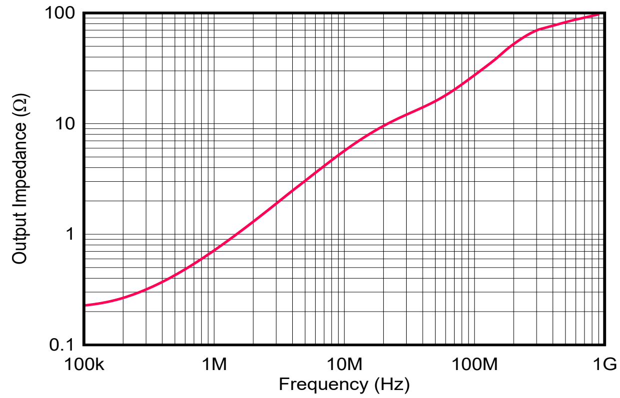


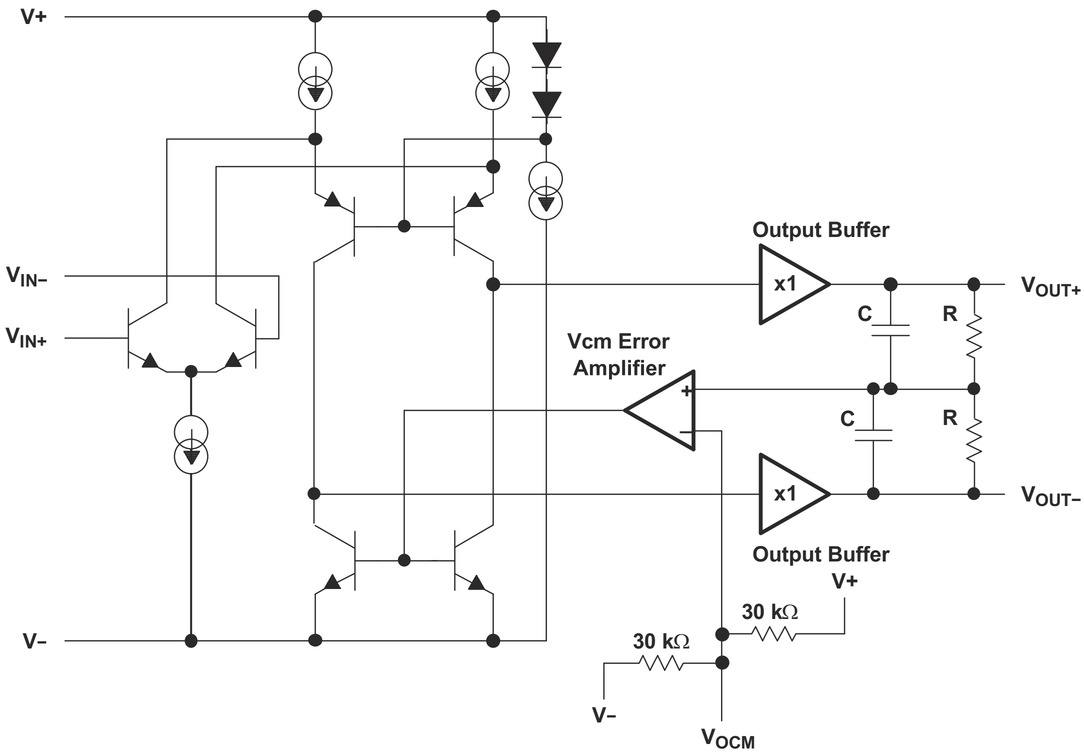
図 6-10. Output Impedance vs Frequency

7 Detailed Description

7.1 Overview

The OPA1632 is a fully differential amplifier (FDA). Differential signal processing offers a number of performance advantages in high-speed analog signal processing systems, including immunity to external common-mode noise, suppression of even-order nonlinearities, and increased dynamic range. FDAs not only serve as the primary means of providing gain to a differential signal chain, but also provide a monolithic solution for converting single-ended signals into differential signals allowing for easy, high-performance processing. For more information on the basic theory of operation for FDAs, refer to the *Fully Differential Amplifiers* application note

7.2 Functional Block Diagram



7.3 Feature Description

図 7-1 and 図 7-2 depict the differences between the operation of the OPA1632 in two different modes. FDAs can work with differential inputs or can be implemented as single input and differential output.

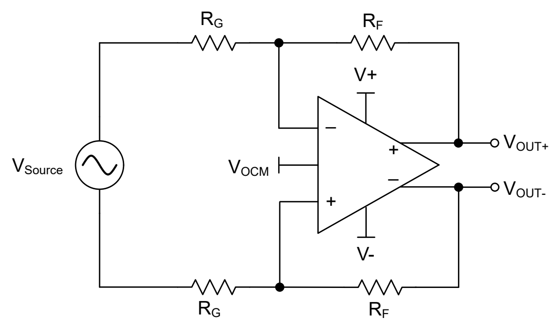


図 7-1. Amplifying Differential Input Signals

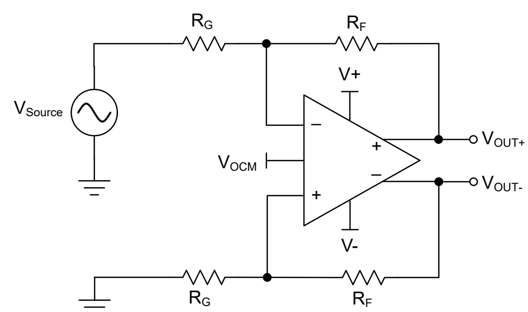


図 7-2. Amplifying Single-Ended Input Signals

7.4 Device Functional Modes

7.4.1 Shutdown Function

The shutdown (enable) function of the OPA1632 is referenced to the negative supply of the operational amplifier. A valid logic low (< 0.8 V above negative supply) applied to the enable pin (pin 7) disables the amplifier output. Voltages applied to pin 7 that are greater than 2 V above the negative supply place the amplifier output in an active state, and the device is enabled. If pin 7 is left disconnected, an internal pull-up resistor enables the device. Turn-on and turn-off times are approximately 2 μs each.

Quiescent current is reduced to approximately 0.85 mA when the amplifier is disabled. When disabled, the output stage is *not* in a high-impedance state. Thus, the shutdown function cannot be used to create a multiplexed switching function in series with multiple amplifiers.

8 Application and Implementation

注

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8.1 Application Information

8.1.1 Output Common-Mode Voltage

The output common-mode voltage pin sets the dc output voltage of the OPA1632. A voltage applied to the V_{OCM} pin from a low-impedance source can be used to directly set the output common-mode voltage. If left floating, the V_{OCM} pin defaults to the mid-rail voltage, defined as:

$$\frac{(V_+) + (V\_)}{2} \quad (1)$$

To minimize common-mode noise, connect a 0.1-uF bypass capacitor to the V_{OCM} pin. Output common-mode voltage causes additional current to flow in the feedback resistor network. This current is supplied by the output stage of the amplifier; therefore, additional power dissipation is created. For commonly-used feedback resistance values, this current is easily supplied by the amplifier. The additional internal power dissipation created by this current can be significant in some applications and can dictate use of the HVSSOP PowerPAD™ integrated circuit package to effectively control self-heating.

8.1.1.1 Resistor Matching

Resistor matching is important in FDAs to maintain good output balance. An ideal differential output signal implies the two outputs of the FDA should be exactly equal in amplitude and shifted 180° in phase. Any imbalance in amplitude or phase between the two output signals results in an undesirable common-mode signal at the output. The output balance error is a measure of how well the outputs are balanced and is defined as the ratio of the output common-mode voltage to the output differential signal.

$$Output\ Balance\ Error = \frac{\left(\frac{V_{OUT+} - V_{OUT-}}{2}\right)}{V_{OUT+} - V_{OUT-}} \quad (2)$$

At low frequencies, resistor mismatch is the primary contributor to output balance errors. Additionally CMRR, PSRR, and HD2 performance diminish if resistor mismatch occurs. Therefore, use 1% tolerance resistors or better to optimize performance. See 表 8-1 for recommended resistor values to use for a particular gain.

表 8-1. Recommended Resistor Values

GAIN (V/V)	R_G (Ω)	R_F (Ω)
1	390	390
2	374	750
5	402	2010
10	402	4020

8.2 Typical Application

図 8-1 shows the OPA1632 used as a differential-output driver for the PCM1804 high-performance audio ADC.

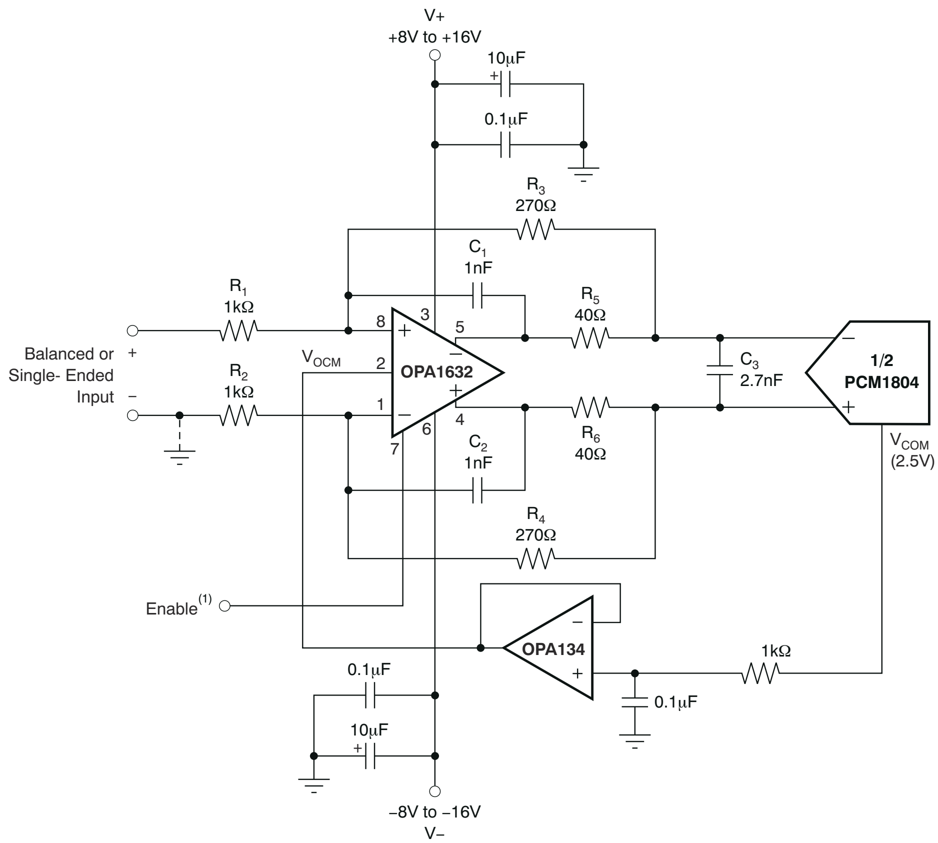

図 8-1. ADC Driver for Professional Audio

8.2.1 Design Requirements

表 8-2 shows example design parameters and values for the typical application design example in 図 7-1.

表 8-2. Design Parameters

DESIGN PARAMETERS	VALUE
Supply voltage	±2.5 V to ±15 V
Amplifier topology	Voltage feedback
Output control	DC-coupled with output common-mode control capability
Filter requirement	500-kHz, multiple-feedback low-pass filter

8.2.2 Detailed Design Procedure

Supply voltages of ±15 V are commonly used for the OPA1632. The relatively low input voltage swing required by the ADC allows use of lower power-supply voltage, if desired. Power supplies as low as ±8 V can be used in this application with excellent performance. Lower-voltage operation reduces power dissipation and heat rise. Bypass power supplies with 10-µF tantalum capacitors in parallel with 0.1-µF ceramic capacitors to avoid possible oscillations and instability.

The V_{COM} reference voltage output on the PCM1804 ADC provides the proper input common-mode reference voltage (2.5 V). This V_{COM} voltage is buffered with op amp A_2 and drives the output common-mode voltage pin of the OPA1632. This biases the average output voltage of the OPA1632 to 2.5 V.

The signal gain of the circuit is generally set to approximately 0.25 to be compatible with commonly-used audio line levels. Gain can be adjusted, if necessary, by changing the values of R_1 and R_2. Keep the feedback resistor values (R_3 and R_4) relatively low, as indicated, for best noise performance.

Resistors R_5 and R_6 and capacitor C_3 provide an input filter and charge glitch reservoir for the ADC. The values shown are generally satisfactory. Some adjustment of the values can help optimize performance with different ADCs.

Make sure to maintain accurate resistor matching on R_1/R_2 and R_3/R_4 to achieve good differential signal balance. Use 1% resistors for highest performance. When connected for single-ended inputs (inverting input grounded, as shown in 図 8-1), the source impedance must be low. Differential input sources must have well-balanced or low source impedance.

Choose capacitors C_1, C_2, and C_3 carefully for good distortion performance. Polystyrene, polypropylene, NPO ceramic, and mica types are generally excellent. Polyester and high-K ceramic types such as Z5U can create distortion.

8.2.3 Application Curves

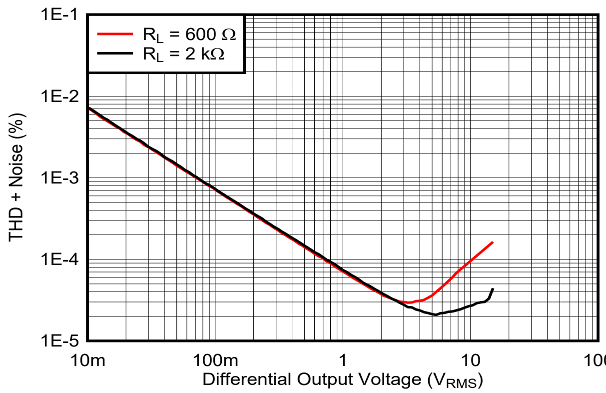

図 8-2. THD + Noise vs Output Voltage

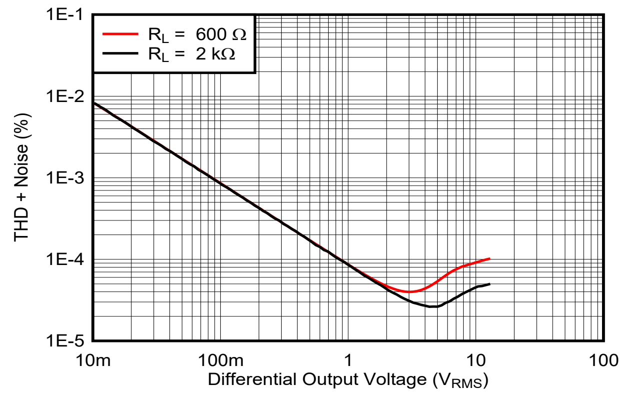

図 8-3. THD + Noise vs Output Voltage

8.3 Power Supply Recommendations

The OPA1632 device is designed to operate on power supplies ranging from ±2.5 V to ±15 V. Single power supplies ranging from 5 V to 30 V can also be used. Use a power-supply accuracy of 5%, or better. When operated on a board with high-speed digital signals, make sure to provide isolation between digital signal noise and the analog input pins. The OPA1632 is connected to power supplies through pin 3 (V_+) and pin 6 (V_-). Decouple each supply pin to GND as close to the device as possible with a low-inductance, surface-mount ceramic capacitor of approximately 10 nF. When vias are used to connect the bypass capacitors to a ground plane configure the vias for minimal parasitic inductance. One method of reducing via inductance is to use multiple vias. For broadband systems, two capacitors per supply pin are advised.

To avoid undesirable signal transients, do not power on the OPA1632 device with large inputs signals present. Careful planning of system power on sequencing is especially important to avoid damage to ADC inputs when an ADC is used in the application.

8.4 Layout

8.4.1 Layout Guidelines

1. The thermal pad is electrically isolated from the silicon and all leads. Connecting the thermal pad to any potential voltage between the power-supply voltages is acceptable, but best practice is to tie to ground because ground is generally the largest conductive plane.
2. Prepare the PCB with a top-side etch pattern as shown in 図 8-4. Use etch for the leads as well as etch for the thermal pad.

3. Place five holes in the area of the thermal pad that are 13 mils (0,03302 cm) in diameter. Keep these holes small so that solder wicking through the holes is not a problem during reflow.
4. Additional vias can be placed anywhere along the thermal plane outside of the thermal pad area. These vias help dissipate the heat generated by the OPA1632 device, and can be larger than the 13-mil diameter vias directly under the thermal pad. These vias can be larger because the vias are not in the thermal pad area to be soldered so that wicking is not a problem.
5. Connect all holes to the internal ground plane.
6. When connecting these holes to the plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This slow heat transfer makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, make sure the holes under the OPA1632 PowerPAD™ integrated circuit package connect to the internal plane with a complete connection around the entire circumference of the plated through-hole.
7. The top-side solder mask must leave the package pins and the thermal pad area with the five holes exposed. The bottom-side solder mask must cover the five holes of the thermal pad area. This configuration prevents solder from being pulled away from the thermal pad area during the reflow process.
8. Apply solder paste to the exposed thermal pad area and all of the device pins.

With these preparatory steps in place, the device is simply placed in position and runs through the solder reflow operation as any standard surface-mount component. This process results in a part that is properly installed.

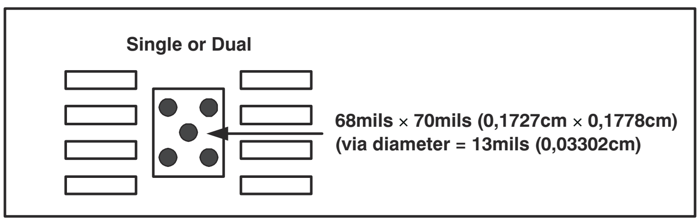

図 8-4. Thermal Pad PCB Etch and Via Pattern

8.4.1.1 PowerPAD™ Integrated Circuit Package Design Considerations

The OPA1632 is available in a thermally-enhanced PowerPAD™ integrated circuit package. This package is constructed using a downset leadframe upon which the die is mounted (see 図 8-5(a) and 図 8-5(b)). This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package (see 図 8-5(c)). Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

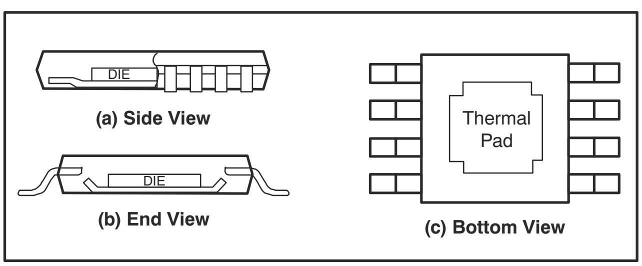

図 8-5. Views of the Thermally-Enhanced Package

The PowerPAD integrated circuit package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad must be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat-dissipating device. Soldering the thermal pad to the printed circuit board (PCB) is always required, even with applications that have low power dissipation. The thermal pad provides the necessary thermal and mechanical connection between the lead frame die pad and the PCB.

8.4.1.2 Power Dissipation and Thermal Considerations

The OPA1632 does not have thermal shutdown protection. Make sure that the maximum junction temperature is not exceeded. Excessive junction temperature can degrade performance or cause permanent damage. For best performance and reliability, make sure that the junction temperature does not exceed the absolute maximum ratings for the junction temperature.

The thermal characteristics of the device are dictated by the package and the circuit board. Maximum power dissipation for a given package can be calculated using the following formula:

$$P_{DMax} = \frac{T_{Max} - T_A}{\theta_{JA}}$$

where:

- P_{DMax} is the maximum power dissipation in the amplifier (W)
- T_{Max} is the absolute maximum junction temperature (°C)
- T_A is the ambient temperature (°C)
- $\theta_{JA} = \theta_{JC} + \theta_{CA}$
- θ_{JC} is the thermal coefficient from the silicon junctions to the case (°C/W)
- θ_{CA} is the thermal coefficient from the case to ambient air (°C/W)

For systems where heat dissipation is more critical, the OPA1632 is offered in an HVSSOP-8 (DGN) PowerPAD integrated circuit package. The thermal coefficient for the PowerPAD integrated circuit package is substantially improved over the traditional SO package. Maximum power dissipation levels are depicted in 図 8-6 for the two packages. The data for the DGN package assume a board layout that follows the layout guidelines listed in セクション 8.4.1.1.

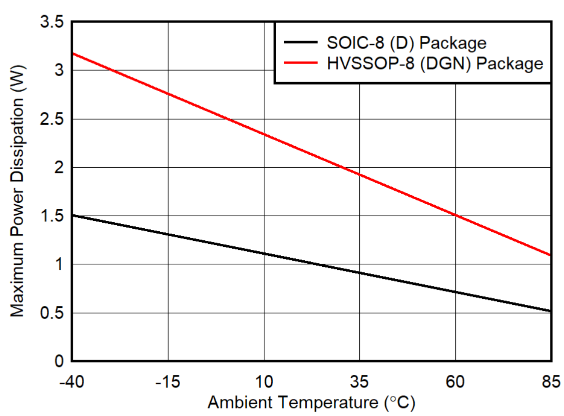

図 8-6. Maximum Power Dissipation vs Ambient Temperature

8.4.2 Layout Example

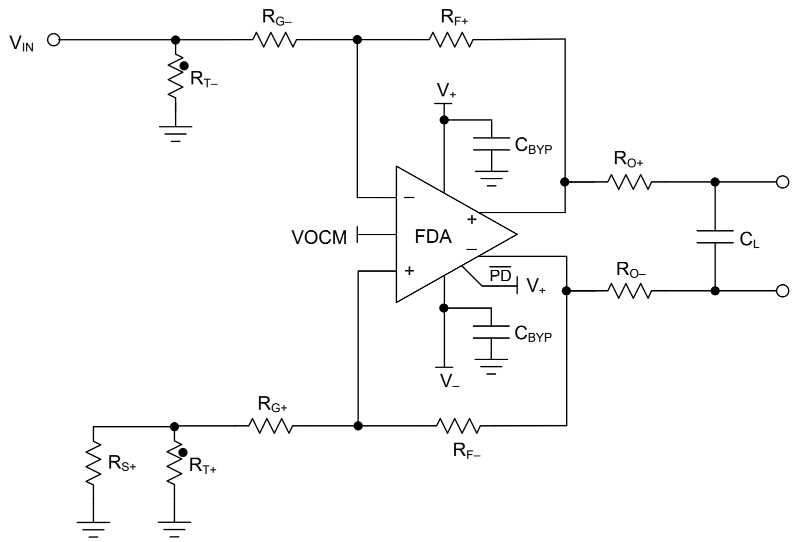

図 8-7. Representative Schematic for Example Layout

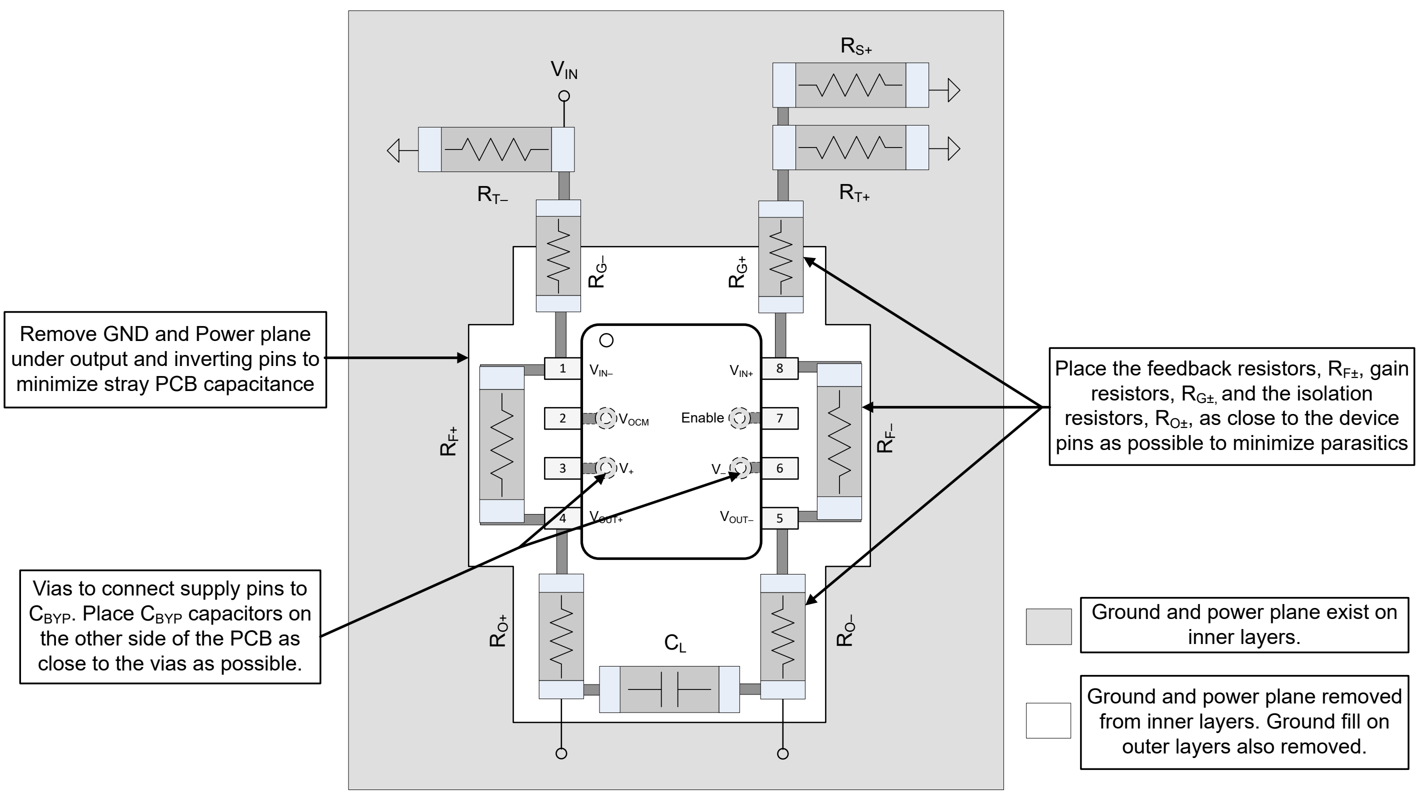

図 8-8. Example Layout

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Fully Differential Amplifiers* application note
- Texas Instruments, *TI Precision Labs - Fully Differential Amplifiers* video series
- Texas Instruments, *Maximizing Signal-Chain Distortion Performance Using High-Speed Amplifiers* application note
- Texas Instruments, *Analog Audio Amplifier Front-End Reference Design With Improved Noise and Distortion*
- Texas Instruments, *Public Announcement Audio Reference Design Utilizing Best in Class Boost Controller*
- Texas Instruments, *Motherboard/Controller for the AMC1210* reference design
- Texas Instruments, TPA6120A2 Stereo, 9.0-V to 33.0-V, Analog Input Headphone Amplifier With 128-dB Dynamic Range
- Texas Instruments, OPAx863 Low-Power, 110-MHz, Rail-to-Rail Input/Output Voltage-Feedback Op Amps
- Texas Instruments, OPA2834 50-MHz, 170-µA, Negative-Rail In, Rail-to-Rail Out, Voltage-Feedback Amplifier

9.2 ドキュメントの更新通知を受け取る方法

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9.3 サポート・リソース

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9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA1632D	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	OPA 1632	
OPA1632DG4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	OPA 1632	
OPA1632DGN	LIFEBUY	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	1632	
OPA1632DGNG4	LIFEBUY	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	1632	
OPA1632DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	1632	Samples
OPA1632DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	OPA 1632	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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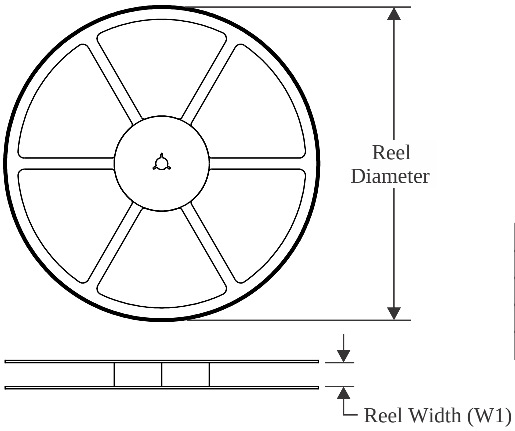
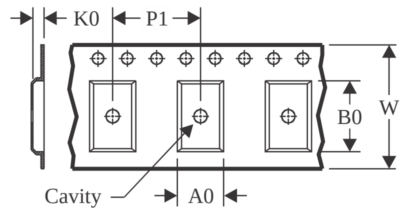
TAPE AND REEL INFORMATION

REEL DIMENSIONS

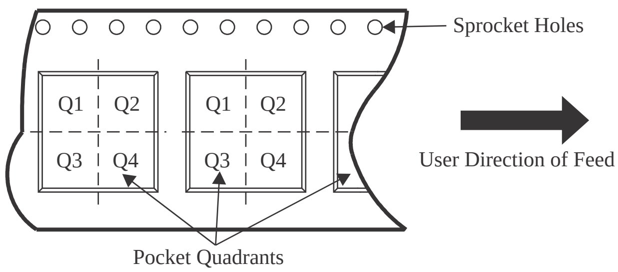


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

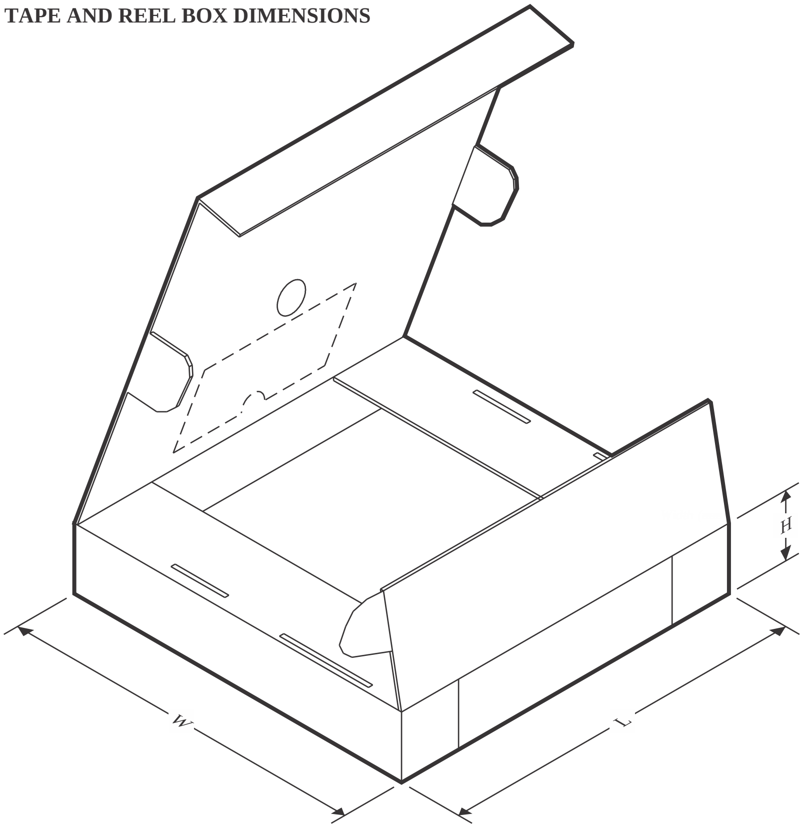
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA1632DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA1632DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

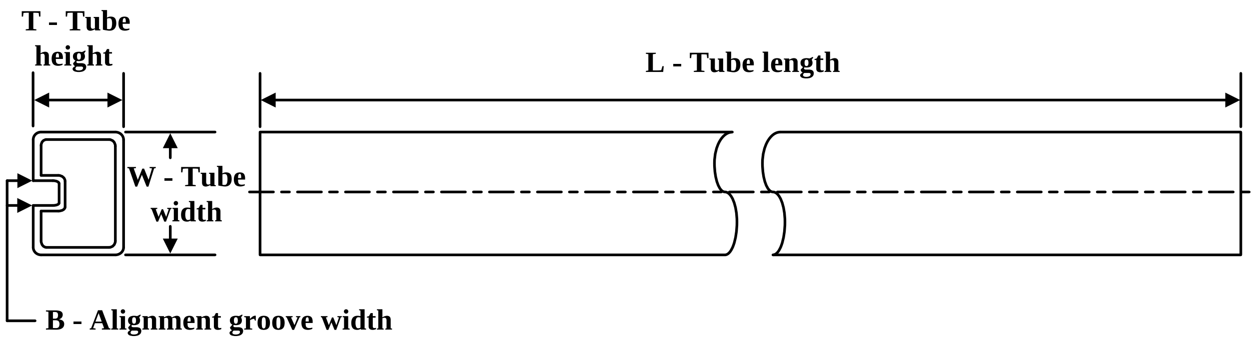
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA1632DGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
OPA1632DR	SOIC	D	8	2500	350.0	350.0	43.0

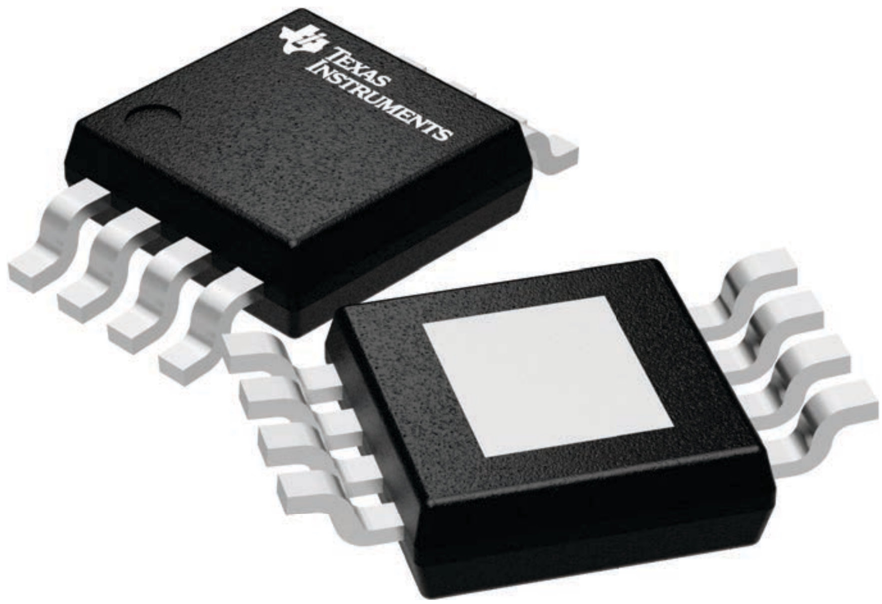
TUBE

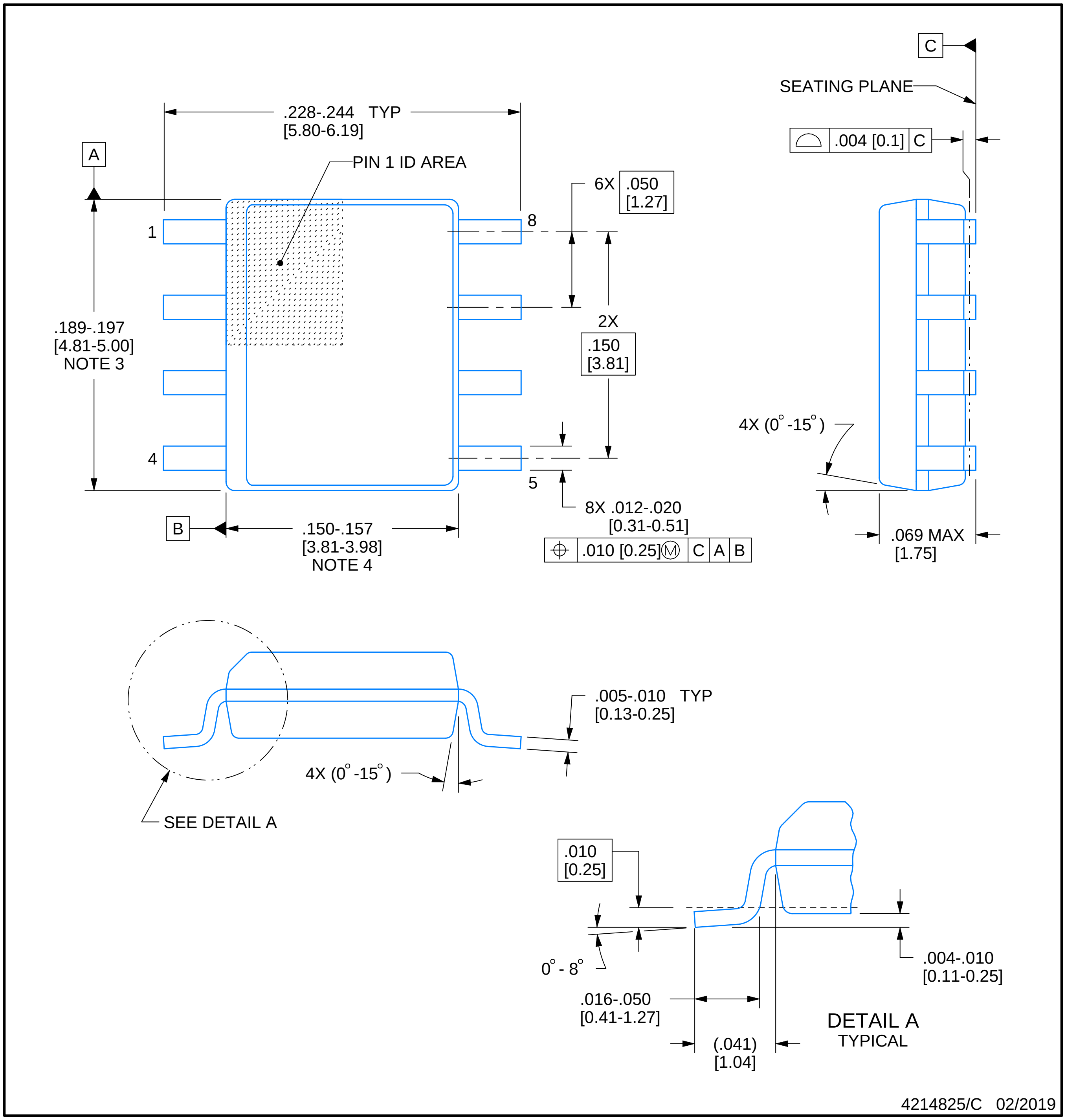


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA1632D	D	SOIC	8	75	505.46	6.76	3810	4
OPA1632DG4	D	SOIC	8	75	505.46	6.76	3810	4

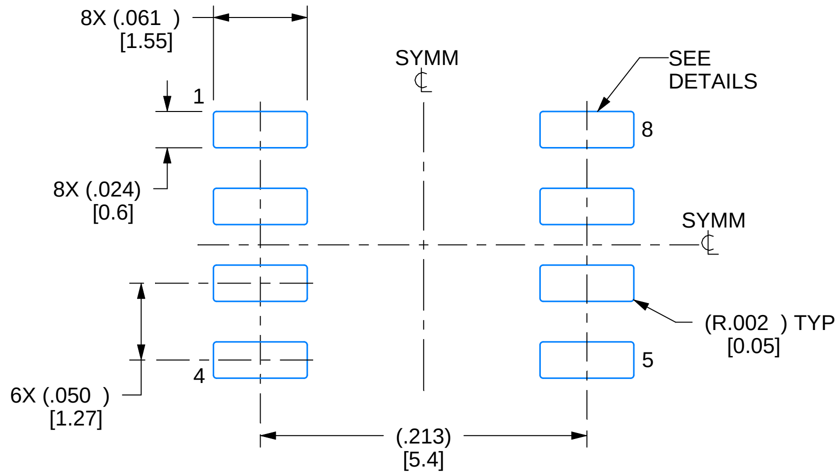
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



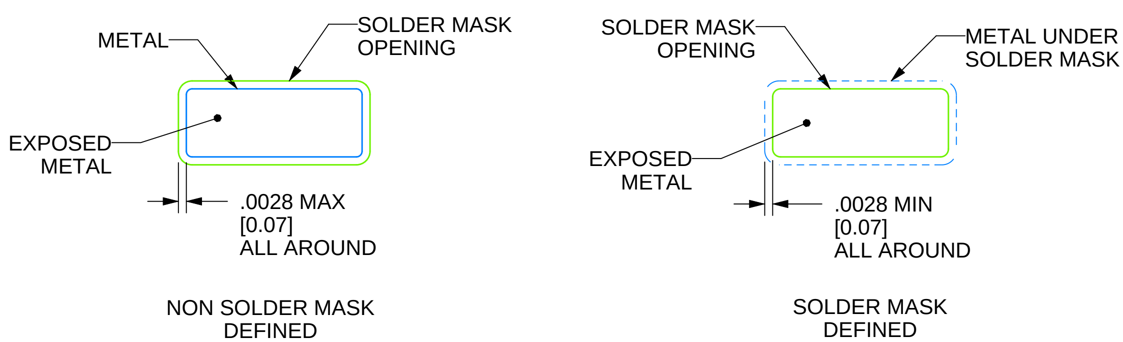


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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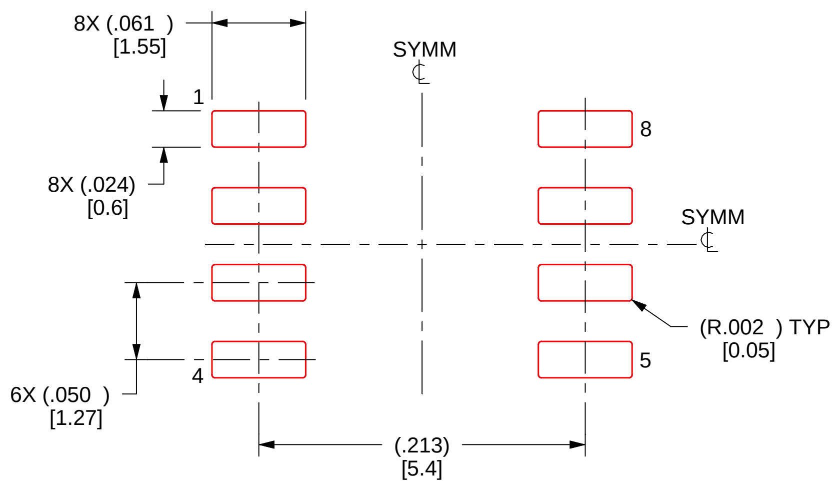
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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