OPAx340 単一電源、レール・ツー・レール・オペアンプ MicroAmplifier™シリーズ

1 特長

- レール・ツー・レール入力
- レール・ツー・レール出力(1mV以内)
- *Micro*Sizeパッケージ
- 広い帯域幅: 5.5MHz
- 高いスルー・レート: 6V/µs
- 低いTHD＋ノイズ: 0.0007% (f = 1kHz)
- 低い静止電流: 750µA/チャネル
- シングル、デュアル、クワッド・バージョン

2 アプリケーション

- A/Dコンバータの駆動
- PCMCIAカード
- データ収集
- プロセス制御
- オーディオ・プロセッシング
- 通信
- アクティブ・フィルタ
- 試験用機器

3 概要

OPA340シリーズのレール・ツー・レールCMOSオペアンプは、低電圧の単一電源で動作するよう最適化された製品です。レール・ツー・レールの入出力と高速動作により、サンプリングA/Dコンバータの駆動に理想的です。これらのオペアンプは、汎用アプリケーションやオーディオ・アプリケーションのほか、D/Aコンバータの出力において電流/電圧(I/V)変換を行うのにも適しています。シングル、デュアル、クワッドの各製品で同一の仕様を備え、設計の柔軟性を高めています。

OPA340シリーズは、最低2.5Vの単一電源で動作し、同相入力電圧がGND - 500mV～電源電圧 + 500mVの範囲に対応します。出力電圧スイングは、100kΩ負荷の場合、電源電圧レールから1mVの範囲です。これらのデバイスは動的応答が非常に優れており(BW = 5.5MHz、SR = 6V/µs)、しかも静止電流がわずか750µAです。デュアルとクワッドは完全に独立した回路であり、クロストークを最小限とし、回路間で相互に影響することはありません。

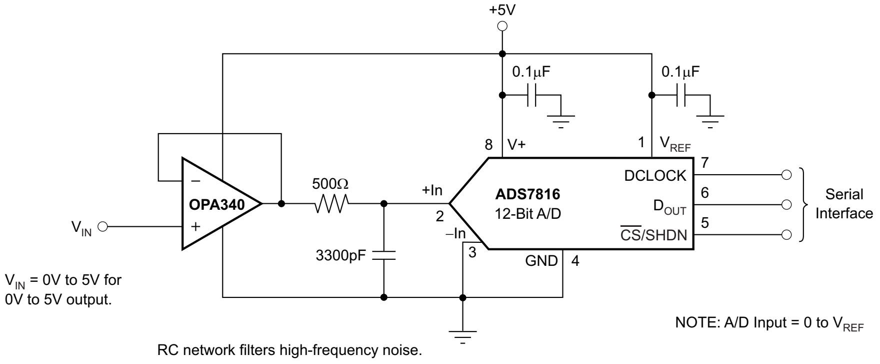
シングル(OPA340)のパッケージは小型の5ピンSOT-23表面実装、8ピンSOIC表面実装、および8ピンDIPです。デュアル(OPA2340)は小型の8ピンVSSOP表面実装、8ピンSOIC表面実装、および8ピンPDIPパッケージで供給されます。クワッド(OPA4340)のパッケージは省スペースの16ピンSSOP表面実装、および14ピンSOIC表面実装です。いずれの製品も、-40℃～85℃が定格内で、-55℃～125℃で動作します。設計解析用のSPICEマクロモデルを利用できます。

製品情報[1]

型番	パッケージ	本体サイズ(公称)
OPA340	SOT-23 (5)	3.00mm×3.00mm
OPA340、OPA2340	PDIP (8)	9.81mm×6.35mm
	SOIC (8)	4.90mm×3.91mm
OPA2340	VSSOP (8)	3.00mm×3.00mm
OPA4340	SOIC (14)	8.65mm×3.91mm
	SSOP (16)	4.90mm×3.90mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

ADS7816を駆動する非反転構成のOPA340



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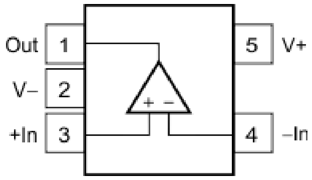
4 改訂履歴

Revision B (November 2007) から Revision C に変更 **Page**

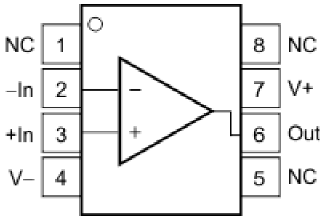
- 「*ESD定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスとドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクション 追加 ... 1
- 「*データシートの末尾にあるPOAを参照し、パッケージ/注文情報*」表を 削除 ... 1

5 Pin Configuration and Functions

OPA340: DBV Package
5-Pin SOT-23
Top View



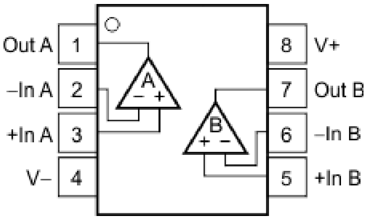
OPA340: P and D Packages
8-Pin PDIP and SOIC
Top View



Pin Functions: OPA340

PIN			I/O	DESCRIPTION
NAME	SOT-23	SOIC, PDIP		
–IN	4	2	I	Negative (inverting) input
+IN	3	3	I	Positive (noninverting) input
NC	—	1, 5, 8	—	No internal connection (can be left floating)
OUT	1	6	O	Output
V–	2	4	—	Negative (lowest) power supply
V+	5	7	—	Positive (highest) power supply

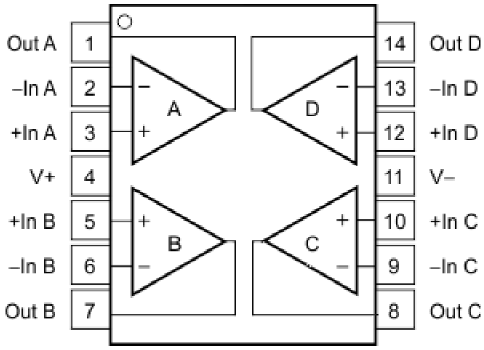
OPA2340: P, D, and DGK Packages
8-Pin PDIP, SOIC, and VSSOP
Top View



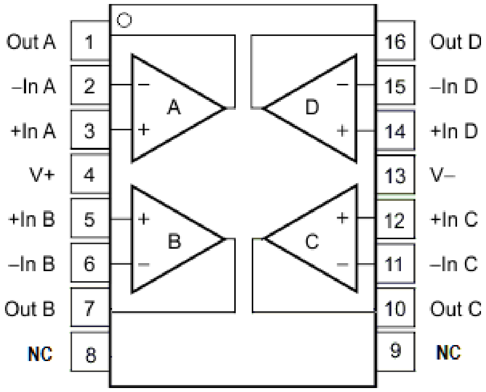
Pin Functions: OPA2340

PIN		I/O	DESCRIPTION
NAME	VSSOP, SOIC, PDIP		
–IN A	2	I	Negative (inverting) input channel A
+IN A	3	I	Positive (noninverting) input channel A
–IN B	6	I	Negative (inverting) input channel B
+IN B	5	I	Positive (noninverting) input channel B
OUT A	1	O	Output channel A
OUT B	7	O	Output channel B
V–	4	—	Negative (lowest) power supply
V+	8	—	Positive (highest) power supply

OPA4340: D Package
14-Pin SOIC
Top View



OPA4340: DBQ Package
16-Pin SSOP
Top View



Pin Functions: OPA4340

PIN			I/O	DESCRIPTION
NAME	SOIC	SSOP		
–IN A	2	2	I	Negative (inverting) input channel A
–IN B	6	6	I	Negative (inverting) input channel B
–IN C	9	11	I	Negative (inverting) input channel C
–IN D	13	15	I	Negative (inverting) input channel D
+IN A	3	3	I	Positive (noninverting) input channel A
+IN B	5	5	I	Positive (noninverting) input channel B
+IN C	10	12	I	Positive (noninverting) input channel C
+IN D	12	14	I	Positive (noninverting) input channel D
NC	—	8, 9	—	No internal connection (can be left floating)
OUT A	1	1	O	Output, channel A
OUT B	7	7	O	Output, channel B
OUT C	8	10	O	Output, channel C
OUT D	14	16	O	Output, channel D
V–	11	13	—	Negative (lowest) power supply
V+	4	4	—	Positive (highest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply voltage		5.5	V
	Signal input terminals(2)	–0.5	0.5	
Current	Signal input terminals(2)		10	mA
	Output short circuit(3)	Continuous		
Temperature	Operating, T_A	–55	125	°C
	Junction, T_J		150	
	Storage, T_{stg}	–55	125	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±600	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage	2.7	5.5	V
Specified temperature	–40	125	°C

6.4 Thermal Information – OPA340

THERMAL METRIC(1)		OPA340				UNIT
		DBV (SOT-23)	P (PDIP)	D (SOIC)	D (SOIC)	
		5 PINS	8 PINS	8 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	207.9	53.1	142	83.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	71.2	42.5	90.2	70.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	36.0	30.3	82.5	59.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.0	19.7	39.4	11.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	35.2	30.2	82	37.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Thermal Information – OPA2340

THERMAL METRIC[1]		OPA2340		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	138.4	169.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	89.5	62.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	78.6	89.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	29.9	7.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	78.1	88.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Thermal Information – OPA4340

THERMAL METRIC[1]		OPA4340	UNIT
		DBQ (SSOP)	
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	58.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	19.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	57.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.7 Electrical Characteristics

At T_A = 25°C, R_L = 10 kΩ connected to $V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage		V_S = 5 V		±150	±500	μV
dV_{OS}/dt	Input offset voltage vs temperature		T_A = –40°C to 85°C, V_S = 5 V		±2.5		μV/°C
PSRR	Input offset voltage vs power supply		V_S = 2.7 V to 5.5 V, V_{CM} = 0 V		30	120	μV/V
		Over temperature	V_S = 2.7 V to 5.5 V, V_{CM} = 0 V, T_A = –40°C to 85°C, V_S = 5 V			120	μV/°C
	Channel separation, DC				0.2		μV/V
INPUT BIAS CURRENT							
I_S	Input bias current				±0.2	±10	pA
		Over temperature	T_A = –40°C to 85°C, V_S = 5 V			±60	
I_{OS}	Input offset current				±0.2	±10	pA
NOISE							
	Input voltage noise		f = 0.1 kHz to 50 kHz		8		μV_{RMS}
e_n	Input voltage noise density		f = 1 kHz		25		$nV/\sqrt{Hz}$
i_n	Current noise density		f = 1 kHz		3		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			–0.3		(V+) + 0.3	V
CMRR	Common-mode rejection ratio		–0.3 V < V_{CM} < (V+) – 1.8 V	80	92		dB
			V_S = 5 V, –0.3 V < V_{CM} < 5.3 V	70	84		
			V_S = 2.7 V, –0.3 V < V_{CM} < 3 V	66	80		

(1) V_S = 5 V.

Electrical Characteristics (continued)

At T_A = 25°C, R_L = 10 kΩ connected to $V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
INPUT IMPEDANCE							
	Differential				10^{13} || 3		Ω || pF
	Common-mode				10^{13} || 6		Ω || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain		R_L = 100 kΩ, 5 mV < V_O < (V+) – 5 mV	106	124		dB
			R_L = 10 kΩ, 5 mV < V_O < (V+) – 50 mV	100	120		
			R_L = 2 kΩ, 200 mV < V_O < (V+) – 200 mV	94	114		
		Over temperature	R_L = 100 kΩ, 5 mV < V_O < (V+) – 5 mV, T_A = –40°C to 85°C, V_S = 5 V	106			
			R_L = 10 kΩ, 5 mV < V_O < (V+) – 50 mV, T_A = –40°C to 85°C, V_S = 5 V	100			
			R_L = 2 kΩ, 200 mV < V_O < (V+) – 200 mV, T_A = –40°C to 85°C, V_S = 5 V	94			
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product		G = 1		5.5		MHz
SR	Slew rate		V_S = 5 V, G = 1, C_L = 100 pF		6		V/µs
	Settling time, 0.1%		V_S = 5 V, 2-V step, C_L = 100 pF		1		µs
	Settling time, 0.01%		V_S = 5 V, 2-V step, C_L = 100 pF		1.6		µs
	Overload recovery time		$V_{IN} \times G = V_S$		0.2		µs
THD+N	Total harmonic distortion + noise		V_S = 5 V, V_O = 3V_{PP}[2], G = 1, f = 1 kHz		0.0007%		
OUTPUT							
	Voltage output swing from rail[2]		R_L = 100 kΩ, A_{OL} ≥ 106 dB		1	5	mV
			R_L = 10 kΩ, A_{OL} ≥ 106 dB		10		
			R_L = 2 kΩ, A_{OL} ≥ 106 dB		40		
		Over temperature	R_L = 100 kΩ, A_{OL} ≥ 106 dB, T_A = –40°C to 85°C, V_S = 5 V			5	
			R_L = 10 kΩ, A_{OL} ≥ 106 dB, T_A = –40°C to 85°C, V_S = 5 V			50	
			R_L = 2 kΩ, A_{OL} ≥ 106 dB, T_A = –40°C to 85°C, V_S = 5 V			200	
I_{SC}	Short-circuit current				±50		mA
C_{LOAD}	Capacitive load drive				See *Typical Characteristics*		
POWER SUPPLY							
V_S	Specified voltage range			2.7		5	V
	Operating voltage range		Lower end		2.5		V
			Higher end		5.5		
I_Q	Quiescent current (per amplifier)		I_O = 0, V_S = 5 V		750	950	µA
		Over temperature	I_O = 0, V_S = 5 V, T_A = –40°C to 85°C			100	
TEMPERATURE RANGE							
	Specified range			–40		85	°C
	Operating range			–55		125	°C
	Storage range			–55		125	°C

(2) Output voltage swings are measured between the output and power-supply rails.

6.8 Typical Characteristics

At T_A = 25°C, V_S = 5 V, and R_L = 10 kΩ connected to V_S/2, unless otherwise noted.

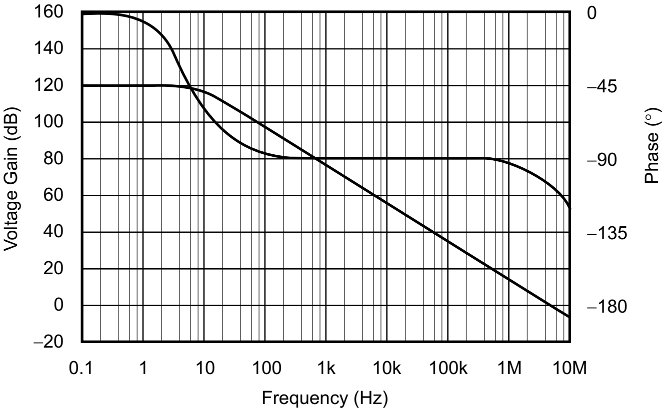


Figure 1. Open-Loop Gain/Phase vs Frequency

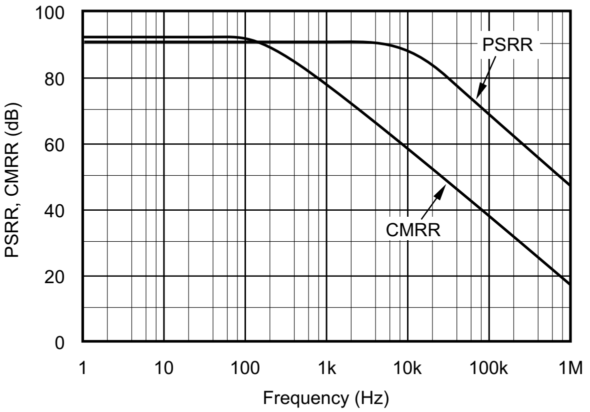


Figure 2. Power-Supply and Common-Mode Rejection vs Frequency

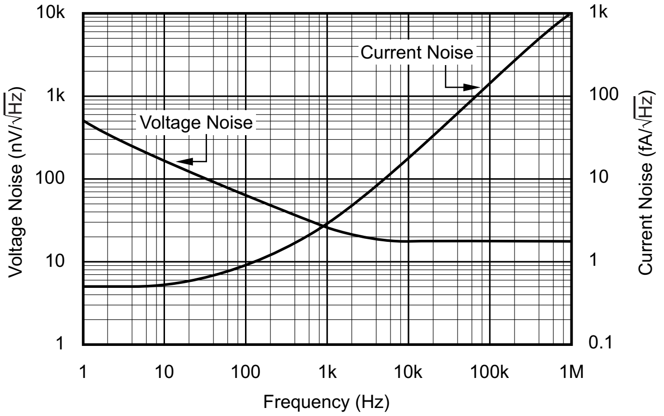


Figure 3. Input Voltage and Current Noise Spectral Density vs Frequency

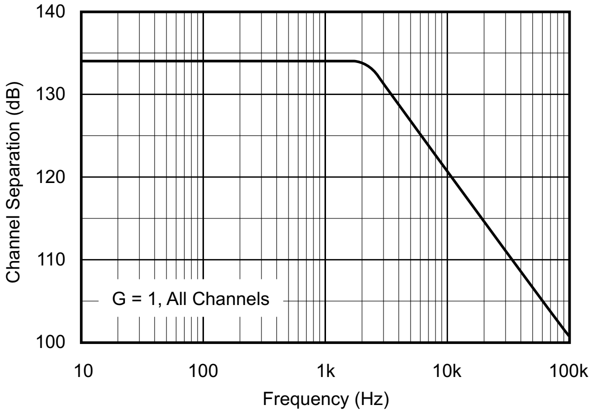


Figure 4. Channel Separation vs Frequency

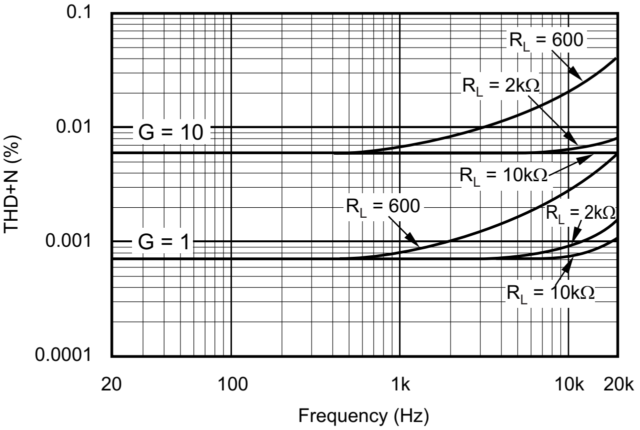


Figure 5. Total Harmonic Distortion + Noise vs Frequency

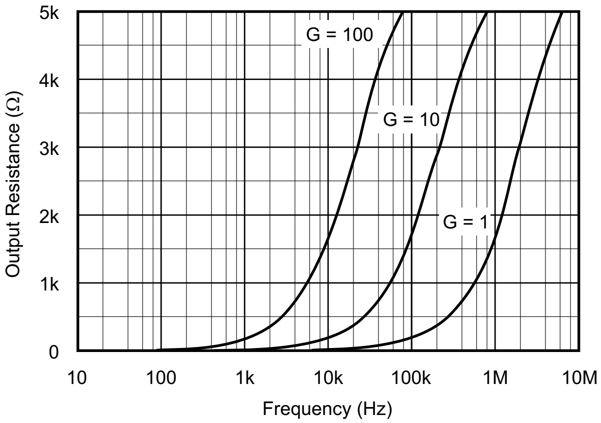


Figure 6. Closed-Loop Output Impedance vs Frequency

Typical Characteristics (continued)

At T_A = 25°C, V_S = 5 V, and R_L = 10 kΩ connected to V_S/2, unless otherwise noted.

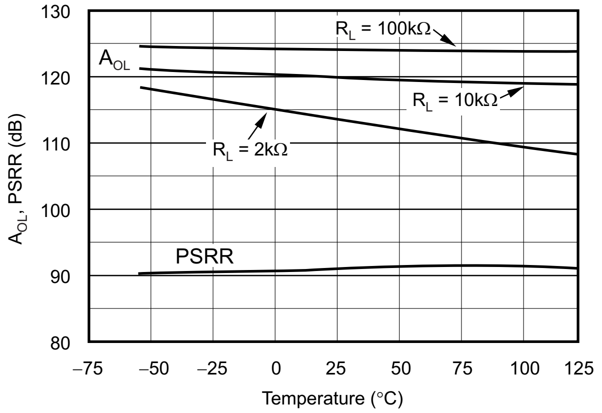


Figure 7. Open-Loop Gain and Power-Supply Rejection vs Temperature

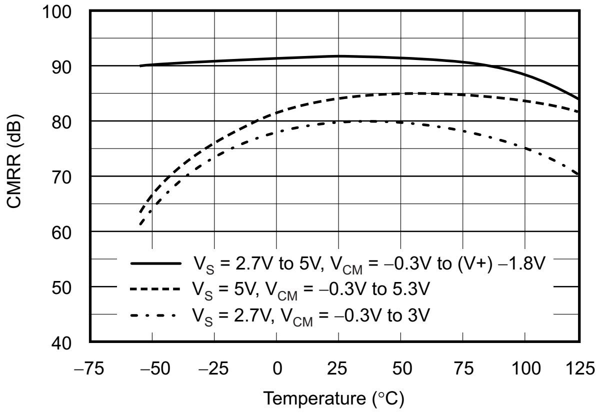


Figure 8. Common-Mode Rejection vs Temperature

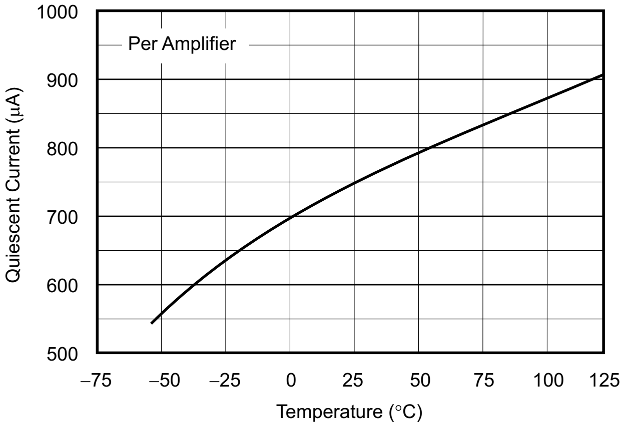


Figure 9. Quiescent Current vs Temperature

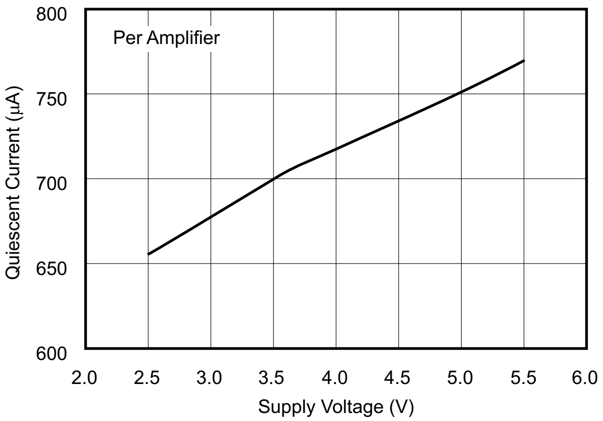


Figure 10. Quiescent Current vs Supply Voltage

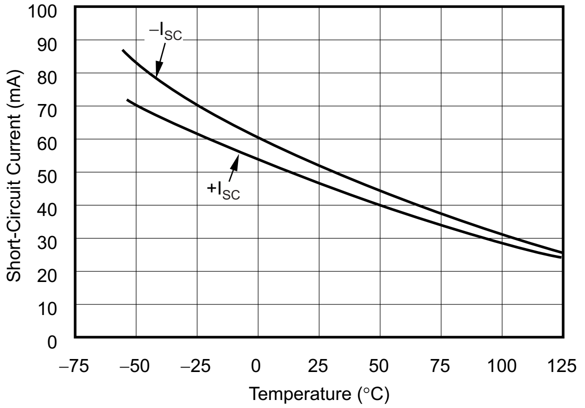


Figure 11. Short-Circuit Current vs Temperature

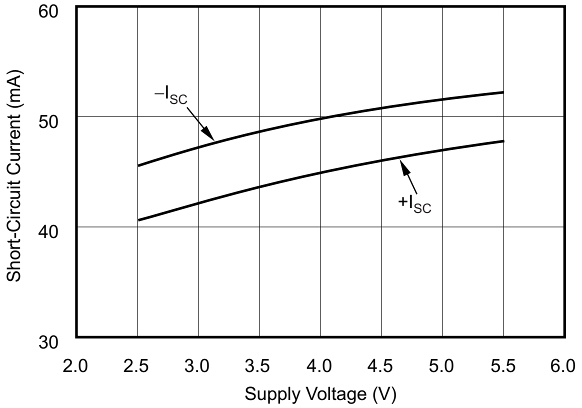


Figure 12. Short-Circuit Current vs Supply Voltage

Typical Characteristics (continued)

At T_A = 25°C, V_S = 5 V, and R_L = 10 kΩ connected to $V_S/2$, unless otherwise noted.

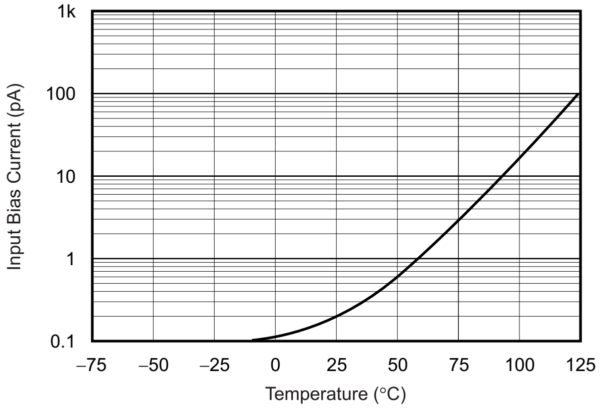


Figure 13. Input Bias Current vs Temperature

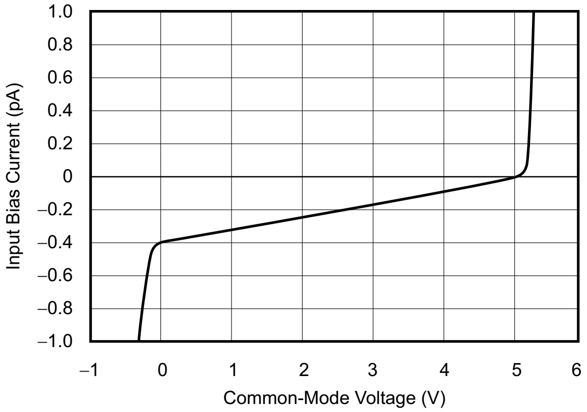


Figure 14. Input Bias Current vs Input Common-Mode Voltage

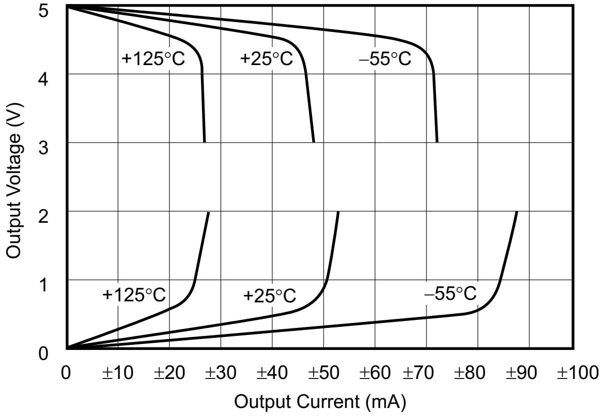


Figure 15. Output Voltage Swing vs Output Current

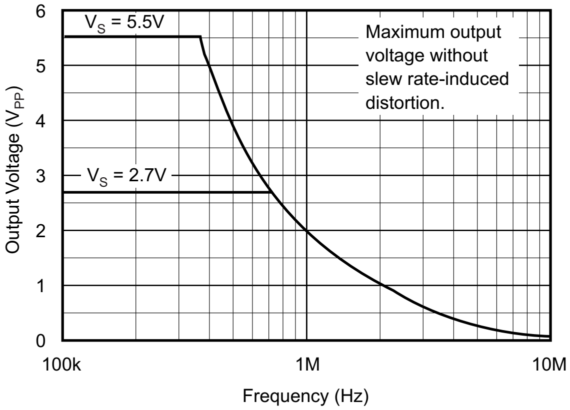


Figure 16. Maximum Output Voltage vs Frequency

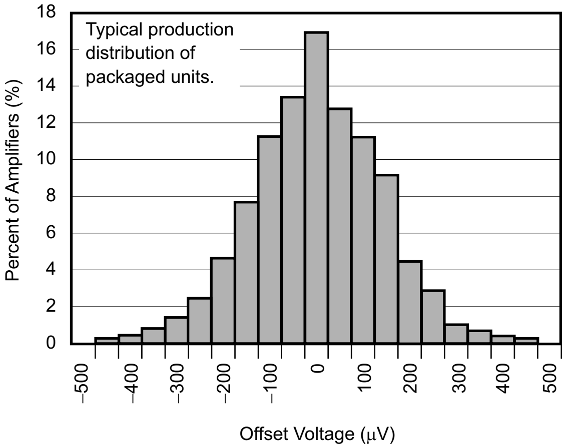


Figure 17. Offset Voltage Production Distribution

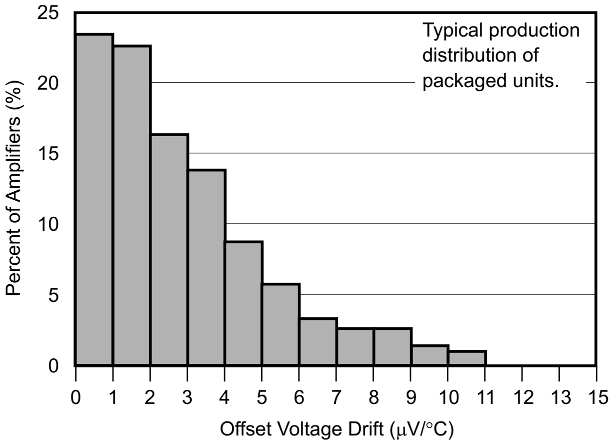
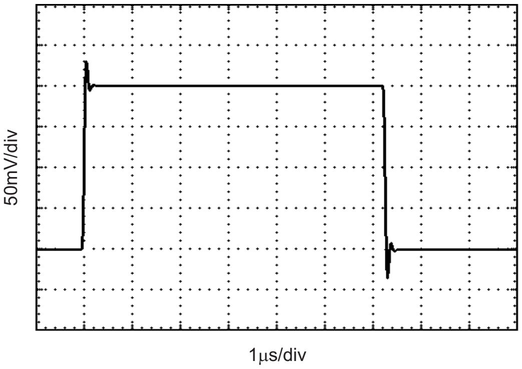


Figure 18. Offset Voltage Drift Magnitude Production Distribution

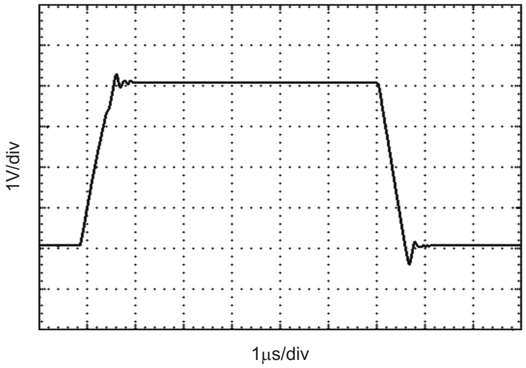
Typical Characteristics (continued)

At $T_A = 25°C$, $V_S = 5$ V, and $R_L = 10$ kΩ connected to $V_S/2$, unless otherwise noted.



$C_L = 100$ pF

Figure 19. Small-Signal Step Response



$C_L = 100$ pF

Figure 20. Large-Signal Step Response

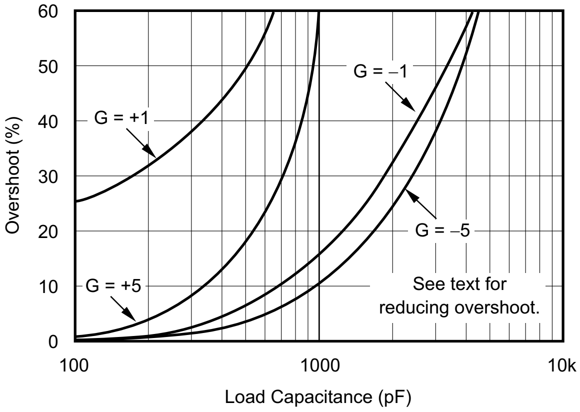


Figure 21. Small-Signal Overshoot vs Load Capacitance

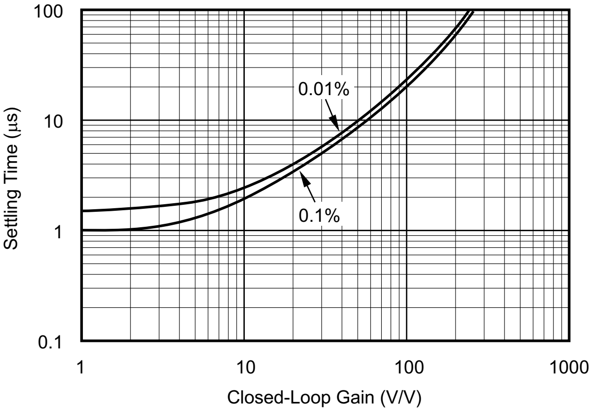


Figure 22. Settling Time vs Closed-Loop Gain

7 Detailed Description

7.1 Overview

The OPA340 series operational amplifiers are fabricated on a state-of-the-art, 0.6-micron CMOS process. These devices are unity-gain stable and suitable for a wide range of general-purpose applications. Rail-to-rail input and output make them ideal for driving sampling A/D converters. In addition, excellent AC performance makes them well-suited for audio applications. The class AB output stage is capable of driving 600-Ω loads series and extends 500 mV beyond the supply. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications. Figure 23 shows the input and output waveforms for the OPA340 in unity-gain configuration. Operation is from a single 5-V supply with a 10-kΩ load connected to V/2. The input is a 5-V_{PP} sinusoid. Output voltage is approximately 4.98 V_{PP}. Power-supply pins must be bypassed with 0.01-µF ceramic capacitors.

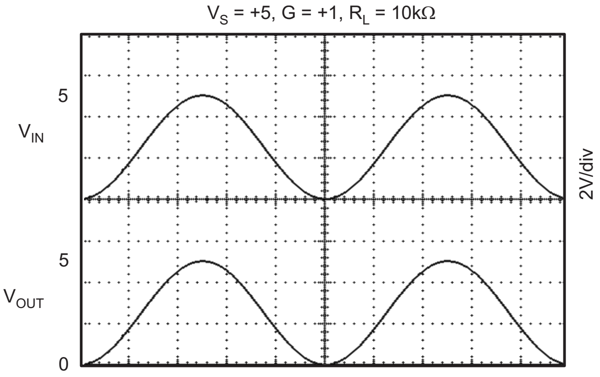
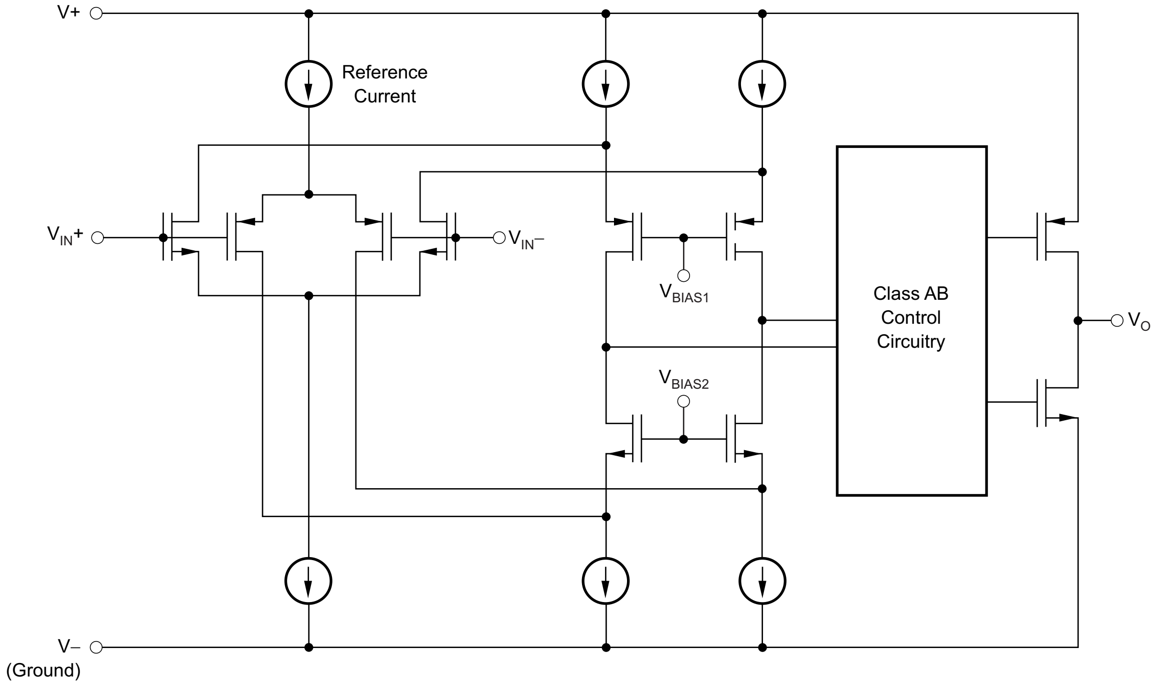


Figure 23. Rail-to-Rail Input and Output

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Operating Voltage

The OPA340 series operational amplifiers are fully specified from 2.7 V to 5 V. However, supply voltage may range from 2.5 V to 5.5 V. Parameters are ensured over the specified supply range—a unique feature of the OPA340 series. In addition, many specifications apply from –40°C to 85°C. Most behavior remains virtually unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltages or temperature are shown in the *Typical Characteristics*.

7.3.2 Rail-to-Rail Input

The input common-mode voltage range of the OPA340 series extends 500 mV beyond the supply rails. This extended range is achieved with a complementary input stage—an N-channel input differential pair in parallel with a P-channel differential pair. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.3 V to 500 mV above the positive supply, while the P-channel pair is on for inputs from 500 mV below the negative supply to approximately (V+) – 1.3 V. There is a small transition region, typically (V+) – 1.5 V to (V+) – 1.1 V, in which both pairs are on. This 400-mV transition region can vary ±300 mV with process variation. Thus, the transition region (both stages on) can range from (V+) – 1.8 V to (V+) – 1.4 V on the low end, up to (V+) – 1.2 V to (V+) – 0.8 V on the high end.

OPA340 series operational amplifiers are laser-trimmed to the reduce offset voltage difference between the N-channel and P-channel input stages, resulting in improved common-mode rejection and a smooth transition between the N-channel pair and the P-channel pair. However, within the 400-mV transition region PSRR, CMRR, offset voltage, offset drift, and THD may be degraded compared to operation outside this region.

A double-folded cascode adds the signal from the two input pairs and presents a differential signal to the class AB output stage. Normally, input bias current is approximately 200 fA; however, input voltages exceeding the power supplies by more than 500 mV can cause excessive current to flow in or out of the input pins. Momentary voltages greater than 500 mV beyond the power supply can be tolerated if the current on the input pins is limited to 10 mA. This current limiting is easily accomplished with an input resistor, as shown in Figure 24. Many input signals are inherently current-limited to less than 10 mA; therefore, a limiting resistor is not required.

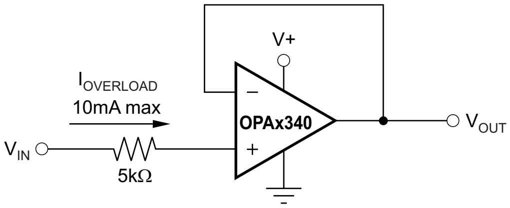

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Figure 24. Input Current Protection for Voltages Exceeding the Supply Voltage

7.3.3 Rail-to-Rail Output

A class AB output stage with common-source transistors is used to achieve rail-to-rail output. For light resistive loads (> 50 kΩ), the output voltage is typically a few millivolts from the supply rails. With moderate resistive loads (2 kΩ to 50 kΩ), the output can swing to within a few tens of millivolts from the supply rails and maintain high open-loop gain (see Figure 15).

7.3.4 Capacitive Load and Stability

OPA340 series operational amplifiers can drive a wide range of capacitive loads. However, all operational amplifiers under certain conditions can become unstable. operational amplifier configuration, gain, and load value are some of the factors to consider when determining stability. An operational amplifier in unity-gain configuration is most susceptible to the effects of capacitive load. The capacitive load reacts with the output resistance of the operational amplifier, along with any additional load resistance, to create a pole in the small-signal response that degrades the phase margin. In unity-gain configuration, the OPA340 series operational amplifiers perform well, with a pure capacitive load up to approximately 1000 pF. Increasing gain enhances the amplifier ability to drive more capacitance (see Figure 21).

Feature Description (continued)

One method of improving capacitive load drive in the unity-gain configuration is to insert a 10-Ω to 20-Ω resistor in series with the output, as shown in Figure 25. This resistor significantly reduces ringing with large capacitive loads. However, if there is a resistive load in parallel with the capacitive load, it creates a voltage divider introducing a DC error at the output and slightly reduces output swing. This error can be insignificant. For instance, with R_L = 10 kΩ and R_S = 20 Ω, there is only an approximate 0.2% error at the output.

When used with the miniature package options of the OPA340 series, the combination is ideal for space-limited and low-power applications. For further information, consult the ADS7816 data sheet, *12-Bit High Speed Micro Power Sampling Analog-To-Digital Converter* (SBAS061). With the OPA340 in a noninverting configuration, an RC network at the output of the amplifier can be used to filter high-frequency noise in the signal (see Figure 26). In the inverting configuration, filtering may be accomplished with a capacitor across the feedback resistor (see Figure 27).

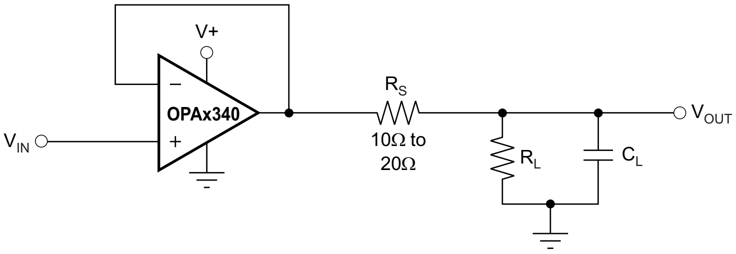

Figure 25. Series Resistor in Unity-Gain Configuration Improves Capacitive Load Drive

7.3.5 Driving A/D Converters

The OPA340 series operational amplifiers are optimized for driving medium-speed (up to 100 kHz) sampling A/D converters. However, they also offer excellent performance for higher speed converters. The OPA340 series provides an effective means of buffering the converter input capacitance and resulting charge injection while providing signal gain. Figure 26 and Figure 27 show the OPA340 driving an ADS7816. The ADS7816 is a 12-bit, micro-power sampling converter in the tiny 8-pin VSSOP package.

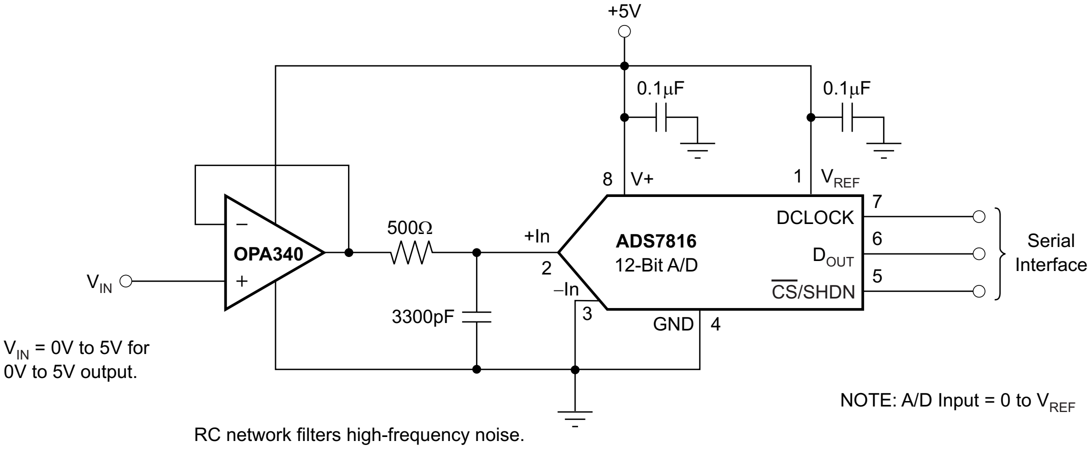

Figure 26. OPA340 in Noninverting Configuration Driving ADS7816

Feature Description (continued)

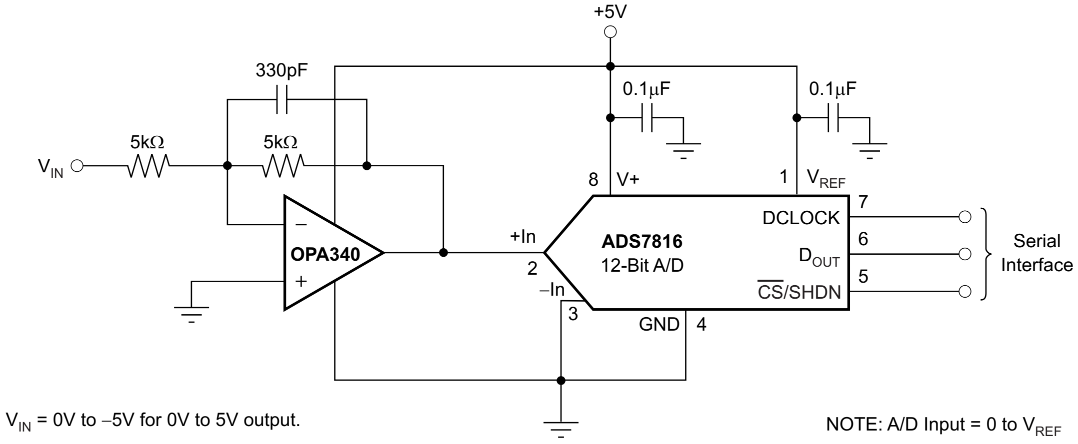

Figure 27. OPA340 in Inverting Configuration Driving ADS7816

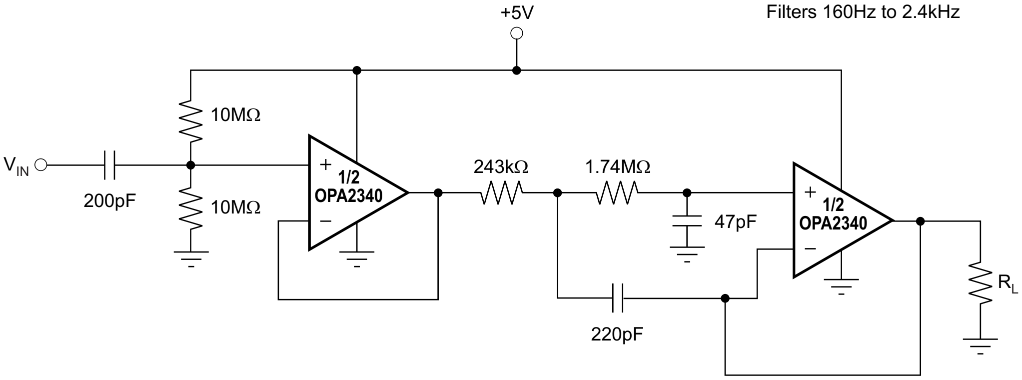

Figure 28. Speech Bandpass Filter

7.4 Device Functional Modes

The OPAx340 has a single functional mode and is operational when the power-supply voltage is greater than 2.7 V (±1.35 V). The maximum power supply voltage for the OPAx340 is 5.5 V (±2.75 V).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPAx340 amplifier is a single-supply, CMOS operational amplifier with 5.5-MHz unity-gain bandwidth and supply current of 950 µA. Its performance is optimized for low-voltage (2.7 V to 5.5 V), single-supply applications, with its input common-mode voltage linear range extending 300 mV beyond the rails and the output voltage swing within 5 mV of either rail. The OPAx340 series features wide bandwidth and unity-gain stability with rail-to-rail input and output for increased dynamic range. Power-supply pins must be bypassed with 0.01-µF ceramic capacitors.

8.2 Typical Applications

8.2.1 Single-Pole, Low-Pass Filter

Figure 29 shows the OPA340 in a typical noninverting application with the input signal bandwidth limited by the input lowpass filter.

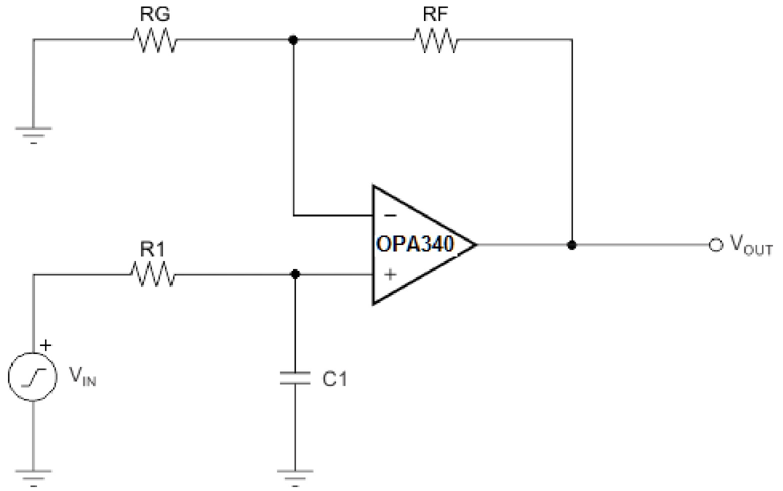

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Figure 29. Single-Pole, Low-Pass Filter

Equation 1 through Equation 2 show calculations for corner frequency and gain:

$$f_{-3\,dB} = \frac{1}{2\pi R_1 C_1} \tag{1}$$

$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR_1C_1}\right) \tag{2}$$

Typical Applications (continued)

8.2.1.1 Design Requirements

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to establish this limited bandwidth is to place an RC filter at the noninverting terminal of the amplifier, as shown in Figure 29. If a steeper attenuation level is required, a two-pole or higher-order filter may be used.

8.2.1.2 Detailed Design Procedure

The design goals for this circuit include these parameters:

- A noninverting gain of 10 V/V (20 dB)
- Design a single-pole response circuit with –3-dB rolloff at 15.9 kHz and 159 Hz
- Modify the design to increase attenuation level to –40 dB/decade (Sallen-Key Filter)

Use these design values:

- C_1 = 0 nF, 10 nF, 1 µF
- R_1 = 1 kΩ
- R_G = 10 kΩ
- R_F = 90 kΩ

Figure 30 shows how the output voltage of OPA340 changes over frequency depending on the value of C_1 with a constant R_1 of 1 kΩ. Without any filtering of the input signal (C_1 = 0), the –3-dB effective bandwidth is a function of the OPA340 unity-gain bandwidth and closed-loop gain, $f_{(-3dB)}$ = UGBW/A_{CL}, where A_{CL} is closed-loop gain and UGBW denotes unity-gain bandwidth. Thus, for a closed-loop gain = 10, $f_{(-3dB)}$ = 1 MHz/10 =100 kHz; see Figure 30.

To further limit the output bandwidth, an appropriate choice of C_1 must be made: for C_1 = 10 nF, $f_C = \frac{1}{2\pi \times R_1C_1} = \frac{1}{2\pi \times 1^{3} \times 1^{-8}}$ = 15.9 kHz.

To further limit the bandwidth, a larger C_1 must be used: choosing C_1 = 1 µF,

$f_C = \frac{1}{2\pi \times R_1C_1} = \frac{1}{2\pi \times 1^{3} \times 1^{-6}}$ = 159 Hz (see Figure 30).

8.2.1.3 Application Curve

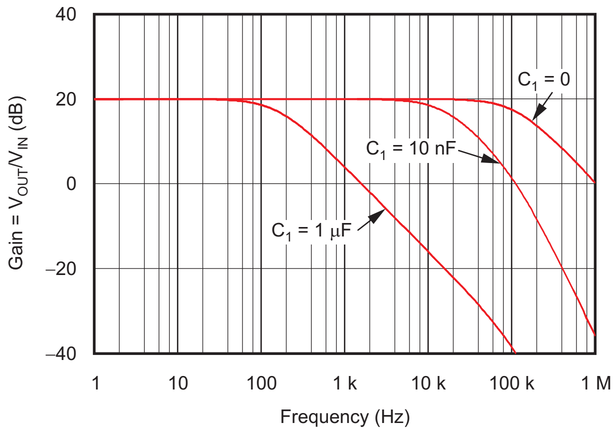

Figure 30. OPA340 Single-Pole AC Gain vs Frequency Response

Typical Applications (continued)

8.2.2 Two-Pole, Low-Pass Filter

If even more attenuation is required, a multiple pole filter is required. The Sallen-Key filter may be used for this task, as shown in Figure 31. For best results, the amplifier must have effective bandwidth that is at least 10 times higher than the filter cutoff frequency. Failure to follow this guideline results in a phase shift of the amplifier, which in turn leads to lower precision of the filter bandwidth. Additionally, to minimize the loading effect between multiple RC pairs on overall the filter cutoff frequency, choose R = 10 × R_1 and C_2 = C1/10; see Figure 32.

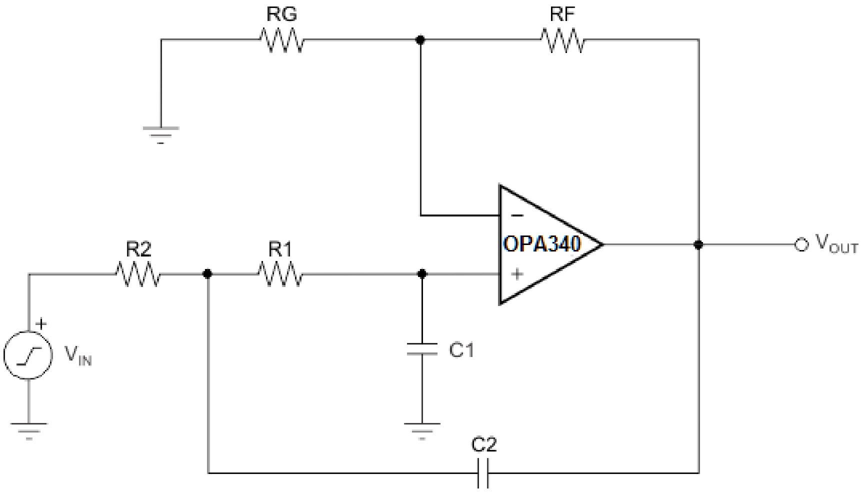

Figure 31. Two-Pole, Lowpass Filter

Equation 3 through Equation 5 show calculations for corner frequency and gain:

$$f_C = \frac{1}{2\pi\sqrt{R_1C_1R_2C_2}} \quad (3)$$

$$\frac{V_{OUT(s)}}{V_{IN(s)}} = \frac{G(2\pi f_c)^2}{s^2 + 2\zeta(2\pi f_c)s + (2\pi f_c)^2} \quad (4)$$

$$G = \frac{R_G + R_F}{R_G} \quad (5)$$

8.2.2.1 Detailed Design Procedure

Use these design values:

- C_1 = 10 nF and C_2 = 1 nF
- R_1 = 1 kΩ and R_2= 10 kΩ
- R_G = 10 kΩ
- R_F = 90 kΩ

Figure 32 shows the Sallen-Key filter second-order response for different RC values: for R and C values above, $f_C = \frac{1}{2\pi\sqrt{R_1C_1R_2C_2}} = \frac{1}{2\pi\sqrt{1^{3} \times 1^{-8} \times 1^{4} \times 1^{-9}}}$ = 15.9 kHz.

To further limit the bandwidth, a larger RC value must be used: increasing C values 100 times, such as C_1 = 1 µF and C_2 = 0.1 µF, with unchanged resistors, results in the second-order rolloff at $f_C = \frac{1}{2\pi\sqrt{R_1C_1R_2C_2}} = \frac{1}{2\pi\sqrt{1^{3} \times 1^{-6} \times 1^{4} \times 1^{-7}}}$ = 159 Hz. See Figure 32.

Typical Applications (continued)

8.2.2.2 Application Curve

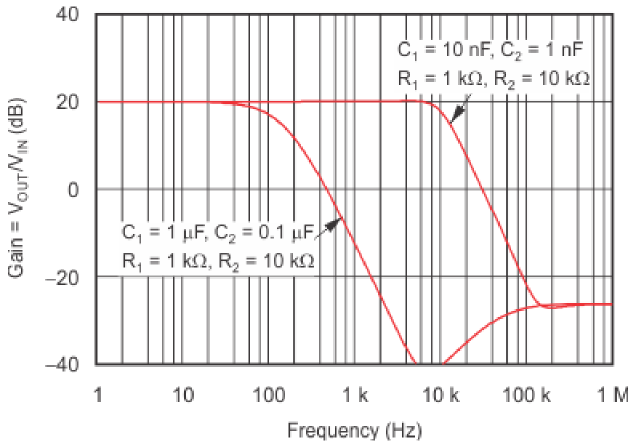

Figure 32. OPA340 Two-Pole, Lowpass Sallen-Key AC Gain vs Frequency Response

9 Power Supply Recommendations

The OPAx340 is specified for operation from 2.7 V to 5.5 V (±1.35 V to ±2.75 V).

CAUTION

Supply voltages larger than 7 V can permanently damage the device (see the *Absolute Maximum Ratings*).

TI recommends placing 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies.

10 Layout

10.1 Layout Guidelines

Pay attention to good layout practices. Keep traces short and when possible, use a printed-circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1-μF capacitor closely across the supply pins. Apply these guidelines throughout the analog circuit to improve performance and provide benefits, such as reducing the electromagnetic interference (EMI) susceptibility.

Operational amplifiers vary in susceptibility to radio frequency interference (RFI). RFI can generally be identified as a variation in offset voltage or DC signal levels with changes in the interfering RF signal. The OPA340 is specifically designed to minimize susceptibility to RFI and demonstrates remarkably low sensitivity compared to previous generation devices. Strong RF fields can still cause varying offset levels.

10.2 Layout Example

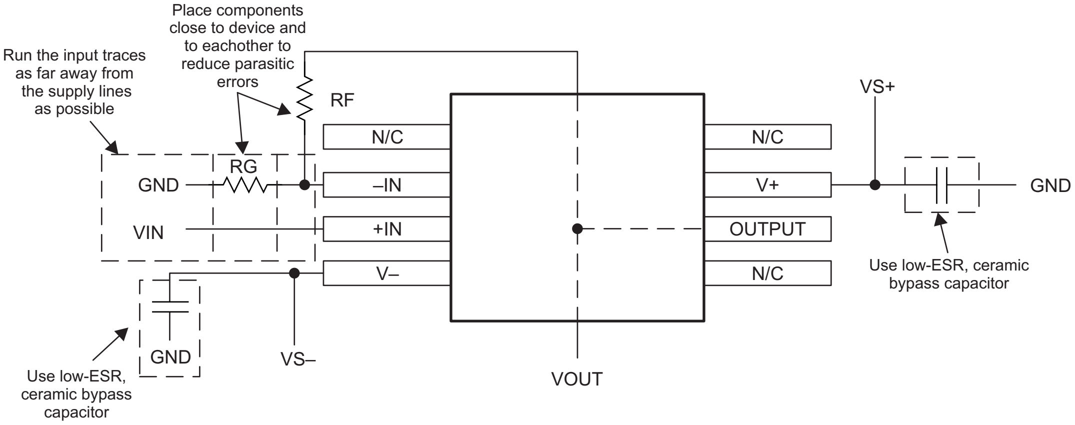

Figure 33. Layout Recommendation

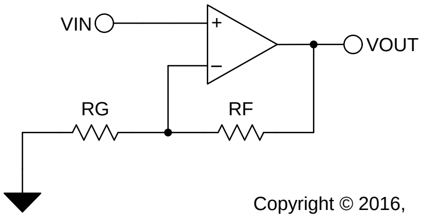

Figure 34. Schematic Representation

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 開発サポート

11.1.1.1 TINA-TI™ (無料のダウンロード・ソフトウェア)

TINA™は、SPICEエンジンをベースにした単純かつ強力な、使いやすい回路シミュレーション・プログラムです。また、TINA-TI™はTINAソフトウェアの無料バージョンで、完全な機能を持ち、パッシブとアクティブ両方のモデルに加えて、マクロ・モデルのライブラリがプリロードされています。TINA-TIには従来型のDC、トランジェント、および周波数ドメインのSPICEによる分析と、追加の設計機能が搭載されています。

TINA-TIはAnalog eLab Design Centerから無料でダウンロードでき、ユーザーが結果をさまざまな方法でフォーマットできる、広範な後処理機能を備えています。仮想計測器により、入力波形を選択し、回路ノード、電圧、および波形をプローブして、動的なクイック・スタート・ツールを作成できます。

注

これらのファイルを使用するには、TINAソフトウェア(DesignSoft™ 製)またはTINA-TIソフトウェアがインストールされている必要があります。TINA-TIフォルダから、無料のTINA-TIソフトウェアをダウンロードしてください。

11.1.1.2 DIPアダプタ評価モジュール

DIPアダプタ評価モジュールツールを使用すると、小さな表面実装ICのプロトタイプを簡単に、低コストで作成できます。この評価ツールは、DまたはU(SOIC-8)、PW(TSSOP-8)、DGK(MSOP-8)、DBV(SOT23-6、SOT23-5、およびSOT23-3)、DCK(SC70-6およびSC70-5)、およびDRL(SOT563-6)のTIパッケージに対応しています。DIPアダプタ評価モジュールは、ターミナル・ストリップとともに使用することも、既存の回路へ直接接続することもできます。

11.1.1.3 ユニバーサル・オペアンプ評価モジュール

ユニバーサル・オペアンプ評価モジュールは一連の汎用のブランクアウト回路基板で、各種のICパッケージ・タイプ向けの回路のプロトタイプ作成を容易にします。評価モジュール基板の設計により、多くの異なる回路を簡単かつ迅速に構築できます。5つのモデルが提供されており、それぞれのモデルは特定のパッケージ・タイプを対象としています。PDIP、SOIC、MSOP、TSSOP、およびSOT23のパッケージがすべてサポートされています。

注

これらの基板には部品が搭載されていないため、ユーザーが独自のICを供給する必要があります。ユニバーサル・オペアンプ評価モジュールを注文するときに、オペアンプ・デバイスのサンプルをいくつか要求することをお勧めします。

11.1.1.4 TI Precision Designs

TI Precision Designsは、TIの高精度アナログ・アプリケーションの専門家により作成されたアナログ・ソリューションで、多くの有用な回路に関して、動作理論、コンポーネント選択、シミュレーション、完全なPCB回路図とレイアウト、部品表、性能測定結果を提供します。TI Precision Designsは、http://www.ti.com/ww/en/analog/precision-designs/からオンラインで入手できます。

11.1.1.5 WEBENCH®Filter Designer

WEBENCH® Filter Designerは単純で強力な、使いやすいアクティブ・フィルタ設計プログラムです。WEBENCH Filter Designerを使用すると、TIのベンダ・パートナーからのTI製オペアンプやパッシブ・コンポーネントを使用して、最適なフィルタ設計を作成できます。

WEBENCH® Filter Designerは、WEBENCH® Design CenterからWebベースのツールとして利用でき、包括的な複数段アクティブ・フィルタ・ソリューションをわずか数分で設計、最適化、シミュレーションできます。

11.2 ドキュメントのサポート

11.2.1 関連資料

参照資料については、以下のアプリケーション・レポートおよび刊行物をご覧ください(www.ti.comからダウンロードできます)。

- *『12ビット高速Micro PowerサンプリングA/Dコンバータ*(SBAS061)
- *『双極性、双方向の電流シャント・モニタ』*(SLYT311)
- *『OPA340、OPA2340、OPA4340のEMI耐性特性』*(SBOZ010)
- *『ADCの全性能を引き出す方法』*(SBAA069)
- *『フィードバック・プロットによるオペアンプAC性能の定義』*(SBOA015)
- *『絶縁抵抗の使用による容量性負荷駆動のソリューション』*(TIPD128)
- *『基板のレイアウト技法』*(SLOA089)

11.3 関連リンク

表 1 に、クイック・アクセス・リンクの一覧を示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 1. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
OPA340	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
OPA2340	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
OPA4340	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

11.4 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.5 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.6 商標

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11.7 静電気放電に関する注意事項

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11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2340EA/250	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR		A40A	Samples
OPA2340EA/250G4	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR		A40A	Samples
OPA2340EA/2K5	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR		A40A	Samples
OPA2340EA/2K5G4	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR		A40A	Samples
OPA2340PA	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI		OPA2340PA	
OPA2340UA	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2340UA	Samples
OPA2340UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		OPA 2340UA	Samples
OPA2340UA/2K5G4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		OPA 2340UA	Samples
OPA340NA/250	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A40	Samples
OPA340NA/250G4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A40	Samples
OPA340NA/3K	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A40	Samples
OPA340NA/3KG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A40	Samples
OPA340PA	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	OPA340PA	Samples
OPA340UA	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 340UA	Samples
OPA340UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 340UA	Samples
OPA340UA/2K5G4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 340UA	Samples
OPA4340EA/250	ACTIVE	SSOP	DBQ	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4340EA	Samples
OPA4340EA/250G4	ACTIVE	SSOP	DBQ	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4340EA	Samples

PACKAGE OPTION ADDENDUM

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA4340EA/2K5	ACTIVE	SSOP	DBQ	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4340EA	Samples
OPA4340UA	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA4340UA	Samples
OPA4340UA/2K5	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA4340UA	Samples
OPA4340UA/2K5G4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA4340UA	Samples
OPA4340UAG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA4340UA	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF OPA340 :

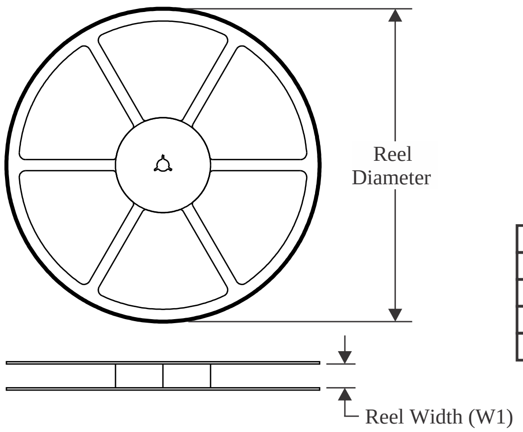
- Enhanced Product : OPA340-EP

NOTE: Qualified Version Definitions:

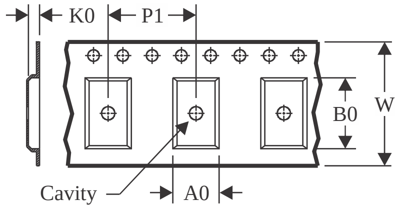
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

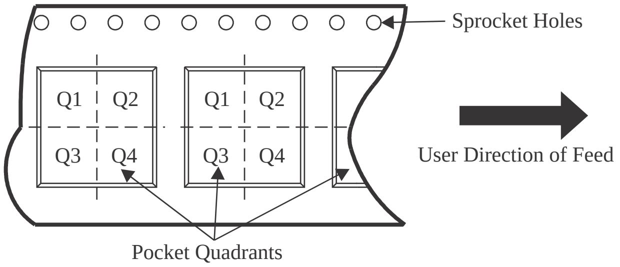


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

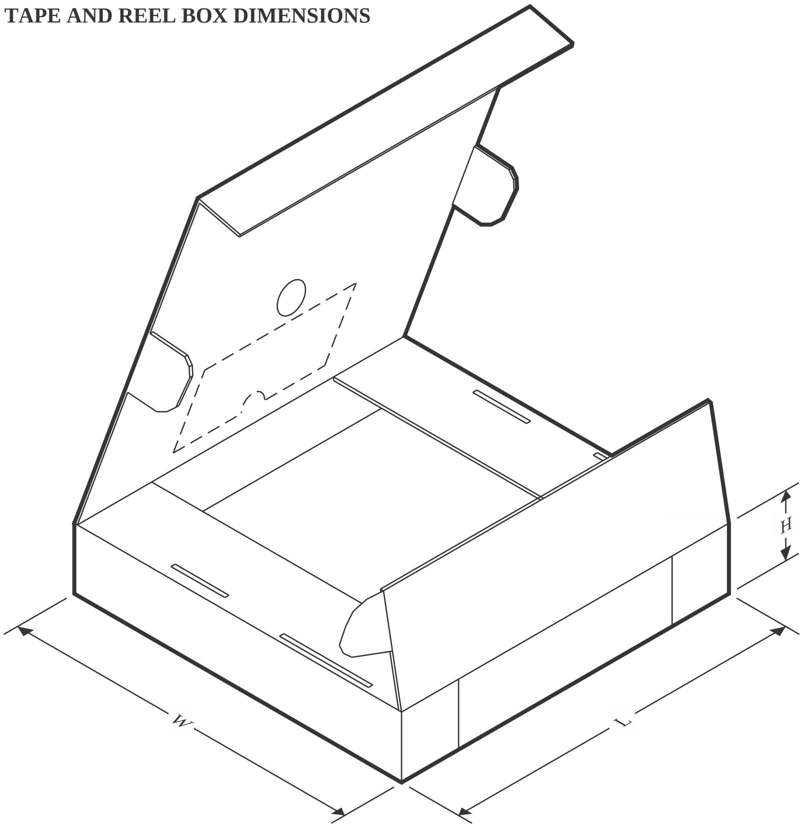
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2340EA/250	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2340EA/250G4	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2340EA/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2340EA/2K5G4	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2340UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA340NA/250	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA340NA/250	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA340NA/3K	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA340NA/3K	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA340UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4340EA/250	SSOP	DBQ	16	250	180.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4340EA/2K5	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4340UA/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

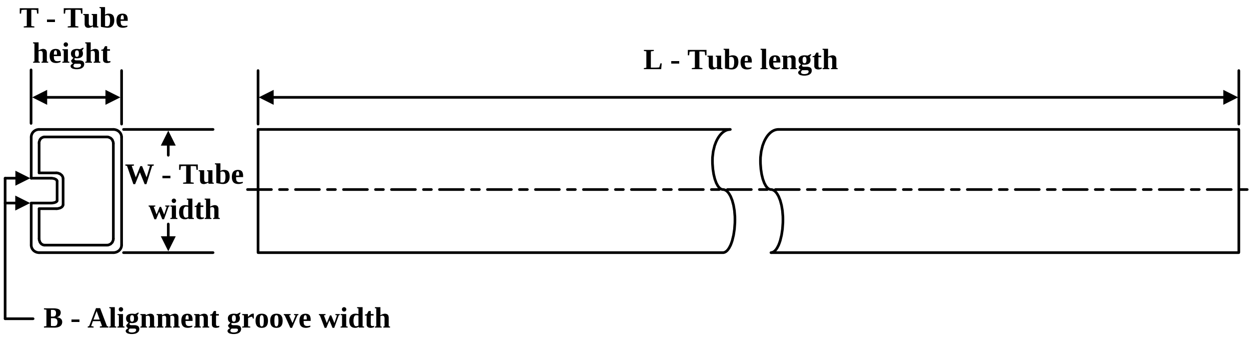
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2340EA/250	VSSOP	DGK	8	250	356.0	356.0	35.0
OPA2340EA/250G4	VSSOP	DGK	8	250	356.0	356.0	35.0
OPA2340EA/2K5	VSSOP	DGK	8	2500	356.0	356.0	35.0
OPA2340EA/2K5G4	VSSOP	DGK	8	2500	356.0	356.0	35.0
OPA2340UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA340NA/250	SOT-23	DBV	5	250	213.0	191.0	35.0
OPA340NA/250	SOT-23	DBV	5	250	180.0	180.0	18.0
OPA340NA/3K	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA340NA/3K	SOT-23	DBV	5	3000	213.0	191.0	35.0
OPA340UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA4340EA/250	SSOP	DBQ	16	250	210.0	185.0	35.0
OPA4340EA/2K5	SSOP	DBQ	16	2500	356.0	356.0	35.0
OPA4340UA/2K5	SOIC	D	14	2500	356.0	356.0	35.0

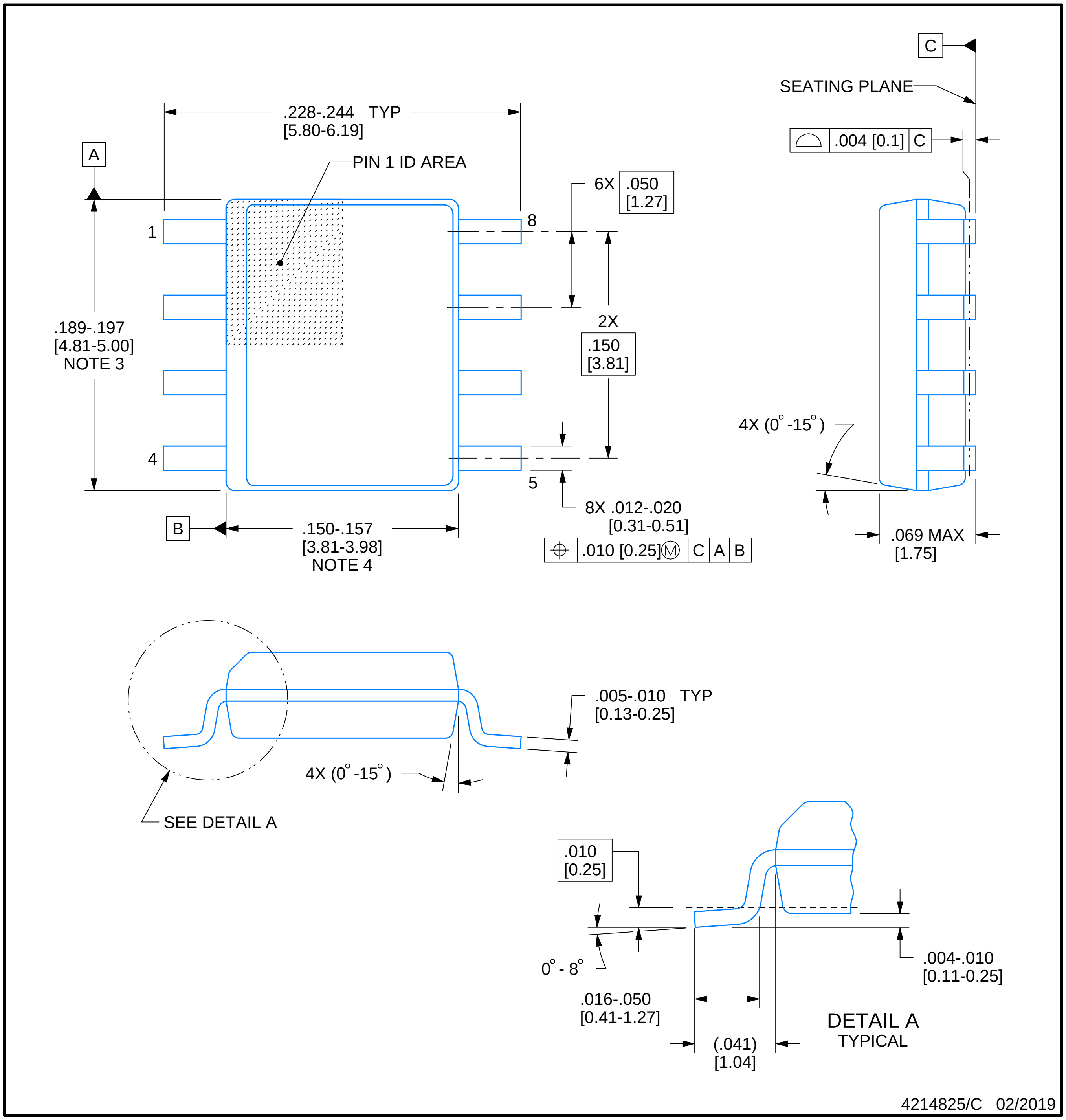
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA2340UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA340PA	P	PDIP	8	50	506	13.97	11230	4.32
OPA340UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA4340UA	D	SOIC	14	50	506.6	8	3940	4.32
OPA4340UAG4	D	SOIC	14	50	506.6	8	3940	4.32

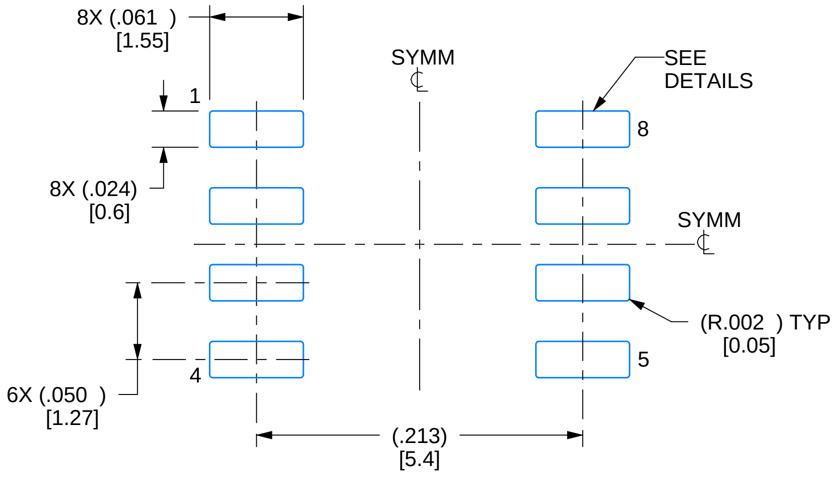
SMALL OUTLINE INTEGRATED CIRCUIT



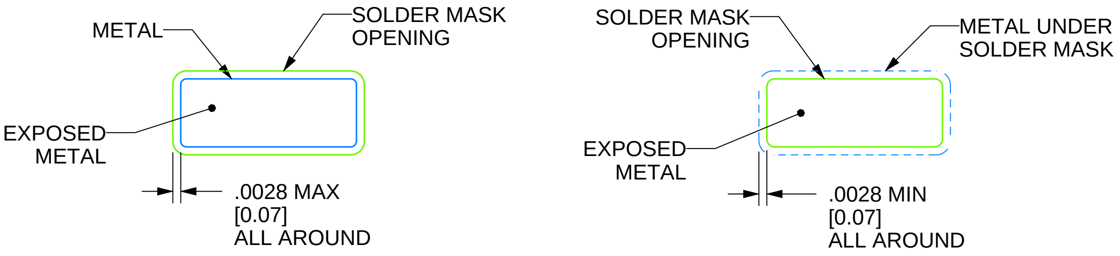
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



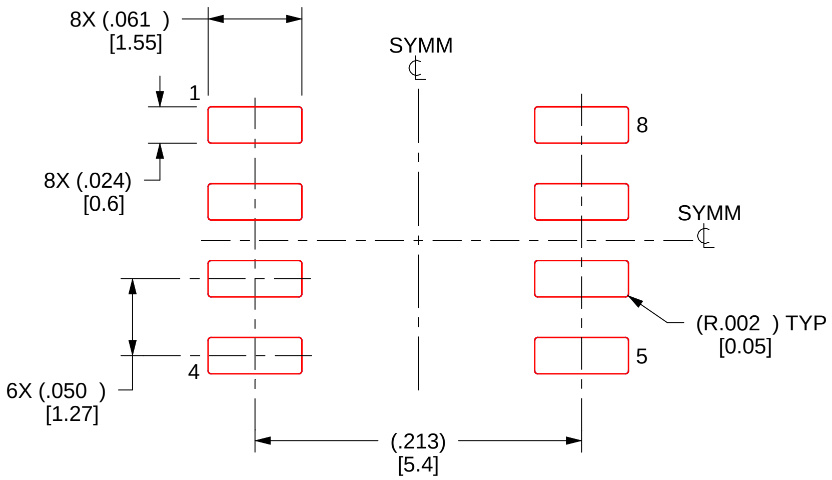
NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

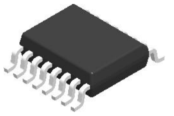


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

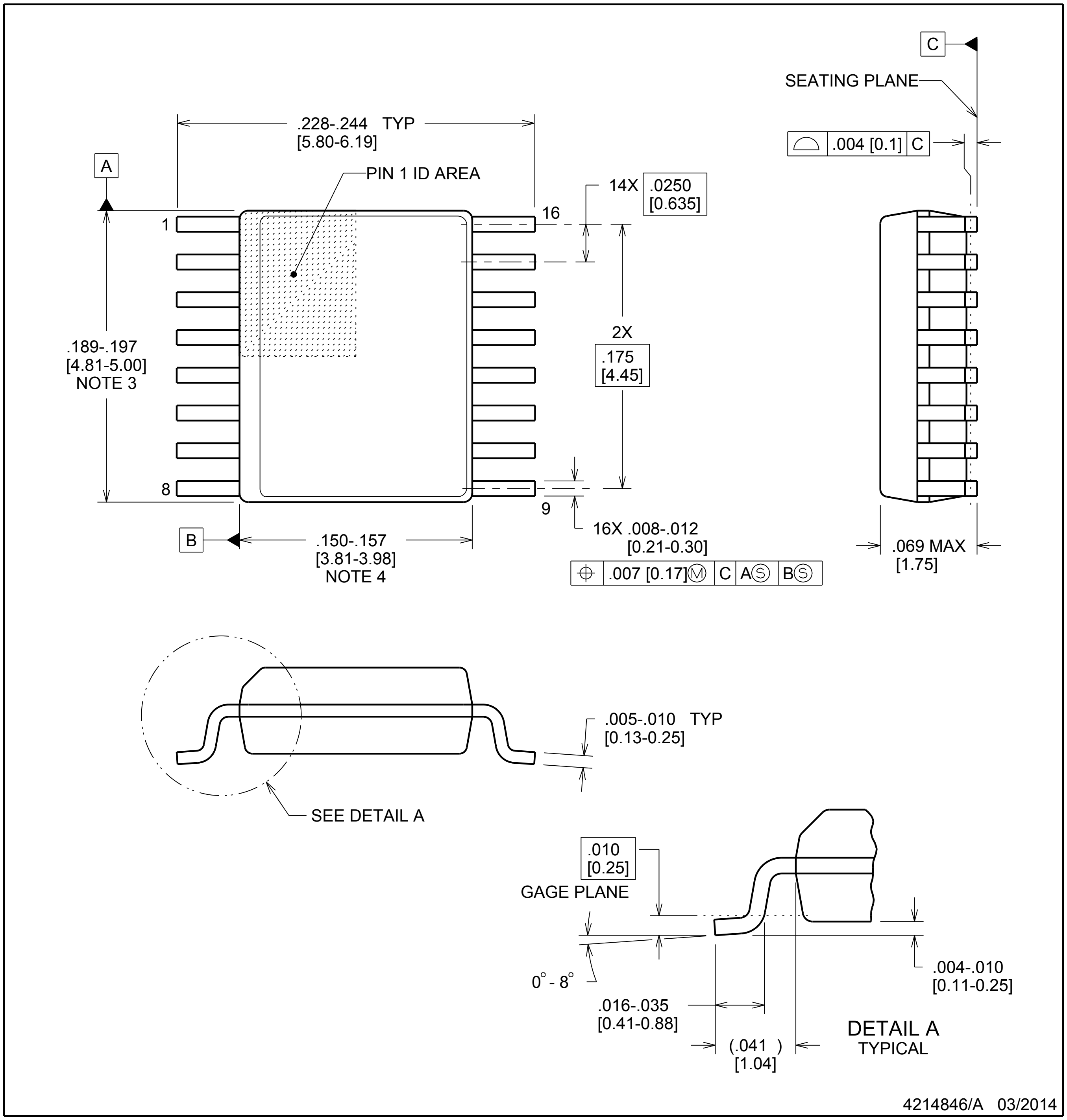


PACKAGE OUTLINE

DBQ0016A

SSOP - 1.75 mm max height

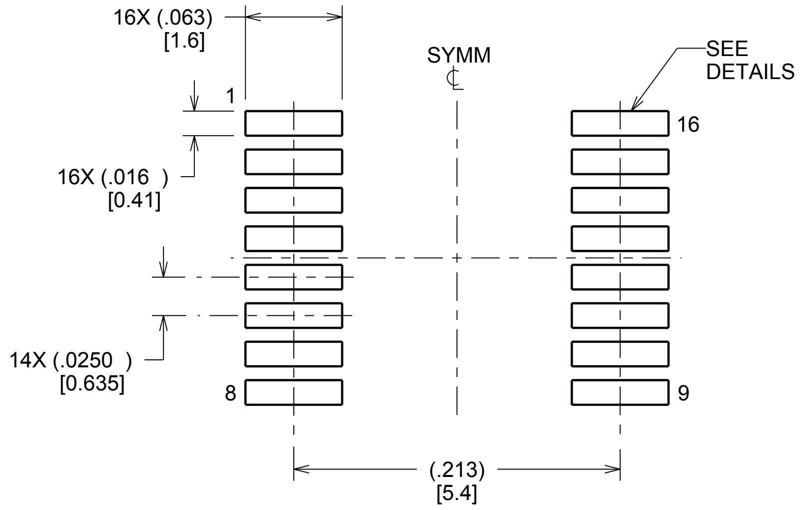
SHRINK SMALL-OUTLINE PACKAGE



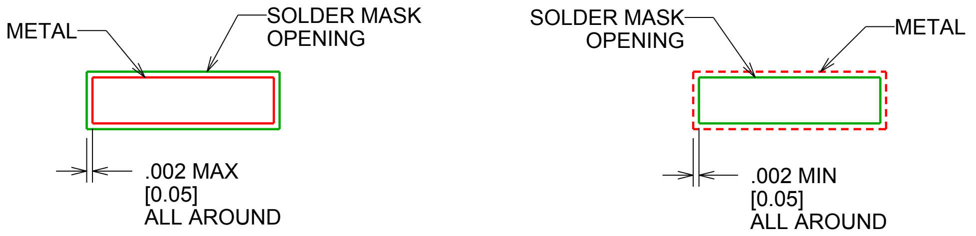
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.

EXAMPLE BOARD LAYOUT



LAND PATTERN EXAMPLE
SCALE:8X



NON SOLDER MASK DEFINED

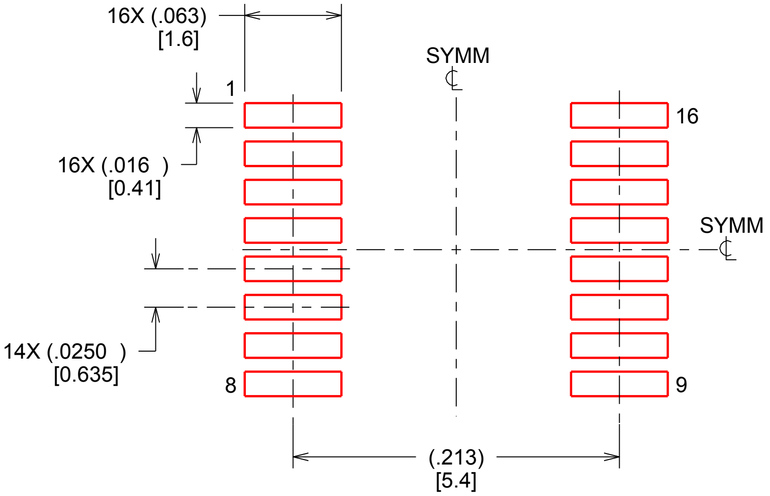
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



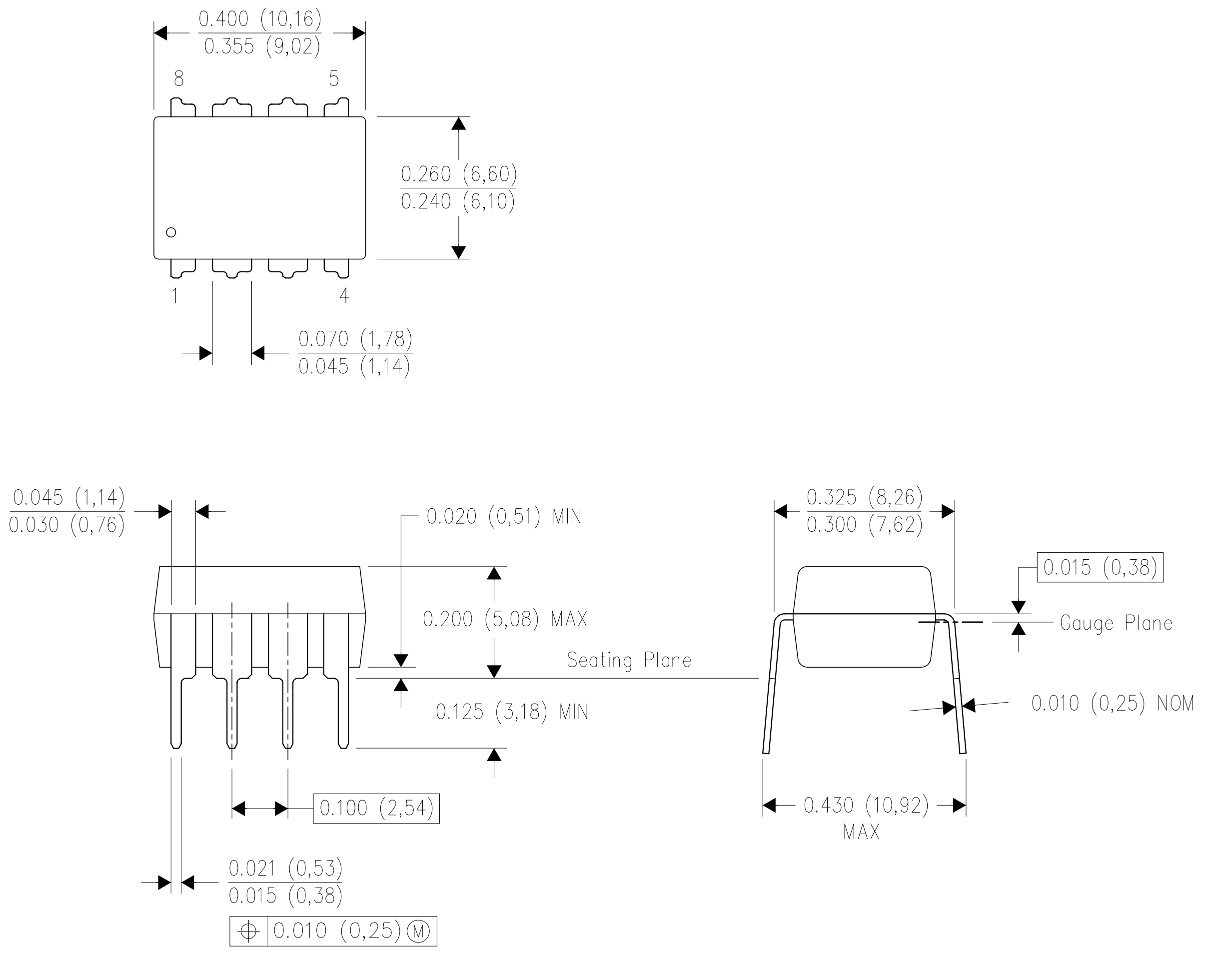
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

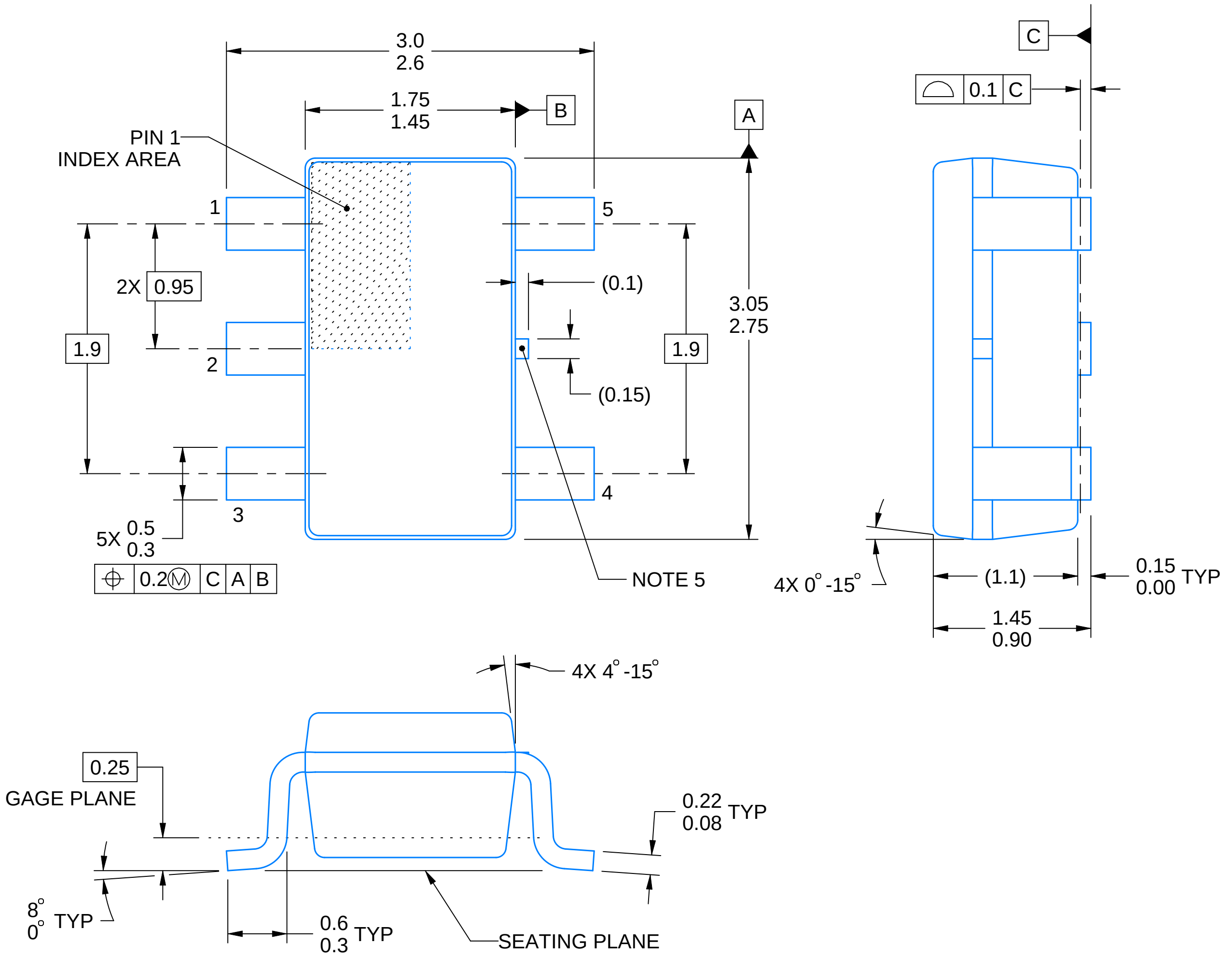
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



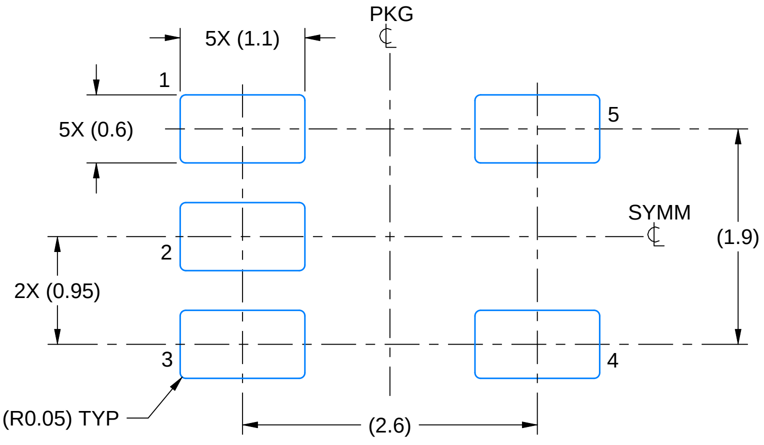
4040082/E 04/2010

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS–001 variation BA.

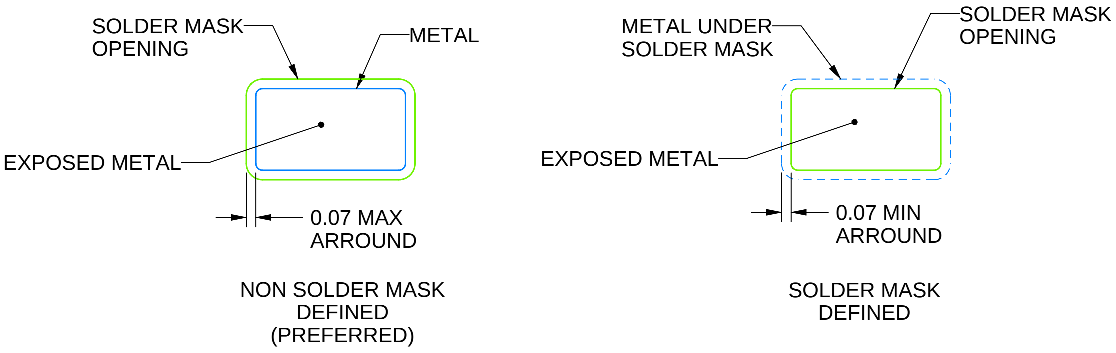


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

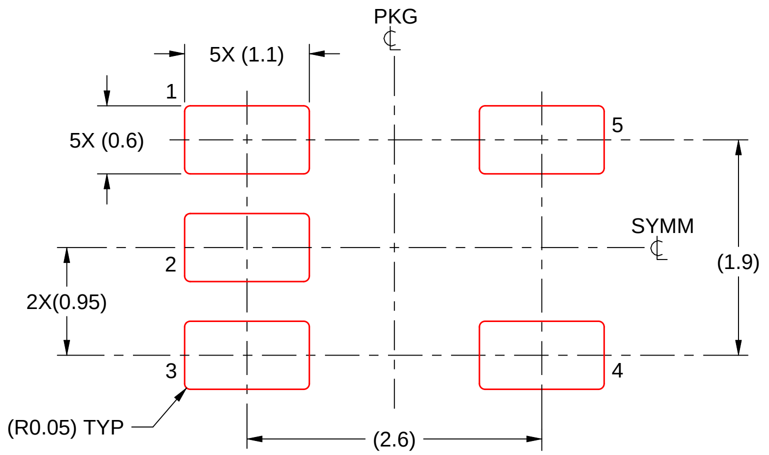


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



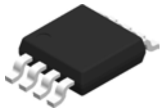
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

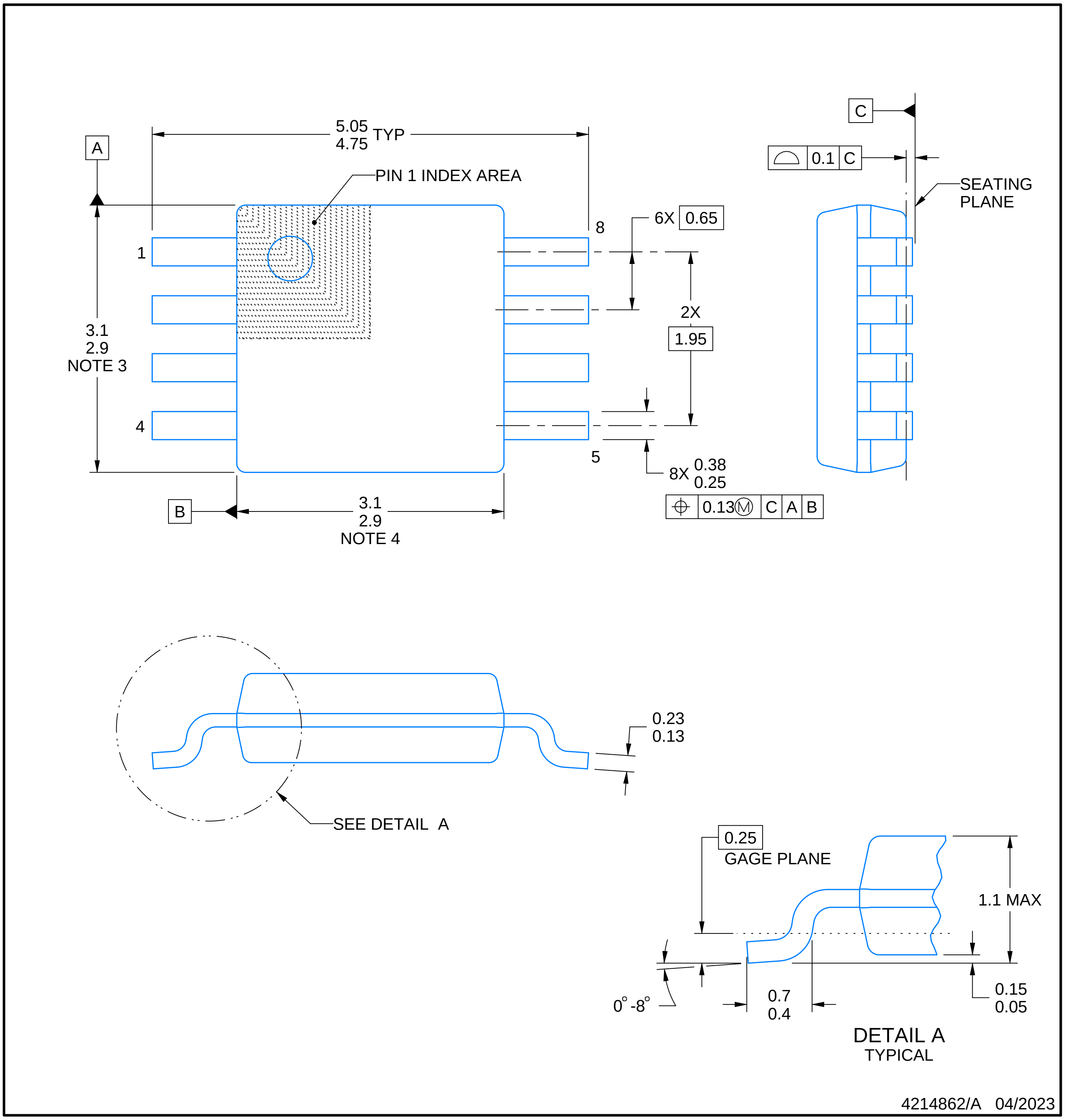
PACKAGE OUTLINE

DGK0008A



VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



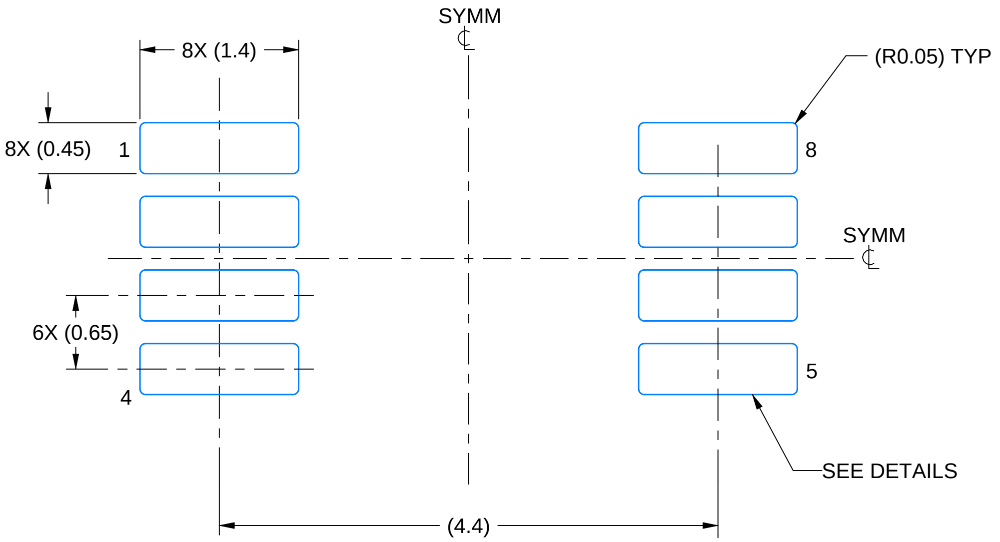
4214862/A 04/2023

PowerPAD is a trademark of Texas Instruments.

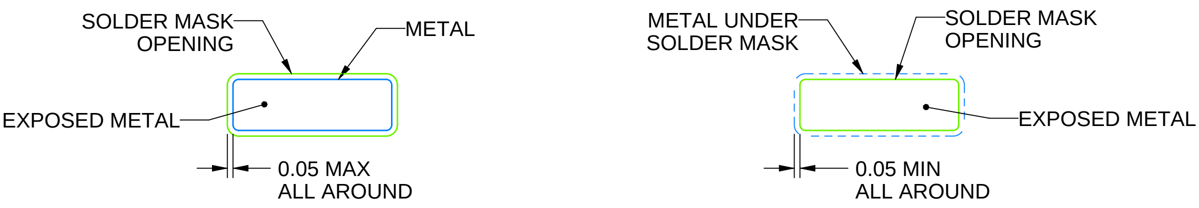
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON-SOLDER MASK
DEFINED
(PREFERRED)

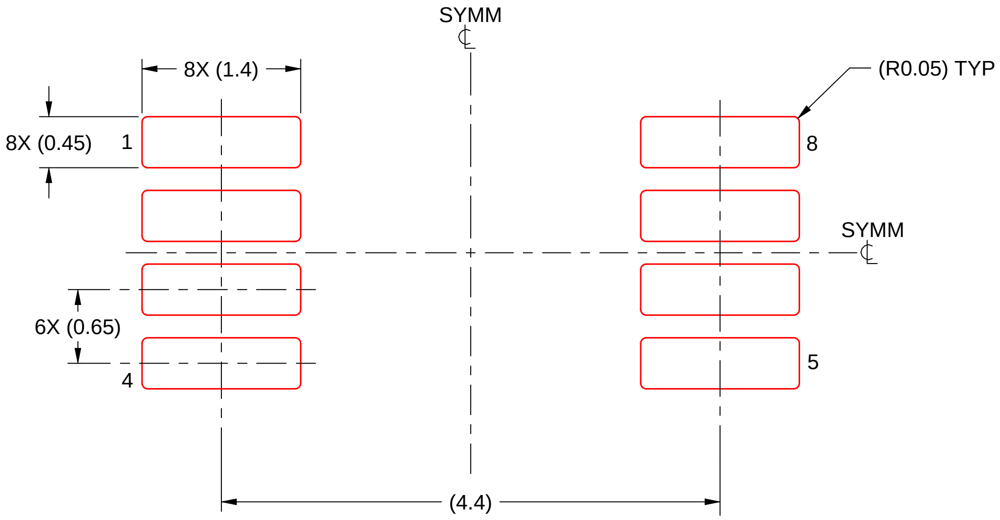
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

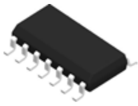


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

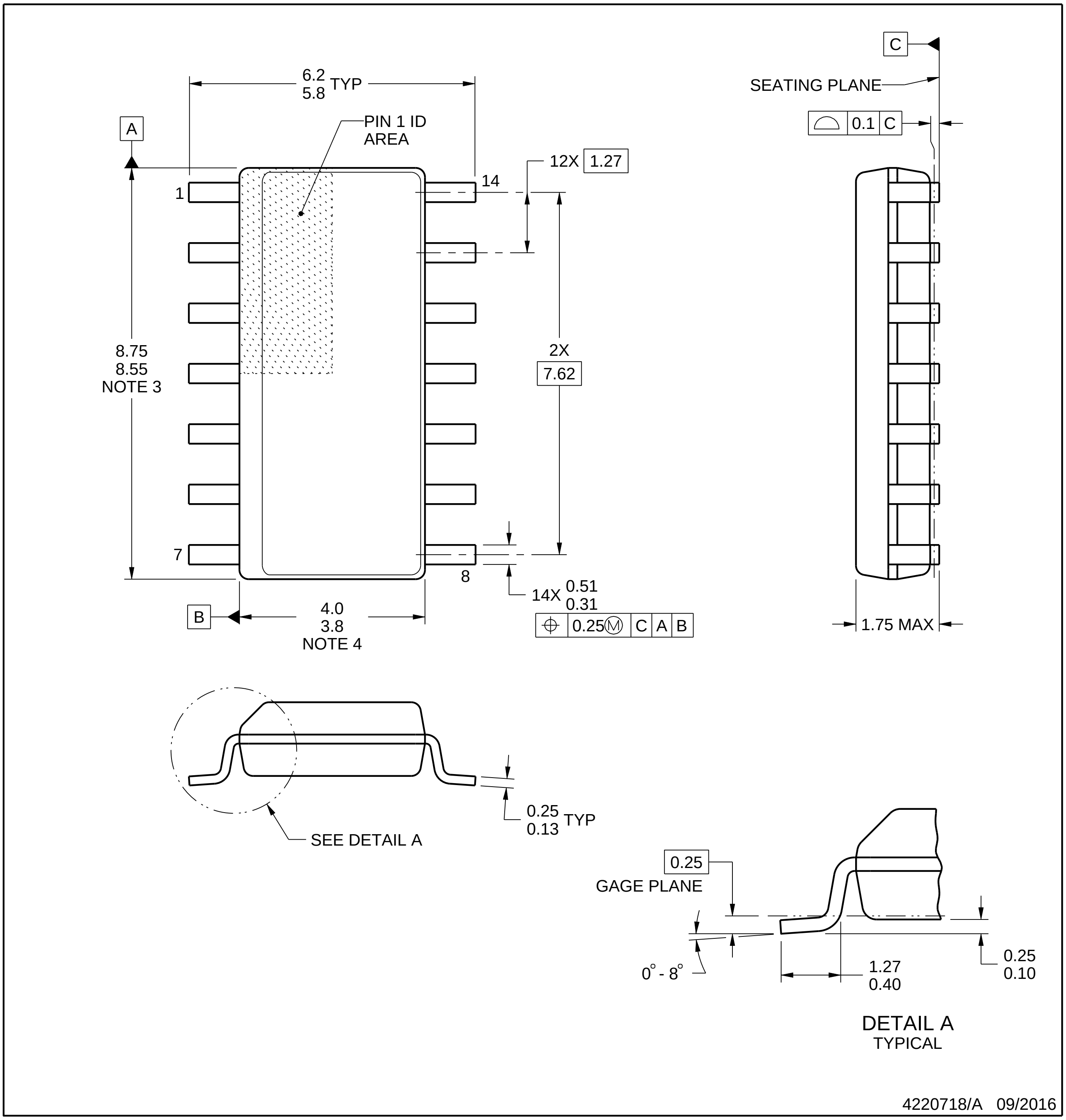


PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

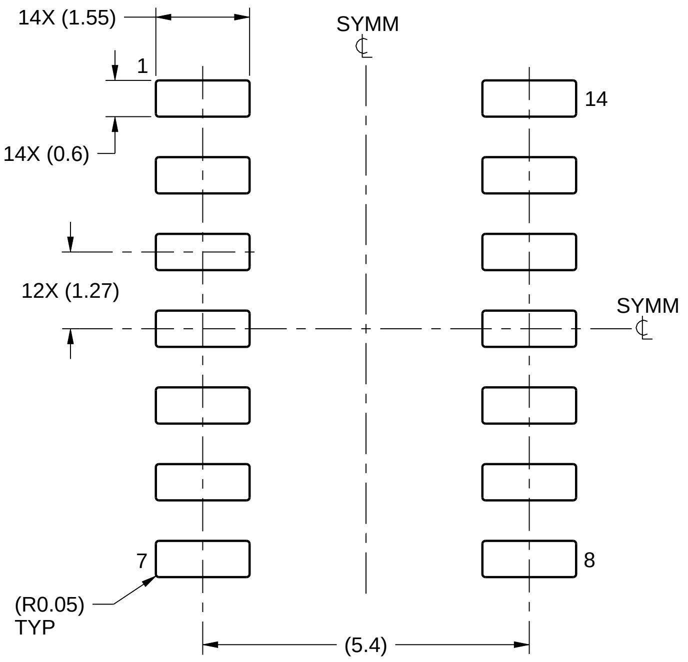
SMALL OUTLINE INTEGRATED CIRCUIT



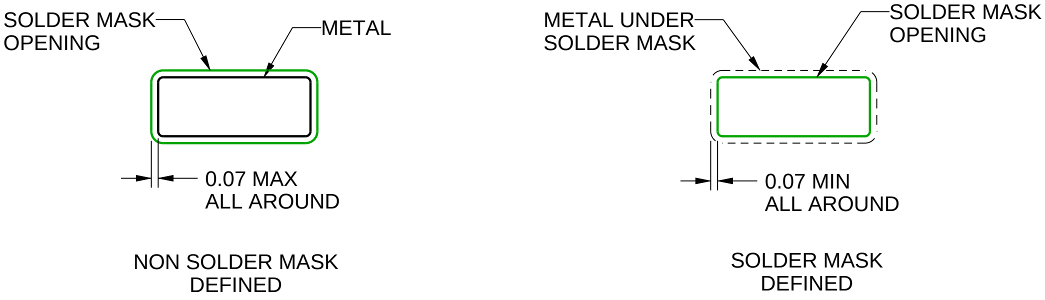
4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X

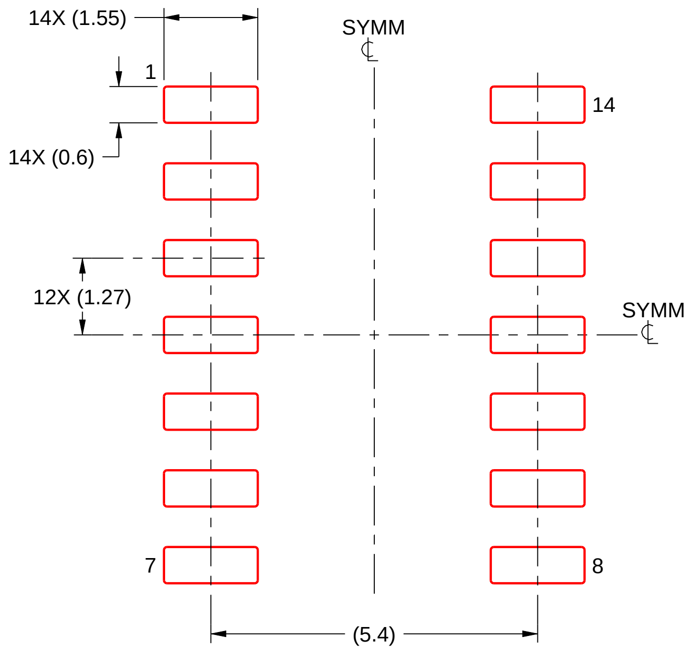


SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.