RC4558 デュアル汎用オペアンプ

1 特長

- 広い同相範囲と差動電圧範囲
- 周波数補償が不要
- 低消費電力
- ラッチアップなし
- ゲイン帯域幅積:4MHz (標準値)
- アンプ間のゲインと位相マッチング
- 低ノイズ:標準値 6.5nV/√Hz (10kHz 時)
- 低い歪みとノイズ:1kHz 時に 0.0001%

2 アプリケーション

- AV レシーバ
- プロフェッショナル オーディオ ミキサ
- サウンドバー
- ワイヤレス スピーカ

3 概要

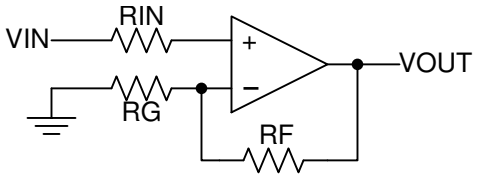
RC4558 デバイスはデュアル汎用オペアンプです。広い電源電圧範囲 (10V～30V)、低ノイズ (6.5nV/√Hz)、歪み性能 (0.0001% THD +N) を兼ね備えているため、RC4558 はさまざまなオーディオ アプリケーションで使用できます。

本デバイスは電圧フォロワー アプリケーション用に設計されており、同相入力電圧範囲が広く、ラッチアップがありません。本デバイスの内部周波数補償機能により、外付け部品を使用しなくても安定性を確保できます。

パッケージ情報 (1)

部品番号	パッケージ	パッケージ サイズ(2)
RC4558	D (SOIC、8)	4.9mm × 6 mm
	DGK (VSSOP、8)	3mm × 4.9 mm
	P (PDIP、8)	9.81mm × 9.43 mm
	PW (TSSOP、8)	3mm × 6.4 mm
	PS (SOP、8)	6.2mm × 7.8 mm

(1) 供給されているすべてのパッケージについては、セクション 10 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



非反転アンプの回路図

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4 Pin Configuration and Functions

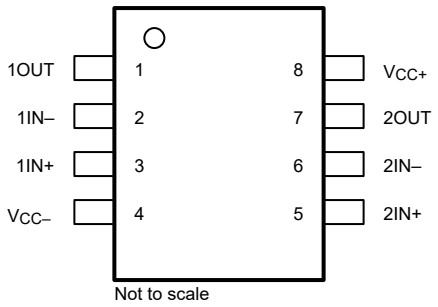


図 4-1. D, DGK, P, PS, or PW Package 8-Pin SOIC, VSSOP, PDIP, TSSOP or SOP (Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
1IN+	3	I	Noninverting input
1IN–	2	I	Inverting Input
1OUT	1	O	Output
2IN+	5	I	Noninverting input
2IN–	6	I	Inverting Input
2OUT	7	O	Output
V_{CC+}	8	—	Positive Supply
$V_{CC–}$	4	—	Negative Supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC+}	Supply voltage(2)		18	V
V_{CC-}			-18	
V_{ID}	Differential input voltage(3)		±30	V
V_I	Input voltage (any input)(2) (4)		±15	V
I_O	Output Current(5)		±125	mA
T_J	Operating virtual junction temperature		150	°C
T_{STG}	Storage temperature	−65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values, unless otherwise noted, are with respect to the midpoint between VCC+ and VCC–.
(3) Differential voltages are at IN+ with respect to IN–.
(4) The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15V, whichever is less
(5) Temperature and supply voltages must be limited to ensure that the dissipation rating is not exceeded.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC+}	Supply voltage		5	15	V
$V_{CC–}$			–5	–15	
T_A	Operating free-air temperature	RC4558	0	70	°C
		RC4558I	–40	85	

5.4 Thermal Information

THERMAL METRIC[1]		RC4558					Unit
		D (SOIC)	DGK (VSSOP)	P (PDIP)	PS (SOP)	PW (TSSOP)	
		8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	120.2	164.8	106	122.9	173.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	59.6	58.8	84.9	60.1	81.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	67.7	99.5	68.6	77.5	112.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.0	3.7	51.6	15.7	16.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	66.7	97.7	67.8	76.0	110.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

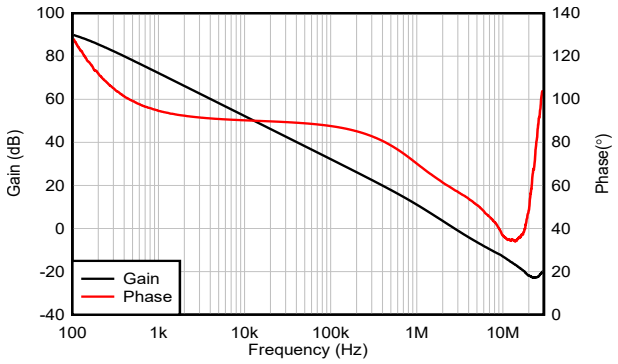
For V_{CC+} = 15 V, V_{CC-} = -15 V at T_A ≅ 25°C, R_L = 2 kΩ unless otherwise noted.

PARAMETER		TEST CONDITIONS(1)	T_A	MIN	TYP	MAX	UNIT
V_{OS}	Input offset voltage	V_O = 0V			0.3	6	mV
			Full range(2)			7.5	
I_{IO}	Input offset current	V_O = 0V			5	200	nA
			Full range(2)			300	
I_{IB}	Input bias current	V_O = 0V			80	500	nA
			Full range(2)			800	
V_{ICR}	Common-mode input voltage range			±12	±14		V
V_{OUT}	Maximum output voltage swing	R_L = 10kΩ		±12	±14.1		V
		R_L = 2kΩ		±10	±13.8		
			Full range(2)	±10			
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 2kΩ, V_O = ±10V		20	830		V/mV
				86	118		dB
			Full range(2)	15			V/mV
				83			dB
GBW	Gain-bandwidth product	f = 10kHz			4		MHz
SSBW	Small-signal bandwidth	V_O = 200mV_{PP}, <1dB peaking			3		MHz
CMRR	Common-mode rejection ratio	(V–) + 3V < V_{ICR} < (V+) – 3V		70	94		dB
	Input impedance	Common-mode			550 || 5.6		MΩ || pF
		Differential			450 || 0.8		kΩ || pF
k_{SVS}	Supply-voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	V_{CC} = ±5V to ±15V			25	150	μV/V
				76	92		dB
e_N	Input voltage noise	f = 0.1Hz to 10Hz			0.38		μV_{PP}
					0.063		μV_{RMS}
	Input voltage noise density	f = 1kHz			7		$nV/\sqrt{Hz}$
		f = 10kHz			6.5		
I_N	Input current noise density	f = 1kHz			0.15		$pA/\sqrt{Hz}$
THD+N	Total harmonic distortion + noise	V_{CC} = 30V, A_{VD} = 1V/V, f = 1kHz, V_O = 3V_{RMS}, R_L = 2kΩ			0.0001		%
					120		dB
I_{CC}	Supply current (both amplifiers)	V_O = 0V, No load			2.5	5.6	mA
			Full range(2)		2.65	6.6	
V_{O1}/V_{O2}	Crosstalk attenuation	R_S = 1kΩ, f = 10kHz, A_{VD} = 1V/V			120		dB
t_r	Rise time	V_I = 20mV, C_L = 100pF			67		ns
	Overshoot	V_I = 20mV, C_L = 100pF			16.8		%
SR	Slew rate	V_{STEP} = 10V, C_L = 100pF		1.1	2.2		V/μs

(1) All characteristics are measured under open-loop conditions with zero common-mode input voltage, unless otherwise specified.
(2) Full range is 0°C to 70°C for RC4558 and –40°C to 85°C for RC4558I.

5.6 Typical Characteristics

at T_A ≅ 25°C, V_{CC} = 30V (±15V), V_{CM} = V_{CC} / 2, R_L = 2kΩ connected to V_{CC} / 2 (unless otherwise noted)



C_L= 22pF

図 5-1. Open-Loop Gain and Phase vs Frequency

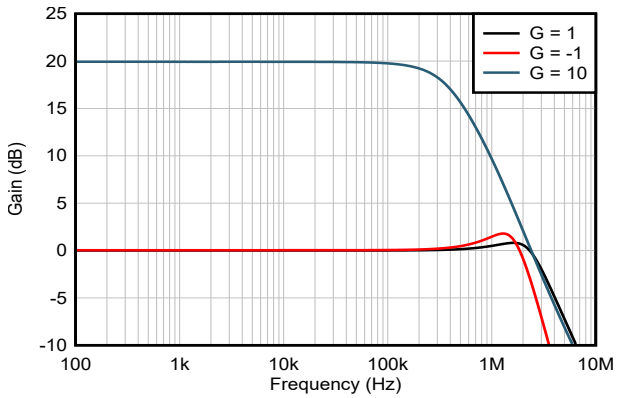


図 5-2. Closed-Loop Gain vs Frequency

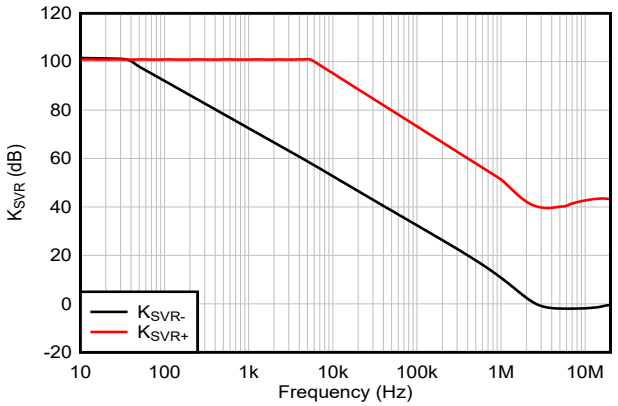


図 5-3. Supply Voltage Sensitivity vs Frequency

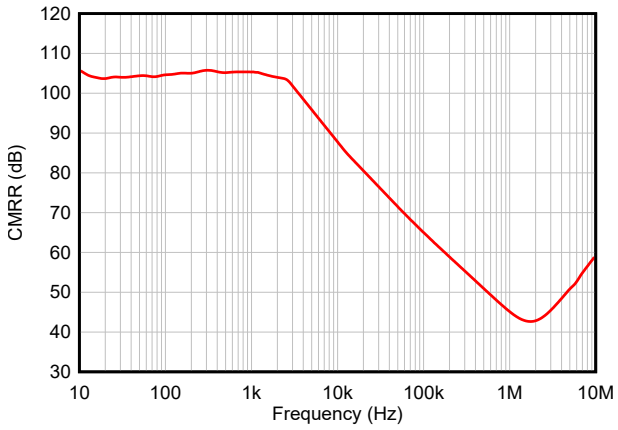


図 5-4. Common-Mode Rejection Ratio vs Frequency

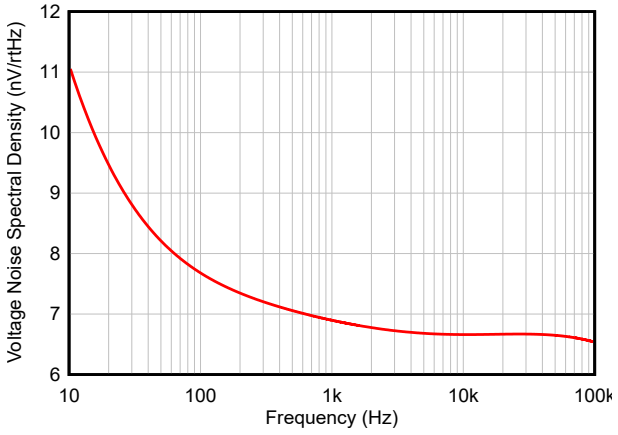


図 5-5. Input Noise Voltage vs Frequency

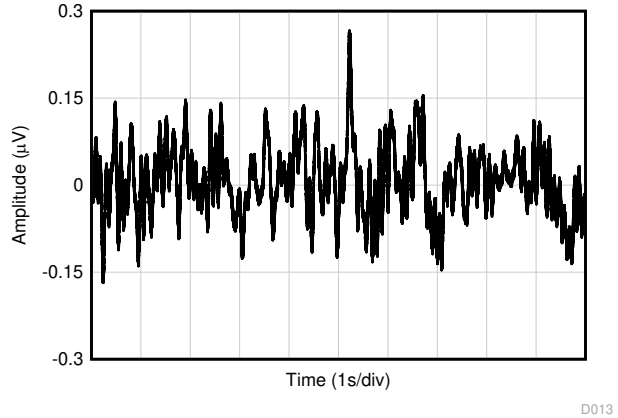
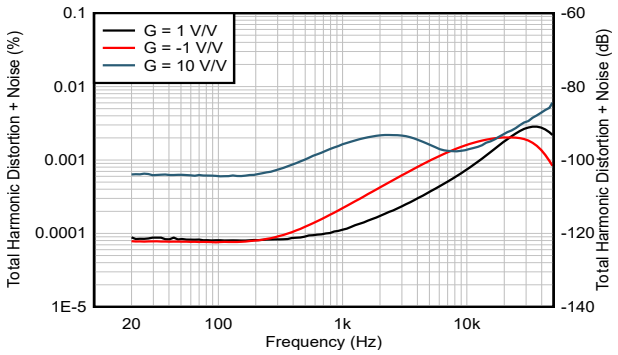
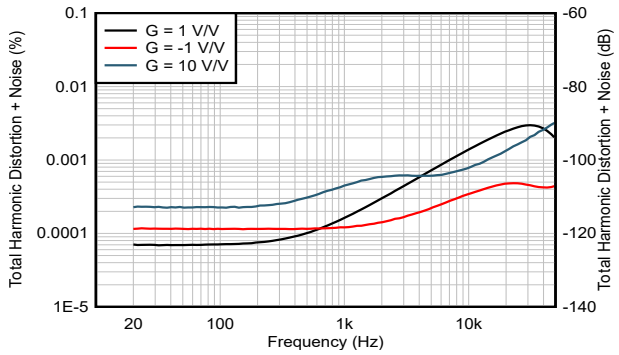


図 5-6. 0.1Hz to 10Hz Noise



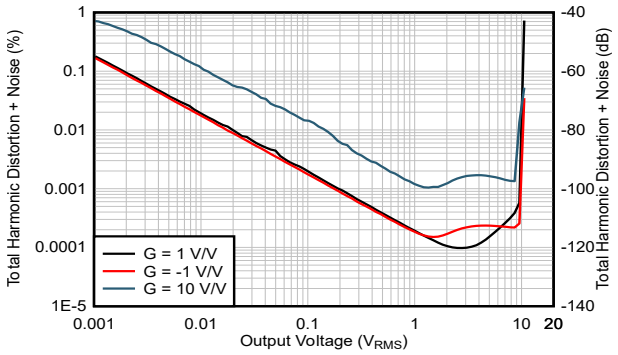
R_L = 2 kΩ

図 5-7. THD+N vs Frequency



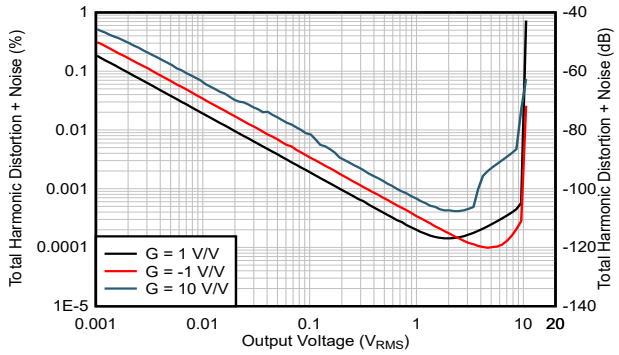
R_L = 10 kΩ

図 5-8. THD+N vs Frequency



R_L = 2 kΩ

図 5-9. THD+N vs Amplitude



R_L = 10 kΩ

図 5-10. THD+N vs Amplitude

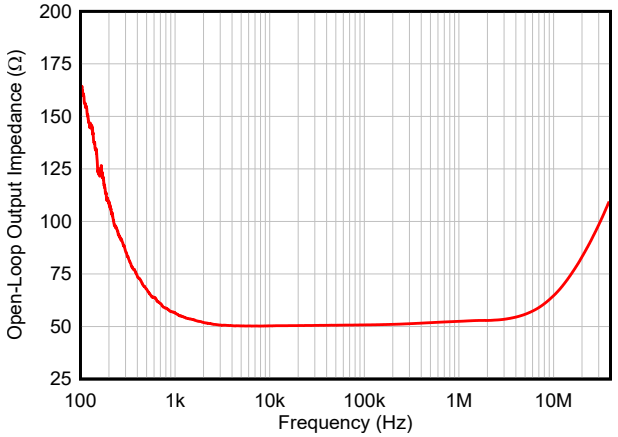


図 5-11. Open-Loop Output Impedance vs Frequency

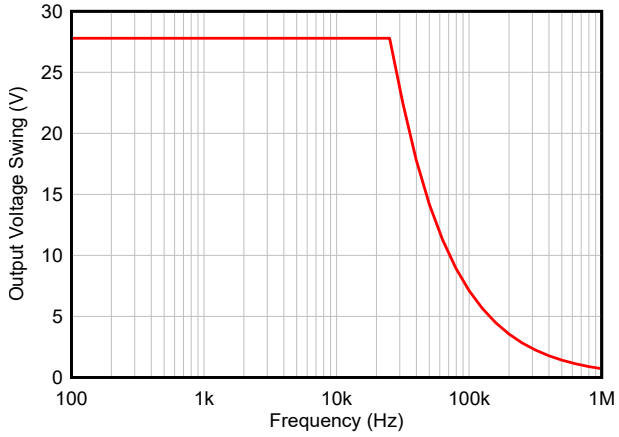
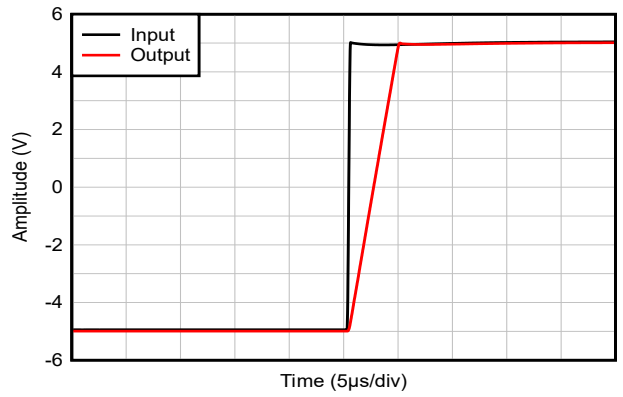
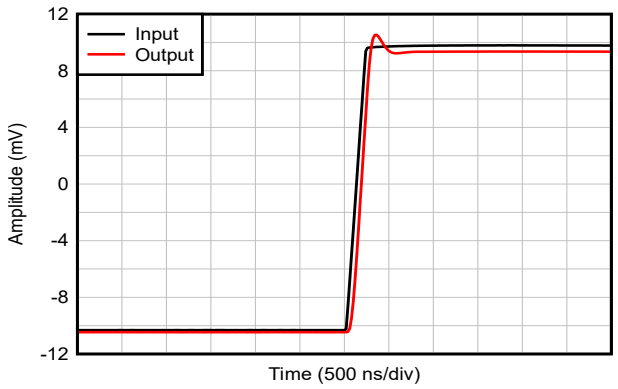


図 5-12. Output Voltage Swing vs Frequency



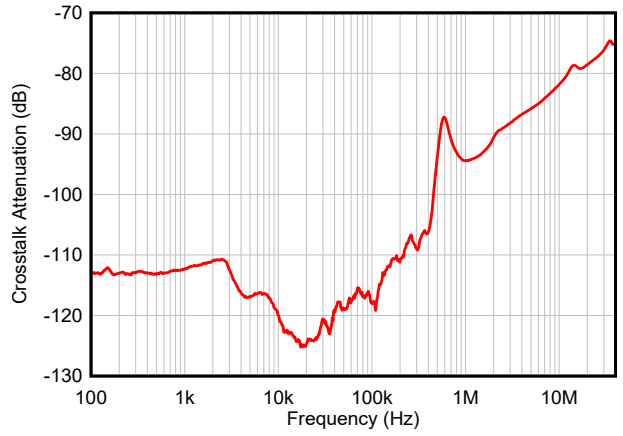
C_L = 100pF, G = 1V/V

図 5-13. Large Signal Step Response



C_L = 100pF, G = 1V/V

図 5-14. Small Signal Step Response



G = 1V/V

図 5-15. Crosstalk Attenuation vs Frequency

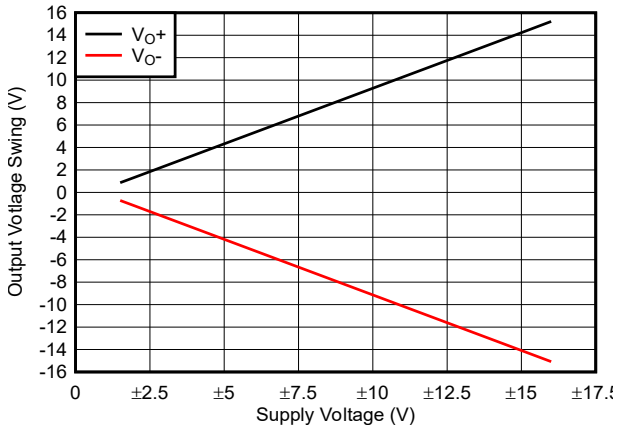


図 5-16. Maximum Output Voltage Swing vs Operating Voltage

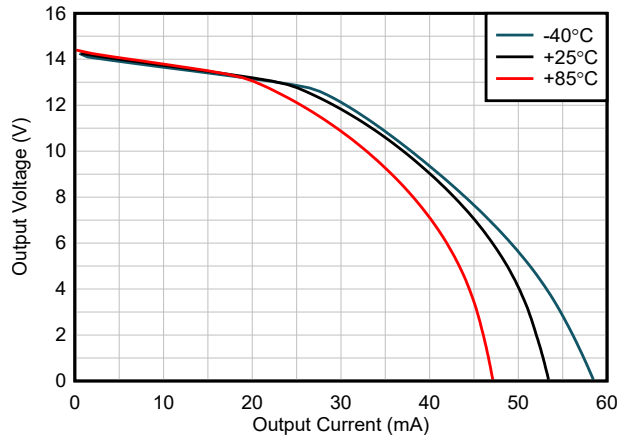


図 5-17. Output Voltage Swing vs Output Current (Sourcing)

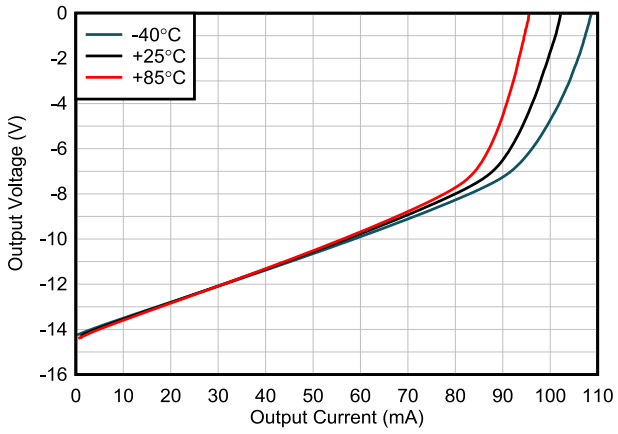


図 5-18. Output Voltage Swing vs Output Current (Sinking)

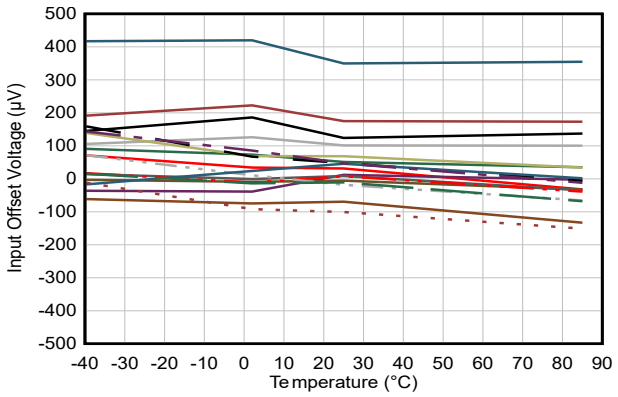


図 5-19. Offset Voltage vs Temperature

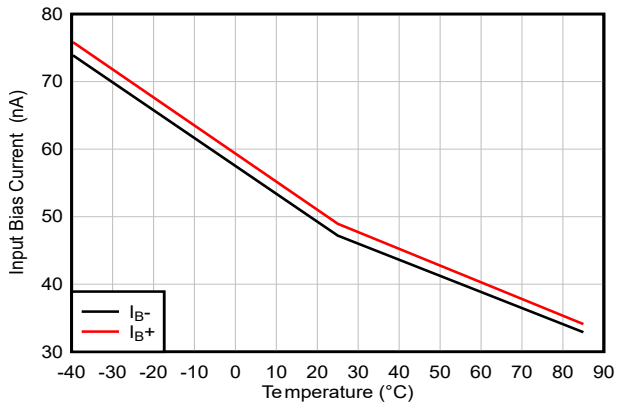


図 5-20. Bias Current vs Temperature

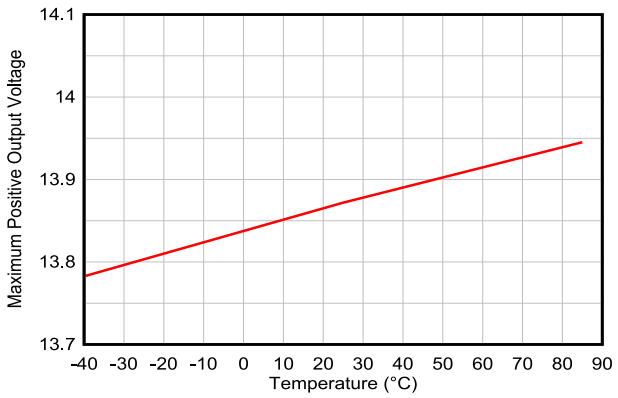


図 5-21. Positive Output Voltage Swing vs Temperature

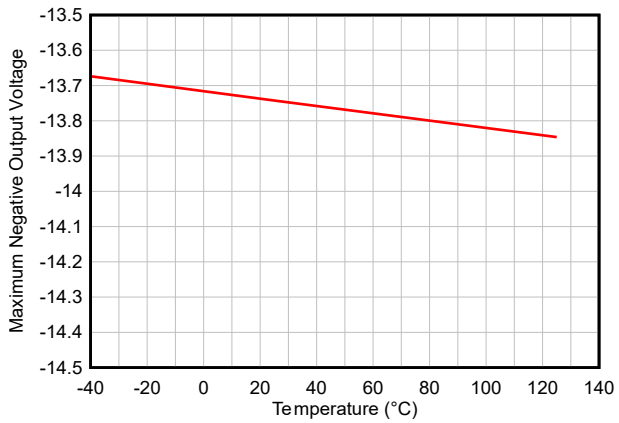


図 5-22. Negative Output Voltage Swing vs Temperature

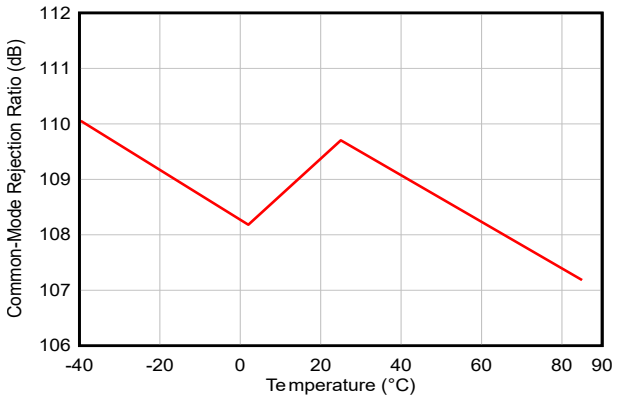


図 5-23. Common-Mode Rejection Ratio vs Temperature

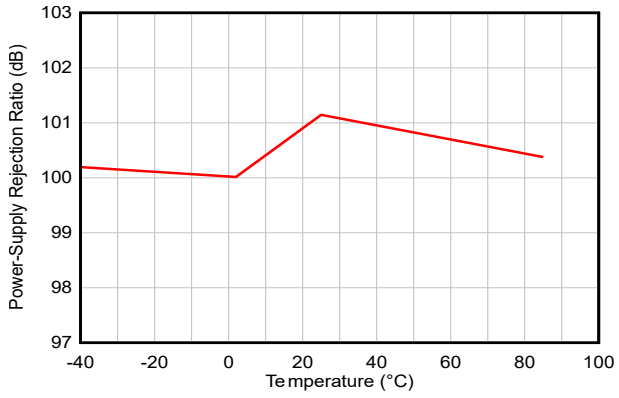


図 5-24. Power Supply Rejection Ratio vs Temperature

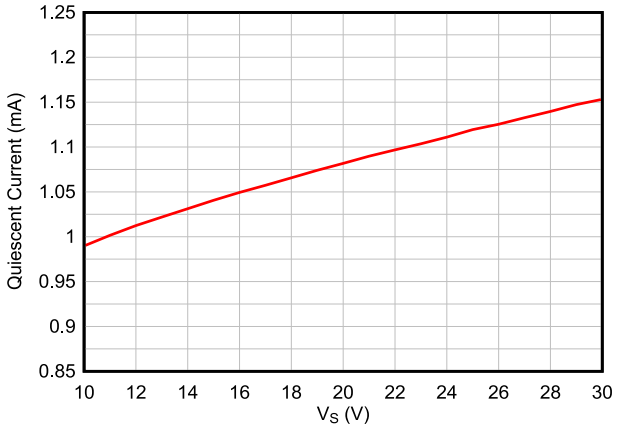


図 5-25. Supply Current vs Supply Voltage

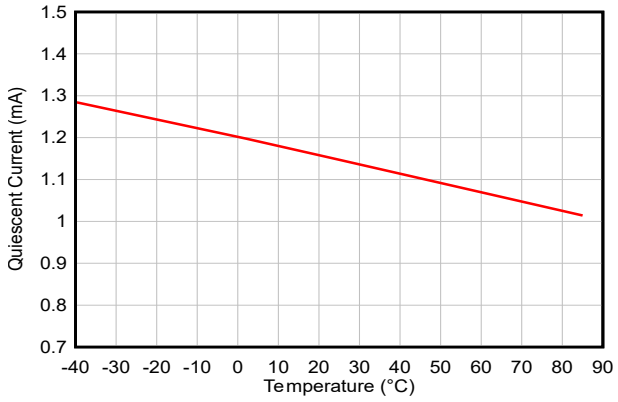


図 5-26. Supply Current vs Temperature

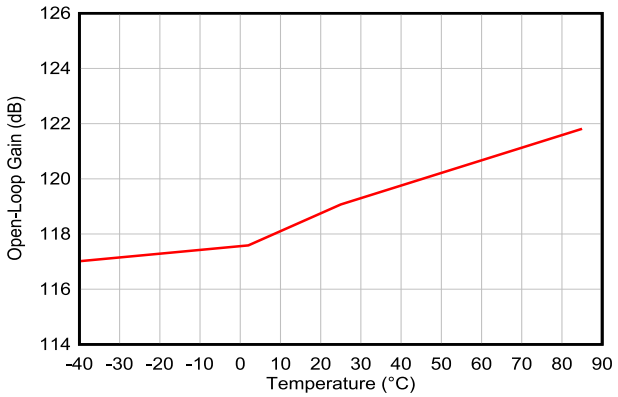


図 5-27. Open-Loop Gain vs Temperature

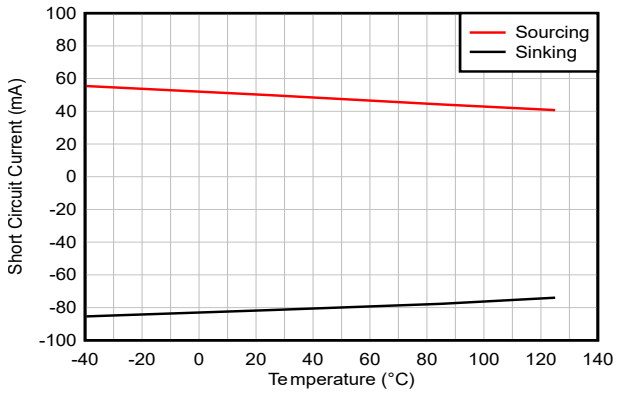


図 5-28. Short-Circuit Current vs Temperature

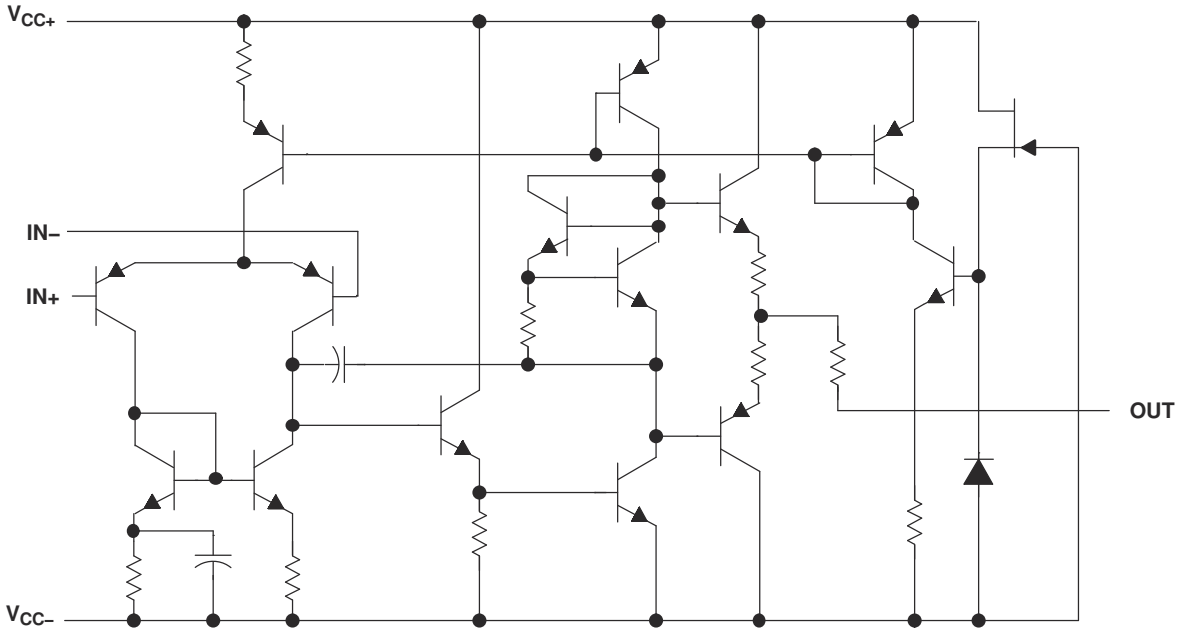
6 Detailed Description

6.1 Overview

The RC4558 device is a dual general-purpose operational amplifier. The combination of the wide supply voltage range (10V to 30V), low noise (6.5nV/√Hz), and distortion performance (0.0001% THD+N) of the device allow the RC4558 to be used in various audio applications.

The high common-mode input voltage range and the absence of latch-up of this device are designed for voltage-follower applications. The internal frequency compensation of the device allows for stability without external components.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Unity-Gain Bandwidth

The unity-gain bandwidth is the frequency up to which an amplifier with a unity gain can be operated without greatly distorting the signal. The RC4558 device has a 4MHz gain-bandwidth product.

6.3.2 Common-Mode Rejection Ratio

The common-mode rejection ratio (CMRR) of an amplifier is a measure of how well the device rejects unwanted input signals common to both input leads. The CMRR is found by taking the ratio of the change in input offset voltage to the change in the input voltage, then converting the ratio to decibels. Ideally the CMRR is infinite, but in practice, amplifiers are designed to have the CMRR as high as possible. The CMRR of the RC4558 device is 94dB.

6.3.3 Slew Rate

The slew rate is the rate at which an operational amplifier can change the output when there is a change on the input. The RC4558 device has a 2.2V/μs slew rate.

6.4 Device Functional Modes

The RC4558 device is powered on when the supply is connected. Each of these devices can be operated as a single-supply operational amplifier or dual-supply amplifier depending on the application.

7 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

7.1 Application Information

The RC4558 is a dual general-purpose device that offers a wide supply range and excellent AC performance. This device operates up to 30V supply rails and offers low noise (6.5nV/$\sqrt{\text{Hz}}$) and distortion performance (0.0001% THD+N). These RC4558 features are designed for both audio and industrial applications.

7.2 Typical Application

Some applications require differential signals. 図 7-1 shows a simple circuit to convert a single-ended input of 2V to 10V into differential output of ±8V on a single 15V supply. The output range is intentionally limited to maximize linearity. The circuit is composed of two amplifiers. One amplifier acts as a buffer and creates a voltage, V_{OUT+}. The second amplifier inverts the input and adds a reference voltage to generate $V_{OUT–}$. Both V_{OUT+} and $V_{OUT–}$ range from 2V to 10V. The difference, V_{DIFF}, is the difference between V_{OUT+} and $V_{OUT–}$.

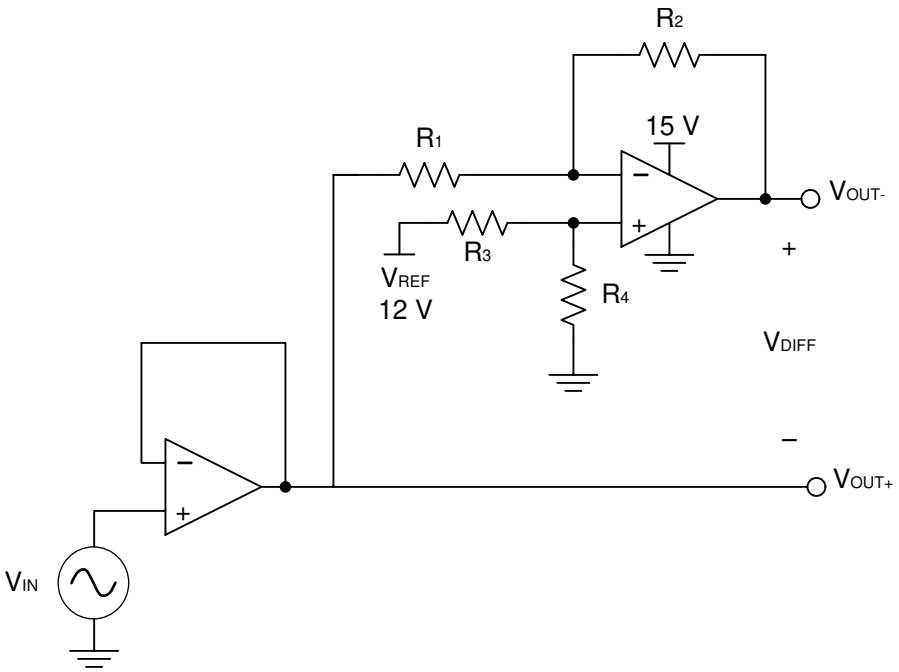


図 7-1. Schematic for Single-Ended Input to Differential Output Conversion

7.2.1 Design Requirements

The design requirements are as follows:

- Supply voltage: 15V
- Reference voltage: 12V
- Input: 2V to 10V
- Output differential: ±8V

7.2.2 Detailed Design Procedure

The circuit in 図 7-1 takes a single-ended input signal, V_{IN}, and generates two output signals, V_{OUT+} and $V_{OUT–}$, using two amplifiers and a reference voltage, V_{REF}. V_{OUT+} is the output of the first amplifier and is a buffered version of the input signal, V_{IN} (see 式 1). $V_{OUT–}$ is the output of the second amplifier which uses V_{REF} to add an offset voltage to V_{IN} and feedback to add inverting gain. The transfer function for $V_{OUT–}$ is 式 2.

$$V_{OUT+} = V_{IN} \tag{1}$$

$$V_{OUT-} = V_{REF} \times \left(\frac{R_4}{R_3 + R_4}\right) \times \left(1 + \frac{R_2}{R_1}\right) - V_{IN} \times \frac{R_2}{R_1} \tag{2}$$

The differential output signal, V_{DIFF}, is the difference between the two single-ended output signals, V_{OUT+} and $V_{OUT–}$. 式 3 shows the transfer function for V_{DIFF}. By applying the conditions that $R_1 = R_2$ and $R_3 = R_4$, the transfer function is simplified into 式 6. Using this configuration, the maximum input signal is equal to the reference voltage and the maximum output of each amplifier is equal to the V_{REF}. The differential output range is $2 \times V_{REF}$. Furthermore, the common-mode voltage is one half of V_{REF} (see 式 7).

$$V_{DIFF} = V_{OUT+} - V_{OUT-} = V_{IN} \times \left(1 + \frac{R_2}{R_1}\right) - V_{REF} \times \left(\frac{R_4}{R_3 + R_4}\right)\left(1 + \frac{R_2}{R_1}\right) \tag{3}$$

$$V_{OUT+} = V_{IN} \tag{4}$$

$$V_{OUT-} = V_{REF} - V_{IN} \tag{5}$$

$$V_{DIFF} = 2 \times V_{IN} - V_{REF} \tag{6}$$

$$V_{CM} = \left(\frac{V_{OUT+} + V_{OUT-}}{2}\right) = \frac{1}{2}V_{REF} \tag{7}$$

7.2.2.1 Amplifier Selection

Linearity over the input range is key for good DC accuracy. The common-mode input range and the output swing limitations determine the linearity. In general, an amplifier with rail-to-rail input and output swing is required. Bandwidth is a key concern for this design. The RC4558 device has a bandwidth of 4MHz, therefore this circuit can only process signals with frequencies of less than 4MHz.

7.2.2.2 Passive Component Selection

The transfer function of $V_{OUT–}$ is heavily reliant on resistors (R_1, R_2, R_3, and R_4), therefore TI recommends to use resistors with low tolerances to maximize performance and minimize error. This design uses resistors with resistance values of
36kΩ with tolerances measured to be within 2% of these resistor values. If the noise of the system is a key parameter, the user can select smaller resistance values (6kΩ or lower) to keep the overall system noise low and the noise from the resistors lower than the amplifier noise.

7.2.3 Application Curves

The measured transfer functions in 図 7-2, 図 7-3, and 図 7-4 were generated by sweeping the input voltage from 0V to 12V. However, this design must only be used between 2V and 10V for optimum linearity.

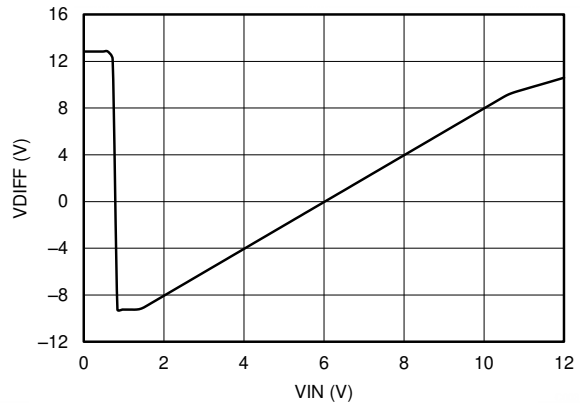


図 7-2. Differential Output Voltage Node vs Input Voltage

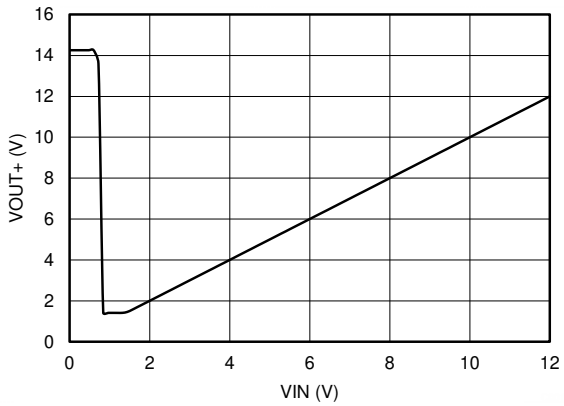


図 7-3. Positive Output Voltage Node vs Input Voltage

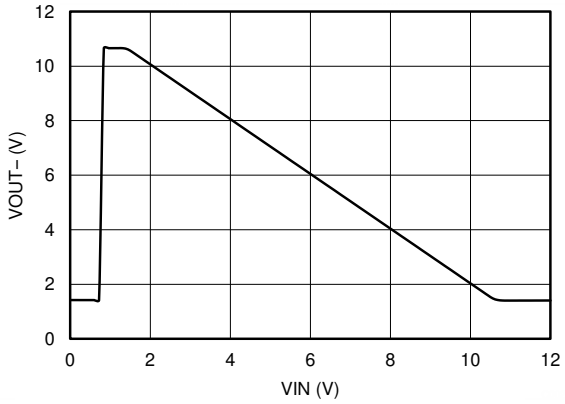


図 7-4. Positive Output Voltage Node vs Input Voltage

7.3 Power Supply Recommendations

The RC4558 device is specified for ±5V to ±15V operation; many specifications apply for –0°C to 70°C. The *Typical Characteristics* section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

> **注意**
>
> Supply voltages outside of the ±18V range can permanently damage the device (see the *Absolute Maximum Ratings*).

Place 0.1µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout Guidelines*.

7.4 Layout

7.4.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the operational amplifier and the power pins of the circuit as a whole. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separating grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep the traces separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in *Layout Example*.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

7.4.2 Layout Example

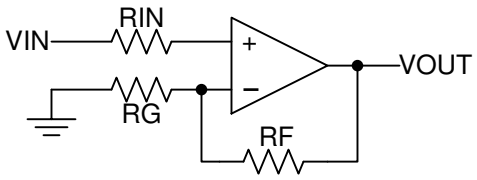


図 7-5. Operational Amplifier Schematic for Noninverting Configuration

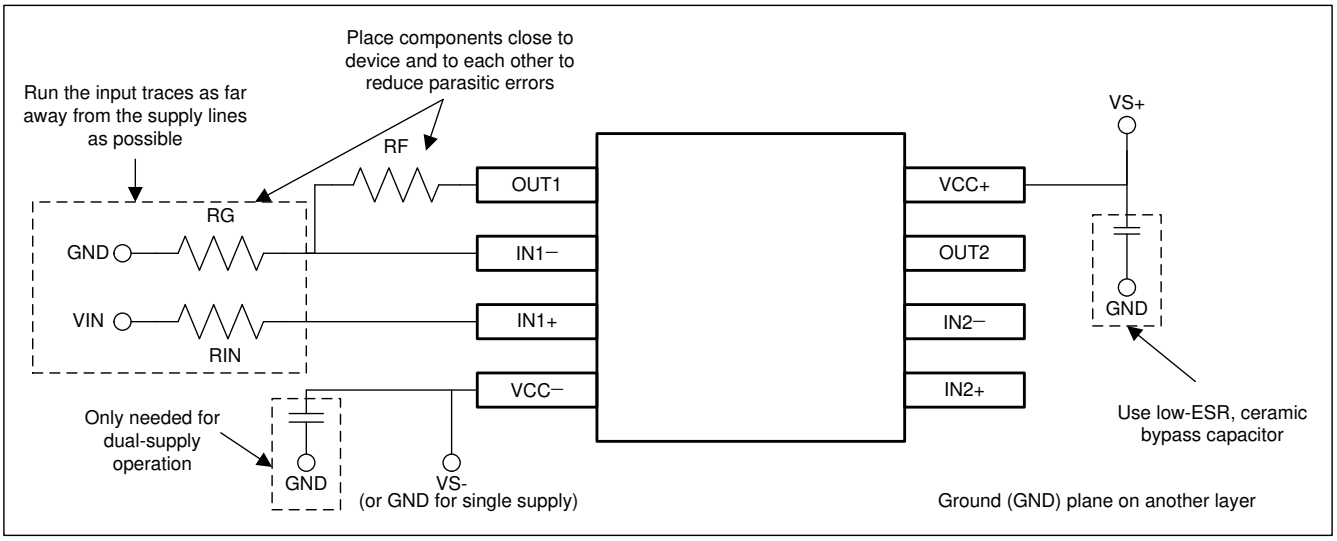


図 7-6. Operational Amplifier Board Layout for Noninverting Configuration

8 Device and Documentation Support

8.1 Trademarks

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8.2 静電気放電に関する注意事項

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8.3 Glossary

SLYZ022 — *TI Glossary.*

This glossary lists and explains terms, acronyms and definitions.

9 Revision History

Changes from Revision G (November 2014) to Revision H (October 2024)	Page
• 「仕様」セクションに記載されている変更を反映するため、「特長」、「アプリケーション」、「概要」、「詳細説明」、「機能説明」、「詳細な設計手順」および「レイアウトのガイドライン」セクションを更新	1
• 「製品情報」表を「パッケージ情報」に変更	1
• Removed *Duration of output short circuit to ground* specification and added maximum output current of ±125mA in *Absolute Maximum Ratings* table	4
• Updated *Handling Ratings* table to *ESD Ratings* table	4
• Updated *Thermal Information* table	5
• Changed the typical *input offset voltage* value from: 0.5mV to 0.3mV in the *Electrical Characteristics* table	6
• Changed the typical *Input bias current* value from: 150nA to 80nA in the *Electrical Characteristics* table	6
• Changed the typical *maximum output voltage swing* value at R_L = 10kΩ from ±14V to ±14.1V in the *Electrical Characteristics* table	6
• Changed the typical *maximum output voltage swing* value at R_L = 2kΩ from: ±13V to ±13.8V in the *Electrical Characteristics* table	6
• Changed the typical *large-signal differential voltage amplification* value from: 300V/mV to 830V/mV in the *Electrical Characteristics* table	6
• Added line items for the *large-signal voltage amplification* parameter to show values in dB units in the *Electrical Characteristics* table	6
• Changed *unity gain-bandwidth* parameter to *gain-bandwidth product* and changed the typical value from: 3MHz to 4MHz in the *Electrical Characteristics* table	6
• Added the *small-signal bandwidth* parameter in the *Electrical Characteristics* table	6
• Added test condition to the *common-mode rejection ratio* parameter in the *Electrical Characteristics* table	6
• Changed the typical *common-mode rejection ratio* value from: 90dB to 94dB in the *Electrical Characteristics* table	6
• Removed the minimum limit for the *input resistance* parameter in the *Electrical Characteristics* table	6
• Updated the *input resistance* parameter to *input impedance* to better reflect device characteristics in the *Electrical Characteristics* table	6
• Changed the test condition of the *supply-voltage sensitivity* parameter from: V_{CC} = *±15V to ±9V* to V_{CC} = *±5V to ±15V* in the *Electrical Characteristics* table	6
• Updated the typical *supply-voltage sensitivity* value from: 30µV/V to 25µV/V in the *Electrical Characteristics* table	6
• Added line items for *supply-voltage sensitivity* parameter to show values in dB units in the *Electrical Characteristics* table	6
• Added *input voltage noise* parameter to the *Electrical Characteristics* table	6

- Changed test conditions of *equivalent input noise voltage (closed loop)* parameter to f = 1 kHz in the *Electrical Characteristics* table.... 6
- Changed typical *equivalent input noise voltage (closed loop)* at f = 1 kHz from 8 nV/√Hz to 7 nV/√Hz in the *Electrical Characteristics* table.... 6
- Changed *equivalent input noise voltage (closed loop)* specification to *input voltage noise density* in the *Electrical Characteristics* table.... 6
- Added *f = 10 kHz* test condition to *equivalent input noise voltage (closed loop)* specification in the *Electrical Characteristics* table.... 6
- Added the *input current noise density* parameter to the *Electrical Characteristics* table.... 6
- Removed the *total power dissipation* parameter in the *Electrical Characteristics* table.... 6
- Changed T_A *min* and T_A *max* conditions for supply current to one full range temperature condition in the *Electrical Characteristics* table.... 6
- Changed the typical *supply current (both amplifiers)* value at full temperature range from: 3 mA to 2.65 mA in the *Electrical Characteristics* table.... 6
- Changed the test condition for the *crosstalk attenuation* parameter from *Open loop* & A_{VD} *= 100 V/V* to A_{VD} *= 1V/V* in the *Electrical Characteristics* table.... 6
- Changed the typical *crosstalk attenuation* value from: 105dB to 120 dB in the *Electrical Characteristics* table 6
- Changed the *rise time* typical value from: 0.13 ns to 67 ns in the *Electrical Characteristics* table.... 6
- Changed the *overshoot* typical value from: 5% to 16.8% in the *Electrical Characteristics* table.... 6
- Changed the *slew rate* typical value from: 1.7V/µs to 2.2V/µs in the *Electrical Characteristics* table.... 6
- Changed and added graphs to the *Typical Characteristics* section.... 7

Changes from Revision F (September 2010) to Revision G (November 2014) Page

- 「アプリケーション」、「デバイス情報」表、「取り扱い定格」表、「機能説明」セクション、「デバイスの機能モード」、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 1
- 「注文情報」表を削除。 1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
RC4558D	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	0 to 70	RC4558	
RC4558DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	0 to 70	(YRP, YRS, YRU)	Samples
RC4558DGKRG4	ACTIVE	VSSOP	DGK	8	2500	TBD	Call TI	Call TI	0 to 70		Samples
RC4558DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	RC4558	Samples
RC4558DRG3	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	0 to 70	RC4558	
RC4558DRG4	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	0 to 70	RC4558	
RC4558ID	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	R4558I	
RC4558IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(YSP, YSS, YSU)	Samples
RC4558IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	R4558I	Samples
RC4558IP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	RC4558IP	Samples
RC4558IPW	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI	-40 to 85	R4558I	
RC4558IPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	R4558I	Samples
RC4558P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	RC4558P	Samples
RC4558PSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	R4558	Samples
RC4558PSRG4	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	R4558	Samples
RC4558PW	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI	0 to 70	R4558	
RC4558PWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	R4558	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

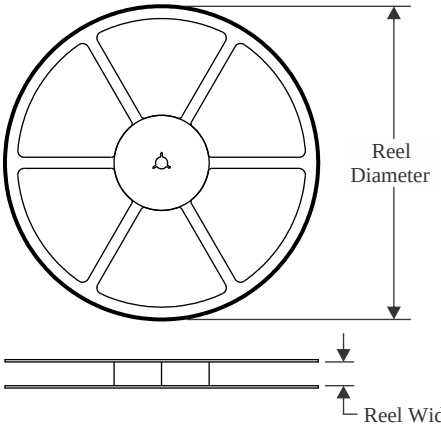
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

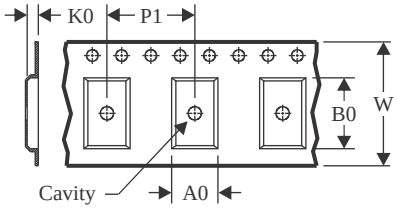
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

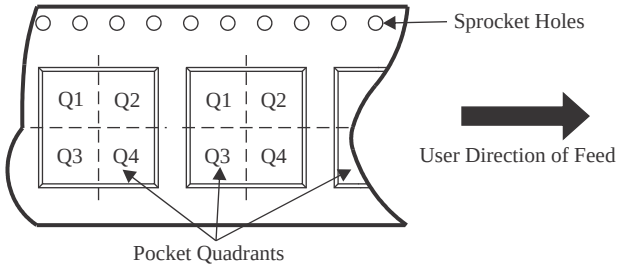


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

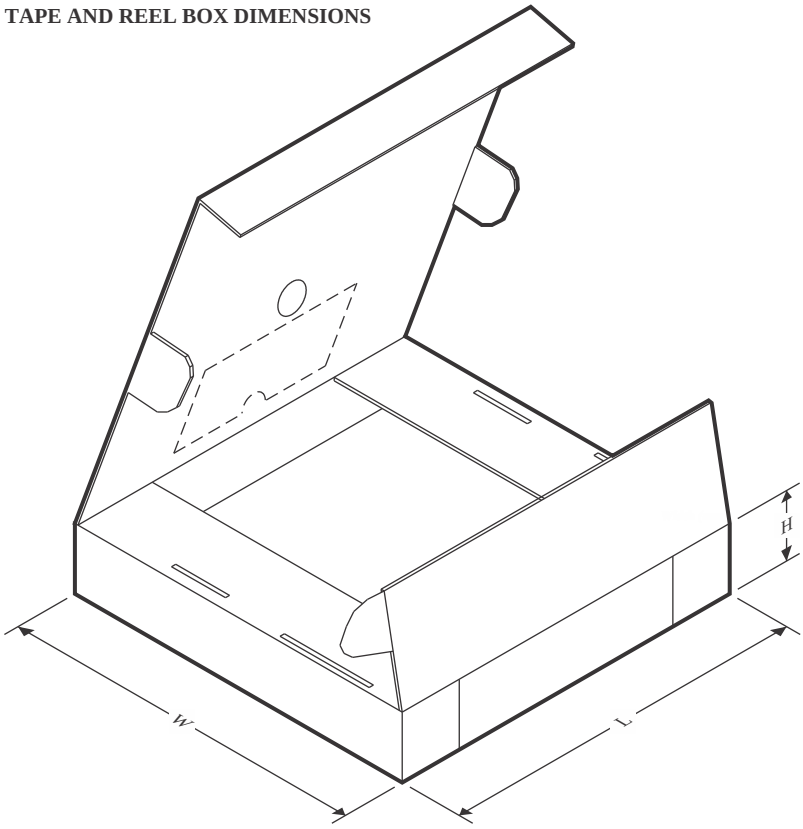
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
RC4558DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
RC4558DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
RC4558DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
RC4558DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
RC4558IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
RC4558IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
RC4558IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
RC4558IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
RC4558IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
RC4558PSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
RC4558PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
RC4558PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

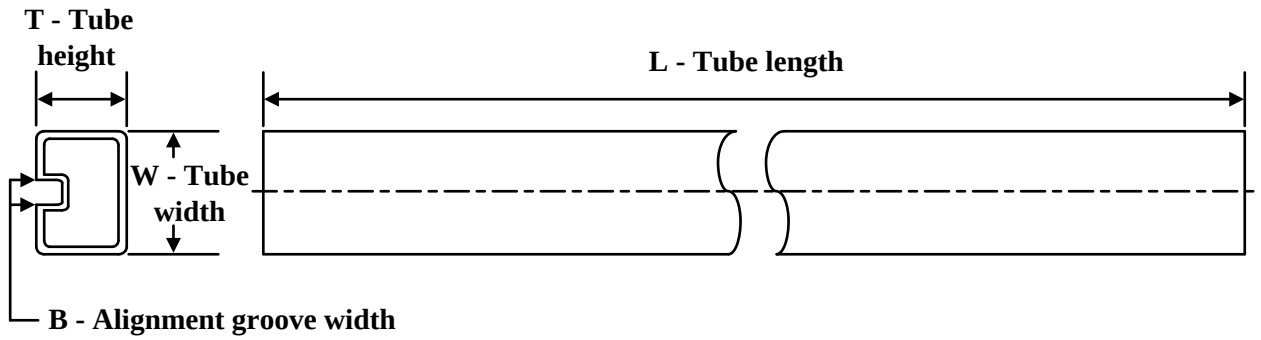
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

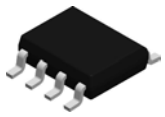
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
RC4558DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
RC4558DGKR	VSSOP	DGK	8	2500	370.0	355.0	55.0
RC4558DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
RC4558DR	SOIC	D	8	2500	353.0	353.0	32.0
RC4558IDGKR	VSSOP	DGK	8	2500	370.0	355.0	55.0
RC4558IDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
RC4558IDR	SOIC	D	8	2500	340.5	338.1	20.6
RC4558IPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
RC4558IPWR	TSSOP	PW	8	2000	353.0	353.0	32.0
RC4558PSR	SO	PS	8	2000	356.0	356.0	35.0
RC4558PWR	TSSOP	PW	8	2000	353.0	353.0	32.0
RC4558PWR	TSSOP	PW	8	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
RC4558IP	P	PDIP	8	50	506	13.97	11230	4.32
RC4558P	P	PDIP	8	50	506	13.97	11230	4.32
RC4558P	P	PDIP	8	50	506	13.97	11230	4.32

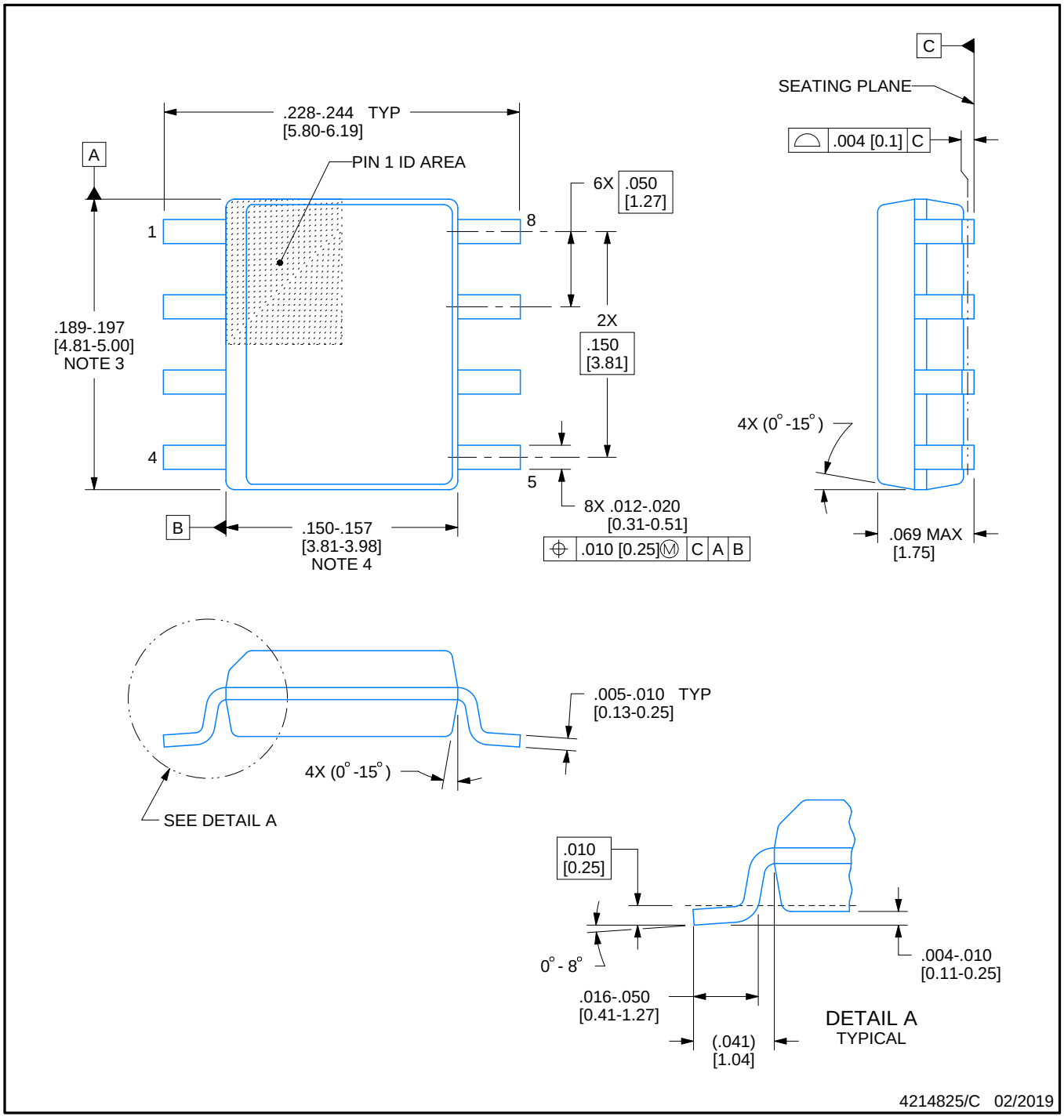


PACKAGE OUTLINE

D0008A

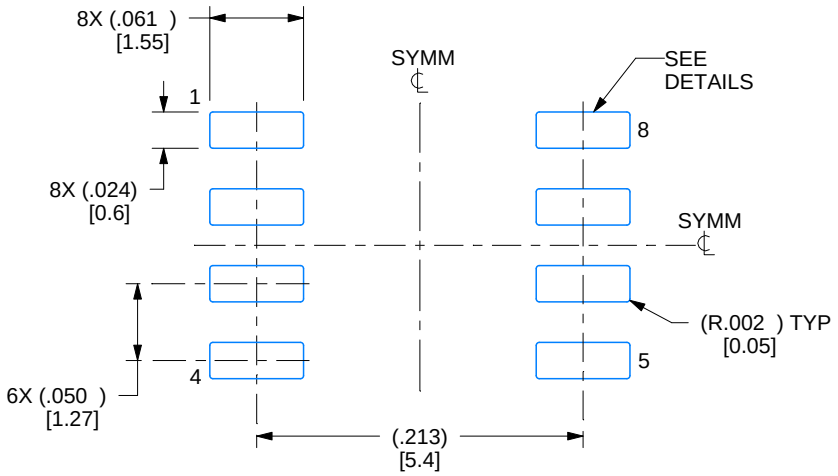
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

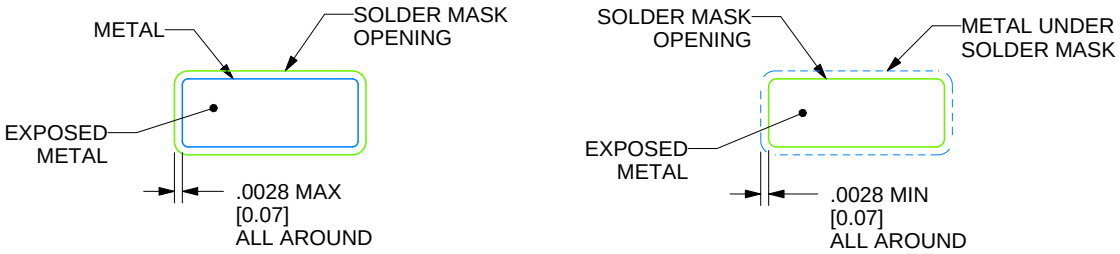


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

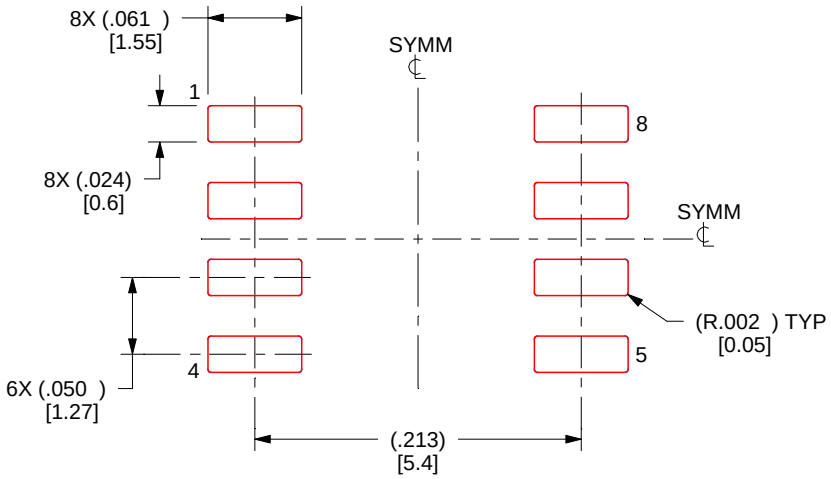
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

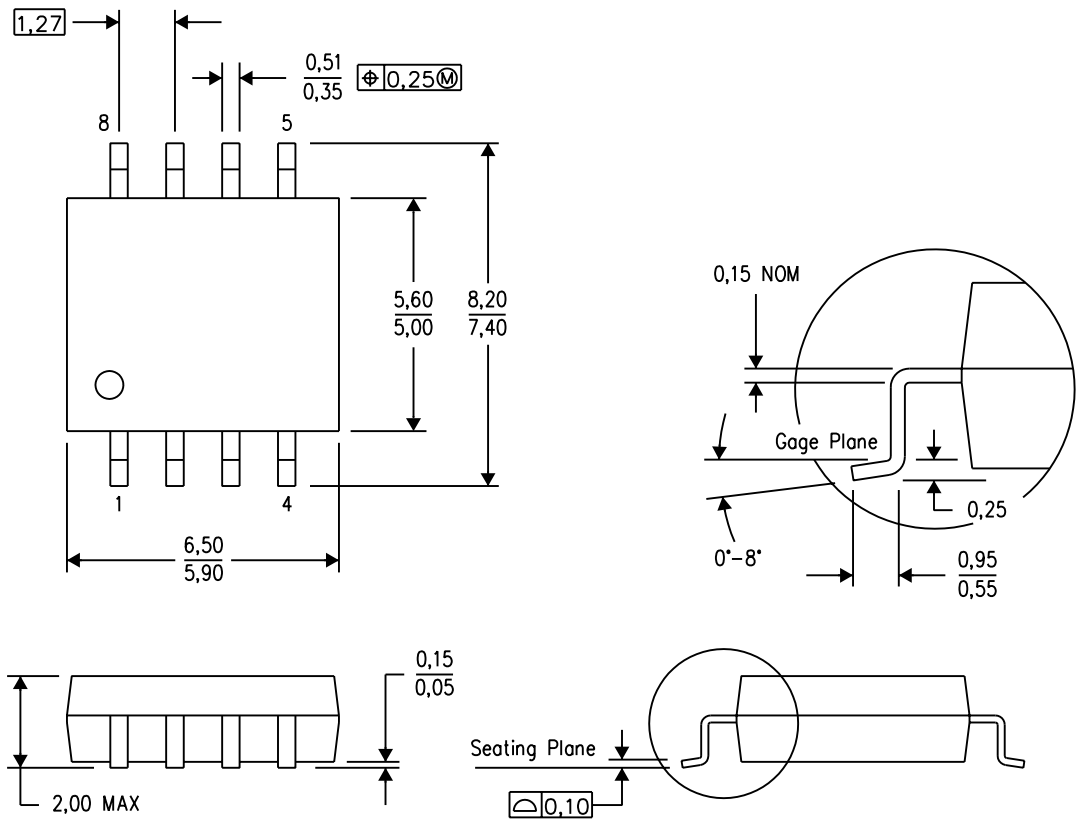
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

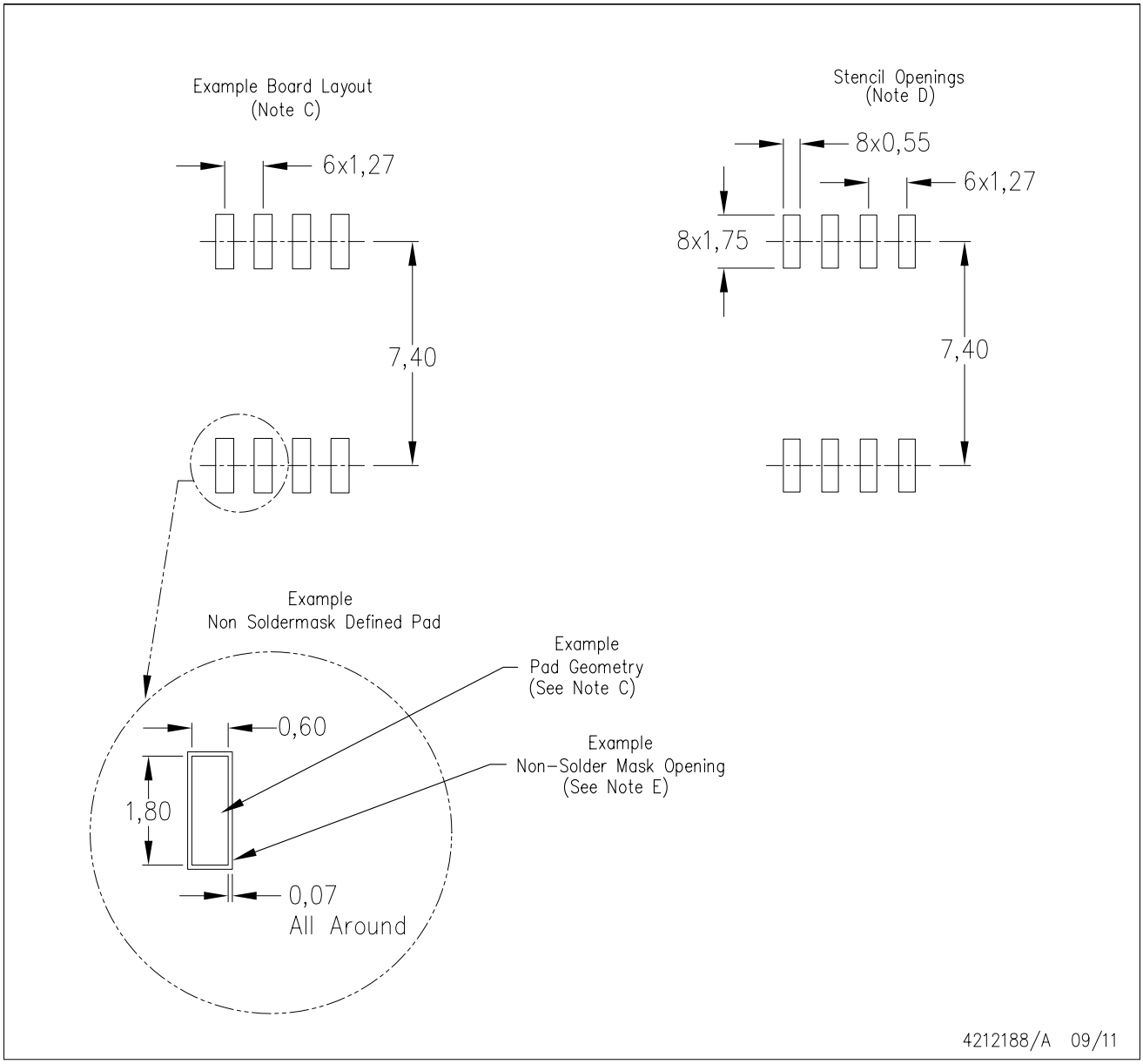
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

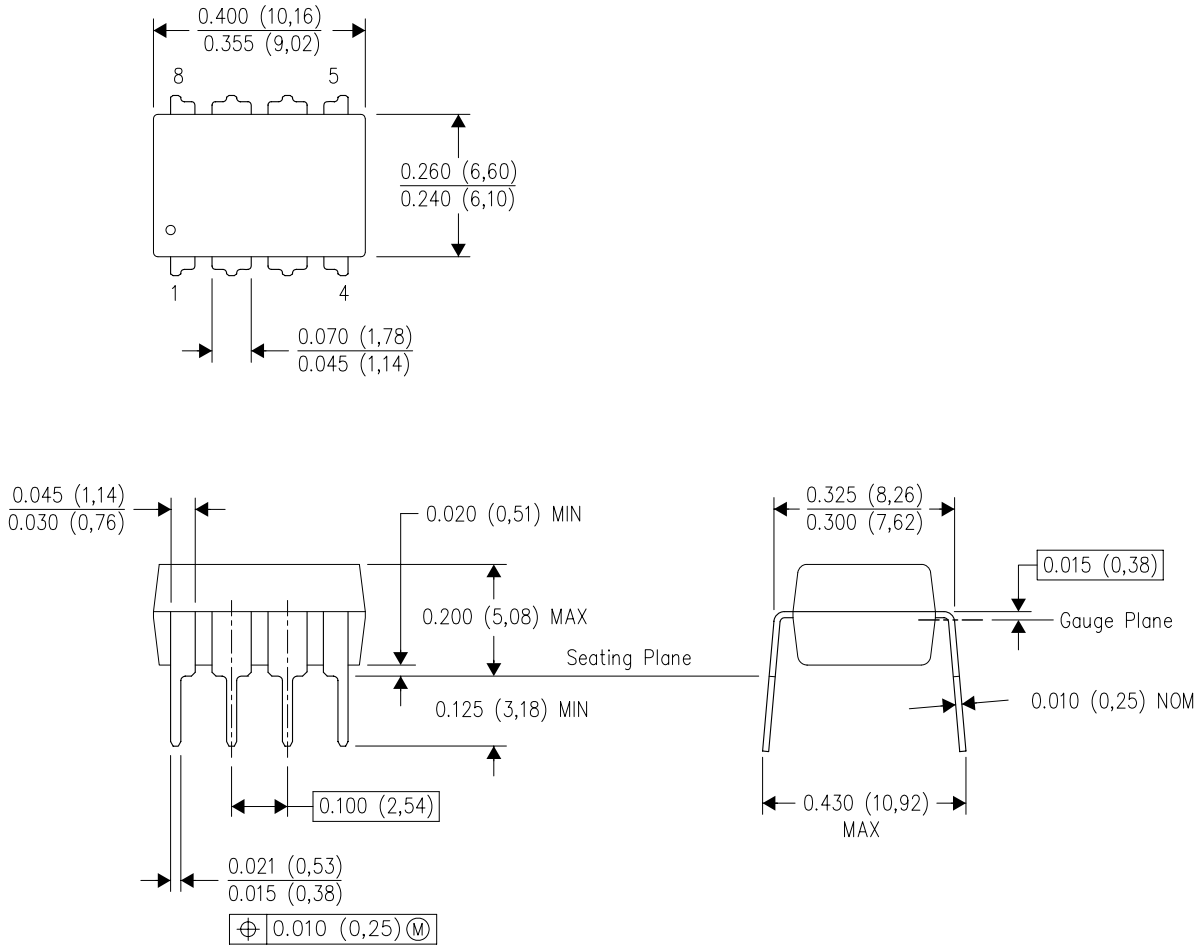
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



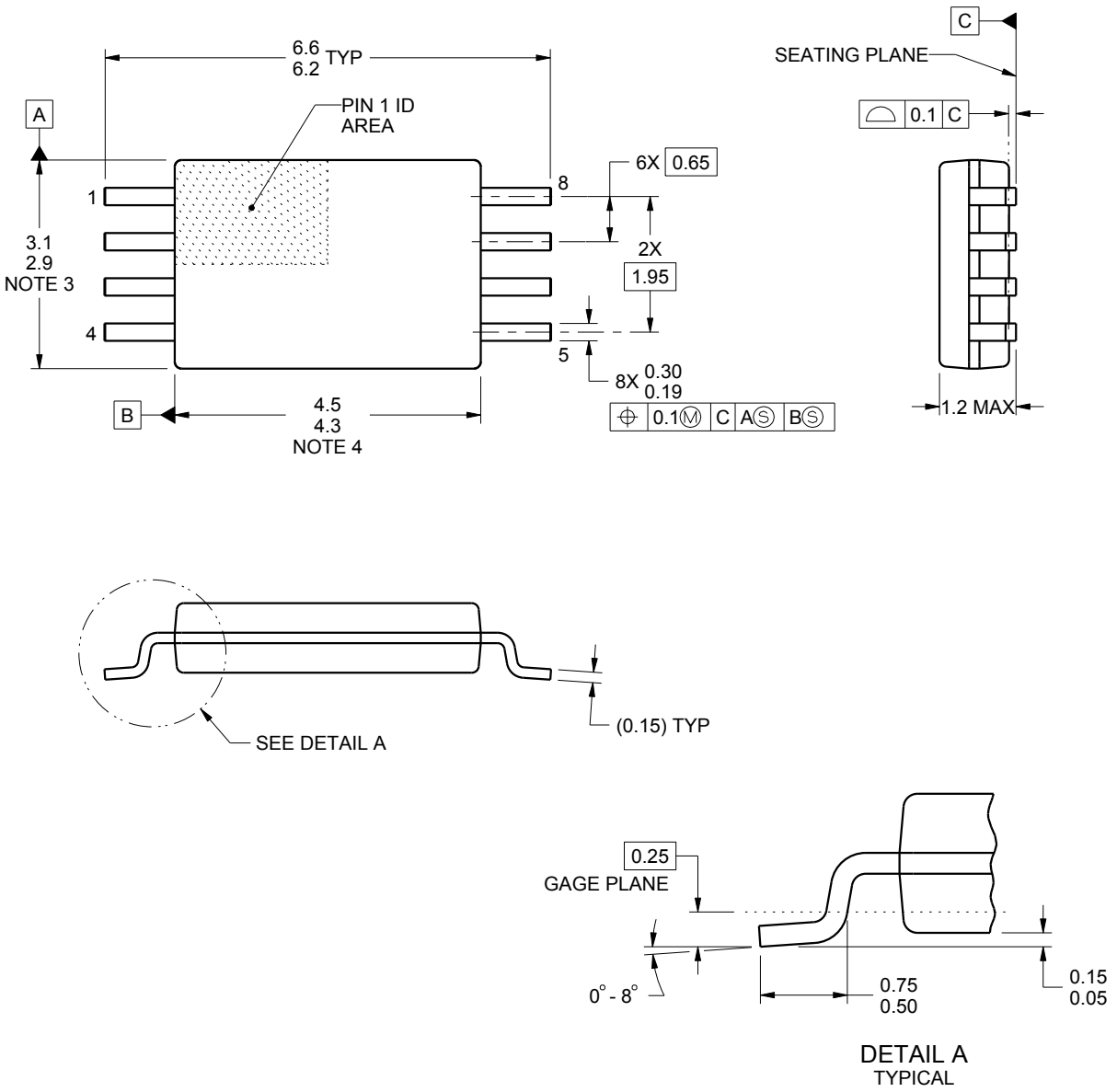
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

PACKAGE OUTLINE

PW0008A

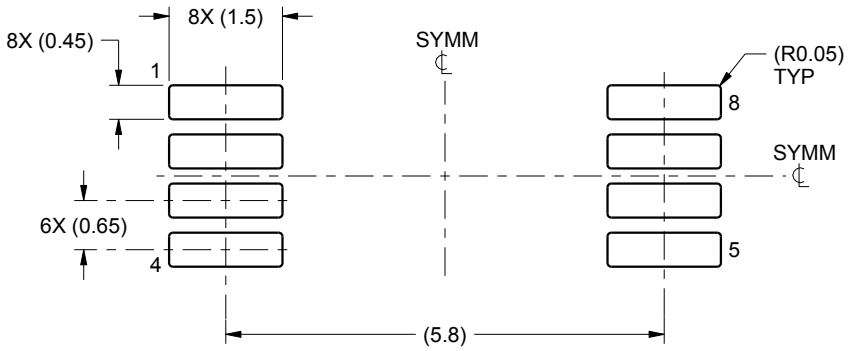
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

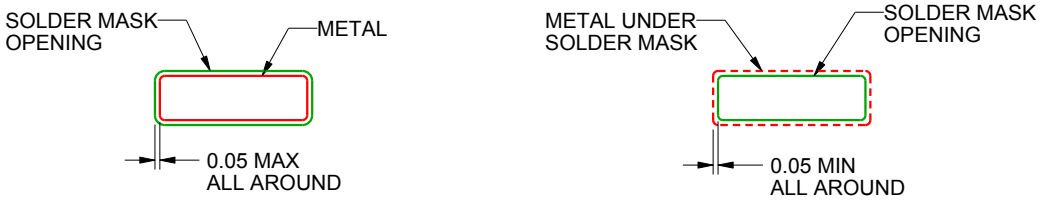


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

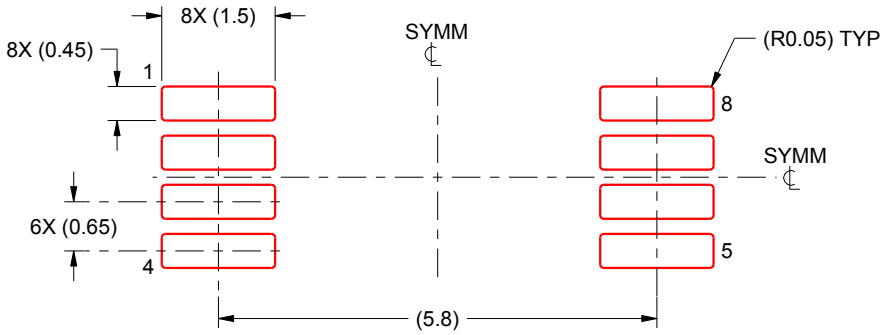


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

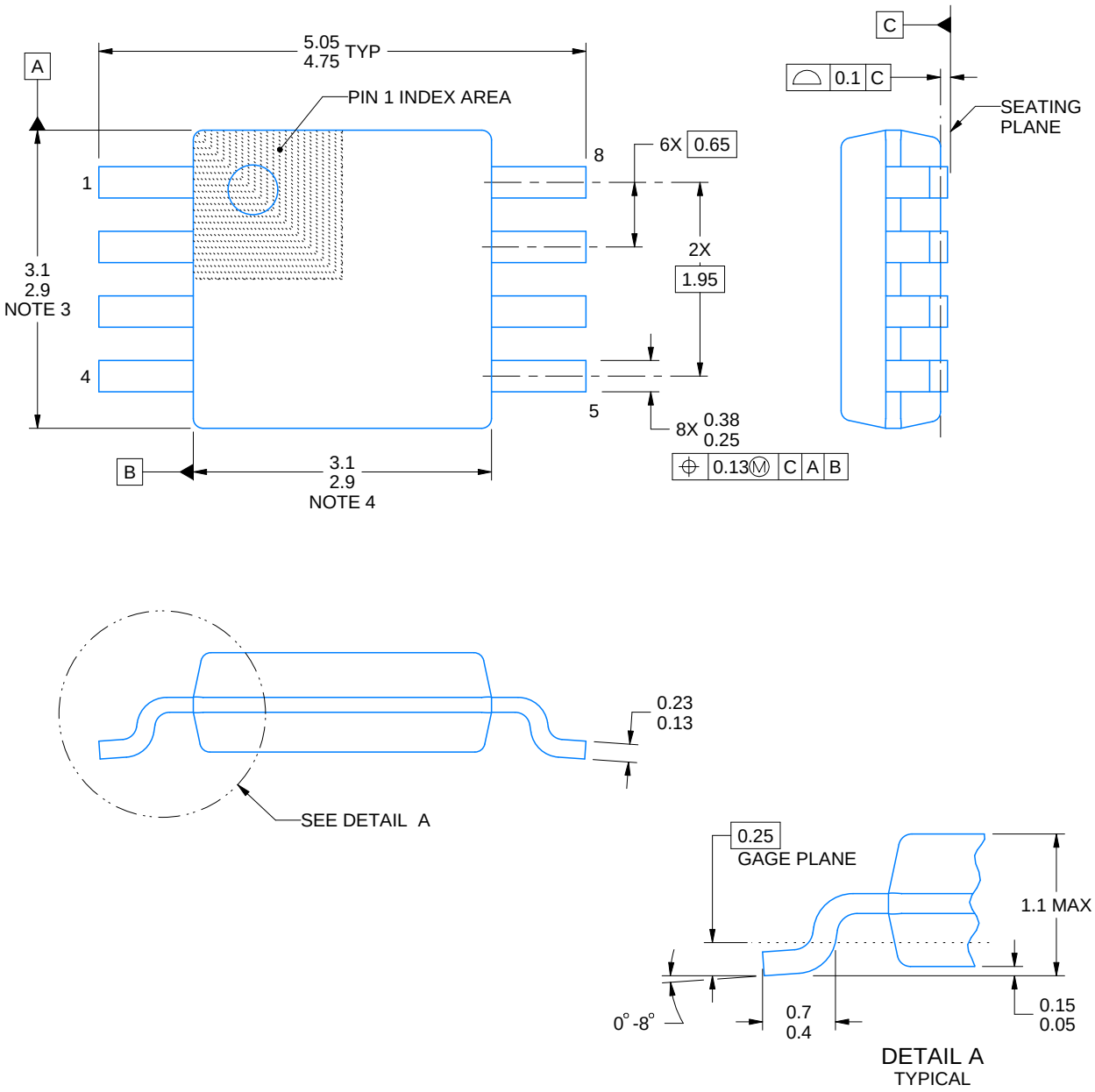
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

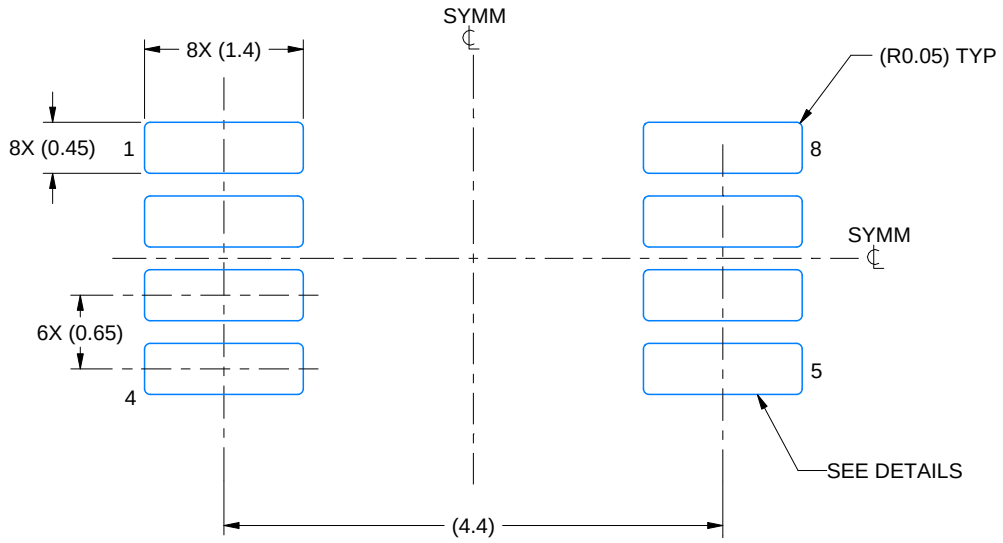
SMALL OUTLINE PACKAGE



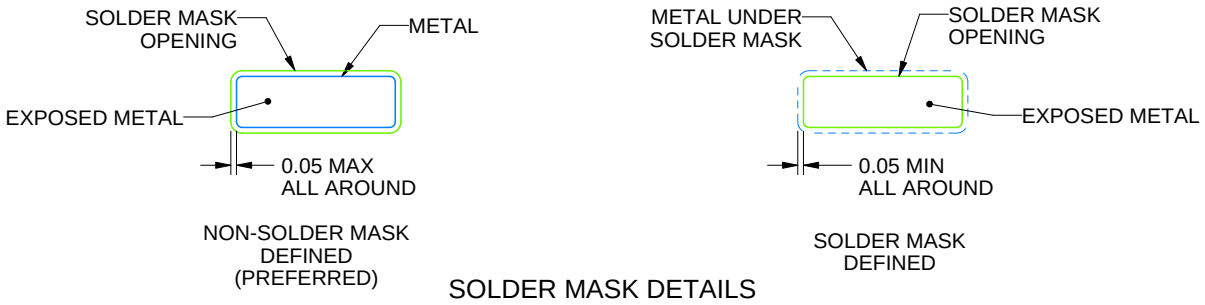
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

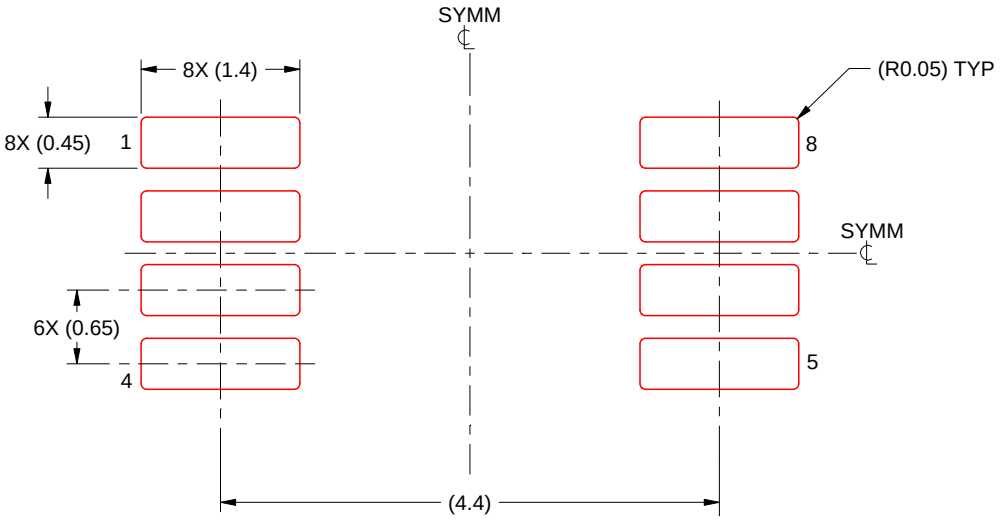


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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