

3V~5.5V、マルチチャネル RS-232 ライン・ドライバおよびレシーバ、 ±15kV ESD 保護

1 特長

- RS-232 バス・ピン用 ESD 保護機能
 - ±15kV 人体モデル (HBM)
 - ±8kV IEC 61000-4-2、接触放電
 - ±15kV IEC 61000-4-2、エアギャップ放電
- TIA/EIA-232-F および ITU v.28 規格の要件に適合またはそれを上回る性能
- 3V~5.5V の V_{CC} 電源で動作
- 最大 1000kbit/s で動作
- 2 つのドライバと 2 つのレシーバ
- 小さいスタンバイ電流 ...1 μ A (標準値)
- 外付けコンデンサ ...4 × 0.1 μ F
- 3.3V 電源で 5V ロジック入力を受容

2 アプリケーション

- 産業用 PC
- 有線ネットワーク
- データ・センターおよびネットワーク機器
- ノート PC
- ハンドヘルド機器

3 概要

SN65C3222E および SN75C3222E は 2 つのライン・ドライバ、2 つのライン・レシーバ、1 つのデュアル・チャージ・ポンプ回路で構成されており、±15kV のピン間 (シリアル・ポート接続ピン、GND を含む) ESD 保護機能を備えています。

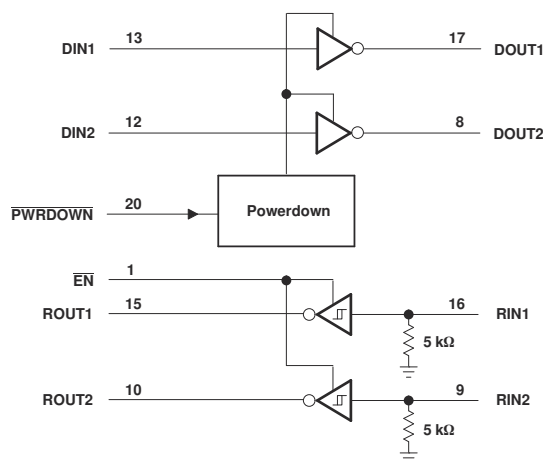
このデバイスは、TIA/EIA-232-F の要件を満たし、非同期通信コントローラとシリアルポート・コネクタの間の電気的インターフェイスとして機能します。チャージ・ポンプと 4 つの小さな外付けコンデンサにより、3V~5.5V の単一電源で動作できます。これらのデバイスは、最大 1000kbps の標準的なデータ信号速度で動作し、業界で広く使用されている 3222 2 ドライバ、2 レシーバの機能に対して改良された完全互換品です。

SN65C3222E および SN75C3222E は、パワーダウン (PWRDOWN) 入力を Low に設定してパワーダウン・モードにすることができます。この状態では電源からわずか 1 μ A しか流れ込みません。デバイスがパワーダウン・モードのとき、ドライバはハイ・インピーダンス状態になりますが、レシーバはアクティブのままです。また、パワーダウン・モード時には、オンボードのチャージ・ポンプがディセーブルになり、 $V+$ が V_{CC} に低下し、 $V-$ が GND に向かって上昇します。レシーバの出力は、イネーブル (\overline{EN}) を HIGH に設定することで、高インピーダンス状態に移行することもできます。

製品情報

| 部品番号 | パッケージ ⁽¹⁾ | 本体サイズ (公称) |
|--------------------------|----------------------|------------------|
| SN65C3222E SN75C3222E | DB (SSOP) (20) | 10.2mm × 5.30mm |
| | DW (SOIC) (20) | 15.4mm × 7.50mm |
| | PW (TSSOP) (20) | 7.80 mm x 4.40mm |

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



ピン番号は、DB、DW、PW パッケージのものです。

論理図 (正論理)



Table of Contents

| | | | |
|--|---|--|-----------|
| 1 特長..... | 1 | 6.11 Switching Characteristics: Receiver..... | 7 |
| 2 アプリケーション..... | 1 | 7 Parameter Measurement Information..... | 8 |
| 3 概要..... | 1 | 8 Detailed Description..... | 10 |
| 4 Revision History..... | 2 | 8.1 Functional Block Diagram..... | 10 |
| 5 Pin Configuration and Functions..... | 3 | 8.2 Device Functional Modes..... | 10 |
| 6 Specifications..... | 4 | 9 Application and Implementation..... | 11 |
| 6.1 Absolute Maximum Ratings..... | 4 | 9.1 Application Information..... | 11 |
| 6.2 ESD Ratings..... | 4 | 9.2 Typical Application..... | 11 |
| 6.3 ESD Ratings - IEC Specifications..... | 4 | 10 Device and Documentation Support..... | 12 |
| 6.4 Recommended Operating Conditions..... | 5 | 10.1 Receiving Notification of Documentation Updates.. | 12 |
| 6.5 Thermal Information: SN65C3222E..... | 5 | 10.2 サポート・リソース..... | 12 |
| 6.6 Thermal Information: SN75C3222E..... | 5 | 10.3 Trademarks..... | 12 |
| 6.7 Electrical Characteristics..... | 5 | 10.4 Electrostatic Discharge Caution..... | 12 |
| 6.8 Electrical Characteristics: Driver..... | 6 | 10.5 Glossary..... | 12 |
| 6.9 Switching Characteristics: Driver..... | 6 | 11 Mechanical, Packaging, and Orderable | |
| 6.10 Electrical Characteristics: Receiver..... | 7 | Information..... | 12 |

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| Changes from Revision A (July 2006) to Revision B (August 2021) | Page |
|--|------|
| • 「アプリケーション」の一覧を更新..... | 1 |
| • 「注文情報」表を削除「製品情報」表から RHL パッケージを削除..... | 1 |
| • 「製品情報」表、「ピン構成および機能」、「詳細説明」セクション、「アプリケーションと実装」セクションを追加..... | 1 |
| • Deleted the Package thermal impedance from the <i>Absolute Maximum Ratings</i> | 4 |
| • Added the <i>ESD Ratings</i> table..... | 4 |
| • Added the <i>Thermal Information: SN65C3222E</i> table..... | 5 |
| • Changed the value of $R_{\theta JA}$ for PW package (previously in the <i>Absolute Maximum Ratings</i> table), and added additional thermal parameters for all packages in the <i>Thermal Information: SN65C3222E</i> table..... | 5 |
| • Added separate <i>Thermal Information</i> table for SN75C3222E..... | 5 |

5 Pin Configuration and Functions

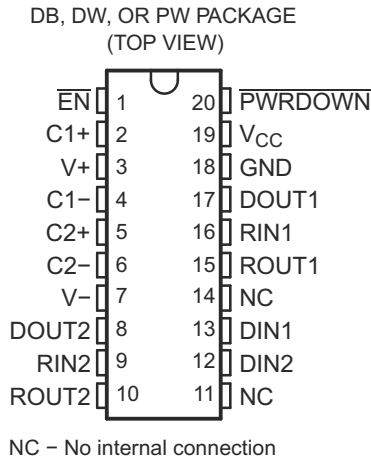


表 5-1. Pin Functions

| PIN | | I/O | DESCRIPTION |
|-----------------|-------|-----|-----------------------------|
| NAME | NO. | | |
| C1+ | 2 | — | Charge pump capacitor pin |
| C1- | 4 | — | Charge pump capacitor pin |
| C2+ | 5 | — | Charge pump capacitor pin |
| C2- | 6 | — | Charge pump capacitor pin |
| DIN1 | 13 | I | Driver logic input |
| DIN2 | 12 | I | Driver logic input |
| DOUT1 | 17 | O | RS-232 driver output |
| DOUT2 | 8 | O | RS-232 driver output |
| EN | 1 | I | Receiver enable, active low |
| GND | 18 | — | Ground |
| NC | 11,14 | — | No internal connection |
| PWRDOWN | 20 | I | Driver disable, active low |
| RIN1 | 16 | I | RS-232 receiver input |
| RIN2 | 9 | I | RS-232 receiver input |
| ROUT1 | 15 | O | Receiver logic output |
| ROUT2 | 10 | O | Receiver logic output |
| V _{CC} | 19 | — | Power Supply |
| V+ | 3 | — | Charge pump capacitor pin |
| V- | 7 | — | Charge pump capacitor pin |

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

| | | MIN | MAX | UNIT | |
|------------------|---|-----------------------|-------|-----------------------|---|
| V _{CC} | Supply voltage range ⁽²⁾ | -0.3 | 6 | V | |
| V+ | Positive-output supply voltage range ⁽²⁾ | -0.3 | 7 | V | |
| V- | Negative-output supply voltage range ⁽²⁾ | 0.3 | -7 | V | |
| V+ – V- | Supply voltage difference ⁽²⁾ | | 13 | V | |
| V _I | Input voltage range | Driver (EN, PWRDOWN) | -0.3 | 6 | V |
| | | Receiver | -25 | 25 | |
| V _O | Output voltage range | Driver | -13.2 | 13.2 | V |
| | | Receiver | -0.3 | V _{CC} + 0.3 | |
| T _J | Operating virtual junction temperature | | 150 | °C | |
| T _{stg} | Storage temperature range | -65 | 150 | °C | |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network GND.

6.2 ESD Ratings

| | | | VALUE | UNIT |
|--------------------|-------------------------|---|---------|------|
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±3,000 | V |
| | | | ±15,000 | |
| | | Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾ | ±1,500 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings - IEC Specifications

| | | | VALUE | UNIT |
|--------------------|-------------------------|---|---------|------|
| V _(ESD) | Electrostatic discharge | IEC 61000-4-2, Contact Discharge ⁽¹⁾ | ±8,000 | V |
| | | IEC 61000-4-2, Air Discharge ⁽¹⁾ | ±15,000 | |

- (1) For the PW Package of SN65C3222E only, a minimum of 1-μF capacitor is required between V_{CC} and GND to meet the specified IEC 61000-4-2 rating

6.4 Recommended Operating Conditions

See [9-1](#) and ⁽¹⁾

| | | MIN | NOM | MAX | UNIT |
|--|-------------------------|-------------------------|-----|-----|------|
| Supply voltage | $V_{CC} = 3.3\text{ V}$ | 3 | 3.3 | 3.6 | V |
| | $V_{CC} = 5\text{ V}$ | 4.5 | 5 | 5.5 | |
| V_{IH} Driver and control high-level input voltage | DIN, EN, PWRDOWN | $V_{CC} = 3.3\text{ V}$ | 2 | | V |
| | | $V_{CC} = 5\text{ V}$ | 2.4 | | |
| V_{IL} Driver and control low-level input voltage | DIN, EN, PWRDOWN | | | 0.8 | V |
| V_I Driver and control input voltage | DIN, EN, PWRDOWN | 0 | 5.5 | | V |
| V_I Receiver input voltage | | -25 | 25 | | V |
| T_A Operating free-air temperature | SN75C3222E | 0 | 70 | | °C |
| | SN65C3222E | -40 | 85 | | |

(1) Test conditions are C1–C4 = 0.1 μF at $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$; C1 = 0.047 μF , C2–C4 = 0.33 μF at $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$.

6.5 Thermal Information: SN65C3222E

| THERMAL METRIC ⁽¹⁾ | | SN65C3222E | | | UNIT |
|-------------------------------|--|------------|-----------|------------|------|
| | | DB (SSOP) | DW (SOIC) | PW (TSSOP) | |
| | | 20 Pins | 20 Pins | 20 Pins | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 70 | 58 | 94.1 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (bottom) thermal resistance | 33.6 | 30.0 | 35.2 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 36.4 | 29.6 | 45.5 | °C/W |
| Ψ_{JT} | Junction-to-top characterization parameter | 4.8 | 7.7 | 3.1 | °C/W |
| Ψ_{JB} | Junction-to-board characterization parameter | 35.9 | 29.3 | 45.1 | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

6.6 Thermal Information: SN75C3222E

| THERMAL METRIC ¹ | | SN75C3222E | | | UNIT |
|-----------------------------|--|------------|-----------|------------|------|
| | | DB (SSOP) | DW (SOIC) | PW (TSSOP) | |
| | | 20 | 20 | 20 | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 70 | 58 | 83 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 33.6 | 30.0 | 24.8 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 36.4 | 29.6 | 39.5 | °C/W |
| Ψ_{JT} | Junction-to-top characterization parameter | 4.8 | 7.7 | 1.1 | °C/W |
| Ψ_{JB} | Junction-to-board characterization parameter | 35.9 | 29.3 | 39.0 | °C/W |

6.7 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [9-1](#))

| PARAMETER | | TEST CONDITIONS ⁽²⁾ | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|-----------|--------------------------------------|--------------------------------|-----|--------------------|---------|---------------|
| I_I | Input leakage current (EN, PWRDOWN) | | | ± 0.01 | ± 1 | μA |
| I_{CC} | Supply current | No load, PWRDOWN at V_{CC} | | 0.3 | 1 | mA |
| | Supply current (powered off) | No load, PWRDOWN at GND | | 1 | 10 | μA |

(1) All typical values are at $V_{CC} = 3.3\text{ V}$ or $V_{CC} = 5\text{ V}$, and $T_A = 25^\circ\text{C}$.

(2) Test conditions are C1–C4 = 0.1 μF at $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$; C1 = 0.047 μF , C2–C4 = 0.33 μF at $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$.

6.8 Electrical Characteristics: Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [9-1](#))

| PARAMETER | | TEST CONDITIONS | | MIN | TYP ⁽¹⁾ (3) | MAX | UNIT |
|-----------------|---|--|---|-----|---------------------------|-----|------|
| V _{OH} | High-level output voltage | DOOUT at R _L = 3 kΩ to GND, DIN = GND | | 5 | 5.4 | | V |
| V _{OL} | Low-level output voltage | DOOUT at R _L = 3 kΩ to GND, DIN = V _{CC} | | -5 | -5.4 | | V |
| I _{IH} | High-level input current | V _I = V _{CC} | | | ±0.01 | ±1 | μA |
| I _{IL} | Low-level input current | V _I at GND | | | ±0.01 | ±1 | μA |
| I _{OS} | Short-circuit output current ⁽²⁾ | V _{CC} = 3.6 V | V _O = 0 V | | ±35 | ±60 | mA |
| | | V _{CC} = 5.5 V | | | | | |
| r _o | Output resistance | V _{CC} , V+, and V- = 0 V, V _O = ±2 V | | 300 | 10M | | Ω |
| I _{OZ} | Output leakage current | PWRDOWN = GND | V _{CC} = 3 V to 3.6 V, V _O = ±12 V | | | ±25 | μA |
| | | | V _{CC} = 4.5 V to 5.5 V, V _O = ±10 V | | | ±25 | |

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(2) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

(3) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

6.9 Switching Characteristics: Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [9-1](#))

| PARAMETER | TEST CONDITIONS ⁽³⁾ | | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|---|--|--|-----------------------------------|--------------------|-----|--------|
| Maximum data rate (See 7-1) | R _L = 3 kΩ, One DOOUT switching | C _L = 1000 pF | | 250 | | kbit/s |
| | | C _L = 250 pF, V _{CC} = 3 V to 4.5 V | | 1000 | | |
| | | C _L = 1000 pF, V _{CC} = 4.5 V to 5.5 V | | 1000 | | |
| t _{sk(p)} | C _L = 150 pF to 2500 pF, R _L = 3 kΩ to 7 kΩ, | See 7-2 | | 300 | | ns |
| SR(tr) Slew rate, transition region (see 7-1) | R _L = 7 kΩ, | C _L = 150 pF to 1000 pF | | 8 | 90 | V/μs |
| | | R _L = 3 kΩ | C _L = 1000 pF | | 12 | |
| | | | C _L = 150 pF to 250 pF | | 24 | |

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(2) Pulse skew is defined as |t_{PLH} - t_{PHL}| of each channel of the same device.

(3) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

6.10 Electrical Characteristics: Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [9-1](#))

| PARAMETER | | TEST CONDITIONS ⁽²⁾ | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|------------------|---|--------------------------------|-----------------------|-----------------------|-----|------|
| V _{OH} | High-level output voltage | I _{OH} = –1 mA | V _{CC} – 0.6 | V _{CC} – 0.1 | | V |
| V _{OL} | Low-level output voltage | I _{OL} = 1.6 mA | | | 0.4 | V |
| V _{IT+} | Positive-going input threshold voltage | V _{CC} = 3.3 V | | 1.5 | 2.4 | V |
| | | V _{CC} = 5 V | | 1.8 | 2.4 | |
| V _{IT–} | Negative-going input threshold voltage | V _{CC} = 3.3 V | 0.6 | 1.2 | | V |
| | | V _{CC} = 5 V | 0.8 | 1.5 | | |
| V _{hys} | Input hysteresis (V _{IT+} – V _{IT–}) | | | 0.3 | | V |
| I _{OZ} | Output leakage current | EN = 1 | | ±0.05 | ±10 | μA |
| r _i | Input resistance | V _I = ±3 V to ±25 V | 3 | 5 | 7 | kΩ |

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(2) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

6.11 Switching Characteristics: Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

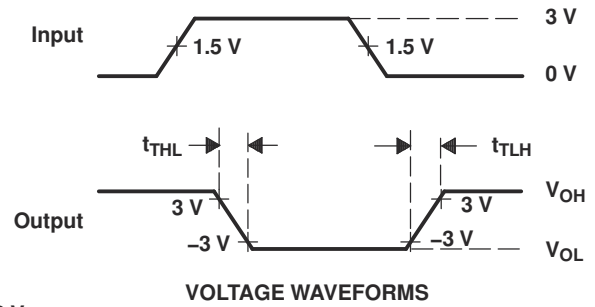
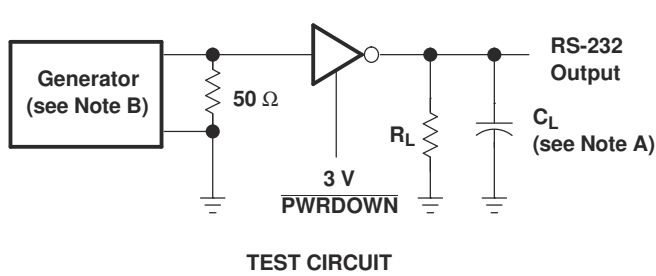
| PARAMETER | | TEST CONDITIONS ⁽³⁾ | TYP ⁽¹⁾ | UNIT |
|--------------------|---|---|--------------------|------|
| t _{PLH} | Propagation delay time, low- to high-level output | C _L = 150 pF, See 7-3 | 300 | ns |
| t _{PHL} | Propagation delay time, high- to low-level output | C _L = 150 pF, See 7-3 | 300 | ns |
| t _{en} | Output enable time | C _L = 150 pF, R _L = 3 kΩ, See 7-4 | 200 | ns |
| t _{dis} | Output disable time | C _L = 150 pF, R _L = 3 kΩ, See 7-4 | 200 | ns |
| t _{sk(p)} | Pulse skew ⁽²⁾ | See 7-3 | 300 | ns |

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(2) Pulse skew is defined as |t_{PLH} – t_{PHL}| of each channel of the same device.

(3) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

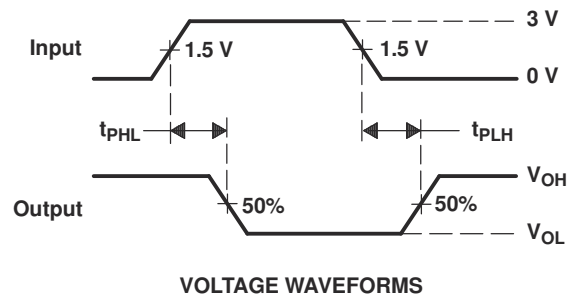
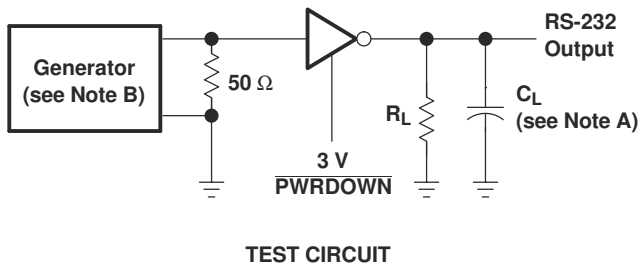
7 Parameter Measurement Information



$$SR(tr) = \frac{6\text{ V}}{t_{THL} \text{ or } t_{TLH}}$$

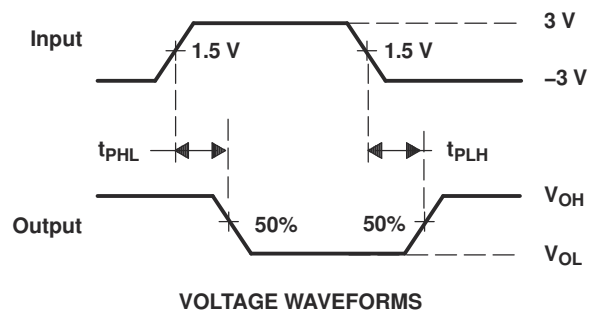
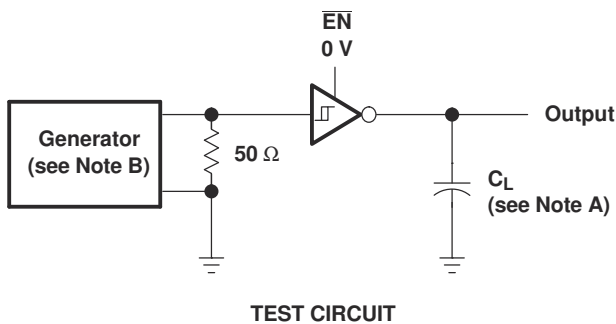
- A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

7-1. Driver Slew Rate



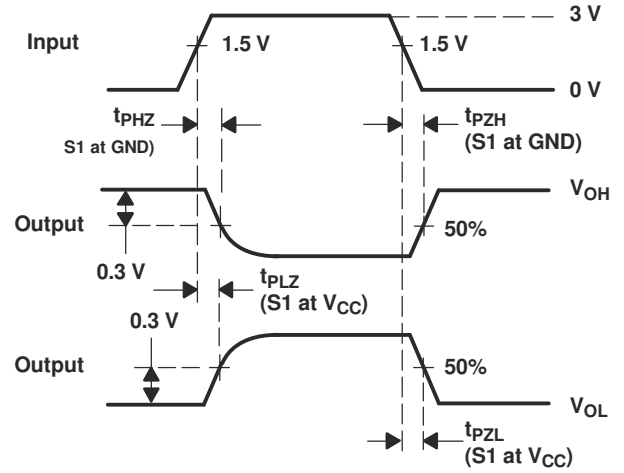
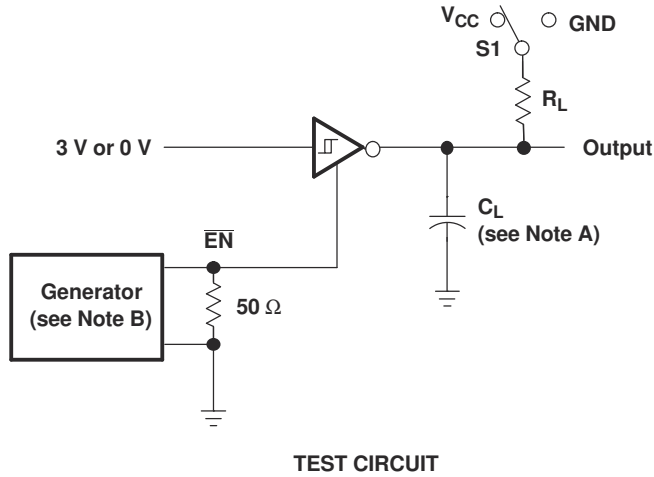
- A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

7-2. Driver Pulse Skew



- A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

7-3. Receiver Propagation Delay Times

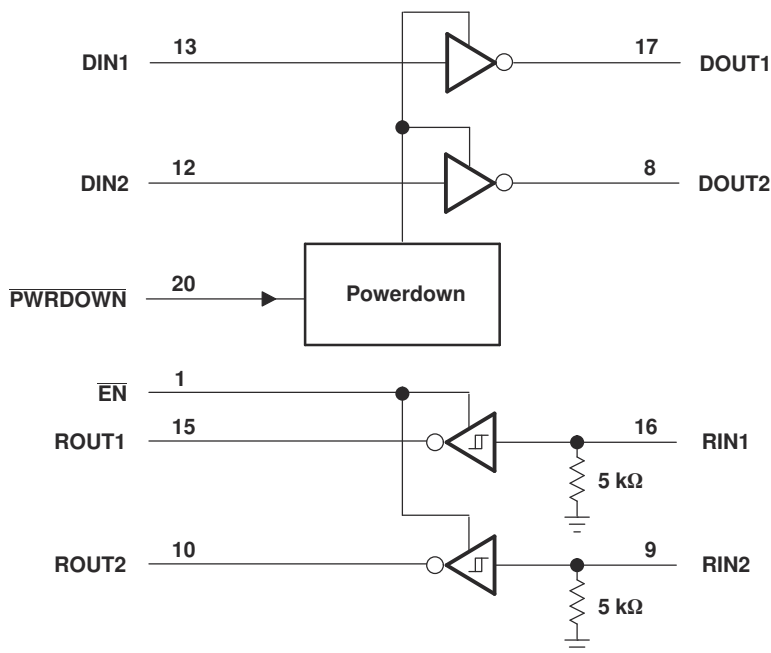


- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

7-4. Receiver Enable and Disable Times

8 Detailed Description

8.1 Functional Block Diagram



Pin numbers are for the DB, DW, and PW packages.

图 8-1. Logic Diagram (Positive Logic)

8.2 Device Functional Modes

表 8-1. Function Tables: Each Driver

| INPUTS ⁽¹⁾ | | OUTPUT DOUT |
|-----------------------|---------|----------------|
| DIN | PWRDOWN | |
| X | L | Z |
| L | H | H |
| H | H | L |

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

表 8-2. Function Table: Each Receiver

| INPUTS ⁽¹⁾ | | OUTPUT ROUT |
|-----------------------|----|----------------|
| RIN | EN | |
| L | L | H |
| H | L | L |
| X | H | Z |
| Open | L | H |

(1) H = high level, L = low level, X = irrelevant,
Z = high impedance (off),
Open = input disconnected or connected driver off

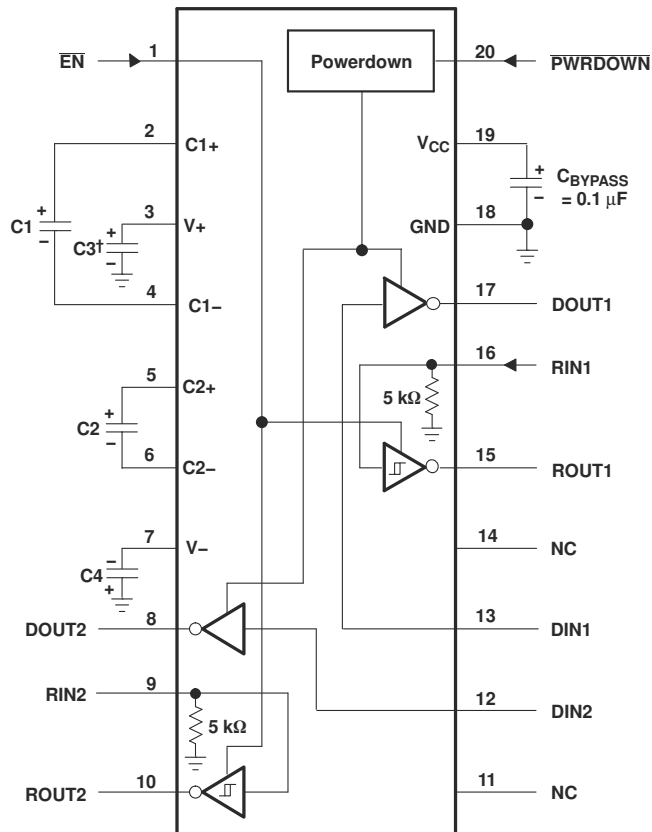
9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

9.2 Typical Application



† C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.

B. NC – No internal connection

C. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V_{CC} vs CAPACITOR VALUES

| V _{CC} | C1 | C2, C3, and C4 |
|-----------------|----------|----------------|
| 3.3 V ± 0.3 V | 0.1 μF | 0.1 μF |
| 5 V ± 0.5 V | 0.047 μF | 0.33 μF |
| 3 V to 5.5 V | 0.1 μF | 0.47 μF |

9-1. Typical Operating Circuit and Capacitor Values

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の [使用条件](#) を参照してください。

10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN65C3222EDB | ACTIVE | SSOP | DB | 20 | 70 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | MU222E | Samples |
| SN65C3222EDBR | ACTIVE | SSOP | DB | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | MU222E | Samples |
| SN65C3222EDW | ACTIVE | SOIC | DW | 20 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 65C3222E | Samples |
| SN65C3222EDWR | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 65C3222E | Samples |
| SN65C3222EPWR | NRND | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | MU222E | |
| SN75C3222EPW | OBSOLETE | TSSOP | PW | 20 | | TBD | Call TI | Call TI | 0 to 70 | MY222E | |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN65C3222EDBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN65C3222EDWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN65C3222EPWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |
| SN65C3222EPWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN65C3222EDBR | SSOP | DB | 20 | 2000 | 356.0 | 356.0 | 35.0 |
| SN65C3222EDWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN65C3222EPWR | TSSOP | PW | 20 | 2000 | 356.0 | 356.0 | 35.0 |
| SN65C3222EPWR | TSSOP | PW | 20 | 2000 | 356.0 | 356.0 | 35.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|--------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN65C3222EDB | DB | SSOP | 20 | 70 | 530 | 10.5 | 4000 | 4.1 |
| SN65C3222EDW | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |

DB0020A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

4220724/A 05/2016

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW0020A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス・デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、または [ti.com](#) やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所 : Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated