TEXAS INSTRUMENTS
SN54HC257, SN54HC258, SN74HC257, SN74HC258
JAJSOD3C – DECEMBER 1982 – REVISED MARCH 2022

SNx4HC257、SNx4HC258 3 ステート出力、クワッド、2 ライン入力 1 ライン出力、データ・セレクタ / マルチプレクサ

1 特長

- 幅広い動作電圧範囲:2V～6V
- 大電流反転出力は最大 15 個の LSTTL 負荷を駆動可能
- 低消費電力、最大 I_{CC} 80μA
- HC257:t_{pd} = 9ns (標準値)
- HC258:t_{pd} = 12ns (標準値)
- 5V で ±6mA の出力駆動能力
- 低い入力電流:最大 1μA
- 高性能システムの複数のソースからバス・インターフェイスを提供

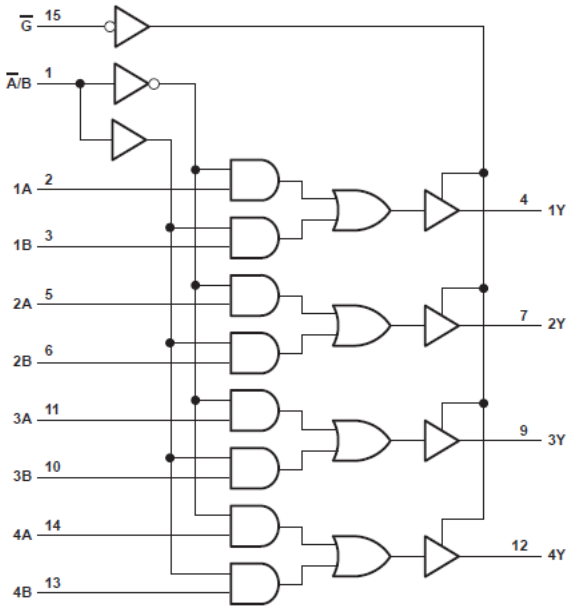
2 概要

SNx4HC257 および 258 は、2 つのデータ源の 1 つを選択するための 4 つのデータ・セレクタ / マルチプレクサを内蔵しています。すべてのチャネルは、同じアドレス選択 ($\overline{A}$/B) 入力とアクティブ LOW のストローブ ($\overline{G}$) 入力により制御されます。$\overline{G}$ ピンが HIGH レベルになると、すべての出力が強制的に高インピーダンス状態になります。257 は非反転出力であり、258 は反転出力です。

デバイス情報

部品番号	パッケージ (1)	本体サイズ (公称)
SN74HC257D	SOIC (16)	9.90mm × 3.90mm
SN74HC257N	PDIP (16)	19.31mm × 6.35mm
SN74HC257NS	SO (16)	6.20mm × 5.30mm
SN74HC257PW	TSSOP (16)	5.00mm × 4.40mm
SN74HC258D	SOIC (16)	9.90mm × 3.90mm
SN74HC258N	PDIP (16)	19.31mm × 6.35mm
SN74HC258NS	SO (16)	6.20mm × 5.30mm
SN74HC258PW	TSSOP (16)	5.00mm × 4.40mm
SN54HC257J	CDIP (16)	24.38mm × 6.92mm
SNJ54HC257FK	LCCC (20)	8.89mm × 8.45mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



ここに示すピン番号は D、J、N、NS、PW の各パッケージのものです。

SN74HC257 の機能ブロック図

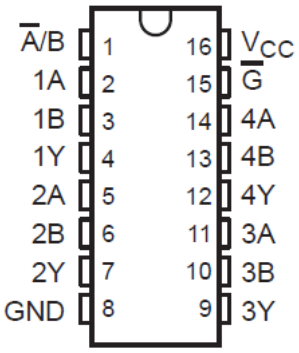
Table of Contents

3 Revision History

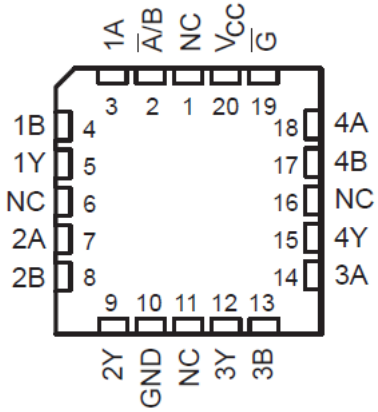
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (September 2003) to Revision C (March 2022)	Page
• 最新のデータシート規格を反映するように、文書全体にわたって表、図、相互参照の採番方法を更新	1

4 Pin Configuration and Functions



J, D, N, NS, or PW package
16-Pin CDIP, SOIC, PDIP, SO, TSSOP
Top View



NC − No internal connection

FK package
20-Pin LCCC
Top View

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	7	V
I_{IK}	Input clamp current(2)	(V_I < 0 or V_I > V_{CC})		±20	mA
I_{OK}	Output clamp current(2)	(V_O < 0 or V_O > V_{CC})		±20	mA
I_O	Continuous output current	(V_O = 0 to V_{CC})		±35	mA
	Continuous current through V_{CC} or GND			±70	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 Recommended Operating Conditions(1)

			SN54HC257, SN54HC258			SN74HC257, SN74HC258			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V			0.3			0.5	V
		V_{CC} = 4.5 V			0.9			1.35	
		V_{CC} = 6 V			1.2			1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition rise/fall time	V_{CC} = 2 V			1000			1000	ns
		V_{CC} = 4.5 V			500			500	
		V_{CC} = 6 V			400			400	
T_A	Operating free-air temperature		-55		125	-40		85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report Implications of Slow or Floating SMOS Inputs, literature number SCBA004.

5.3 Thermal Information

THERMAL METRIC		D (SOIC) 16 PINS	N (PDIP) 16 PINS	NS (SO) 16 PINS	PW (TSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)	73	67	64	108	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS[1]	V_{CC}	T_A = 25°C			SN54HC257, SN54HC258		SN74HC257, SN74HC258		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −20 µA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	I_{OH} = −6 mA	4.5 V	3.98	4.3		3.7		3.84		
	I_{OH} = −7.8 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	I_{OL} = 20 µA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
	I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0	6 V		±0.01	±0.5		±10		±5	µA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	µA
C_i		2 V to 6 V		3	10		10		10	pF

(1) V_I = V_{IH} or V_{IL}, unless otherwise noted.

5.5 Switching Characteristics

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (See Figure 6)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CC} (V)	T_A = 25°C			SN54HC257		SN74HC257		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A or B	Any Y	2		50	100		150		125	ns
				4.5		10	20		30		25	
				6		9	17		25		21	
		$\overline{A}$/B	Any Y	2		50	100		150		125	
				4.5		10	20		30		25	
				6		9	17		25		21	
t_{en}	Enable time	$\overline{G}$	Any Y	2		75	150		225		190	ns
				4.5		15	30		45		38	
				6		13	26		38		32	
t_{dis}	Diable time	$\overline{G}$	Any Y	2		75	150		225		190	ns
				4.5		15	30		45		38	
				6		13	26		38		32	
t_t	Transition time		Any Y	2		28	60		90		75	ns
				4.5		8	12		18		15	
				6		6	10		15		13	

5.5 Switching Characteristics

over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (See Figure 6)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CC} (V)	T_A = 25°C			SN54HCT257		SN74HC257		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A or B	Any Y	2		75	150		245		190	ns
				4.5		15	30		45		38	
				6		13	26		38		32	
		$\overline{A}$/B	Any Y	2		75	150		245		190	
				4.5		15	30		45		38	
				6		13	26		38		32	
t_{en}	Enable time	$\overline{G}$	Any Y	2		100	200		300		250	ns
				4.5		24	40		60		50	
				6		18	34		51		43	
t_t	Transition time		Any Y	2		45	210		315		265	ns
				4.5		17	42		63		53	
				6		13	36		53		45	

5.5 Switching Characteristics

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (See Figure 6)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CC} (V)	T_A = 25°C			SN54HC258		SN74HC258		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A or B	Any Y	2		60	100		150		125	ns
				4.5		13	20		30		25	
				6		12	17		25		21	
		$\overline{A}$/B	Any Y	2		60	115		175		145	
				4.5		13	23		35		29	
				6		12	20		30		25	
t_{en}	Enable time	$\overline{G}$	Any Y	2		70	150		225		190	ns
				4.5		15	30		45		38	
				6		13	26		38		32	
t_{dis}	Diable time	$\overline{G}$	Any Y	2		75	150		225		190	ns
				4.5		15	30		45		38	
				6		13	26		38		32	
t_t	Transition time		Any Y	2		28	60		90		75	ns
				4.5		8	12		18		15	
				6		6	10		15		13	

5.5 Switching Characteristics

over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (See Figure 6)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CC} (V)	T_A = 25°C			SN54HC258		SN74HC258		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A or B	Any Y	2		95	150		245		190	ns
				4.5		23	30		45		38	
				6		21	26		38		32	
		$\overline{A}$/B	Any Y	2		95	165		240		210	
				4.5		23	33		48		42	
				6		21	28		41		36	
t_{en}	Enable time	$\overline{G}$	Any Y	2		100	200		300		250	ns
				4.5		24	40		60		50	
				6		18	34		51		43	
t_t	Transition time		Any Y	2		45	210		315		265	ns
				4.5		17	42		63		53	
				6		13	36		53		45	

5.6 Operating Characteristics

T_A = 25°C

		Test Conditions	TYP	UNIT
C_{pd}	Power dissipation capacitance per multiplexer	No load	40	pF

6 Parameter Measurement Information

t_{pd} is the maximum between t_{PLH} and t_{PHL}

t_t is the maximum between t_{TLH} and t_{THL}

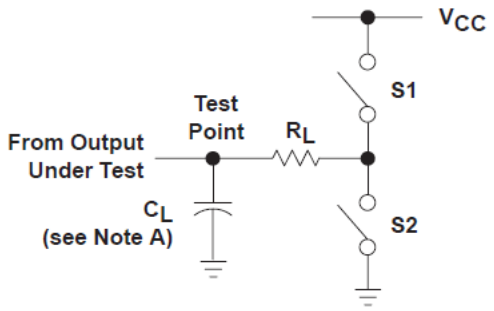


図 6-1. Load Circuit

PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		--	50 pF or 150 pF	Open	Open

図 6-2.

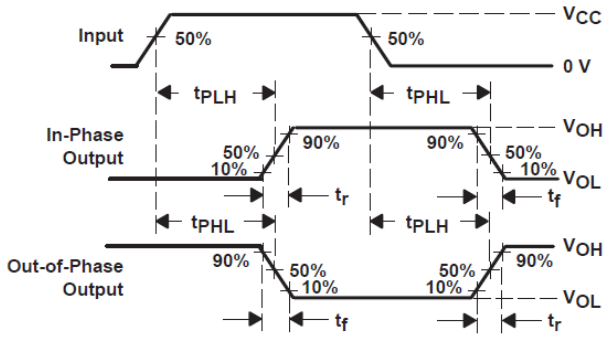


図 6-3. Voltage Waveforms
Propagation Delay and Output Transition Times

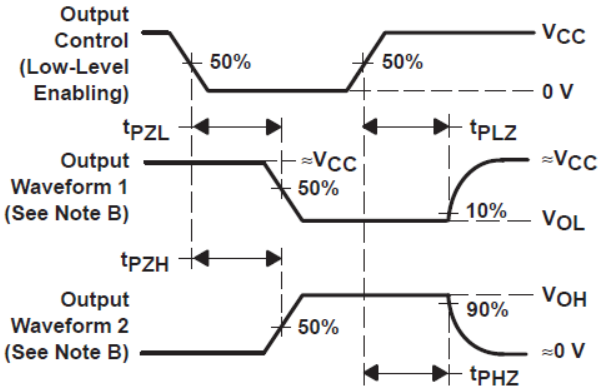


図 6-4. Voltage Waveforms
Enable and Disable Times For 3-State Outputs

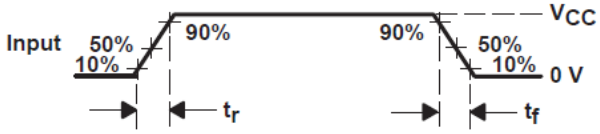


図 6-5. Voltage Waveform
Input Rise and Fall Times

A. C_L includes probe and test-fixture capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when diabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when diabled by the output control.

C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following charactersitics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.

D. The outputs are measured one at a time with one input transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

F. t_{PZL} and t_{PZH} are the same as t_{en}.

7 Detailed Description

7.1 Overview

These devices are designed to multiplex signals from 4-bit data sources to 4-output data lines in bus-organized systems. The 3-state outputs do not load the data lines when the output-enable ($\overline{G}$) input is at a high logic level.

To ensure the high-impedance state during power up or power down, $\overline{G}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

7.2 Functional Block Diagram

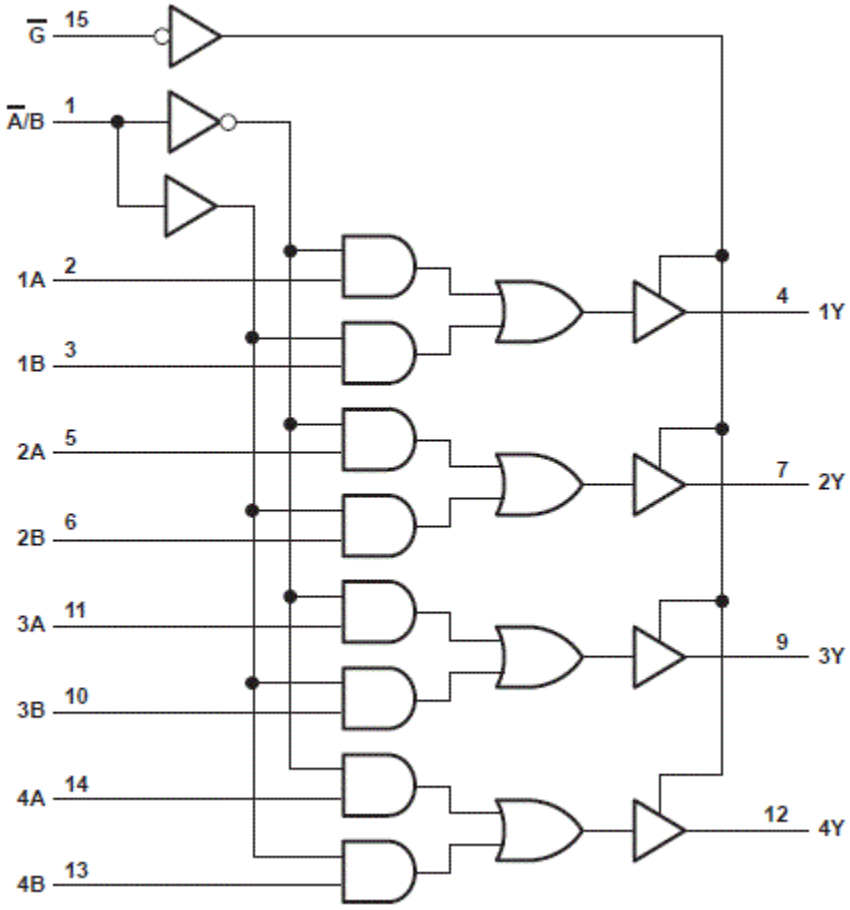


図 7-1. SN74HC257 Functional Block Diagram

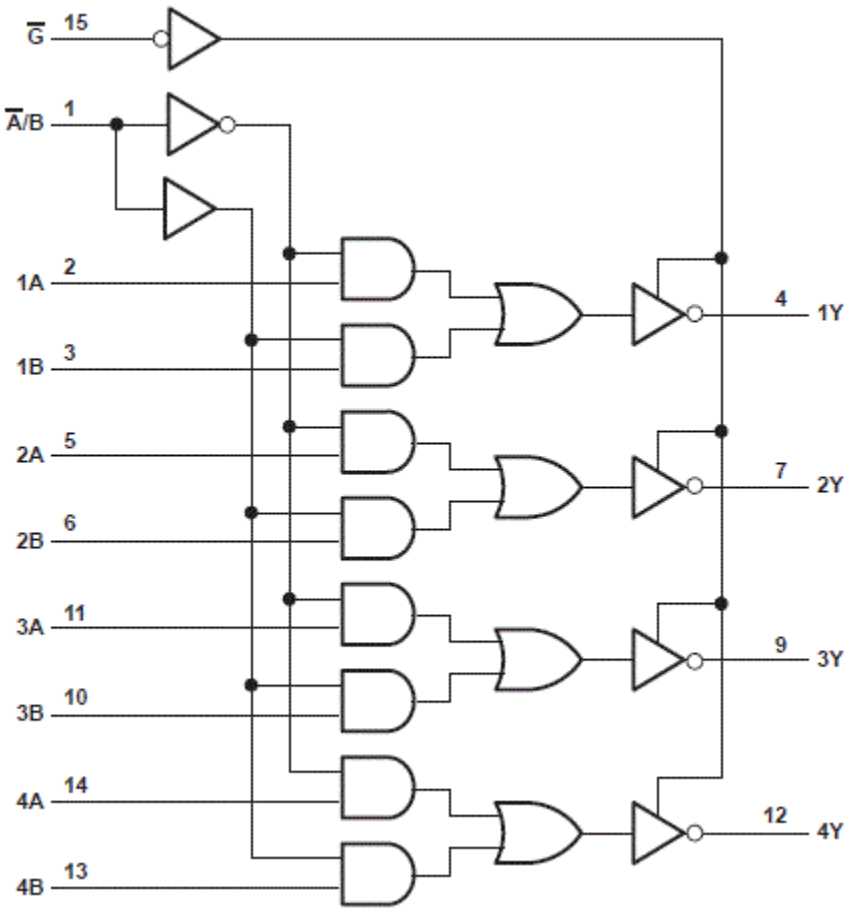


図 7-2. SN74HC258 Functional Block Diagram

7.3 Device Functional Modes

表 7-1. Function Table

INPUTS				OUTPUT Y	
$\overline{G}$	$\overline{A}$/B	A	B	'HC257	'HC258
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
85124012A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	85124012A SNJ54HC 257FK	Samples
8512401EA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8512401EA SNJ54HC257J	Samples
SN54HC257J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54HC257J	Samples
SN74HC257D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 85	HC257	
SN74HC257DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	HC257	Samples
SN74HC257DT	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 85	HC257	
SN74HC257N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC257N	Samples
SN74HC257NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC257	Samples
SN74HC257PW	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-40 to 85	HC257	
SN74HC257PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	HC257	Samples
SN74HC258D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 85	HC258	
SN74HC258DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC258	Samples
SN74HC258N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC258N	Samples
SN74HC258NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC258	Samples
SN74HC258PW	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-40 to 85	HC258	
SN74HC258PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC258	Samples
SNJ54HC257FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	85124012A SNJ54HC 257FK	Samples
SNJ54HC257J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8512401EA SNJ54HC257J	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN54HC257, SN74HC257 :

- Catalog : SN74HC257
- Military : SN54HC257

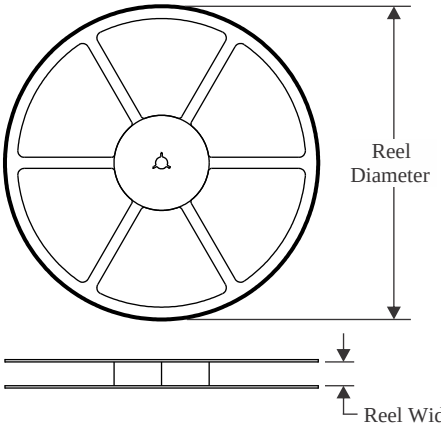
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

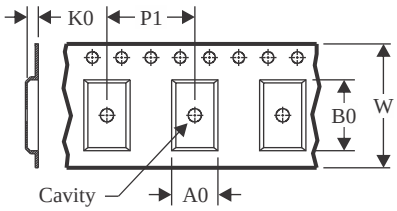
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

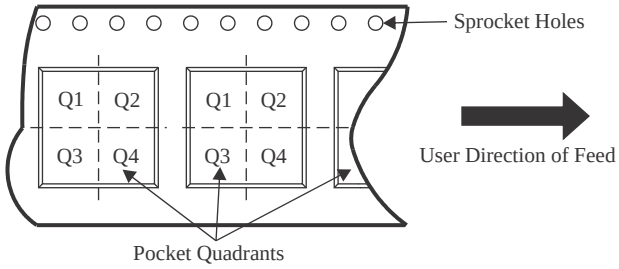


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

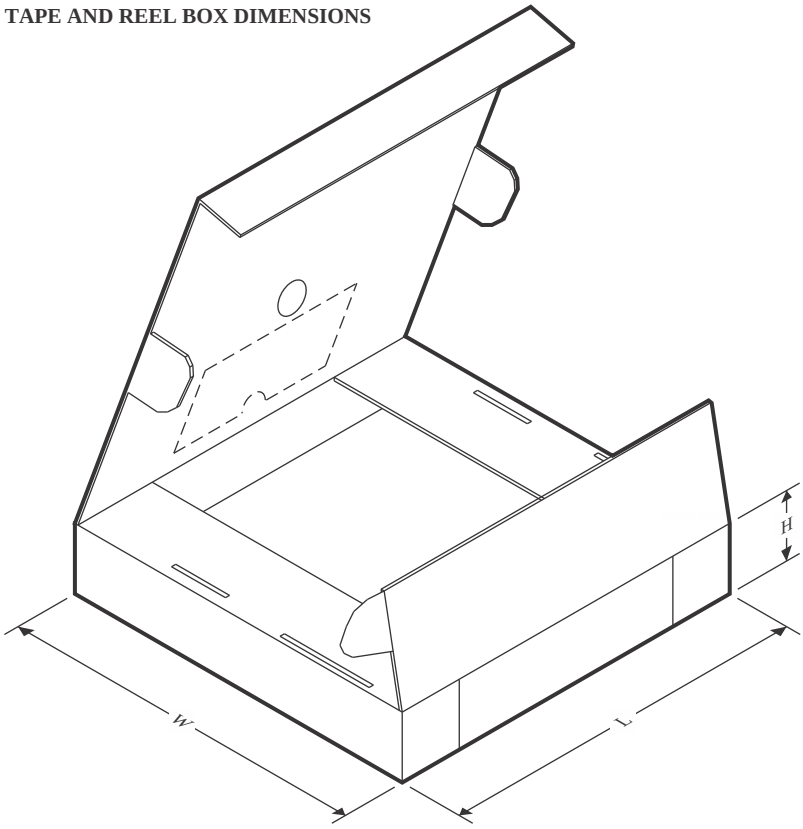
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC257DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC257NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74HC257NSR	SO	NS	16	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
SN74HC257PWR	TSSOP	PW	16	2000	330.0	12.4	6.85	5.45	1.6	8.0	12.0	Q1
SN74HC257PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC257PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC258DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC258NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74HC258PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

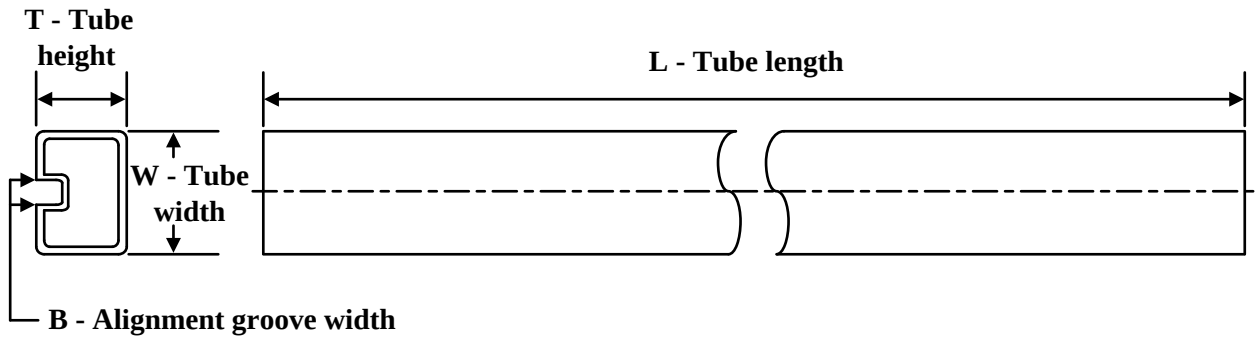
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC257DR	SOIC	D	16	2500	356.0	356.0	35.0
SN74HC257NSR	SO	NS	16	2000	356.0	356.0	35.0
SN74HC257NSR	SO	NS	16	2000	356.0	356.0	35.0
SN74HC257PWR	TSSOP	PW	16	2000	366.0	364.0	50.0
SN74HC257PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74HC257PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74HC258DR	SOIC	D	16	2500	340.5	336.1	32.0
SN74HC258NSR	SO	NS	16	2000	356.0	356.0	35.0
SN74HC258PWR	TSSOP	PW	16	2000	356.0	356.0	35.0

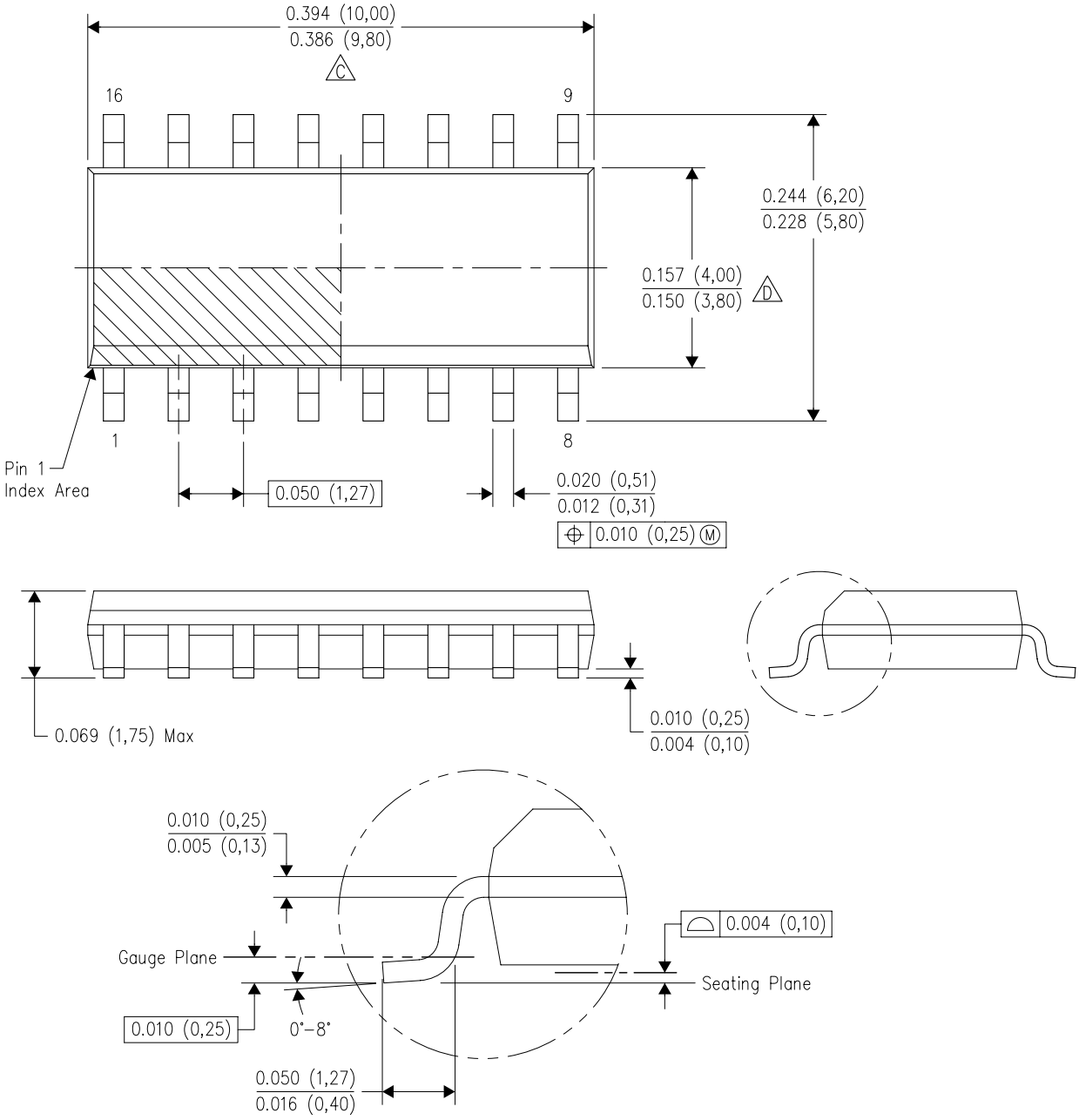
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
85124012A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN74HC257N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC257N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC258N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC258N	N	PDIP	16	25	506	13.97	11230	4.32
SNJ54HC257FK	FK	LCCC	20	55	506.98	12.06	2030	NA

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



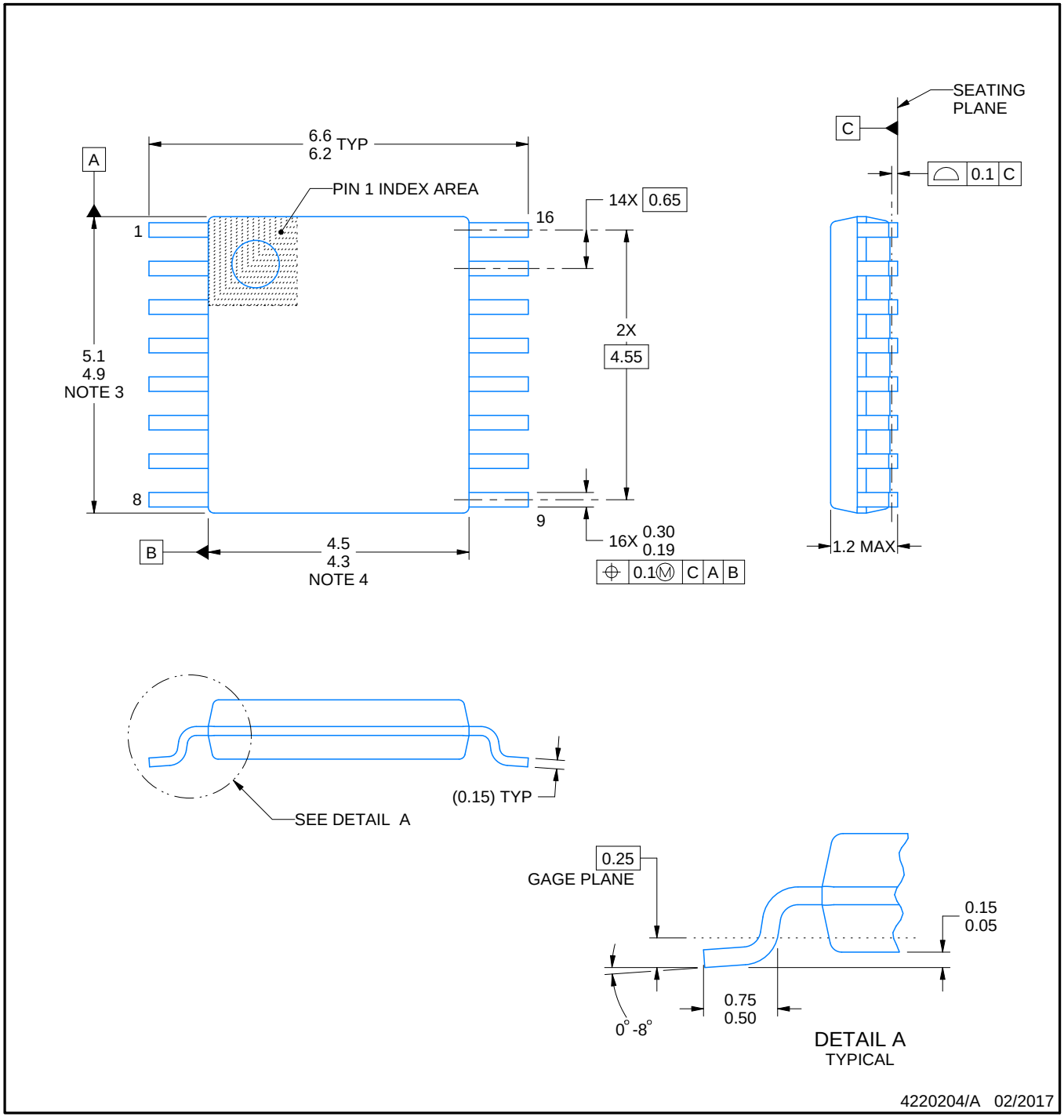
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

PACKAGE OUTLINE

PW0016A

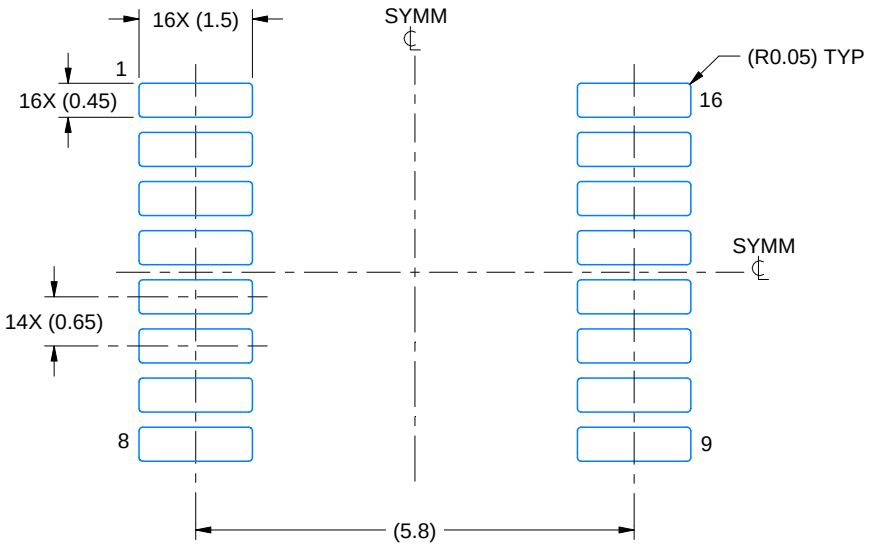
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

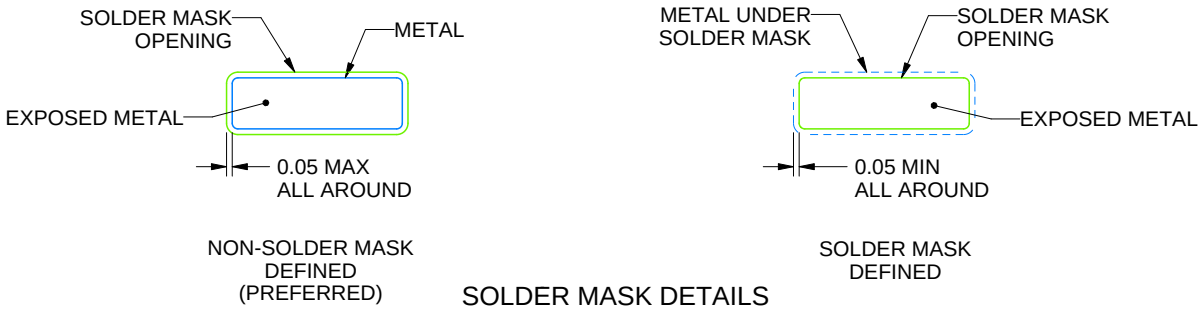


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

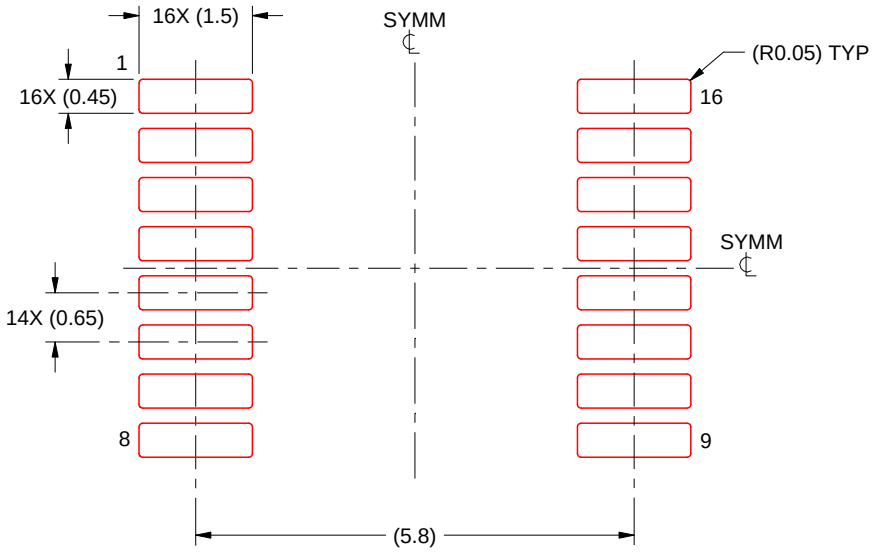


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

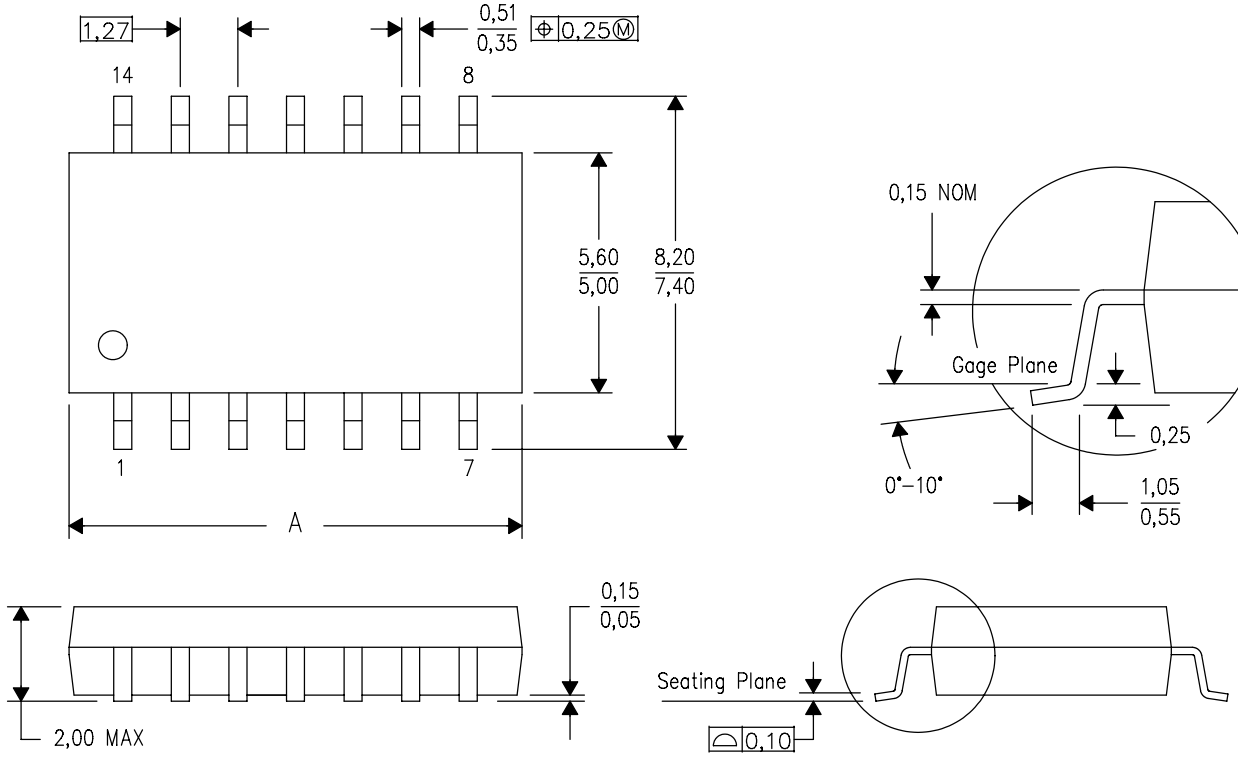
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

GENERIC PACKAGE VIEW

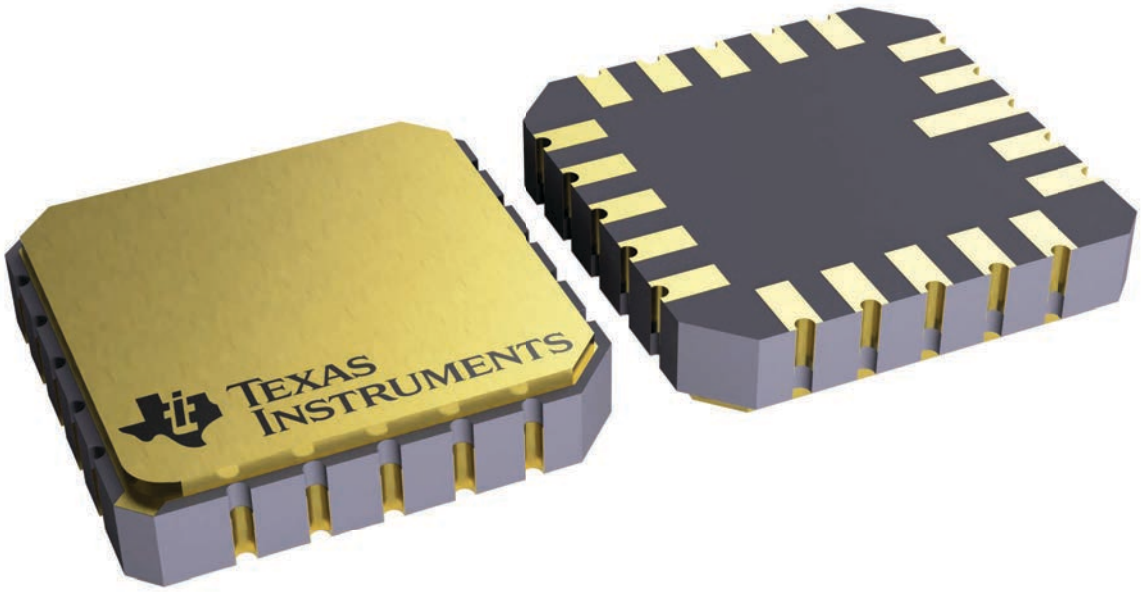
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

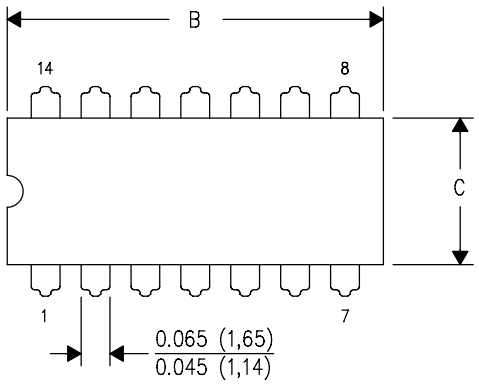


4229370VA\

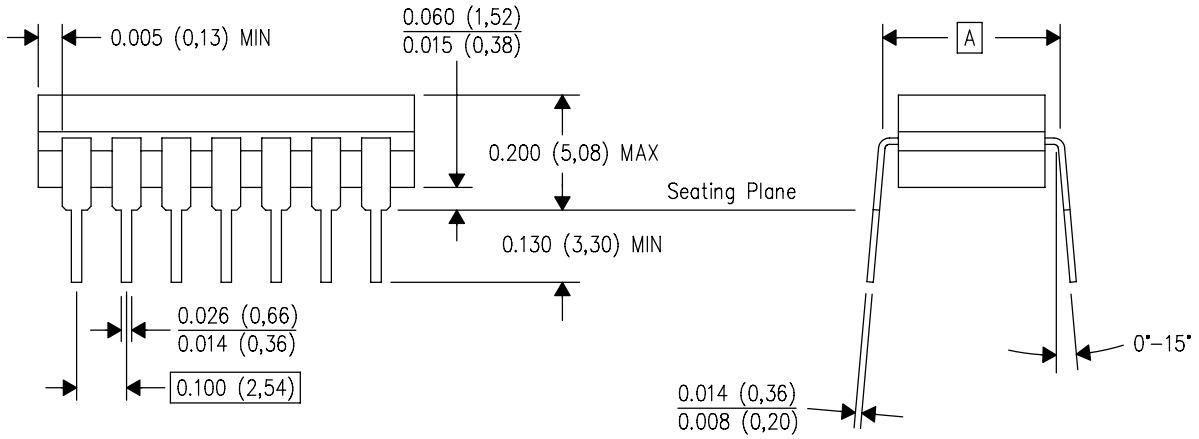
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



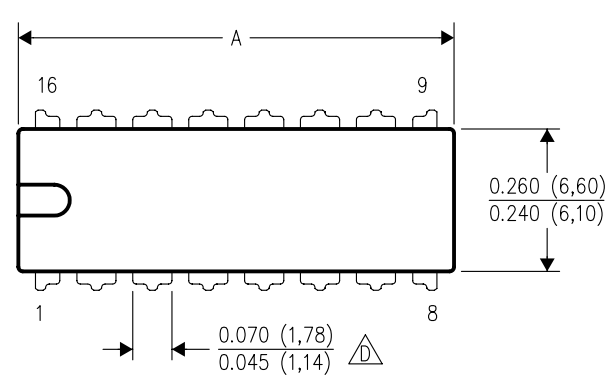
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

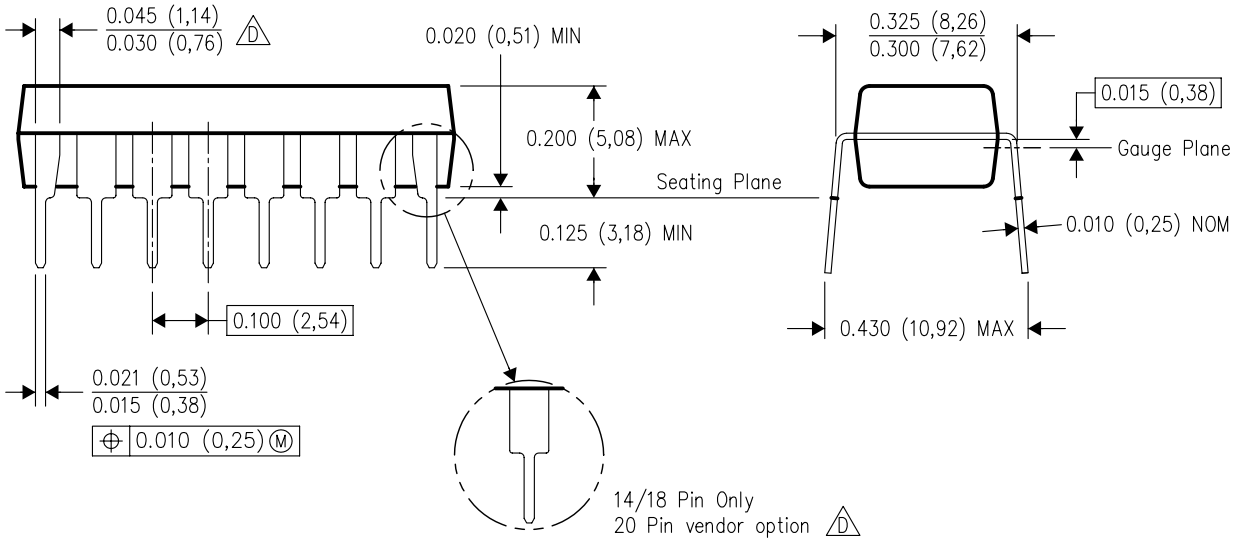
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

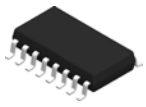


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

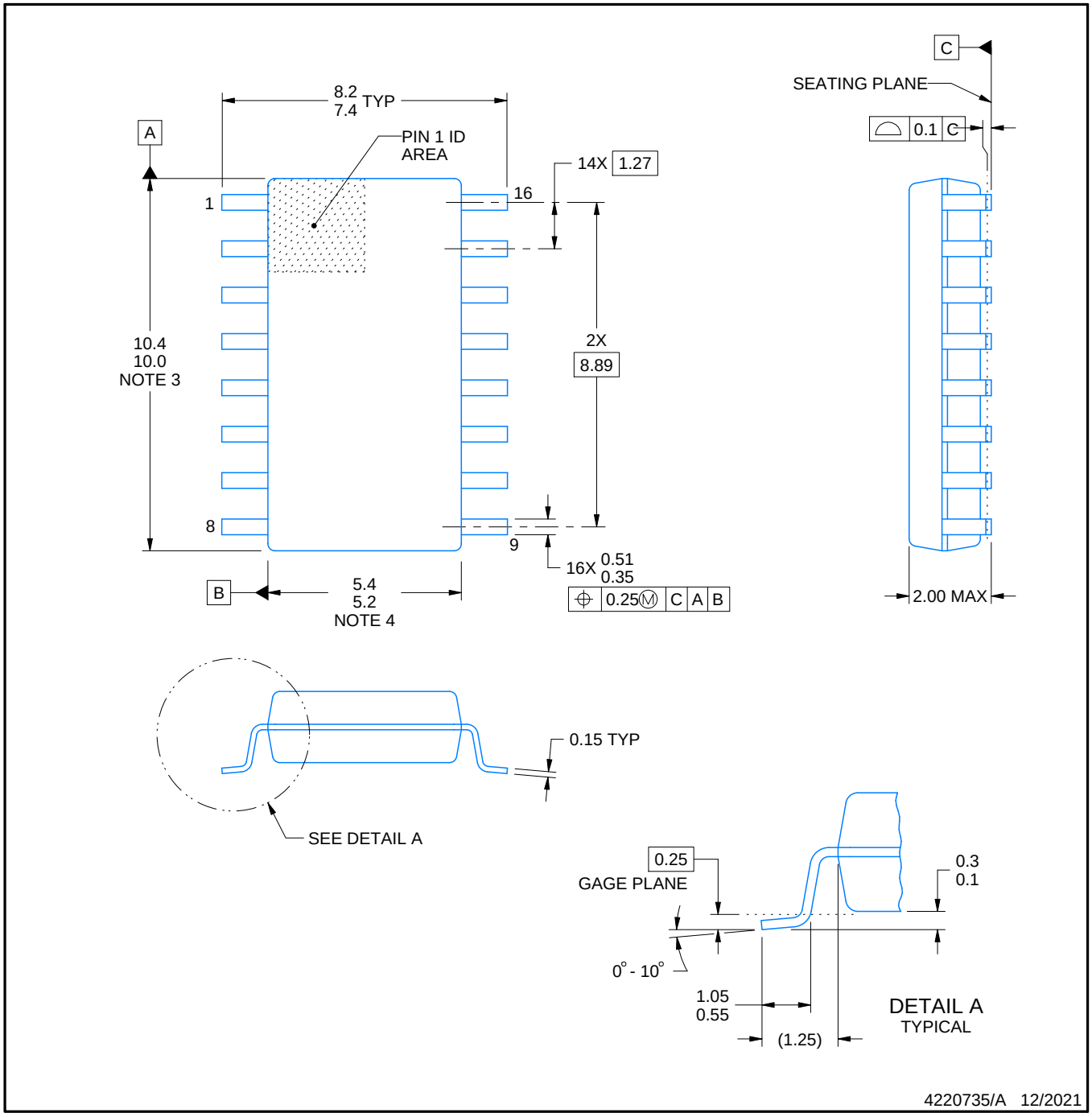


PACKAGE OUTLINE

NS0016A

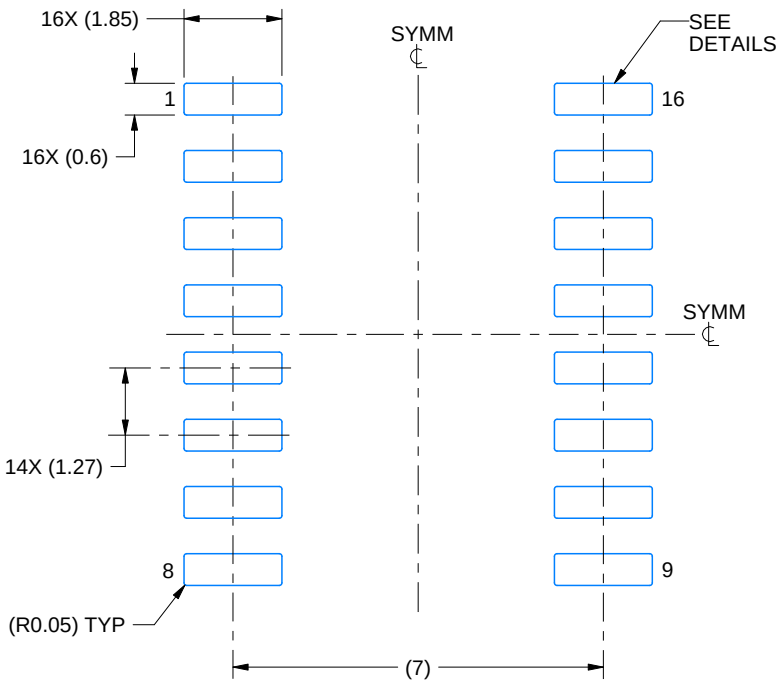
SOP - 2.00 mm max height

SOP

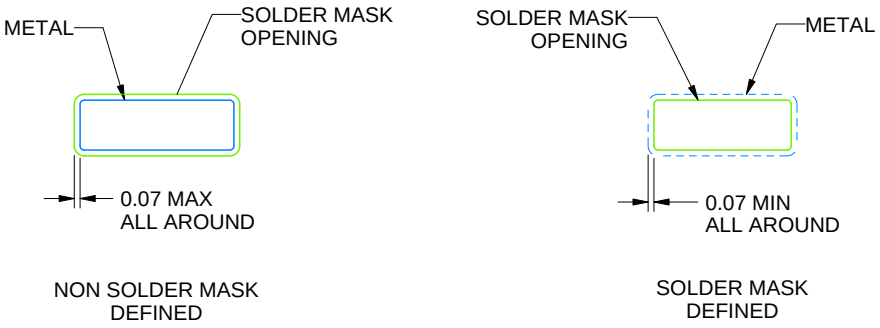


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

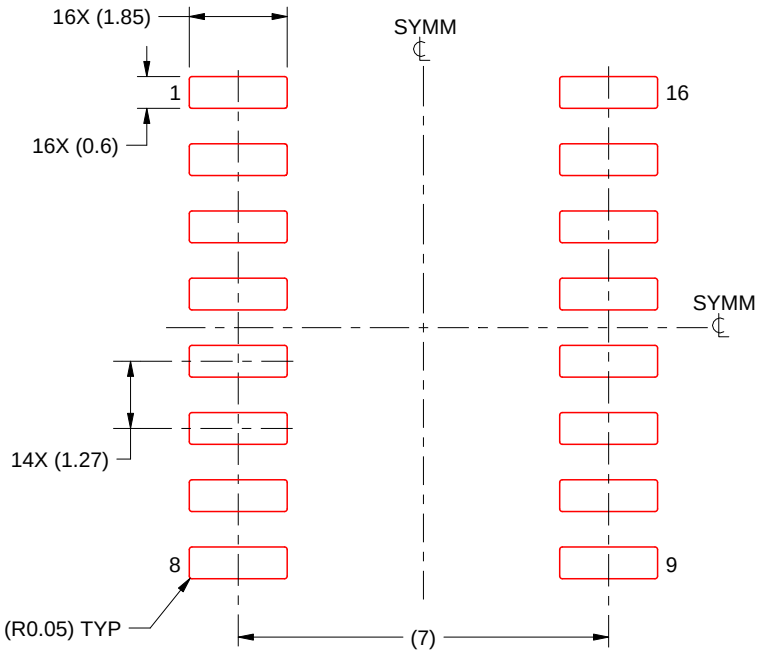
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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