

## SNx4HC540 3 ステート出力、オクタール・バッファ/ライン・ドライバ

### 1 特長

- 幅広い動作電圧範囲：2V～6V
- バス・ラインを直接、または最大 15 の LSTTL 負荷を駆動する大電流 3 ステート出力
- 低消費電力、 $I_{CC}$ ：80 $\mu$ A 以下
- $t_{pd}$  = 8ns (標準値)
- 5V で  $\pm$ 6mA の出力駆動能力
- 低い入力電流：最大 1 $\mu$ A
- データ・フロースルーのピン配置 (すべての入力は出力の反対側)

### 2 概要

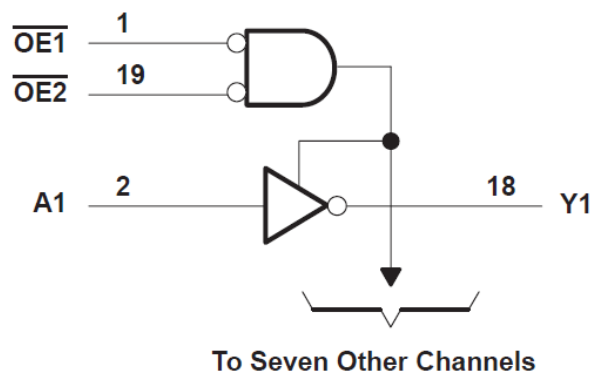
これらのオクタール・バッファおよびライン・ドライバは、一般的な HC240 シリーズの性能を備え、パッケージの反対側に各入力ピンと出力を配置しています。この配置により、プリント基板のレイアウトが大幅に簡素化されます。

3 ステート制御ゲートは、2 入力 NOR です。いずれかの出力イネーブル ( $\overline{OE1}$  または  $\overline{OE2}$ ) 入力が High の場合、8 つの出力はすべて高インピーダンス状態になります。HC540 デバイスの出力のデータは、反転されます。

### 製品情報

| 部品番号         | パッケージ <sup>(1)</sup> | 本体サイズ (公称)       |
|--------------|----------------------|------------------|
| SN54HC540J   | CDIP (20)            | 26.92mm × 6.92mm |
| SN74HC540DW  | SOIC (20)            | 12.80mm × 7.50mm |
| SN74HC540N   | PDIP (20)            | 25.40mm × 6.35mm |
| SN74HC540NSR | SO (20)              | 15.00mm × 5.30mm |
| SN74HC540PW  | TSSOP (20)           | 6.50mm × 4.40mm  |

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



機能ブロック図



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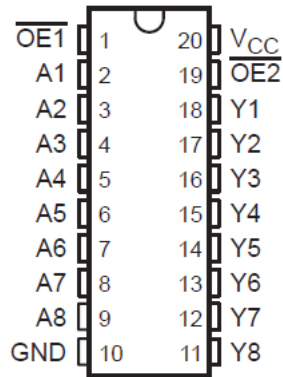
### 3 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

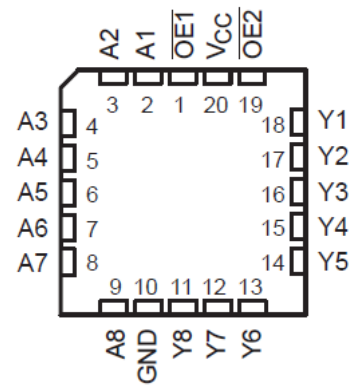
| <b>Changes from Revision E (January 2022) to Revision F (July 2022)</b>  | <b>Page</b> |
|--|-------------|
| • Junction-to-ambient thermal resistance values increased. DW was 58 is now 109.1, N was 69 is now 84.6, NS was 60 is now 113.4, PW was 83 is now 131.8..... | 4           |

| <b>Changes from Revision D (August 2003) to Revision E (January 2022)</b> | <b>Page</b> |
|---|-------------|
| • 最新のデータシート規格を反映するように、文書全体の採番、書式設定、表、図、相互参照を更新.....                       | 1           |

## 4 Pin Configuration and Functions



**J, DW, N, NS, PW package**  
**20-Pin CDIP, SOIC, PDIP, SO, TSSOP**  
**Top View**



**FK Package**  
**20-Pin CDIP**  
**Top View**

## 5 Specifications

### 5.1 Absolute Maximum Ratings

overoperating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                  |  | MIN  | MAX | UNIT |
|------------------|--|--|-----|------|
| V <sub>CC</sub>  | Supply voltage range                                     | -0.5   | 7   | V    |
| I <sub>IK</sub>  | Input clamp current <sup>(2)</sup>                       | V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>CC</sub> | ±20 | mA   |
| I <sub>OK</sub>  | Output clamp current <sup>(2)</sup>                      | V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> | ±20 | mA   |
| I <sub>O</sub>   | Continuous output current                                | V <sub>O</sub> = 0 to V <sub>CC</sub>                  | ±35 | mA   |
|                  | Continuous current through V <sub>CC</sub> or GND        |  | ±70 | mA   |
| T <sub>J</sub>   | Junction temperature                                     |  | 150 | °C   |
| T <sub>stg</sub> | Storage temperature range                                | -65  | 150 | °C   |
|                  | Lead temperature (Soldering 10s) (SOIC - Lead Tips Only) |  | 300 | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 5.2 Recommended Operating Conditions<sup>(1)</sup>

|                 |                                 | SN54HC540               |      |                 | SN74HC540 |      |                 | UNIT |
|-----------------|---------------------------------|-------------------------|------|-----------------|-----------|------|-----------------|------|
|                 |                                 | MIN                     | NOM  | MAX             | MIN       | NOM  | MAX             |      |
| V <sub>CC</sub> | Supply voltage                  | 2                       | 5    | 6               | 2         | 5    | 6               | V    |
| V <sub>IH</sub> | High-level input voltage        | V <sub>CC</sub> = 2 V   | 1.5  |                 | 1.5       |      |                 | V    |
|                 |                                 | V <sub>CC</sub> = 4.5 V | 3.15 |                 | 3.15      |      |                 |      |
|                 |                                 | V <sub>CC</sub> = 6 V   | 4.2  |                 | 4.2       |      |                 |      |
| V <sub>IL</sub> | Low-level input voltage         | V <sub>CC</sub> = 2 V   |      | 0.5             |           |      | 0.5             | V    |
|                 |                                 | V <sub>CC</sub> = 4.5 V |      | 1.35            |           | 1.35 |                 |      |
|                 |                                 | V <sub>CC</sub> = 6 V   |      | 1.8             |           | 1.8  |                 |      |
| V <sub>I</sub>  | Input voltage                   | 0                       |      | V <sub>CC</sub> | 0         |      | V <sub>CC</sub> | V    |
| V <sub>O</sub>  | Output voltage                  | 0                       |      | V <sub>CC</sub> | 0         |      | V <sub>CC</sub> | V    |
| Δt/Δv           | Input transition rise/fall time | V <sub>CC</sub> = 2 V   |      | 1000            |           |      | 1000            | ns   |
|                 |                                 | V <sub>CC</sub> = 4.5 V |      | 500             |           | 500  |                 |      |
|                 |                                 | V <sub>CC</sub> = 6 V   |      | 400             |           | 400  |                 |      |
| T <sub>A</sub>  | Operating free-air temperature  | -55                     |      | 125             | -40       |      | 85              | °C   |

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

### 5.3 Thermal Information

| THERMAL METRIC        |   | DW (SOIC) | N (PDIP) | NS (SO) | PW (TSSOP) | UNIT |
|-----------------------|---|-----------|----------|---------|------------|------|
|                       |   | 20 PINS   | 20 PINS  | 20 PINS | 20 PINS    |      |
| R <sub>θJA</sub>      | Junction-to-ambient thermal resistance <sup>(1)</sup> | 109.1     | 84.6     | 113.4   | 131.8      | °C/W |
| R <sub>θJC(top)</sub> | Junction-to-case (top) thermal resistance             | 76        | 72.5     | 78.6    | 72.2       | °C/W |
| R <sub>θJB</sub>      | Junction-to-board thermal resistance                  | 77.6      | 65.3     | 78.4    | 82.8       | °C/W |
| Ψ <sub>JT</sub>       | Junction-to-top characterization parameter            | 51.5      | 55.3     | 47.1    | 21.5       | °C/W |
| Ψ <sub>JB</sub>       | Junction-to-board characterization parameter          | 77.1      | 65.2     | 78.1    | 82.4       | °C/W |

### 5.3 Thermal Information (continued)

| THERMAL METRIC       |  | DW (SOIC) | N (PDIP) | NS (SO) | PW (TSSOP) | UNIT |
|----------------------|--|-----------|----------|---------|------------|------|
|                      |  | 20 PINS   | 20 PINS  | 20 PINS | 20 PINS    |      |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A       | N/A      | N/A     | N/A        | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

### 5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS                |                             | $V_{CC}$ | $T_A = 25^\circ\text{C}$ |           |      | SN54HC540  |     | SN74HC540  |               | UNIT |
|-----------|--------------------------------|-----------------------------|----------|--------------------------|-----------|------|------------|-----|------------|---------------|------|
|           |                                |                             |          | MIN                      | TYP       | MAX  | MIN        | MAX | MIN        | MAX           |      |
| $V_{OH}$  | $V_I = V_{IH}$ or $V_{IL}$     | $I_{OH} = -20\ \mu\text{A}$ | 2 V      | 1.9                      | 1.998     |      | 1.9        |     | 1.9        | V             |      |
|           |                                |                             | 4.5 V    | 4.4                      | 4.499     |      | 4.4        |     | 4.4        |               |      |
|           |                                |                             | 6 V      | 5.9                      | 5.999     |      | 5.9        |     | 5.9        |               |      |
|           |                                | $I_{OH} = -6\ \text{mA}$    | 4.5 V    | 3.98                     | 4.3       |      | 3.7        |     | 3.84       |               |      |
|           |                                |                             | 6 V      | 5.48                     | 5.8       |      | 5.2        |     | 5.34       |               |      |
| $V_{OL}$  | $V_I = V_{IH}$ or $V_{IL}$     | $I_{OL} = 20\ \mu\text{A}$  | 2 V      |                          | 0.002     | 0.1  |            | 0.1 |            | 0.1           | V    |
|           |                                |                             | 4.5 V    |                          | 0.001     | 0.1  |            | 0.1 |            | 0.1           |      |
|           |                                |                             | 6 V      |                          | 0.001     | 0.1  |            | 0.1 |            | 0.1           |      |
|           |                                | $I_{OL} = 6\ \text{mA}$     | 4.5 V    |                          | 0.17      | 0.26 |            | 0.4 |            | 0.33          |      |
|           |                                |                             | 6 V      |                          | 0.15      | 0.26 |            | 0.4 |            | 0.33          |      |
| $I_I$     | $V_I = V_{CC}$ or 0            | 6 V                         |          | $\pm 0.1$                | $\pm 100$ |      | $\pm 1000$ |     | $\pm 1000$ | nA            |      |
| $I_{OZ}$  | $V_O = V_{CC}$ or 0            | 6 V                         |          | $\pm 0.01$               | $\pm 0.5$ |      | $\pm 10$   |     | $\pm 5$    | $\mu\text{A}$ |      |
| $I_{CC}$  | $V_I = V_{CC}$ or 0, $I_O = 0$ | 6 V                         |          |                          | 8         |      | 160        |     | 80         | $\mu\text{A}$ |      |
| $C_i$     |                                | 2 V to 6 V                  |          | 3                        | 10        |      | 10         |     | 10         | pF            |      |

### 5.5 Switching Characteristics

over recommended operating free-air temperature range,  $C_L = 50\ \text{pF}$  (unless otherwise noted) (see [Figure 6-1](#))

| PARAMETER | FROM (INPUT)    | TO (OUTPUT) | $V_{CC}$ | $T_A = 25^\circ\text{C}$ |     |     | SN54HC540 |     | SN74HC540 |     | UNIT |
|-----------|-----------------|-------------|----------|--------------------------|-----|-----|-----------|-----|-----------|-----|------|
|           |                 |             |          | MIN                      | TYP | MAX | MIN       | MAX | MIN       | MAX |      |
| $t_{pd}$  | A               | Y           | 2 V      |                          | 35  | 100 |           | 149 |           | 125 | ns   |
|           |                 |             | 4.5 V    |                          | 10  | 20  |           | 30  |           | 25  |      |
|           |                 |             | 6 V      |                          | 8   | 17  |           | 25  |           | 21  |      |
| $t_{en}$  | $\overline{OE}$ | Y           | 2 V      |                          | 75  | 150 |           | 224 |           | 188 | ns   |
|           |                 |             | 4.5 V    |                          | 15  | 30  |           | 45  |           | 38  |      |
|           |                 |             | 6 V      |                          | 13  | 26  |           | 38  |           | 32  |      |
| $t_{dis}$ | $\overline{OE}$ | Y           | 2 V      |                          | 40  | 150 |           | 224 |           | 188 | ns   |
|           |                 |             | 4.5 V    |                          | 18  | 30  |           | 45  |           | 38  |      |
|           |                 |             | 6 V      |                          | 17  | 26  |           | 38  |           | 32  |      |
| $t_t$     |                 | Y           | 2 V      |                          | 28  | 60  |           | 90  |           | 75  | ns   |
|           |                 |             | 4.5 V    |                          | 8   | 12  |           | 18  |           | 15  |      |
|           |                 |             | 6 V      |                          | 6   | 10  |           | 15  |           | 13  |      |

## 5.6 Switching Characteristics

over recommended operating free-air temperature range,  $C_L = 150$  pF (unless otherwise noted) (see [Figure 6-1](#))

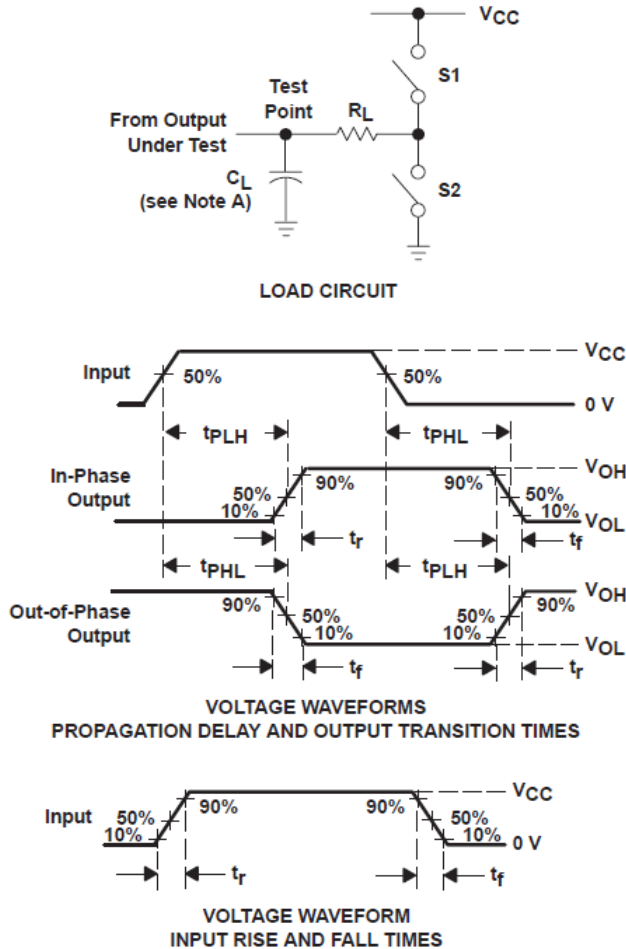
| PARAMETER | FROM (INPUT)    | TO (OUTPUT) | $V_{CC}$ | $T_A = 25^\circ\text{C}$ |     |     | SN54HC540 |     | SN74HC540 |     | UNIT |
|-----------|-----------------|-------------|----------|--------------------------|-----|-----|-----------|-----|-----------|-----|------|
|           |                 |             |          | MIN                      | TYP | MAX | MIN       | MAX | MIN       | MAX |      |
| $t_{pd}$  | A               | Y           | 2 V      |                          | 60  | 150 |           | 224 |           | 188 | ns   |
|           |                 |             | 4.5 V    |                          | 15  | 30  |           | 45  |           | 38  |      |
|           |                 |             | 6 V      |                          | 13  | 26  |           | 38  |           | 32  |      |
| $t_{en}$  | $\overline{OE}$ | Y           | 2 V      |                          | 100 | 200 |           | 298 |           | 250 | ns   |
|           |                 |             | 4.5 V    |                          | 20  | 40  |           | 60  |           | 50  |      |
|           |                 |             | 6 V      |                          | 17  | 34  |           | 51  |           | 43  |      |
| $t_t$     |                 | Y           | 2 V      |                          | 45  | 210 |           | 315 |           | 265 | ns   |
|           |                 |             | 4.5 V    |                          | 17  | 42  |           | 63  |           | 53  |      |
|           |                 |             | 6 V      |                          | 13  | 36  |           | 53  |           | 45  |      |

## 5.7 Operating Characteristics

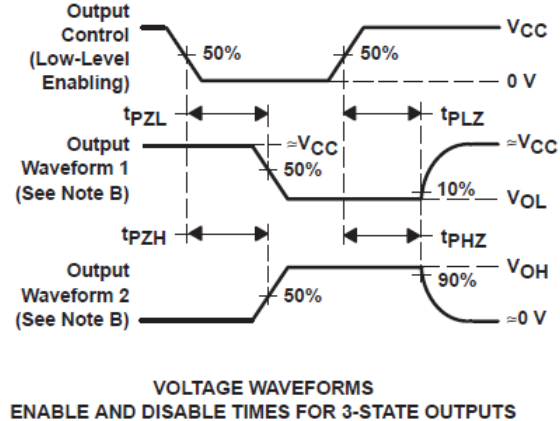
$T_A = 25^\circ\text{C}$

| PARAMETER |   | TEST CONDITIONS | TYP | UNIT |
|-----------|---|-----------------|-----|------|
| $C_{pd}$  | Power dissipation capacitance per buffer/driver | No load         | 35  | pF   |

## 6 Parameter Measurement Information



| PARAMETER         | $R_L$        | $C_L$           | S1     | S2     |
|-------------------|--------------|-----------------|--------|--------|
| $t_{en}$          | 1 k $\Omega$ | 50 pF or 150 pF | Open   | Closed |
|                   |              |                 | Closed | Open   |
| $t_{dis}$         | 1 k $\Omega$ | 50 pF           | Open   | Closed |
|                   |              |                 | Closed | Open   |
| $t_{pd}$ or $t_t$ | --           | 50 pF or 150 pF | Open   | Open   |



- $C_L$  includes probe and test-fixture capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.
- The outputs are measured one at a time with one input transition per measurement.
- $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

6-1. Load Circuit and Voltage Waveforms

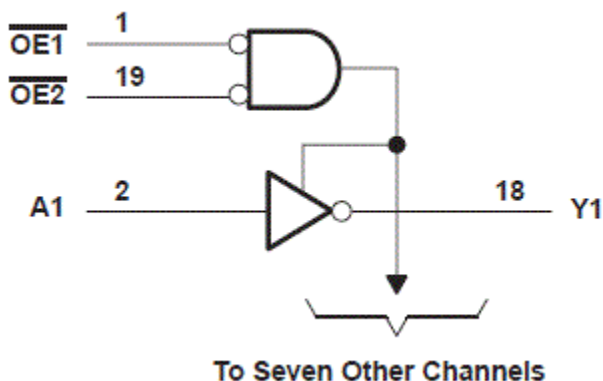
## 7 Detailed Description

### 7.1 Overview

These octal buffers and line drivers feature the performance of the popular 'HC240 series and offer a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly facilitates printed circuit board layout.

The 3-state control gate is a 2-input NOR. If either output-enable ( $\overline{OE1}$  or  $\overline{OE2}$ ) input is high, all eight outputs are in the high-impedance state. The 'HC540 devices provide inverted data at the outputs.

### 7.2 Functional Block Diagram



### 7.3 Device Functional Modes

**表 7-1. Function Table  
(Each Buffer/Driver)**

| INPUTS           |                  |   | OUTPUT<br>Y |
|------------------|------------------|---|-------------|
| $\overline{OE1}$ | $\overline{OE2}$ | A |             |
| L                | L                | L | H           |
| L                | L                | H | L           |
| H                | X                | X | Z           |
| X                | H                | X | Z           |



## 8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- $\mu\text{F}$  capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- $\mu\text{F}$  and 1- $\mu\text{F}$  capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 9 Layout

### 9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

## 10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 10.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の [使用条件](#) を参照してください。

### 10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
すべての商標は、それぞれの所有者に帰属します。

### 10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)  | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|------------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| JM38510/65710BRA | ACTIVE        | CDIP         | J               | 20   | 20          | Non-RoHS & Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/<br>65710BRA    | <a href="#">Samples</a> |
| M38510/65710BRA  | ACTIVE        | CDIP         | J               | 20   | 20          | Non-RoHS & Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/<br>65710BRA    | <a href="#">Samples</a> |
| SN54HC540J       | ACTIVE        | CDIP         | J               | 20   | 20          | Non-RoHS & Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SN54HC540J              | <a href="#">Samples</a> |
| SN74HC540DWR     | ACTIVE        | SOIC         | DW              | 20   | 2000        | RoHS & Green     | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | HC540                   | <a href="#">Samples</a> |
| SN74HC540N       | ACTIVE        | PDIP         | N               | 20   | 20          | RoHS & Green     | NIPDAU                               | N / A for Pkg Type   | -40 to 85    | SN74HC540N              | <a href="#">Samples</a> |
| SN74HC540NSR     | ACTIVE        | SO           | NS              | 20   | 2000        | RoHS & Green     | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | HC540                   | <a href="#">Samples</a> |
| SN74HC540PWR     | ACTIVE        | TSSOP        | PW              | 20   | 2000        | RoHS & Green     | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | HC540                   | <a href="#">Samples</a> |
| SN74HC540PWRE4   | ACTIVE        | TSSOP        | PW              | 20   | 2000        | RoHS & Green     | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | HC540                   | <a href="#">Samples</a> |
| SNJ54HC540J      | ACTIVE        | CDIP         | J               | 20   | 20          | Non-RoHS & Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SNJ54HC540J             | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54HC540, SN74HC540 :**

- Catalog : [SN74HC540](#)
- Military : [SN54HC540](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74HC540DWR | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.9    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| SN74HC540DWR | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.9    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| SN74HC540NSR | SO           | NS              | 20   | 2000 | 330.0              | 24.4               | 8.4     | 13.0    | 2.5     | 12.0    | 24.0   | Q1            |
| SN74HC540PWR | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.0     | 1.4     | 8.0     | 16.0   | Q1            |
| SN74HC540PWR | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.0     | 1.4     | 8.0     | 16.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74HC540DWR | SOIC         | DW              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| SN74HC540DWR | SOIC         | DW              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| SN74HC540NSR | SO           | NS              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| SN74HC540PWR | TSSOP        | PW              | 20   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74HC540PWR | TSSOP        | PW              | 20   | 2000 | 356.0       | 356.0      | 35.0        |

**TUBE**


\*All dimensions are nominal

| Device     | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74HC540N | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14                     | 16                     | 18                     | 20                     |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A             | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX         | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN         | —                      | —                      | —                      | —                      |
| C MAX         | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN         | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



# EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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