TEXAS INSTRUMENTS
SN54HC595, SN74HC595
JAJSN44J – DECEMBER 1982 – REVISED OCTOBER 2021

SNx4HC595 3 ステート出力レジスタ搭載 8 ビット・シフト・レジスタ

1 特長

- 8 ビットのシリアル・イン / パラレル・アウト・シフト
- 幅広い動作電圧範囲：2V～6V
- 大電流 3 ステート出力により最大 15 個の LSTTL 負荷を駆動可能
- 低い消費電力：I_{CC} = 80μA 以下
- t_{pd} = 13ns (標準値)
- 5V で ±6mA の出力駆動能力
- 入力電流ロー：1μA 以下
- シフト・レジスタはダイレクト・クリアを装備
- MIL-PRF-38535 準拠の製品については、特に記述のない限り、すべてのパラメータはテスト済みです。その他のすべての製品については、量産プロセスにすべてのパラメータのテストが含まれているとは限りません。

2 アプリケーション

- ネットワーク・スイッチ
- 電力インフラストラクチャ
- LED ディスプレイ
- サーバー

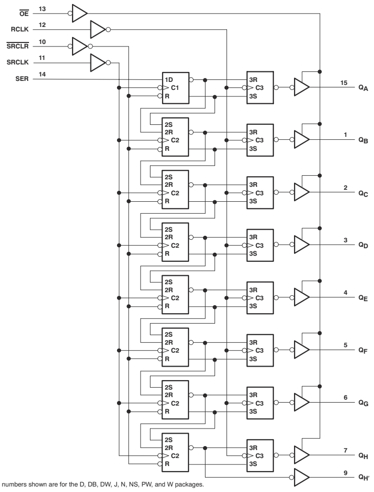
3 概要

SNx4HC595 には 8 ビットのシリアル・イン、パラレル・アウトのシフト・レジスタが搭載されており、8 ビットの D タイプ・ストレージ・レジスタへデータを供給します。ストレージ・レジスタはパラレル 3 ステート出力を備えています。シフト・レジスタとストレージ・レジスタの両方に、それぞれ独立したクロックが供給されます。シフト・レジスタはダイレクト・オーバーライディング・クリア ($\overline{\text{SRCLR}}$) 入力、シリアル (SER) 入力、カスケード用シリアル出力を備えています。出力イネーブル ($\overline{\text{OE}}$) 入力が HIGH のとき、出力は高インピーダンス状態になります。

製品情報

部品番号	パッケージ [1]	本体サイズ (公称)
SN54HC595FK	LCCC (20)	8.89mm × 8.89mm
SN54HC595J	CDIP (16)	21.34mm × 6.92mm
SN74HC595N	PDIP (16)	19.31mm × 6.35mm
SN74HC595D	SOIC (16)	9.90mm × 3.90mm
SN74HC595DW	SOIC (16)	10.30mm × 7.50mm
SN74HC595DB	SSOP (16)	6.20mm × 5.30mm
SN74HC595PW	TSSOP (16)	5.00mm × 4.40mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



Pin numbers shown are for the D, DB, DW, J, N, NS, PW, and W packages.

機能ブロック図

Table of Contents

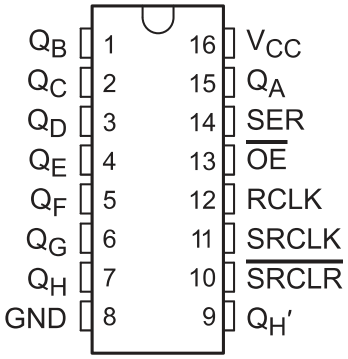
4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

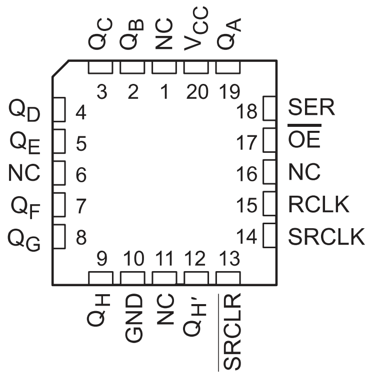
Changes from Revision H (November 2009) to Revision I (August 2015)	Page
• 「アプリケーション」セクション、「製品情報」表、「ピン構成および機能」セクション、「ESD 定格」表、「熱に関する情報」表、「機能説明」セクション、「デバイスの機能モード」、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加。	1
• 「注文情報」表を削除。	1
• 「特長」の一覧に軍事利用についての免責事項を追加。	1

Changes from Revision I (August 2015) to Revision J (October 2021)	Page
• 「製品情報」表、「ESD 定格」表、「デバイスの機能モード」表を、最新のデータシート規格に合うように更新。	1

5 Pin Configuration and Functions



D, N, NS, J, DB, or PW Package
16-Pin SOIC, PDIP, SO, CDIP, SSOP, or TSSOP
Top View



FK Package
20-Pin LCCC
Top View

表 5-1. Pin Functions

PIN			I/O(1)	DESCRIPTION
NAME	SOIC, PDIP, SO, CDIP, SSOP, or TSSOP	LCCC		
GND	8	10	—	Ground Pin
$\overline{OE}$	13	17	I	Output Enable
Q_A	15	19	O	Q_A Output
Q_B	1	2	O	Q_B Output
Q_C	2	3	O	Q_C Output
Q_D	3	4	O	Q_D Output
Q_E	4	5	O	Q_E Output
Q_F	5	7	O	Q_F Output
Q_G	6	8	O	Q_G Output
Q_H	7	9	O	Q_H Output
$Q_{H'}$	9	12	O	$Q_{H'}$ Output
RCLK	12	14	I	RCLK Input
SER	14	18	I	SER Input
SRCLK	11	14	I	SRCLK Input
$\overline{SRCLR}$	10	13	I	$\overline{SRCLR}$ Input
NC	—	1 16 11 16	—	No Connection
V_{CC}	—	20	—	Power Pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
I_{IK}	Input clamp current(2)	$V_I < 0$ or $V_I > V_{CC}$		±20	mA
I_{OK}	Output clamp current (2)	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±35	mA
	Continuous current through V_{CC} or GND			±70	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			SN54HC595			SN74HC595			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V			0.5			0.5	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 6 V			1.8			1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall time(2)	V_{CC} = 2 V			1000			1000	ns
		V_{CC} = 4.5 V			500			500	
		V_{CC} = 6 V			400			400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.
(2) If this device is used in the threshold region (from V_{IL}max = 0.5 V to V_{IH} min = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t_t = 1000 ns and V_{CC} = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

6.4 Thermal Information

THERMAL METRIC(1)		SN74HC595						UNIT
		D (SOIC)	DB (SSOP)	DW (SOIC)	N (PDIP)	NS (SO)	PW (TSSOP)	
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	73	82	57	67	64	108	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

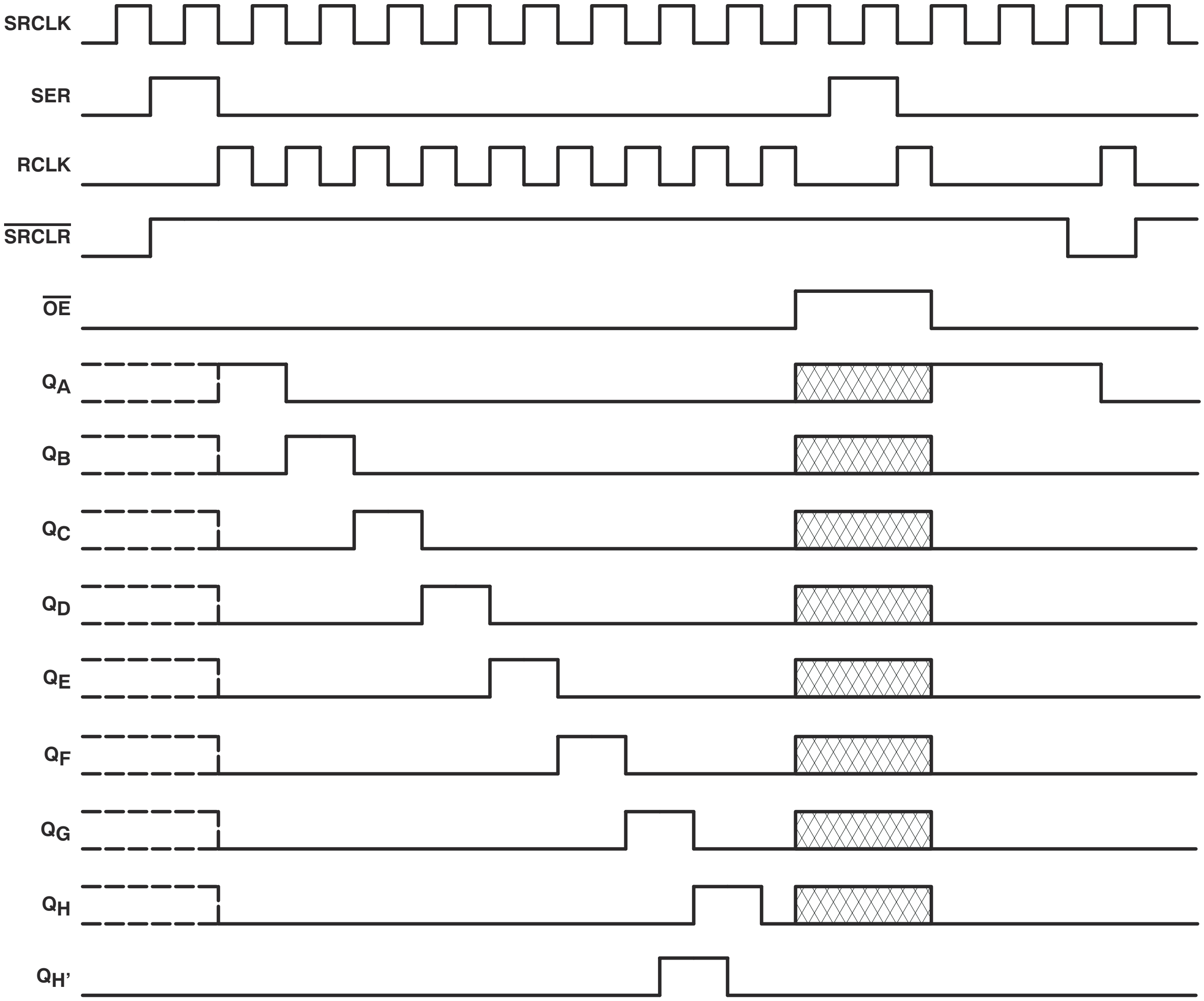
PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC595		SN74HC595		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = –20 µA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		$Q_{H'}$, I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		$Q_A – Q_H$, I_{OH} = –6 mA		3.98	4.3		3.7		3.84		
		$Q_{H'}$, I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
		$Q_A – Q_H$, I_{OH} = –7.8 mA		5.48	5.8		5.2		5.34		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 µA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		$Q_{H'}$, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		$Q_A – Q_H$, I_{OL} = 6 mA			0.17	0.26		0.4		0.33	
		$Q_{H'}$, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
		$Q_A – Q_H$, I_{OL} = 7.8 mA			0.15	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	$V_O = V_{CC}$ or 0, $Q_A – Q_H$		6 V		±0.01	±0.5		±10		±5	µA
I_{CC}	$V_I = V_{CC}$ or 0, I_O = 0		6 V			8		160		80	µA
C_i			2 V to 6 V		3	10		10		10	pF

6.6 Timing Requirements

over operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC595		SN74HC595		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V		6		4.2		5	MHz
			4.5 V		31		21		25	
			6 V		36		25		29	
t_w	Pulse duration	SRCLK or RCLK high or low	2 V	80		120		100		ns
			4.5 V	16		24		20		
			6 V	14		20		17		
		$\overline{\text{SRCLR}}$ low	2 V	80		120		100		
			4.5 V	16		24		20		
			6 V	14		20		17		
t_{su}	Set-up time	SER before SRCLK ↑	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
		SRCLK ↑ before RCLK ↑ (1)	2 V	75		113		94		
			4.5 V	15		23		19		
			6 V	13		19		16		
		$\overline{\text{SRCLR}}$ low before RCLK ↑	2 V	50		75		65		
			4.5 V	10		15		13		
			6 V	9		13		11		
		$\overline{\text{SRCLR}}$ high (inactive) before SRCLK ↑	2 V	50		75		60		
			4.5 V	10		15		12		
			6 V	9		13		11		
t_h	Hold time, SER after SRCLK ↑		2 V	0		0		0		ns
			4.5 V	0		0		0		
			6 V	0		0		0		

(1) This set-up time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.



NOTE: ▨ implies that the output is in 3-State mode.

図 6-1. Timing Diagram

6.7 Switching Characteristics

Over recommended operating free-air temperature range.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	T_A = 25°C			SN54HC595		SN74HC595		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			50 pF	2 V	6	26		4.2		5		MHz
				4.5 V	31	38		21		25		
				6 V	36	42		25		29		
t_{pd}	SRCLK	$Q_{H'}$	50 pF	2 V		50	160		240		200	ns
				4.5 V		17	32		48		40	
				6 V		14	27		41		34	
	RCLK	$Q_A – Q_H$	50 pF	2 V		50	150		225		187	
				4.5 V		17	30		45		37	
				6 V		14	26		38		32	
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$	50 pF	2 V		51	175		261		219	ns
				4.5 V		18	35		52		44	
				6 V		15	30		44		37	
t_{en}	$\overline{OE}$	$Q_A – Q_H$	50 pF	2 V		40	150		255		187	ns
				4.5 V		15	30		45		37	
				6 V		13	26		38		32	
t_{dis}	$\overline{OE}$	$Q_A – Q_H$	50 pF	2 V		42	200		300		250	ns
				4.5 V		23	40		60		50	
				6 V		20	34		51		43	
t_t		$Q_A – Q_H$	50 pF	2 V		28	60		90		75	ns
				4.5 V		8	12		18		15	
				6 V		6	10		15		13	
		$Q_{H'}$	50 pF	2 V		28	75		110		95	
				4.5 V		8	15		22		19	
				6 V		6	13		19		16	
t_{pd}	RCLK	$Q_A – Q_H$	150 pf	2 V		60	200		300		250	ns
				4.5 V		22	40		60		50	
				6 V		19	34		51		43	
t_{en}	$\overline{OE}$	$Q_A – Q_H$	150 pf	2 V		70	200		298		250	ns
				4.5 V		23	40		60		50	
				6 V		19	34		51		43	
t_t		$Q_A – Q_H$	150 pf	2 V		45	210		315		265	ns
				4.5 V		17	42		63		53	
				6 V		13	36		53		45	

6.8 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	400	pF

6.9 Typical Characteristics

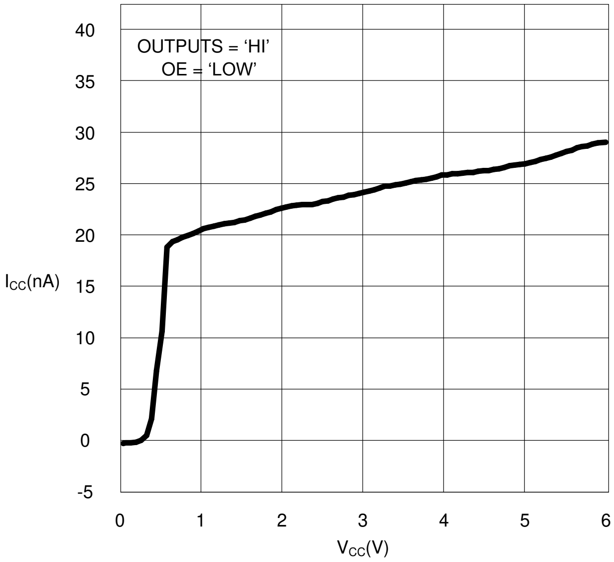
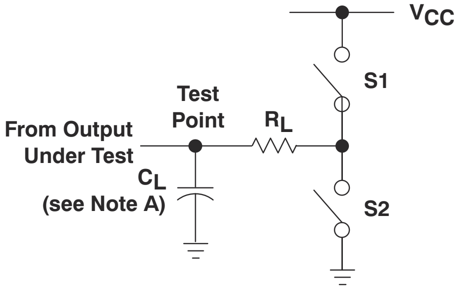


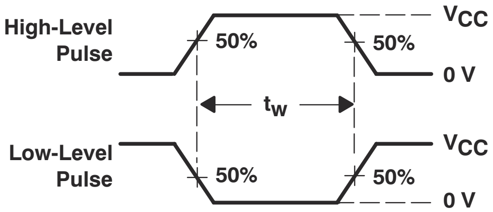
図 6-2. SN74HC595 I_{CC} vs. V_{CC}

7 Parameter Measurement Information

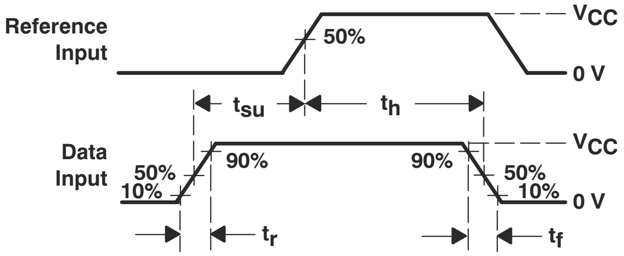


LOAD CIRCUIT

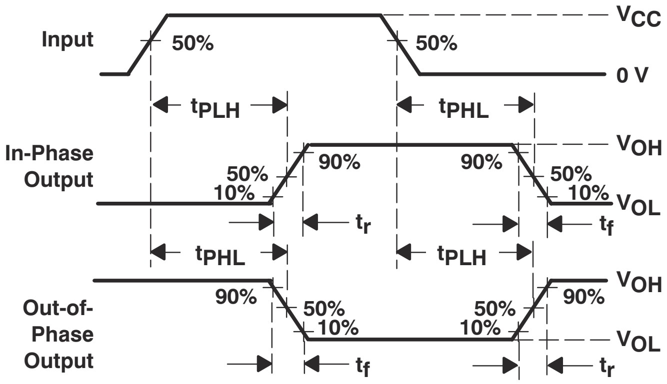
PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t			50 pF or 150 pF	Open	Open



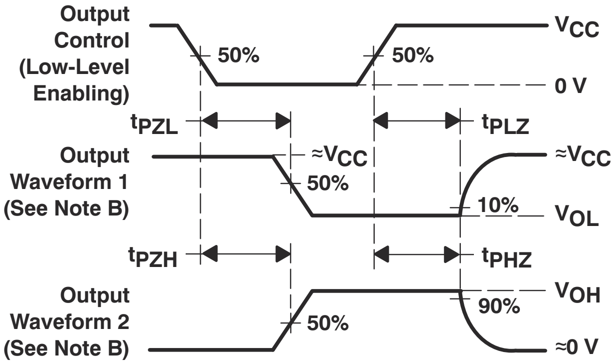
VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES:
- A. C_L includes probe and test-fixture capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
- D. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
- E. The outputs are measured one at a time, with one input transition per measurement.
- F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- G. t_{PZL} and t_{PZH} are the same as t_{en}.
- H. t_{PLH} and t_{PHL} are the same as t_{pd}.

図 7-1. Load Circuit and Voltage Waveforms

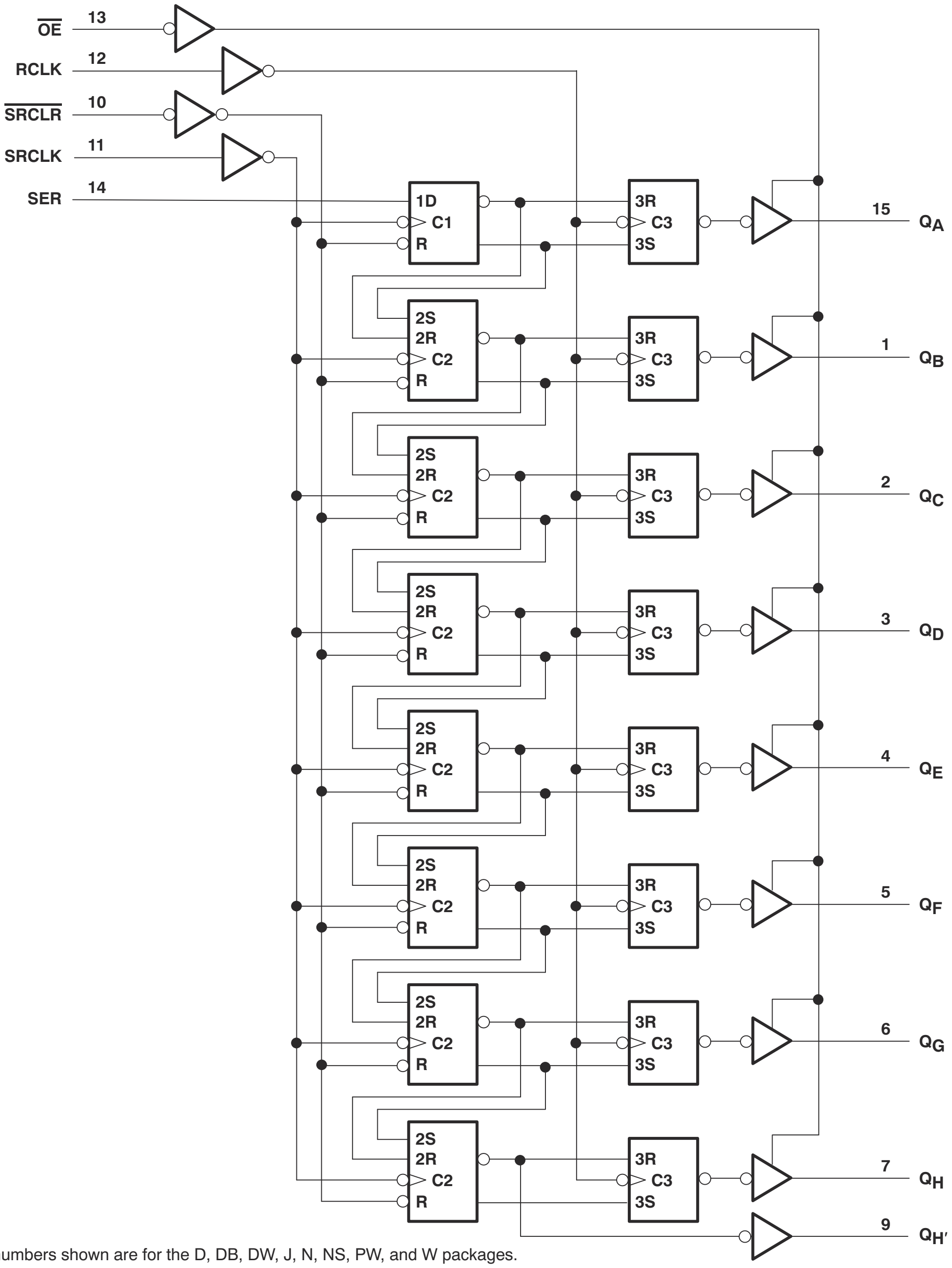
8 Detailed Description

8.1 Overview

The SNx4HC595 is part of the HC family of logic devices intended for CMOS applications. The SNx4HC595 is an 8-bit shift register that feeds an 8-bit D-type storage register.

Both the shift register clock (SRCLK) and storage register clock (RCLK) are positive-edge triggered. If both clocks are connected together, the shift register always is one clock pulse ahead of the storage register.

8.2 Functional Block Diagram



Pin numbers shown are for the D, DB, DW, J, N, NS, PW, and W packages.

8.3 Feature Description

The SNx4HC595 devices are 8-bit Serial-In, Parallel-Out Shift Registers. They have a wide operating current of 2 V to 6 V, and the high-current 3-state outputs can drive up to 15 LSTTL Loads. The devices have a low power consumption of 80-µA (Maximum) I_{CC}. Additionally, the devices have a low input current of 1 µA (Maximum) and a ±6-mA Output Drive at 5 V.

8.4 Device Functional Modes

表 8-1 lists the functional modes of the SNx4HC595 devices.

表 8-1. Function Table

INPUTS					FUNCTION
SER	SRCLK	$\overline{\text{SRCLR}}$	RCLK	$\overline{\text{OE}}$	
X	X	X	X	H	Outputs Q_A – Q_H are disabled.
X	X	X	X	L	Outputs Q_A – Q_H are enabled.
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of the shift register goes high. Other stages store the data of previous stage, respectively.
X	X	X	↑	X	Shift-register data is stored in the storage register.

9 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。また、お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The SNx4HC595 is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs.

9.2 Typical Application

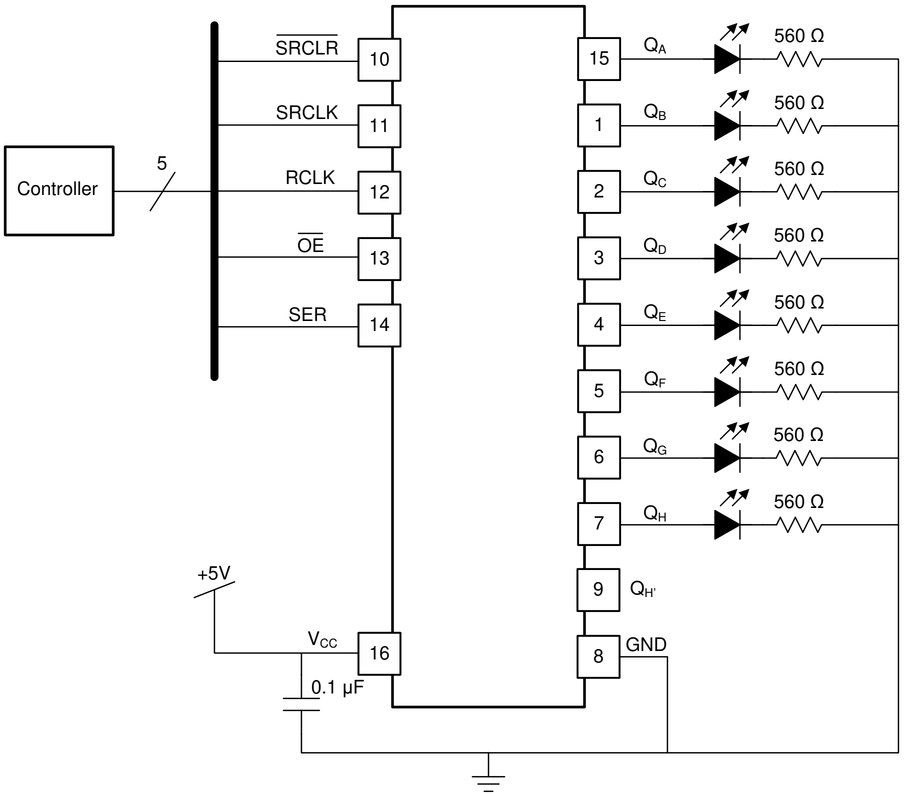


図 9-1. Typical Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

- Recommended input conditions
  - Specified high and low levels. See (V_{IH} and V_{IL}) in *セクション 6.3* table.
  - Specified high and low levels. See (V_{IH} and V_{IL}) in *セクション 6.3* table.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}
- Recommend output conditions
  - Load currents should not exceed 35 mA per output and 70 mA total for the part
  - Outputs should not be pulled above V_{CC}

9.2.3 Application Curves

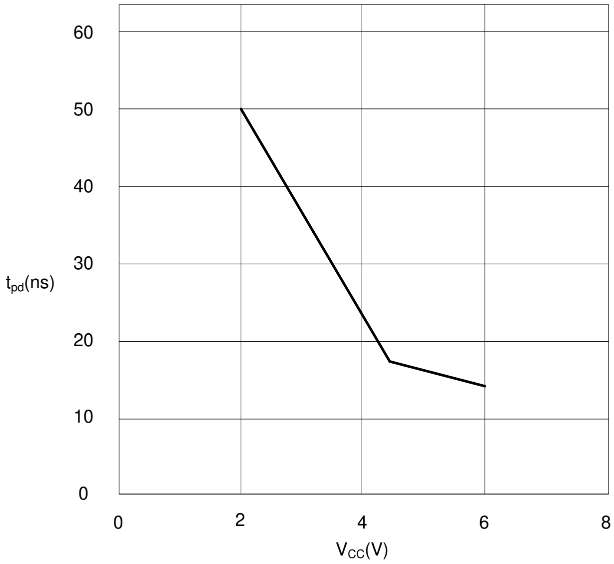


図 9-2. SN75HC595 t_{pd} vs. V_{CC}

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in *セクション 6.3* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µf is recommended; if there are multiple V_{CC} pins, then 0.01 µf or 0.022 µf is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 µf and a 1 µf are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. 図 11-1 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the I/Os, so they cannot float when disabled.

11.2 Layout Example

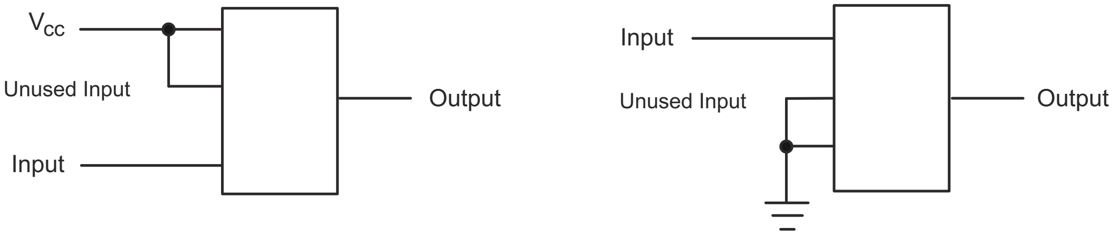


図 11-1. Layout Diagram

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application brief

12.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-86816012A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-86816012A SNJ54HC595FK	Samples
5962-8681601EA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8681601EA SNJ54HC595J	Samples
5962-8681601VEA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8681601VEA SNV54HC595J	Samples
5962-8681601VFA	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8681601VFA SNV54HC595W	Samples
SN54HC595J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54HC595J	Samples
SN74HC595DBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC595	Samples
SN74HC595DBRE4	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC595	Samples
SN74HC595DBRG4	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC595	Samples
SN74HC595DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	HC595	Samples
SN74HC595DRE4	ACTIVE				2500	TBD	Call TI	Call TI	-40 to 85		Samples
SN74HC595DRG3	ACTIVE	SOIC	D	16	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	HC595	Samples
SN74HC595DRG4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC595	Samples
SN74HC595DT	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 85	HC595	
SN74HC595DW	OBSOLETE	SOIC	DW	16		TBD	Call TI	Call TI	-40 to 85	HC595	
SN74HC595DWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC595	Samples
SN74HC595N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC595N	Samples
SN74HC595NE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC595N	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HC595NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC595	Samples
SN74HC595PW	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-40 to 85	HC595	
SN74HC595PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	HC595	Samples
SN74HC595PWRG4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC595	Samples
SNJ54HC595FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-86816012A SNJ54HC 595FK	Samples
SNJ54HC595J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8681601EA SNJ54HC595J	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54HC595, SN54HC595-SP, SN74HC595 :

- Catalog : SN74HC595, SN54HC595

- Enhanced Product : SN74HC595-EP, SN74HC595-EP

- Military : SN54HC595

- Space : SN54HC595-SP

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

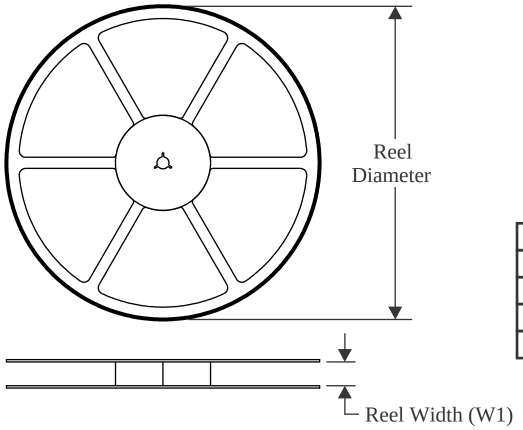
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

- Military - QML certified for Military and Defense Applications

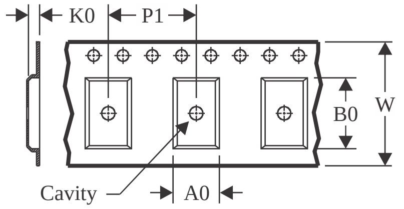
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

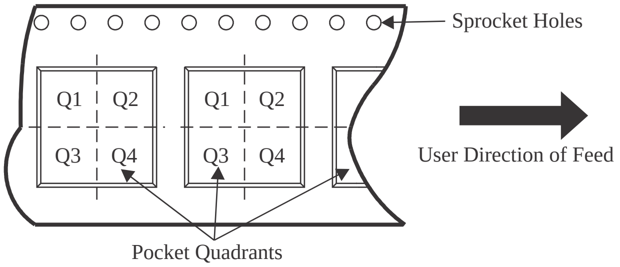


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

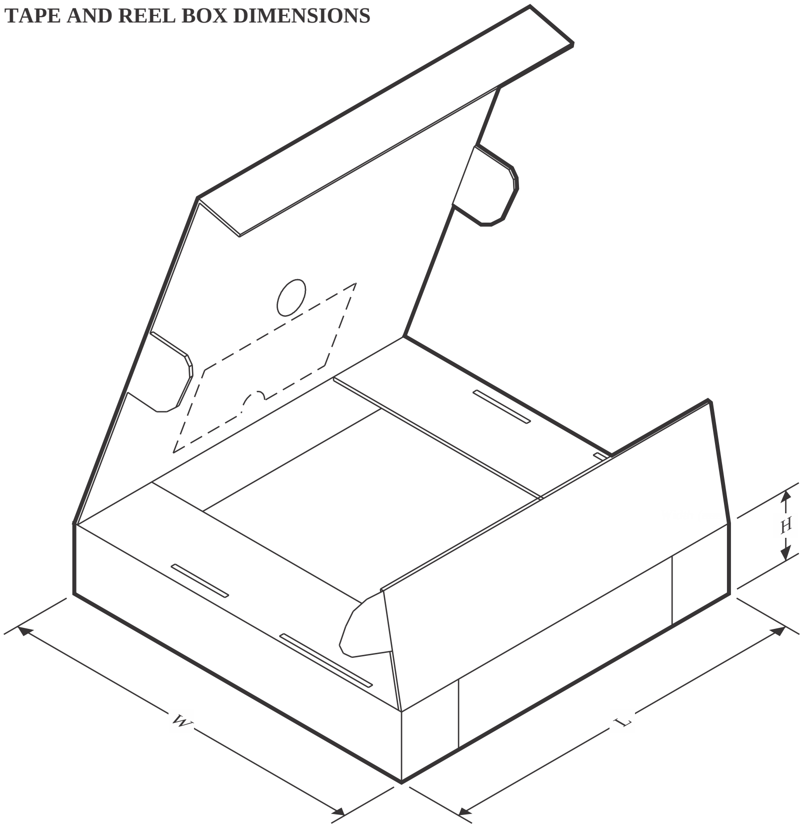
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC595DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74HC595DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC595DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC595DRG3	SOIC	D	16	2500	330.0	16.4	6.6	9.3	2.1	8.0	16.0	Q1
SN74HC595DRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC595DRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC595DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
SN74HC595NSR	SO	NS	16	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
SN74HC595NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74HC595PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC595PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC595PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC595PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

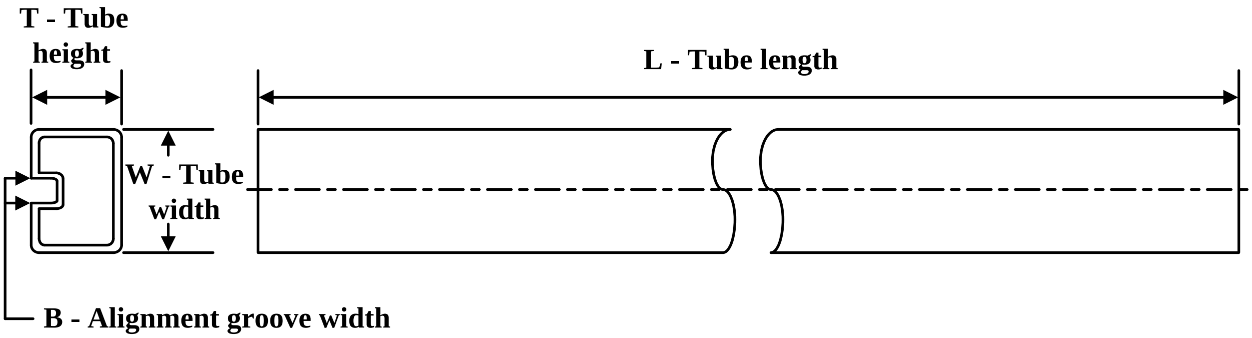
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC595DBR	SSOP	DB	16	2000	356.0	356.0	35.0
SN74HC595DR	SOIC	D	16	2500	356.0	356.0	35.0
SN74HC595DR	SOIC	D	16	2500	356.0	356.0	35.0
SN74HC595DRG3	SOIC	D	16	2500	366.0	364.0	50.0
SN74HC595DRG4	SOIC	D	16	2500	356.0	356.0	35.0
SN74HC595DRG4	SOIC	D	16	2500	356.0	356.0	35.0
SN74HC595DWR	SOIC	DW	16	2000	350.0	350.0	43.0
SN74HC595NSR	SO	NS	16	2000	356.0	356.0	35.0
SN74HC595NSR	SO	NS	16	2000	367.0	367.0	38.0
SN74HC595PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74HC595PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74HC595PWRG4	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74HC595PWRG4	TSSOP	PW	16	2000	356.0	356.0	35.0

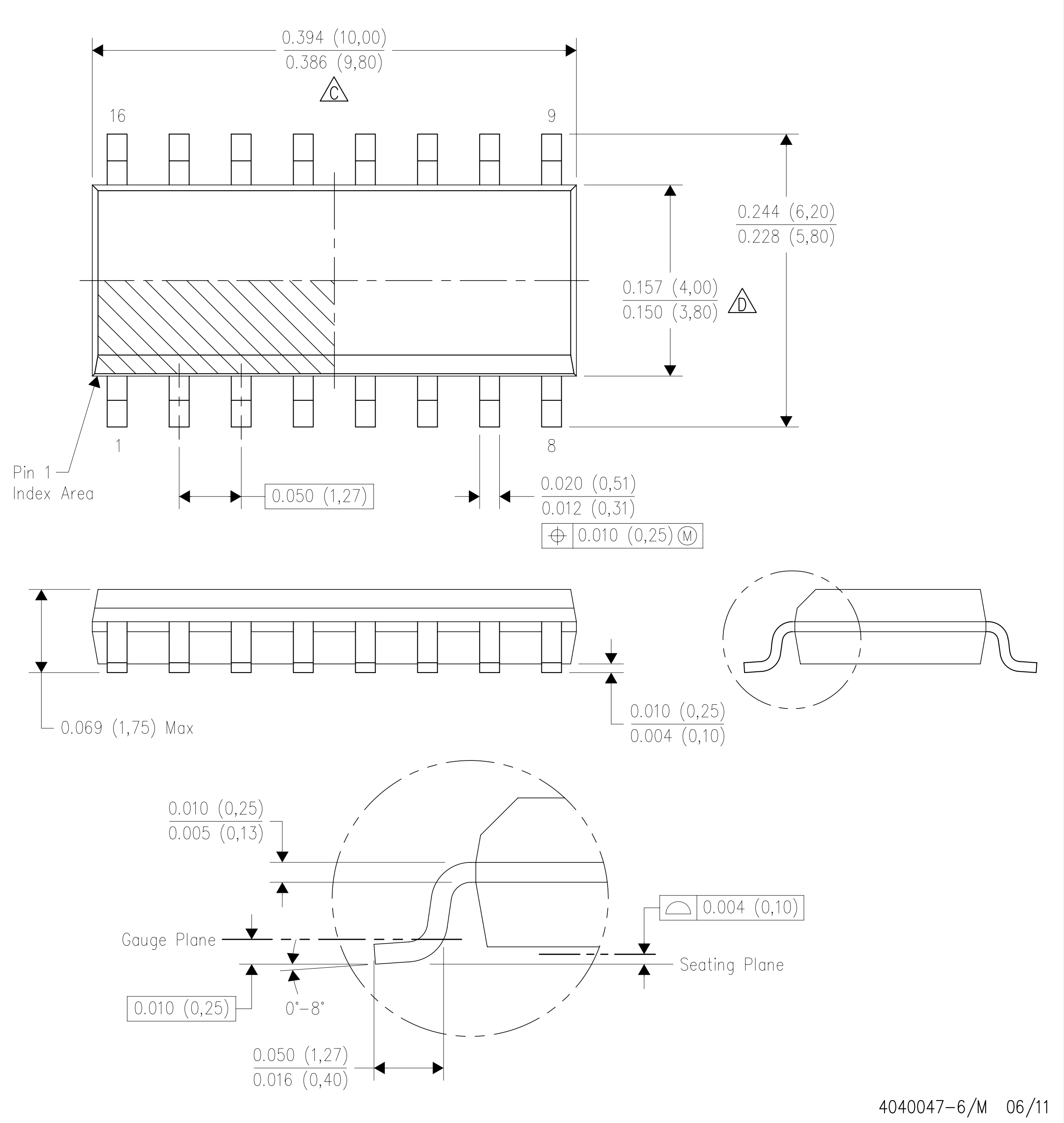
TUBE



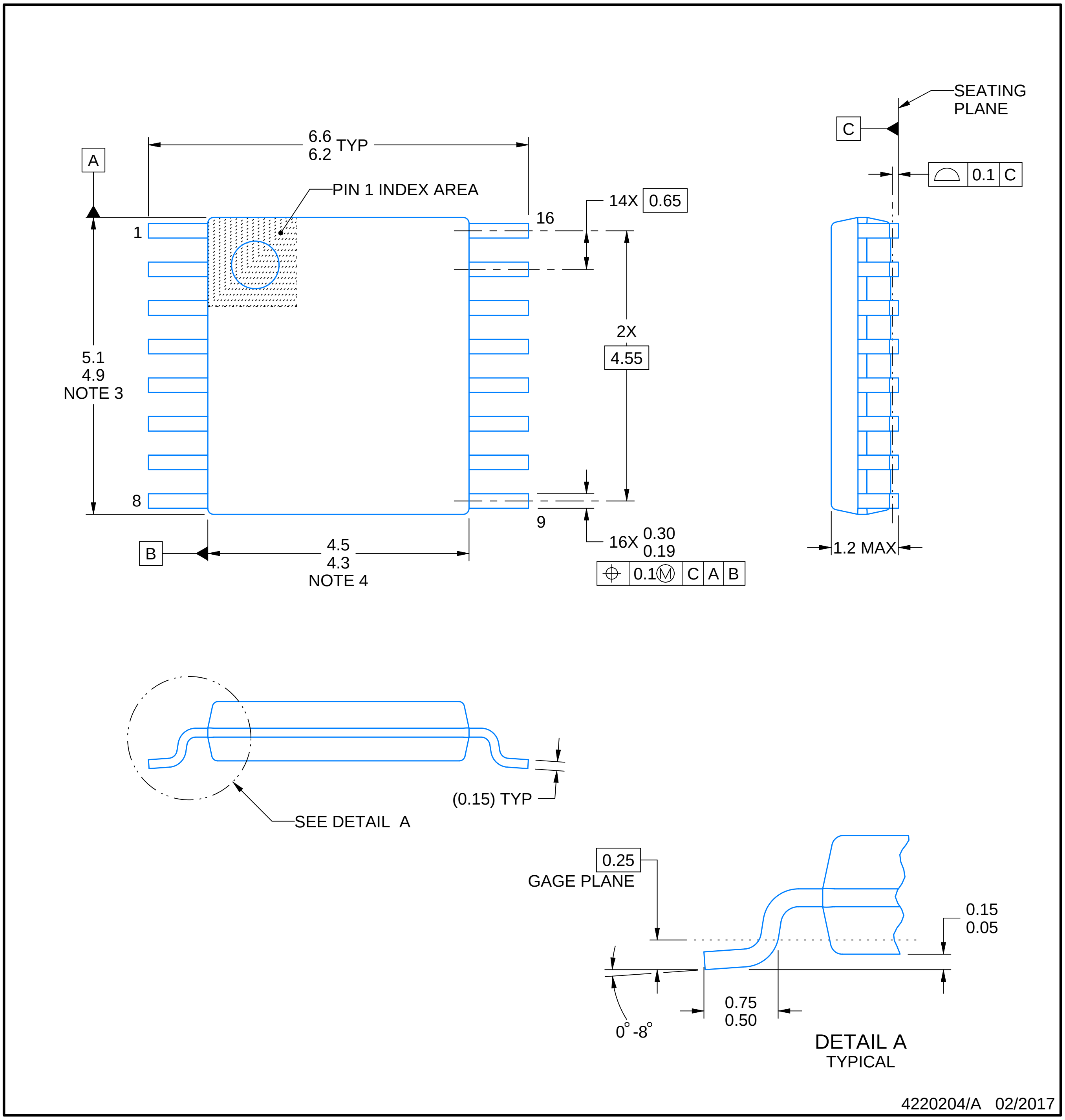
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-86816012A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-8681601EA	J	CDIP	16	25	506.98	15.24	13440	NA
5962-8681601VEA	J	CDIP	16	25	506.98	15.24	13440	NA
5962-8681601VFA	W	CFP	16	25	506.98	26.16	6220	NA
SN74HC595N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC595N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC595NE4	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC595NE4	N	PDIP	16	25	506	13.97	11230	4.32
SNJ54HC595FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54HC595J	J	CDIP	16	25	506.98	15.24	13440	NA

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



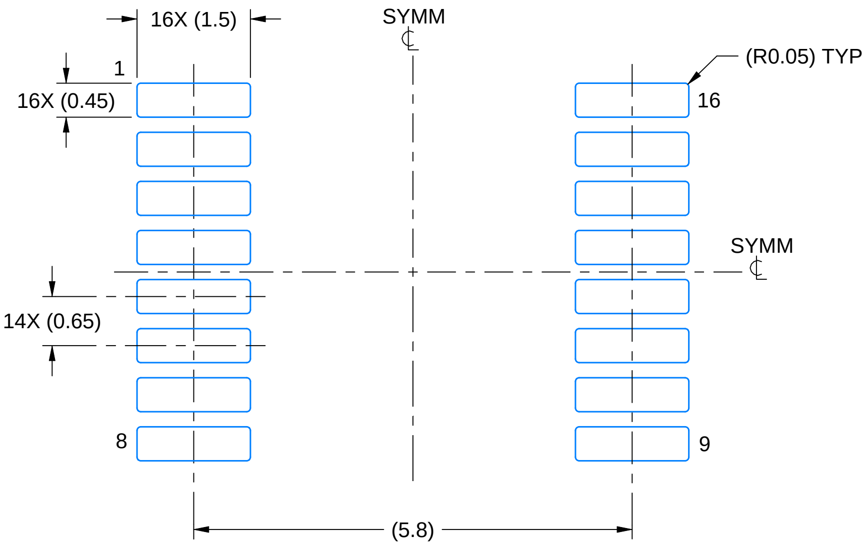
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AC.



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

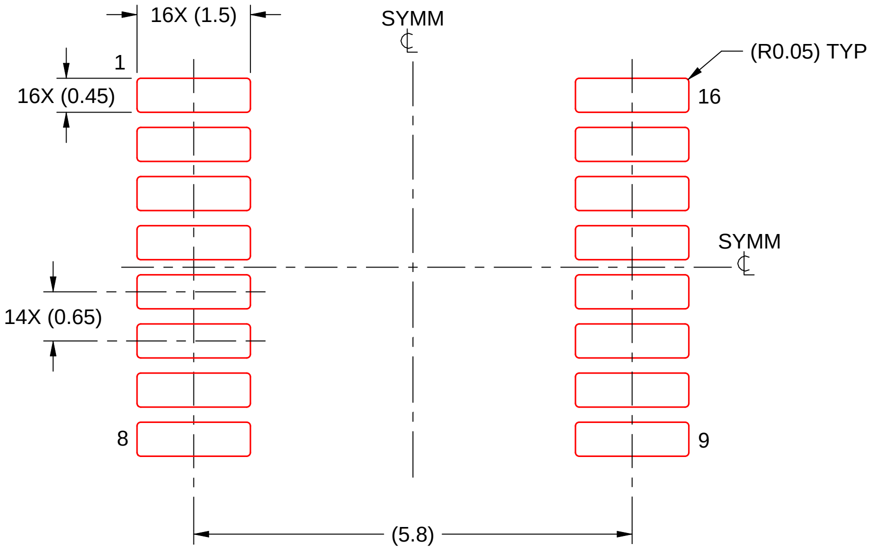
NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

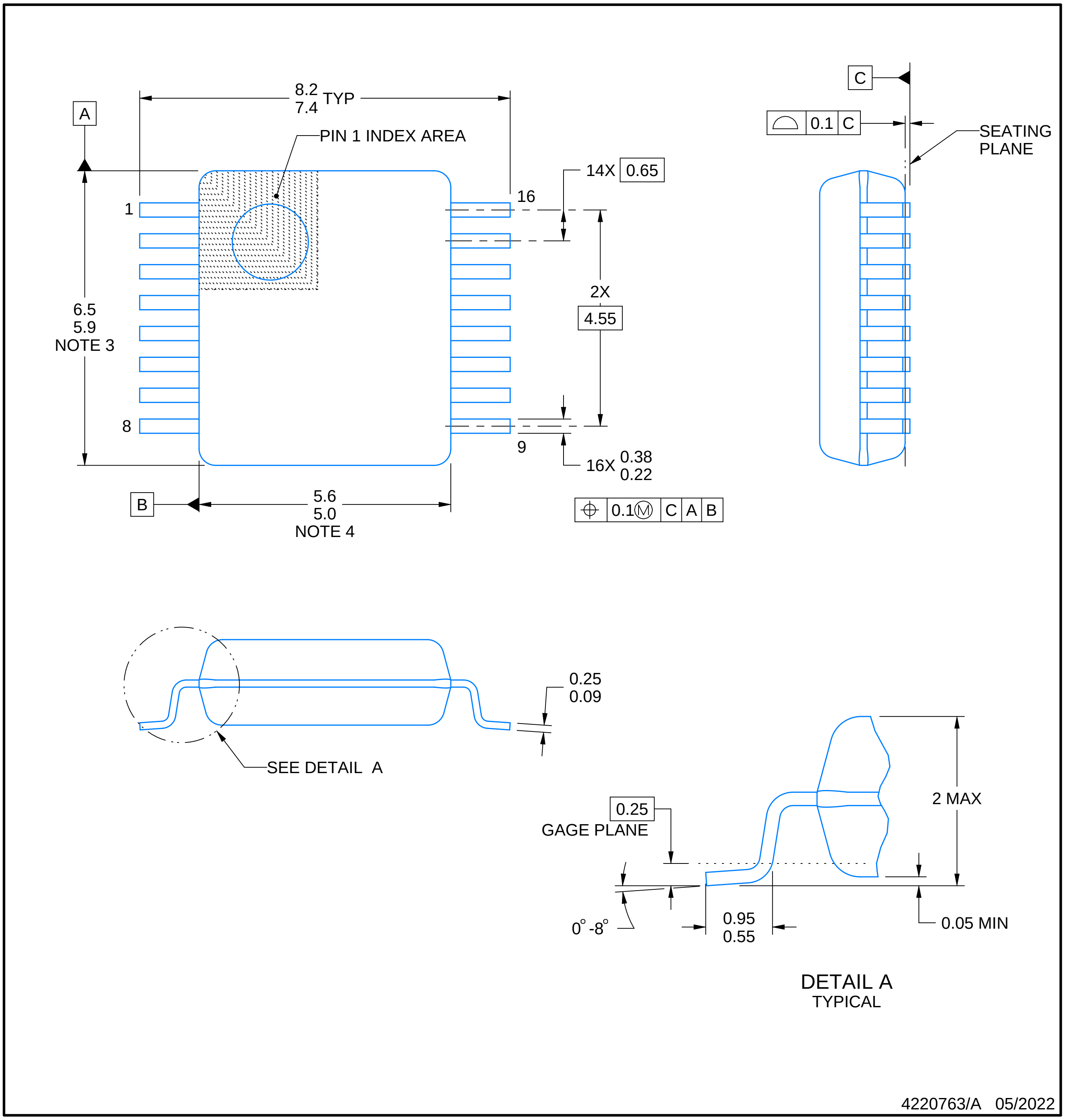


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

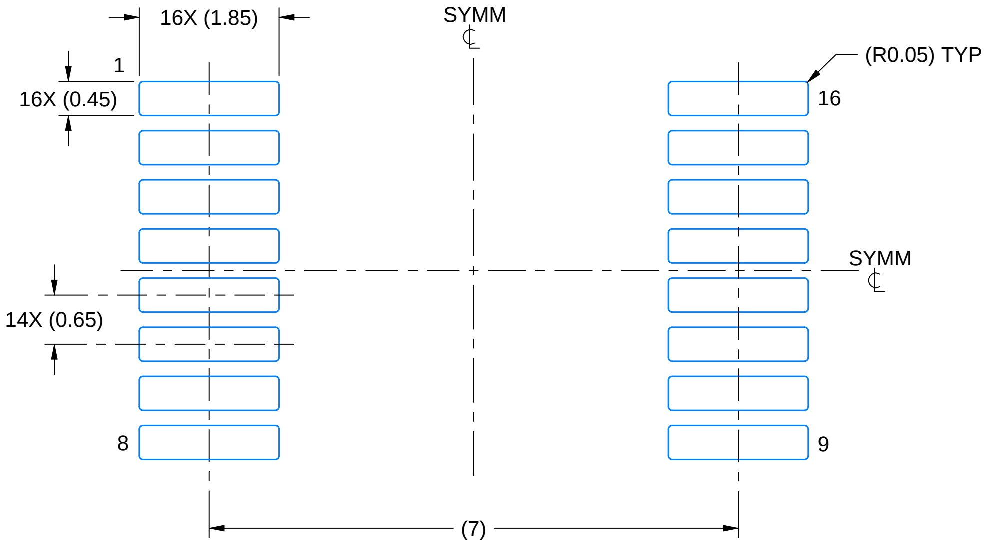
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



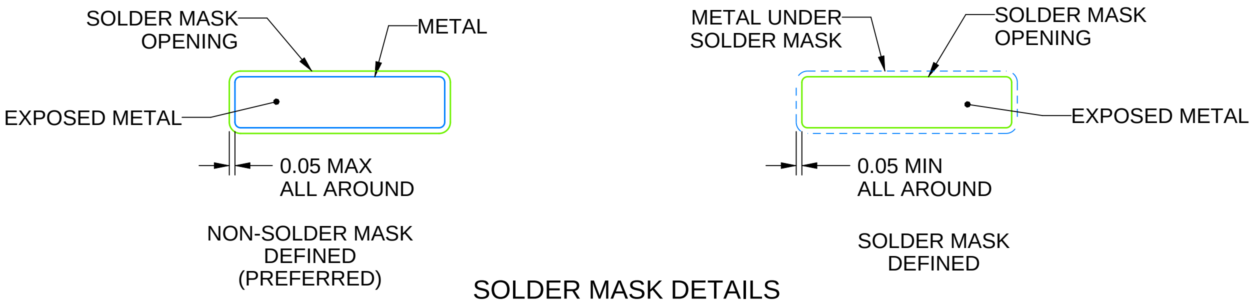
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

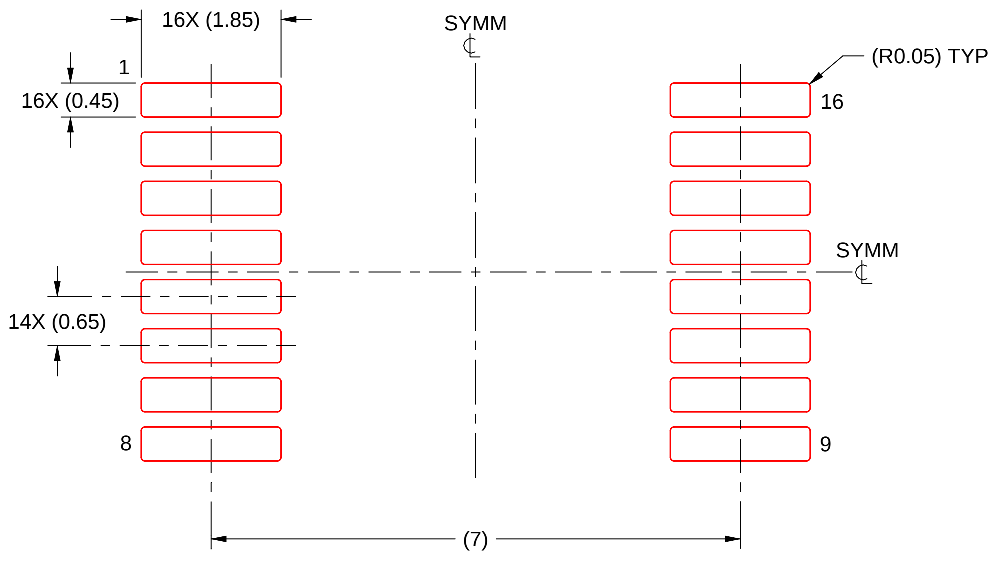


SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

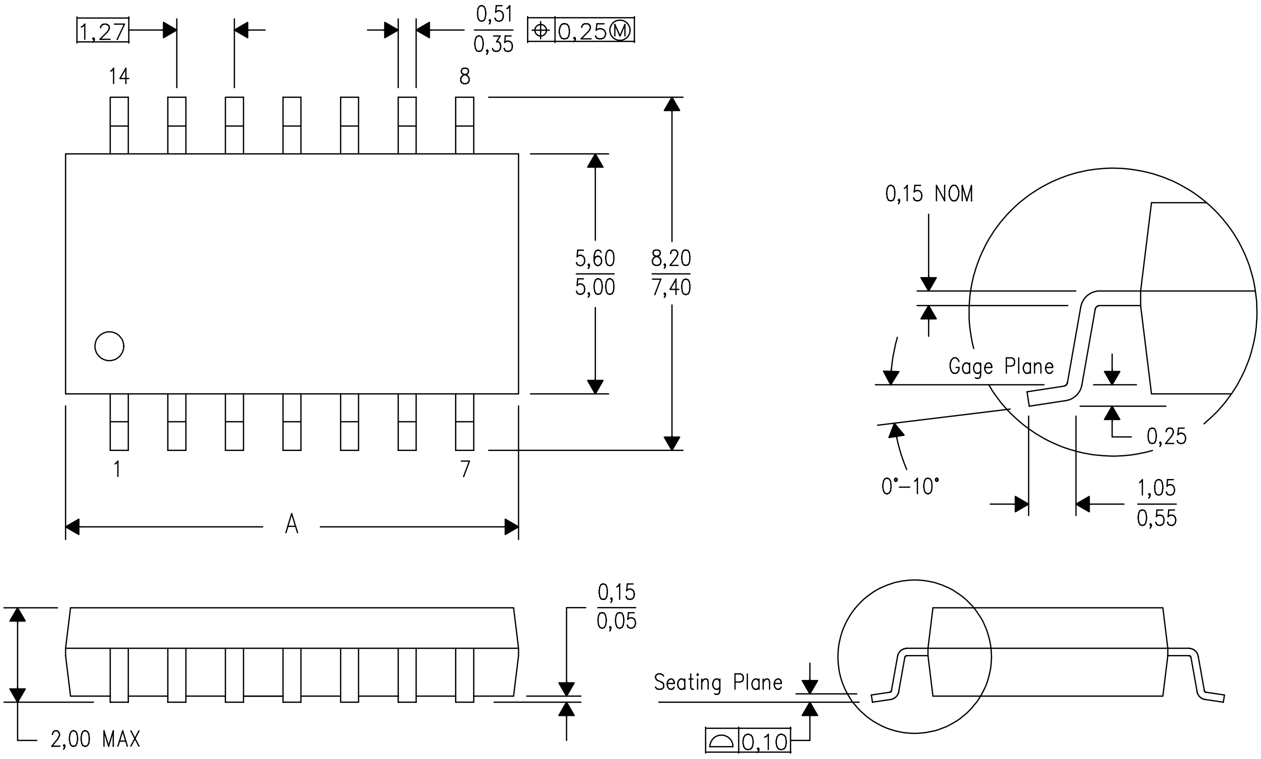
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

GENERIC PACKAGE VIEW

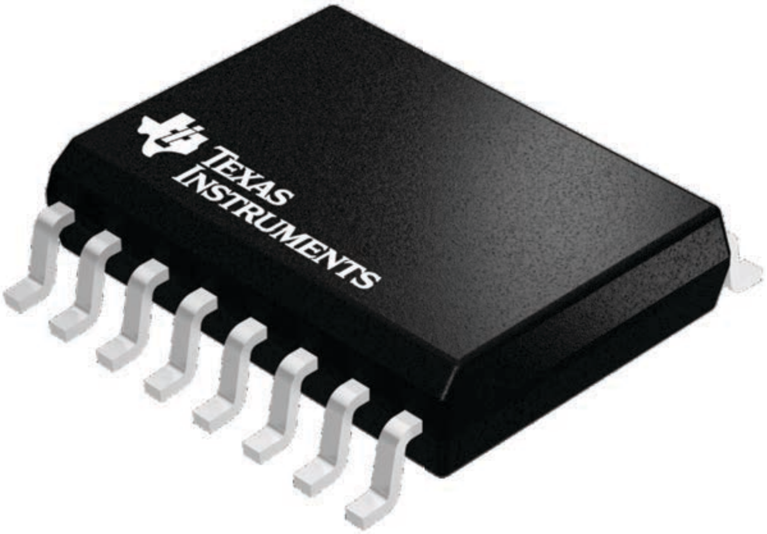
DW 16

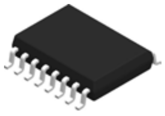
SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



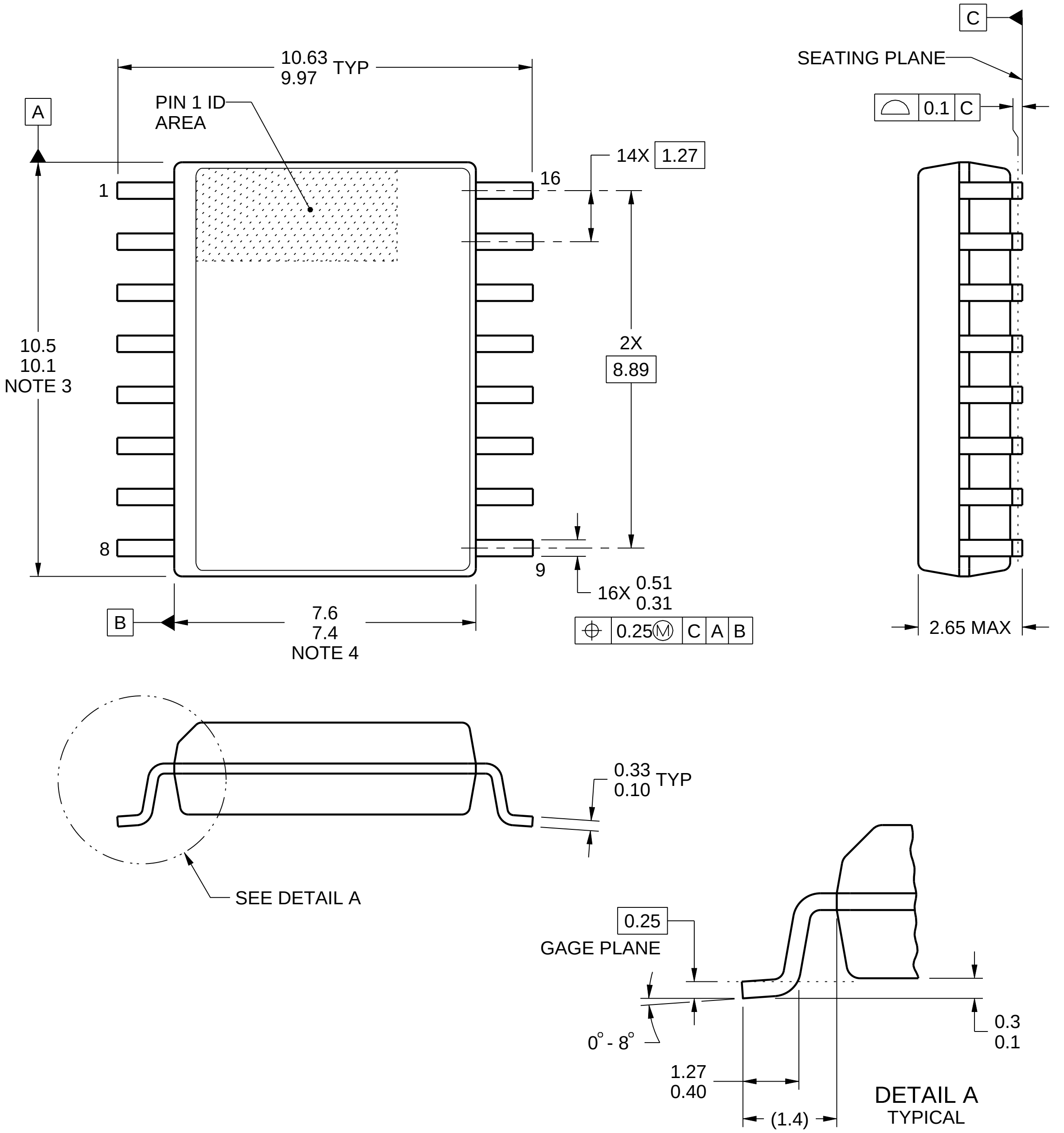


PACKAGE OUTLINE

DW0016A

SOIC - 2.65 mm max height

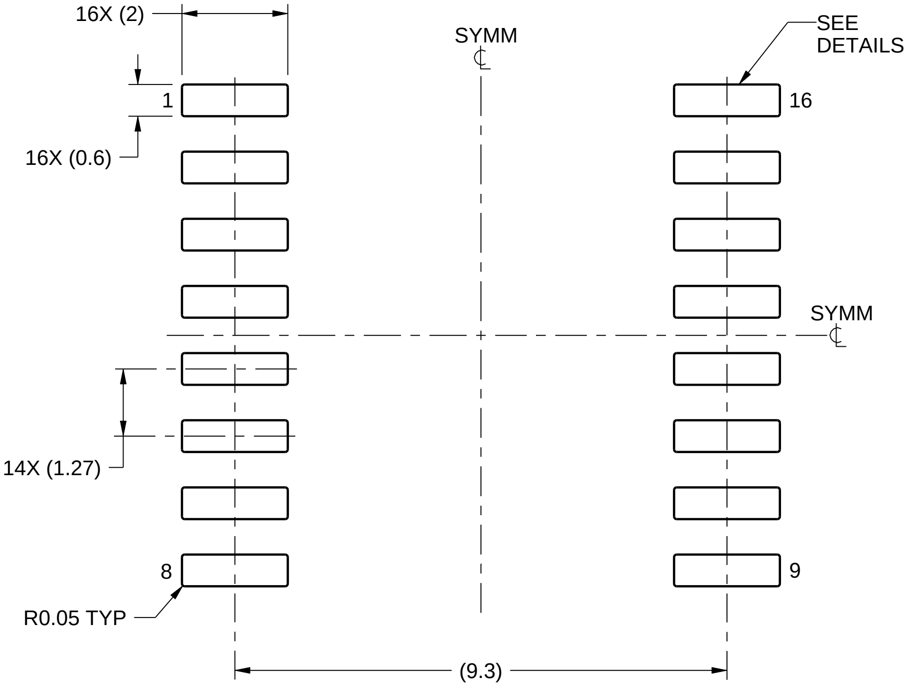
SOIC



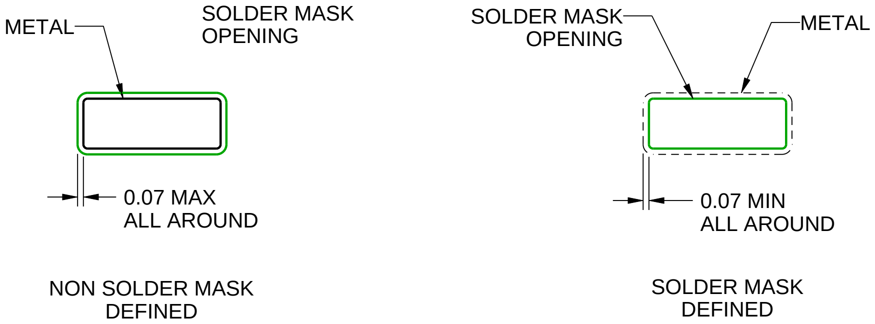
4220721/A 07/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

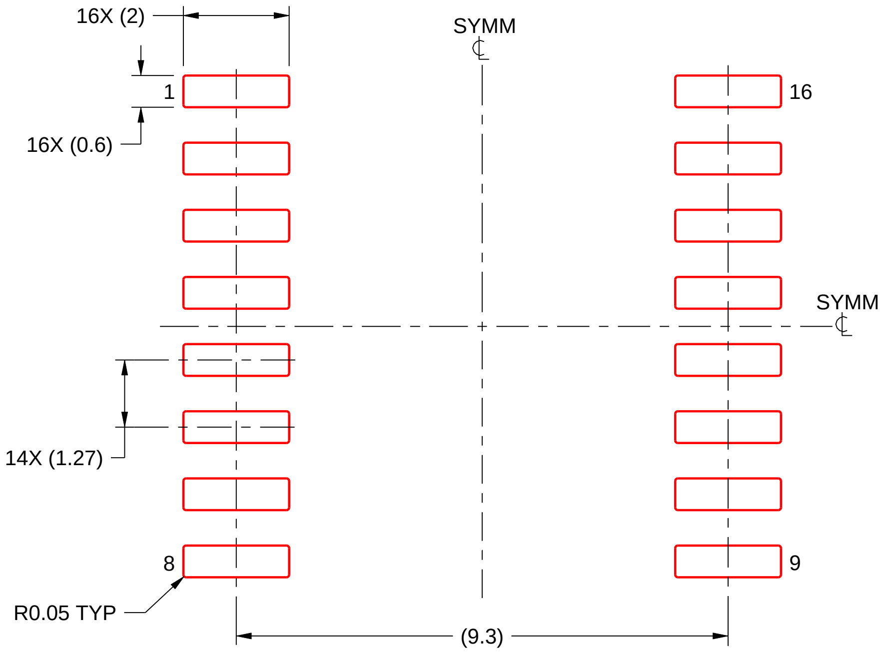


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



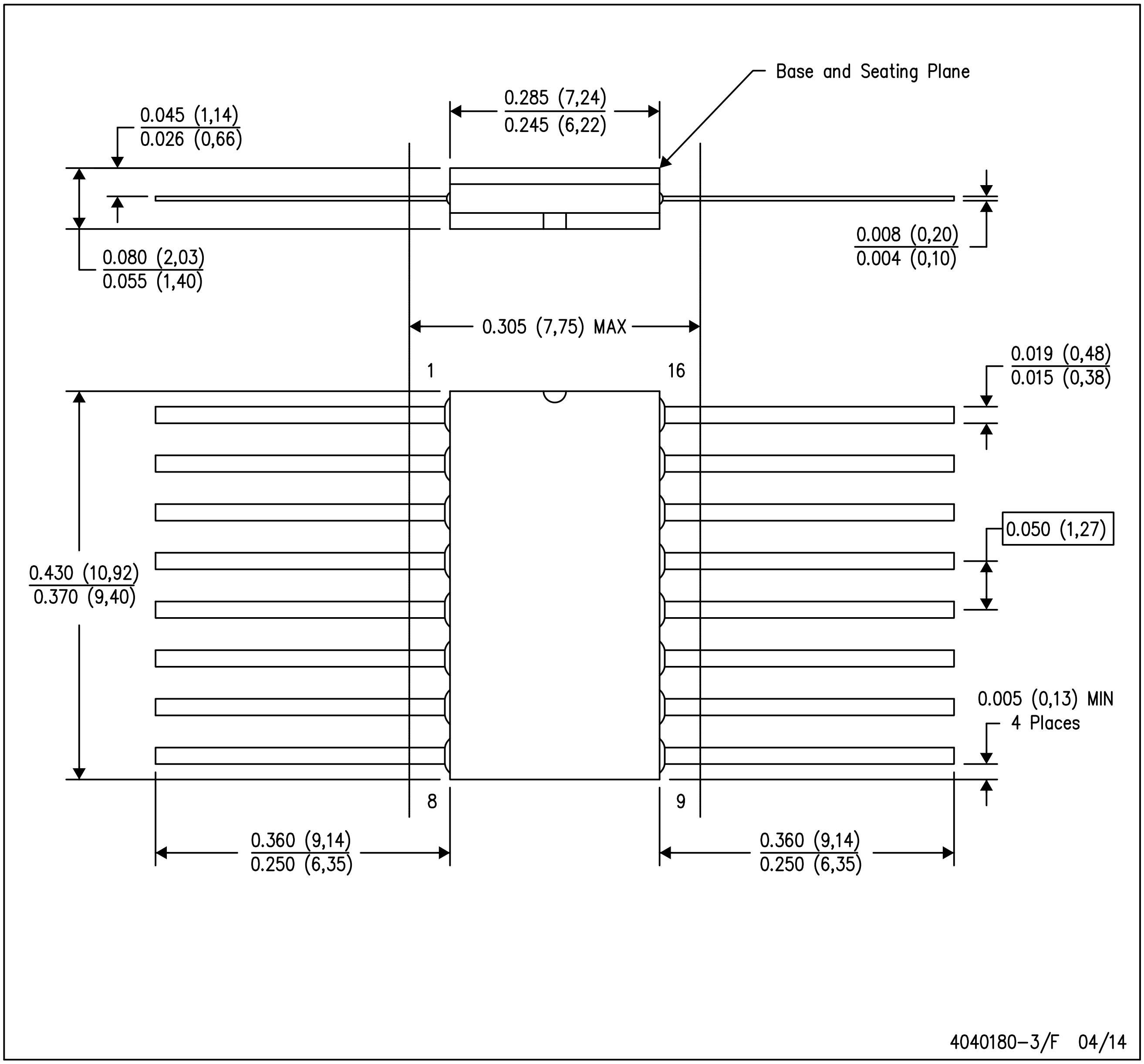
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R–GDFP–F16) CERAMIC DUAL FLATPACK



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP2–F16

GENERIC PACKAGE VIEW

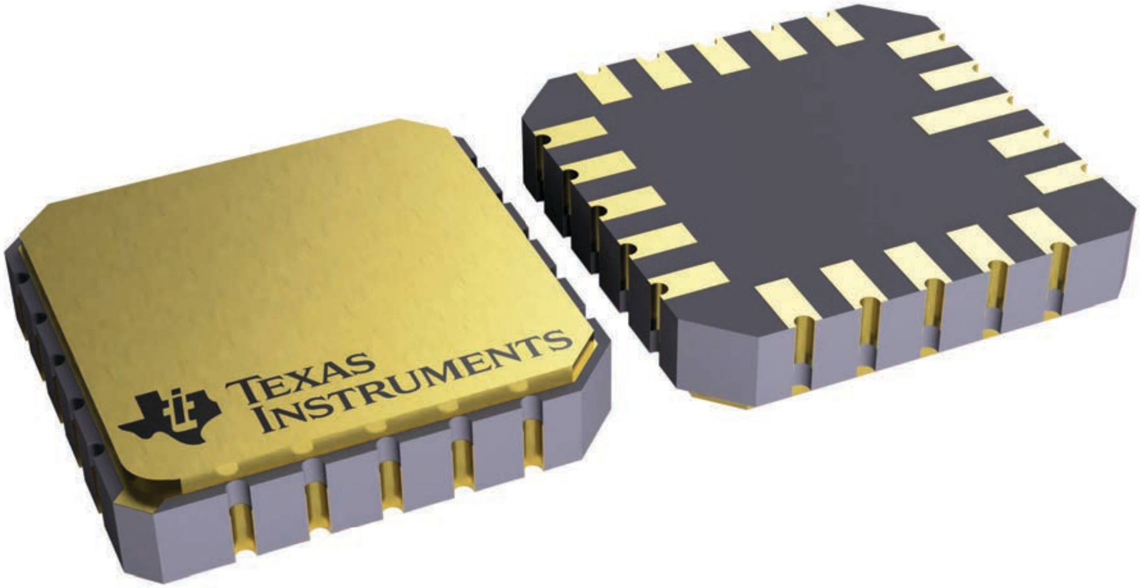
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

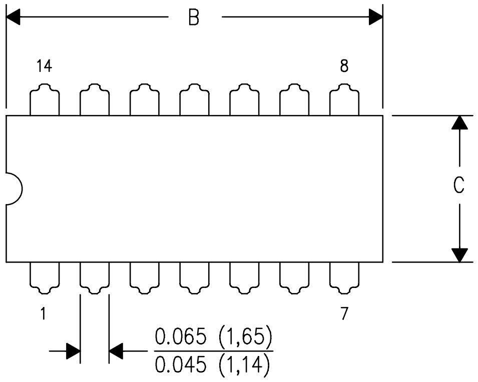
LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

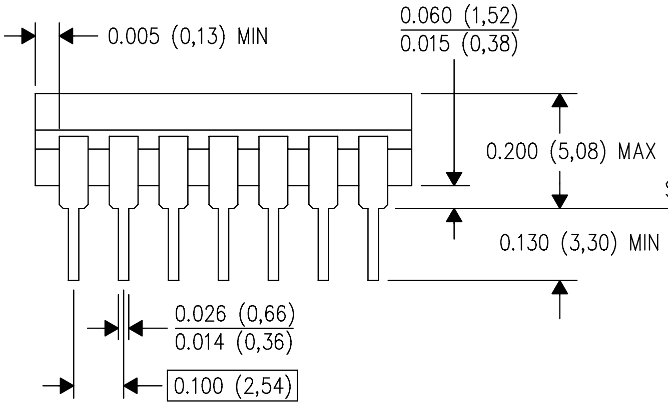


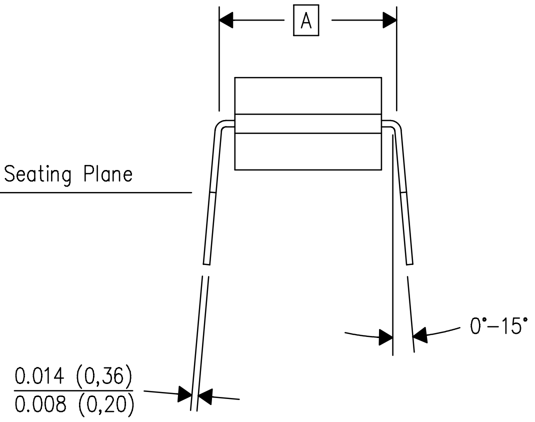
J (R–GDIP–T**) CERAMIC DUAL IN–LINE PACKAGE

14 LEADS SHOWN



PINS ** DIM	14	16	18	20
$\boxed{A}$	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



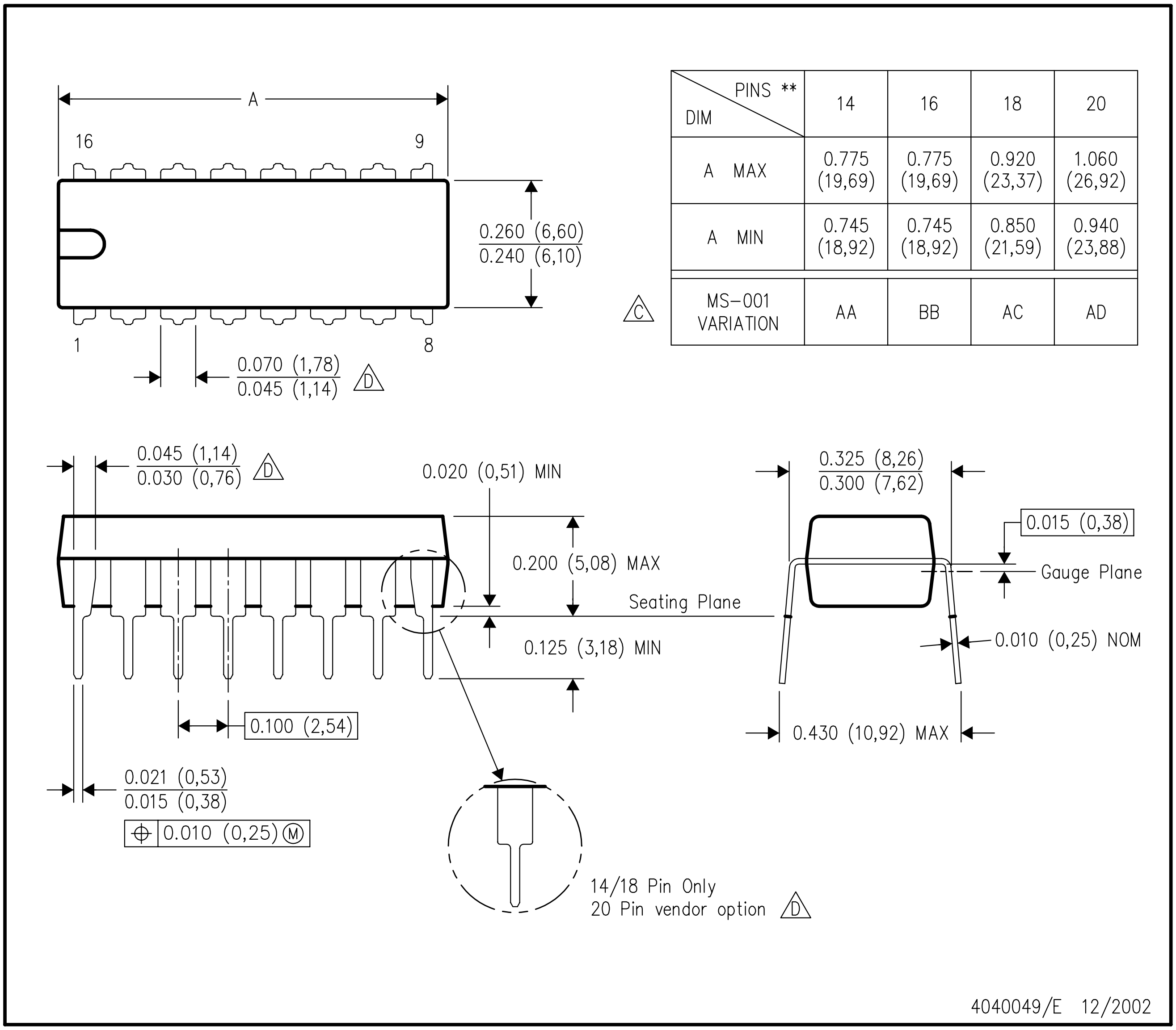


4040083/F 03/03

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

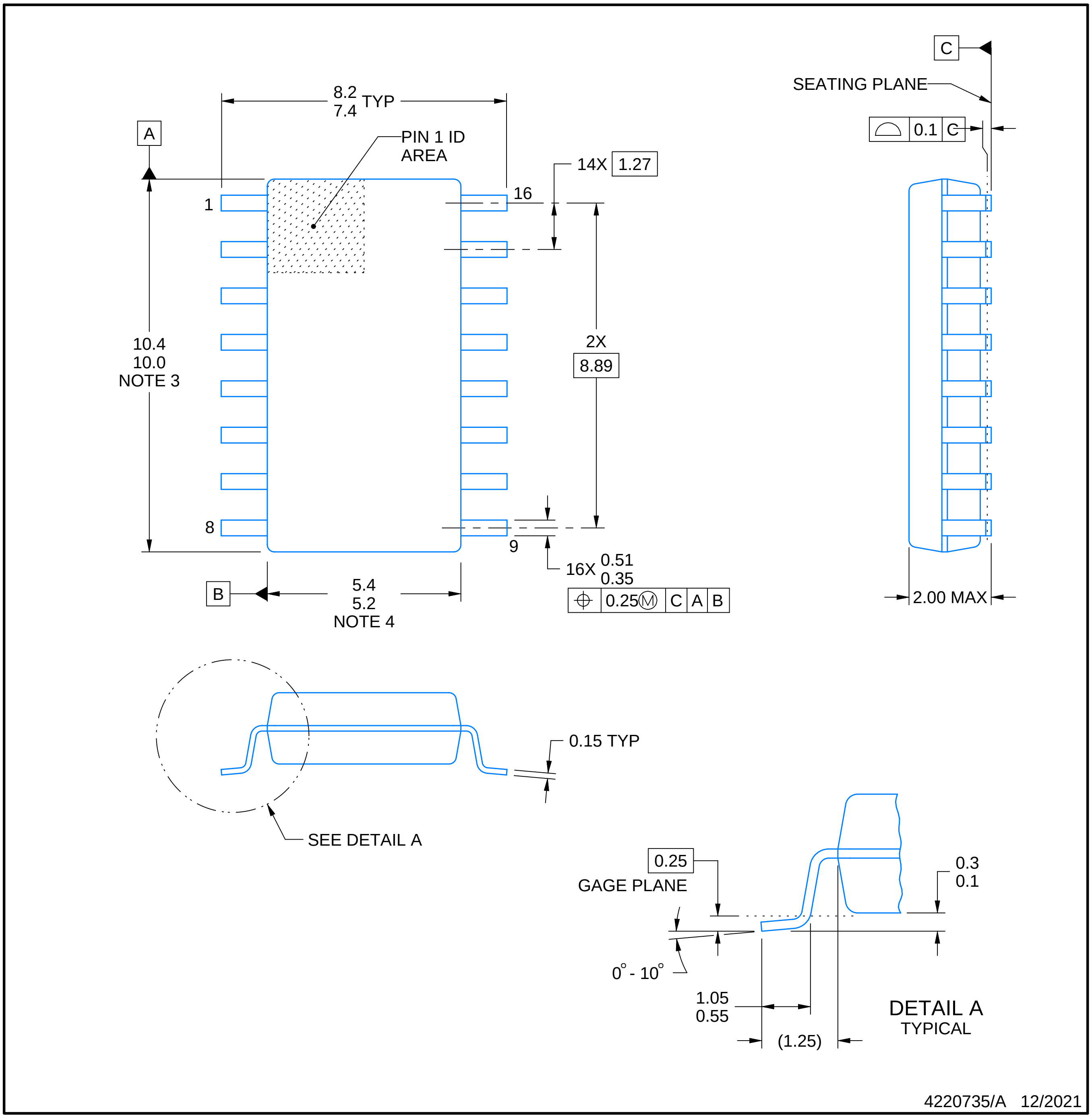
16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION	AA	BB	AC	AD

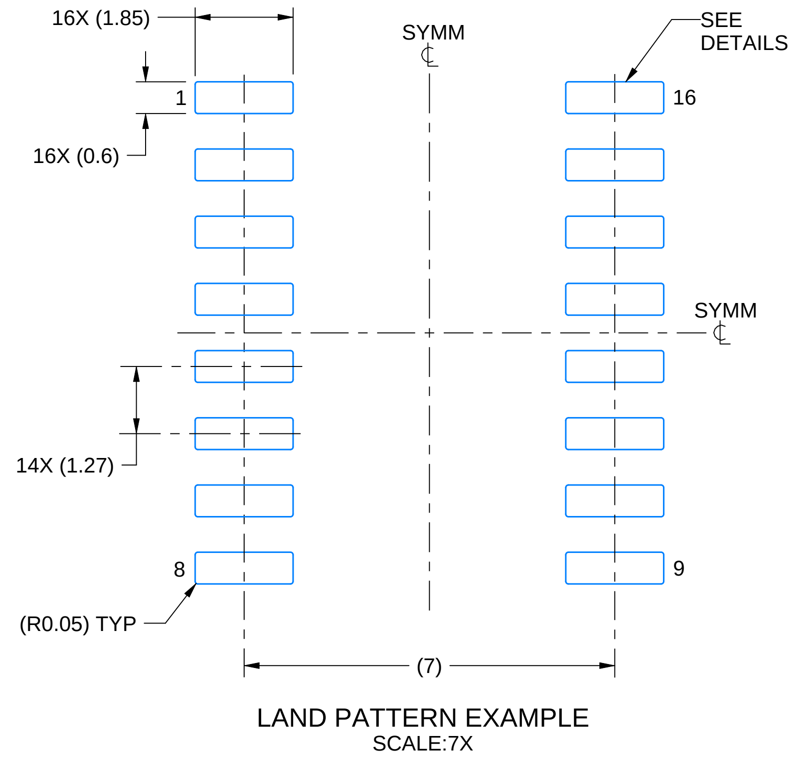
4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

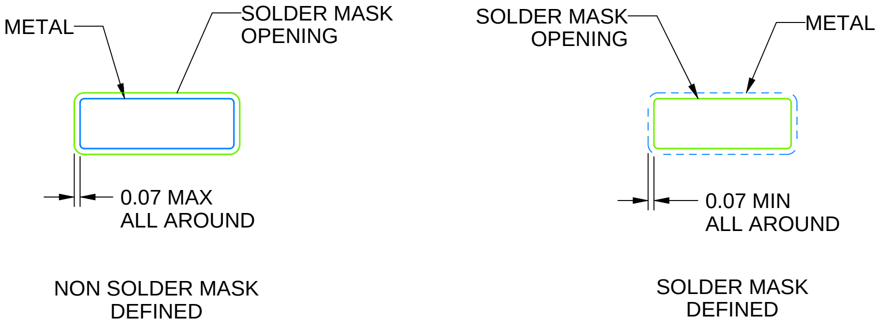


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X

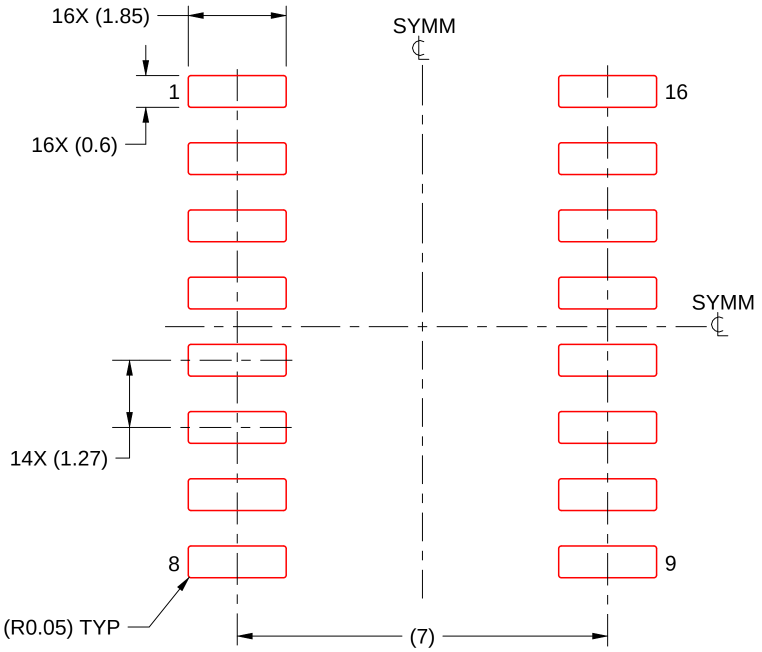


SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265