SNx5175 クワッド差動ライン・レシーバ

1 特長

- ANSI 規格 EIA/TIA-422-B、RS-423-B、および RS-485 の要件を満たす、または超える
- ITU 勧告 V.10、V.11、X.26、X.27 に適合
- ノイズの多い環境の、長いバス・ラインでのマルチポイント・バス伝送用に設計
- 3 ステート出力
- 同相入力電圧範囲:−12V～12V
- 入力感度:±200mV
- 入力ヒステリシス:50mV (標準値)
- 高い入力インピーダンス:12kΩ (最小値)
- 5V 単一電源で動作
- 低消費電力要件
- MC3486 のプラグイン代替品

2 アプリケーション

- モータ・ドライブ
- ファクトリ・オートメーション / 制御

3 概要

SN65175 および SN75175 は、3 ステート出力を搭載したモノリシック・クワッド差動ライン・レシーバです。これらのデバイスは、ANSI 規格 EIA/TIA-422-B、RS-423-B、RS-485 およびいくつかの ITU 勧告の要件を満たすように設計されています。これらの規格は、最大 10 Mbps の速度で平衡マルチポイント・バス伝送を実現するためのものです。レシーバの 2 ペアのそれぞれに、共通のアクティブ High イネーブルがあります。

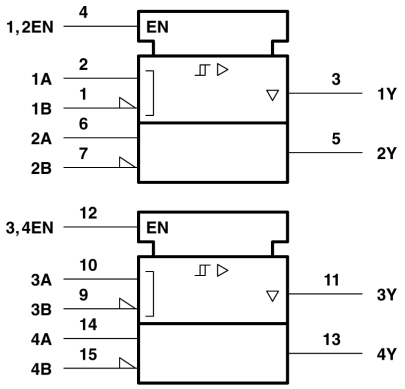
これらのレシーバは、高い入力インピーダンス、ノイズ耐性を高める入力ヒステリシス、±12V の同相入力電圧範囲にわたって ±200mV の入力感度を特長としています。SN65175 および SN75175 は、SN75172 または SN75174 クワッド差動ライン・ドライバと組み合わせて使用すると、最適な性能を発揮するよう設計されています。

SN65175 は -40℃～85℃での動作が規定されています。SN75175 は 0℃～70℃での動作が規定されています。

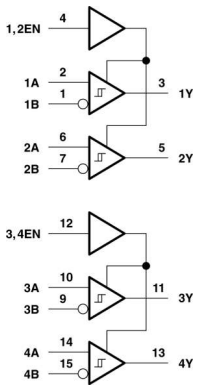
パッケージ情報

部品番号	パッケージ (1)	パッケージ・サイズ (2)
SN65175	D (SOIC、16)	9.9mm × 6mm
SN75175	N (PDIP、16)	19.3mm × 9.4mm
	D (SOIC、16)	9.9mm × 6mm
	NS (SOP、16)	10.2mm × 7.8mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ・サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



論理記号 [1]



論理図 (正論理)

[1] この記号は ANSI/IEEE 規格 91-1984 と IEC Publication 617-12 に準拠しています。

Table of Contents

4 Pin Configuration and Functions

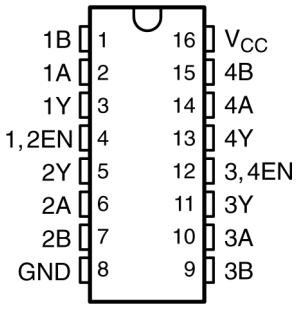


図 4-1. D, N, or NS Package (Top View)

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1B	1	I	Channel 1 Differential Receiver Inverting Input
1A	2	I	Channel 1 Differential Receiver Non-Inverting Input
1Y	3	O	Channel 1 Single Ended Output
1,2EN	4	I	Active High Enable for Channels 1 and 2
2Y	5	O	Channel 2 Single Ended Output
2A	6	I	Channel 2 Differential Receiver Non-Inverting Input
2B	7	I	Channel 2 Differential Receiver Inverting Input
GND	8	GND	Device GND
3B	9	I	Channel 3 Differential Receiver Inverting Input
3A	10	I	Channel 3 Differential Receiver Non-Inverting Input
3Y	11	O	Channel 3 Single Ended Output
3,4EN	12	I	Active High Enable for Channels 3 and 4
4Y	13	O	Channel 4 Single Ended Output
4A	14	I	Channel 4 Differential Receiver Non-Inverting Input
4B	15	I	Channel 4 Differential Receiver Inverting Input
V_{CC}	16	PWR	Device V_{CC} (4.75 V to 5.25 V)

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIX	MAX	UNIT
V_{CC} (2)	Supply voltage			7	V
V_I	Input voltage (A or B inputs)			±25	V
V_{ID} (3)	Differential input voltage			±25	V
$V_{I(EN)}$	Enable input voltage			7	V
I_{OL}	Low-level output current			50	mA
	Continuous total dissipation		See *Dissipation Rating* table		
T_A	Operating free-air temperature range:	SN65175	−40	85	°C
		SN75175	0	70	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			260	°C
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential input voltage, are with respect to network ground terminal.
(3) Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.

5.2 Dissipation Rating

PACKAGE	T_A ≤ 25°C POWER RATING	DERATING FACTOR	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

5.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Common-mode input voltage, V_{IC}				±12	V
Differential input voltage, V_{ID}				±12	V
High-level enable-input voltage, V_{IH}		2			V
Low-level enable-input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}				−400	µA
Low-level output current, I_{OL}				16	mA
Operating free-air temperature, T_A	SN65175	−40		85	°C
	SN75175	0		70	

5.4 Thermal Information

THERMAL METRIC[1]		D (SOIC)	N (PDIP)	NS (SOP)	UNIT
		16-PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.6	60.6	88.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.5	48.1	46.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.2	40.6	50.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.4	27.5	13.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.8	40.3	50.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.5 Electrical Characteristics

over recommended ranges of common-mode input voltage, supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS			MIN	TYP[1]	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_O = 2.7 V,	I_O = –0.4 mA				0.2	V
V_{IT-}	Negative-going input threshold voltage	V_O = 0.5 V,	I_O = 16 mA		–0.2[2]			V
V_{hys}	Hysteresis voltage (V_{IT+} - V_{IT-})	See 図 5-1				50		mV
V_{IK}	Enable-input clamp voltage	I_I = –18 mA					-1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV,	I_{OH} = –400 µA,	See 図 6-1	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = –200 mV,	See 図 6-1	I_{OL} = 8 mA			0.45	V
				I_{OL} = 16 mA			0.5	
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V					±20	µA
I_I	Line input current	Other input at 0 V,	See [4]	V_I = 12 V			1	mA
				V_I = –7 V			-0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V					20	µA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V					-100	µA
r_i	Input resistance				12			kΩ
I_{OS}	Short-circuit output current[3]				-15		-85	mA
I_{CC}	Supply current	Outputs disabled					70	mA

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(2) The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold voltage levels only.
(3) Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
(4) Refer to ANSI Standards EIA/TIA-422-B, RS-423-B, and RS-485 for exact conditions.

5.6 Switching Characteristics

V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	See 図 6-2		22	35	ns
t_{PHL}	Propagation delay time, high- to low-level output			25	35	ns
t_{PZH}	Output enable time to high level	See 図 6-3		13	30	ns
t_{PZL}	Output enable time to low level			19	30	ns
t_{PHZ}	Output disable time from high level	See 図 6-3		26	35	ns
t_{PLZ}	Output disable time from low level			25	35	ns

5.7 Typical Characteristics

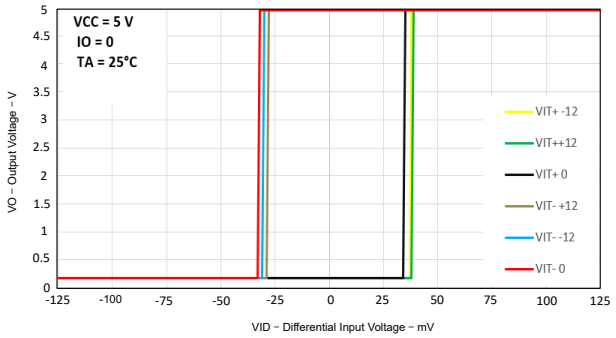


図 5-1. Output Voltage vs Differential Input Voltage

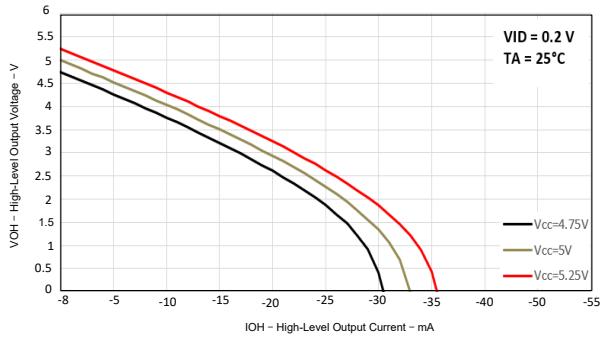


図 5-2. High-level Output Voltage vs High-level Output Current

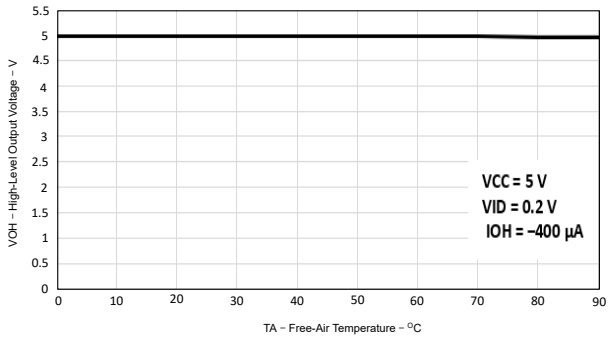


図 5-3. High-level Output Voltage vs Free-air Temperature 5

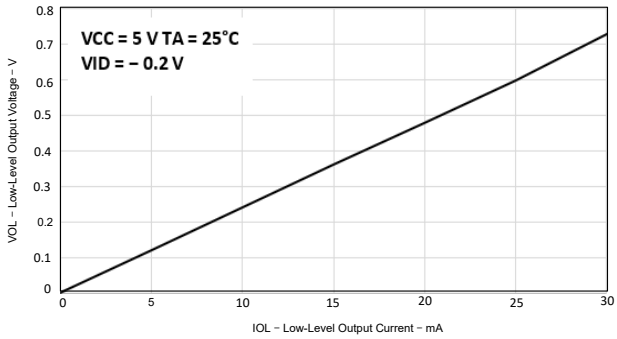


図 5-4. Low-level Output Voltage vs Low-level Output Current

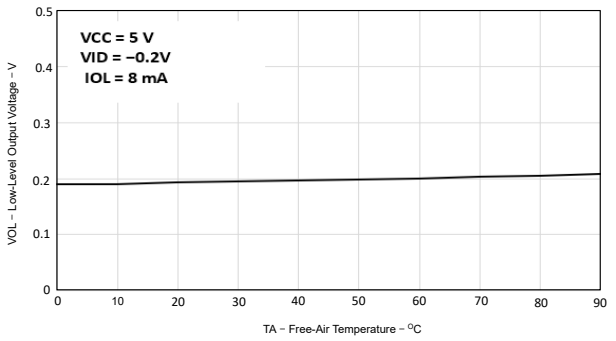


図 5-5. Low-level Output Voltage vs Free-air Temperature

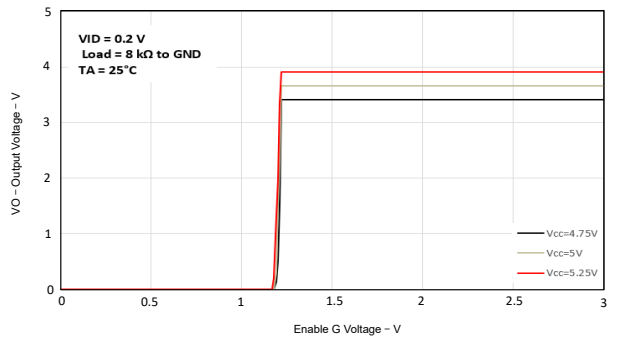


図 5-6. Output Voltage vs Enable G Voltage

5.7 Typical Characteristics (continued)

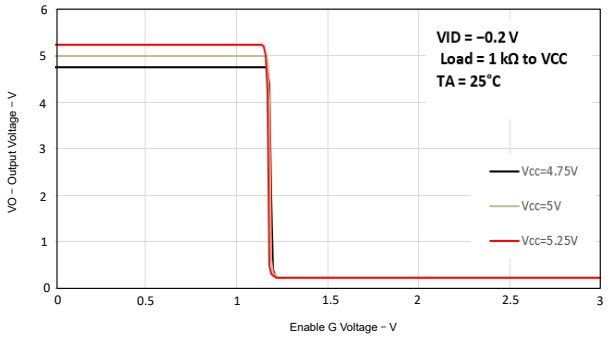


図 5-7. Output Voltage vs Enable G Voltage

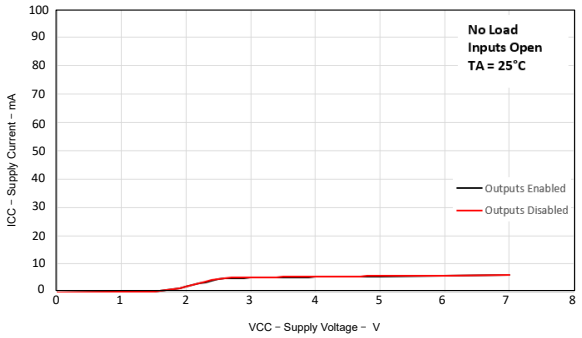


図 5-8. Supply Current (All Receivers) vs Supply Voltage

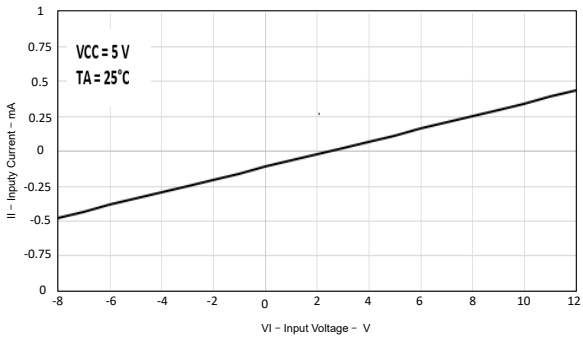


図 5-9. Input Current vs Input Voltage

6 Parameter Measurement Information

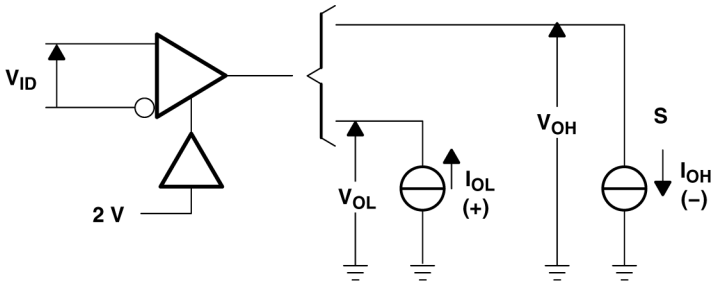
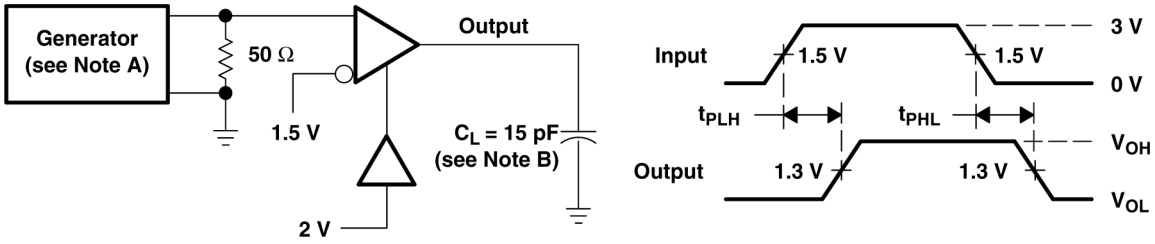


図 6-1. V_{OH}, V_{OL}

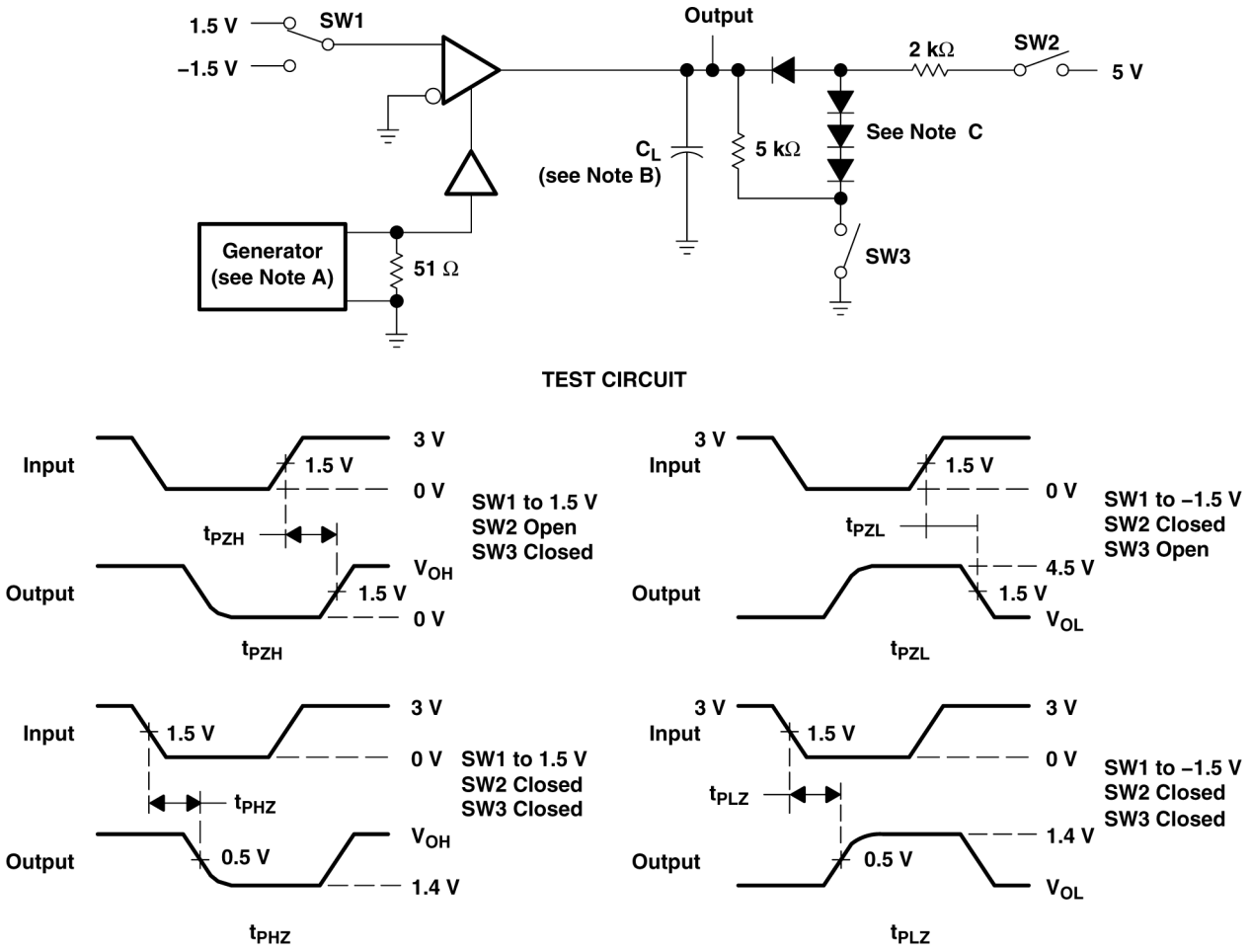


TEST CIRCUIT VOLTAGE WAVEFORMS

A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes probe and stray capacitance.

図 6-2. Test Circuit and Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_f ≤ 6 ns, t_r ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes probe and stray capacitance.

C. All diodes are 1N916 or equivalent.

図 6-3. Test Circuit and Voltage Waveforms

7 Detailed Description

7.1 Device Functional Modes

表 7-1. Function Table (Each Receiver)

DIFFERENTIAL A − B[(1)]	ENABLE	OUTPUT Y
$V_{ID} \geq 0.2$ V	H	H
−0.2 V < V_{ID} < 0.2 V	H	?
$V_{ID} \leq -0.2$ V	H	L
X	L	Z
Open circuit	H	?

(1) H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

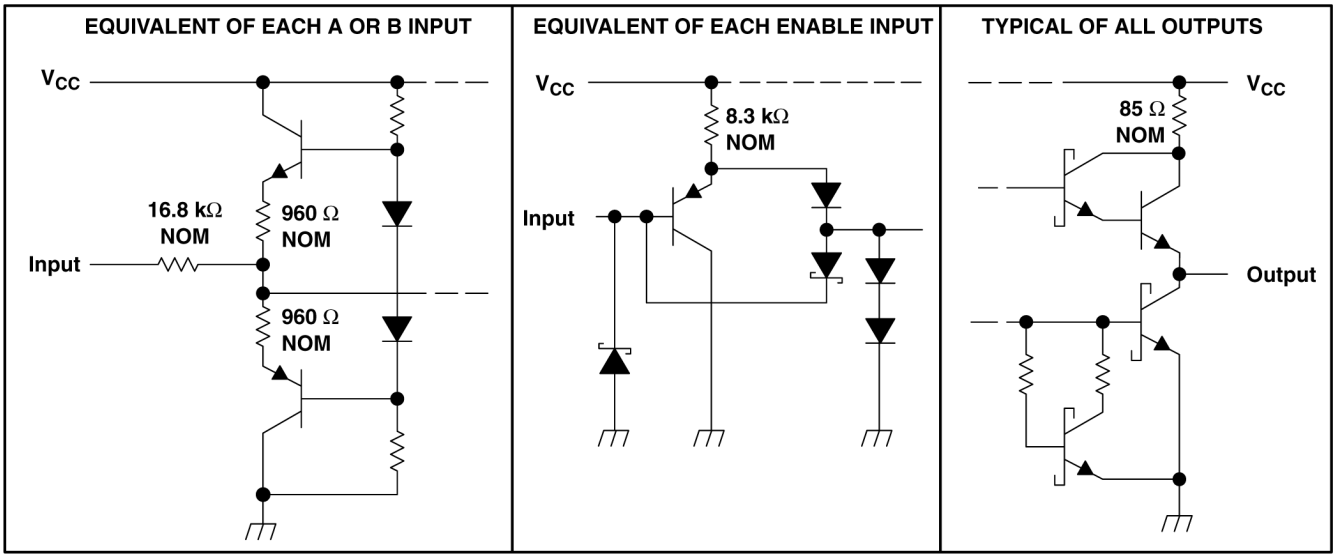


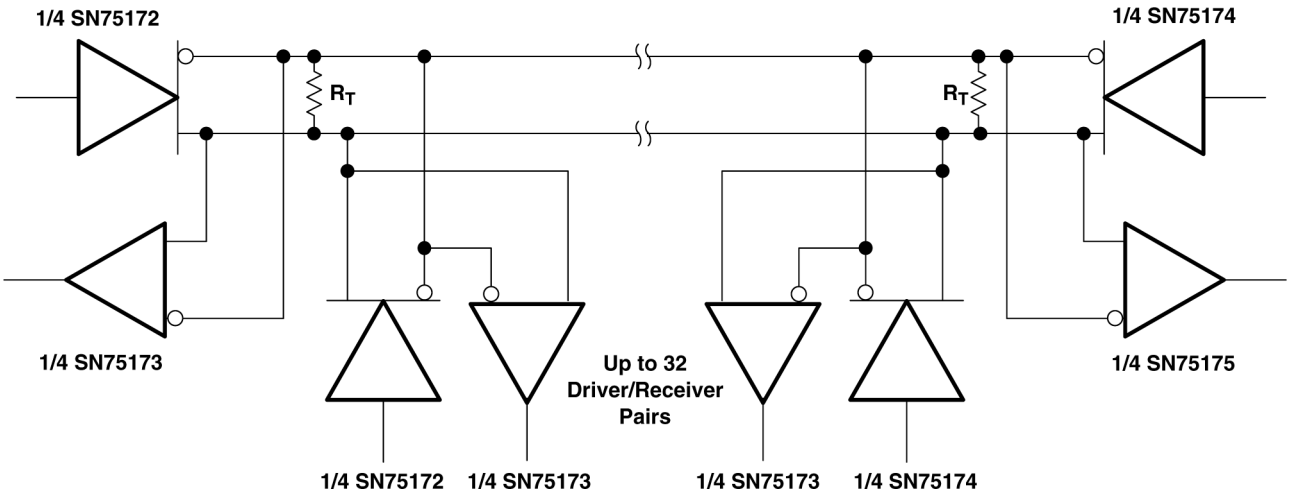
図 7-1. Schematics of Inputs and Outputs

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information



A. The line should be terminated at both ends in its characteristicc impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

図 8-1. Typical Application Circuit

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

9.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

9.4 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (November 2006) to Revision D (October 2023)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を変更	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65175D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SN65175	Samples
SN65175DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SN65175	Samples
SN75175D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	0 to 70	SN75175	
SN75175DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75175	Samples
SN75175N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75175N	Samples
SN75175NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75175	Samples
SN75175NSRG4	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75175	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

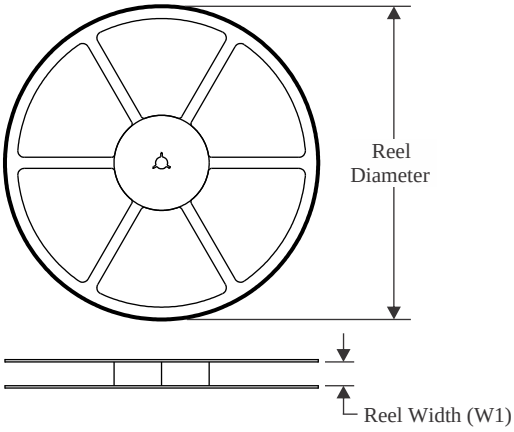
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

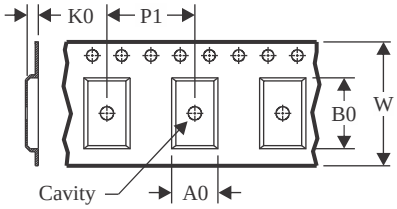
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

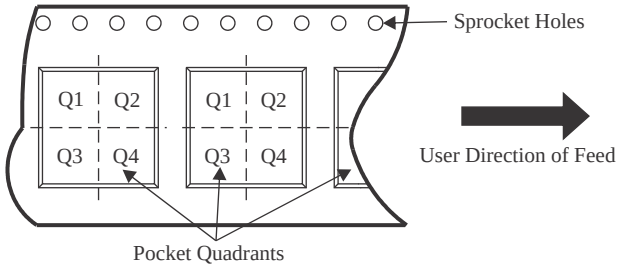


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

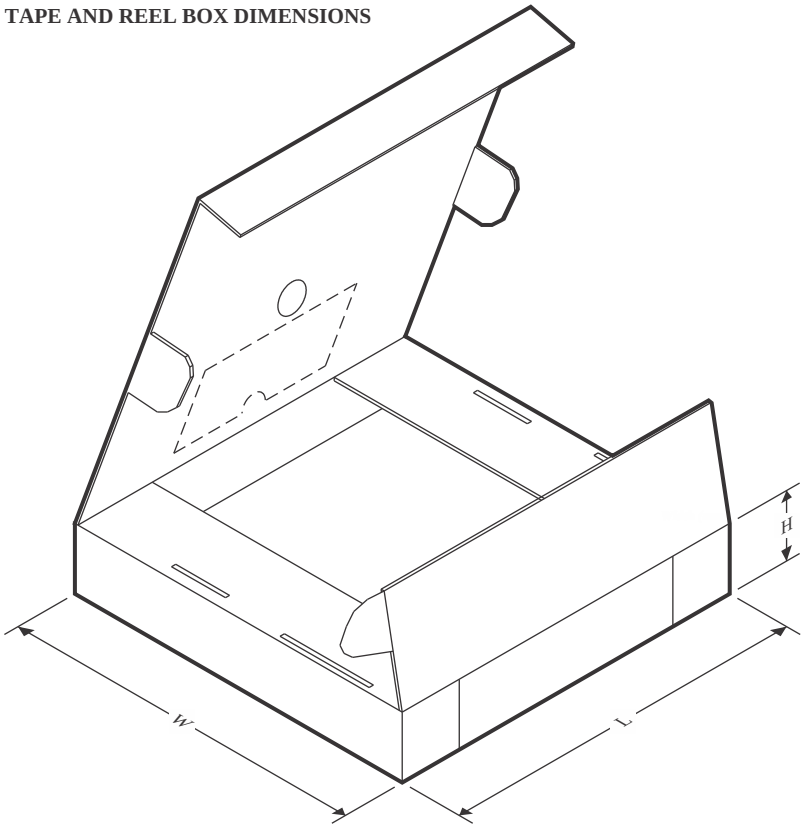
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65175DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN75175DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN75175DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN75175NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN75175NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

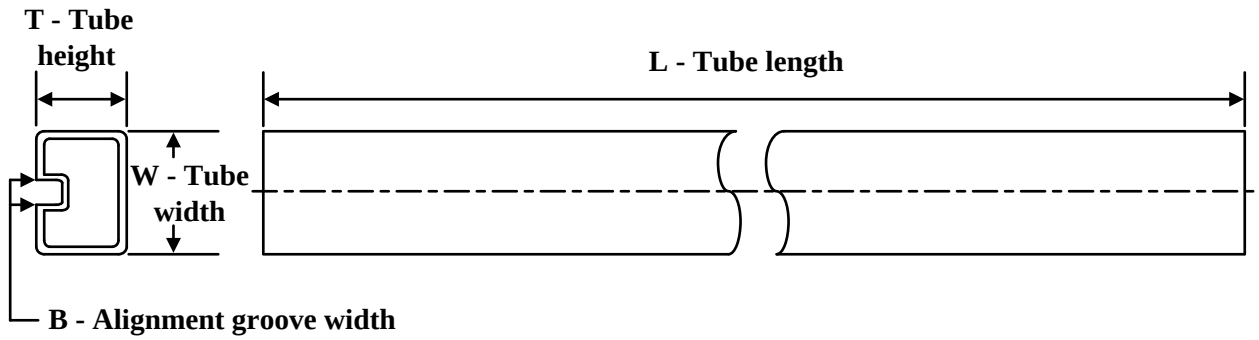
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65175DR	SOIC	D	16	2500	353.0	353.0	32.0
SN75175DR	SOIC	D	16	2500	353.0	353.0	32.0
SN75175DR	SOIC	D	16	2500	356.0	356.0	35.0
SN75175NSR	SO	NS	16	2000	353.0	353.0	32.0
SN75175NSR	SO	NS	16	2000	356.0	356.0	35.0

TUBE



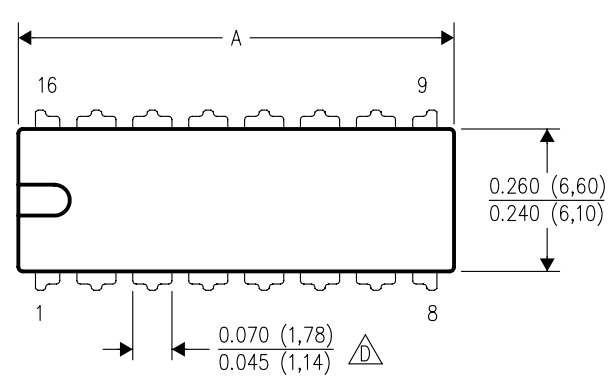
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65175D	D	SOIC	16	40	507	8	3940	4.32
SN75175N	N	PDIP	16	25	506	13.97	11230	4.32

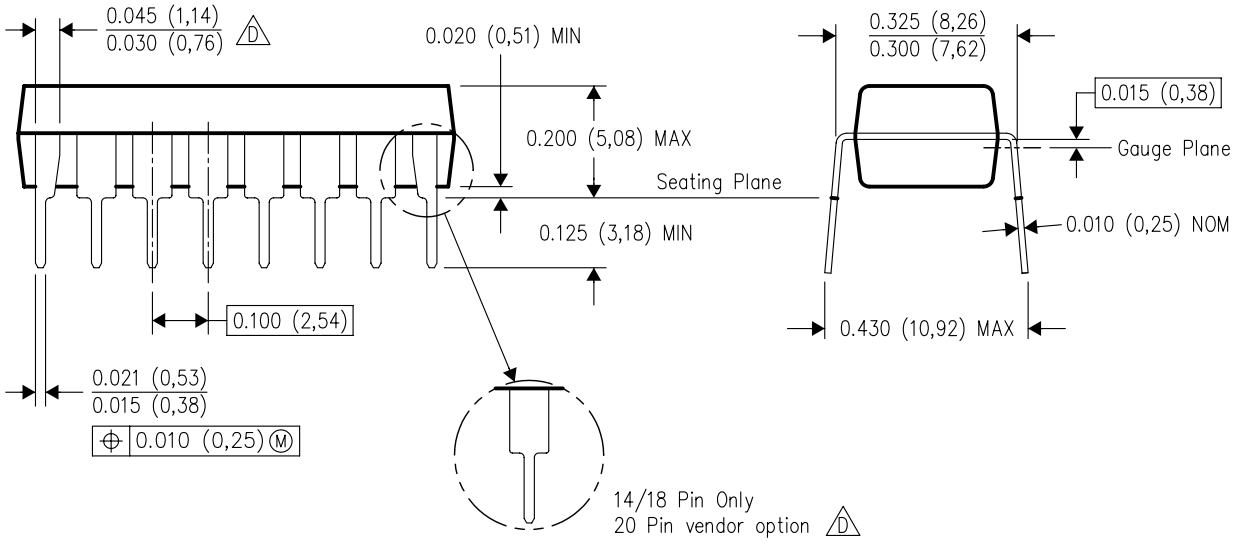
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

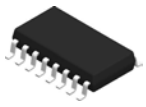


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

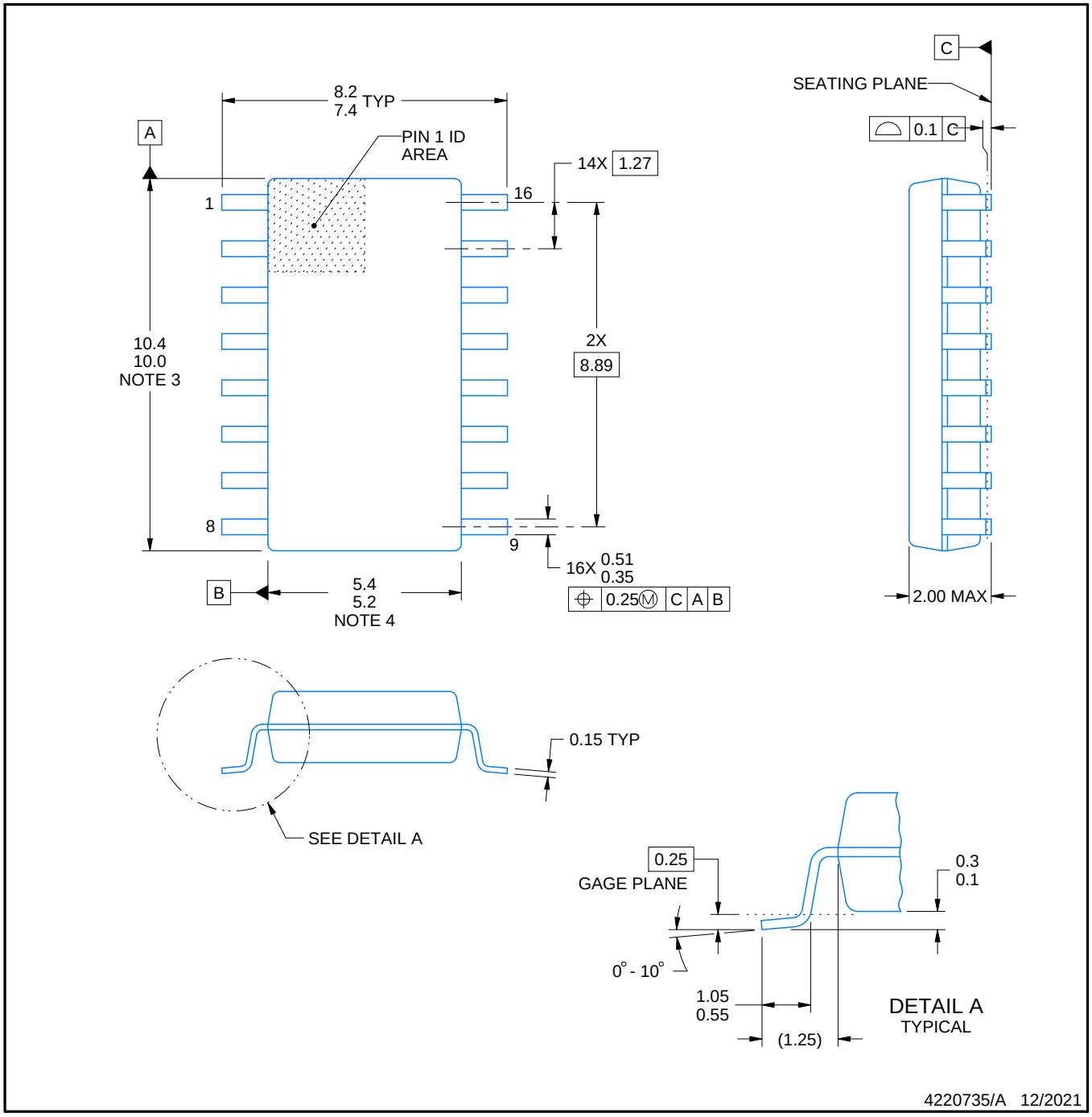


PACKAGE OUTLINE

NS0016A

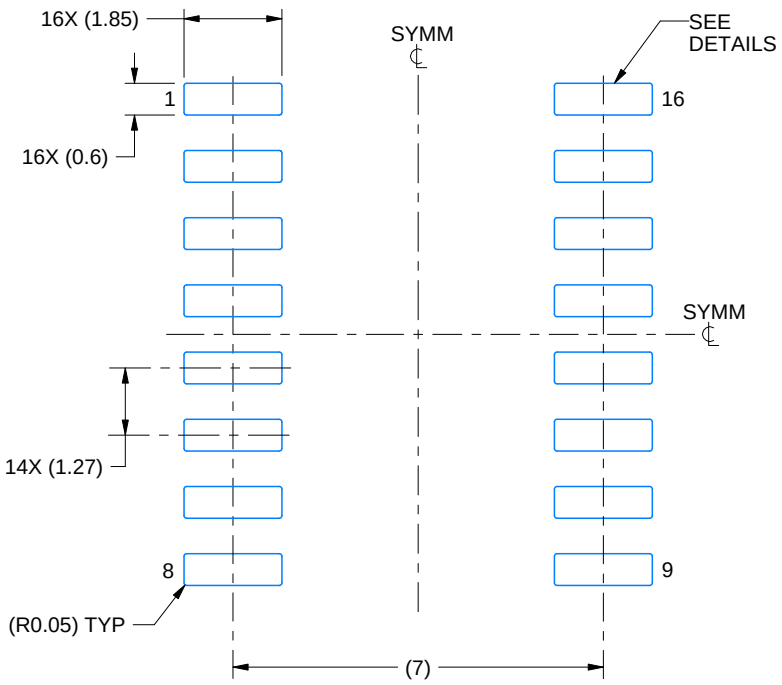
SOP - 2.00 mm max height

SOP

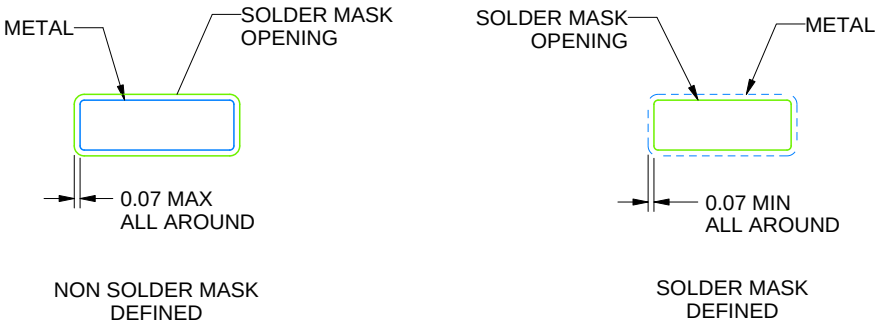


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

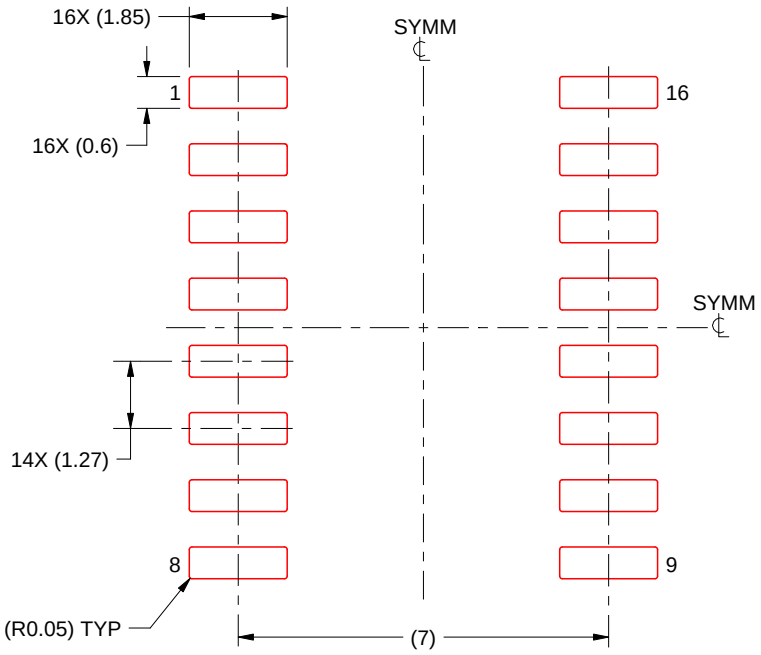
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



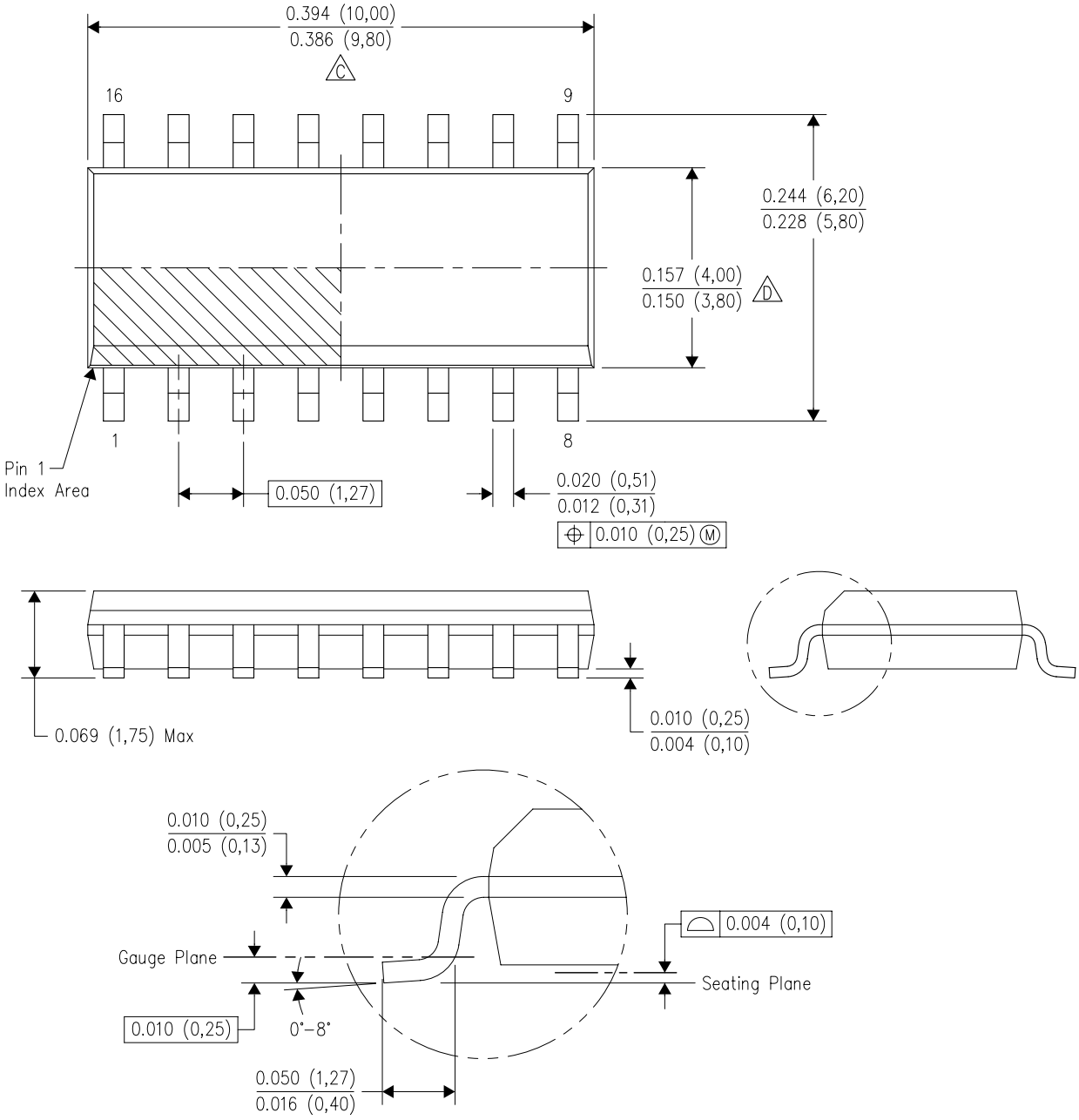
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

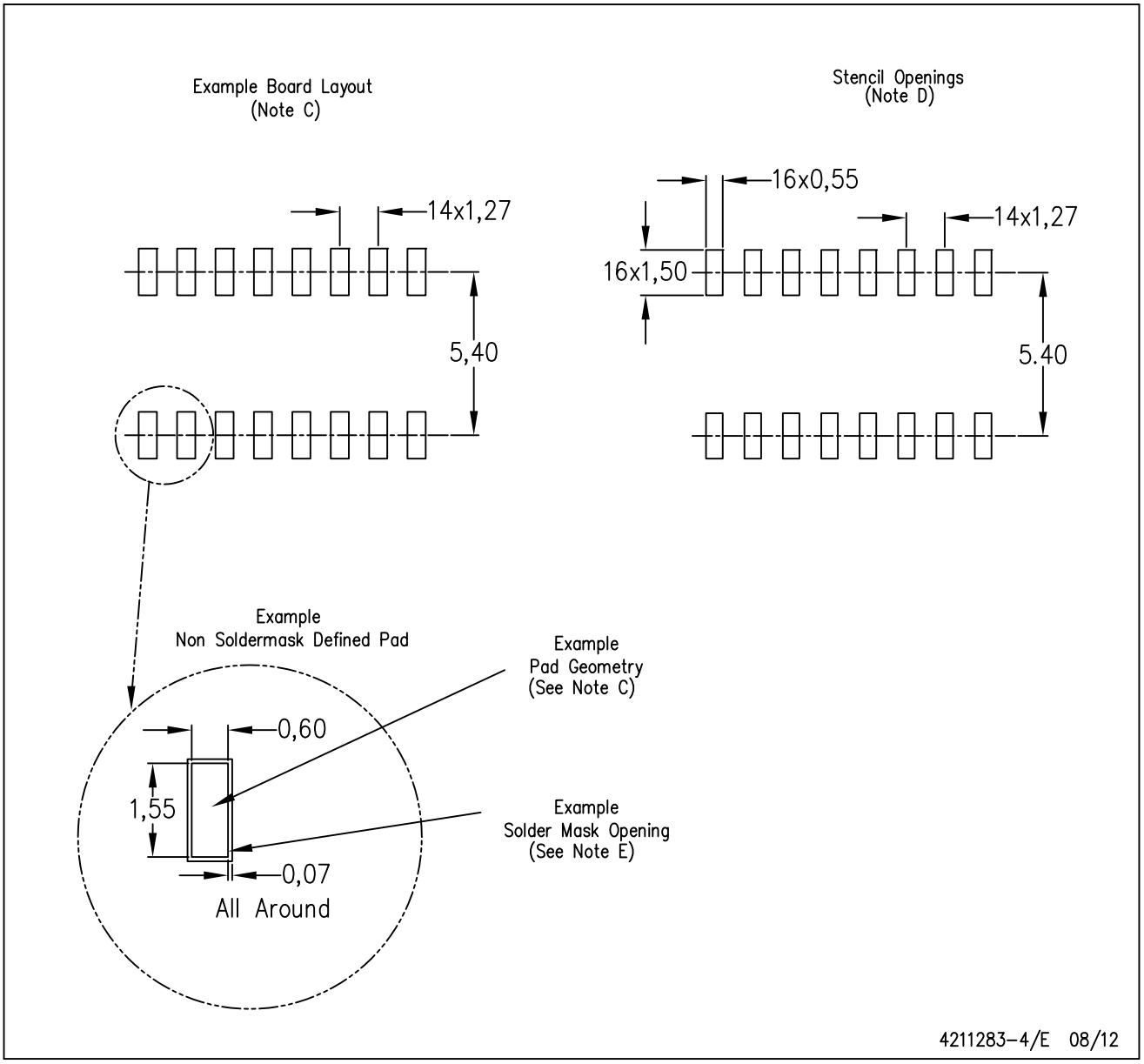
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

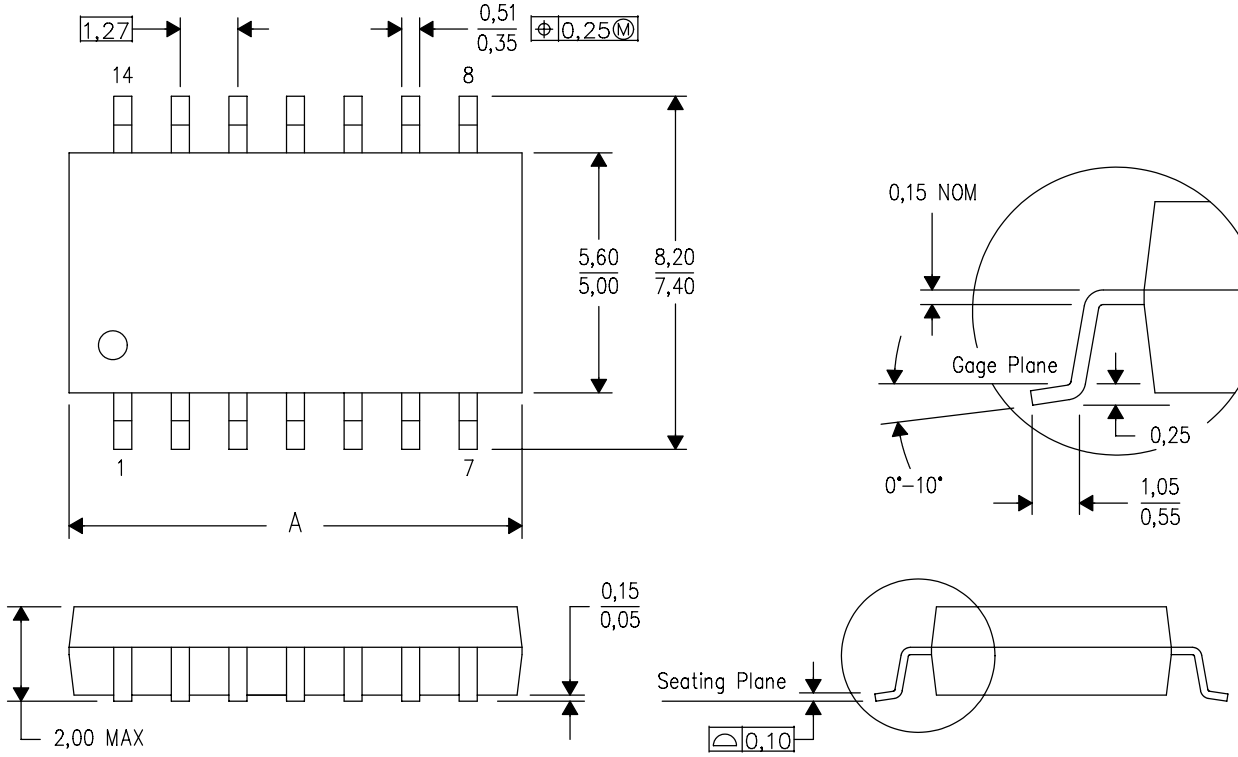


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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