

THS403x 100MHz、低ノイズ、高速アンプ

1 特長

- 1.2nV/√Hz の非常に低い電圧ノイズ
- 高速度:
 - 100MHz の帯域幅 [G = 2 (-1), -3dB]
 - スルー レート: 100V/μs
- 非常に低い歪み
 - THD = -81dBc (f = 1MHz, R_L = 150Ω)
 - THD = -96dBc (f = 1MHz, R_L = 1kΩ)
- 低い入力オフセット電圧: 0.3mV (標準値)
- 200mA の出力電流ドライブ (標準値)
- ±4.5V~±16V の標準動作範囲
- THS4031 のオフセットヌルピン

2 アプリケーション

- 産業アプリケーション向けの低ノイズ、広帯域アンプ
- 電圧制御の発振器
- アクティブ フィルタ
- ビデオ アンプ
- ケーブルドライバ
- 超音波スキャナ
- ベクトル信号トランシーバ (VST)
- データ アクイジション (DAQ)

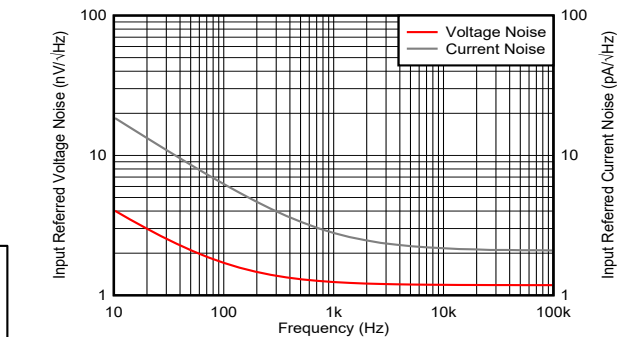
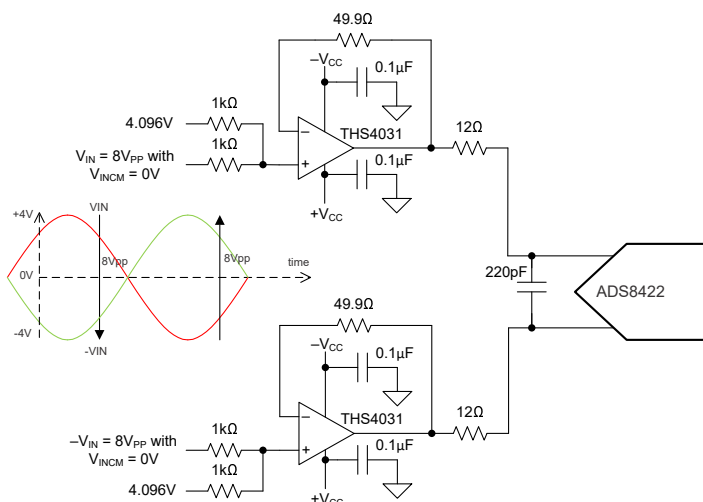
3 概要

THS4031 および THS4032(THS403x) は電圧ノイズが非常に低い高速電圧帰還アンプで、通信やイメージングなど低い電圧ノイズが要求されるアプリケーションに最適です。シングル アンプの THS4031 とデュアル アンプの THS4032 は AC 特性が優れており、100MHz の帯域幅 (G = 2)、100V/μs のスルーレート、70ns のセトリング タイム (0.1%) を実現しています。THS403x は、120MHz の帯域幅でユニティゲイン安定です。これらのアンプには、200mA の大きい駆動能力があり、チャンネルごとに 7.5mA の電流しか消費しません。THS403x は、f = 1MHz において総高調波歪 (THD) が -96dBc で、ノイズが 1.2nV/√Hz と非常に低く、A/D コンバータのバッファなど、低い歪みと低ノイズが要求されるアプリケーション向けに設計されています。

パッケージ情報

部品番号	アンプ	パッケージ (1)	パッケージ サイズ (2)
THS4031	1	D (SOIC, 8)	4.9mm × 6mm
		DGN (HVSSOP, 8)	3.0mm × 4.9mm
THS4032	2	D (SOIC, 8)	4.9mm × 6mm
		DGN (HVSSOP, 8)	3.0mm × 4.9mm

- (1) 詳細については、[セクション 10](#) を参照してください。
- (2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



電圧ノイズおよび電流ノイズと周波数との関係

16 ビット SAR ADC 用の高性能、低ノイズのドライバ



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4 Pin Configuration and Functions

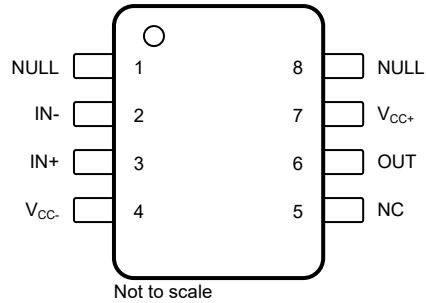


図 4-1. THS4031: D Package, 8-Pin SOIC, or DGN Package, 8-pin HVSSOP (Top View)

表 4-1. Pin Functions: THS4031

PIN		TYPE	DESCRIPTION
NAME	NO.		
IN-	2	Input	Inverting input
IN+	3	Input	Non-inverting input
NC	5	—	No connection
NULL	1, 8	Input	Voltage offset adjust
OUT	6	Output	Output of amplifier
V _{CC-}	4	—	Negative power supply
V _{CC+}	7	—	Positive power supply

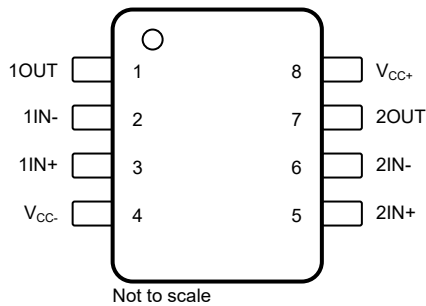


図 4-2. THS4032: D Package, 8-Pin SOIC, or DGN Package, 8-pin HVSSOP (Top View)

表 4-2. Pin Functions: THS4032

PIN		TYPE	DESCRIPTION
NAME	NO.		
1IN-	2	Input	Channel 1 inverting input
1IN+	3	Input	Channel 1 non-inverting input
1OUT	1	Output	Channel 1 output
2IN-	6	Input	Channel 2 inverting input
2IN+	5	Input	Channel 2 non-inverting input
2OUT	7	Output	Channel 2 output
V _{CC-}	4	—	Negative power supply
V _{CC+}	8	—	Positive power supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT	
V_{CC-} to V_{CC+}	Supply voltage		33	V	
V_I	Input voltage		$\pm V_{CC}$	V	
I_O	Output current ⁽²⁾		240	mA	
V_{IO}	Differential input voltage		± 1.5	V	
I_{IN}	Continuous input current		10	mA	
T_A	Operating free-air temperature	C-suffix	0	70	°C
		I-suffix	-40	85	
T_J	Junction temperature	Any condition		150	°C
		Maximum junction temperature, continuous operation, long term reliability ⁽³⁾		130	
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300	°C	
T_{stg}	Storage temperature	-65	150	°C	

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) When continuously operating at any output current, do not exceed the maximum junction temperature. Keep the output current less than the absolute maximum rating regardless of time interval.
- (3) The maximum junction temperature for continuous operation is limited by package constraints. Operation greater than this temperature can result in reduced reliability, lifetime of the device, or both.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins ⁽¹⁾	± 1000	V
		Charged device model (CDM), per JEDEC specification JS-002 ⁽²⁾	± 1000	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	Dual-supply	± 4.5	± 15	± 16	V
		Single-supply	9	30	32	
T_A	Operating free-air temperature	C-suffix	0	25	70	°C
		I-suffix	-40	25	85	

5.4 Thermal Information - THS4031

THERMAL METRIC ⁽¹⁾		THS4031		UNIT
		D (SOIC)	DGN (HVSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	124.5	60.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	65.0	87.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	72.2	33	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	13.6	7.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	71.3	32.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	17.2	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.5 Thermal Information - THS4032

THERMAL METRIC ⁽¹⁾		THS4032		UNIT
		D (SOIC)	DGN (HVSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	121.2	56.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	72.8	48.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61.4	37.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	18.2	2.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	61	37.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	9.9	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.6 Electrical Characteristics - THS4031, $R_L = 150\Omega$

at $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{V}$, and $R_L = 150\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE							
BW	Small-signal bandwidth (–3dB)	Gain = –1V/V or 2V/V	$V_{CC} = \pm 15\text{V}$		100		MHz
			$V_{CC} = \pm 5\text{V}$		90		
	Bandwidth for 0.1dB flatness	Gain = –1V/V or 2V/V	$V_{CC} = \pm 15\text{V}$		9		MHz
			$V_{CC} = \pm 5\text{V}$		9		
SR	Slew rate ⁽¹⁾	Gain = –1V/V	$V_{CC} = \pm 15\text{V}$, 20V step		100		V/ μs
			$V_{CC} = \pm 5\text{V}$, 5V step		80		
t_s	Settling time	To 0.1%, gain = –1V/V	$V_{CC} = \pm 15\text{V}$, 5V step		70		ns
			$V_{CC} = \pm 5\text{V}$, 2.5V step		55		
		To 0.01%, gain = –1V/V	$V_{CC} = \pm 15\text{V}$, 5V step		90		
			$V_{CC} = \pm 5\text{V}$, 2.5V step		80		
NOISE AND DISTORTION PERFORMANCE							
THD	Total harmonic distortion	Gain = 2V/V, $V_{CC} = \pm 5\text{V}$ or $\pm 15\text{V}$, $f = 1\text{MHz}$ $V_{O(pp)} = 2\text{V}$			–81		dBc
V_n	Input voltage noise	$V_{CC} = \pm 5\text{V}$ or $\pm 15\text{V}$, $f > 10\text{kHz}$			1.2		nV/ $\sqrt{\text{Hz}}$
I_n	Input current noise	$V_{CC} = \pm 5\text{V}$ or $\pm 15\text{V}$, $f > 10\text{kHz}$			2.3		pA/ $\sqrt{\text{Hz}}$
	Differential gain error	Gain = 2V/V, 40 IRE modulation, NTSC and PAL, ± 100 IRE ramp	$V_{CC} = \pm 15\text{V}$		0.015%		°
			$V_{CC} = \pm 5\text{V}$		0.02%		
	Differential phase error		$V_{CC} = \pm 15\text{V}$		0.025		°
			$V_{CC} = \pm 5\text{V}$		0.03		
DC PERFORMANCE							
	Open-loop gain	$V_{CC} = \pm 15\text{V}$, $V_O = \pm 10\text{V}$	$T_A = 25^\circ\text{C}$	93	100		dB
			$T_A = \text{full range}$	92			
		$V_{CC} = \pm 5\text{V}$, $V_O = \pm 2.5\text{V}$	$T_A = 25^\circ\text{C}$	90	98		
			$T_A = \text{full range}$	89			
V_{OS}	Input offset voltage	$V_{CC} = \pm 5\text{V}$ or $\pm 15\text{V}$	$T_A = 25^\circ\text{C}$		0.3	2	mV
			$T_A = \text{full range}$			3	
	Offset voltage drift	$V_{CC} = \pm 5\text{V}$ or $\pm 15\text{V}$, $T_A = \text{full range}$			2		$\mu\text{V}/^\circ\text{C}$
I_{IB}	Input bias current	$V_{CC} = \pm 5\text{V}$ or $\pm 15\text{V}$	$T_A = 25^\circ\text{C}$		9	20	μA
			$T_A = \text{full range}$			33	
I_{OS}	Input offset current	$V_{CC} = \pm 5\text{V}$ or $\pm 15\text{V}$	$T_A = 25^\circ\text{C}$		30	250	nA
			$T_A = \text{full range}$			400	
	Input offset current	$V_{CC} = \pm 5\text{V}$ or $\pm 15\text{V}$, $T_A = \text{full range}$			0.2		nA/ $^\circ\text{C}$
INPUT CHARACTERISTICS							
V_{ICR}	Common-mode input voltage range	$V_{CC} = \pm 15\text{V}$		± 13.5	± 14.3		V
		$V_{CC} = \pm 5\text{V}$		± 3.8	± 4.3		
CMRR	Common-mode rejection ratio	$V_{CC} = \pm 15\text{V}$, $V_{ICR} = \pm 12\text{V}$	$T_A = 25^\circ\text{C}$	85	95		dB
			$T_A = \text{full range}$	80			
		$V_{CC} = \pm 5\text{V}$, $V_{ICR} = \pm 2.5\text{V}$	$T_A = 25^\circ\text{C}$	90	100		
			$T_A = \text{full range}$	85			
R_i	Input resistance				2		M Ω
C_i	Input capacitance				1.5		pF
OUTPUT CHARACTERISTICS							
V_O	Output voltage swing	$V_{CC} = \pm 15\text{V}$, $R_L = 250\Omega$		± 12	± 12.9		V
		$V_{CC} = \pm 5\text{V}$		± 3	± 3.5		
I_O	Output current ⁽²⁾	$R_L = 10\Omega$	$V_{CC} = \pm 15\text{V}$	60	200		mA
			$V_{CC} = \pm 5\text{V}$	50	160		
R_O	Output resistance	Open loop			5		Ω

5.6 Electrical Characteristics - THS4031, $R_L = 150\Omega$ (続き)

at $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{V}$, and $R_L = 150\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY							
V_{CC}	Supply voltage	Dual supply		± 4.5		± 16.5	V
		Single supply		9		33	
I_{CC}	Supply current (each amplifier)	$V_{CC} = \pm 15\text{V}$	$T_A = 25^\circ\text{C}$		7.5	10	mA
			$T_A = \text{full range}$			11	
		$V_{CC} = \pm 5\text{V}$	$T_A = 25^\circ\text{C}$		6.5	9	
			$T_A = \text{full range}$			10.5	
PSRR	Power-supply rejection ratio	$V_{CC} = \pm 5\text{V}$ or $\pm 15\text{V}$	$T_A = 25^\circ\text{C}$	85	95		dB
			$T_A = \text{full range}$	80			

(1) Slew rate is measured from an output level range of 25% to 75%.

(2) Keep junction temperature less than the absolute maximum rating when the output is heavily loaded or shorted; see also [Section 5.1](#).

5.7 Electrical Characteristics - THS4031, $R_L = 1\text{k}\Omega$

at $T_A = \text{full range}$, $V_{CC} = \pm 15\text{V}$, and $R_L = 1\text{k}\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE							
	Unity gain bandwidth	$V_{CC} = \pm 15\text{V}$, closed loop		100 ⁽¹⁾	120		MHz
BW	Small-signal bandwidth (-3dB)	Gain = -1V/V or 2V/V	$V_{CC} = \pm 15\text{V}$		100		MHz
			$V_{CC} = \pm 5\text{V}$		90		
	Bandwidth for 0.1dB flatness	Gain = -1V/V or 2V/V	$V_{CC} = \pm 15\text{V}$		9		MHz
			$V_{CC} = \pm 5\text{V}$		9		
	Full power bandwidth ⁽²⁾	$V_{CC} = \pm 15\text{V}$, $V_{O(pp)} = 20\text{V}$			1.6		MHz
		$V_{CC} = \pm 5\text{V}$, $V_{O(pp)} = 5\text{V}$			5.1		
SR	Slew rate			80 ⁽¹⁾	100		V/ μs
t_s	Settling time	To 0.1%, gain = -1V/V	$V_{CC} = \pm 15\text{V}$, 5V step		70		ns
			$V_{CC} = \pm 5\text{V}$, 2.5V step		55		
		To 0.01%, gain = -1V/V	$V_{CC} = \pm 15\text{V}$, 5V step		90		
			$V_{CC} = \pm 5\text{V}$, 2.5V step		80		
NOISE AND DISTORTION PERFORMANCE							
THD	Total harmonic distortion	Gain = 2V/V , $V_{CC} = \pm 5\text{V}$ or $\pm 15\text{V}$, $f = 1\text{MHz}$, $V_{O(pp)} = 2\text{V}$			-96		dBc
DC PERFORMANCE							
	Open-loop gain	$V_{CC} = \pm 15\text{V}$, $V_O = \pm 10\text{V}$	$T_A = 25^\circ\text{C}$	93	100		dB
			$T_A = \text{full range}$	92			
		$V_{CC} = \pm 5\text{V}$, $V_O = \pm 2.5\text{V}$	$T_A = 25^\circ\text{C}$	92	98		
			$T_A = \text{full range}$	91			
V_{OS}	Input offset voltage	$V_{CC} = \pm 5\text{V}$ or $\pm 15\text{V}$	$T_A = 25^\circ\text{C}$		0.3	2	mV
			$T_A = \text{full range}$			3	
	Offset voltage drift	$V_{CC} = \pm 5\text{V}$ or $\pm 15\text{V}$, $T_A = \text{full range}$			2		$\mu\text{V}/^\circ\text{C}$
I_{IB}	Input bias current	$V_{CC} = \pm 5\text{V}$ or $\pm 15\text{V}$	$T_A = 25^\circ\text{C}$		9	20	μA
			$T_A = \text{full range}$			33	
I_{OS}	Input offset current	$V_{CC} = \pm 5\text{V}$ or $\pm 15\text{V}$	$T_A = 25^\circ\text{C}$		30	250	μA
			$T_A = \text{full range}$			400	
	Input offset current drift	$V_{CC} = \pm 5\text{V}$ or $\pm 15\text{V}$, $T_A = \text{full range}$			0.2		$\text{nA}/^\circ\text{C}$

5.7 Electrical Characteristics - THS4031, $R_L = 1k\Omega$ (続き)

at $T_A =$ full range, $V_{CC} = \pm 15V$, and $R_L = 1k\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS							
V_{ICR}	Common-mode input voltage range	$V_{CC} = \pm 15V$		± 13.5	± 14.3		V
		$V_{CC} = \pm 5V$		± 3.8	± 4.3		
$CMRR$	Common-mode rejection ratio	$V_{CC} = \pm 15V, V_{ICR} = \pm 12V$	$T_A = 25^\circ C$	85	95		dB
			$T_A =$ full range	80			
		$V_{CC} = \pm 5V, V_{ICR} = \pm 2.5V$	$T_A = 25^\circ C$	90	100		
			$T_A =$ full range	85			
R_i	Input resistance				2		M Ω
C_i	Input capacitance				1.5		pF
OUTPUT CHARACTERISTICS							
V_O	Output voltage swing	$V_{CC} = \pm 15V$		± 13	± 13.6		V
		$V_{CC} = \pm 5V$		± 3.4	± 3.8		
R_O	Output resistance	Open loop			5		Ω
POWER SUPPLY							
V_{CC}	Supply voltage operating range	Dual supply		± 4.5		± 16.5	V
		Single supply		9		33	
I_{CC}	Supply current (each amplifier)	$V_{CC} = \pm 15V$	$T_A = 25^\circ C$		7.5	10	mA
			$T_A =$ full range			11	
		$V_{CC} = \pm 5V$	$T_A = 25^\circ C$		6.5	9	
			$T_A =$ full range			10	
$PSRR$	Power-supply rejection ratio	$V_{CC} = \pm 5V$ or $\pm 15V$		$T_A = 25^\circ C$	85	95	dB
				$T_A =$ full range	80		

- (1) This minimum value is not tested.
- (2) Full power bandwidth = slew rate / $[\pi V_{O(P-P)}]$.

5.8 Electrical Characteristics - THS4032, $R_L = 150\Omega$

at $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{V}$, and $R_L = 150\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE							
BW	Small-signal bandwidth (–3 dB)	Gain = –1V/V or 2V/V	$V_{CC} = \pm 15\text{V}$		100		MHz
			$V_{CC} = \pm 5\text{V}$		90		
	Bandwidth for 0.1dB flatness	Gain = –1V/V or 2V/V	$V_{CC} = \pm 15\text{V}$		50		MHz
			$V_{CC} = \pm 5\text{V}$		45		
SR	Slew rate ⁽¹⁾	Gain = –1V/V	$V_{CC} = \pm 15\text{V}$, 20V step		100		V/ μs
			$V_{CC} = \pm 5\text{V}$, 5V step		80		
t_s	Settling time	To 0.1%, Gain = –1V/V	$V_{CC} = \pm 15\text{V}$, 5V step		60		ns
			$V_{CC} = \pm 5\text{V}$, 2.5V step		45		
		To 0.01%, Gain = –1V/V	$V_{CC} = \pm 15\text{V}$, 5V step		90		
			$V_{CC} = \pm 5\text{V}$, 2.5V step		80		
NOISE AND DISTORTION PERFORMANCE							
THD	Total harmonic distortion	Gain = 2V/V, $V_{CC} = \pm 5\text{V}$ or $\pm 15\text{V}$, $f = 1\text{MHz}$ $V_{O(pp)} = 2\text{V}$			–72		dBc
V_n	Input voltage noise	$V_{CC} = \pm 5\text{V}$ or $\pm 15\text{V}$, $f > 10\text{kHz}$			1.6		nV/ $\sqrt{\text{Hz}}$
I_n	Input current noise	$V_{CC} = \pm 5\text{V}$ or $\pm 15\text{V}$, $f > 10\text{kHz}$			1.2		pA/ $\sqrt{\text{Hz}}$
	Differential gain error	Gain = 2V/V, 40 IRE modulation, NTSC and PAL, ± 100 IRE ramp	$V_{CC} = \pm 15\text{V}$		0.015%		
			$V_{CC} = \pm 5\text{V}$		0.02%		
	Differential phase error		$V_{CC} = \pm 15\text{V}$		0.025		°
			$V_{CC} = \pm 5\text{V}$		0.03		
	Channel-to-channel crosstalk (THS4032 only)	$V_{CC} = \pm 5\text{V}$ or $\pm 15\text{V}$, $f = 1\text{MHz}$			–61		dBc
DC PERFORMANCE							
V_{OS}	Input offset voltage	$V_{CC} = \pm 5\text{V}$ or $\pm 15\text{V}$	$T_A = 25^\circ\text{C}$		0.5	2	mV
			$T_A = \text{full range}$			3	
I_{OS}	Input offset current	$V_{CC} = \pm 5\text{V}$ or $\pm 15\text{V}$	$T_A = 25^\circ\text{C}$		30	250	nA
			$T_A = \text{full range}$			400	
	Offset voltage drift	$V_{CC} = \pm 5\text{V}$ or $\pm 15\text{V}$, $T_A = \text{full range}$			2		$\mu\text{V}/^\circ\text{C}$
	Input offset current drift	$V_{CC} = \pm 5\text{V}$ or $\pm 15\text{V}$, $T_A = \text{full range}$			0.2		nA/ $^\circ\text{C}$
INPUT CHARACTERISTICS							
V_{ICR}	Common-mode input voltage range	$V_{CC} = \pm 15\text{V}$		± 13.5	± 14		V
		$V_{CC} = \pm 5\text{V}$		± 3.8	± 4		
CMRR	Common-mode rejection ratio	$V_{CC} = \pm 15\text{V}$, $V_{ICR} = \pm 12\text{V}$	$T_A = 25^\circ\text{C}$	85	95		dB
			$T_A = \text{full range}$	80			
		$V_{CC} = \pm 5\text{V}$, $V_{ICR} = \pm 2.5\text{V}$	$T_A = 25^\circ\text{C}$	90	100		
			$T_A = \text{full range}$	85			
R_i	Input resistance				2		M Ω
C_i	Input capacitance				1.5		pF
OUTPUT CHARACTERISTICS							
V_O	Output voltage swing	$V_{CC} = \pm 15\text{V}$, $R_L = 250\Omega$		± 12	± 12.9		V
		$V_{CC} = \pm 5\text{V}$		± 3	± 3.5		
I_O	Output current ⁽²⁾	$R_L = 20\Omega$	$V_{CC} = \pm 15\text{V}$	60	90		mA
			$V_{CC} = \pm 5\text{V}$	50	70		
I_{SC}	Short-circuit current ⁽²⁾	$V_{CC} = \pm 15\text{V}$			150		mA
R_O	Output resistance	Open loop			13		Ω

5.8 Electrical Characteristics - THS4032, $R_L = 150\Omega$ (続き)

 at $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{V}$, and $R_L = 150\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY							
V_{CC}	Supply voltage operating range	Dual supply		± 4.5		± 16.5	V
		Single supply		9		33	
I_{CC}	Supply current (each amplifier)	$V_{CC} = \pm 15\text{V}$	$T_A = 25^\circ\text{C}$		8.5	10	mA
			$T_A = \text{full range}$			11	
		$V_{CC} = \pm 5\text{V}$	$T_A = 25^\circ\text{C}$		7.5	9	
			$T_A = \text{full range}$			10.5	
PSRR	Power-supply rejection ratio	$V_{CC} = \pm 5\text{V}$ or $\pm 15\text{V}$	$T_A = 25^\circ\text{C}$	85	95	dB	
			$T_A = \text{full range}$	80			

(1) Slew rate is measured from an output level range of 25% to 75%.

 (2) Keep junction temperature less than the absolute maximum rating when the output is heavily loaded or shorted; see also [セクション 5.1](#).

5.9 Electrical Characteristics - THS4032, $R_L = 1\text{k}\Omega$

 at $T_A = \text{full range}$, $V_{CC} = \pm 15\text{V}$, and $R_L = 1\text{k}\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE							
	Unity gain bandwidth	$V_{CC} = \pm 15\text{V}$, closed loop		100 ⁽¹⁾	120		MHz
BW	Small-signal bandwidth (-3dB)	Gain = -12V/V or 2V/V	$V_{CC} = \pm 15\text{V}$		100		MHz
			$V_{CC} = \pm 5\text{V}$		90		
	Bandwidth for 0.1dB flatness	Gain = -1V/V or 2V/V	$V_{CC} = \pm 15\text{V}$		50		MHz
			$V_{CC} = \pm 5\text{V}$		45		
	Full power bandwidth ⁽²⁾	$V_{CC} = \pm 15\text{V}$, $V_{O(pp)} = 20\text{V}$			2.3		MHz
		$V_{CC} = \pm 5\text{V}$, $V_{O(pp)} = 5\text{V}$			7.1		
SR	Slew rate	$V_{CC} = \pm 15\text{V}$		80 ⁽¹⁾	100		V/ μs
t_s	Settling time	To 0.1%, Gain = -1V/V	$V_{CC} = \pm 15\text{V}$, 5V step		60		ns
			$V_{CC} = \pm 5\text{V}$, 2.5V step		45		
		To 0.01%, Gain = -1V/V	$V_{CC} = \pm 15\text{V}$, 5V step		90		
			$V_{CC} = \pm 5\text{V}$, 2.5V step		80		
NOISE AND DISTORTION PERFORMANCE							
THD	Total harmonic distortion	$V_{CC} = \pm 5\text{V}$ or $\pm 15\text{V}$, $f = 1\text{MHz}$, Gain = 2V/V , $V_{O(pp)} = 2\text{V}$, $T_A = 25^\circ\text{C}$			-96		dBc
DC PERFORMANCE							
	Open loop gain	$V_{CC} = \pm 15\text{V}$, $V_O = \pm 10\text{V}$	$T_A = 25^\circ\text{C}$	93	98	dB	
			$T_A = \text{full range}$	92			
		$V_{CC} = \pm 5\text{V}$, $V_O = \pm 2.5\text{V}$	$T_A = 25^\circ\text{C}$	92	95		
			$T_A = \text{full range}$	91			
V_{OS}	Input offset voltage	$V_{CC} = \pm 5\text{V}$ or $\pm 15\text{V}$	$T_A = 25^\circ\text{C}$		0.5	2	mV
			$T_A = \text{full range}$			3	
I_{IB}	Input bias current	$V_{CC} = \pm 5\text{V}$ or $\pm 15\text{V}$	$T_A = 25^\circ\text{C}$		3	6	μA
			$T_A = \text{full range}$			8	
I_{OS}	Input offset current	$V_{CC} = \pm 5\text{V}$ or $\pm 15\text{V}$	$T_A = 25^\circ\text{C}$		30	250	nA
			$T_A = \text{full range}$			400	
	Input offset current drift	$V_{CC} = \pm 5\text{V}$ or $\pm 15\text{V}$, $T_A = \text{full range}$			0.2		nA/ $^\circ\text{C}$
	Offset voltage drift	$V_{CC} = \pm 5\text{V}$ or $\pm 15\text{V}$, $T_A = \text{full range}$			2		$\mu\text{V}/^\circ\text{C}$

5.9 Electrical Characteristics - THS4032, $R_L = 1\text{k}\Omega$ (続き)

at $T_A = \text{full range}$, $V_{CC} = \pm 15\text{ V}$, and $R_L = 1\text{ k}\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS							
V_{ICR}	Common-mode input voltage range	$V_{CC} = \pm 15\text{V}$		± 13.5	± 14.3		V
		$V_{CC} = \pm 5\text{V}$		± 3.8	± 4.3		
$CMRR$	Common-mode rejection ratio	$V_{CC} = \pm 15\text{V}$, $V_{ICR} = \pm 12\text{V}$	$T_A = 25^\circ\text{C}$	85	95		dB
			$T_A = \text{full range}$	80			
		$V_{CC} = \pm 5\text{V}$, $V_{ICR} = \pm 2.5\text{V}$	$T_A = 25^\circ\text{C}$	90	100		
			$T_A = \text{full range}$	85			
R_i	Input resistance				2		M Ω
C_i	Input capacitance				1.5		pF
OUTPUT CHARACTERISTICS							
V_O	Output voltage swing	$V_{CC} = \pm 15\text{V}$		± 13	± 13.6		V
		$V_{CC} = \pm 5\text{V}$		± 3.4	± 3.8		V
I_O	Output current ⁽²⁾	$R_L = 20\Omega$	$V_{CC} = \pm 15\text{V}$	60	90		mA
			$V_{CC} = \pm 5\text{V}$	50	70		
I_{SC}	Short-circuit current ⁽³⁾	$V_{CC} = \pm 15\text{V}$			150		mA
R_O	Output resistance	Open loop			13		Ω
POWER SUPPLY							
V_{CC}	Supply voltage operating range	Dual supply		± 4.5		± 16.5	V
		Single supply		9		33	
I_{CC}	Supply current (each amplifier)	$V_{CC} = \pm 15\text{V}$	$T_A = 25^\circ\text{C}$		8.5	10	mA
			$T_A = \text{full range}$			11	
		$V_{CC} = \pm 5\text{V}$	$T_A = 25^\circ\text{C}$		7.5	9	
			$T_A = \text{full range}$			10	
PSRR	Power-supply rejection ratio	$V_{CC} = \pm 5\text{V}$ or $\pm 15\text{V}$		$T_A = 25^\circ\text{C}$	85	95	dB
				$T_A = \text{full range}$	80		

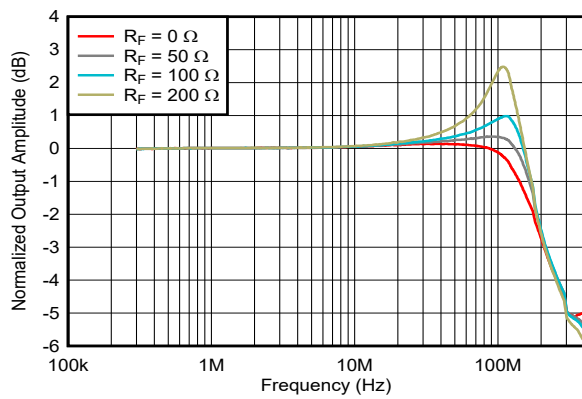
(1) This minimum value is not tested.

(2) Full power bandwidth = slew rate / $[\sqrt{2} \pi V_{OC(\text{Peak})}]$.

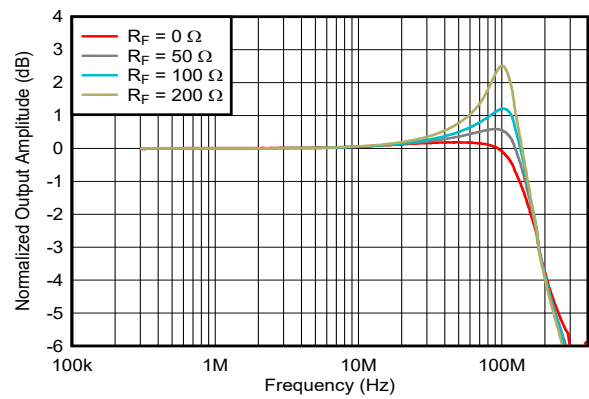
(3) Keep junction temperature less than the absolute maximum rating when the output is heavily loaded or shorted; see also [セクション 5.1](#).

5.10 Typical Characteristics - THS4031

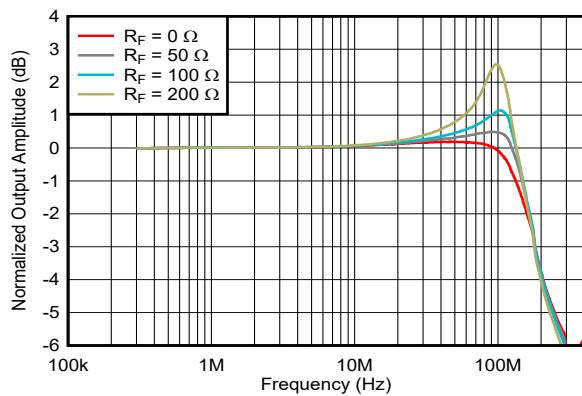
at $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{ V}$, gain = +1 V/V, $R_L = 150\ \Omega$, and $R_F = 300\ \Omega$ (unless otherwise noted)



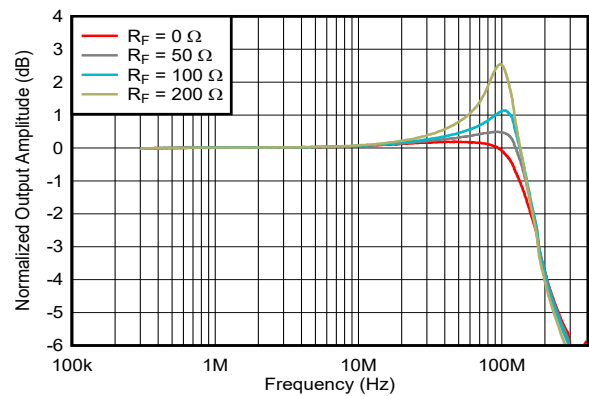
5-1. Frequency Response vs Feedback Resistance



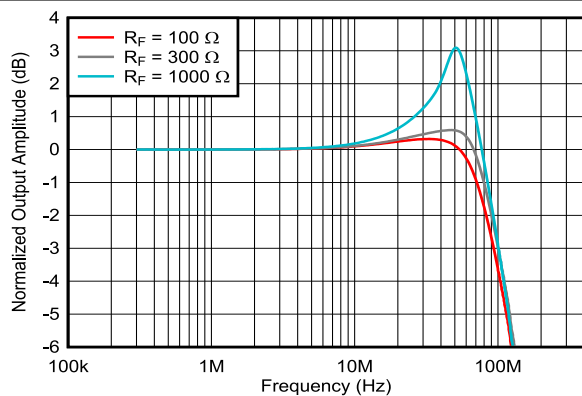
5-2. Frequency Response vs Feedback Resistance



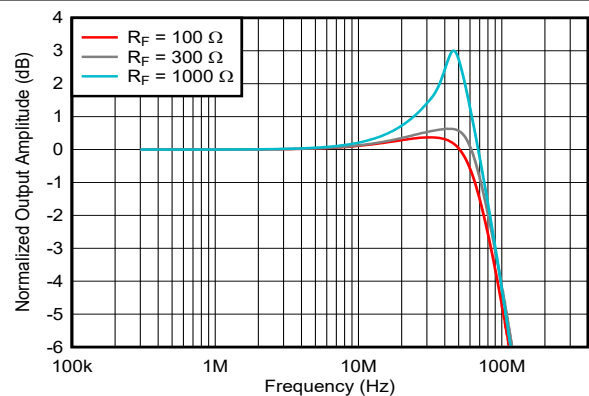
5-3. Frequency Response vs Feedback Resistance



5-4. Frequency Response vs Feedback Resistance



5-5. Frequency Response vs Feedback Resistance



5-6. Frequency Response vs Feedback Resistance

5.10 Typical Characteristics - THS4031 (continued)

at $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{ V}$, gain = +1 V/V, $R_L = 150\ \Omega$, and $R_F = 300\ \Omega$ (unless otherwise noted)

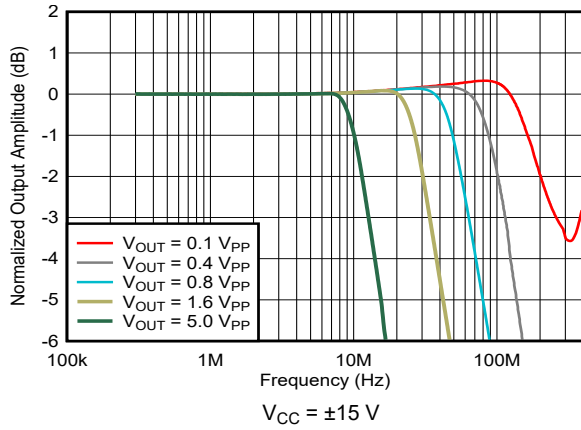


図 5-7. Large-Signal Frequency Response

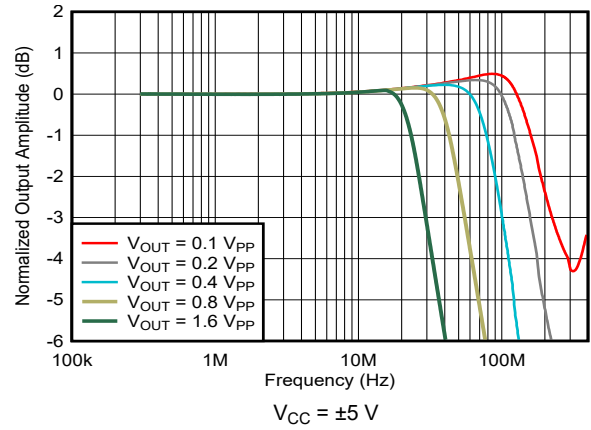


図 5-8. Large-Signal Frequency Response

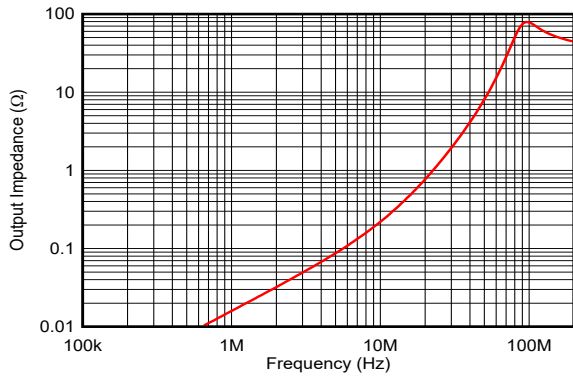


図 5-9. Closed-Loop Output Impedance

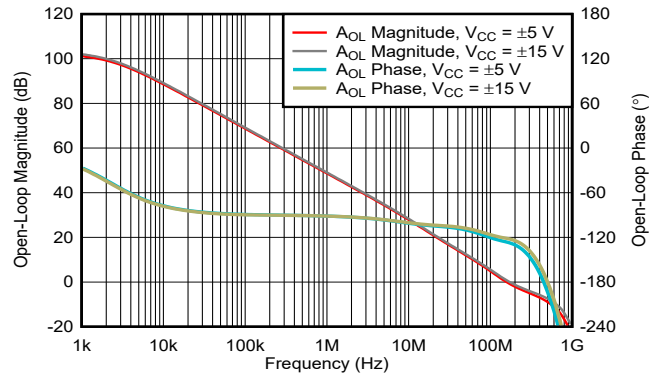


図 5-10. Open-Loop Gain and Phase Response

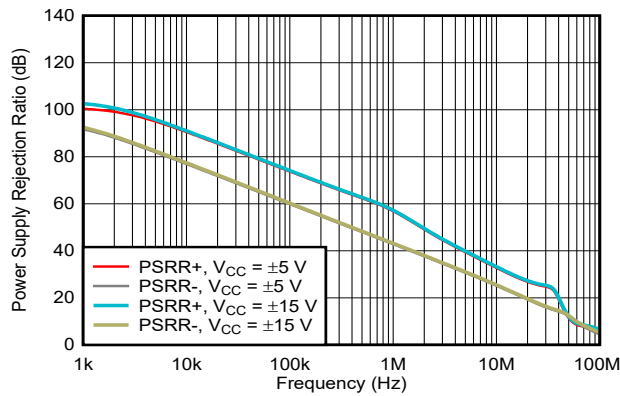


図 5-11. Power-Supply Rejection Ratio vs Frequency

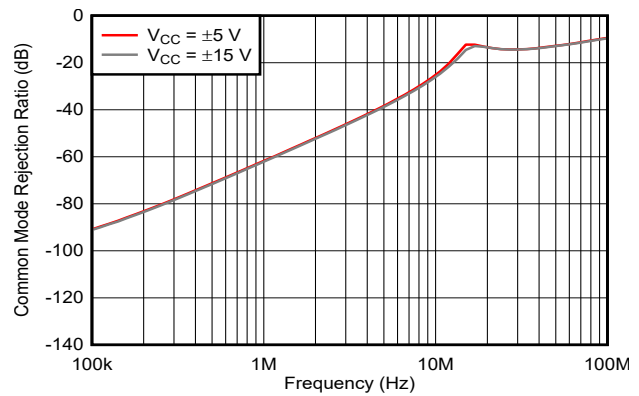


図 5-12. Common-Mode Rejection Ratio vs Frequency

5.10 Typical Characteristics - THS4031 (continued)

at $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{ V}$, gain = +1 V/V, $R_L = 150\ \Omega$, and $R_F = 300\ \Omega$ (unless otherwise noted)

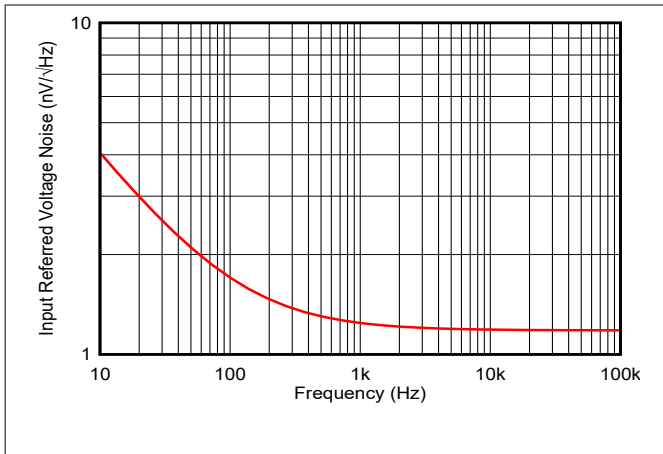


图 5-13. Input-Referred Voltage Noise vs Frequency

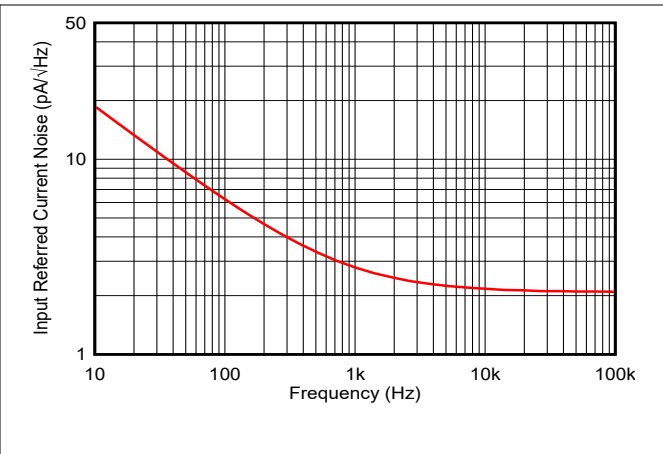


图 5-14. Input-Referred Current Noise vs Frequency

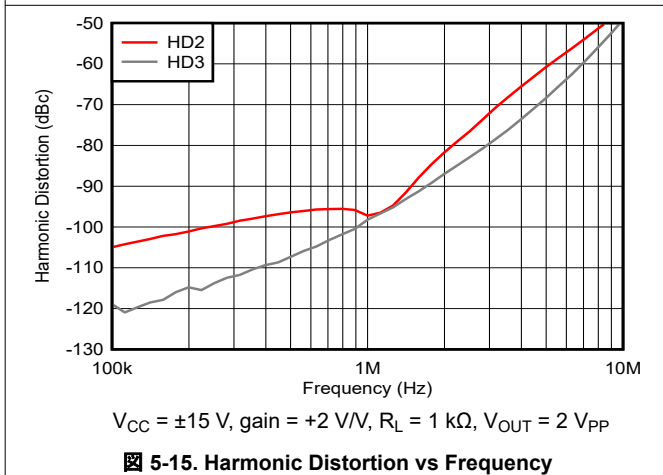


图 5-15. Harmonic Distortion vs Frequency

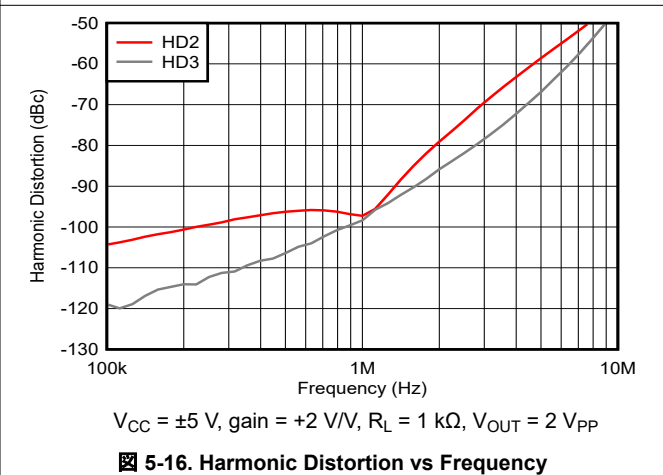


图 5-16. Harmonic Distortion vs Frequency

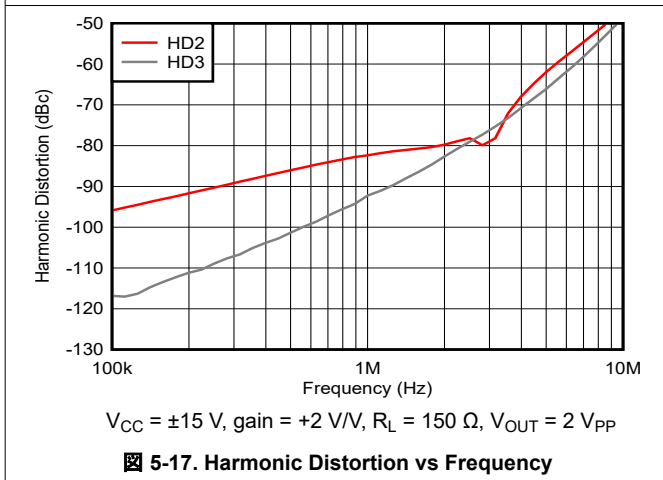


图 5-17. Harmonic Distortion vs Frequency

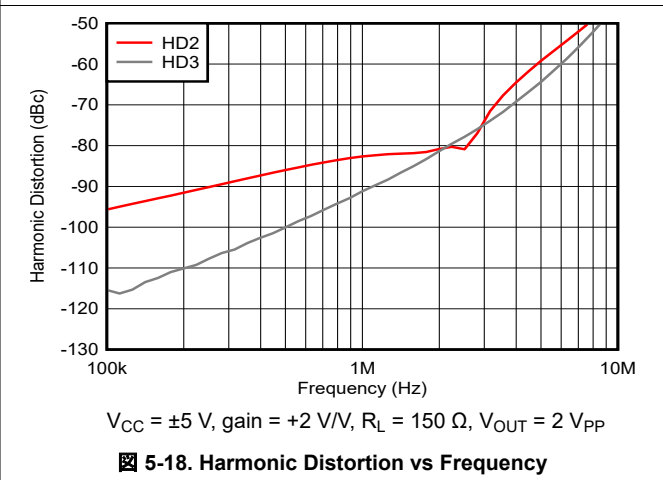
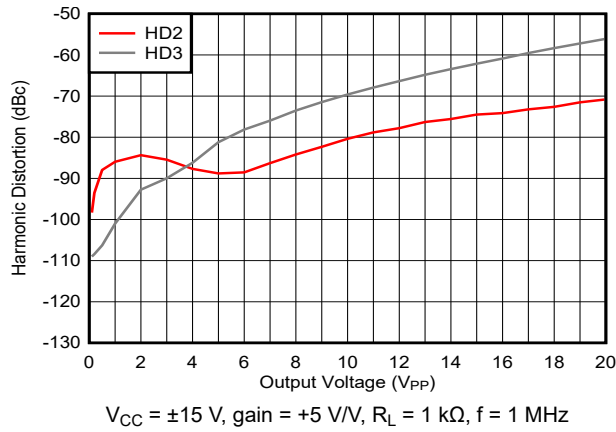


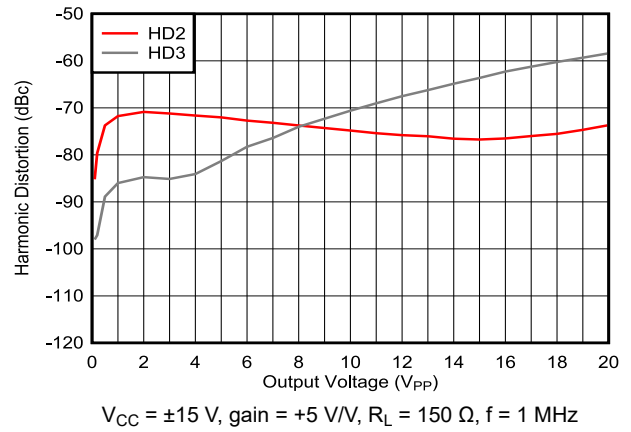
图 5-18. Harmonic Distortion vs Frequency

5.10 Typical Characteristics - THS4031 (continued)

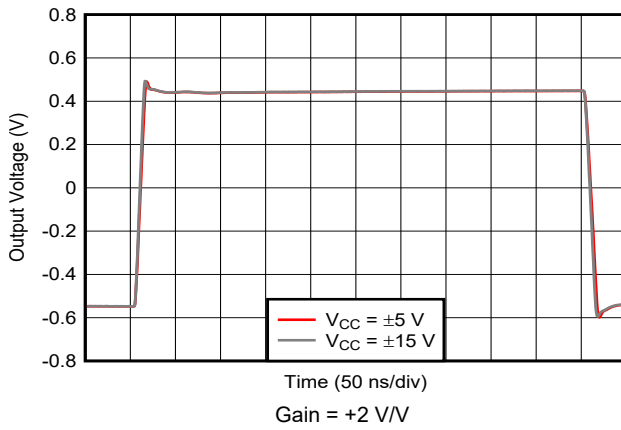
at $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{ V}$, gain = +1 V/V, $R_L = 150\ \Omega$, and $R_F = 300\ \Omega$ (unless otherwise noted)



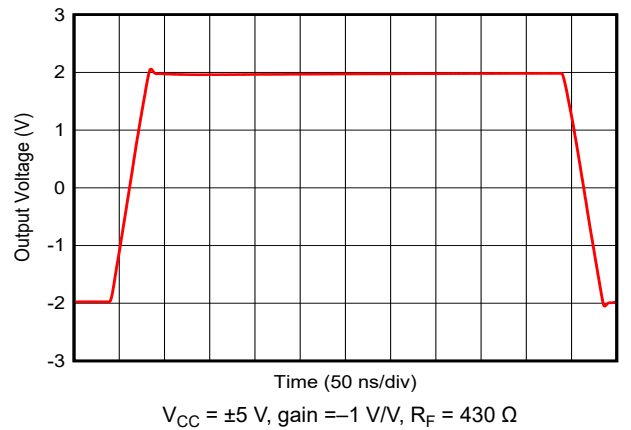
5-19. Harmonic Distortion vs Peak-to-Peak Output Voltage



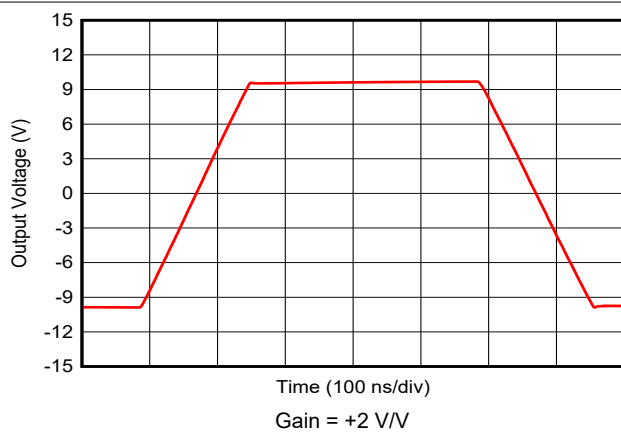
5-20. Harmonic Distortion vs Peak-to-Peak Output Voltage



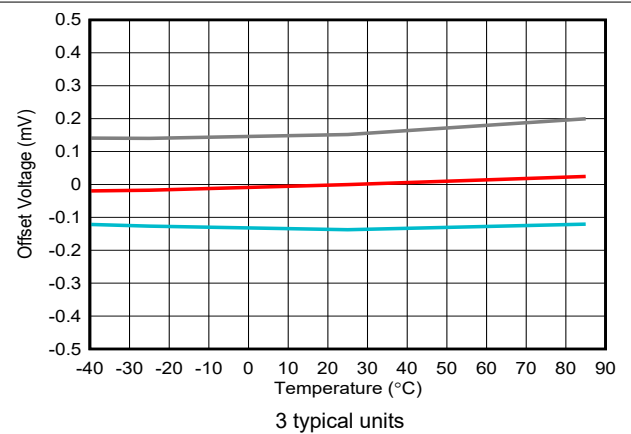
5-21. 1-V Step Response



5-22. 4-V Step Response



5-23. 20-V Step Response



5-24. Input Offset Voltage vs Ambient Temperature

5.10 Typical Characteristics - THS4031 (continued)

at $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{ V}$, gain = +1 V/V, $R_L = 150\ \Omega$, and $R_F = 300\ \Omega$ (unless otherwise noted)

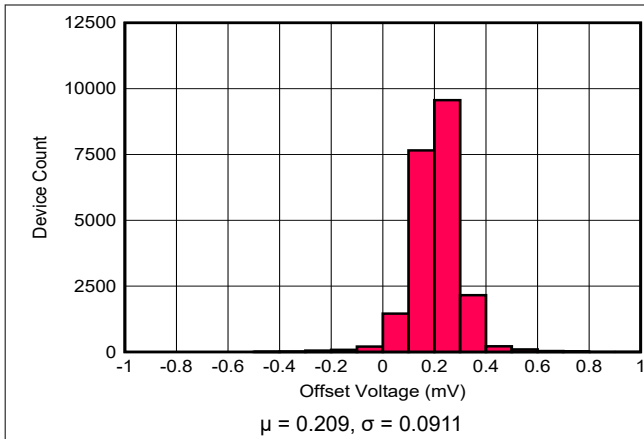


图 5-25. Voltage Offset Distribution

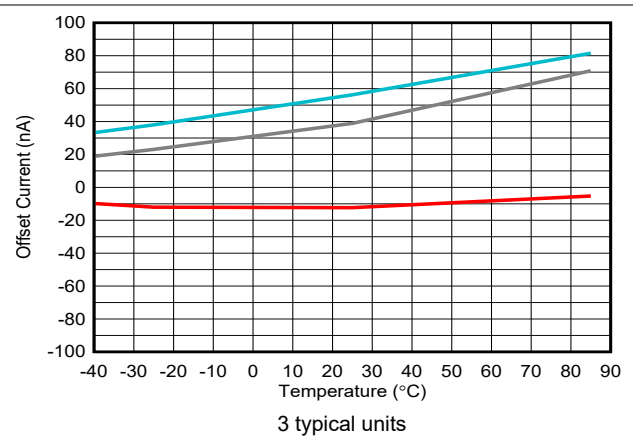


图 5-26. Input Offset Current vs Ambient Temperature

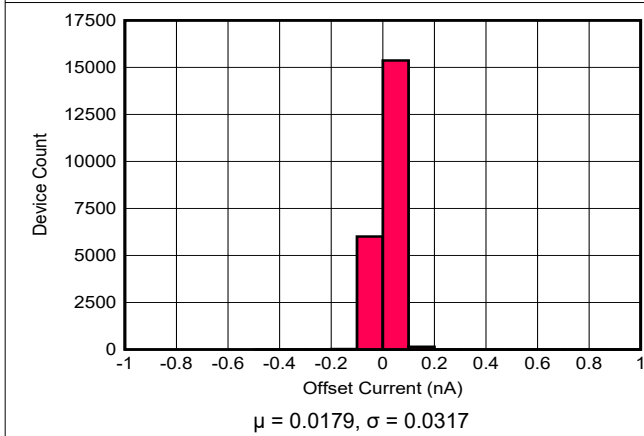


图 5-27. Input Offset Current vs Ambient Temperature

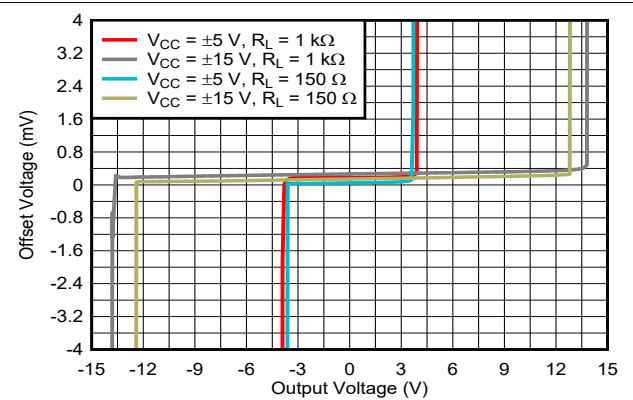


图 5-28. Offset Voltage vs Output Voltage

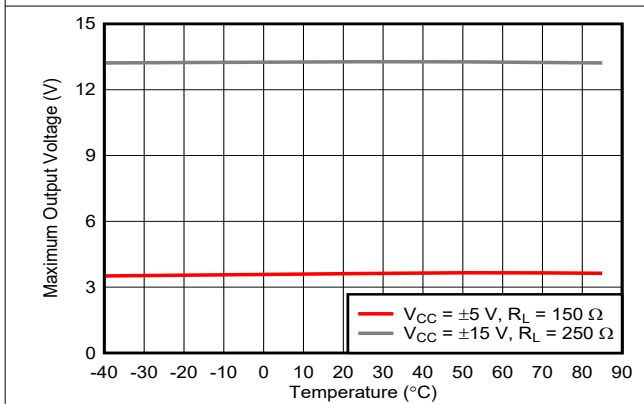


图 5-29. Maximum Output Voltage Swing vs Ambient Temperature

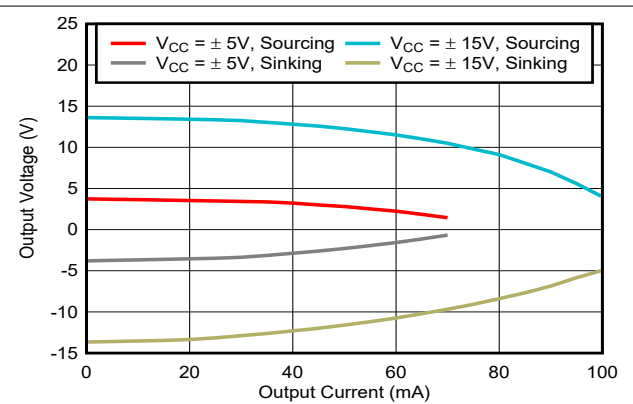


图 5-30. Output Swing vs Load Current

5.10 Typical Characteristics - THS4031 (continued)

at $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{ V}$, gain = +1 V/V, $R_L = 150\ \Omega$, and $R_F = 300\ \Omega$ (unless otherwise noted)

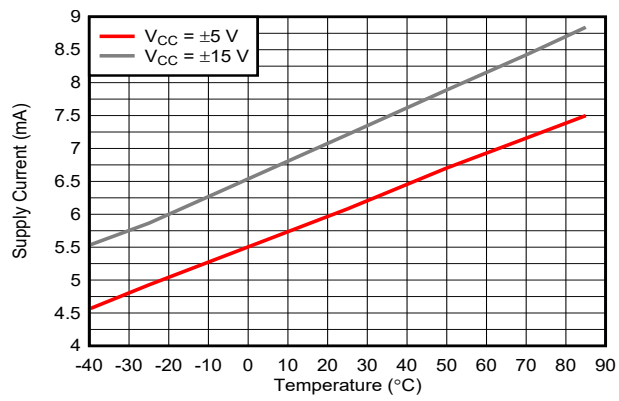
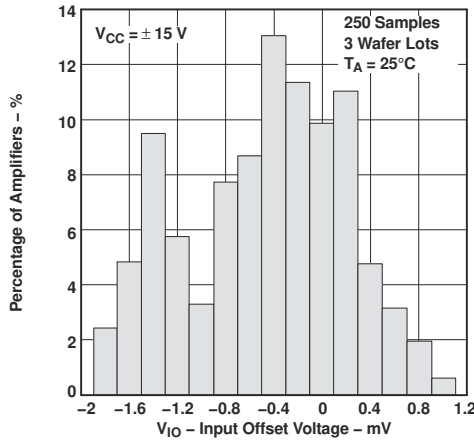
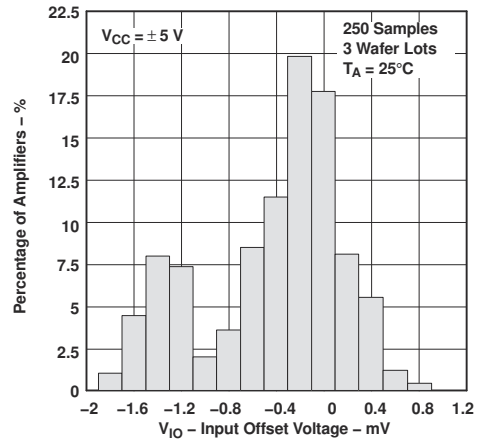


図 5-31. Supply Current vs Ambient Temperature

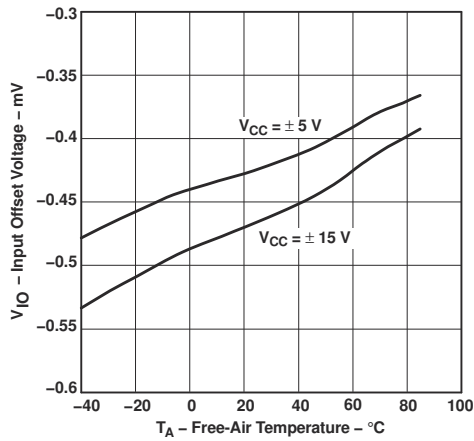
5.11 Typical Characteristics - THS4032



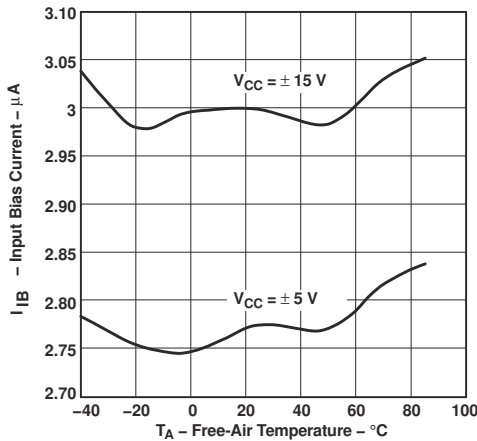
5-32. Input Offset Voltage Distribution



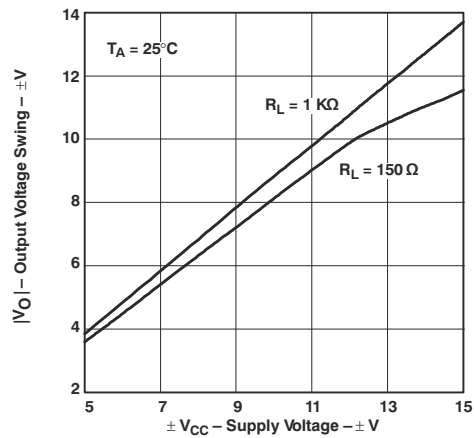
5-33. Input Offset Voltage Distribution



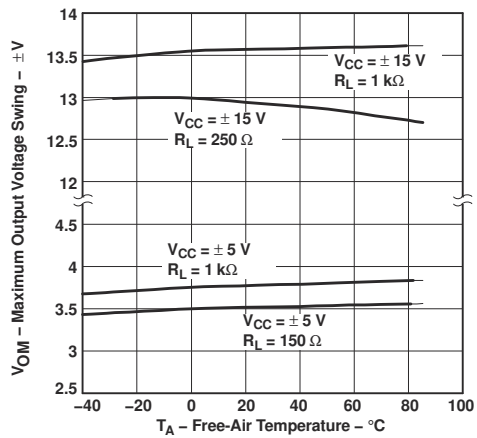
5-34. Input Offset Voltage vs Free-Air Temperature



5-35. Input Bias Current vs Free-Air Temperature

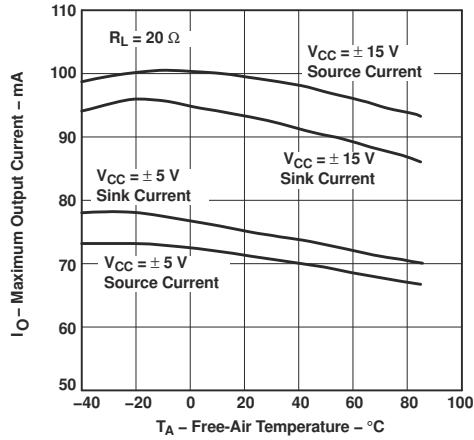


5-36. Output Voltage Swing vs Supply Voltage

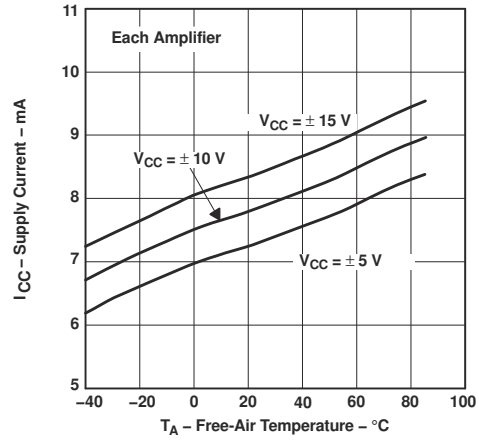


5-37. Maximum Output Voltage Swing vs Free-Air Temperature

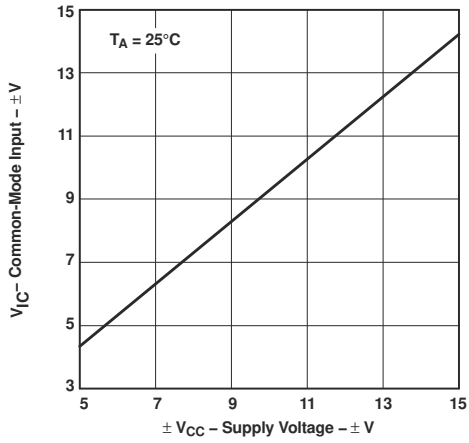
5.11 Typical Characteristics - THS4032 (continued)



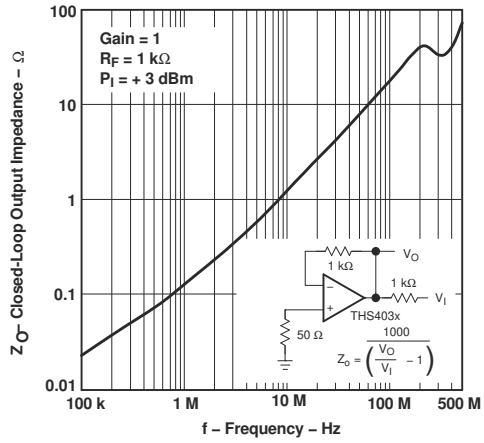
5-38. Maximum Output Current vs Free-Air Temperature



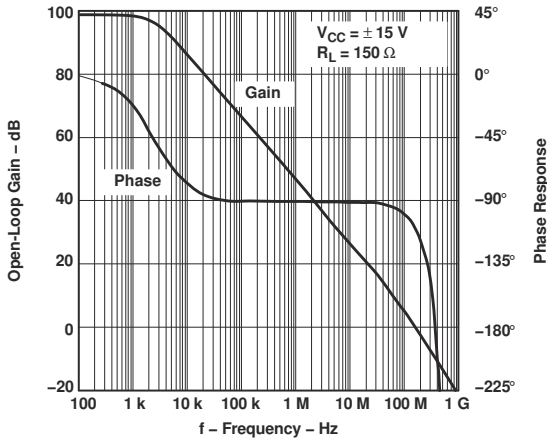
5-39. Supply Current vs Free-Air Temperature



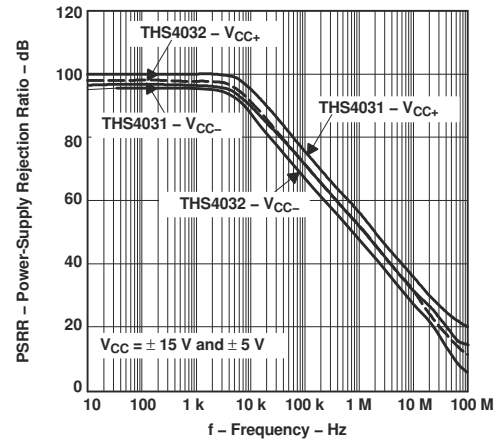
5-40. Common-Mode Input Voltage vs Supply Voltage



5-41. Closed-Loop Output Impedance vs Frequency

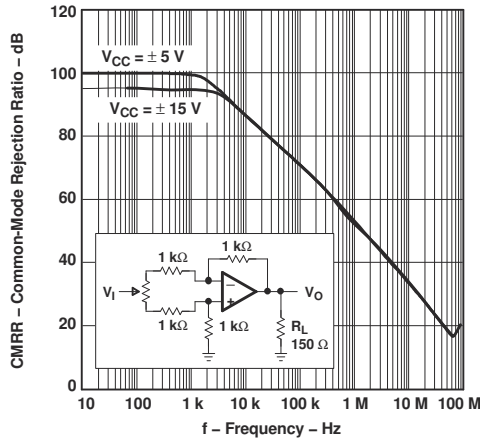


5-42. Open-Loop Gain and Phase Response

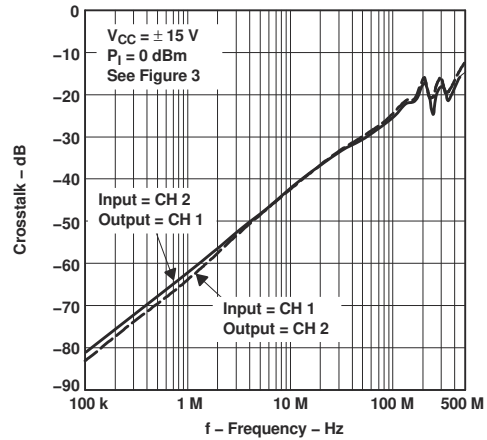


5-43. Power-Supply Rejection Ratio vs Frequency

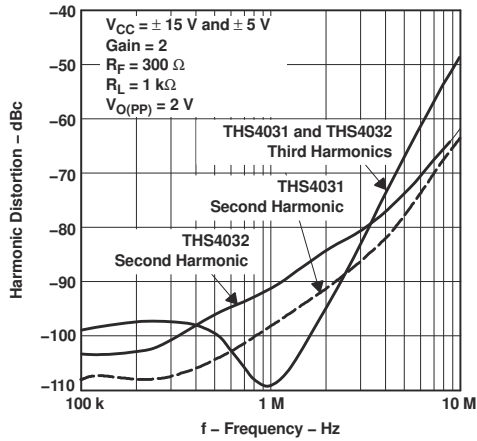
5.11 Typical Characteristics - THS4032 (continued)



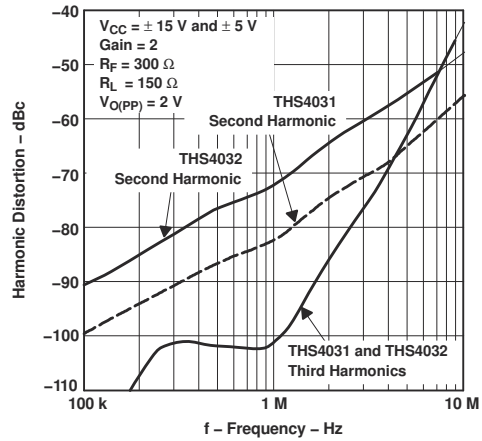
5-44. Common-Mode Rejection Ratio vs Frequency



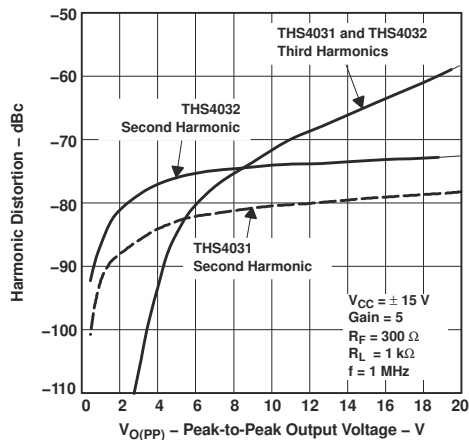
5-45. THS4032 Crosstalk vs Frequency



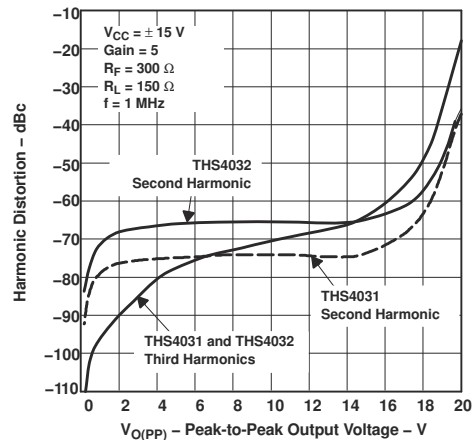
5-46. Harmonic Distortion vs Frequency



5-47. Harmonic Distortion vs Frequency

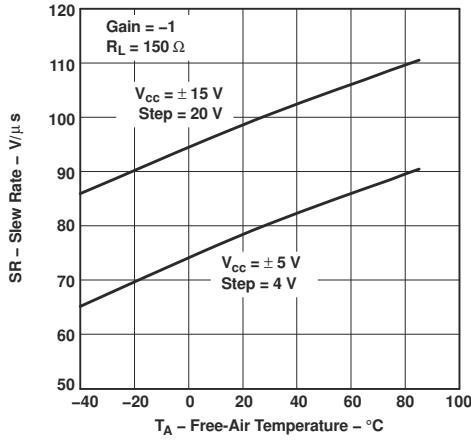


5-48. Harmonic Distortion vs Peak-to-Peak Output Voltage

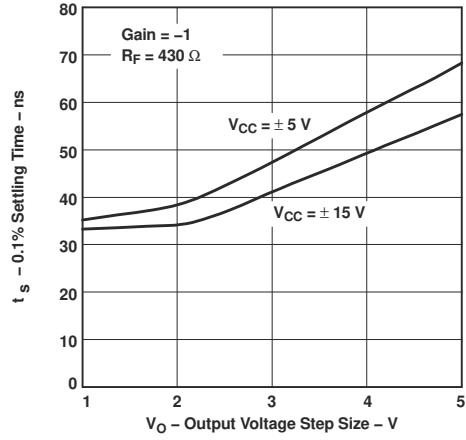


5-49. Harmonic Distortion vs Peak-to-Peak Output Voltage

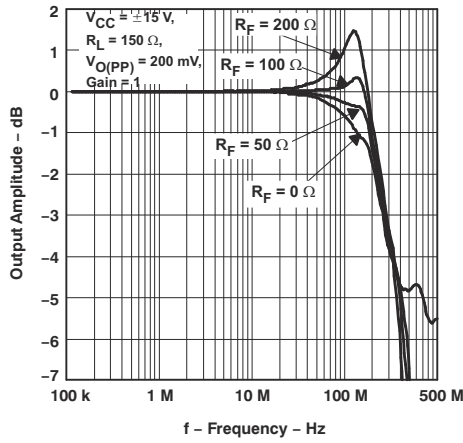
5.11 Typical Characteristics - THS4032 (continued)



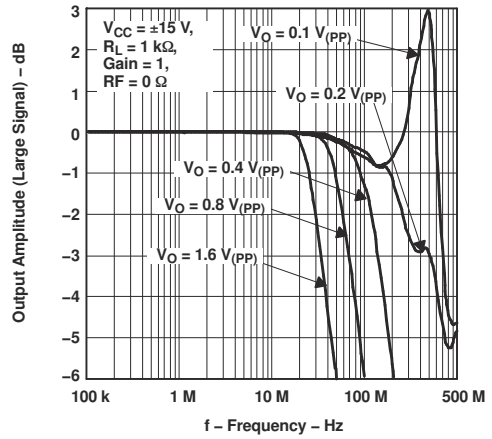
5-50. Slew Rate vs Free-Air temperature



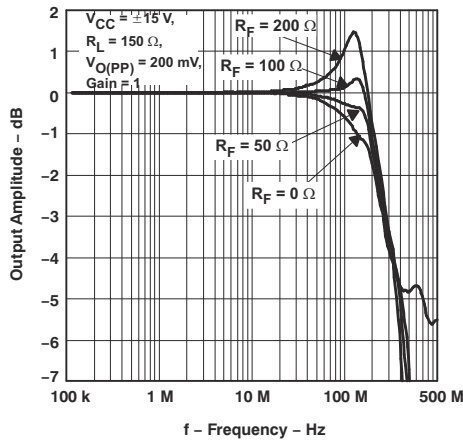
5-51. 0.1% Settling Time vs Output Voltage Step Size



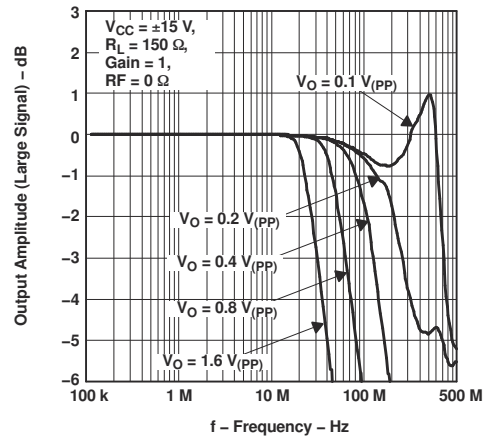
5-52. Small-Signal Frequency Response With Varying Feedback Resistance



5-53. Frequency Response With Varying Output Voltage Swing

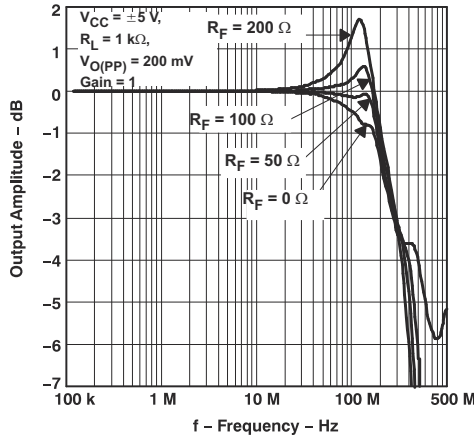


5-54. Small-Signal Frequency Response With Varying Feedback Resistance

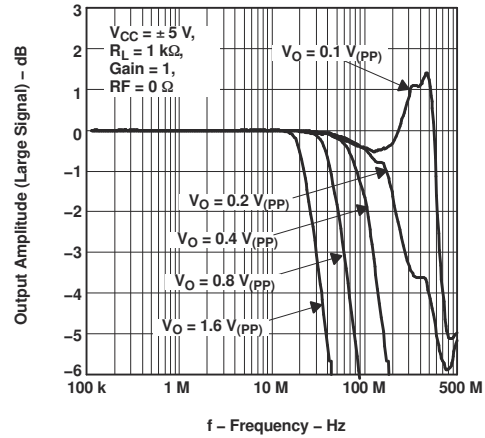


5-55. Frequency Response With Varying Output Voltage Swing

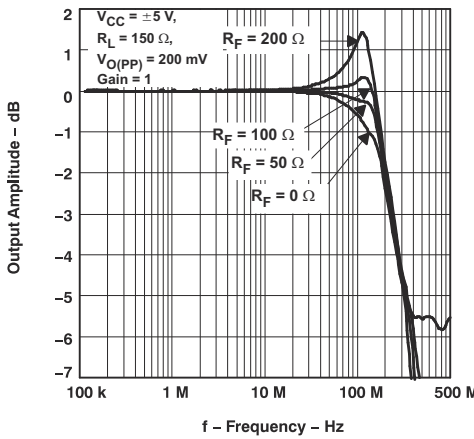
5.11 Typical Characteristics - THS4032 (continued)



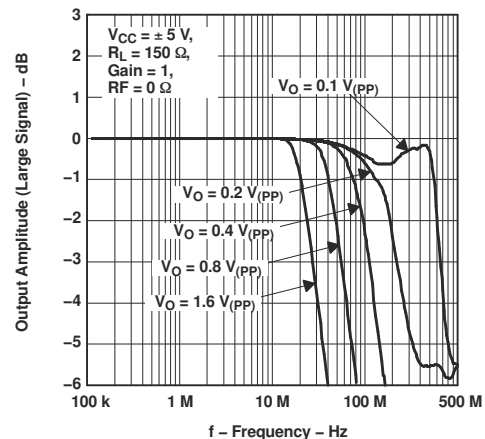
5-56. Small-Signal Frequency Response With Varying Feedback Resistance



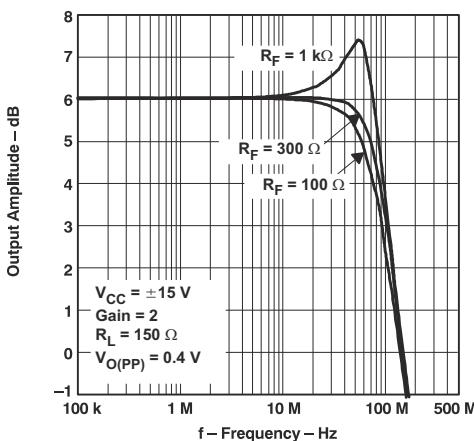
5-57. Frequency Response With Varying Output Voltage Swing



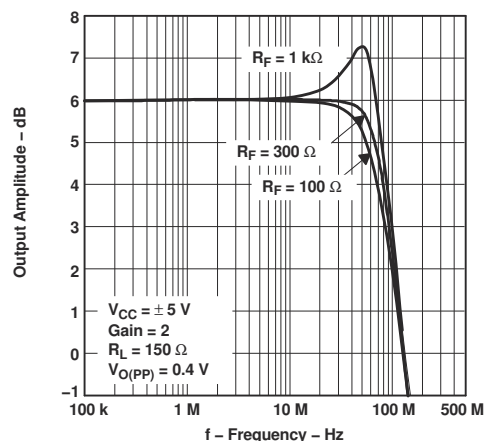
5-58. Small-Signal Frequency Response With Varying Feedback Resistance



5-59. Frequency Response With Varying Output Voltage Swing

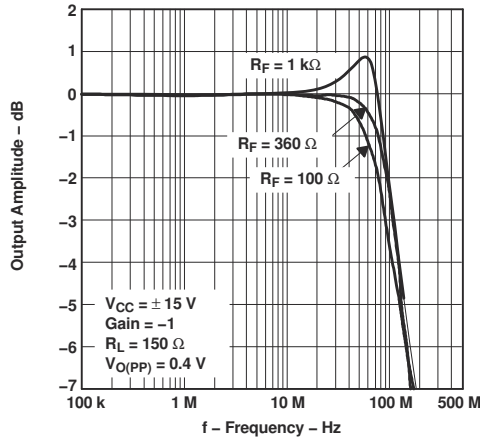


5-60. Small-Signal Frequency Response With Varying Feedback Resistance

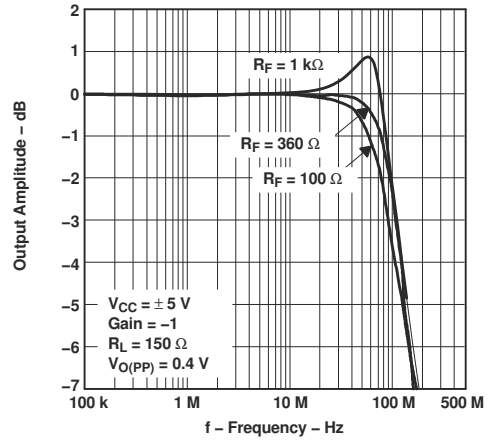


5-61. Small-Signal Frequency Response With Varying Feedback Resistance

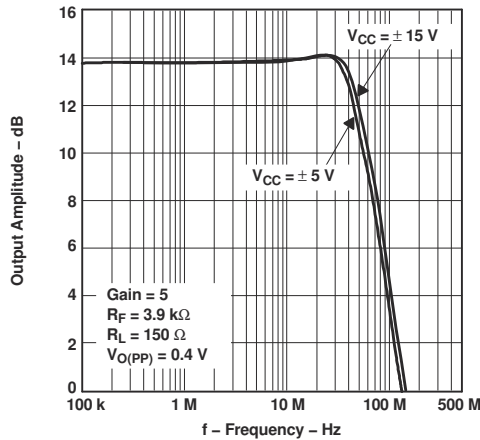
5.11 Typical Characteristics - THS4032 (continued)



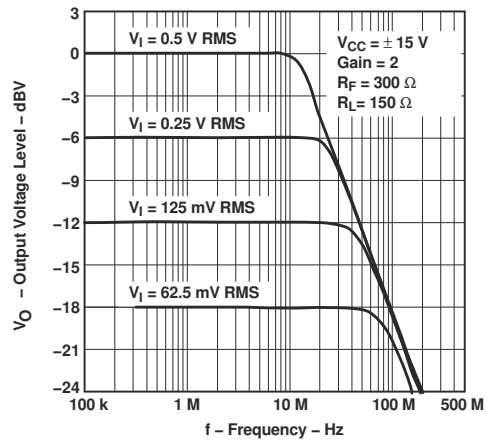
5-62. Small-Signal Frequency Response With Varying Feedback Resistance



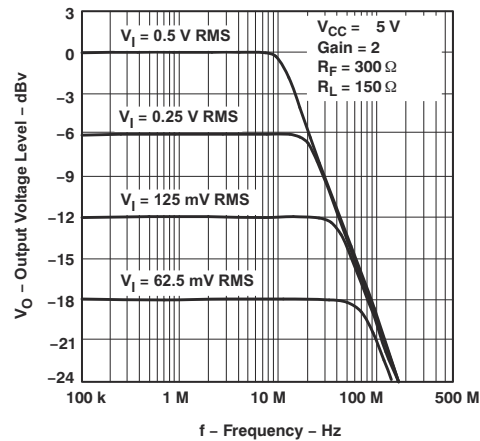
5-63. Small-Signal Frequency Response With Varying Feedback Resistance



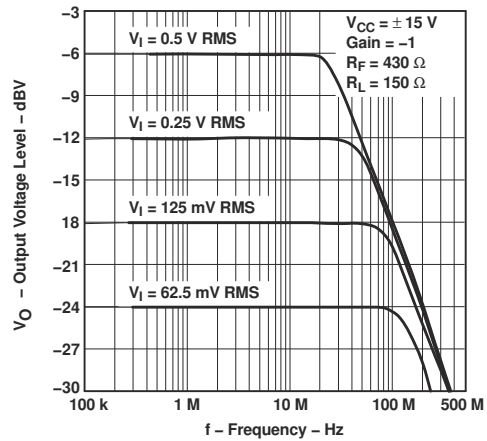
5-64. Small-Signal Frequency Response



5-65. Output Amplitude vs Frequency



5-66. Output Amplitude vs Frequency



5-67. Output Amplitude vs Frequency

5.11 Typical Characteristics - THS4032 (continued)

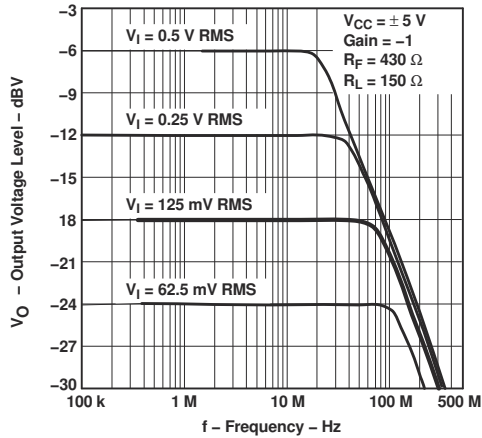


图 5-68. Output Amplitude vs Frequency

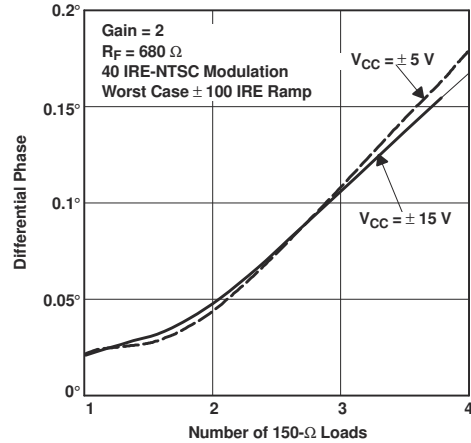


图 5-69. Differential Phase vs Number of 150-Ω Loads

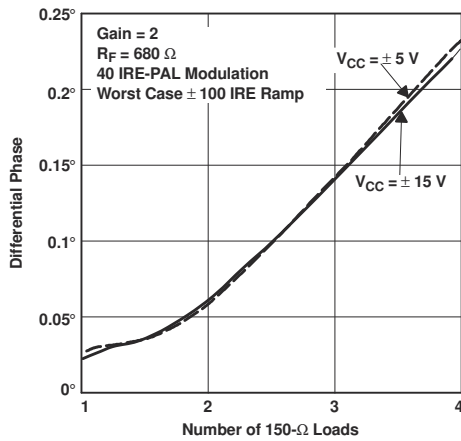


图 5-70. Differential Phase vs Number of 150-Ω Loads

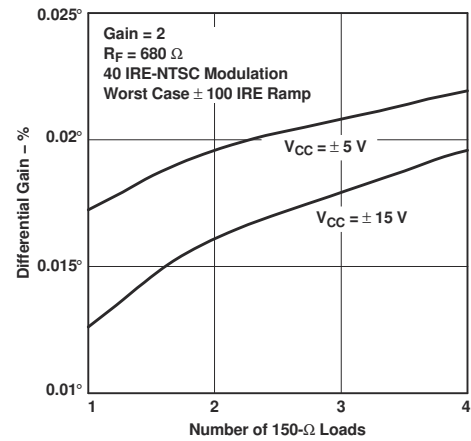


图 5-71. Differential Gain vs Number of 150-Ω Loads

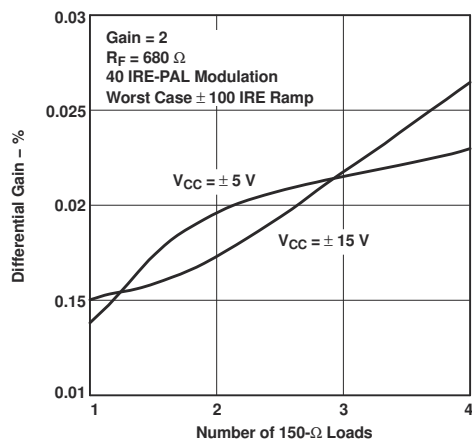


图 5-72. Differential Gain vs Number of 150-Ω Loads

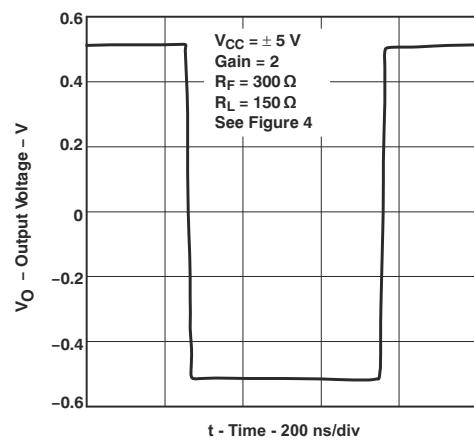


图 5-73. 1-V Step Response

5.11 Typical Characteristics - THS4032 (continued)

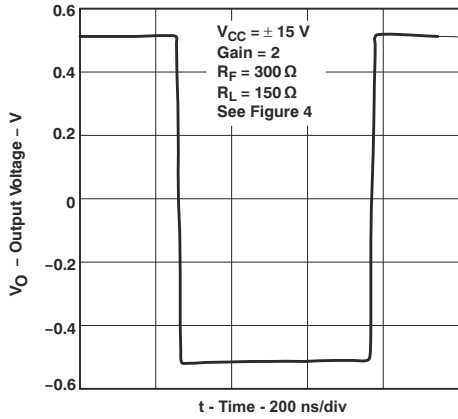


Figure 5-74. 1-V Step Response

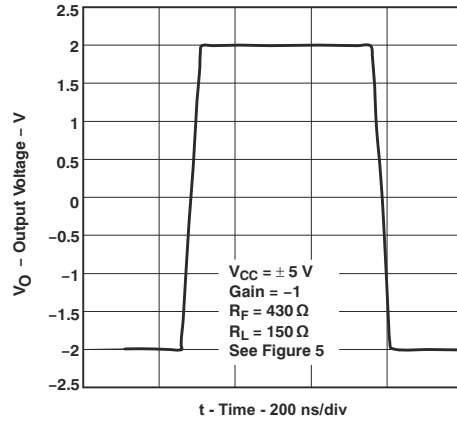


Figure 5-75. 4-V Step Response

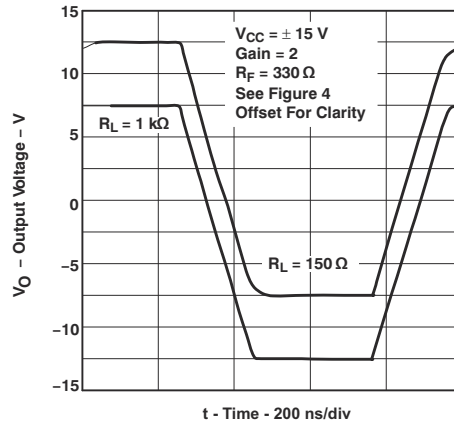


Figure 5-76. 20-V Step Response

6 Detailed Description

6.1 Overview

The THS403x are high-speed operational amplifiers configured in a voltage-feedback architecture. These amplifiers are built using a 30-V, complementary bipolar process with NPN and PNP transistors that possess an f_T of several GHz. This configuration results in exceptionally high-performance amplifiers with wide bandwidth, high slew rate, fast settling time, and low distortion.

6.2 Functional Block Diagrams

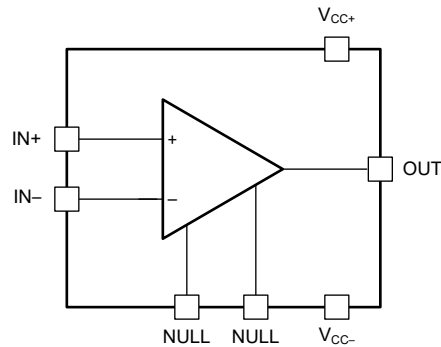


图 6-1. THS4031: Single Channel

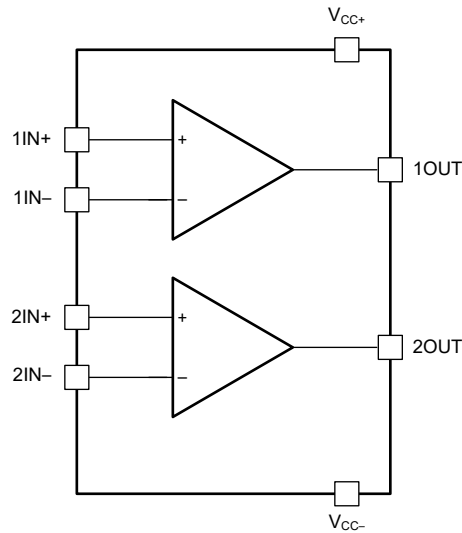


图 6-2. THS4032: Dual Channel

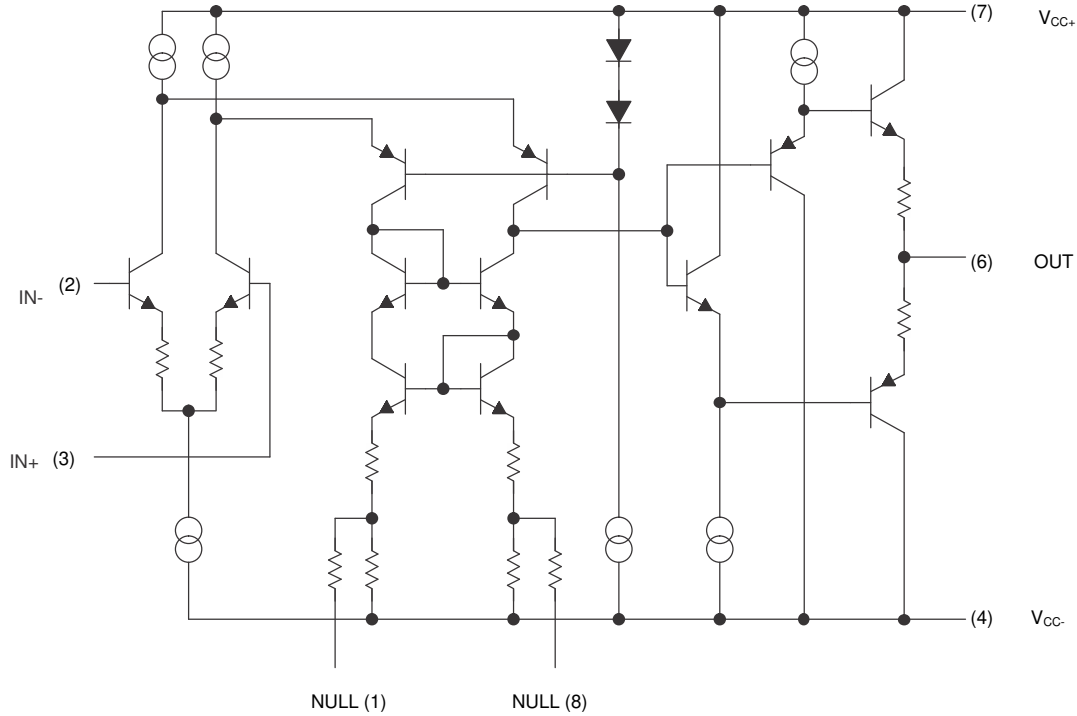


図 6-3. THS4031 Simplified Schematic

6.3 Feature Description

6.3.1 Offset Nulling

The THS403x have a very low input offset voltage for high-speed amplifiers. However, if additional correction is required, an offset nulling function has been provided on the THS4031. To adjust the input offset voltage, place a potentiometer between pin 1 and pin 8 of the device, and tie the wiper to the negative supply. 図 6-4 shows this feature.

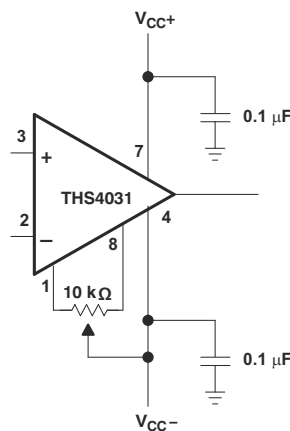


図 6-4. Offset Nulling Schematic

6.4 Device Functional Modes

The THS403x family has a single functional mode and can be used with both single-supply or split power-supply configurations. The power-supply voltage must be greater than 9 V (± 4.5 V) and less than 33 V (± 16.5 V).

7 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

7.1 Application Information

7.1.1 Driving a Capacitive Load

The THS403x devices are internally compensated to maximize bandwidth and slew-rate performance. Take additional precautions when driving capacitive loads with a high-performance amplifier to maintain stability. As a result of the internal compensation, significant capacitive loading directly on the output node decreases the device phase margin, and potentially leads to high-frequency ringing or oscillations. Therefore, for capacitive loads greater than 10 pF, place an isolation resistor in series with the output of the amplifier. [図 7-1](#) shows this configuration. For most applications, a minimum resistance of 20 Ω is recommended. In 75- Ω transmission systems, setting the series resistor value to 75 Ω is a beneficial choice because this value isolates any capacitance loading and provides source impedance matching.

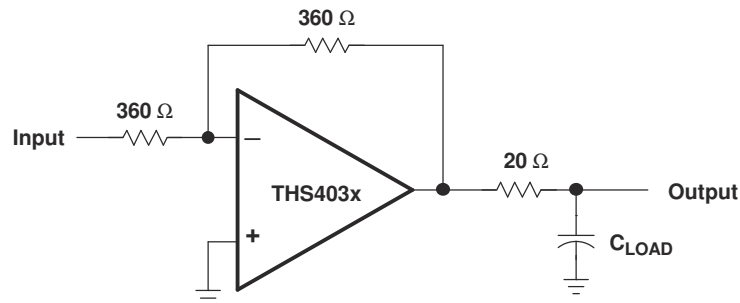


図 7-1. Driving a Capacitive Load

7.1.2 Low-Pass Filter Configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. [Figure 7-2](#) shows that the simplest way to accomplish this limiting is to place an RC filter at the noninverting pin of the amplifier.

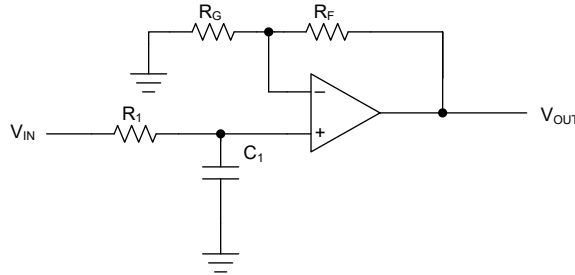


Figure 7-2. Single-Pole Low-Pass Filter

$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right) \times \left(\frac{1}{1 + sR_1C_1}\right) \quad (1)$$

If more attenuation at higher frequencies is required, a multiple-pole filter is required. [Figure 7-3](#) shows a common implementation of a second-order filter called a Sallen-Key filter. When designing this type of filter, choose an amplifier whose bandwidth is approximately an order of magnitude larger than the desired filter bandwidth. See [Active Low-pass Filter Design](#) for more detailed active-filter design information.

Assuming $R_1 = R_2 = R$ and $C_1 = C_2 = C$, use [Equation 2](#) to set the bandwidth of the filter.

$$f_{3dB} = \frac{1}{2\pi RC} \quad (2)$$

The Q-factor of a filter controls the amount of peaking of the small-signal frequency response and the settling time of the pulse response. Set Q to 0.707 to provide a Butterworth response with a maximally flat pass band. Use [Equation 3](#) to choose the ratio of R_F and R_G to obtain the desired Q value.

$$\frac{R_F}{R_G} = 2 - \frac{1}{Q} \quad (3)$$

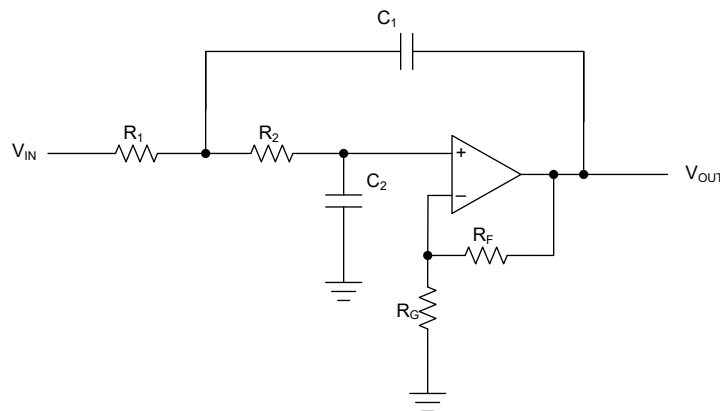


Figure 7-3. Two-Pole Low-Pass Sallen-Key Filter

7.2 Typical Application

This section demonstrates multiplexing several analog input signals to a high-performance driver amplifier which subsequently drives a single high-resolution, high-speed SAR analog-to-digital converter (ADC). This example uses the [ADS8411](#) and the [TS5A3159](#) or [TS5A3359](#) as the ADC and the multiplexer, respectively. This application uses the THS403x as the operational amplifier.

As detailed in [Figure 7-4](#), the example system consists of an ADC (ADS8411), a driving operational amplifier (THS4031), a multiplexer (TS5A3159), an ac source, a dc source, and two driving operational amplifiers.

The driving amplifiers OPA1 and OPA2 are shown as two THS4031 amplifiers. Alternatively, use a single THS4032 to save on cost and board space. The purpose of these op-amps is make the input sources present a low impedance to rest of the circuit. Additionally, to maintain signal fidelity, these operational amplifiers must have low noise and distortion. The third THS4031 labeled OPA3 in [Figure 7-4](#) is used to maintain switching speed and drive the ADC. The passive band-pass filter before the ADC reduces unwanted noise.

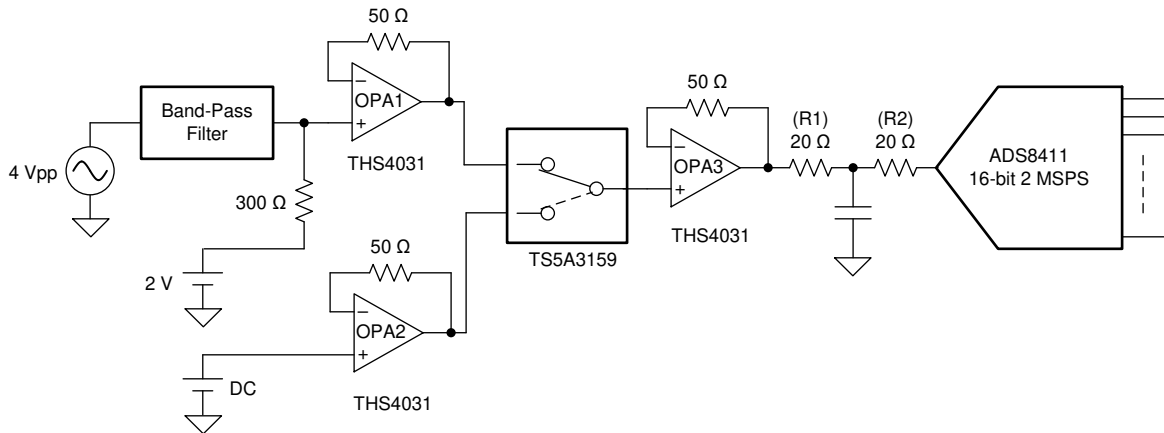


Figure 7-4. Multiplexing Setup to Drive a High-Performance ADC

7.2.1 Design Requirements

The objective is to design a multiplexed digitizer system with the dynamic performance shown in [Table 7-1](#).

Table 7-1. Design Specifications

DEVICE SPEED (MSPS)	INPUT FREQUENCY (kHz)	SNR (dB)	THD (dB)	CROSSTALK (dB)
2	20	> 84	< -90	< -110
2	100	> 84	< -90	< -96

7.2.2 Detailed Design Procedure

The ADS8411 is a 16-bit, 2-MSPS analog-to-digital converter (ADC) with a 4-V reference. The ADS8411 has a unipolar single-ended input and includes a 16-bit capacitor-based SAR ADC, with inherent sample and hold. The output is a 16-bit parallel interface.

The TS5A3159 is a single-pole, double-throw (SPDT) analog switch that is designed to operate from 1.65 V to 5.5 V. The TS5A3159 offers a low ON state resistance and an excellent ON resistance matching with the break-before-make feature to prevent signal distortion during the transfer of a signal from one channel to another. Additionally, the TS5A3159 provides excellent total harmonic distortion (THD) performance and consumes low power. The TS5A3359 is a single-pole, triple-throw (SP3T) version of the same switch.

7.2.2.1 Selection of Multiplexer

Figure 7-5 shows an equivalent circuit diagram of one of the channels of a multiplexer. C_S is the input capacitance of the channel; C_D is the output capacitance of the channel. R_{ON} is the resistance of the channel when the channel is turned ON. C_L and R_L are the load capacitance and resistance, respectively. V_{IN} is the input voltage of the source. R_S is the resistance of the source. V_{OUT} is the output voltage of the multiplexer.

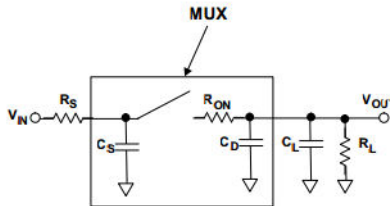


Figure 7-5. Multiplexer Equivalent Circuit

Settling time is improved when the values of R_S , R_{ON} , C_S , C_D , and C_L are small, and the value of R_L is large.

For TS5A3159:

- $R_{ON} = 1 \Omega$
- $C_S = C_D = 84 \text{ pF}$

Typical values for the extrinsic parameters are

- $R_S = 50 \Omega$
- $C_L = 5 \text{ pF}$
- $R_L = 10 \text{ k}\Omega$
- T_{RC} (time constant) = 8.65 ns

For a 16-bit system, at least 18-bit settling is desired to minimize distortion from settling artifacts. For an 18-bit settling, the circuit response time required is $(18 \times \ln 2) \times T_{RC} = 108 \text{ ns}$, which is less than 2 MSPS sampling time of 500 ns. If the settling time is more than the conversion time of the ADC, the output of the multiplexer does not settle to the required accuracy resulting in distortion.

One more important parameter to consider when selecting a multiplexer is the on-state resistance variation with voltage. This variation also affects distortion because R_{ON} and R_L act like a resistor divider circuit. Any variation of R_{ON} with voltage affects the output voltage.

7.2.2.2 Signal Source

The input signal source must be a low-noise, low-distortion source with low source resistance. As discussed in the earlier section, the source resistance also must be small to avoid impacting settling time. If the source is not a low-noise and low-distortion source, a passive band-pass filter can be added to improve the signal quality as shown in Figure 7-4.

7.2.2.3 Driving Amplifier

The driving operational amplifier (OPA3 in Figure 7-4) in this application must have good slew rate, bandwidth, low noise, and distortion. The input of the operational amplifier can result in a maximum step of 4-V because of MUX switching. As a result, even if the signal bandwidth is low, the driving amplifier must settle from a 4-V step within one ADC sampling frame to avoid signal distortion. In this example, the settling requirement due to the ADC selection is 500 ns. The THS4031 is a good choice in this application due to the high slew rate and low distortion of this operational amplifier.

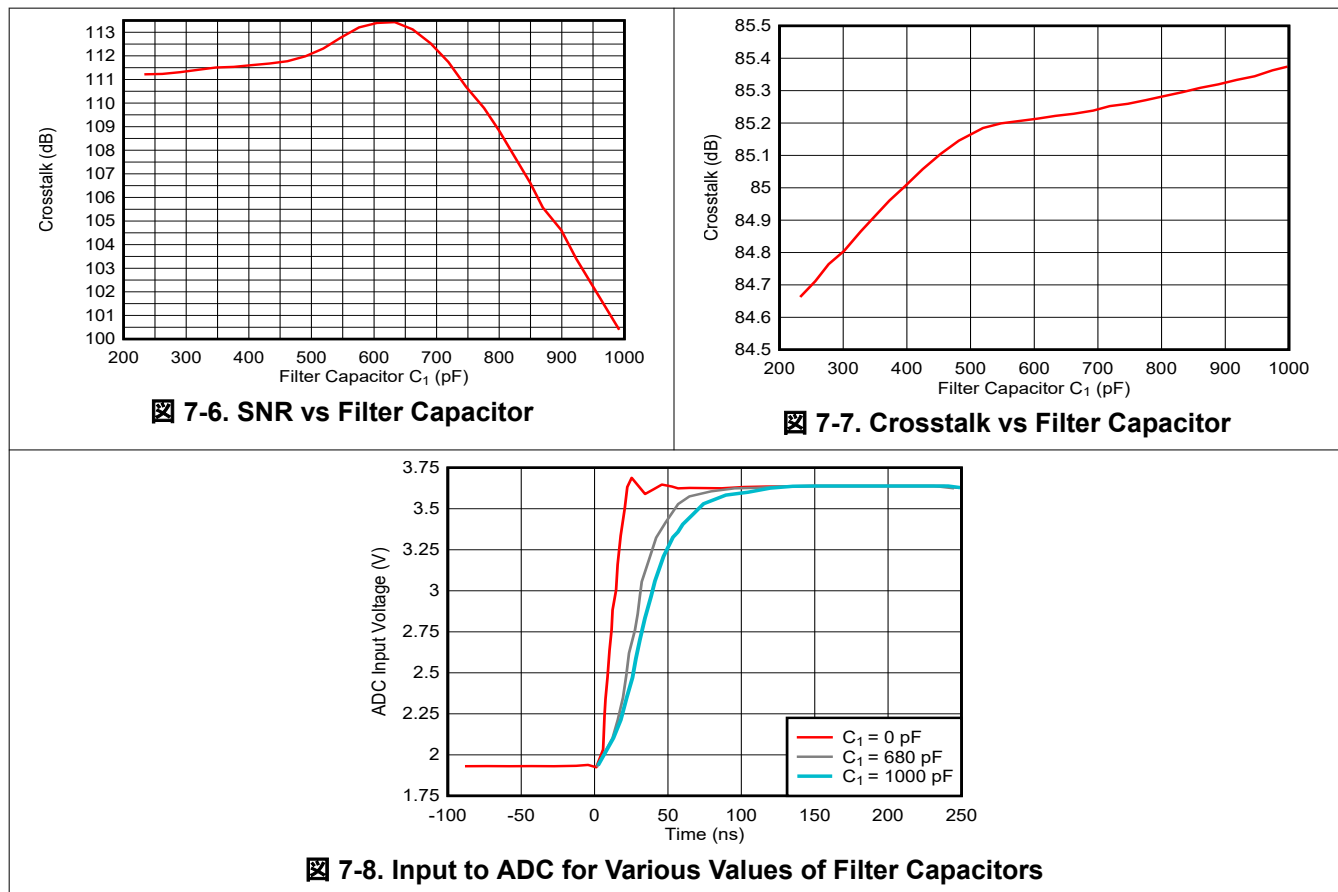
7.2.2.4 Driving Amplifier Bandwidth Restriction

The restriction of excess bandwidth by use of a passive RC filter before the ADC results in better SNR and THD. However, restricting the bandwidth too much results in a excessive operational amplifier settling time. If the amplifier output does not settle quick enough, some residual charge of the previous channel remains in the next sampling interval and appears as crosstalk. One approach to solve this settling issue is to reduce the throughput of the ADC. However, often the high sample rate ADC was chosen to the need to acquire higher frequency signals limiting the freedom to reduce the ADC throughput. Due to these tradeoffs, the choice of the filter capacitor becomes critical. [Figure 7-6](#) and [Figure 7-7](#) show SNR and crosstalk as a function of the filter capacitor.

[Figure 7-8](#) shows input settling behavior with three different filter capacitor values. The value of the capacitor changes to filter bandwidth. As the filter bandwidth increases, the settling time improves as shown in [Equation 4](#).

$$\text{Filter Bandwidth} \cong \frac{1}{2\pi R_1 C_1} \tag{4}$$

7.2.3 Application Curves



7.3 Power Supply Recommendations

The THS403x family operates off a single supply or with dual supplies. Choose supplies that provide for the required headroom to supply rails as specified by the common-mode input range (CMIR). Operating from a single supply has numerous advantages. With the negative supply at ground, the dc errors due to the $-PSRR$ term are minimized. Decouple supplies with low inductance capacitors to ground as close to the amplifier as possible. When operating on a board with high-speed digital signals, provide isolation between digital signal noise and the analog input pins. When using a ground plane, remove the ground plane close to input sensitive pins to reduce stray parasitics that adversely impact device performance. For split-supply operation, an optional supply decoupling capacitor across the two power supplies improves second harmonic distortion performance.

7.4 Layout

7.4.1 Layout Guidelines

To achieve the levels of high-frequency performance of the THS403x, follow proper printed-circuit board (PCB), high-frequency design techniques. The following is a general set of guidelines. In addition, a THS403x evaluation board is available to use as a guide for layout or for evaluating the device performance.

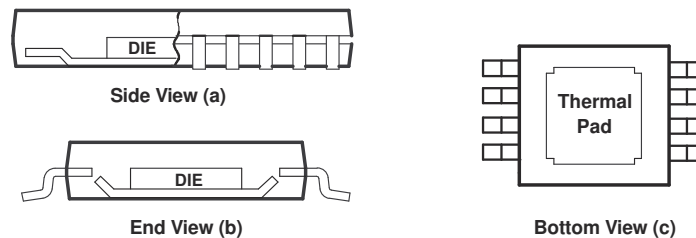
- **Ground planes**—make sure that the ground plane used on the board provides all components with a low-inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize stray capacitance.
- **Proper power-supply decoupling**—use a 6.8- μF tantalum capacitor in parallel with a 0.1- μF ceramic capacitor on each supply pin. Sharing the tantalum capacitor among several amplifiers is possible depending on the application, but always use a 0.1- μF ceramic capacitor on the supply pin of every amplifier. In addition, place the 0.1- μF capacitor as close as possible to the supply pin. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. Strive for distances of less than 0.1 inch (2.54 mm) between the device power pins and the ceramic capacitors.
- **Short trace runs or compact part placements**—optimum high-frequency performance is achieved when stray series inductance is minimized. To minimize stray inductance, make the circuit layout as compact as possible, thereby minimizing the length of all trace runs. Pay particular attention to the inputs of the amplifier, keeping the trace lengths as short as possible. This layout helps to minimize stray capacitance at the input of the amplifier.
- **Sockets**—TI does not recommend sockets for high-speed operational amplifiers. The additional lead inductance in the socket pins often leads to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- **Short trace runs and compact part placements**—Improved high-frequency performance is achieved when stray series inductance is minimized. To reduce stray series inductance, the circuit layout must be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention must be paid to the inverting input of the amplifier. The length must be kept as short as possible to minimize stray capacitance at the input of the amplifier.

7.4.1.1 General PowerPAD™ Integrated Circuit Package Design Considerations

The THS403x are available in a thermally-enhanced DGN package, which is a member of the PowerPAD™ integrated circuit package family. This package is constructed using a downset lead frame upon which the die is mounted [see [Figure 7-9\(a\)](#) and [Figure 7-9\(b\)](#)]. This arrangement results in the lead frame exposed as a thermal pad on the underside of the package [see [Figure 7-9\(c\)](#)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD integrated circuit package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are soldered), the thermal pad can be soldered to a copper area under the package. By using thermal paths within this copper area, heat is conducted away from the package into a ground plane or other heat-dissipating device.

The PowerPAD integrated circuit package represents a breakthrough in combining the small area and ease of assembly of surface mount with the more-recent, awkward mechanical methods of sinking heat.



Note: The thermal pad is electrically isolated from all pins in the package.

Figure 7-9. Views of Thermally-Enhanced DGN Package

Although there are many ways to properly dissipate heat from this device, the following steps show the recommended approach.

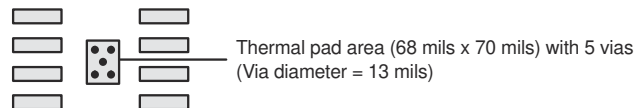
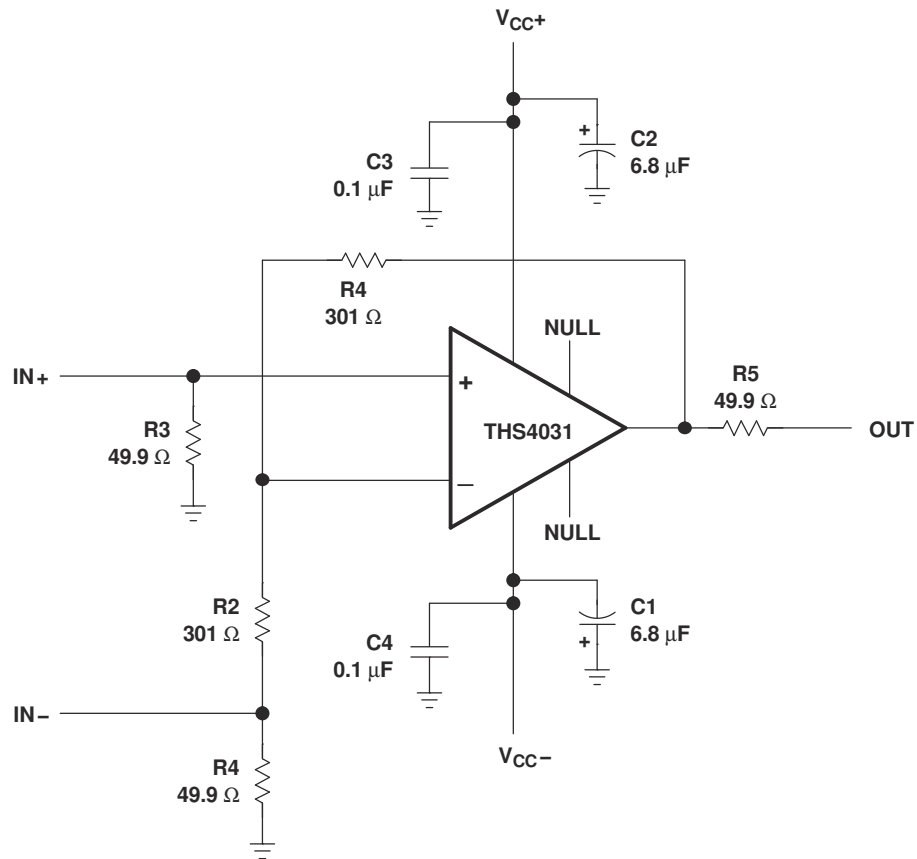


Figure 7-10. PowerPAD™ PCB Etch and Via Pattern

1. Prepare the PCB with a top-side etch pattern as shown in [Figure 7-10](#). There must be etch for the leads as well as etch for the thermal pad.
2. Place five holes in the area of the thermal pad. These holes must be 13 mils (0.3302 mm) in diameter. The reason to keep the holes small is to discourage solder wicking through the holes during reflow.
3. Additional vias can be placed anywhere along the thermal plane outside of the thermal pad area. This action helps dissipate the heat generated by the THS403x device. The additional vias can be of any diameter because wicking is not a concern outside of the thermal pad area.
4. Connect all holes to the internal ground plane.
5. When connecting these holes to the ground plane, *do not* use the typical web or spoke via connection methodology. Web connections have a high thermal-resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS403x package must connect to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask must leave the pins of the package and the thermal pad area with the five holes exposed. The bottom-side solder mask must cover the five holes of the thermal pad area, which prevents solder from pulling away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and to all the device pins.
8. With these preparatory steps in place, the THS403x device is placed in position and run through the solder reflow operation as any standard surface-mount component.

7.4.2 Layout Example



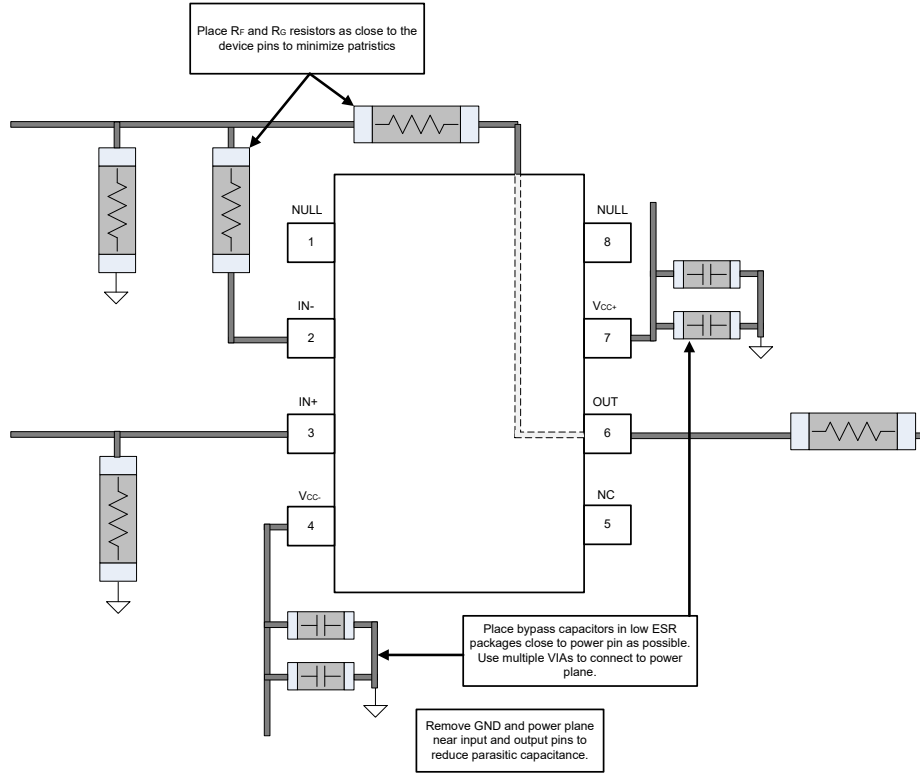


图 7-11. Layout Recommendations

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Noise Analysis for High-Speed Op Amps](#), application report
- Texas Instruments, [PowerPAD™ Thermally-Enhanced Package](#), application report
- Texas Instruments, [THS4031 High-Speed Op Amp](#), EVM user's guide
- Texas Instruments, [THS4032 Dual High-Speed Op Amp](#), EVM user's guide

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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8.5 静電気放電に関する注意事項



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8.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision J (February 2024) to Revision K (May 2024)	Page
Deleted Total harmonic distortion + noise and Intermodulation distortion specifications from <i>Electrical Characteristics - THS4031, R_L = 150 Ω</i>	6
Deleted Total harmonic distortion + noise and Intermodulation distortion specifications from <i>Electrical Characteristics - THS4031, R_L = 1 kΩ</i>	7
Changed gain from +2 V/V to +1 V/V in <i>Typical Characteristics - THS4031</i>	12
Changed abscissa axis label from 10 ns/div to 100 ns/div in Figure 5-23, <i>20V Step Response</i>	12

Changes from Revision I (May 2018) to Revision J (February 2024)	Page
ドキュメント全体にわたって表、図、相互参照の採番方法を更新.....	1

• Changed table note 1 in <i>Absolute Maximum Ratings</i> to add additional clarification.....	4
• Changed output current max in <i>Absolute Maximum Ratings</i> from 150 mA to 240 mA.....	4
• Changed differential supply voltage in <i>Absolute Maximum Ratings</i> from ± 4 V to ± 1.5 V.....	4
• Added continuous input current in <i>Absolute Maximum Ratings</i>	4
• Deleted M-suffix temperature range and in <i>Absolute Maximum Ratings</i>	4
• Deleted JG and FK package references in <i>Absolute Maximum Ratings</i>	4
• Changed charged-device model (CDM) reference from JESD22-C101 to JS-002 in <i>ESD Ratings</i>	4
• Updated <i>Thermal Information: THS4031</i> for the D and DGN packages.....	5
• Deleted full-power bandwidth specification from <i>Electrical Characteristics - THS4031, $R_L = 150 \Omega$</i>	6
• Added <i>Electrical Characteristics - THS4031, $R_L = 150 \Omega$</i> section.....	6
• Changed bandwidth for 0.1-dB flatness in <i>Electrical Characteristics - THS4031, $R_L = 150 \Omega$</i> from 50 MHz to 9 MHz for $V_{CC} = \pm 15$ V.....	6
• Changed bandwidth for 0.1-dB flatness in <i>Electrical Characteristics - THS4031, $R_L = 150 \Omega$</i> from 45 MHz to 9 MHz for $V_{CC} = \pm 5$ V.....	6
• Changed settling time to 0.1% in <i>Electrical Characteristics - THS4031, $R_L = 150 \Omega$</i> from 60 ns to 70 ns for $V_{CC} = \pm 15$ V.....	6
• Changed settling time to 0.1% in <i>Electrical Characteristics - THS4031, $R_L = 150 \Omega$</i> from 45 ns to 55 ns for $V_{CC} = \pm 5$ V.....	6
• Deleted total harmonic distortion for 1 k Ω in <i>Electrical Characteristics - THS4031, $R_L = 150 \Omega$</i>	6
• Changed input voltage noise - in <i>Electrical Characteristics - THS4031, $R_L = 150 \Omega$</i> from 1.6 nV/ $\sqrt{\text{Hz}}$ to 1.2 nV/ $\sqrt{\text{Hz}}$	6
• Changed input current noise in <i>Electrical Characteristics - THS4031, $R_L = 150 \Omega$</i> from 1.2 pA/ $\sqrt{\text{Hz}}$ to 2.3 pA/ $\sqrt{\text{Hz}}$	6
• Changed open loop gain condition in <i>Electrical Characteristics - THS4031, $R_L = 150 \Omega$</i> from 1 k Ω to 150 Ω	6
• Changed open loop gain minimum in <i>Electrical Characteristics - THS4031, $R_L = 150 \Omega$</i> from 98 dB to 100 dB for $V_{CC} = \pm 15$ V, $T_A = 25$ $^{\circ}\text{C}$	6
• Changed open loop gain minimum specification in <i>Electrical Characteristics - THS4031, $R_L = 150 \Omega$</i> from 95 dB to 98 dB for $V_{CC} = \pm 5$ V, $T_A = 25$ $^{\circ}\text{C}$	6
• Updated input offset voltage values and units specification in <i>Electrical Characteristics - THS4031, $R_L = 150 \Omega$</i>	6
• Added input offset current specification in <i>Electrical Characteristics - THS4031, $R_L = 150 \Omega$</i> table.....	6
• Changed common-mode input voltage range typical in <i>Electrical Characteristics - THS4031, $R_L = 150 \Omega$</i> from ± 14 V to ± 14.3 V for $V_{CC} = \pm 15$ V.....	6
• Changed common-mode input voltage range typical in <i>Electrical Characteristics - THS4031, $R_L = 150 \Omega$</i> from ± 4 V to ± 4.3 V for $V_{CC} = \pm 5$ V.....	6
• Deleted output voltage swing for $R_L = 1$ k Ω in <i>Electrical Characteristics - THS4031, $R_L = 150 \Omega$</i>	6
• Changed output voltage swing condition for $V_{CC} = \pm 15$ V in <i>Electrical Characteristics - THS4031, $R_L = 150 \Omega$</i> from 150 Ω to 250 Ω	6
• Changed output voltage swing condition for $V_{CC} = \pm 5$ V in <i>Electrical Characteristics - THS4031, $R_L = 150 \Omega$</i> from 250 Ω to 150 Ω	6
• Deleted short circuit current in <i>Electrical Characteristics - THS4031, $R_L = 150 \Omega$</i>	6
• Changed output current load resistance typical in <i>Electrical Characteristics - THS4031, $R_L = 150 \Omega$</i> from 20 Ω to 10 Ω	6
• Changed output current typical in <i>Electrical Characteristics - THS4031, $R_L = 150 \Omega$</i> from 90 mA to 200 mA for $V_{CC} = \pm 15$ V.....	6
• Changed output current typical in <i>Electrical Characteristics - THS4031, $R_L = 150 \Omega$</i> from 70 mA to 160 mA for $V_{CC} = \pm 5$ V.....	6
• Changed output resistance typical in <i>Electrical Characteristics - THS4031, $R_L = 150 \Omega$</i> from 13 Ω to 5 Ω	6
• Changed supply current (each amplifier) typical in <i>Electrical Characteristics - THS4031, $R_L = 150 \Omega$</i> from 8.5 mA to 7.5 mA for $V_{CC} = \pm 15$ V.....	6
• Changed supply current (each amplifier) typical in <i>Electrical Characteristics - THS4031, $R_L = 150 \Omega$</i> from 7.5 mA to 6.5 mA for $V_{CC} = \pm 5$ V.....	6

• Changed bandwidth for 0.1-dB flatness in <i>Electrical Characteristics - THS4031</i> , $R_L = 1\text{ k}\Omega$ from 50 MHz to 9 MHz for $V_{CC} = \pm 15\text{ V}$	7
• Changed bandwidth for 0.1-dB flatness in <i>Electrical Characteristics - THS4031</i> , $R_L = 1\text{ k}\Omega$ from 45 MHz to 9 MHz for $V_{CC} = \pm 5\text{ V}$	7
• Changed full power bandwidth calculation from slew rate / $[\sqrt{10}V_{OC(Peak)}]$ to slew rate / $[\pi V_{O(P-P)}]$ in <i>Electrical Characteristics - THS4031</i> , $R_L = 1\text{ k}\Omega$	7
• Changed full power bandwidth in <i>Electrical Characteristics - THS4031</i> , $R_L = 1\text{ k}\Omega$ from 2.3 to 1.6 for $V_{CC} = \pm 15\text{ V}$	7
• Changed full power bandwidth specification in <i>Electrical Characteristics - THS4031</i> , $R_L = 1\text{ k}\Omega$ from 7.1 to 5.1 for $V_{CC} = \pm 5\text{ V}$	7
• Changed 0.1% setting time in <i>Electrical Characteristics - THS4031</i> , $R_L = 1\text{ k}\Omega$ from 60 to 70 for $V_{CC} = \pm 15\text{ V}$	7
• Changed 0.1% setting time in <i>Electrical Characteristics - THS4031</i> , $R_L = 1\text{ k}\Omega$ from 45 to 55 for $V_{CC} = \pm 15\text{ V}$	7
• Deleted total harmonic distortion, voltage noise, current noise, differential gain error, and differential phase error for $R_L = 150\ \Omega$ in <i>Electrical Characteristics - THS4031</i> , $R_L = 1\text{ k}\Omega$	7
• Changed open loop gain minimum in <i>Electrical Characteristics - THS4031</i> , $R_L = 1\text{ k}\Omega$ from 98 dB to 100 dB for $V_{CC} = \pm 15\text{ V}$, $T_A = 25\text{ }^\circ\text{C}$	7
• Changed open loop gain minimum in <i>Electrical Characteristics - THS4031</i> , $R_L = 1\text{ k}\Omega$ from 95 dB to 98 dB for $V_{CC} = \pm 5\text{ V}$, $T_A = 25\text{ }^\circ\text{C}$	7
• Changed input offset voltage typical in <i>Electrical Characteristics - THS4031</i> , $R_L = 1\text{ k}\Omega$ from 0.5 mV to 0.3 mV.....	7
• Changed input bias current typical in <i>Electrical Characteristics - THS4031</i> , $R_L = 1\text{ k}\Omega$ from 3 μA to 9 μA for $T_A = 25\text{ }^\circ\text{C}$	7
• Changed input bias current max in <i>Electrical Characteristics - THS4031</i> , $R_L = 1\text{ k}\Omega$ from 6 μA to 20 μA for $T_A = 25\text{ }^\circ\text{C}$	7
• Changed input bias current max in <i>Electrical Characteristics - THS4031</i> , $R_L = 1\text{ k}\Omega$ from 8 μA to 33 μA for $T_A = \text{full range}$	7
• Deleted output voltage swing for $R_L = 150\ \Omega$ and $R_L = 250\ \Omega$ in <i>Electrical Characteristics - THS4031</i> , $R_L = 1\text{ k}\Omega$ table.....	7
• Deleted output current in <i>Electrical Characteristics - THS4031</i> , $R_L = 1\text{ k}\Omega$ table.....	7
• Deleted output resistance in <i>Electrical Characteristics - THS4031</i> , $R_L = 1\text{ k}\Omega$	7
• Changed supply current (each amplifier) typical in <i>Electrical Characteristics - THS4031</i> , $R_L = 1\text{ k}\Omega$ from 8.5 mA to 7.5 mA for $V_{CC} = \pm 15\text{ V}$	7
• Changed supply current (each amplifier) in <i>Electrical Characteristics - THS4031</i> , $R_L = 1\text{ k}\Omega$ from 7.5 mA to 6.5 mA for $V_{CC} = \pm 5\text{ V}$	7
• Deleted full-power bandwidth specification from <i>Electrical Characteristics - THS4032</i> , $R_L = 150\ \Omega$	9
• Changed title of <i>Electrical Characteristics - $R_L = 150\ \Omega$</i> to <i>Electrical Characteristics - THS4032</i> , $R_L = 150\ \Omega$	9
• Updated input offset voltage units specification in <i>Electrical Characteristics - THS4032</i> , $R_L = 150\ \Omega$	9
• Deleted 1k Ω open loop gain specification from in <i>Electrical Characteristics - THS4032</i> , $R_L = 150\ \Omega$	9
• Changed title of <i>Electrical Characteristics: $R_L = 1\text{ k}\Omega$</i> to <i>Electrical Characteristics - THS4032 $R_L = 1\text{ k}\Omega$</i>	10
• Deleted 150 Ω input voltage noise, input current noise, differential gain error, and differential phase error, specifications from <i>Electrical Characteristics - THS4032</i> , $R_L = 1\text{ k}\Omega$	10
• Deleted output voltage swing for $R_L = 150\ \Omega$ and $R_L = 250\ \Omega$ in <i>Electrical Characteristics - THS4032</i> , $R_L = 1\text{ k}\Omega$ table	10
• Added <i>Typical Characteristics - THS4031</i> section.....	12
• Changed title of <i>Typical Characteristics</i> to <i>Typical Characteristics - THS4032</i>	18
• Deleted <i>Parameter Measurement Information</i> section.....	26
• Deleted <i>Noise Calculation and Noise Figure, Optimizing Frequency Response, and Offset Voltage</i> sections.....	27
• Changed <i>Application Information</i> section to latest standard format.....	28
• Changed name of <i>General Configuration</i> section to <i>Low-pass Filter Configurations</i>	29
• Deleted thermal calculations in <i>General PowerPAD™ Integrated Circuit Package Design Considerations</i> ...	34

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS4031CD	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	4031C	
THS4031CDGN	LIFEBUY	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	ACM	
THS4031CDGNR	LIFEBUY	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	ACM	
THS4031CDR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	0 to 70	4031C	
THS4031ID	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4031I	
THS4031IDG4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4031I	
THS4031IDGN	LIFEBUY	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	ACN	
THS4031IDGNG4	LIFEBUY	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACN	
THS4031IDGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	ACN	Samples
THS4031IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4031I	Samples
THS4032CDGN	OBSOLETE	HVSSOP	DGN	8		TBD	Call TI	Call TI	0 to 70	ABD	
THS4032CDR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	0 to 70	4032C	
THS4032ID	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4032I	
THS4032IDG4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4032I	
THS4032IDGN	OBSOLETE	HVSSOP	DGN	8		TBD	Call TI	Call TI	-40 to 85	ABG	
THS4032IDGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	ABG	Samples
THS4032IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4032I	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF THS4031, THS4032 :

● Enhanced Product : [THS4032-EP](#)

● Military : [THS4031M](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS4031CDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4031CDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4031IDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4031IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS4032IDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4032IDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4032IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS4031CDGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0
THS4031CDGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
THS4031IDGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0
THS4031IDR	SOIC	D	8	2500	350.0	350.0	43.0
THS4032IDGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
THS4032IDGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0
THS4032IDR	SOIC	D	8	2500	350.0	350.0	43.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
THS4031CD	D	SOIC	8	75	505.46	6.76	3810	4
THS4031CDGN	DGN	HVSSOP	8	80	330	6.55	500	2.88
THS4031ID	D	SOIC	8	75	505.46	6.76	3810	4
THS4031IDG4	D	SOIC	8	75	505.46	6.76	3810	4
THS4031IDGN	DGN	HVSSOP	8	80	330	6.55	500	2.88
THS4031IDGNG4	DGN	HVSSOP	8	80	330	6.55	500	2.88
THS4032ID	D	SOIC	8	75	505.46	6.76	3810	4
THS4032IDG4	D	SOIC	8	75	505.46	6.76	3810	4

GENERIC PACKAGE VIEW

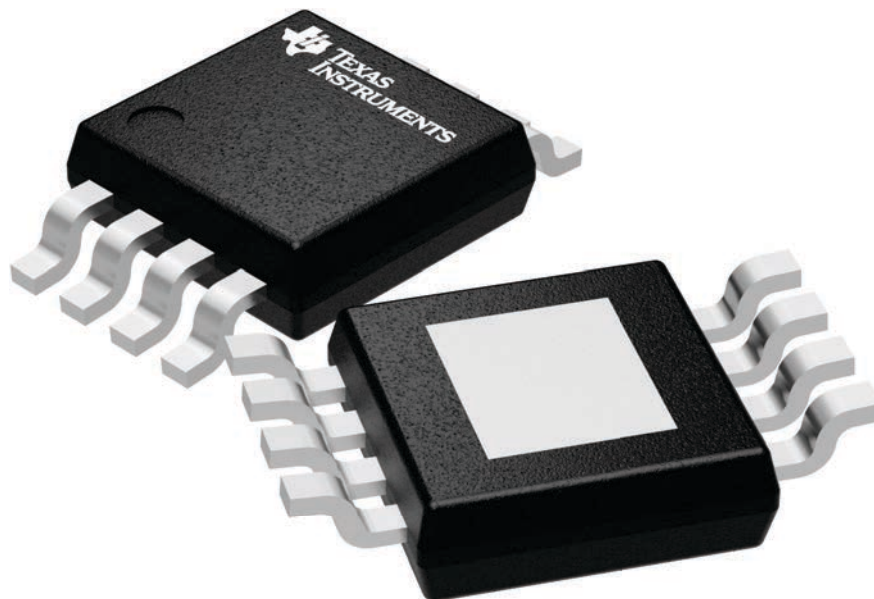
DGN 8

PowerPAD VSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/A



PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

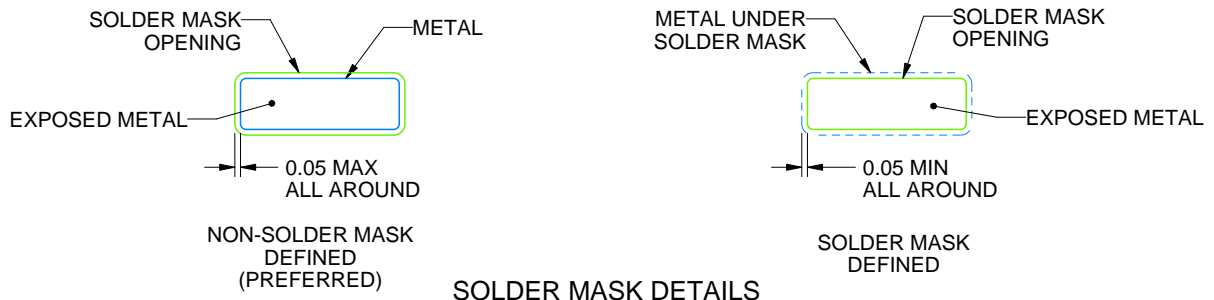
DGN0008D

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4225481/A 11/2019

NOTES: (continued)

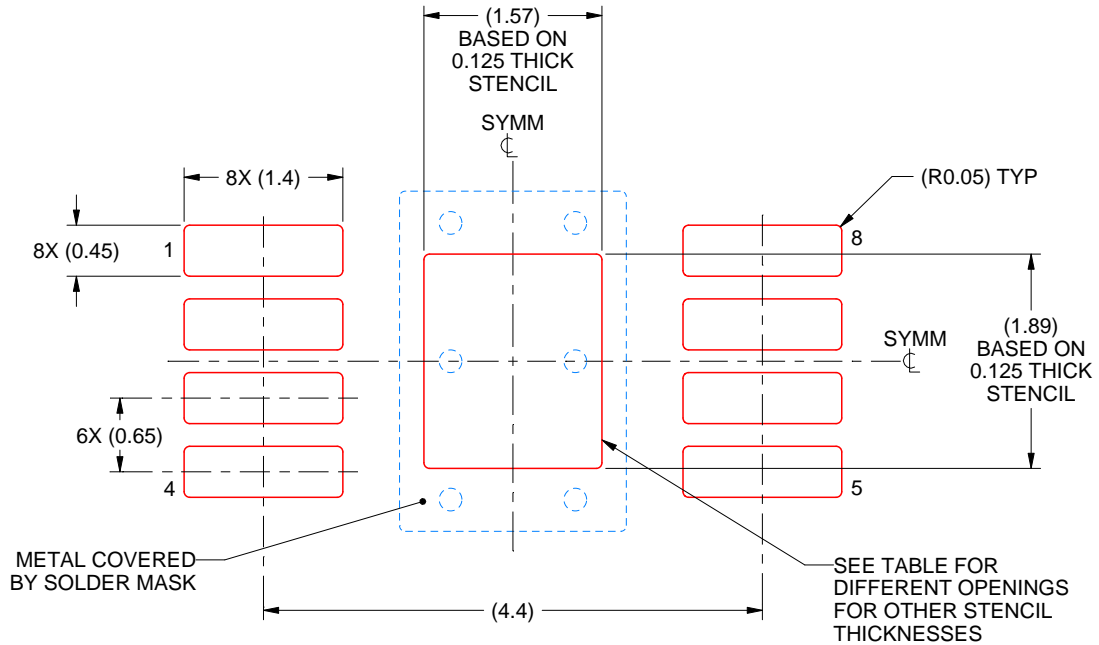
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGN0008D

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



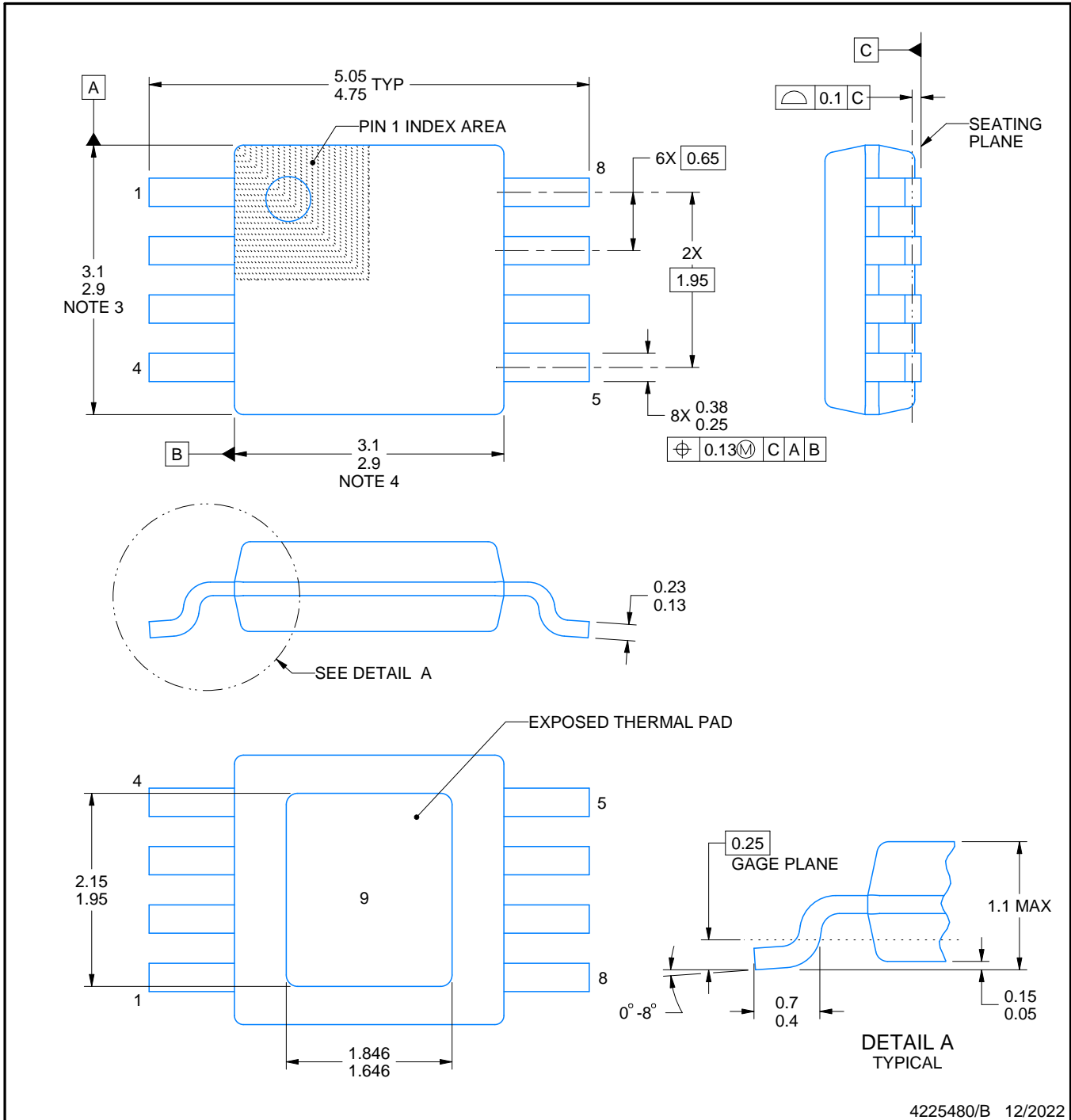
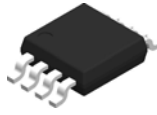
SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225481/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.



4225480/B 12/2022

PowerPAD is a trademark of Texas Instruments.

NOTES:

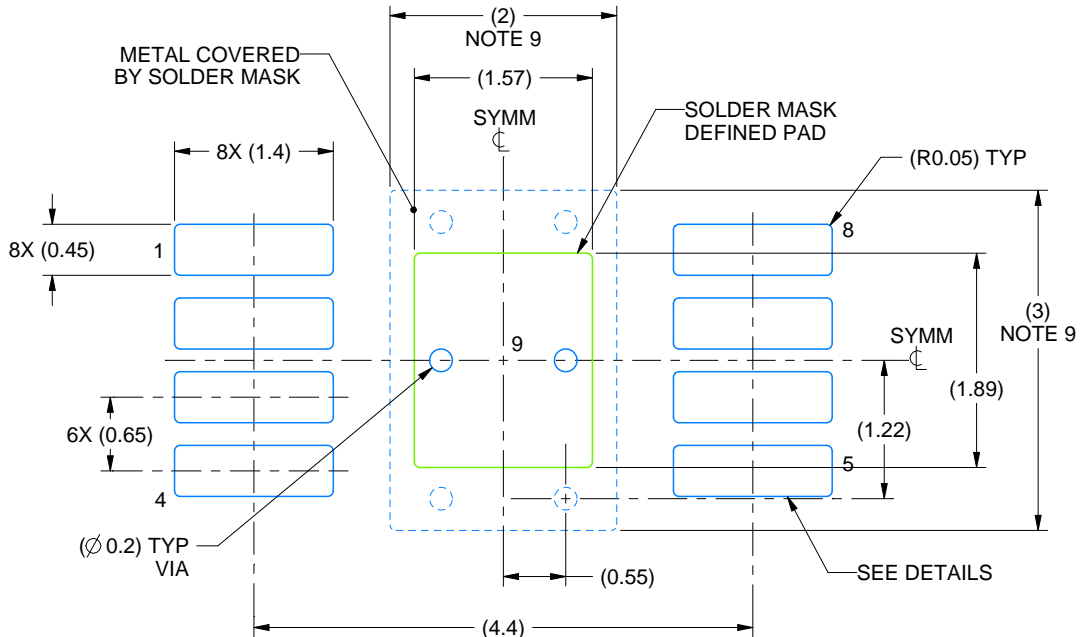
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

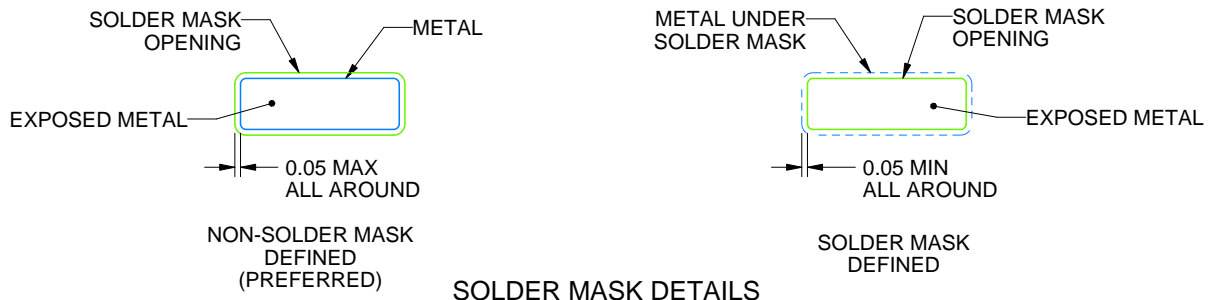
DGN0008G

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4225480/B 12/2022

NOTES: (continued)

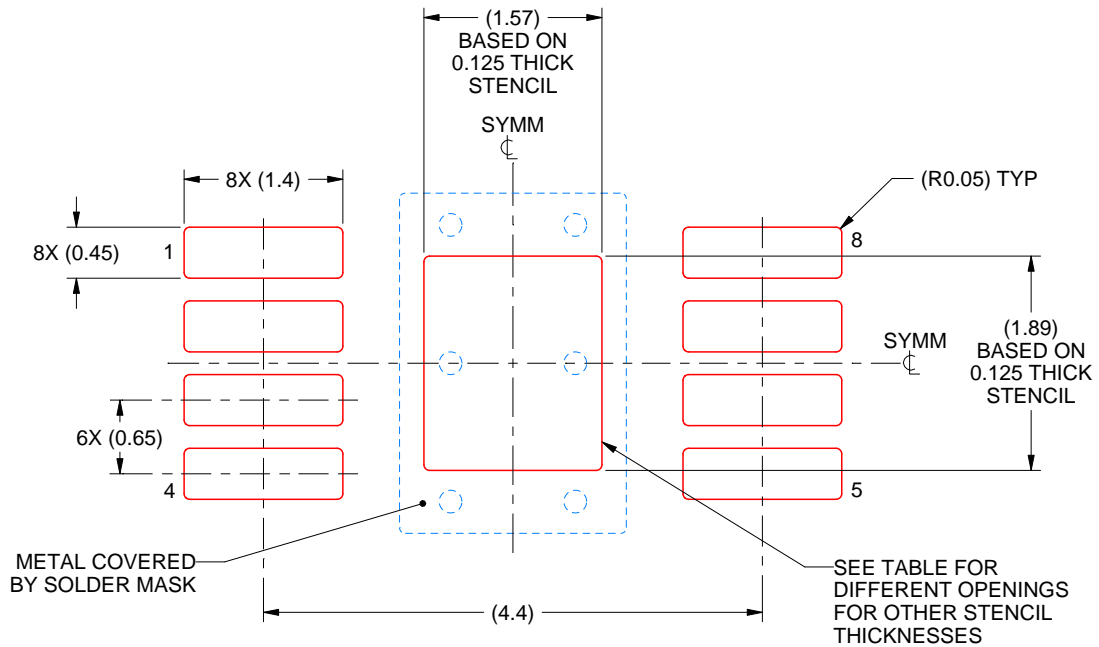
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
- 8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
- 9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGN0008G

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



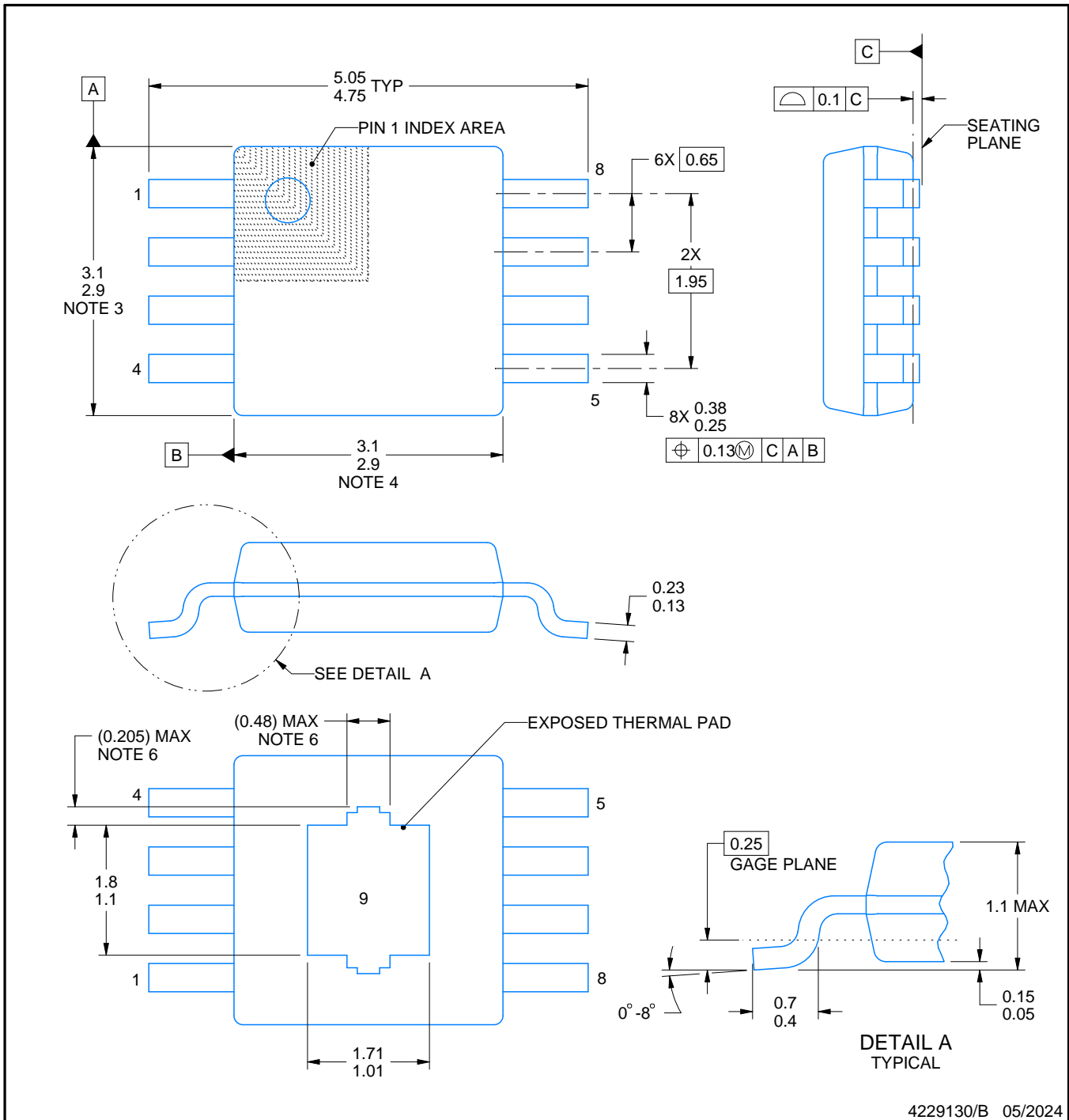
SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225480/B 12/2022

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.



4229130/B 05/2024

NOTES:

PowerPAD is a trademark of Texas Instruments.

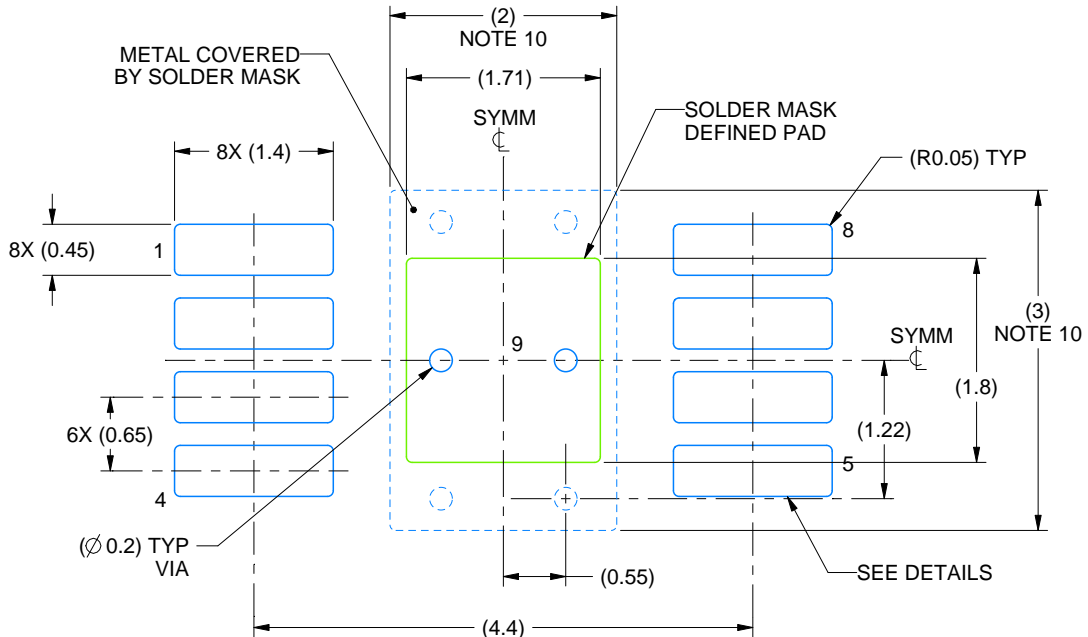
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.
6. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

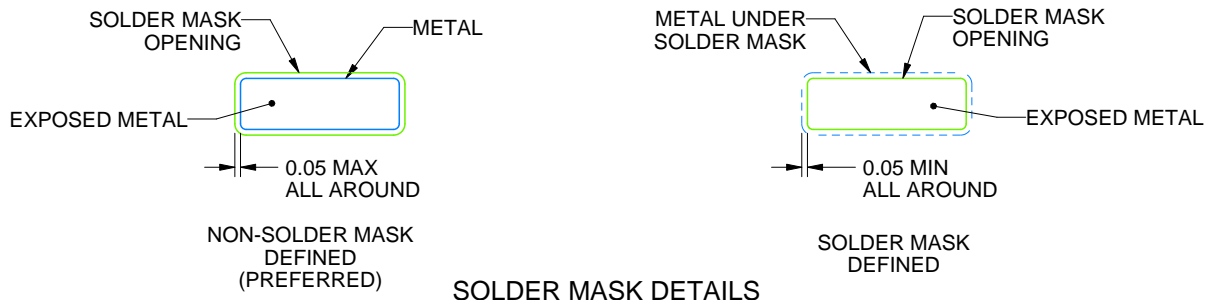
DGN0008H

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4229130/B 05/2024

NOTES: (continued)

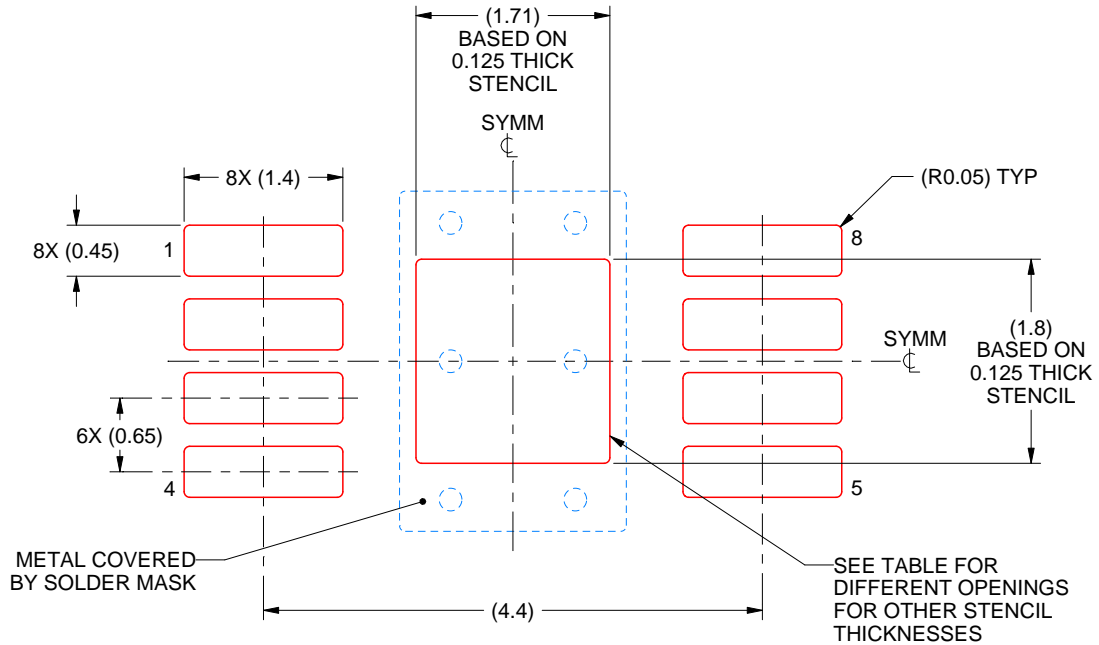
7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
9. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGN0008H

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.91 X 2.01
0.125	1.71 X 1.80 (SHOWN)
0.15	1.56 X 1.64
0.175	1.45 X 1.52

4229130/B 05/2024

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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