TLV320AIC3104-Q1 インフォテインメントおよびクラスタ向け、車載、低消費電力、ステレオ・オーディオ・コーデック

1 特長

- 車載アプリケーション用に認定済み
- 下記内容で AEC-Q100 認定済み:
  - デバイス温度グレード 2:-40℃～105℃の周囲動作温度範囲
  - デバイス HBM ESD 分類レベル 2
  - デバイス CDM ESD 分類レベル C6
- ステレオ オーディオ DAC:
  - 102dBA の信号対雑音比
  - 16、20、24、32 ビットのデータ
  - 8kHz～96kHz のサンプル レートに対応
  - 3D、バス、トレブル、EQ、ディエンファシスのエフェクト
  - 柔軟な省電力モードと性能が利用可能
- ステレオ オーディオ ADC:
  - 92dBA の信号対雑音比
  - 8kHz～96kHz のサンプル レートに対応
  - 録音時にデジタル信号処理とノイズ フィルタリングが利用可能
- 6 本のオーディオ入力ピン:
  - シングルエンド入力のステレオ ペア × 1
  - 完全差動入力のステレオ ペア × 1
- 6 つのオーディオ出力ドライバ:
  - ステレオの完全差動またはシングルエンド ヘッドホン ドライバ
  - 完全差動ステレオ ライン出力
- 低消費電力:14mW ステレオ、3.3V アナログ電源による 48kHz 再生
- パッシブ アナログ バイパスによる超低消費電力モード
- 入出力アナログ ゲインをプログラム可能
- 録音時の自動ゲイン制御 (AGC)
- プログラム可能なマイクロフォン バイアス レベル
- プログラム可能な PLL による柔軟なクロック生成
- I^2C 制御バス
- オーディオ シリアル データ バスは I^2S、左揃えおよび右揃えの DSP および TDM モードをサポート
- 包括的なモジュール型電源制御
- 電源
  - アナログ:2.7V～3.6V
  - デジタル コア:1.525V～1.95V
  - デジタル I/O:1.1V～3.6V

2 アプリケーション

- クラスタ
- ヘッド ユニット
- カー オーディオ
- 緊急通報 (E-Call)
- テレマティクス制御ユニット

3 概要

TLV320AIC3104-Q1 は、ステレオ ヘッドホン アンプを内蔵した低消費電力ステレオ オーディオ コーデックであり、シングル エンドまたは完全差動構成でプログラム可能な複数の入力と出力を備えています。レジスタ ベースの包括的な電源制御機能が搭載されており、3.3V のアナログ電源からわずか 14mW のステレオ 48kHz DAC 再生が可能なため、このデバイスはクラスタおよびヘッド ユニット システムの車載用オーディオ アプリケーションに最適な選択です。

TLV320AIC3104-Q1 の録音パスには、内蔵マイクロフォン バイアス、デジタル制御のステレオ マイク プリアンプ、自動ゲイン制御 (AGC) が含まれており、複数のアナログ入力の間に MIX および MUX 機能があります。録音時にプログラム可能なフィルタを使用でき、e-Call システムがアクティブになっているときなど、ノイズの多い予測不可能な環境で発生する可能性がある可聴ノイズを除去できます。再生パスには MIX および MUX 機能があり、ステレオ DAC および選択した入力から、プログラム可能なボリューム制御を介して各種の出力が可能です。

TLV320AIC3104-Q1 には、4 つの大電力出力ドライバと 2 つの完全差動出力ドライバが内蔵されています。大電力出力ドライバは、AC カップリング コンデンサを使用した最大 4 チャネルのシングルエンド 16Ω ヘッドホン、あるいはコンデンサレス出力構成のステレオ 16Ω ヘッドホンなど、さまざまな負荷構成を駆動できます。これらのパラメータにより、TLV320AIC3104-Q1 は、インフォテインメントおよびクラスタ分野のさまざまなオーディオ アプリケーションで、TPA3111D1-Q1 などの MCU とスピーカ アンプの間のインターフェイスとして動作できます。

ステレオ オーディオ DAC は 8kHz～96kHz のサンプリング レートをサポートし、DAC パスにプログラマブル デジタル フィルタを備えており、3D、バス、トレブル、ミッドレンジ エフェクト、スピーカ イコライゼーション、32kHz、44.1kHz、48kHz の各サンプリング レートのディエンファシスを実現します。ステレオ オーディオ ADC は、8kHz～96kHz のサンプリング レートをサポートし、前段に、低レベルのマイク入力に対して最大 59.5dB のアナログ ゲインを実現できるプログラマブル ゲイン アンプ (PGA) または自動ゲイン制御 (AGC) 回路が搭載されています。TLV320AIC3104-Q1 は、アタック (8ms～1,408ms) とディケイ (0.05 秒～22.4 秒) の両方に対して非常に広範囲にわたるプログラマビリティを実現します。AGC 範囲が広いので、AGC を多くの種類のアプリケーションに合わせてチューニングできます。

アナログ信号処理とデジタル信号処理のどちらも必要ない場合、デバイスを特別なアナログ信号パススルー モードに設定できます。このモードでは、パススルー動作中にほとんどのデバイスがパワーダウンするため、消費電力が大幅に削減されます。

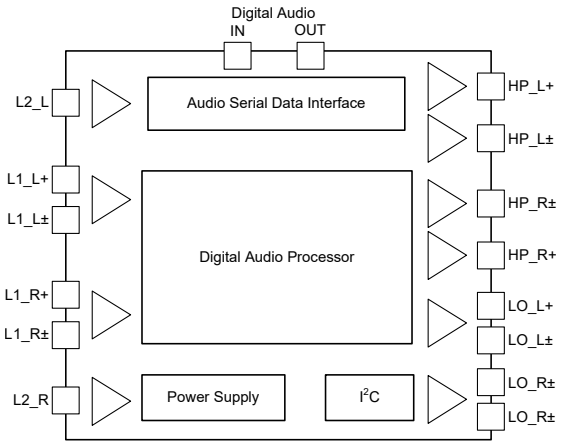
シリアル制御バスは I^2C プロトコルをサポートし、シリアル オーディオ データ バスは I^2S、左 / 右揃えの DSP または TDM モードにプログラムできます。高度にプログラム可能な PLL が内蔵されており、柔軟なクロック生成ができ、512kHz～50MHz の広い範囲の MCLK から、標準的なオーディオ速度のすべてをサポートしています。これには最も一般的な 12MHz、13MHz、16MHz、19.2MHz、19.68MHz のシステム クロックが含まれるように特に注意を払っています。

TLV320AIC3104-Q1 は、2.7V～3.6V のアナログ電源、1.525V～1.95V のデジタル コア電源、1.1V～3.6V のデジタル入出力電源で動作します。

製品情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
TLV320AIC3104-Q1	VQFN (32)	5.00mm × 5.00mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



簡略ブロック図

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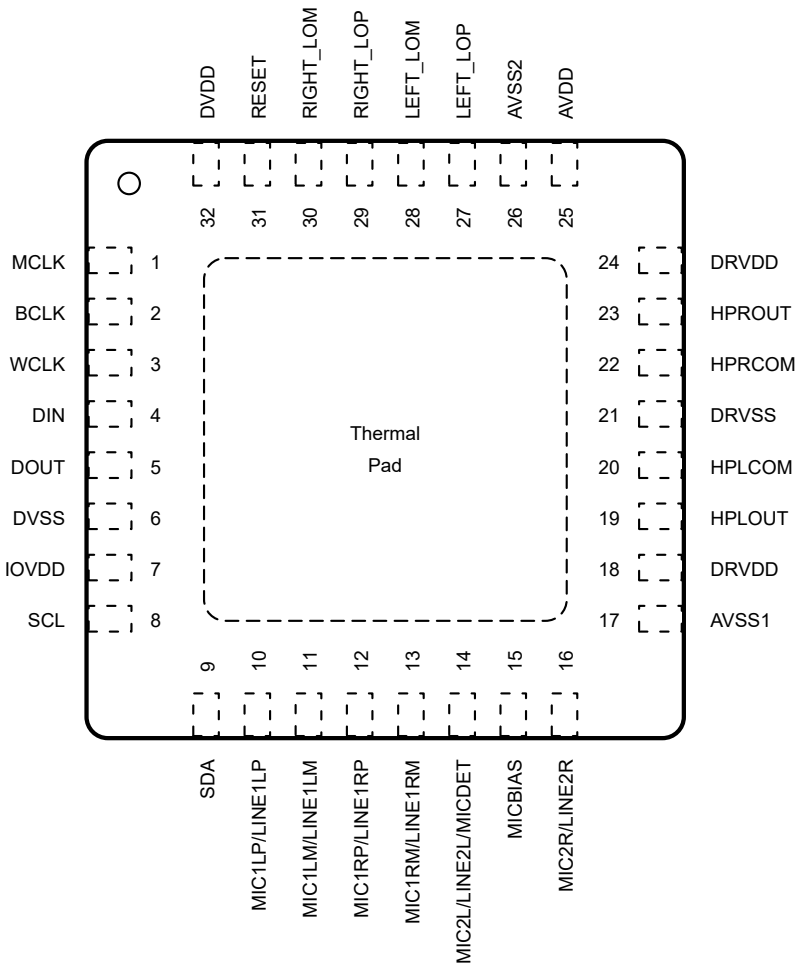
4 Device Comparison

表 4-1. Device Comparison Table

DEVICE NAME	DIFFERENCES	
TLV320AIC3104-Q1	6 inputs	6 outputs
TLV320AIC3106-Q1	10 inputs	7 outputs

5 Pin Configuration and Functions

RHB Package
32-Pin VQFN With Exposed Thermal Pad
Top View



NOTE: Connect the device thermal pad to DRVSS.

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
AVDD	25	—	Analog DAC voltage supply, 2.7 V to 3.6 V
AVSS1	17	—	Analog ADC ground supply, 0 V
AVSS2	26	—	Analog DAC ground supply, 0 V
BCLK	2	I/O	Audio serial data bus bit clock input/output

表 5-1. Pin Functions (続き)

PIN		TYPE	DESCRIPTION
NAME	NO.		
DIN	4	I	Audio serial data bus data input
DOUT	5	O	Audio serial data bus data output
DRVDD	18	—	Analog ADC and output driver voltage supply, 2.7 V to 3.6 V
DRVDD	24	—	Analog output driver voltage supply, 2.7 V to 3.6 V
DRVSS	21	—	Analog output driver ground supply, 0 V
DVDD	32	—	Digital core voltage supply, 1.525 V to 1.95 V
DVSS	6	—	Digital core / I/O ground supply, 0 V
HPLCOM	20	O	High-power output driver (left –, or multifunctional)
HPLOUT	19	O	High-power output driver (left +)
HPRCOM	22	O	High-power output driver (right –, or multifunctional)
HPROUT	23	O	High-power output driver (right +)
IOVDD	7	—	Digital I/O voltage supply, 1.1 V to 3.6 V
LEFT_LOM	28	O	Left line output (–)
LEFT_LOP	27	O	Left line output (+)
MCLK	1	I	Master clock input
MIC1LM/LINE1LM	11	I	Left input – (diff only)
MIC1LP/LINE1LP	10	I	Left input 1 (SE) or left input + (diff)
MIC1RM/LINE1RM	13	I	Right input – (diff only)
MIC1RP/LINE1RP	12	I	Right input 1 (SE) or right input + (diff)
MIC2L/LINE2L/MICDET	14	I	Left input 2 (SE); can support microphone detection
MIC2R/LINE2R	16	I	Right input 2 (SE)
MICBIAS	15	O	Microphone bias voltage output
$\overline{\text{RESET}}$	31	I	Reset
RIGHT_LOM	30	O	Right line output (–)
RIGHT_LOP	29	O	Right line output (+)
SCL	8	I/O	I^2C serial clock input
SDA	9	I/O	I^2C serial data input/output
WCLK	3	I/O	Audio serial data bus word clock input/output

6 Specifications

6.1 Absolute Maximum Ratings

(1)

	MIN	MAX	UNIT
AVDD to AVSS, DRVDD to DRVSS	–0.3	3.9	V
AVDD to DRVSS	–0.3	3.9	V
IOVDD to DVSS	–0.3	3.9	V
DVDD to DVSS	–0.3	2.5	V
AVDD to DRVDD	–0.1	0.1	V
Analog input voltage to AVSS	–0.3	AVDD + 0.3	V
Digital input voltage to DVSS	–0.3	IOVDD + 0.3	V
Power dissipation	(T_J Max - T_A) / $R_{\theta JA}$		W
Junction temperature, T_J		107	°C
Operating temperature range	–40	105	°C
Storage, T_{stg}	–40	105	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
AVDD, DRVDD 1/2	Analog supply voltage [1]	2.7	3.3	3.6	V
DVDD	Digital core supply voltage [1]	1.525	1.8	1.95	V
IOVDD	Digital I/O supply voltage [1]	1.1	1.8	3.6	V
V_I	Analog full-scale, 0-dB input voltage (DRVDD = 3.3 V)		0.707		V_{RMS}
	Stereo line output load resistance	10			kΩ
	Stereo headphone output load resistance	16			Ω
	Digital output load capacitance		10		pF
T_A	Operating free-air temperature	–40		105	°C

(1) Analog voltage values are with respect to AVSS, DRVSS; digital voltage values are with respect to DVSS.

6.4 Thermal Information

THERMAL METRIC[1]		TLV320AIC3104-Q1 RHB (VQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	17.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	6.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at 25°C, AVDD = DRVDD = IOVDD = 3.3 V, DVDD = 1.8 V, f_S = 48 kHz, and 16-bit audio data (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AUDIO ADC						
	Input signal level	Single-ended configurations		0.707		V_{RMS}
SNR	Signal-to-noise ratio(1) (2)	A-weighted, f_S = 48 kSPS, 0-dB PGA gain, inputs ac-shorted to ground	80	92		dB
DR	Dynamic range(1) (2)	f_S = 48 kSPS; 0-dB PGA gain; 1-kHz, –60-dB, full-scale input signal		93		dB
THD	Total harmonic distortion	f_S = 48 kSPS; 0-dB PGA gain; 1-kHz, –2-dB, full-scale input signal		–89	–75	dB
PSRR	Power-supply rejection ratio	217-Hz signal applied to DRVDD		55		dB
		1-kHz signal applied to DRVDD		44		
	Input channel separation	1-kHz, –2-dB, full-scale signal, MIC1 to MIC2		–71		dB
	Gain error	f_S = 48 kSPS; 0-dB PGA gain; 1-kHz, –2-dB, full-scale input signal		0.82		dB
	ADC programmable-gain amplifier maximum gain	1-kHz input tone		59.5		dB
	ADC programmable-gain amplifier step size			0.5		dB
	Input resistance	MIC1L/MIC1R inputs routed to single ADC input MIX attenuation = 0 dB		20		kΩ
		MIC1L/MIC1R inputs routed to single ADC input MIX attenuation = 12 dB		80		
		MIC2L/MIC2R inputs routed to single ADC input MIX attenuation = 0 dB		20		
		MIC2L/MIC2R inputs routed to single ADC input MIX attenuation = 12 dB		80		
	Input resistance			80		kΩ
	Input capacitance	MIC1/LINE1 inputs		10		pF
	Input level control minimum attenuation setting			0		dB
	Input level control maximum attenuation setting			12		dB
	Input level control attenuation step size			1.5		dB
ANALOG PASSTHROUGH MODE						
$R_{DS(on)}$	Input-to-output switch resistance	MIC1/LINE1 to LINEOUT		330		Ω
		MIC2/LINE2 to LINEOUT		330		
INPUT SIGNAL LEVEL, DIFFERENTIAL						
SNR	Signal-to-noise ratio	A-weighted, f_S = 48 kSPS, 0-dB PGA gain, inputs ac-shorted to ground		92		dB
THD	Total harmonic distortion	f_S = 48 kHz; 0-dB PGA gain, 1-kHz, –2-dB, full-scale input signal		–94		dB
ADC DIGITAL DECIMATION FILTER (f_S = 48 kHz)						
	Filter gain	From 0 f_S to 0.39 f_S		±0.1		dB
		At 0.4125 f_S		–0.25		
		At 0.45 f_S		–3		
		At 0.5 f_S		–17.5		
		From 0.55 f_S to 64 f_S		–75		
	Filter group delay			17/f_S		s

at 25°C, AVDD = DRVDD = IOVDD = 3.3 V, DVDD = 1.8 V, f_S = 48 kHz, and 16-bit audio data (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MICROPHONE BIAS						
	Bias voltage	Programmable setting = 2 V		2		V
		Programmable setting = 2.5 V	2.3	2.455	2.7	
		Programmable setting = DRVDD		DRVDD - 0.24		
	Current sourcing	Programmable setting = 2.5 V		4		mA
AUDIO DAC, DIFFERENTIAL LINE OUTPUT (R_{LOAD} = 10 kΩ)						
	Full-scale output voltage	0-dB input full-scale signal, output common-mode setting = 1.35 V, output volume control = 0 dB		1.414		V_{RMS}
				4		V_{PP}
	Signal-to-noise ratio[3]	A-weighted, f_S = 48 kHz, output volume control = 0 dB, no input signal, referenced to full-scale input level	90	102		dB
	Dynamic range	A-weighted, f_S = 48 kHz, –60-dB input full-scale signal, output volume control = 0 dB, output common-mode setting = 1.35 V		97		dB
	Total harmonic distortion	f_S = 48 kHz; 0-dB, 1-kHz input full-scale signal; output volume control = 0 dB; output common-mode setting = 1.35 V		–95	–75	dB
PSRR	Power-supply rejection ratio	217-Hz signal applied to DRVDD, AVDD_DAC		78		dB
		1-kHz signal applied to DRVDD, AVDD_DAC		80		
	DAC channel separation	0-dB full-scale input signal between left and right lineout		86		dB
	DAC interchannel gain mismatch	1-kHz input, 0-dB gain		0.1		dB
	DAC gain error	0-dB, 1-kHz input full-scale signal; output volume control = 0 dB; output common-mode setting = 1.35 V; f_S = 48 kHz		–0.2		dB
AUDIO DAC, SINGLE-ENDED LINE OUTPUT (R_{LOAD} = 10 kΩ)						
	Full-scale output voltage	0-dB input full-scale signal, output common-mode setting = 1.35 V, output volume control = 0 dB		0.707		V_{RMS}
SNR	Signal-to-noise ratio	A-weighted, f_S = 48 kHz, output volume control = 0 dB, no input signal, output common-mode setting = 1.35 V		97		dB
THD	Total harmonic distortion	f_S = 48 kHz; 0-dB, 1-kHz input full-scale signal; output volume control = 0 dB; output common-mode setting = 1.35 V		-84		dB
	DAC gain error	0-dB, 1-kHz input full-scale signal; output volume control = 0 dB; output common-mode setting = 1.35 V; f_S = 48 kHz		0.55		dB

at 25°C, AVDD = DRVDD = IOVDD = 3.3 V, DVDD = 1.8 V, f_S = 48 kHz, and 16-bit audio data (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AUDIO DAC, SINGLE-ENDED HEADPHONE OUTPUT (R_{LOAD} = 16 Ω)						
	Full-scale output voltage	0-dB input full-scale signal, output common-mode setting = 1.35 V, output volume control = 0 dB		0.707		V_{RMS}
SNR	Signal-to-noise ratio	A-weighted, f_S = 48 kHz, output volume control = 0 dB, no input signal, referenced to full-scale input level		96		dB
		A-weighted, f_S = 48 kHz, output volume control = 0 dB, no input signal, referenced to full-scale input level, 50% DAC current-boost mode		97		
	Dynamic range	A-weighted, f_S = 48 kHz, –60-dB input full-scale signal, output volume control = 0 dB, output common-mode setting = 1.35 V		91		dB
THD	Total harmonic distortion	f_S = 48 kHz, 0-dB input full-scale signal, output volume control = 0 dB, output common-mode setting = 1.35 V		–71	–65	dB
PSRR	Power-supply rejection ratio	217-Hz signal applied to DRVDD, AVDD_DAC		43		dB
		1-kHz signal applied to DRVDD, AVDD_DAC		41		
	DAC channel seperation	Right headphone out		89		dB
	DAC gain error	0-dB, 1-kHz input full-scale signal; output volume control = 0 dB; output common-mode setting = 1.35 V; f_S = 48 kHz		–0.85		dB
DAC DIGITAL INTERPOLATION FILTER (f_S = 48 kHz)						
	Pass band		0		0.45 f_S	Hz
	Pass-band ripple			±0.06		dB
	Transition band		0.45 f_S		0.55 f_S	Hz
	Stop band		0.55 f_S		7.5 f_S	Hz
	Stop-band attenuation			65		dB
	Group delay			21 / f_S		s
STEREO HEADPHONE DRIVER (AC-Coupled Output Configuration[3])						
	0-dB full-scale output voltage	0-dB gain to high-power outputs, output common-mode voltage setting = 1.35 V		0.707		V_{RMS}
	Programmable output common-mode voltage (applicable to line outputs also)	First option		1.35		V
		Second option		1.5		
		Third option		1.65		
		Fourth option		1.8		
	Maximum programmable output level control gain			9		dB
	Programmable output level control gain step size			1		dB
P_O	Maximum output power	R_L = 32 Ω		15		mW
		R_L = 16 Ω		30		
SNR	Signal-to-noise ratio[4]	A-weighted		94		dB

at 25°C, AVDD = DRVDD = IOVDD = 3.3 V, DVDD = 1.8 V, f_S = 48 kHz, and 16-bit audio data (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THD	Total harmonic distortion	1-kHz output, P_O = 5 mW, R_L = 32 Ω		–77		dB%
				0.014		
		1-kHz output, P_O = 10 mW, R_L = 32 Ω		–76		
				0.016		
		1-kHz output, P_O = 10 mW, R_L = 16 Ω		–73		
				0.022		
		1-kHz output, P_O = 20 mW, R_L = 16 Ω		–71		
				0.028		
	Channel separation	1-kHz, 0-dB input		90		dB
PSRR	Power-supply rejection ratio	217 Hz, 100 mV_{PP} on AVDD, DRVDD1/2		48		dB
	Mute attenuation	1-kHz output		107		dB
DIGITAL I/O						
V_{IL}	Input low level		–0.3		0.3 IOVDD	V
V_{IH}	Input high level(5)	IOVDD > 1.6 V	0.7 IOVDD			V
		IOVDD ≤ 1.6 V	1.1			
V_{OL}	Output low level				0.1 IOVDD	V
V_{OH}	Output high level		0.8 IOVDD			V
CURRENT CONSUMPTION (DRVDD = AVDD = IOVDD = 3.3 V, DVDD = 1.8 V)						
I_{IN}	I_{DRVDD} + I_{AVDD_DAC}	$\overline{\text{RESET}}$ held low		0.1		μA
	I_{DVDD}			0.2		
	I_{DRVDD} + I_{AVDD_DAC}	Mono ADC record, f_S = 8 kSPS, I^2S slave, AGC off, no signal		2.15		mA
	I_{DVDD}			0.48		
	I_{DRVDD} + I_{AVDD_DAC}	Stereo ADC record, f_S = 8 ksps, I^2S slave, AGC off, no signal		4.1		
	I_{DVDD}			0.62		
	I_{DRVDD} + I_{AVDD_DAC}	Stereo ADC record, f_S = 48 kSPS, I^2S slave, AGC off, no signal		4.31(6)		
	I_{DVDD}			2.45(6)		
	I_{DRVDD} + I_{AVDD_DAC}	Stereo DAC playback to lineout, analog mixer bypassed, f_S = 48 kSPS, I^2S slave		3.5		
	I_{DVDD}			2.3		
	I_{DRVDD} + I_{AVDD_DAC}	Stereo DAC playback to lineout, f_S = 48 kSPS, I^2S slave, no signal		4.9		
	I_{DVDD}			2.3		
	I_{DRVDD} + I_{AVDD_DAC}	Stereo DAC playback to mono single-ended headphone, f_S = 48 kSPS, I^2S slave, no signal		6.7		
	I_{DVDD}			2.3		
	I_{DRVDD} + I_{AVDD_DAC}	Stereo line in to mono line out, no signal		3.11		
	I_{DVDD}			0		
	I_{DRVDD} + I_{AVDD_DAC}	Extra power when PLL enabled		1.4		
	I_{DVDD}			0.9		
	I_{DRVDD} + I_{AVDD_DAC}	All blocks powered down, headset detection enabled, headset not inserted		28		μA
	I_{DVDD}			2		

(1) Ratio of output level with 1-kHz, full-scale, sine-wave input to the output level with the inputs short-circuited, measured A-weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.
(2) All performance measurements done with 20-kHz, low-pass filter and an A-weighted filter, where noted. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the *Electrical Characteristics*. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.
(3) Unless otherwise noted, all measurements use an output common-mode voltage setting of 1.35 V, a 0-dB output level control gain, and a 16-Ω single-ended load.
(4) Ratio of output level with a 1-kHz, full-scale input to the output level playing an all-zero signal, measured A-weighted over a 20-Hz to 20-kHz bandwidth.

(5) When IOVDD < 1.6 V, minimum V_{IH} is 1.1 V.
(6) Additional power is consumed when the PLL is powered.

6.6 Switching Characteristics I²S/LJF/RJF Timing in Master Mode

All specifications at 25°C, DVDD = 1.8 V. See 図 6-1

PARAMETER		IOVDD = 1.1 V		IOVDD = 3.3 V		UNIT
		MIN	MAX	MIN	MAX	
t_d(WS)	ADWS, WCLK delay time		50		15	ns
t_d(DO-WS)	ADWS, WCLK to DOUT delay time		50		20	ns
t_d(DO-BCLK)	BCLK to DOUT delay time		50		15	ns
t_s(DI)	DIN setup time	10		6		ns
t_h(DI)	DIN hold time	10		6		ns
t_r	Rise time		30		10	ns
t_f	Fall time		30		10	ns

6.7 Switching Characteristics I2S/LJF/RJF Timing in Slave Mode

All specifications at 25°C, DVDD = 1.8 V. See 図 6-2

PARAMETER		IOVDD = 1.1 V		IOVDD = 3.3 V		UNIT
		MIN	MAX	MIN	MAX	
t_H(BCLK)	BCLK high period	70		35		ns
t_L(BCLK)	BCLK low period	70		35		ns
t_S(WS)	ADWS/WCLK setup time	10		6		ns
t_h(WS)	ADWS, WCLK hold time	10		6		ns
t_d(DO-WS)	ADWS, WCLK to DOUT delay time (for LJF Mode only)		50		35	ns
t_d(DO-BCLK)	BCLK to DOUT delay time		50		20	ns
t_s(DI)	DIN setup time	10		6		ns
t_h(DI)	DIN hold time	10		6		ns
t_r	Rise time		8		4	ns
t_f	Fall time		8		4	ns

6.8 Switching Characteristics DSP Timing in Master Mode

All specifications at 25°C, DVDD = 1.8 V. See 図 6-3

		IOVDD = 1.1 V		IOVDD = 3.3 V		UNIT
		MIN	MAX	MIN	MAX	
t_d(WS)	ADWS, WCLK delay time		50		15	ns
t_d(DO-BCLK)	BCLK to DOUT delay time		50		15	ns
t_s(DI)	DIN setup time	10		6		ns
t_h(DI)	DIN hold time	10		6		ns
t_r	Rise time		30		10	ns
t_f	Fall time		30		10	ns

6.9 Switching Characteristics DSP Timing in Slave Mode

All specifications at 25°C, DVDD = 1.8 V. See 図 6-4

PARAMETR		IOVDD = 1.1 V		IOVDD = 3.3 V		UNIT
		MIN	MAX	MIN	MAX	
t_H(BCLK)	BCLK high period	70		35		ns
t_L(BCLK)	BCLK low period	70		35		ns
t_s(WS)	ADWS, WCLK setup time	10		8		ns
t_h(WS)	ADWS/WCLK hold time	10		8		ns
t_d(DO-BCLK)	BCLK to DOUT delay time		50		20	ns
t_s(DI)	DIN setup time	10		6		ns
t_h(DI)	DIN hold time	10		6		ns
t_r	Rise time		8		4	ns
t_f	Fall time		8		4	ns

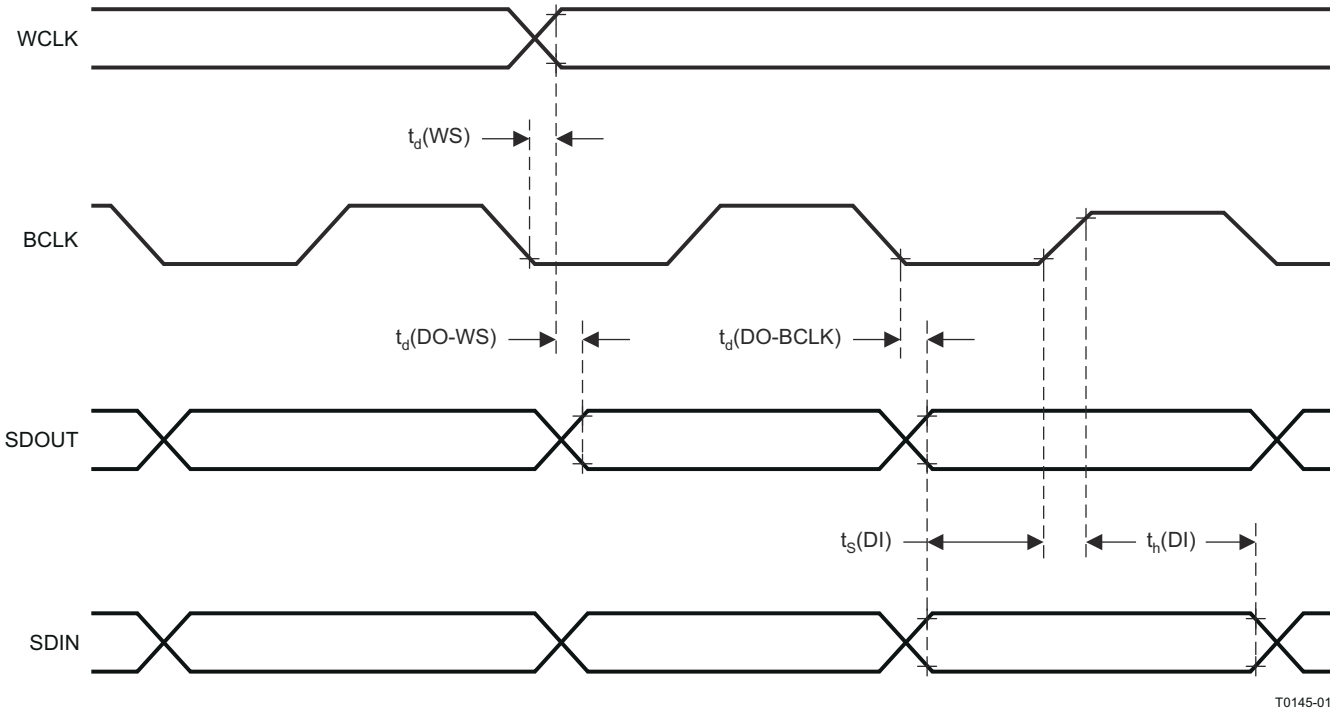


図 6-1. I²S/LJF/RJF Timing in Master Mode

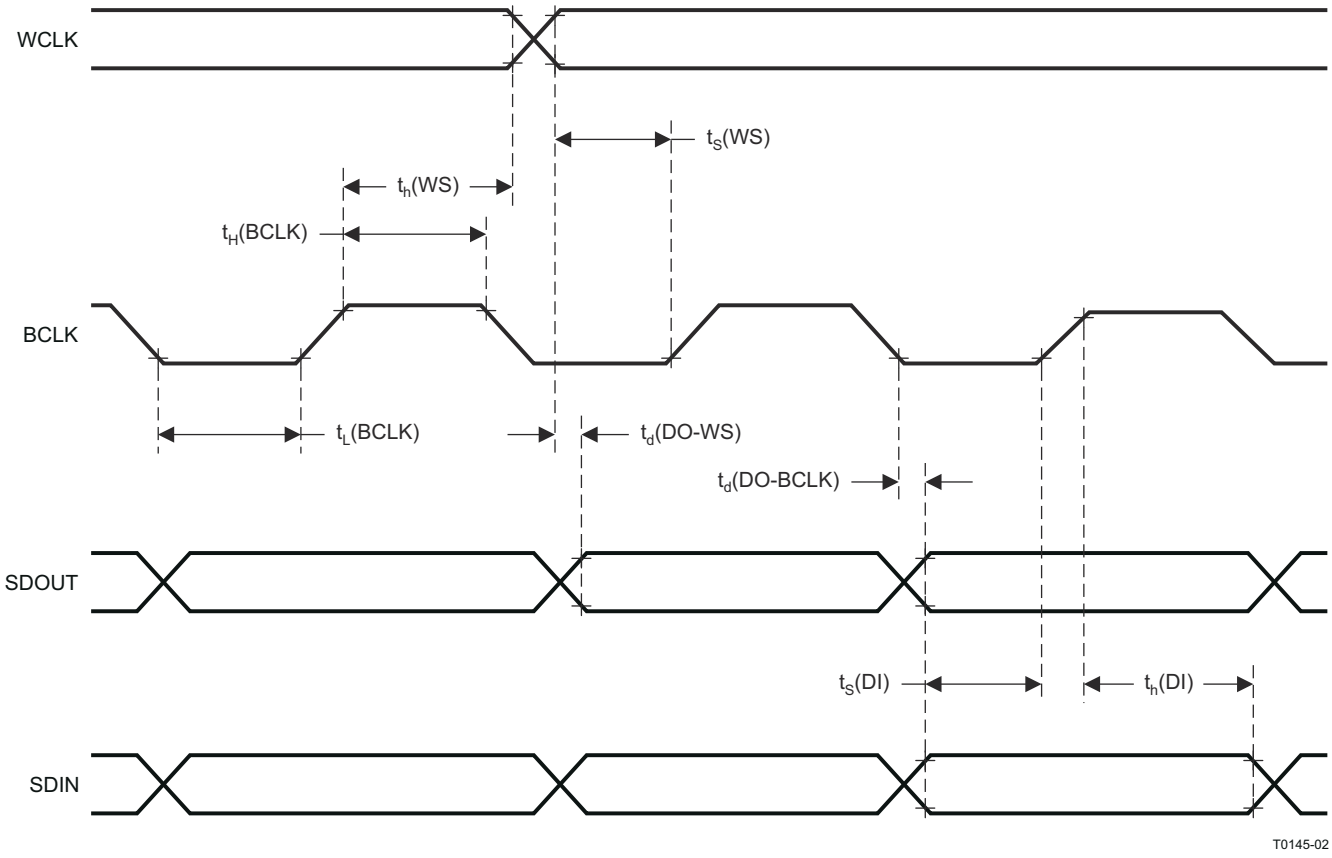


図 6-2. I²S/LJF/RJF Timing in Slave Mode

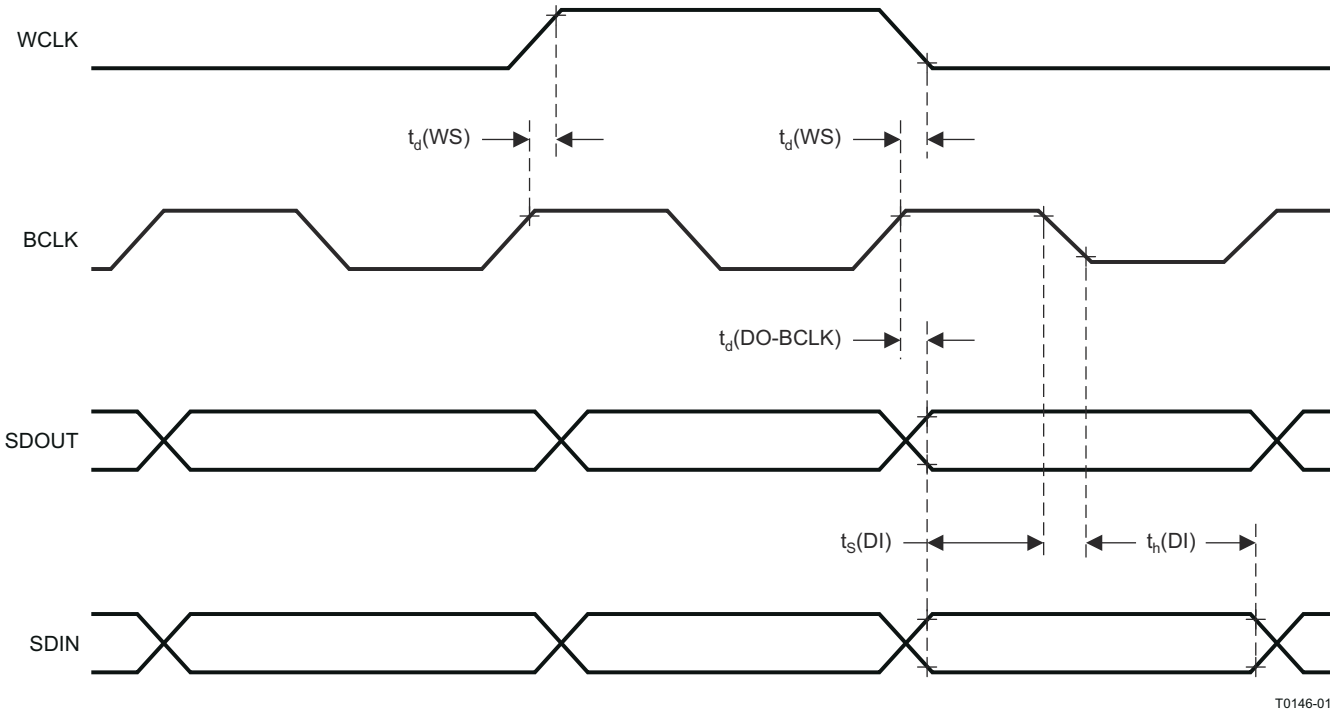


図 6-3. DSP Timing in Master Mode

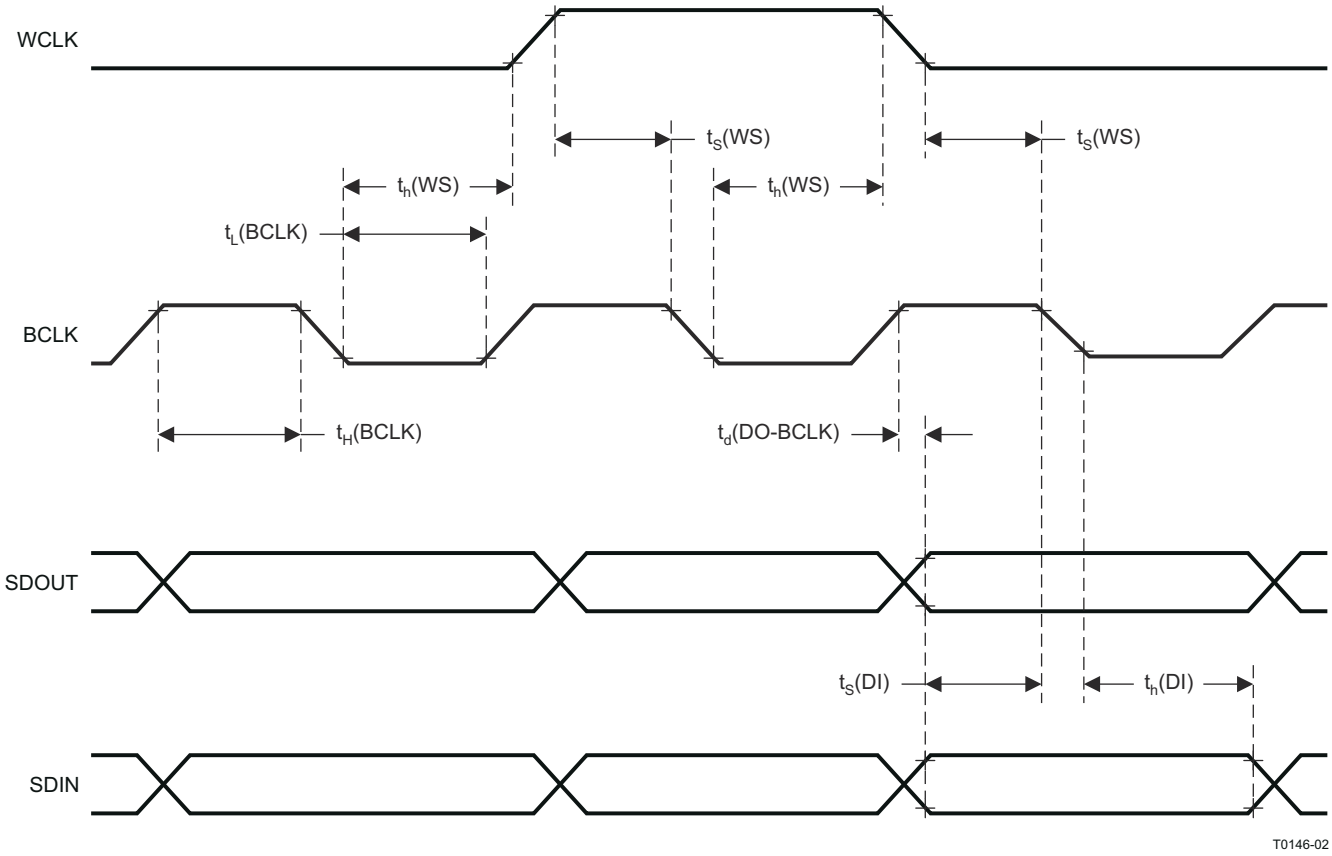


図 6-4. DSP Timing in Slave Mode

6.10 Typical Characteristics

at 25°C, AVDD = DRVDD = IOVDD = 3.3 V, DVDD = 1.8 V, f_S = 48 kHz, and 16-bit audio data (unless otherwise noted)

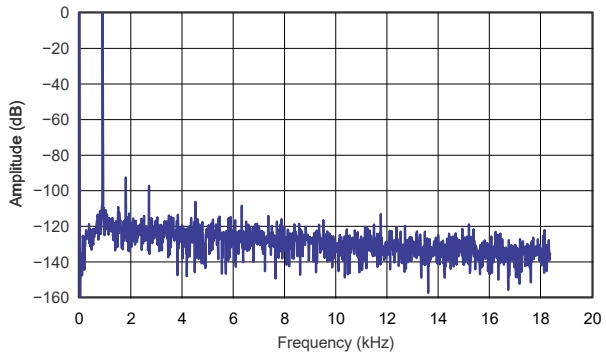


図 6-5. DAC to Line Output FFT Plot

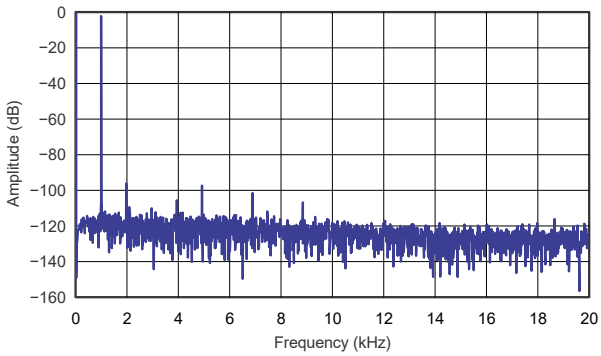
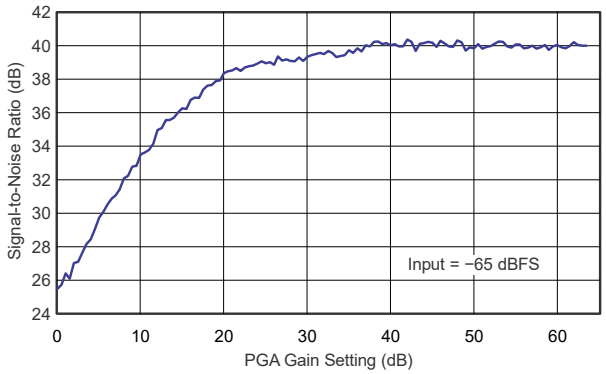


図 6-6. Line Input to ADC FFT Plot



Input = –65 dBFS

図 6-7. ADC SNR vs PGA Gain Setting, –65-dBFS Input

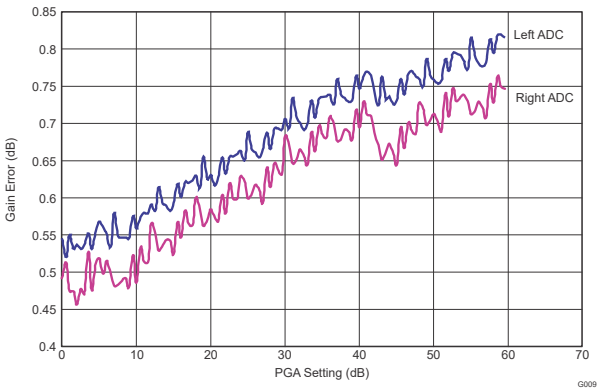


図 6-8. ADC Gain Error vs PGA Gain Setting

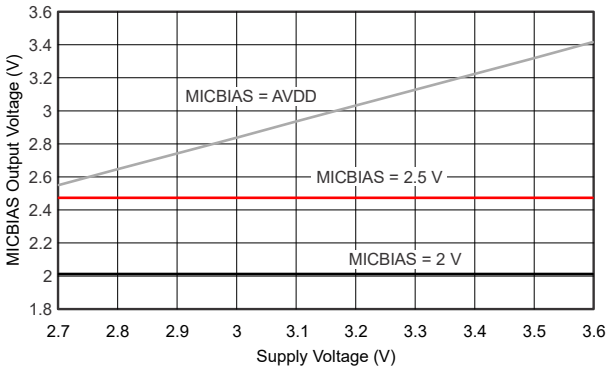


図 6-9. MICBIAS Output Voltage vs AVDD

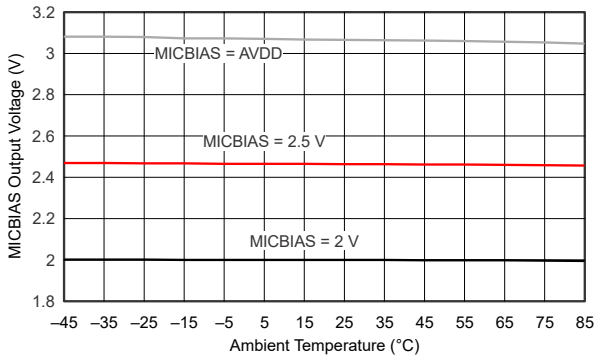


図 6-10. MICBIAS Output Voltage vs Ambient Temperature

7 Detailed Description

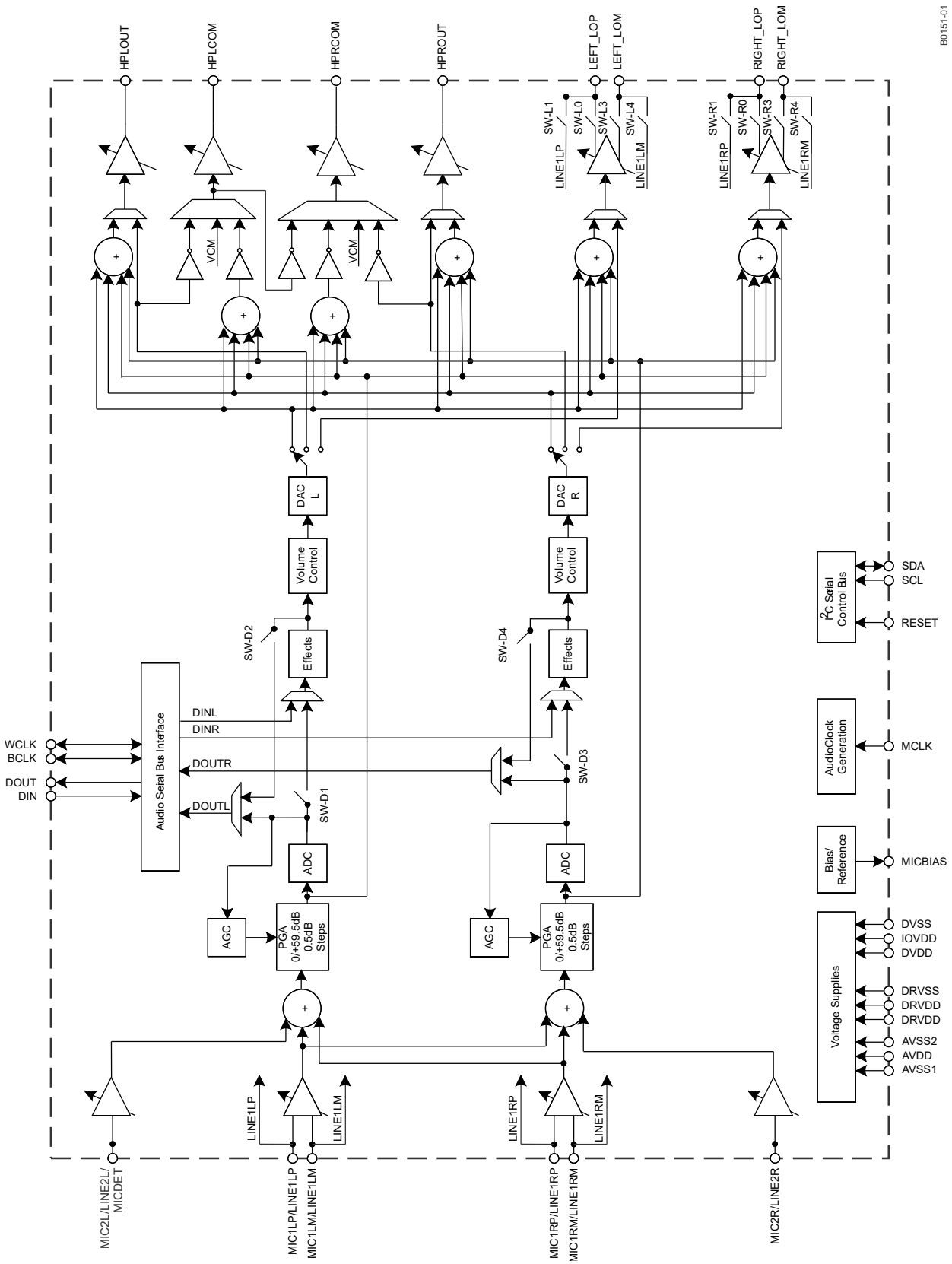
7.1 Overview

The TLV320AIC3104-Q1 is a highly flexible, low-power, stereo audio codec with extensive feature integration, intended for applications in infotainment or cluster systems such as head unit, telematics, cluster, emergency calls (eCall), navigation systems, and other car entertainment applications. The device integrates a host of features to reduce cost, board space, and power consumption in space-constrained, battery-powered, portable applications.

The TLV320AIC3104-Q1 consists of the following blocks:

- Stereo audio multibit delta-sigma DAC (8 kHz to 96 kHz)
- Stereo audio multibit delta-sigma ADC (8 kHz to 96 kHz)
- Programmable digital audio effects processing (3D, bass, treble, midrange, EQ, notch filter, de-emphasis)
- Four audio inputs
- Four high-power audio output drivers (headphone drive capability)
- Two fully differential line output drivers
- Fully programmable PLL
- Headphone/headset jack detection available as register status bit

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Audio Data Converters

The TLV320AIC3104-Q1 supports the following standard audio sampling rates: 8 kHz, 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, and 96 kHz. The converters also can operate at different sampling rates in various combinations, which are described further as follows.

The data converters are based on the concept of an $f_{S(ref)}$ rate that is used internal to the device, and is related to the actual sampling rates of the converters through a series of ratios. For typical sampling rates, $f_{S(ref)}$ is either 44.1 kHz or 48 kHz, although $f_{S(ref)}$ can realistically be set over a wider range of rates up to 53 kHz, with additional restrictions if the PLL is used. This concept is used to set the sampling rates of the ADC and DAC, and also to enable high-quality playback of low-sampling-rate data without high-frequency audible noise being generated.

The sampling rate of the ADC and DAC is determined by the clock divider (NCODEC). The sampling rate can be set to $f_{S(ref)}$ / NCODEC or 2 × $f_{S(ref)}$ / NCODEC, with NCODEC being 1, 1.5, 2, 2.5, 3, 3.5, 4, 4.5, 5, 5.5, or 6 for both the NDAC and NADC settings. In the TLV320AIC3104-Q1, NDAC and NADC must be set to the same value because the device only supports a common sampling rate for the ADC and DAC channels. Therefore, NCODEC = NDAC = NADC and this value is programmed by setting the value of bits D7 to D4 equal to the value of bits D3 to D0 in register 2, page 0.

7.3.2 Stereo Audio ADC

The TLV320AIC3104-Q1 includes a stereo audio ADC, which uses a delta-sigma modulator with 128-times oversampling in single-rate mode, followed by a digital decimation filter. The ADC supports sampling rates from 8 kHz to 48 kHz in single-rate mode, and up to 96 kHz in dual-rate mode. Whenever the ADC or DAC is in operation, the device requires that an audio master clock be provided and appropriate audio clock generation be set up within the device.

In order to provide optimal system power dissipation, the stereo ADC can be powered one channel at a time, to support the case where only mono record capability is required. In addition, both channels can be fully powered or entirely powered down.

The integrated digital decimation filter removes high-frequency content and downsamples the audio data from an initial sampling rate of 128 f_S to the final output sampling rate of fS. The decimation filter provides a linear phase output response with a group delay of 17 / fS. The –3-dB bandwidth of the decimation filter extends to 0.45 f_S and scales with the sample rate (fS). The filter has minimum 75-dB attenuation over the stop band from 0.55 fS to 64 fS. Independent digital high-pass filters are also included with each ADC channel, with a corner frequency that can be independently set.

Because of the oversampling nature of the audio ADC and the integrated digital decimation filtering, requirements for analog antialiasing filtering are very relaxed. The TLV320AIC3104-Q1 integrates a second-order analog antialiasing filter with 20-dB attenuation at 1 MHz. This filter, combined with the digital decimation filter, provides sufficient antialiasing filtering without requiring additional external components.

The ADC is preceded by a programmable gain amplifier (PGA), which allows analog gain control from 0 dB to 59.5 dB in steps of 0.5 dB. The PGA gain changes are implemented with an internal soft-stepping algorithm that only changes the actual volume level by one 0.5-dB step every one or two ADC output samples, depending on the register programming (see page 0, registers 19 and 22). This soft-stepping ensures that volume control changes occur smoothly with no audible artifacts. On reset, the PGA gain defaults to a mute condition, and on power down, the PGA soft-steps the volume to mute before shutting down. A read-only flag is set whenever the gain applied by PGA equals the desired value set by the register. The soft-stepping control can also be disabled by programming a register bit. When soft stepping is enabled, the audio master clock must be applied to the part after the ADC power-down register is written to ensure the soft-stepping to mute has completed. When the ADC power-down flag is no longer set, the audio master clock can be shut down.

7.3.2.1 Stereo Audio ADC High-Pass Filter

Often in audio applications it is desirable to remove the dc offset from the converted audio data stream. The TLV320AIC3104-Q1 has a programmable first-order high-pass filter which can be used for this purpose. The digital filter coefficients are in 16-bit format and therefore use two 8-bit registers for each of the three coefficients, N0, N1, and D1. The transfer function of the digital high-pass filter is of the form:

$$H(z) = \frac{N0 + N1 \times z^{-1}}{32,768 - D1 \times z^{-1}} \quad (1)$$

Programming the left channel is done by writing to page 1, registers 65 to 70, and the right channel is programmed by writing to page 1, registers 71 to 76. After the coefficients have been loaded, these ADC highpass filter coefficients can be selected by writing to page 0, register 107, bits D7 to D6, and the high-pass filter can be enabled by writing to page 0, register 12, bits D7 to D4.

7.3.3 Automatic Gain Control (AGC)

An automatic gain control (AGC) circuit is included with the ADC and can be used to maintain nominally constant output signal amplitude when recording speech signals (the AGC can be fully disabled if not needed). This circuitry automatically adjusts the PGA gain when the input signal becomes overly loud or very weak, such as when a person speaking into a microphone moves closer or farther from the microphone. The AGC algorithm has several programmable settings, including target level, attack and decay time constants, noise threshold, and maximum PGA gain applicable that allow the algorithm to be fine-tuned for any particular application. These AGC features are explained in this section, and 図 7-1 illustrates their operation. The algorithm uses the absolute average of the signal (which is the average of the absolute value of the signal) as a measure of the nominal amplitude of the output signal.

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Completely independent AGC circuitry is included with each ADC channel with entirely independent control over the algorithm from one channel to the next. This is attractive in cases where two microphones are used in a system, but may have different placement in the end equipment and require different dynamic performance for optimal system operation

The TLV320AIC3104-Q1 allows programming of eight different target levels, which can be programmed from –5.5 dB to –24 dB relative to a full-scale signal. Because the device reacts to the signal absolute average and not to peak levels, it is recommended that the target level be set with enough margin to avoid clipping at the occurrence of loud sounds.

Attack can be varied from 7 ms to 1,408 ms. The extended right-channel attack time can be programmed by writing to page 0, register 103, and the left channel is programmed by writing to page 0, register 105.

Decay time can be varied in the range from 0.05 s to 22.4 s. The extended right-channel decay time can be programmed by writing to page 0, register 104, and the left channel is programmed by writing to page 0, register 106.

The actual AGC decay time maximum is based on a counter length, so the maximum decay time scales with the clock setup that is used. 表 7-1 shows the relationship of the NCODEC ratio to the maximum time available for the AGC decay. In practice, these maximum times are extremely long for audio applications and should not limit any practical AGC decay time that is needed by the system.

表 7-1. AGC Decay Time Restriction

NCODEC RATIO	MAXIMUM DECAY TIME (SECONDS)
1	4
1.5	5.6
2	8
2.5	9.6
3	11.2

表 7-1. AGC Decay Time Restriction (続き)

NCODEC RATIO	MAXIMUM DECAY TIME (SECONDS)
3.5	11.2
4	16
4.5	16
5	19.2
5.5	22.4
6	22.4

In this situation, the AGC considers the input signal as a silence and will set the noise threshold flag while reducing the gain down to 0 dB in steps of 0.5 dB every sample period. The gain stays at 0 dB unless the input speech signal average rises above the noise threshold setting. This ensures that noise does not get gained up in the absence of speech. Noise threshold level in the AGC algorithm is programmable from –30 dB to –90 dB relative to full scale. A disable noise gate feature is also available. This operation includes programmable debounce and hysteresis functionality to avoid the AGC gain from cycling between high gain and 0 dB when signals are near the noise threshold level. When the noise threshold flag is set, the status of gain applied by the AGC and the saturation flag should be ignored.

The Maximum PGA gain applicable can be set by the user, which restricts the maximum PGA gain that can be applied by the AGC algorithm. This can be used for limiting PGA gain in situations where environmental noise is greater than programmed noise threshold. It can be programmed from 0 dB to 59.5 dB in steps of 0.5 dB.

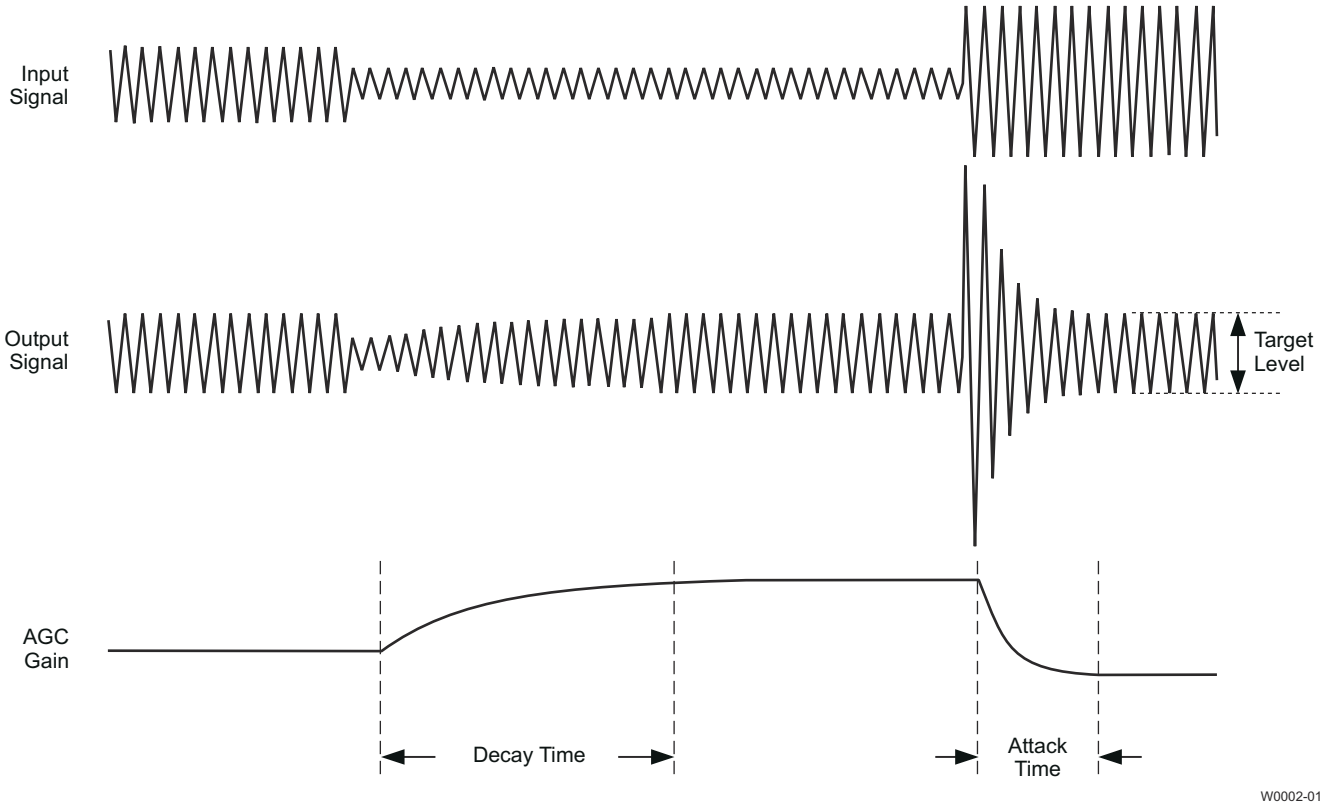

図 7-1. Typical Operation of the AGC Algorithm During Speech Recording

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The time constants here are correct when the ADC is not in double-rate audio mode. The time constants are achieved using the fS(ref) value programmed in the control registers. However, if the fS(ref) is set in the registers to, for example, 48 kHz, but the actual audio clock or PLL programming actually results in a different fS(ref) in practice, then the time constants would not be correct.

The actual AGC decay time maximum is based on a counter length, so the maximum decay time scales with the clock setup that is used. 表 7-1 shows the relationship of the NCODEC ratio to the maximum time available for the AGC decay. In practice, these maximum times are extremely long for audio applications and should not limit any practical AGC decay time that is needed by the system.

7.3.4 Stereo Audio DAC

The TLV320AIC3104-Q1 includes a stereo audio DAC supporting sampling rates from 8 kHz to 96 kHz. Each channel of the stereo audio DAC consists of a digital audio processing block, a digital interpolation filter, multibit digital delta-sigma modulator, and an analog reconstruction filter. The DAC is designed to provide enhanced performance at low sampling rates through increased oversampling and image filtering, thereby keeping quantization noise generated within the delta-sigma modulator and signal images strongly suppressed within the audio band to beyond 20 kHz. This is realized by keeping the upsampled rate constant at 128 $f_{S(ref)}$ and changing the oversampling ratio as the input sample rate is changed. For an $f_{S(ref)}$ of 48 kHz, the digital delta-sigma modulator always operates at a rate of 6.144 MHz. This ensures that quantization noise generated within the delta-sigma modulator stays low within the frequency band below 20 kHz at all sample rates. Similarly, for an $f_{S(ref)}$ rate of 44.1 kHz, the digital delta-sigma modulator always operates at a rate of 5.6448 MHz.

The following restrictions apply in the case when the PLL is powered down and double-rate audio mode is enabled in the DAC.

- Allowed Q values = 4, 8, 9, 12, 16
- Q values where equivalent $f_{S(ref)}$ can be achieved by turning on the PLL
- Q = 5, 6, 7 (set P = 5, 6, or 7, K = 16, and PLL enabled)
- Q = 10, 14 (set P = 5 or 7, K = 8, and PLL enabled)

7.3.5 Digital Audio Processing for Playback

The DAC channel consists of optional filters for de-emphasis and bass, treble, midrange level adjustment, speaker equalization, and 3D effects processing. The de-emphasis function is implemented by a programmable digital filter block with fully programmable coefficients (see page 1, registers 21 to 26 for the left channel and page 1, registers 47 to 52 for the right channel). If de-emphasis is not required in a particular application, this programmable filter block can be used for some other purpose. The de-emphasis filter transfer function is given by:

$$H(z) = \frac{N0 + N1 \times z^{-1}}{32,768 - D1 \times z^{-1}} \quad (2)$$

where the N0, N1, and D1 coefficients are fully programmable individually for each channel. The coefficients that should be loaded to implement standard de-emphasis filters are given in 表 7-2

表 7-2. De-Emphasis Coefficients for Common Audio Sampling Rates

SAMPLING FREQUENCY	N0	N1	D1
32 kHz	16,950	–1,220	17,037
44.1 kHz	15,091	–2,877	20,555
48 kHz(1)	14,677	–3,283	21,374

(1) The 48-kHz coefficients listed in 表 7-2 are used as defaults.

In addition to the de-emphasis filter block, the DAC digital effects processing includes a fourth-order digital IIR filter with programmable coefficients. This filter is implemented as a cascade of two biquad sections with the frequency response given by:

$$\left(\frac{N0 + 2 \times N1 \times z^{-1} + N2 \times z^{-2}}{32,768 - 2 \times D1 \times z^{-1} - D2 \times z^{-2}}\right)\left(\frac{N3 + 2 \times N4 \times z^{-1} + N5 \times z^{-2}}{32,768 - 2 \times D4 \times z^{-1} - D5 \times z^{-2}}\right) \quad (3)$$

The N and D coefficients are fully programmable, and the entire filter can be enabled or bypassed. The structure of the filtering when configured for independent channel processing is shown in 図 7-2, with LB1 corresponding to the first left-channel biquad filter using coefficients N0, N1, N2, D1, and D2. LB2 similarly corresponds to the second left-channel biquad filter using coefficients N3, N4, N5, D4, and D5. The RB1 and RB2 filters refer to the first and second right-channel biquad filters, respectively.

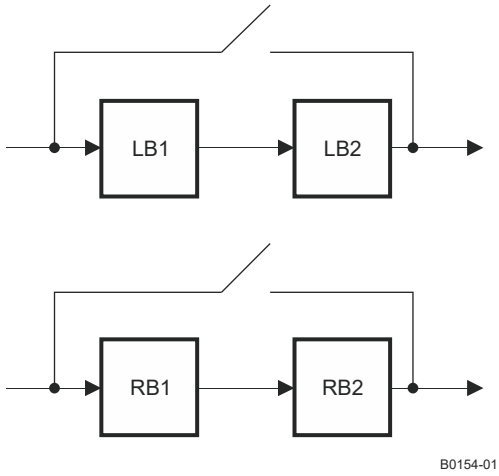

図 7-2. Structure of Digital Effects Processing for Channel Processing

The coefficients for this filter implement a variety of sound effects, with bass boost or treble boost being the most commonly used in portable audio applications. The default N and D coefficients in the device are given in 表 7-3 and implement a shelving filter with 0-dB gain from dc to approximately 150 Hz, at which point the filter rolls off to a 3-dB attenuation for higher frequency signals, thus giving a 3-dB boost to signals below 150 Hz. The N and D coefficients are represented by 16-bit, 2's-complement numbers with values ranging from –32,768 to 32,767.

表 7-3. Default Digital Effects Processing Filter Coefficients, When in Independent Channel Processing Configuration

COEFFICIENTS				
N0 = N3	**D1 = D4**	**N1 = N4**	**D2 = D5**	**N2 = N5**
27,619	32,131	–27,034	–31,506	26,461

The digital processing also includes capability to implement 3-D processing algorithms by providing means to process the mono mix of the stereo input, and then combine this with the individual channel signals for stereo output playback. The architecture of this processing mode, and the programmable filters available for use in the system, are shown in 図 7-3. Note that the programmable attenuation block provides a method of adjusting the level of 3-D effect introduced into the final stereo output. This, combined with the fully programmable biquad filters in the system, enables the user to optimize the audio effects for a particular system and provide extensive differentiation from other systems using the same device.

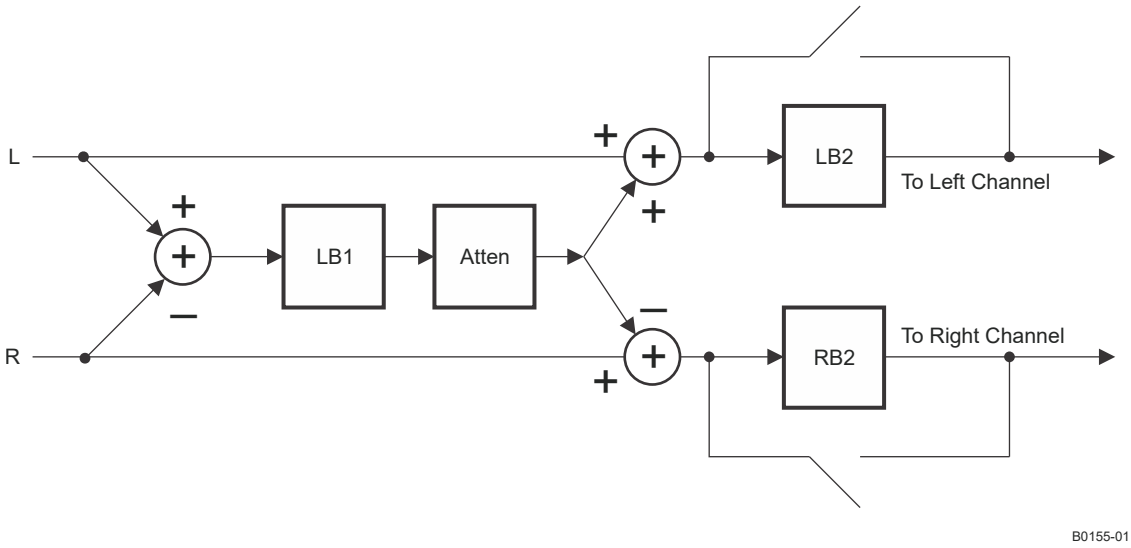

図 7-3. Architecture of Digital Audio Processing With 3-D Effects Enabled

It is recommended that the digital effects filters should be disabled while the filter coefficients are being modified. While new coefficients are being written to the device over the control port, it is possible that a filter using partially updated coefficients may actually implement an unstable system and lead to oscillation or objectionable audio output. By disabling the filters, changing the coefficients, and then re-enabling the filters, these types of effects can be entirely avoided.

7.3.6 Digital Interpolation Filter

The digital interpolation filter upsamples the output of the digital audio processing block by the required oversampling ratio before data are provided to the digital delta-sigma modulator and analog reconstruction filter stages. The filter provides a linear phase output with a group delay of 21 / f_S. In addition, programmable digital interpolation filtering is included to provide enhanced image filtering and reduce signal images caused by the upsampling process that are below 20 kHz. For example, upsampling an 8-kHz signal produces signal images at multiples of 8-kHz (that is, 8 kHz, 16 kHz, 24 kHz, and so forth). The images at 8 kHz and 16 kHz are below 20 kHz and are still audible to the listener; therefore, these images must be filtered heavily to maintain a good quality output. The interpolation filter is designed to maintain at least 65-dB rejection of images that are below 7.455 f_S. In order to use the programmable interpolation capability, program $f_{S(ref)}$ to a higher rate (restricted to be in the range of 39 kHz to 53 kHz when the PLL is in use), and the actual f_S is set using the NCODEC divider, where NCODEC = NDAC = NADC. For example, if f_S = 8 kHz is required, then $f_{S(ref)}$ can be set to 48 kHz and the DAC f_S set to $f_{S(ref)}$ / 6. This setting ensures that all images of the 8-kHz data are sufficiently attenuated well beyond a 20-kHz audible frequency range.

7.3.7 Delta-Sigma Audio DAC

The stereo audio DAC incorporates a third-order multibit delta-sigma modulator followed by an analog reconstruction filter. The DAC provides high-resolution, low-noise performance, using oversampling and noise shaping techniques. The analog reconstruction filter design consists of a six-tap analog FIR filter followed by a continuous-time RC filter. The analog FIR operates at a rate of 128 $f_{S(ref)}$ (6.144 MHz when $f_{S(ref)}$ = 48 kHz, 5.6448 MHz when $f_{S(ref)}$ = 44.1 kHz). Note that the DAC analog performance may be degraded by excessive clock jitter on the MCLK input. Therefore, care must be taken to keep jitter on this clock to a minimum.

7.3.8 Audio DAC Digital Volume Control

The audio DAC includes a digital volume control block which implements a programmable digital gain. The volume level can be varied from 0 dB to –63.5 dB in 0.5-dB steps, or set to mute, independently for each channel. The volume level of both channels can also be changed simultaneously by the master volume control. Gain changes are implemented with a soft-stepping algorithm, which only changes the actual volume by one

step per input sample, either up or down, until the desired volume is reached. The rate of soft-stepping can be slowed to one step per two input samples through a register bit.

Because of soft-stepping, the host does not know when the DAC has been actually muted. This may be important if the host wishes to mute the DAC before making a significant change, such as changing sample rates. In order to help with this situation, the device provides a flag back to the host via a read-only register bit that alerts the host when the part has completed the soft-stepping and the actual volume has reached the desired volume level. The soft-stepping feature can be disabled through register programming. If soft-stepping is enabled, the MCLK signal should be kept applied to the device until the DAC power-down flag is set. When this flag is set, the internal soft-stepping process and power-down sequence is complete, and the MCLK can then be stopped if desired.

The TLV320AIC3104-Q1 also includes functionality to detect when the user changes the selection of de\u0002emphasis or digital audio processing functionality. When the new selection is detected, the TLV320AIC3104-Q1 (1) soft-mutes the DAC volume control, (2) changes the operation of the digital effects processing to match the new selection, and (3) soft-unmutes the device. This avoids any possible pop/clicks in the audio output due to instantaneous changes in the filtering. A similar algorithm is used when first powering up or powering down the DAC. The circuit begins operation at power up with the volume control muted, then soft-steps it up to the desired volume level. At power down, the logic first soft-steps the volume down to a mute level, then powers down the circuitry.

7.3.9 Analog Output Common-mode Adjustment

The output common-mode voltage and output range of the analog output are determined by an internal band-gap reference, in contrast to other codecs that may use a scaled version of the analog supply. This scheme is used to reduce the coupling of noise that may be on the supply into the audio signal path.

However, due to the possible wide variation in analog supply range (2.7 V to 3.6 V), an output common-mode voltage setting of 1.35 V, which would be used for a 2.7-V supply case, would be overly conservative if the supply is actually much larger, such as 3.3 V or 3.6 V. In order to optimize device operation, the TLV320AIC3104-Q1 includes a programmable output common-mode level, which can be set by register programming to a level most appropriate to the actual supply range used by a particular customer. The output common-mode level can be varied among four different values, ranging from 1.35 V (most appropriate for low supply ranges, near 2.7 V) to 1.8 V (most appropriate for high supply ranges, near 3.6 V). Note that the recommended DVDD voltage is dependent on the common-mode setting, as shown in 表 7-4.

表 7-4. Appropriate Settings

CM SETTING	RECOMMENDED AVDD, DRVDD	RECOMMENDED DVDD
1.35 V	2.7 V–3.6 V	1.525 V–1.95 V
1.5 V	3 V–3.6 V	1.65 V–1.95 V
1.65 V	3.3 V–3.6 V	1.8 V–1.95 V
1.8 V	3.6 V	1.95 V

7.3.10 Audio DAC Power Control

The stereo DAC can be fully powered up or down, and in addition, the analog circuitry in each DAC channel can be powered up or down independently. This provides power savings when only a mono playback stream is needed.

7.3.11 Audio Analog Inputs

The TLV320AIC3104-Q1 includes six single-ended audio inputs. These pins connect through series resistors and switches to the virtual ground terminals of two fully differential operational amplifiers (one per ADC/PGA channel). By selecting to turn on only one set of switches per operational amplifier at a time, the inputs can be multiplexed effectively to each ADC/PGA channel.

By selecting to turn on multiple sets of switches per operational amplifier at a time, mixing can also be achieved. Mixing of multiple inputs can easily lead to PGA outputs that exceed the range of the internal operational amplifiers, resulting in saturation and clipping of the mixed output signal. Whenever mixing is being implemented, the user should take adequate precautions to avoid such saturation from occurring. In general, the mixed signal should not exceed 2 V_{P-P} (single-ended).

In most mixing applications, there is also a general need to adjust the levels of the individual signals being mixed. For example, if a soft signal and a large signal are to be mixed and played together, the soft signal generally should be amplified to a level comparable to the large signal before mixing. In order to accommodate this need, the TLV320AIC3104-Q1 includes input level control on each of the individual inputs before they are mixed or multiplexed into the ADC PGAs, with gain programmable from 0 dB to –12 dB in 1.5-dB steps. Note that this input level control is not intended to be a volume control, but instead used occasionally for level setting. Soft-stepping of the input level control settings is implemented in this device, with the speed and functionality following the settings used by the ADC PGA for soft-stepping.

図 7-4 sshows the single-ended mixing configuration for the left-channel ADC PGA, which enables mixing of the signals LINE1L, LINE2L, LINE1R, MIC2L, and MIC2R. The right-channel ADC PGA mix is similar, enabling mixing of the signals LINE1R, LINE2R, LINE1L, MIC2L, and MIC2R.

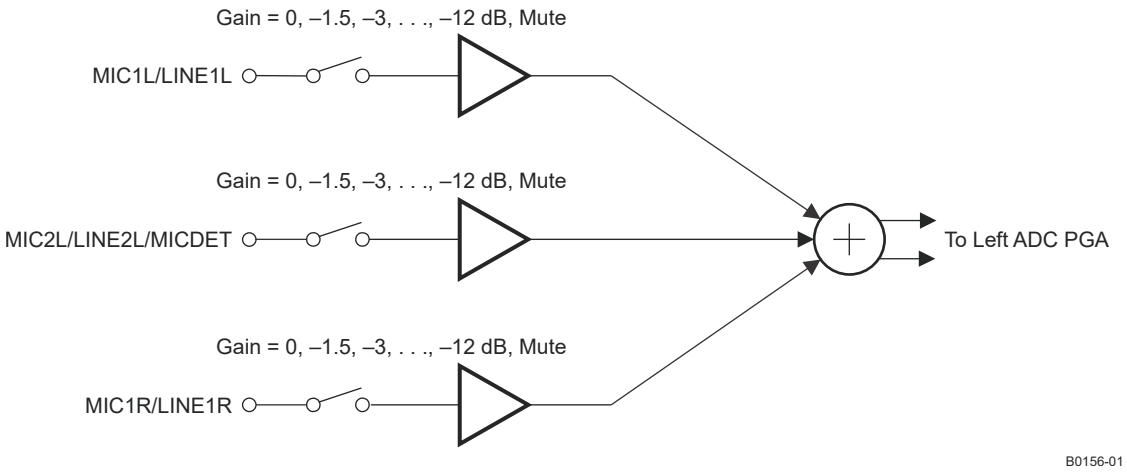

図 7-4. Single-Ended Analog Input Mixing Configuration

7.3.12 Analog Input Bypass Path Functionality

The TLV320AIC3104-Q1 includes the additional ability to route some analog input signals past the integrated data converters, for mixing with other analog signals and then direct connection to the output drivers. The TLV320AIC3104-Q1 supports this in a low-power mode by providing a direct analog path through the device to the output drivers, while all ADCs and DACs can be completely powered down to save power.

When programmed correctly, the device can pass the LINE1L and LINE1R signals directly to the output stage.

7.3.13 ADC PGA Signal Bypass Path Functionality

In addition to the input bypass path described previously, the TLV320AIC3104-Q1 also includes the ability to route the ADC PGA output signals past the ADC, for mixing with other analog signals and then direct connection to the output drivers. These bypass functions are described in more detail in the sections on output mixing and output driver configurations.

7.3.14 Input Impedance and VCM Control

The TLV320AIC3104-Q1 includes several programmable settings to control analog input pins, particularly when they are not selected for connection to an ADC PGA. The default option allows unselected inputs to be put into a high-impedance state, such that the input impedance seen looking into the device is extremely high. Note, however, that the pins on the device do include protection diode circuits connected to AVDD and AVSS. Thus, if any voltage is driven onto a pin approximately one diode drop (~0.6 V) above AVDD or one diode drop below AVSS, these protection diodes begin conducting current, resulting in an effective impedance that no longer appears as a high-impedance state.

n most cases, the analog input pins on the TLV320AIC3104-Q1 should be AC-coupled to analog input sources, the exception to this being if an ADC is being used for dc voltage measurement. The AC-coupling capacitor causes a high-pass filter pole to be inserted into the analog signal path, so the size of the capacitor must be chosen to move that filter pole sufficiently low in frequency to cause minimal effect on the processed analog signal. The input impedance of the analog inputs when selected for connection to an ADC PGA varies with the setting of the input level control, starting at approximately 20 kΩ with an input level control setting of 0 dB, and increasing to approximately 80 kΩ when the input level control is set at –12 dB. For example, using a 0.1-µF AC\u0002coupling capacitor at an analog input results in a high-pass filter pole of 80 Hz when the 0-dB input level control setting is selected.

7.3.15 MICBIAS Generation

The TLV320AIC3104-Q1 includes a programmable microphone bias output voltage (MICBIAS), capable of providing output voltages of 2 V or 2.5 V (both derived from the on-chip band-gap voltage) with 4-mA output current drive. In addition, the MICBIAS can be programmed to be connected to AVDD directly through an on-chip switch, or it can be powered down completely when not needed, for power savings. This function is controlled by register programming in page 0, register 25.

7.3.16 Analog Fully Differential Line Output Drivers

The TLV320AIC3104-Q1 has two fully differential line output drivers, each capable of driving a 10-kΩ differential load. The output stage design leading to the fully differential line output drivers is shown in 図 7-5 and 図 7-6. This design includes extensive capability to adjust signal levels independently before any mixing occurs, beyond that already provided by the PGA gain and the DAC digital volume control.

The PGA_L/R signals refer to the outputs of the ADC PGA stages that are similarly passed around the ADC to the output stage. Note that because both left- and right-channel signals are routed to all output drivers, a mono mix of any of the stereo signals can easily be obtained by setting the volume controls of both left- and right\u0002channel signals to –6 dB and mixing them. Undesired signals can also be disconnected from the mix through register control

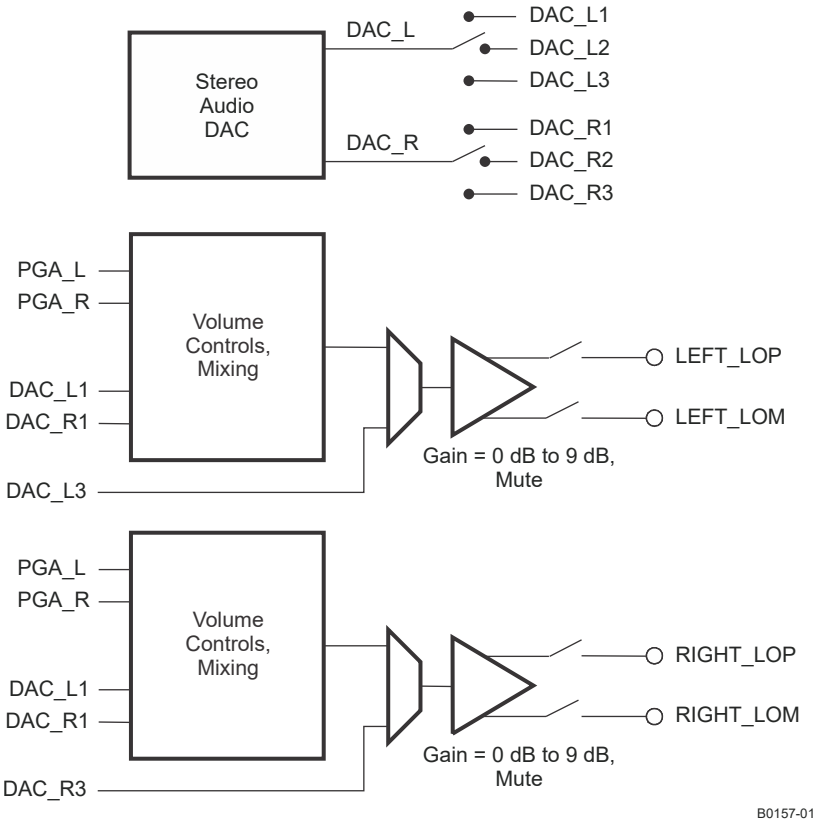

図 7-5. Architecture of Output Stage Leading to Fully-Differential Line Output Drivers

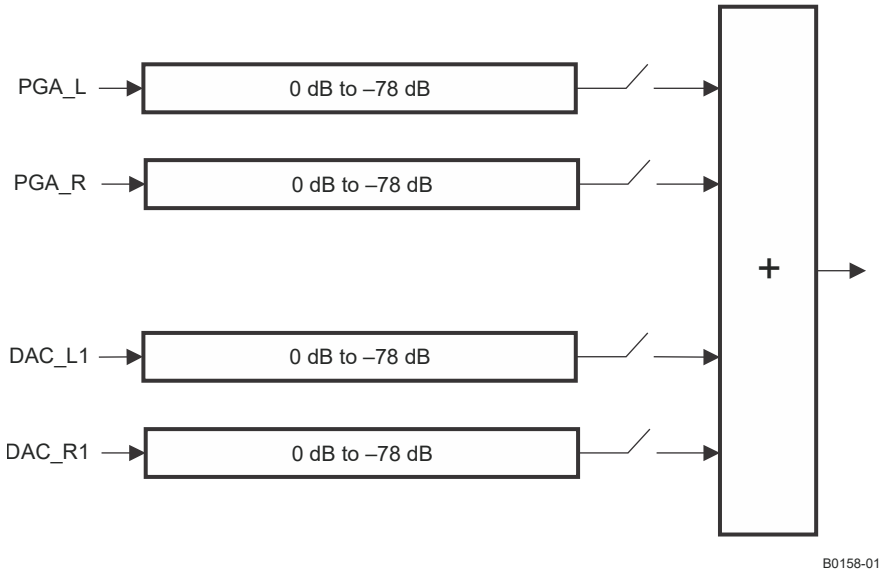

図 7-6. Detail of Volume Control and Mixing Function

The DAC_L/R signals are the outputs of the stereo audio DAC, which can be steered by register control based on the requirements of the system. If mixing of the DAC audio with other signals is not required, and the DAC output is only needed at the stereo line outputs, then it is recommended to use the routing through path DAC_L3/R3 to the fully differential stereo line outputs. This results not only in higher-quality output performance, but also in lower-power operation, because the analog volume controls and mixing blocks ahead of these drivers can be powered down.

If instead the DAC analog output must be routed to multiple output drivers simultaneously (such as to LEFT_LOP/M and RIGHT_LOP/M) or must be mixed with other analog signals, then the DAC outputs should be switched through the DAC_L1/R1 path. This option provides the maximum flexibility for routing of the DAC analog signals to the output drivers.

The TLV320AIC3104-Q1 includes an output level control on each output driver with limited gain adjustment from 0 dB to 9 dB. The output driver circuitry in this device is designed to provide a low-distortion output while playing full-scale stereo DAC signals at a 0-dB gain setting. However, a higher amplitude output can be obtained at the cost of increased signal distortion at the output. This output level control allows the user to make this tradeoff based on the requirements of the end equipment. Note that this output level control is not intended to be used as a standard output volume control. It is expected to be used only sparingly for level setting, i.e., adjustment of the full-scale output range of the device.

Each differential line output driver can be powered down independently of the others when it is not needed in the system. When placed into power down through register programming, the driver output pins are placed into a high-impedance state.

7.3.17 Analog High-Power Output Drivers

The TLV320AIC3104-Q1 includes four high-power output drivers with extensive flexibility in their usage. These output drivers are individually capable of driving 30 mW each into a 16-Ω load in single-ended configuration, and they can be used in pairs connected in bridge-terminated load (BTL) configuration between two driver outputs.

The high-power output drivers can be configured in a variety of ways, including:

1. Driving up to two fully differential output signals
2. Driving up to four single-ended output signals
3. Driving two single-ended output signals, with one or two of the remaining drivers driving a fixed VCM level, for a pseudo-differential stereo output

The output stage architecture leading to the high-power output drivers is shown in 図 7-7, with the volume control and mixing blocks being effectively identical to those shown in 図 7-6. Note that each of these drivers has an output level control block like those included with the line output drivers, allowing gain adjustment up to 9 dB on the output signal. As in the previous case, this output level adjustment is not intended to be used as a standard volume control, but instead is included for additional full-scale output signal-level control.

Two of the output drivers, HPROUT and HPLOUT, include a direct connection path for the stereo DAC outputs to be passed directly to the output drivers and bypass the analog volume controls and mixing networks, using theDAC_L2/R2 path. As in the line output case, this functionality provides the highest quality DAC playback performance with reduced power dissipation, but can only be used if the DAC is not being routed to multiple output drivers simultaneously, and if mixing of the DAC output with other analog signals is not needed.

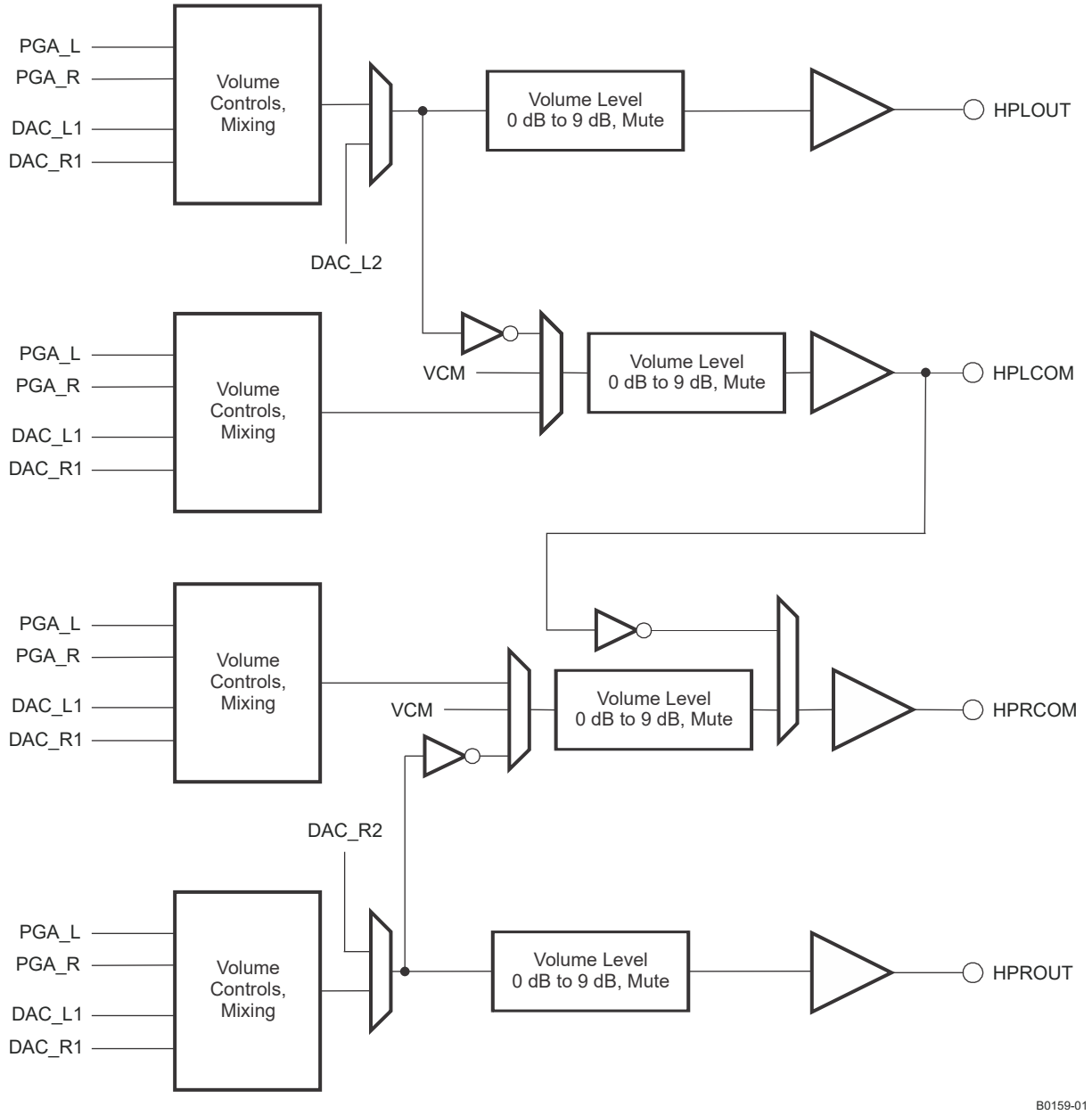

図 7-7. Architecture of Output Stage Leading to High-Power Output Drivers

The high-power output drivers include additional circuitry to avoid artifacts on the audio output during power-on and power-off transient conditions. The user should first program the type of output configuration being used in page 0, register 14, to allow the device to select the optimal power-up scheme to avoid output artifacts. The power-up delay time for the high-power output drivers is also programmable over a wide range of time delays, from instantaneous up to 4 s, using page 0, register 42.

When these output drivers are powered down, they can be placed into a variety of output conditions based on register programming. If lowest-power operation is desired, then the outputs can be placed into a high-impedance state, and all power to the output stage is removed. However, this generally results in the output nodes drifting to rest near the upper or lower analog supply, due to small leakage currents at the pins. This then results in a longer delay requirement to avoid output artifacts during driver power on. In order to reduce this required power-on delay, the TLV320AIC3104-Q1 includes an option for the output pins of the drivers to be weakly driven to the VCM level they would normally rest at when powered with no signal applied. This output VCM level is determined by an internal band-gap voltage reference, and thus results in extra power dissipation when the drivers are in power down. However, this option provides the fastest method for transitioning the drivers from power down to full-power operation without any output artifact introduced.

The device includes a further option that falls between the other two—although it requires less power drawn while the output drivers are in power down, it also takes a slightly longer delay to power up without artifact than if the band-gap reference is kept alive. In this alternate mode, the powered-down output driver pin is weakly drive nto a voltage of approximately half the DRVDD1/2 supply level using an internal voltage divider. This voltage does not match the actual VCM of a fully powered driver, but due to the output voltage being close to its final value, a much shorter power-up delay time setting can be used and still avoid any audible output artifacts. These output voltage options are controlled in page 0, register 42.

The high-power output drivers can also be programmed to power up first with the output level (gain) control in a highly attenuated state; then the output driver automatically reduces the output attenuation slowly to reach the programmed output gain. This capability is enabled by default but can be enabled in page 0, register 40.

7.3.18 Short-Circuit Output Protection

The TLV320AIC3104-Q1 includes programmable short-circuit protection for the high-power output drivers, for maximum flexibility in a given application. By default, if these output drivers are shorted, they automatically limit the maximum amount of current that can be sourced to or sunk from a load, thereby protecting the device from an overcurrent condition. In this mode, the user can read page 0, register 95 to determine whether the part is in short-circuit protection or not, and then decide whether to program the device to power down the output drivers. However, the device includes further capability to power down an output driver automatically whenever it goes into short-circuit protection, without requiring intervention from the user. In this case, the output driver stays in a power-down condition until the user specifically programs it to power down and then power back up again, to clear the short-circuit flag.

7.3.19 Jack and Headset Detection

The TLV320AIC3104-Q1 includes extensive capability to monitor a headphone, microphone, or headset jack, determine if a plug has been inserted into the jack, and then determine what type of headset or headphone is wired to the plug. 図 7-8 shows one configuration of the device that enables detection and determination of headset type when a pseudo-differential (capacitor free) mono headphone output configuration is used. The registers used for this function are registers 14, 96, 97, and 13, page 0. The type of headset detected can be read back from register 13, page 0. For best results, select a MICBIAS value as high as possible and program the output driver common-mode level at a 1.35-V or 1.5-V level.

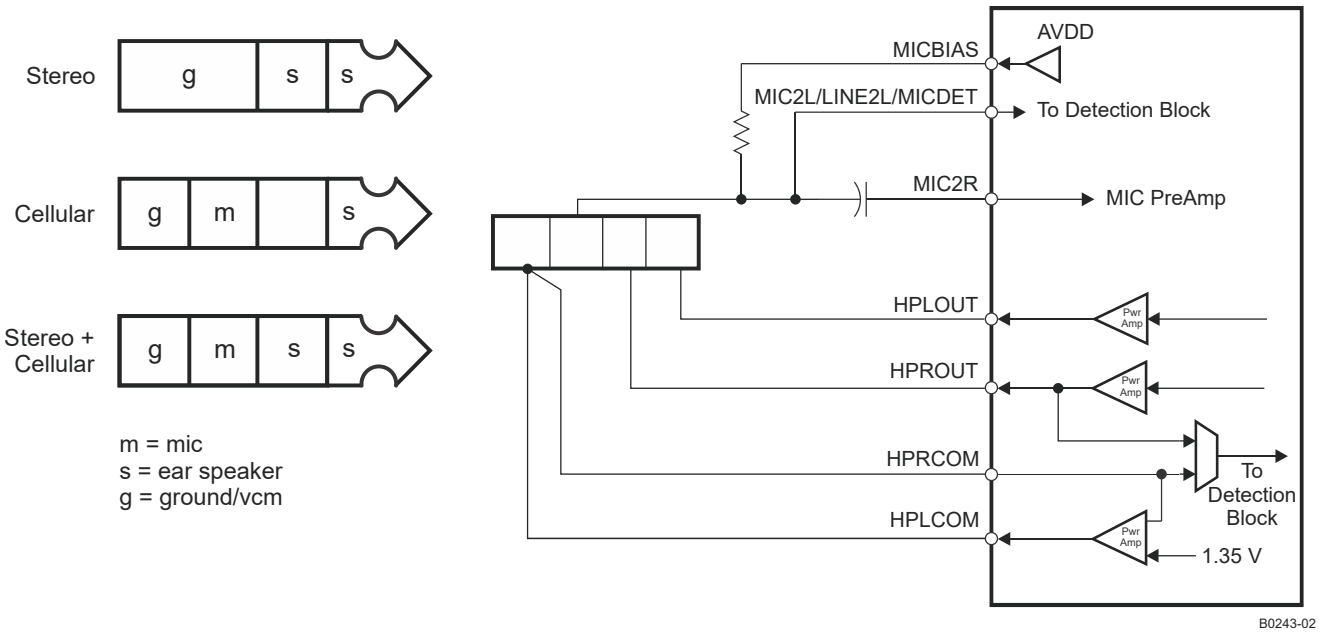

図 7-8. Configuration of Device for Jack Detection Using Pseudo-Differential (Capless) Headphone Output Connection

A modified output configuration used when the output drivers are AC-coupled is shown in 図 7-9. Note that in this mode, the device cannot accurately determine if the inserted headphone is a mono or stereo headphone.

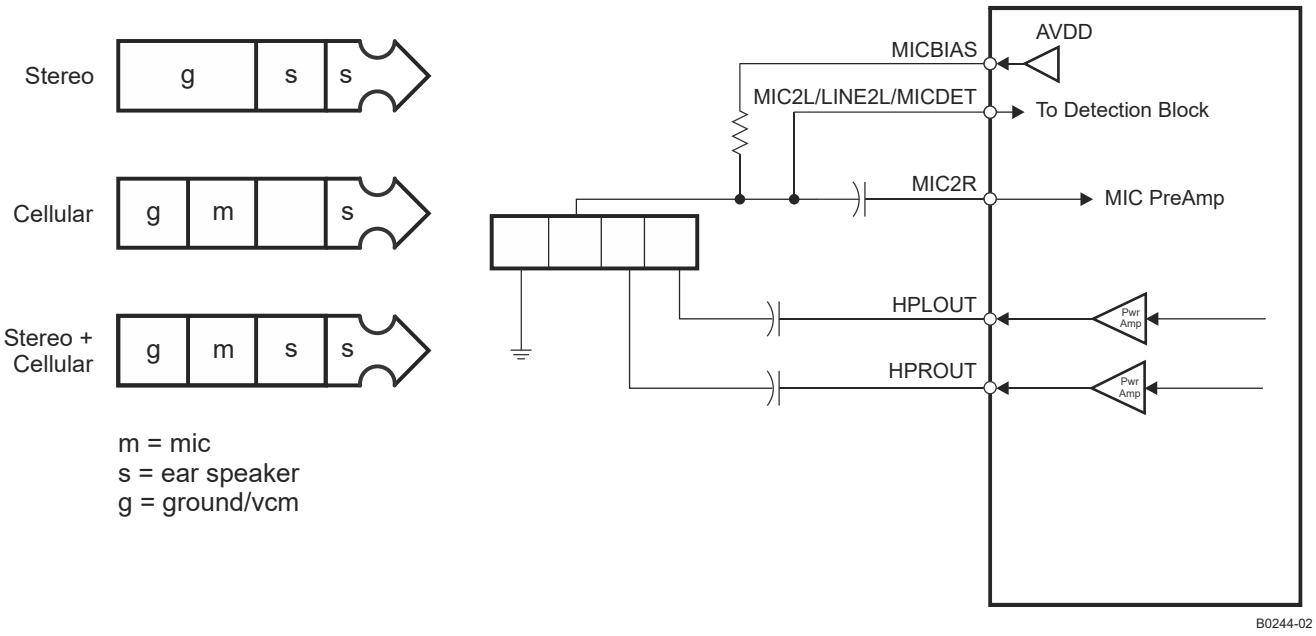

図 7-9. Configuration of Device for Jack Detection Using AC-Coupled Stereo Headphone Output Connection

An output configuration for the case of the outputs driving fully differential stereo headphones is shown in 図 7-10. In this mode, there is a requirement on the jack side that either HPLCOM or HPLOUT get shorted to ground if the plug is removed, which can be implemented using a spring terminal in a jack. For this mode to function properly, short-circuit detection should be enabled and configured to power down the drivers if a short\u0002circuit is detected. The registers that control this functionality are in page 0, register 38, bits D2 to D1.

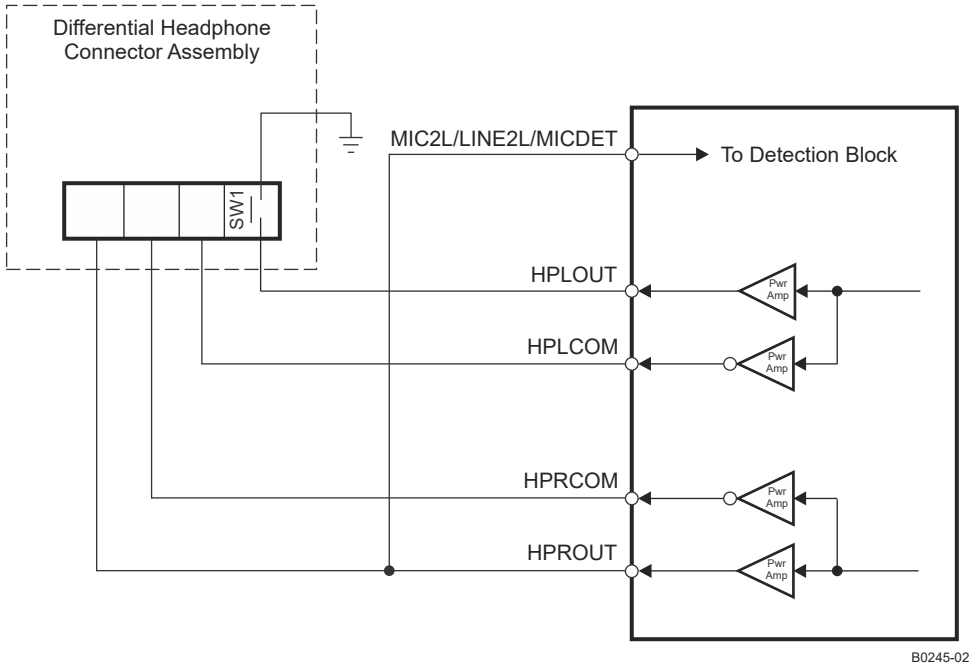

図 7-10. Configuration of Device for Jack Detection Using Fully-Differential Stereo Headphone Output Connection

7.4 Device Functional Modes

7.4.1 Digital Audio Processing for Record Path

In applications where record-only is selected, and DAC is powered down, the playback path signal processing blocks can be used in the ADC record path. These filtering blocks can support high-pass, low-pass, band-pass or notch filtering. In this mode, the record-only path has switches SW-D1 through SW-D4 closed, and reroutes the ADC output data through the digital signal processing blocks. Because the DAC digital signal processing blocks are being re-used, naturally the addresses of these digital filter coefficients are the same as for the DAC digital processing and are located on page 1, registers 1 to 52. This record-only mode is enabled by powering down both DACs by writing to page 0, register 37, bits D7 to D6 (D7 = D6 = 0). Next, enable the digital filter pathway for the ADC by writing a 1 to page 0, register 107, bit D3. (Note, this pathway is only enabled if both DACs are powered down.) This record-only path can be seen in 図 7-11.

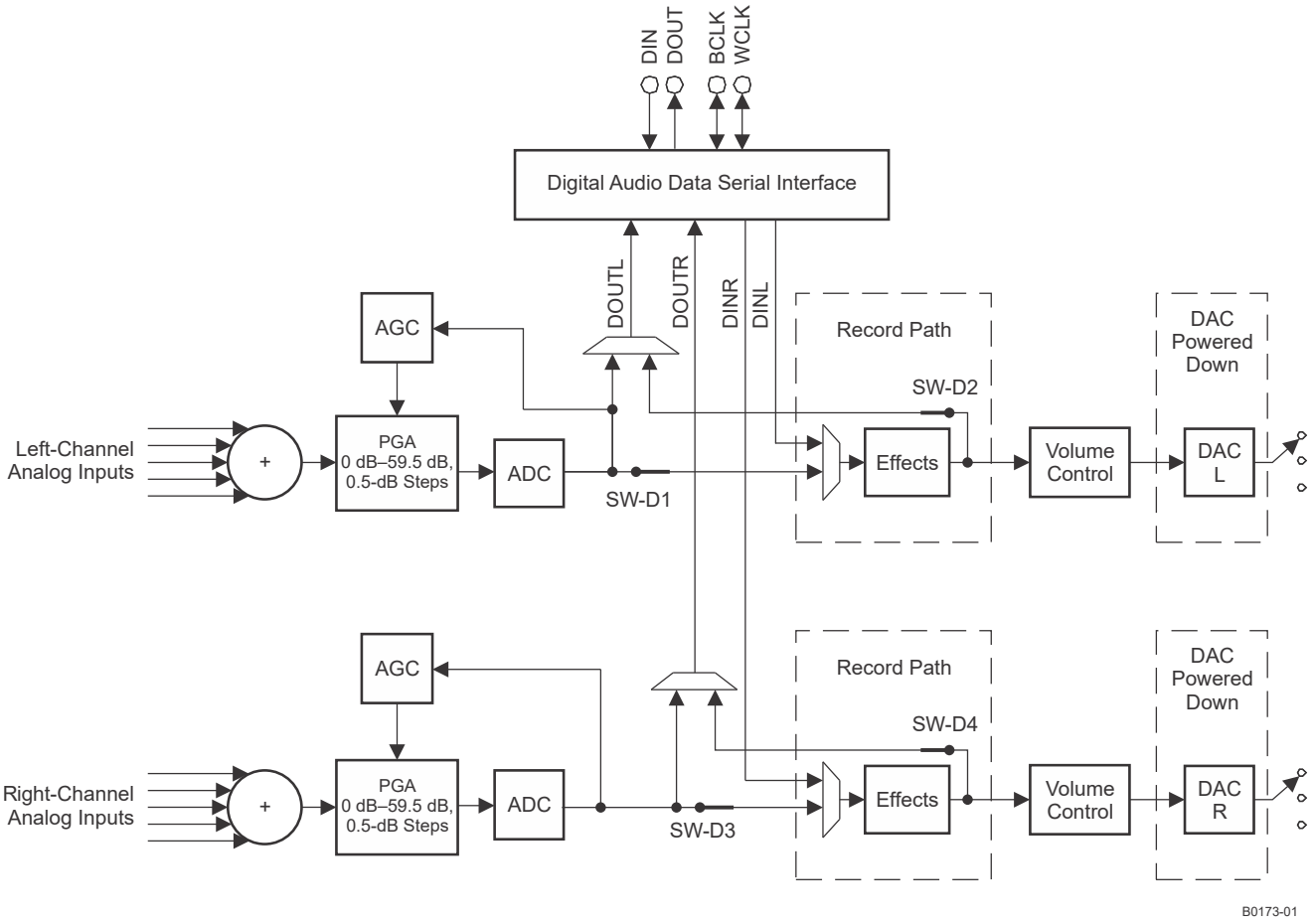

図 7-11. Record-Only Mode With Digital Processing Path Enabled

7.4.2 Increasing DAC Dynamic Range

The TLV320AIC3104-Q1 allows trading off dynamic range with power consumption. The DAC dynamic range can be increased by writing to page 0, register 109, bits D7 to D6. The lowest DAC current setting is the default, and the dynamic range is displayed in *Electrical Characteristics*. Increasing the current can increase the DAC dynamic range by up to 1.5 dB.

7.4.3 Passive Analog Bypass During Power Down

Programming the TLV320AIC3104-Q1 to passive analog bypass occurs by configuring the output stage switches for passthrough. This is done by opening switches SW-L0, SW-L3, SW-R0, and SW-R3 and closing SW-L1 and SW-R1. See 図 7-12. Programming this mode is done by writing to page 0, register 108.

Connecting the MIC1LP/LINE1LP input signal to the LEFT_LOP pin is done by closing SW-L1 and opening SWL0; this action is done by writing a 1 to page 0, register 108, bit D0. Connecting the MIC1LM/LINE1LM input signal to the LEFT_LOM pin is done by closing SW-L4 and opening SW-L3; this action is done by writing a 1 to page 0, register 108, bit D1.

Connecting the MIC1RP/LINE1RP input signal to the RIGHT_LOP pin is done by closing SW-R1 and opening SW-R0; this action is done by writing a 1 to page 0, register 108, bit D4. Connecting MIC1RM/LINE1RM input signal to the RIGHT_LOM pin is done by closing SW-R4 and opening SW-R3; this action is done by writing a 1 to page 0, register 108, bit D5. A diagram of the passive analog bypass mode configuration is shown in 図 7-12.

In general, connecting two switches to the same output pin should be avoided, as this error shorts two input signals together, and would likely cause distortion of the signal as the two signals are in contention. Poor frequency response would also likely occur.

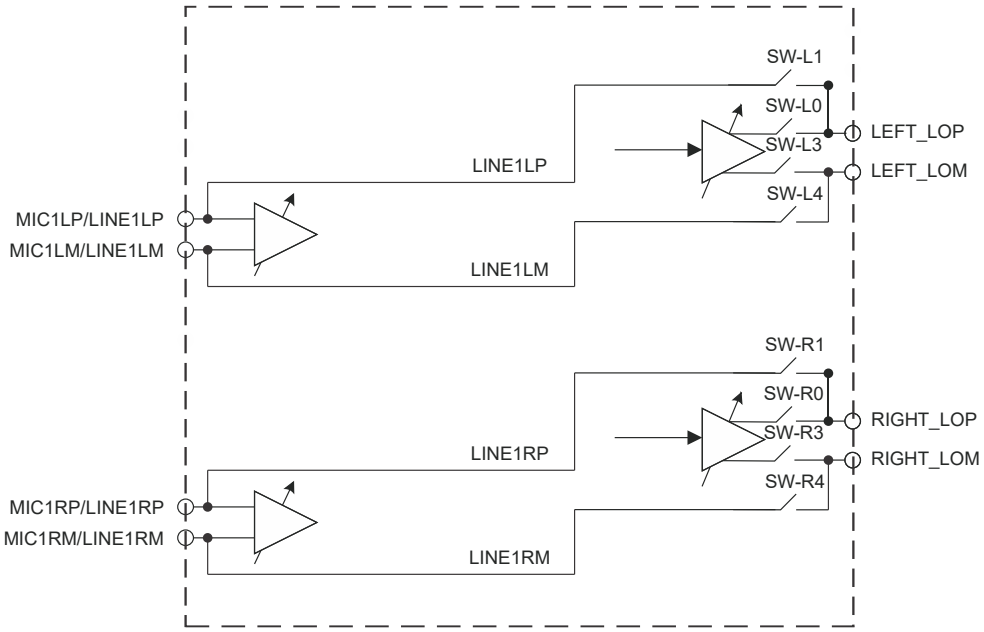

図 7-12. Passive Analog Bypass Mode Configuration

7.4.4 Hardware Reset

The TLV320AIC3104-Q1 requires a hardware reset after power-up for proper operation. After all power supplies are at their specified values, the $\overline{\text{RESET}}$ pin must be driven low for at least 10 ns. If this reset sequence is not performed, the TLV320AIC3104-Q1 may not respond properly to register reads or writes.

In cases where the ESD events generate a device reset, TI recommends to add at least a 1-nF capacitor connected between the RESET pin and DVSS. This capacitor avoids ESD events that could place the codec in default state. A 10-kΩ pullup resistor can be added to the RESET pin in addition to the capacitor.

This device has a software reset (page 0, register 1) that can be used by the host to reset all registers on page 0 and page 1 to their reset values. In cases where changes are needed only to routing or volume-control registers, the changes should be accomplished by writing directly to the appropriate registers rather than using the software or hardware reset.

7.5 Programming

7.5.1 Digital Control Serial Interface

The register map of the TLV320AIC3104-Q1 actually consists of two pages of registers, with each page containing 128 registers. The register at address zero on each page is used as a page-control register, and writing to this register determines the active page for the device. All subsequent read/write operations access the page that is active at the time, unless a register write is performed to change the active page. The active page defaults to page 0 on device reset.

For example, at device reset, the active page defaults to page 0, and thus all register read/write operations for addresses 1 to 127 access registers in page 0. If registers on page 1 must be accessed, the user must write the 8-bit sequence 0x01 to register 0, the page control register, to change the active page from page 0 to page 1. After this write, it is recommended that the user also read back the page control register, to ensure the change in page control has occurred properly. Future read/write operations to addresses 1 to 127 now access registers in page 1. When page-0 registers must be accessed again, the user writes the 8-bit sequence 0x00 to register 0, the page control register, to change the active page back to page 0. After a recommended read of the page control register, all further read/write operations to addresses 1 to 127 access page-0 registers again.

7.5.2 I²C Control Interface

The TLV320AIC3104-Q1 supports the I 2C control protocol using 7-bit addressing and is capable of both standard and fast modes. For I 2C fast mode, note that the minimum timing for each of tHD-STA, tSU-STA, and tSU-STO is 0.9 µs, as seen in 図 7-13. The TLV320AIC3104-Q1 responds to the I 2C address of 001 1000. I 2C is a two-wire, open\u0002drain interface supporting multiple devices and masters on a single bus. Devices on the I 2C bus only drive the bus lines LOW by connecting them to ground; they never drive the bus lines HIGH. Instead, the bus wires are pulled HIGH by pullup resistors, so the bus wires are HIGH when no device is driving them LOW. This way, two devices cannot conflict; if two devices drive the bus simultaneously, there is no driver contention.

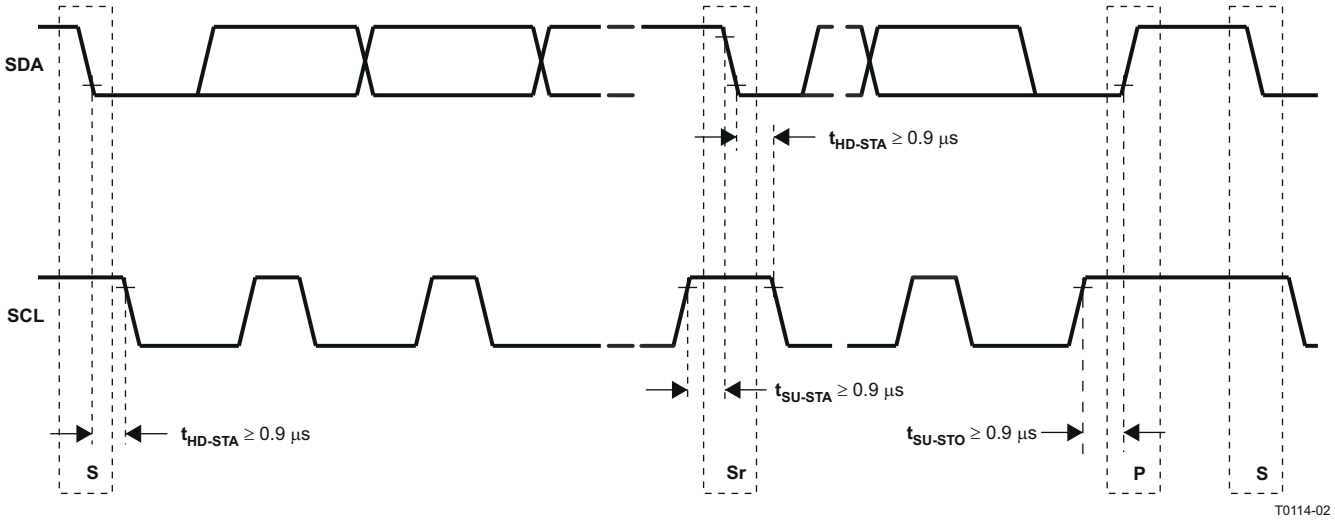

図 7-13. I²C Interface Timing

Communication on the I²C bus always takes place between two devices, one acting as the master and the other acting as the slave. Both masters and slaves can read and write, but slaves can only do so under the direction of the master. Some I²C devices can act as masters or slaves, but the TLV320AIC3104-Q1 can only act as a slave device.

An I 2C bus consists of two lines, SDA and SCL. SDA carries data; SCL provides the clock. All data is transmitted across the I 2C bus in groups of eight bits. To send a bit on the I 2C bus, the SDA line is driven to the appropriate level while SCL is LOW (a LOW on SDA indicates the bit is zero; a HIGH indicates the bit is one).

Once the SDA line has settled, the SCL line is brought HIGH, then LOW. This pulse on SCL clocks the SDA bit into the receiver shift register.

The I^{2}C bus is bidirectional: the SDA line is used both for transmitting and receiving data. When a master reads from a slave, the slave drives the data line; when a master sends to a slave, the master drives the data line. Under normal circumstances the master drives the clock line.

Most of the time the bus is idle, no communication is taking place, and both lines are HIGH. When communication is taking place, the bus is active. Only master devices can start a communication. They do this by causing a START condition on the bus. Normally, the data line is only allowed to change state while the clock line is LOW. If the data line changes state while the clock line is HIGH, it is either a START condition or its counterpart, a STOP condition. A START condition is when the clock line is HIGH and the data line goes from HIGH to LOW. A STOP condition is when the clock line is HIGH and the data line goes from LOW to HIGH.

After the master issues a START condition, it sends a byte that indicates which slave device it wants to communicate with. This byte is called the address byte. Each device on an I ^{2}C bus has a unique 7-bit address to which it responds. (Slaves can also have 10-bit addresses; see the I ^{2}C specification for details.) The master sends an address in the address byte, together with a bit that indicates whether it wishes to read from or write to the slave device.

Every byte transmitted on the I^{2}C bus, address or data, is acknowledged with an acknowledge bit. When a master finishes sending a byte (eight data bits) to a slave, the master stops driving SDA and waits for the slave to acknowledge the byte. The slave acknowledges the byte by pulling SDA low. The master then sends a clock pulse to clock the acknowledge bit. Similarly, when a master finishes reading a byte, the master pulls SDA low to acknowledge this operation to the slave. The master then sends a clock pulse to clock the bit.

A not-acknowledge is performed by simply leaving SDA HIGH during an acknowledge cycle. If a device is not present on the bus and the master attempts to address the device, the master receives a not-acknowledge because no device is present at that address to pull the line LOW.

When a master has finished communicating with a slave, it may issue a STOP condition. When a STOP condition is issued, the bus becomes idle again. A master may also issue another START condition. When a START condition is issued while the bus is active, it is called a repeated START condition.

The TLV320AIC3104-Q1 also responds to and acknowledges a general call, which consists of the master issuing a command with a slave-address byte of 00h.

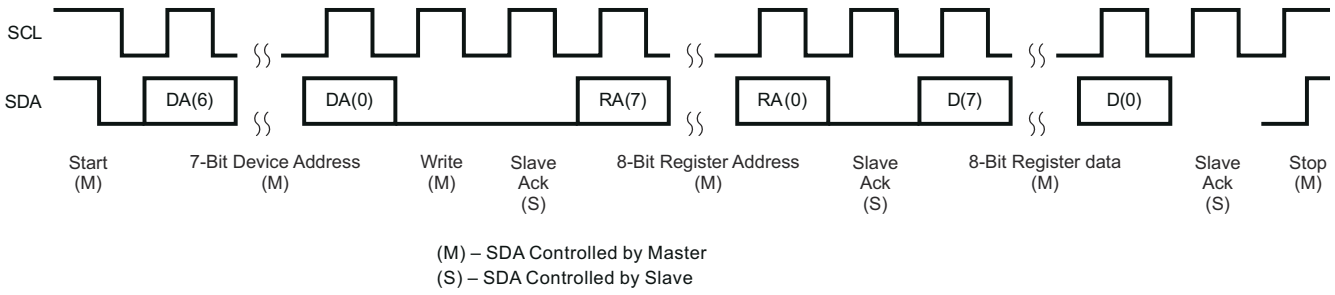

図 7-14. I^{2}C Write

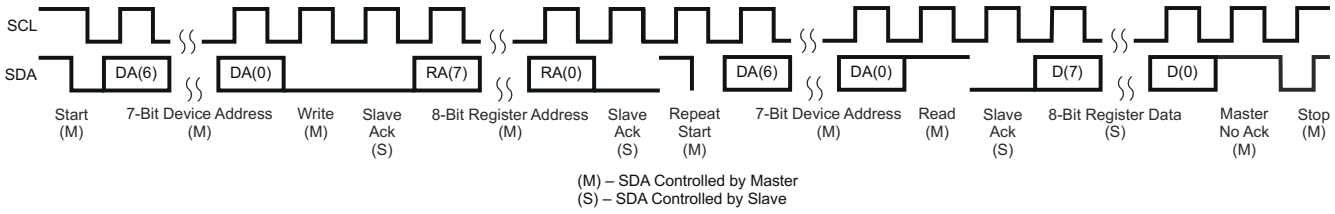

図 7-15. I²C Read

In the case of an I ²C register write, if the master does not issue a STOP condition, then the device enters auto\u0002increment mode. So in the next eight clocks, the data on SDA is treated as data for the next incremental register

Similarly, in the case of an I²C register read, after the device has sent out the 8-bit data from the addressed register, if the master issues an acknowledge, the slave takes over control of the SDA bus and transmits for the next 8 clocks the data of the next incremental register.

7.5.3 I²C Bus Debug in a Glitched System

Occasionally, some systems may encounter noise or glitches on the I²C bus. In the unlikely event that this affects bus performance, then it can be useful to use the I²C Debug register. This feature terminates the I²C bus error allowing this I²C device and system to resume communications. The I²C bus error detector is enabled by default. The TLV320AIC3104-Q1 I²C error detector status can be read from page 0, register 107, bit D0. If desired, the detector can be disabled by writing to page 0, register 107, bit D2.

7.5.4 Digital Audio Data Serial Interface

Audio data is transferred between the host processor and the TLV320AIC3104-Q1 via the digital audio data serial interface. The audio bus of the TLV320AIC3104-Q1 can be configured for left- or right-justified, I ²S, DSP, or TDM modes of operation, where communication with standard audio interfaces is supported within the TDM mode. These modes are all MSB-first, with data width programmable as 16, 20, 24, or 32 bits. In addition, the word clock (WCLK) and bit clock (BCLK) can be independently configured in either master or slave mode, for flexible connectivity to a wide variety of processors.

The word clock (WCLK) is used to define the beginning of a frame, and can be programmed as either a pulse or a square-wave signal. The frequency of this clock corresponds to the selected ADC and DAC sampling frequency.

The bit clock (BCLK) is used to clock in and out the digital audio data across the serial bus. When in master mode, this signal can be programmed in two further modes: continuous transfer mode, and 256-clock mode. In continuous transfer mode, only the minimal number of bit clocks required to transfer the audio data are generated, so in general the number of bit clocks per frame is two times the data width. For example, if the data width is chosen as 16 bits, then 32-bit clocks are generated per frame. If the bit clock signal in master mode is to be used by a PLL in another device, then the 16-bit or 32-bit data-width selections are recommended be used. These cases result in a low-jitter bit clock signal being generated, with frequencies of 32 f_S or 64 f_S. For a 20-bit and 24-bit data width in master mode, the bit clocks generated in each frame are not all of equal period because the device does not have a clean 40-f_S or 48-f_S clock signal readily available. The average frequency of the bit clock signal is still accurate in these cases (40 f_S or 48 f_S), but the resulting clock signal has higher jitter than in the 16-bit and 32-bit cases.

In 256-clock mode, a constant 256 bit clocks per frame are generated, independent of the data width chosen. The TLV320AIC3104-Q1 further includes programmability to place the DOUT line in the high-impedance state during all bit clocks when valid data are not being sent. By combining this capability with the ability to program at what bit clock in a frame the audio data begins, time-division multiplexing (TDM) can be accomplished, resulting in multiple codecs able to use a single audio serial data bus.

When the digital audio data serial interface is powered down when configured in master mode, the pins associated with the interface are put into a high-impedance state.

7.5.5 Right-Justified Mode

In right-justified mode, the LSB of the left channel is valid on the rising edge of the bit clock preceding the falling edge of word clock. Similarly, the LSB of the right channel is valid on the rising edge of the bit clock preceding the rising edge of the word clock.

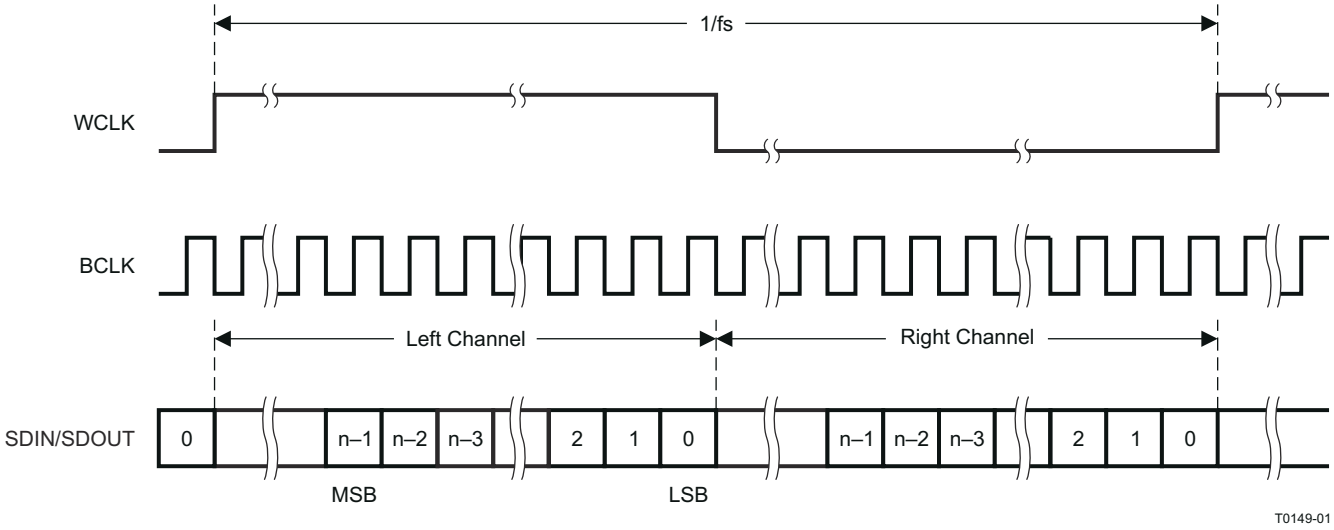

図 7-16. Right-Justified Serial Data Bus Mode Operation

7.5.6 Left-Justified Mode

In left-justified mode, the MSB of the right channel is valid on the rising edge of the bit clock following the falling edge of the word clock. Similarly, the MSB of the left channel is valid on the rising edge of the bit clock following the rising edge of the word clock.

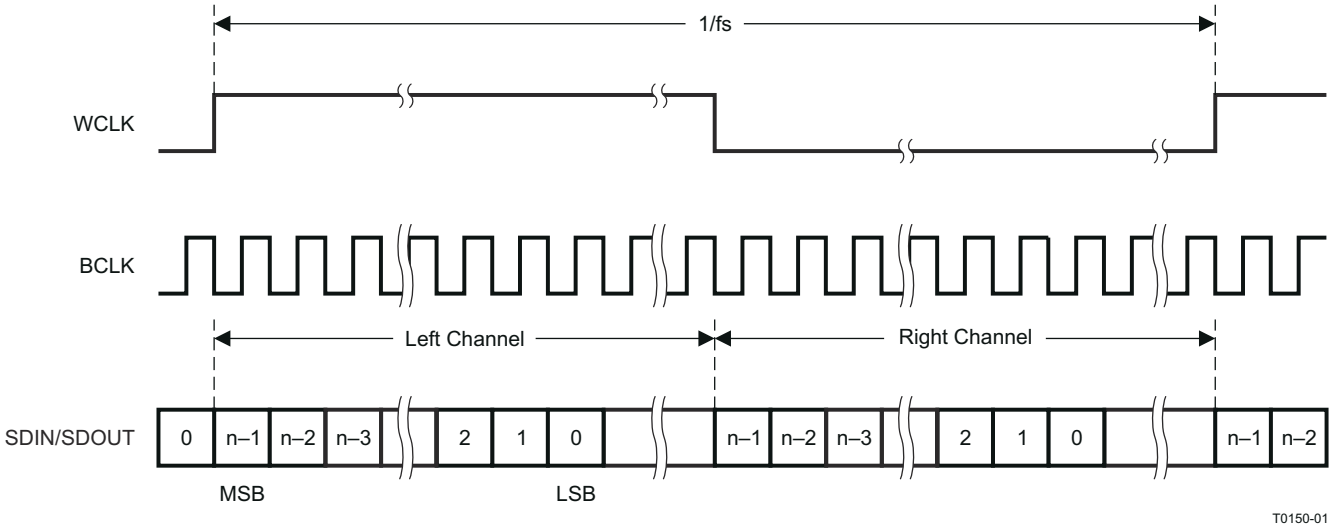

図 7-17. Left-Justified Serial Data Bus Mode Operation

7.5.7 I²S Mode

In I²S mode, the MSB of the left channel is valid on the second rising edge of the bit clock after the falling edge of the word clock. Similarly, the MSB of the right channel is valid on the second rising edge of the bit clock after the rising edge of the word clock. 図 7-18 shows a timing diagram of this operation.

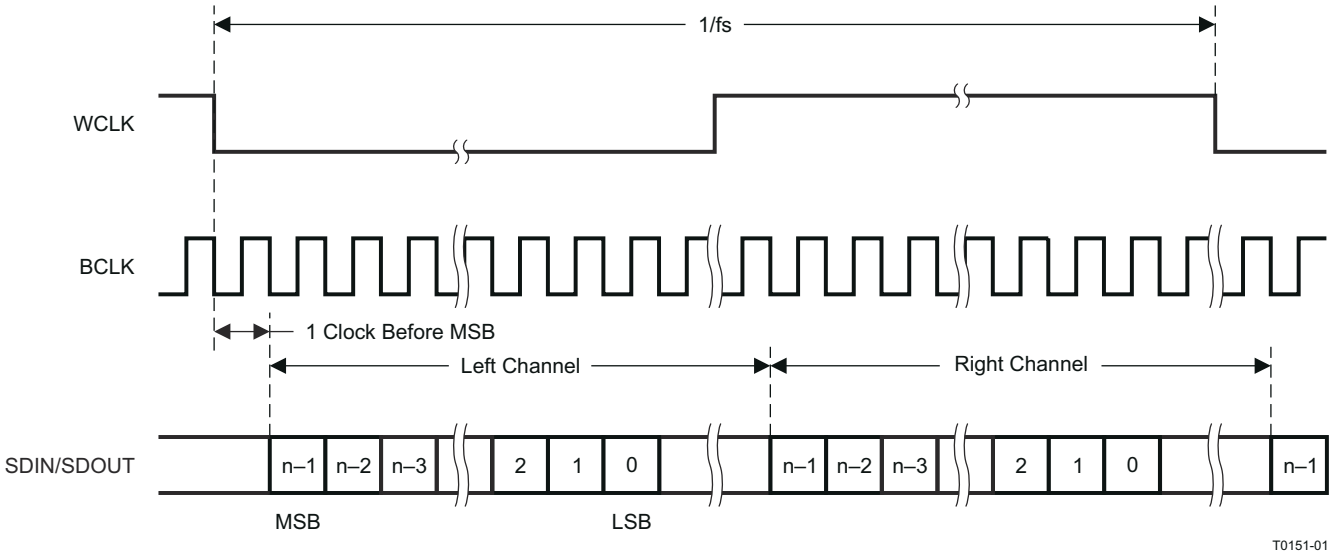

図 7-18. I²S Serial Data Bus Mode Operation

7.5.8 DSP Mode

In DSP mode, the rising edge of the word clock starts the data transfer with the left-channel data first, immediately followed by the right-channel data. Each data bit is valid on the falling edge of the bit clock.

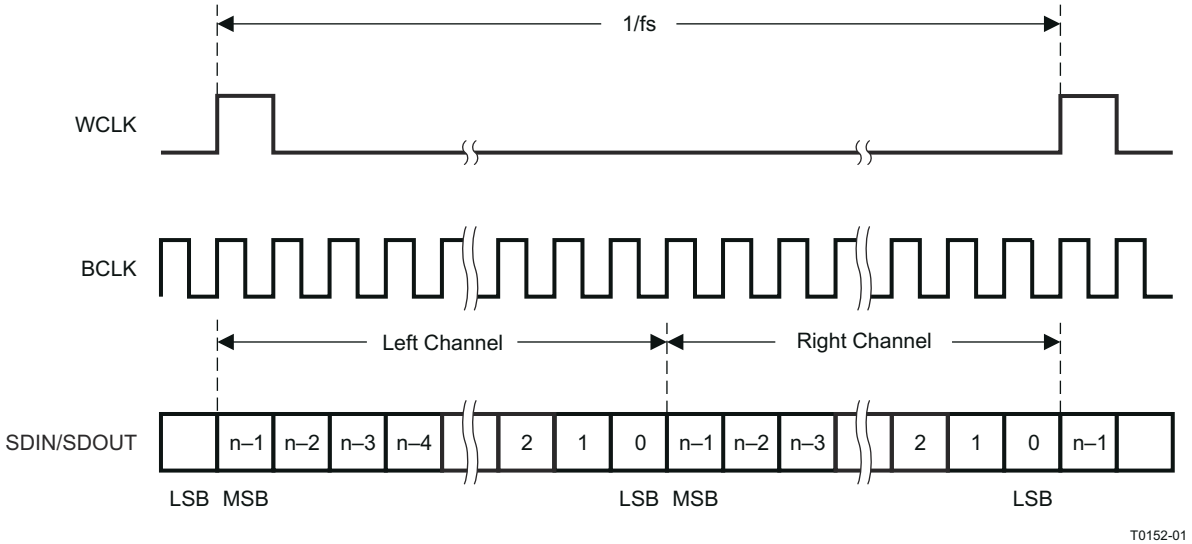

図 7-19. DSP Serial Data Bus Mode Operation

7.5.9 TDM Data Transfer

Time-division multiplexed data transfer can be realized in any of the left- transfer modes if the 256-clock bit-clock mode is selected, although it is recommended to be used in either left-justified mode or DSP mode. By changing the programmable offset, the bit clock in each frame where the data begins can be changed, and the serial data

output driver (DOUT) can also be programmed to the high-impedance state during all bit clocks except when valid data is being put onto the bus. This allows other codecs to be programmed with different offsets and to drive their data onto the same DOUT line, just in a different slot. For incoming data, the codec simply ignores data on the bus except where it is expected, based on the programmed offset.

Note that the location of the data when an offset is programmed is different, depending on what transfer mode is selected. In DSP mode, both left and right channels of data are transferred immediately adjacent to each other in the frame. This differs from left-justified mode, where the left- and right-channel data are always a half-frame apart in each frame. In this case, as the offset is programmed from zero to some higher value, both the left- and right-channel data move across the frame, but still stay a full half-frame apart from each other. This is depicted in 図 7-20 for the two cases.

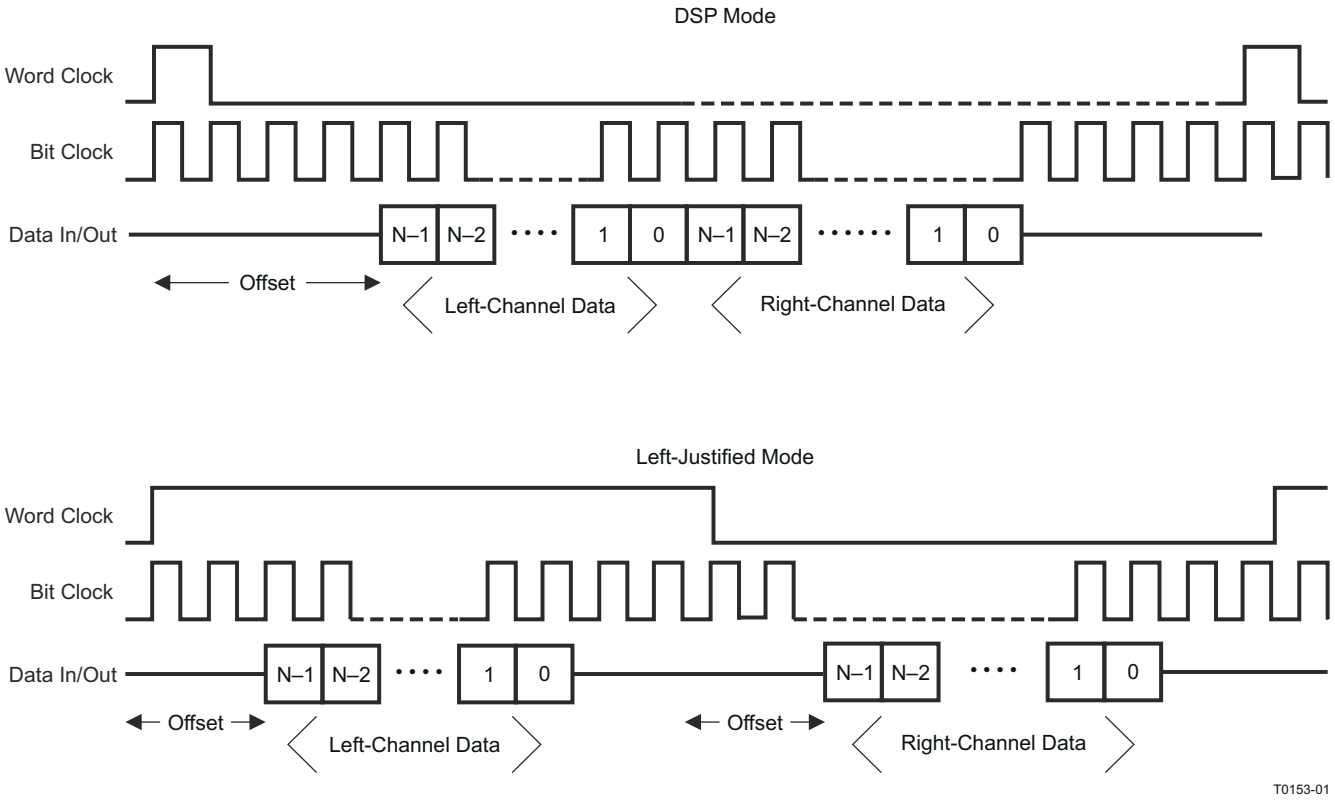

図 7-20. DSP Mode and Left-Justified Mode, Showing the Effect of a Programmed Data-Word Offset

7.5.10 Audio Clock Generation

The audio converters in the TLV320AIC3104-Q1 need an internal audio master clock at a frequency of 256 fS(ref), which can be obtained in a variety of manners from an external clock signal applied to the device.

A more detailed diagram of the audio clock section of the TLV320AIC3104-Q1 is shown in 図 7-21.

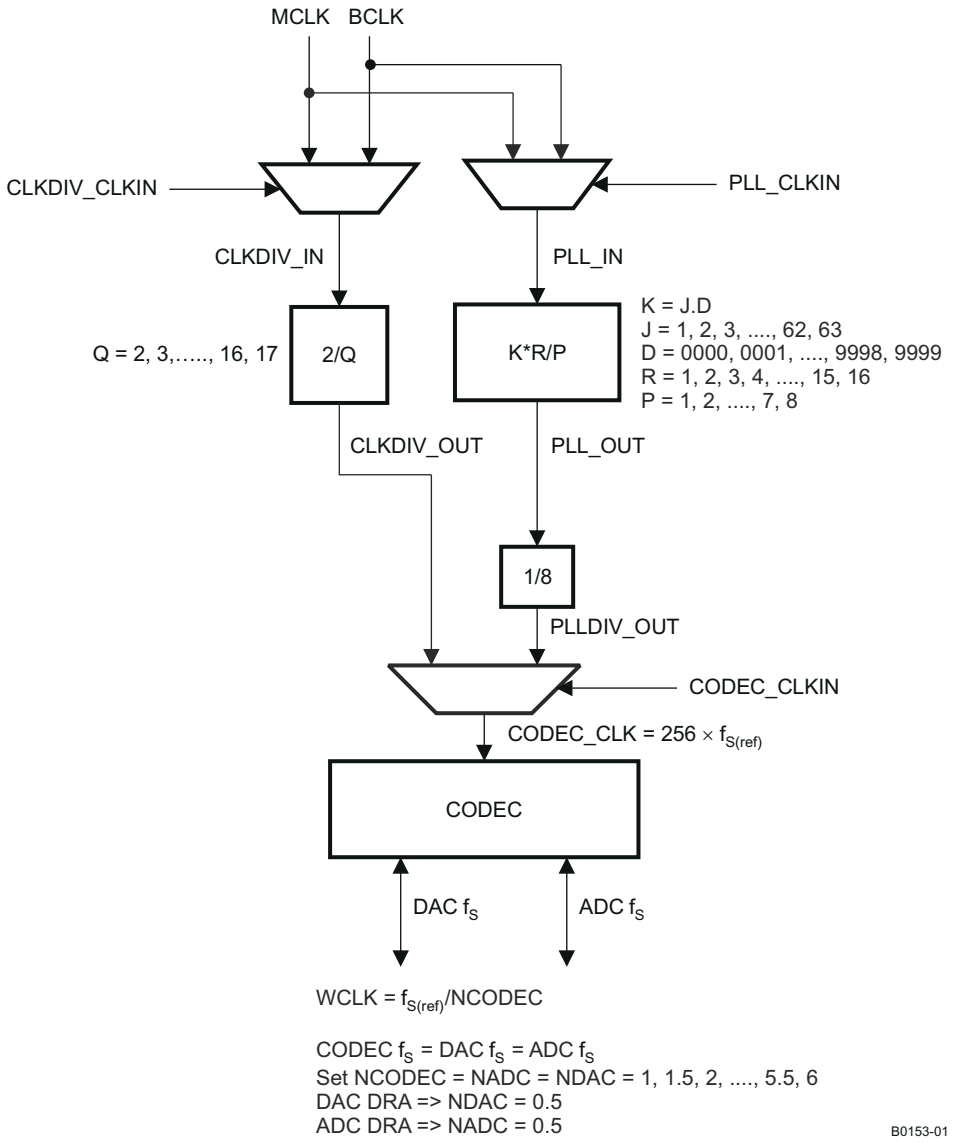

図 7-21. Audio Clock Generation Processing

The device can accept an MCLK input from 512 kHz to 50 MHz that can then be passed through either a programmable divider or a PLL to get the proper internal audio master clock required by the device. The BCLK input can also be used to generate the internal audio master clock.

A primary concern is proper operation of the codec at various sample rates with the limited MCLK frequencies available in the system. This device includes a highly programmable PLL to accommodate such situations easily. The integrated PLL can generate audio clocks from a wide variety of possible MCLK inputs, with particular focus paid to the standard MCLK rates already widely used.

When the PLL is disabled,

$$f_{S(ref)} = CLKDIV\_IN / (128 \times Q) \quad (4)$$

where

- Q = {2 to 17}. Q is register programmable and can be set in page 0, register 3, bits D6 to D3
- CLKDIV_IN can be MCLK or BCLK, selected by register 102, bits D7 to D6

注

When NCODEC = 1.5, 2.5, 3.5, 4.5, or 5.5, odd values of Q are not allowed. In this mode, MCLK can be as high as 50 MHz, and fS(ref) should fall within 39 kHz to 53 kHz, inclusive.

When the PLL is enabled,

$$f_{S(ref)} = (PLLCLK\_IN \times K \times R) / (2048 \times P) \quad (5)$$

where

- P = {1 to 8}
- R = {1 to 16}
- K = J.D
- J = {1 to 63}
- D = {0000 to 9999}
- PLLCLK_IN can be MCLK or BCLK, selected by Page 0, register 102, bits D5 to D4

P, R, J, and D are register programmable. J is the integer portion of K (the numbers to the left of the decimal point), while D is the fractional portion of K (the numbers to the right of the decimal point, assuming four digits of precision). P can be set in page 0, register 3, bits D2 to D0. R can be set in page 0, register 11, bits D3 to D0. J can be set in page 0, register 4, bits D7 to D2. The most-significant bits of D can be set in page 0, register 5, bits D7 to D0, and the least-significant bits of D can be set in page 0, register 6, bits D7 to D2.

Examples:

If K = 8.5, then J = 8, D = 5000
If K = 7.12, then J = 7, D = 1200
If K = 14.03, then J = 14, D = 0300
If K = 6.0004, then J = 6, D = 0004

When the PLL is enabled and D = 0000, the following conditions must be satisfied to meet specified performance:

2 MHz ≤ (PLLCLK_IN / P) ≤ 20 MHz
80 MHz ≤ (PLLCLK _IN × K × R / P) ≤ 110 MHz
4 ≤ J ≤ 55

When the PLL is enabled and D ≠ 0000, the following conditions must be satisfied to meet specified performance:

10 MHz ≤ PLLCLK _IN / P ≤ 20 MHz
80 MHz ≤ PLLCLK _IN × K × R / P ≤ 110 MHz
4 ≤ J ≤ 11
R = 1

Example:

MCLK = 12 MHz and $f_{S(ref)}$ = 44.1 kHz
Select P = 1, R = 1, K = 7.5264, which results in J = 7, D = 5264

Example:

MCLK = 12 MHz and $f_{S(ref)}$ = 48 kHz
Select P = 1, R = 1, K = 8.192, which results in J = 8, D = 1920

表 7-5 lists several example cases of typical MCLK rates and how to program the PLL to achieve $f_{S(ref)}$ = 44.1 kHz or 48 kHz.

表 7-5. Typical MCLK Rates

MCLK (MHz)	P	R	J	D	ACHIEVED f_S(ref)	% ERROR
$f_{S(ref)}$ = 44.1 kHz						
2.8224	1	1	32	0	44,100	0
5.6448	1	1	16	0	44,100	0
12	1	1	7	5264	44,100	0
13	1	1	6	9474	44,099.71	–0.0007
16	1	1	5	6448	44,100	0
19.2	1	1	4	7040	44,100	0
19.68	1	1	4	5893	44,100.3	0.0007
48	4	1	7	5264	44,100	0
$f_{S(ref)}$ = 48 kHz						
2.048	1	1	48	0	48,000	0
3.072	1	1	32	0	48,000	0
4.096	1	1	24	0	48,000	0
6.144	1	1	16	0	48,000	0
8.192	1	1	12	0	48,000	0
12	1	1	8	1920	48,000	0
13	1	1	7	5618	47,999.71	–0.0006
16	1	1	6	1440	48,000	0
19.2	1	1	5	1200	48,000	0
19.68	1	1	4	9951	47,999.79	–0.0004
48	4	1	8	1920	48,000	0

8 Register Maps

The control registers for the TLV320AIC3104 are described in detail as follows. All registers are 8 bits in width, with D7 referring to the most-significant bit of each register, and D0 referring to the least-significant bit.

表 8-1. Page 0, Register 0: Page Select Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D1	R	0000 000	Reserved. Write only zeros to these bits.
D0	R/W	0	Page Select Bit Writing zero to this bit sets page 0 as the active page for following register accesses. Writing a one to this bit sets page 1 as the active page for following register accesses. It is recommended that the user read this register bit back after each write, to ensure that the proper page is being accessed for future register read or writes.

表 8-2. Page 0, Register 1: Software Reset Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	W	0	Software Reset Bit 0 : Don't care 1 : Self-clearing software reset
D6–D0	W	000 0000	Reserved. Do not write to these bits.

表 8-3. Page 0, Register 2: Codec Sample Rate Select Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	0000	ADC Sample Rate Select (1) 0000: ADC $f_S = f_{S(ref)} / 1$ 0001: ADC $f_S = f_{S(ref)} / 1.5$ 0010: ADC $f_S = f_{S(ref)} / 2$ 0011: ADC $f_S = f_{S(ref)} / 2.5$ 0100: ADC $f_S = f_{S(ref)} / 3$ 0101: ADC $f_S = f_{S(ref)} / 3.5$ 0110: ADC $f_S = f_{S(ref)} / 4$ 0111: ADC $f_S = f_{S(ref)} / 4.5$ 1000: ADC $f_S = f_{S(ref)} / 5$ 1001: ADC $f_S = f_{S(ref)} / 5.5$ 1010: ADC $f_S = f_{S(ref)} / 6$ 1011–1111: Reserved. Do not write these sequences.
D3–D0	R/W	0000	DAC Sample Rate Select (1) 0000: DAC $f_S = f_{S(ref)} / 1$ 0001: DAC $f_S = f_{S(ref)} / 1.5$ 0010: DAC $f_S = f_{S(ref)} / 2$ 0011: DAC $f_S = f_{S(ref)} / 2.5$ 0100: DAC $f_S = f_{S(ref)} / 3$ 0101: DAC $f_S = f_{S(ref)} / 3.5$ 0110: DAC $f_S = f_{S(ref)} / 4$ 0111: DAC $f_S = f_{S(ref)} / 4.5$ 1000: DAC $f_S = f_{S(ref)} / 5$ 1001: DAC $f_S = f_{S(ref)} / 5.5$ 1010: DAC $f_S = f_{S(ref)} / 6$ 1011–1111 : Reserved, do not write these sequences.

(1) In the TLV320AIC3104-Q1, the ADC f_S must be set equal to the DAC f_S. This is done by setting the value of bits D7–D4 equal to the value of bits D3–D0.

表 8-4. Page 0, Register 3: PLL Programming Register A

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PLL Control Bit 0: PLL is disabled. 1: PLL is enabled.

表 8-4. Page 0, Register 3: PLL Programming Register A (続き)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6–D3	R/W	0010	PLL Q Value 0000: Q = 16 0001: Q = 17 0010: Q = 2 0011: Q = 3 0100: Q = 4 … 1110: Q = 14 1111: Q = 15
D2–D0	R/W	000	PLL P Value 000: P = 8 001: P = 1 010: P = 2 011: P = 3 100: P = 4 101: P = 5 110: P = 6 111: P = 7

表 8-5. Page 0, Register 4: PLL Programming Register B

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D2	R/W	0000 01	PLL J Value 0000 00: Reserved, do not write this sequence 0000 01: J = 1 0000 10: J = 2 0000 11: J = 3 … 1111 10: J = 62 1111 11: J = 63
D1–D0	R/W	00	Reserved. Write only zeros to these bits.

表 8-6. Page 0, Register 5: PLL Programming Register C

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	PLL D Value. Eight most-significant bits of a 14-bit unsigned integer valid values for D are from zero to 9999, represented by a 14-bit integer located in page 0, registers 5–6. Values should not be written into these registers that would result in a D value outside the valid range. (1)

(1) Whenever the D value is changed, register 5 should be written, immediately followed by register 6. Even if only the MSB or LSB of the value changes, both registers should be written.

表 8-7. Page 0, Register 6: PLL Programming Register D

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D2	R/W	0000 00	PLL D Value. Six least-significant bits of a 14-bit unsigned integer valid values for D are from zero to 9999, represented by a 14-bit integer located in page 0, registers 5–6. Values should not be written into these registers that would result in a D value outside the valid range. (1)
D1–D0	R	00	Reserved. Write only zeros to these bits.

(1) Whenever the D value is changed, register 5 should be written, immediately followed by register 6. Even if only the MSB or LSB of the value changes, both registers should be written.

表 8-8. Page 0, Register 7: Codec Data-Path Setup Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	$f_{S(ref)}$ Setting This register setting controls timers related to the AGC time constants. 0: $f_{S(ref)}$ = 48 kHz 1: $f_{S(ref)}$ = 44.1 kHz

表 8-8. Page 0, Register 7: Codec Data-Path Setup Register (続き)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6	R/W	0	ADC Dual-Rate Control 0: ADC dual-rate mode is disabled. 1: ADC dual-rate mode is enabled. Note: ADC dual-rate mode must match DAC dual-rate mode.
D5	R/W	0	DAC Dual-Rate Control 0: DAC dual-rate mode is disabled. 1: DAC dual-rate mode is enabled.
D4–D3	R/W	00	Left-DAC Data Path Control 00: Left-DAC data path is off (muted). 01: Left-DAC data path plays left-channel input data. 10: Left-DAC data path plays right-channel input data. 11: Left-DAC data path plays mono mix of left- and right-channel input data.
D2–D1	R/W	00	Right-DAC Data-Path Control 00: Right-DAC data path is off (muted). 01: Right-DAC data path plays right-channel input data. 10: Right-DAC data path plays left-channel input data. 11: Right-DAC data path plays mono mix of left- and right-channel input data.
D0	R/W	0	Reserved. Write only zero to this bit.

表 8-9. Page 0, Register 8: Audio Serial Data Interface Control Register A

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Bit Clock Directional Control 0: BCLK is an input (slave mode). 1: BCLK is an output (master mode).
D6	R/W	0	Word Clock Directional Control 0: WCLK is an input (slave mode). 1: WCLK is an output (master mode).
D5	R/W	0	Serial Output Data Driver (DOUT) 3-State Control 0: Do not place DOUT in high-impedance state when valid data is not being sent. 1: Place DOUT in high-impedance state when valid data is not being sent.
D4	R/W	0	Bit, Word Clock Drive Control 0: BCLK/WCLK does not continue to be transmitted when running in master mode if codec is powered down. 1: BCLK/WCLK continues to be transmitted when running in master mode, even if codec is powered down.
D3	R/W	0	Reserved. Do not write to this register bit.
D2	R/W	0	3-D Effect Control 0: Disable 3-D digital effect processing 1: Enable 3-D digital effect processing
D1–D0	R/W	00	Reserved. Write only zeros to these bits.

表 8-10. Page 0, Register 9: Audio Serial Data Interface Control Register B

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	Audio Serial Data Interface Transfer Mode 00: Serial data bus uses I^2S mode. 01: Serial data bus uses DSP mode. 10: Serial data bus uses right-justified mode. 11: Serial data bus uses left-justified mode.
D5–D4	R/W	00	Audio Serial Data Word Length Control 00: Audio data word length = 16 bits 01: Audio data word length = 20 bits 10: Audio data word length = 24 bits 11: Audio data word length = 32 bits

表 8-10. Page 0, Register 9: Audio Serial Data Interface Control Register B (続き)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D3	R/W	0	Bit Clock Rate Control This register only has effect when bit clock is programmed as an output. 0: Continuous-transfer mode used to determine master mode bit clock rate 1: 256-clock transfer mode used, resulting in 256 bit clocks per frame
D2	R/W	0	DAC Re-Sync 0: Don't care 1: Re-sync stereo DAC with codec interface if the group delay changes by more than ±DAC (f_S / 4).
D1	R/W	0	ADC Re-Sync 0: Don't care 1: Re-sync stereo ADC with codec interface if the group delay changes by more than ±ADC (f_S / 4).
D0	R/W	0	Re-Sync Mute Behavior 0: Re-sync is done without soft-muting the channel (ADC / DAC). 1: Re-sync is done by internally soft-muting the channel (ADC / DAC).

表 8-11. Page 0, Register 10: Audio Serial Data Interface Control Register C

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	Audio Serial Data Word Offset Control This register determines where valid data is placed or expected in each frame, by controlling the offset from beginning of the frame where valid data begins. The offset is measured from the rising edge of word clock when in DSP mode. 0000 0000: Data offset = 0 bit clocks 0000 0001: Data offset = 1 bit clock 0000 0010: Data offset = 2 bit clocks … Note: In continuous transfer mode the maximum offset is 17 for I^2S, LJF, RJF modes and 16 for DSP mode. In 256-clock mode, the maximum offset is 242 for I^2S, LJF, RJF and 241 for DSP modes. 1111 1110: Data offset = 254 bit clocks 1111 1111: Data offset = 255 bit clocks

表 8-12. Page 0, Register 11: Audio Codec Overflow Flag Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Left-ADC Overflow Flag This is a sticky bit, which stays set if an overflow occurs, even if the overflow condition is removed. The register bit is reset to 0 after it is read. 0: No overflow has occurred. 1: An overflow has occurred.
D6	R	0	Right-ADC Overflow Flag This is a sticky bit, which stays set if an overflow occurs, even if the overflow condition is removed. The register bit is reset to 0 after it is read. 0: No overflow has occurred. 1: An overflow has occurred.
D5	R	0	Left-DAC Overflow Flag This is a sticky bit, which stays set if an overflow occurs, even if the overflow condition is removed. The register bit is reset to 0 after it is read. 0: No overflow has occurred. 1: An overflow has occurred.
D4	R	0	Right-DAC Overflow Flag This is a sticky bit, which stays set if an overflow occurs, even if the overflow condition is removed. The register bit is reset to 0 after it is read. 0: No overflow has occurred. 1: An overflow has occurred.

表 8-12. Page 0, Register 11: Audio Codec Overflow Flag Register (続き)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D3–D0	R/W	0001	PLL R Value 0000: R = 16 0001: R = 1 0010: R = 2 0011: R = 3 0100: R = 4 … 1110: R = 14 1111: R = 15

表 8-13. Page 0, Register 12: Audio Codec Digital Filter Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	Left-ADC High-Pass Filter Control 00: Left-ADC high-pass filter disabled 01: Left-ADC high-pass filter –3-dB frequency = 0.0045 × ADC f_S 10: Left-ADC high-pass filter –3-dB frequency = 0.0125 × ADC f_S 11: Left-ADC high-pass filter –3-dB frequency = 0.025 × ADC f_S
D5–D4	R/W	00	Right-ADC High-Pass Filter Control 00: Right-ADC high-pass filter disabled 01: Right-ADC high-pass filter –3-dB frequency = 0.0045 × ADC f_S 10: Right-ADC high-pass filter –3-dB frequency = 0.0125 × ADC f_S 11: Right-ADC high-pass filter –3-dB frequency = 0.025 × ADC f_S
D3	R/W	0	Left-DAC Digital Effects Filter Control 0: Left-DAC digital effects filter disabled (bypassed) 1: Left-DAC digital effects filter enabled
D2	R/W	0	Left-DAC De-Emphasis Filter Control 0: Left-DAC de-emphasis filter disabled (bypassed) 1: Left-DAC de-emphasis filter enabled
D1	R/W	0	Right-DAC Digital Effects Filter Control 0: Right-DAC digital effects filter disabled (bypassed) 1: Right-DAC digital effects filter enabled
D0	R/W	0	Right-DAC De-Emphasis Filter Control 0: Right-DAC de-emphasis filter disabled (bypassed) 1: Right-DAC de-emphasis filter enabled

表 8-14. Page 0, Register 13: Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Reserved. Write only zeros to this register.

表 8-15. Page 0, Register 14: Headset, Button Press Detection Register B

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Driver Capacitive Coupling 0: Programs high-power outputs for capacitor free driver configuration 1: Programs high-power outputs for ac-coupled driver configuration
D6 (1)	R/W	0	Stereo Output Driver Configuration A Note: Do not set bits D6 and D3 both high at the same time. 0: A stereo fully differential output configuration is not being used 1: A stereo fully differential output configuration is being used
D5	R	0	Reserved. Write only zero to this bit.
D4	R	0	Headset Detection Flag 0: A headset has not been detected. 1: A headset has been detected.

表 8-15. Page 0, Register 14: Headset, Button Press Detection Register B (続き)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D3 (1)	R/W	0	Stereo Output Driver Configuration B Note: Do not set bits D6 and D3 both high at the same time. 0: A stereo pseudodifferential output configuration is not being used. 1: A stereo pseudodifferential output configuration is being used.
D2–D0	R	000	Reserved. Write only zeros to these bits.

(1) Do not set D6 and D3 to 1 simultaneously.

表 8-16. Page 0, Register 15: Left-ADC PGA Gain Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	1	Left-ADC PGA Mute 0: The left-ADC PGA is not muted 1: The left-ADC PGA is muted
D6–D0	R/W	000 0000	Left-ADC PGA Gain Setting 000 0000: Gain = 0 dB 000 0001: Gain = 0.5 dB 000 0010: Gain = 1 dB … 111 0110: Gain = 59 dB 111 0111: Gain = 59.5 dB 111 1000: Gain = 59.5 dB … 111 1111: Gain = 59.5 dB

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表 8-17. Page 0, Register 16: Right-ADC PGA Gain Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	1	Right-ADC PGA Mute 0: The right ADC PGA is not muted. 1: The right ADC PGA is muted.
D6–D0	R/W	000 0000	Right-ADC PGA Gain Setting 000 0000: Gain = 0 dB 000 0001: Gain = 0.5 dB 000 0010: Gain = 1 dB … 111 0110: Gain = 59 dB 111 0111: Gain = 59.5 dB 111 1000: Gain = 59.5 dB … 111 1111: Gain = 59.5 dB

表 8-18. Page 0, Register 17: MIC2L/R to Left-ADC Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	1111	MIC2L Input Level Control for Left-ADC PGA Mix Setting the input level control to one of the following gains automatically connects MIC2L to the left-ADC PGA mix. 0000: Input level control gain = 0 dB 0001: Input level control gain = –1.5 dB 0010: Input level control gain = –3 dB 0011: Input level control gain = –4.5 dB 0100: Input level control gain = –6 dB 0101: Input level control gain = –7.5 dB 0110: Input level control gain = –9 dB 0111: Input level control gain = –10.5 dB 1000: Input level control gain = –12 dB 1001–1110: Reserved. Do not write these sequences to these register bits. 1111: MIC2L is not connected to the left-ADC PGA.
D3–D0	R/W	1111	MIC2R/LINE2R Input Level Control for Left-ADC PGA Mix Setting the input level control to one of the following gains automatically connects MIC2R to the left-ADC PGA mix. 0000: Input level control gain = 0 dB 0001: Input level control gain = –1.5 dB 0010: Input level control gain = –3 dB 0011: Input level control gain = –4.5 dB 0100: Input level control gain = –6 dB 0101: Input level control gain = –7.5 dB 0110: Input level control gain = –9 dB 0111: Input level control gain = –10.5 dB 1000: Input level control gain = –12 dB 1001–1110: Reserved. Do not write these sequences to these register bits. 1111: MIC2R/LINE2R is not connected to the left-ADC PGA.

表 8-19. Page 0, Register 18: MIC2/LINE2 to Right-ADC Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	1111	MIC2L/LINE2L Input Level Control for Right -DC PGA Mix Setting the input level control to one of the following gains automatically connects MIC2L to the right-ADC PGA mix. 0000: Input level control gain = 0 dB 0001: Input level control gain = –1.5 dB 0010: Input level control gain = –3 dB 0011: Input level control gain = –4.5 dB 0100: Input level control gain = –6 dB 0101: Input level control gain = –7.5 dB 0110: Input level control gain = –9 dB 0111: Input level control gain = –10.5 dB 1000: Input level control gain = –12 dB 1001–1110: Reserved. Do not write these sequences to these register bits. 1111: MIC2L/LINE2L is not connected to the right-ADC PGA.
D3–D0	R/W	1111	MIC2R/LINE2R Input Level Control for Right-ADC PGA Mix Setting the input level control to one of the following gains automatically connects MIC2R to the right-ADC PGA mix. 0000: Input level control gain = 0 dB 0001: Input level control gain = –1.5 dB 0010: Input level control gain = –3 dB 0011: Input level control gain = –4.5 dB 0100: Input level control gain = –6 dB 0101: Input level control gain = –7.5 dB 0110: Input level control gain = –9 dB 0111: Input level control gain = –10.5 dB 1000: Input level control gain = –12 dB 1001–1110: Reserved. Do not write these sequences to these register bits. 1111: MIC2R/LINE2R is not connected to right-ADC PGA.

表 8-20. Page 0, Register 19: MIC1LP/LINE1LP to Left-ADC Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	MIC1LP/LINE1LP Single-Ended vs Fully Differential Control. If MIC1LP/LINE1LP is selected to both left- and right-ADC channels, both connections must use the same configuration (single-ended or fully differential mode). 0: MIC1LP/LINE1LP is configured in single-ended mode. 1: MIC1LP/LINE1LP and MIC1LM/LINE1LM are configured in fully differential mode.
D6–D3	R/W	1111	MIC1LP/LINE1LP Input Level Control for Left-ADC PGA Mix Setting the input level control to one of the following gains automatically connects LINE1L to the left-ADC PGA mix. 0000: Input level control gain = 0 dB 0001: Input level control gain = –1.5 dB 0010: Input level control gain = –3 dB 0011: Input level control gain = –4.5 dB 0100: Input level control gain = –6 dB 0101: Input level control gain = –7.5 dB 0110: Input level control gain = –9 dB 0111: Input level control gain = –10.5 dB 1000: Input level control gain = –12 dB 1001–1110: Reserved. Do not write these sequences to these register bits. 1111: LINE1L is not connected to the left-ADC PGA.
D2	R/W	0	Left-ADC Channel Power Control 0: Left-ADC channel is powered down. 1: Left-ADC channel is powered up.
D1–D0	R/W	00	Left-ADC PGA Soft-Stepping Control 00: Left-ADC PGA soft-stepping at once per sample period 01: Left-ADC PGA soft-stepping at once per two sample periods 10–11: Left-ADC PGA soft-stepping is disabled.

表 8-21. Page 0, Register 20: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0111 1000	Reserved. Do not write to this register.

表 8-22. Page 0, Register 21: MIC1RP/LINE1RP to Left-ADC Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	MIC1RP/LINE1RP Single-Ended vs Fully Differential Control. If MIC1RP/LINE1RP is selected to both left- and right-ADC channels, both connections must use the same configuration (single-ended or fully differential mode). 0: MIC1RP/LINE1RP is configured in single-ended mode. 1: MIC1RP/LINE1RP and MIC1RM/LINE1RM are configured in fully differential mode.
D6–D3	R/W	1111	MIC1RP/LINE1RP Input Level Control for Left-ADC PGA Mix Setting the input level control to one of the following gains automatically connects LINE1R to the left-ADC PGA mix. 0000: Input level control gain = 0 dB 0001: Input level control gain = –1.5 dB 0010: Input level control gain = –3 dB 0011: Input level control gain = –4.5 dB 0100: Input level control gain = –6 dB 0101: Input level control gain = –7.5 dB 0110: Input level control gain = –9 dB 0111: Input level control gain = –10.5 dB 1000: Input level control gain = –12 dB 1001–1110: Reserved. Do not write these sequences to these register bits. 1111: LINE1R is not connected to the left-ADC PGA.
D2–D0	R	000	Reserved. Write only zeros to these bits.

表 8-23. Page 0, Register 22: MIC1RP/LINE1RP to Right-ADC Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	MIC1RP/LINE1RP Single-Ended vs Fully Differential Control. If MIC1RP/LINE1RP is selected to both left- and right-ADC channels, both connections must use the same configuration (single-ended or fully differential mode). 0: MIC1RP/LINE1RP is configured in single-ended mode. 1: MIC1RP/LINE1RP and MIC1RM/LINE1RM are configured in fully differential mode.
D6–D3	R/W	1111	MIC1RP/LINE1RP Input Level Control for Right-ADC PGA Mix Setting the input level control to one of the following gains automatically connects LINE1R to the right-ADC PGA mix. 0000: Input level control gain = 0 dB 0001: Input level control gain = –1.5 dB 0010: Input level control gain = –3 dB 0011: Input level control gain = –4.5 dB 0100: Input level control gain = –6 dB 0101: Input level control gain = –7.5 dB 0110: Input level control gain = –9 dB 0111: Input level control gain = –10.5 dB 1000: Input level control gain = –12 dB 1001–1110: Reserved. Do not write these sequences to these register bits. 1111: LINE1R is not connected to the right-ADC PGA.
D2	R/W	0	Right-ADC Channel Power Control 0: Right-ADC channel is powered down. 1: Right-ADC channel is powered up.
D1–D0	R/W	00	Right-ADC PGA Soft-Stepping Control 00: Right-ADC PGA soft-stepping at once per sample period 01: Right-ADC PGA soft-stepping at once per two sample periods 10–11: Right-ADC PGA soft-stepping is disabled.

表 8-24. Page 0, Register 23: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0111 1000	Reserved. Do not write to this register.

表 8-25. Page 0, Register 24: MIC1LP/LINE1LP to Right-ADC Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	MIC1LP/LINE1LP Single-Ended vs Fully Differential Control. If MIC1LP/LINE1LP is selected to both left- and right-ADC channels, both connections must use the same configuration (single-ended or fully differential mode). 0: MIC1LP/LINE1LP is configured in single-ended mode. 1: MIC1LP/LINE1LP and MIC1LM/LINE1LM are configured in fully differential mode.
D6–D3	R/W	1111	MIC1LP/LINE1LP Input Level Control for Right-ADC PGA Mix Setting the input level control to one of the following gains automatically connects LINE1L to the right-ADC PGA mix. 0000: Input level control gain = 0 dB 0001: Input level control gain = –1.5 dB 0010: Input level control gain = –3 dB 0011: Input level control gain = –4.5 dB 0100: Input level control gain = –6 dB 0101: Input level control gain = –7.5 dB 0110: Input level control gain = –9 dB 0111: Input level control gain = –10.5 dB 1000: Input level control gain = –12 dB 1001–1110: Reserved. Do not write these sequences to these register bits. 1111: LINE1L is not connected to the right-ADC PGA.
D2–D0	R	000	Reserved. Write only zeros to these bits.

表 8-26. Page 0, Register 25: MICBIAS Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	MICBIAS Level Control 00: MICBIAS output is powered down. 01: MICBIAS output is powered to 2 V. 10: MICBIAS output is powered to 2.5 V. 11: MICBIAS output is connected to AVDD.
D5–D3	R	000	Reserved. Write only zeros to these bits.
D2–D0	R	XXX	Reserved. Write only zeros to these bits.

表 8-27. Page 0, Register 26: Left-AGC Control Register A

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Left-AGC Enable 0: Left AGC is disabled. 1: Left AGC is enabled.
D6–D4	R/W	000	Left-AGC Target Level 000: Left-AGC target level = –5.5 dB 001: Left-AGC target level = –8 dB 010: Left-AGC target level = –10 dB 011: Left-AGC target level = –12 dB 100: Left-AGC target level = –14 dB 101: Left-AGC target level = –17 dB 110: Left-AGC target level = –20 dB 111: Left-AGC target level = –24 dB
D3–D2	R/W	00	Left-AGC Attack Time These time constants [1] are not accurate when double-rate audio mode is enabled. 00: Left-AGC attack time = 8 ms 01: Left-AGC attack time = 11 ms 10: Left-AGC attack time = 16 ms 11: Left-AGC attack time = 20 ms
D1–D0	R/W	00	Left-AGC Decay Time These time constants [1] are not accurate when double-rate audio mode is enabled. 00: Left-AGC decay time = 100 ms 01: Left-AGC decay time = 200 ms 10: Left-AGC decay time = 400 ms 11: Left-AGC decay time = 500 ms

1. Time constants are valid when DRA is not enabled. The values change if DRA is enabled.

表 8-28. Page 0, Register 27: Left-AGC Control Register B

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D1	R/W	1111 111	Left-AGC Maximum Gain Allowed 0000 000: Maximum gain = 0 dB 0000 001: Maximum gain = 0.5 dB 0000 010: Maximum gain = 1 dB … 1110 110: Maximum gain = 59 dB 1110 111–111 111: Maximum gain = 59.5 dB
D0	R/W	0	Reserved. Write only zero to this bit.

表 8-29. Page 0, Register 28: Left-AGC Control Register C

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	Noise Gate Hysteresis Level Control 00: Hysteresis = 1 dB 01: Hysteresis = 2 dB 10: Hysteresis = 3 dB 11: Hysteresis is disabled.

表 8-29. Page 0, Register 28: Left-AGC Control Register C (続き)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5–D1	R/W	00 000	Left-AGC Noise Threshold Control 00000: Left-AGC noise, silence detection disabled 00001: Left-AGC noise threshold = –30 dB 00010: Left-AGC noise threshold = –32 dB 00011: Left-AGC noise threshold = –34 dB … 11101: Left-AGC noise threshold = –86 dB 11110: Left-AGC noise threshold = –88 dB 11111: Left-AGC noise threshold = –90 dB
D0	R/W	0	Left-AGC Clip Stepping Control 0: Left-AGC clip stepping disabled 1: Left-AGC clip stepping enabled

表 8-30. Page 0, Register 29: Right-AGC Control Register A

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Right-AGC Enable 0: Right AGC is disabled. 1: Right AGC is enabled.
D6–D4	R/W	000	Right-AGC Target Level 000: Right-AGC target level = –5.5 dB 001: Right-AGC target level = –8 dB 010: Right-AGC target level = –10 dB 011: Right-AGC target level = –12 dB 100: Right-AGC target level = –14 dB 101: Right-AGC target level = –17 dB 110: Right-AGC target level = –20 dB 111: Right-AGC target level = –24 dB
D3–D2	R/W	00	Right-AGC Attack Time These time constants are not accurate when double-rate audio mode is enabled. 00: Right-AGC attack time = 8 ms 01: Right-AGC attack time = 11 ms 10: Right-AGC attack time = 16 ms 11: Right-AGC attack time = 20 ms
D1–D0	R/W	00	Right-AGC Decay Time These time constants are not accurate when double-rate audio mode is enabled. 00: Right-AGC decay time = 100 ms 01: Right-AGC decay time = 200 ms 10: Right-AGC decay time = 400 ms 11: Right-AGC decay time = 500 ms

表 8-31. Page 0, Register 30: Right-AGC Control Register B

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D1	R/W	1111 111	Right-AGC Maximum Gain Allowed 0000 000: Maximum gain = 0 dB 0000 001: Maximum gain = 0.5 dB 0000 010: Maximum gain = 1 dB … 1110 110: Maximum gain = 59 dB 1110 111–1111 111: Maximum gain = 59.5 dB
D0	R/W	0	Reserved. Write only zero to this bit.

表 8-32. Page 0, Register 31: Right-AGC Control Register C

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	Noise Gate Hysteresis Level Control 00: Hysteresis = 1 dB 01: Hysteresis = 2 dB 10: Hysteresis = 3 dB 11: Hysteresis is disabled.
D5–D1	R/W	00 000	Right-AGC Noise Threshold Control 00 000: Right-AGC noise, silence detection disabled 00 001: Right-AGC noise threshold = –30 dB 00 010: Right-AGC noise threshold = –32 dB 00 011: Right-AGC noise threshold = –34 dB … 11 101: Right-AGC noise threshold = –86 dB 11 110: Right-AGC noise threshold = –88 dB 11 111: Right-AGC noise threshold = –90 dB
D0	R/W	0	Right-AGC Clip Stepping Control 0: Right-AGC clip stepping disabled 1: Right-AGC clip stepping enabled

表 8-33. Page 0, Register 32: Left-AGC Gain Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Left-Channel Gain Applied by AGC Algorithm 1110 1000: Gain = –12 dB 1110 1001: Gain = –11.5 dB 1110 1010: Gain = –11 dB … 0000 0000: Gain = 0.0 dB 0000 0001: Gain = 0.5 dB … 0111 0110: Gain = 59 dB 0111 0111: Gain = 59.5 dB

表 8-34. Page 0, Register 33: Right-AGC Gain Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Right-Channel Gain Applied by AGC Algorithm 1110 1000: Gain = –12 dB 1110 1001: Gain = –11.5 dB 1110 1010: Gain = –11 dB … 0000 0000: Gain = 0 dB 0000 0001: Gain = +0.5-dB … 0111 0110: Gain = 59 dB 0111 0111: Gain = 59.5 dB

表 8-35. Page 0, Register 34: Left-AGC Noise Gate Debounce Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D3	R/W	0000 0	Left-AGC Noise Detection Debounce Control These times (1) are not accurate when double-rate audio mode is enabled. 0000 0: Debounce = 0 ms 0000 1: Debounce = 0.5 ms 0001 0: Debounce = 1 ms 0001 1: Debounce = 2 ms 0010 0: Debounce = 4 ms 0010 1: Debounce = 8 ms 0011 0: Debounce = 16 ms 0011 1: Debounce = 32 ms 0100 0: Debounce = 64 × 1 = 64 ms 0100 1: Debounce = 64 × 2 = 128 ms 0101 0: Debounce = 64 × 3 = 192 ms … 1111 0: Debounce = 64 × 23 = 1,472 ms 1111 1: Debounce = 64 × 24 = 1,536 ms
D2–D0	R/W	000	Left-AGC Signal Detection Debounce Control These times (1) are not accurate when double-rate audio mode is enabled. 000: Debounce = 0 ms 001: Debounce = 0.5 ms 010: Debounce = 1 ms 011: Debounce = 2 ms 100: Debounce = 4 ms 101: Debounce = 8 ms 110: Debounce = 16 ms 111: Debounce = 32 ms

(1) Time constants are valid when DRA is not enabled. The values change when DRA is enabled.

表 8-36. Page 0, Register 35: Right-AGC Noise Gate Debounce Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D3	R/W	0000 0	Right-AGC Noise Detection Debounce Control These times (1) are not accurate when double-rate audio mode is enabled. 00000: Debounce = 0 ms 00001: Debounce = 0.5 ms 00010: Debounce = 1 ms 00011: Debounce = 2 ms 00100: Debounce = 4 ms 00101: Debounce = 8 ms 00110: Debounce = 16 ms 00111: Debounce = 32 ms 01000: Debounce = 64 × 1 = 64 ms 01001: Debounce = 64 × 2 = 128 ms 01010: Debounce = 64 × 3 = 192 ms … 11110: Debounce = 64 × 23 = 1,472 ms 11111: Debounce = 64 × 24 = 1,536 ms
D2–D0	R/W	000	Right-AGC Signal Detection Debounce Control These times (1) are not accurate when double-rate audio mode is enabled. 000: Debounce = 0 ms 001: Debounce = 0.5 ms 010: Debounce = 1 ms 011: Debounce = 2 ms 100: Debounce = 4 ms 101: Debounce = 8 ms 110: Debounce = 16 ms 111: Debounce = 32 ms

(1) Time constants are valid when DRA is not enabled. The values change when DRA is enabled.

表 8-37. Page 0, Register 36: ADC Flag Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Left-ADC PGA Status 0: Applied gain and programmed gain are not the same. 1: Applied gain = programmed gain
D6	R	0	Left-ADC Power Status 0: Left ADC is in a power-down state. 1: Left ADC is in a power-up state.
D5	R	0	Left-AGC Signal Detection Status 0: Signal power is greater than or equal to noise threshold. 1: Signal power is less than noise threshold.
D4	R	0	Left-AGC Saturation Flag 0: Left AGC is not saturated. 1: Left-AGC gain applied = maximum allowed gain for left AGC
D3	R	0	Right-ADC PGA Status 0: Applied gain and programmed gain are not the same. 1: Applied gain = programmed gain
D2	R	0	Right-ADC Power Status 0: Right ADC is in a power-down state. 1: Right ADC is in a power-up state.
D1	R	0	Right-AGC Signal Detection Status 0: Signal power is greater than or equal to noise threshold. 1: Signal power is less than noise threshold.
D0	R	0	Right-AGC Saturation Flag 0: Right AGC is not saturated. 1: Right-AGC gain applied = maximum allowed gain for right AGC

表 8-38. Page 0, Register 37: DAC Power and Output Driver Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Left-DAC Power Control 0: Left DAC is not powered up. 1: Left DAC is powered up.
D6	R/W	0	Right-DAC Power Control 0: Right DAC is not powered up. 1: Right DAC is powered up.
D5–D4	R/W	00	HPLCOM Output Driver Configuration Control 00: HPLCOM configured as differential of HPLOUT 01: HPLCOM configured as constant VCM output 10: HPLCOM configured as independent single-ended output 11: Reserved. Do not write this sequence to these register bits.
D3–D0	R	0000	Reserved. Write only zeros to these bits.

表 8-39. Page 0, Register 38: High-Power Output Driver Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R	00	Reserved. Write only zeros to these register bits.
D5–D3	R/W	000	HPRCOM Output Driver Configuration Control 000: HPRCOM configured as differential of HPROUT 001: HPRCOM configured as constant VCM output 010: HPRCOM configured as independent single-ended output 011: HPRCOM configured as differential of HPLCOM 100: HPRCOM configured as external feedback with HPLCOM as constant VCM output 101–111: Reserved. Do not write these sequences to these register bits.
D2	R/W	0	Short-Circuit Protection Control 0: Short-circuit protection on all high-power output drivers is disabled. 1: Short-circuit protection on all high-power output drivers is enabled.

表 8-39. Page 0, Register 38: High-Power Output Driver Control Register (続き)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D1	R/W	0	Short-Circuit Protection Mode Control 0: If short-circuit protection is enabled, it limits the maximum current to the load. 1: If short-circuit protection is enabled, it powers down the output driver automatically when a short is detected.
D0	R	0	Reserved. Write only zero to this bit.

表 8-40. Page 0, Register 39: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved. Do not write to this register.

表 8-41. Page 0, Register 40: High-Power Output Stage Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	Output Common-Mode Voltage Control 00: Output common-mode voltage = 1.35 V 01: Output common-mode voltage = 1.5 V 10: Output common-mode voltage = 1.65 V 11: Output common-mode voltage = 1.8 V
D5–D2	R/W	0000	Reserved. Write only zeros to these bits.
D1–D0	R/W	00	Output Volume Control Soft-Stepping 00: Output soft-stepping = one step per sample period 01: Output soft-stepping = one step per two sample periods 10: Output soft-stepping disabled 11: Reserved. Do not write this sequence to these bits.

表 8-42. Page 0, Register 41: DAC Output Switching Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	Left-DAC Output Switching Control 00: Left-DAC output selects DAC_L1 path. 01: Left-DAC output selects DAC_L3 path to left line output driver. 10: Left-DAC output selects DAC_L2 path to left high-power output drivers. 11: Reserved. Do not write this sequence to these register bits.
D5–D4	R/W	00	Right-DAC Output Switching Control 00: Right-DAC output selects DAC_R1 path. 01: Right-DAC output selects DAC_R3 path to right line output driver. 10: Right-DAC output selects DAC_R2 path to right high-power output drivers. 11: Reserved. Do not write this sequence to these register bits.
D3–D2	R/W	00	Reserved. Write only zeros to these bits.
D1–D0	R/W	00	DAC Digital Volume Control Functionality 00: Left- and right-DAC channels have independent volume controls. 01: Left-DAC volume follows the right-DAC digital volume control register. 10: Right-DAC volume follows the left-DAC digital volume control register. 11: Left- and right-DAC channels have independent volume controls (same as 00).

表 8-43. Page 0, Register 42: Output Driver Pop Reduction Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	0000	Output Driver Power-On Delay Control 0000: Driver power-on time = 0 µs 0001: Driver power-on time = 10 µs 0010: Driver power-on time = 100 µs 0011: Driver power-on time = 1 ms 0100: Driver power-on time = 10 ms 0101: Driver power-on time = 50 ms 0110: Driver power-on time = 100 ms 0111: Driver power-on time = 200 ms 1000: Driver power-on time = 400 ms 1001: Driver power-on time = 800 ms 1010: Driver power-on time = 2 s 1011: Driver power-on time = 4 s 1100–1111: Reserved. Do not write these sequences to these register bits.
D3–D2	R/W	00	Driver Ramp-Up Step Timing Control 00: Driver ramp-up step time = 0 ms 01: Driver ramp-up step time = 1 ms 10: Driver ramp-up step time = 2 ms 11: Driver ramp-up step time = 4 ms
D1	R/W	0	Weak Output Common-Mode Voltage Control 0: Weakly driven output common-mode voltage is generated from resistor divider off the AVDD supply. 1: Weakly driven output common-mode voltage is generated from band-gap reference.
D0	R/W	0	Reserved. Write only zero to this bit.

表 8-44. Page 0, Register 43: Left-DAC Digital Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	1	Left-DAC Digital Mute 0: The left-DAC channel is not muted. 1: The left-DAC channel is muted.
D6–D0	R/W	000 0000	Left-DAC Digital Volume Control Setting 000 0000: Gain = 0 dB 000 0001: Gain = –0.5 dB 000 0010: Gain = –1 dB … 111 1101: Gain = –62.5 dB 111 1110: Gain = –63 dB 111 1111: Gain = –63.5 dB

表 8-45. Page 0, Register 44: Right-DAC Digital Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	1	Right-DAC Digital Mute 0: The right-DAC channel is not muted. 1: The right-DAC channel is muted.
D6–D0	R/W	000 0000	Right-DAC Digital Volume Control Setting 000 0000: Gain = 0 dB 000 0001: Gain = –0.5 dB 000 0010: Gain = –1 dB … 111 1101: Gain = –62.5 dB 111 1110: Gain = –63 dB 111 1111: Gain = –63.5 dB

8.1 Output Stage Volume Controls

A basic analog volume control with range from 0 dB to –78 dB and mute is replicated multiple times in the output stage network, connected to each of the analog signals that route to the output stage. In addition, to enable

completely independent mixing operations to be performed for each output driver, each analog signal coming into the output stage may have up to seven separate volume controls. These volume controls all have approximately 0.5-dB step programmability over most of the gain range, with steps increasing slightly at the lowest attenuations. 表 8-46 lists the detailed gain versus programmed setting for this basic volume control.

表 8-46. Output Stage Volume Control Settings and Gains

Gain Setting	Analog Gain (dB)	Gain Setting	Analog Gain (dB)	Gain Setting	Analog Gain (dB)	Gain Setting	Analog Gain (dB)
0	0	30	–15	60	–30.1	90	–45.2
1	–0.5	31	–15.5	61	–30.6	91	–45.8
2	–1	32	–16	62	–31.1	92	–46.2
3	–1.5	33	–16.5	63	–31.6	93	–46.7
4	–2	34	–17	64	–32.1	94	–47.4
5	–2.5	35	–17.5	65	–32.6	95	–47.9
6	–3	36	–18	66	–33.1	96	–48.2
7	–3.5	37	–18.6	67	–33.6	97	–48.7
8	–4	38	–19.1	68	–34.1	98	–49.3
9	–4.5	39	–19.6	69	–34.6	99	–50
10	–5	40	–20.1	70	–35.1	100	–50.3
11	–5.5	41	–20.6	71	–35.7	101	–51
12	–6	42	–21.1	72	–36.1	102	–51.4
13	–6.5	43	–21.6	73	–36.7	103	–51.8
14	–7	44	–22.1	74	–37.1	104	–52.2
15	–7.5	45	–22.6	75	–37.7	105	–52.7
16	–8	46	–23.1	76	–38.2	106	–53.7
17	–8.5	47	–23.6	77	–38.7	107	–54.2
18	–9	48	–24.1	78	–39.2	108	–55.3
19	–9.5	49	–24.6	79	–39.7	109	–56.7
20	–10	50	–25.1	80	–40.2	110	–58.3
21	–10.5	51	–25.6	81	–40.7	111	–60.2
22	–11	52	–26.1	82	–41.2	112	–62.7
23	–11.5	53	–26.6	83	–41.7	113	–64.3
24	–12	54	–27.1	84	–42.2	114	–66.2
25	–12.5	55	–27.6	85	–42.7	115	–68.7
26	–13	56	–28.1	86	–43.2	116	–72.2
27	–13.5	57	–28.6	87	–43.8	117	–78.3
28	–14	58	–29.1	88	–44.3	118–127	Mute
29	–14.5	59	–29.6	89	–44.8		

表 8-47. Page 0, Register 45: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	Reserved. Do not write to this register.

表 8-48. Page 0, Register 46: PGA_L to HPLOUT Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_L Output Routing Control 0: PGA_L is not routed to HPLOUT 1: PGA_L is routed to HPLOUT

表 8-48. Page 0, Register 46: PGA_L to HPLOUT Volume Control Register (続き)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6–D0	R/W	000 0000	PGA_L to HPLOUT Analog Volume Control For 7-bit register settings versus analog gain values, see 表 8-46.

表 8-49. Page 0, Register 47: DAC_L1 to HPLOUT Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_L1 Output Routing Control 0: DAC_L1 is not routed to HPLOUT. 1: DAC_L1 is routed to HPLOUT.
D6–D0	R/W	000 0000	DAC_L1 to HPLOUT Analog Volume Control For 7-bit register settings versus analog gain values, see 表 8-46.

表 8-50. Page 0, Register 48: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	Reserved. Do not write to this register.

表 8-51. Page 0, Register 49: PGA_R to HPLOUT Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_R Output Routing Control 0: PGA_R is not routed to HPLOUT 1: PGA_R is routed to HPLOUT
D6–D0	R/W	000 0000	PGA_R to HPLOUT Analog Volume Control For 7-bit register settings versus analog gain values, see 表 8-46.

表 8-52. Page 0, Register 50: DAC_R1 to HPLOUT Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_R1 Output Routing Control 0: DAC_R1 is not routed to HPLOUT. 1: DAC_R1 is routed to HPLOUT.
D6–D0	R/W	000 0000	DAC_R1 to HPLOUT Analog Volume Control For 7-bit register settings versus analog gain values, see 表 8-46.

表 8-53. Page 0, Register 51: HPLOUT Output Level Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	0000	HPLOUT Output Level Control 0000: Output level control = 0 dB 0001: Output level control = 1 dB 0010: Output level control = 2 dB ... 1000: Output level control = 8 dB 1001: Output level control = 9 dB 1010–1111: Reserved. Do not write these sequences to these register bits.
D3	R/W	0	HPLOUT Mute 0: HPLOUT is muted. 1: HPLOUT is not muted.
D2	R/W	1	HPLOUT Power-Down Drive Control 0: HPLOUT is weakly driven to a common-mode when powered down. 1: HPLOUT is high-impedance when powered down.
D1	R	0	HPLOUT Volume Control Status 0: Not all programmed gains to HPLOUT have been applied yet. 1: All programmed gains to HPLOUT have been applied.

表 8-53. Page 0, Register 51: HPLOUT Output Level Control Register (続き)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D0	R/W	0	HPLOUT Power Control 0: HPLOUT is not fully powered up. 1: HPLOUT is fully powered up.

表 8-54. Page 0, Register 52: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	Reserved. Do not write to this register.

表 8-55. Page 0, Register 53: PGA_L to HPLCOM Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_L Output Routing Control 0: PGA_L is not routed to HPLCOM. 1: PGA_L is routed to HPLCOM.
D6–D0	R/W	000 0000	PGA_L to HPLCOM Analog Volume Control For 7-bit register settings versus analog gain values, see 表 8-46.

表 8-56. Page 0, Register 54: DAC_L1 to HPLCOM Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_L1 Output Routing Control 0: DAC_L1 is not routed to HPLCOM. 1: DAC_L1 is routed to HPLCOM.
D6–D0	R/W	000 0000	DAC_L1 to HPLCOM Analog Volume Control For 7-bit register settings versus analog gain values, see 表 8-46.

表 8-57. Page 0, Register 55: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	Reserved. Do not write to this register.

表 8-58. Page 0, Register 56: PGA_R to HPLCOM Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_R Output Routing Control 0: PGA_R is not routed to HPLCOM. 1: PGA_R is routed to HPLCOM.
D6–D0	R/W	000 0000	PGA_R to HPLCOM Analog Volume Control For 7-bit register settings versus analog gain values, see 表 8-46.

表 8-59. Page 0, Register 57: DAC_R1 to HPLCOM Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_R1 Output Routing Control 0: DAC_R1 is not routed to HPLCOM. 1: DAC_R1 is routed to HPLCOM.
D6–D0	R/W	000 0000	DAC_R1 to HPLCOM Analog Volume Control For 7-bit register settings versus analog gain values, see 表 8-46.

表 8-60. Page 0, Register 58: HPLCOM Output Level Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	0000	HPLCOM Output Level Control 0000: Output level control = 0 dB 0001: Output level control = 1 dB 0010: Output level control = 2 dB ... 1000: Output level control = 8 dB 1001: Output level control = 9 dB 1010–1111: Reserved. Do not write these sequences to these register bits.
D3	R/W	0	HPLCOM Mute 0: HPLCOM is muted. 1: HPLCOM is not muted.
D2	R/W	1	HPLCOM Power-Down Drive Control 0: HPLCOM is weakly driven to a common mode when powered down. 1: HPLCOM is high-impedance when powered down.
D1	R	1	HPLCOM Volume Control Status 0: Not all programmed gains to HPLCOM have been applied yet. 1: All programmed gains to HPLCOM have been applied.
D0	R/W	0	HPLCOM Power Control 0: HPLCOM is not fully powered up. 1: HPLCOM is fully powered up.

表 8-61. Page 0, Register 59: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	Reserved. Do not write to this register.

表 8-62. Page 0, Register 60: PGA_L to HPROUT Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_L Output Routing Control 0: PGA_L is not routed to HPROUT. 1: PGA_L is routed to HPROUT.
D6–D0	R/W	000 0000	PGA_L to HPROUT Analog Volume Control For 7-bit register settings versus analog gain values, see 表 8-46.

表 8-63. Page 0, Register 61: DAC_L1 to HPROUT Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_L1 Output Routing Control 0: DAC_L1 is not routed to HPROUT. 1: DAC_L1 is routed to HPROUT.
D6–D0	R/W	000 0000	DAC_L1 to HPROUT Analog Volume Control For 7-bit register settings versus analog gain values, see 表 8-46.

表 8-64. Page 0, Register 62: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	Reserved. Do not write to this register.

表 8-65. Page 0, Register 63: PGA_R to HPROUT Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_R Output Routing Control 0: PGA_R is not routed to HPROUT. 1: PGA_R is routed to HPROUT.

表 8-65. Page 0, Register 63: PGA_R to HPROUT Volume Control Register (続き)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6–D0	R/W	000 0000	PGA_R to HPROUT Analog Volume Control For 7-bit register settings versus analog gain values, see 表 8-46.

表 8-66. Page 0, Register 64: DAC_R1 to HPROUT Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_R1 Output Routing Control 0: DAC_R1 is not routed to HPROUT. 1: DAC_R1 is routed to HPROUT.
D6–D0	R/W	000 0000	DAC_R1 to HPROUT Analog Volume Control For 7-bit register settings versus analog gain values, see 表 8-46.

表 8-67. Page 0, Register 65: HPROUT Output Level Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	0000	HPROUT Output Level Control 0000: Output level control = 0 dB 0001: Output level control = 1 dB 0010: Output level control = 2 dB ... 1000: Output level control = 8 dB 1001: Output level control = 9 dB 1010–1111: Reserved. Do not write these sequences to these register bits.
D3	R/W	0	HPROUT Mute 0: HPROUT is muted. 1: HPROUT is not muted.
D2	R/W	1	HPROUT Power-Down Drive Control 0: HPROUT is weakly driven to a common mode when powered down. 1: HPROUT is high-impedance when powered down.
D1	R	1	HPROUT Volume Control Status 0: Not all programmed gains to HPROUT have been applied yet. 1: All programmed gains to HPROUT have been applied.
D0	R/W	0	HPROUT Power Control 0: HPROUT is not fully powered up. 1: HPROUT is fully powered up.

表 8-68. Page 0, Register 66: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	Reserved. Do not write to this register.

表 8-69. Page 0, Register 67: PGA_L to HPRCOM Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_L Output Routing Control 0: PGA_L is not routed to HPRCOM. 1: PGA_L is routed to HPRCOM.
D6–D0	R/W	000 0000	PGA_L to HPRCOM Analog Volume Control For 7-bit register settings versus analog gain values, see 表 8-46.

表 8-70. Page 0, Register 68: DAC_L1 to HPRCOM Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_L1 Output Routing Control 0: DAC_L1 is not routed to HPRCOM. 1: DAC_L1 is routed to HPRCOM.

表 8-70. Page 0, Register 68: DAC_L1 to HPRCOM Volume Control Register (続き)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6–D0	R/W	000 0000	DAC_L1 to HPRCOM Analog Volume Control For 7-bit register settings versus analog gain values, see 表 8-46.

表 8-71. Page 0, Register 69: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	Reserved. Do not write to this register.

表 8-72. Page 0, Register 70: PGA_R to HPRCOM Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_R Output Routing Control 0: PGA_R is not routed to HPRCOM. 1: PGA_R is routed to HPRCOM.
D6–D0	R/W	000 0000	PGA_R to HPRCOM Analog Volume Control For 7-bit register settings versus analog gain values, see 表 8-46.

表 8-73. Page 0, Register 71: DAC_R1 to HPRCOM Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_R1 Output Routing Control 0: DAC_R1 is not routed to HPRCOM. 1: DAC_R1 is routed to HPRCOM.
D6–D0	R/W	000 0000	DAC_R1 to HPRCOM Analog Volume Control For 7-bit register settings versus analog gain values, see 表 8-46.

表 8-74. Page 0, Register 72: HPRCOM Output Level Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	0000	HPRCOM Output Level Control 0000: Output level control = 0 dB 0001: Output level control = 1 dB 0010: Output level control = 2 dB ... 1000: Output level control = 8 dB 1001: Output level control = 9 dB 1010–1111: Reserved. Do not write these sequences to these register bits.
D3	R/W	0	HPRCOM Mute 0: HPRCOM is muted. 1: HPRCOM is not muted.
D2	R/W	1	HPRCOM Power-Down Drive Control 0: HPRCOM is weakly driven to a common mode when powered down. 1: HPRCOM is high-impedance when powered down.
D1	R	1	HPRCOM Volume Control Status 0: Not all programmed gains to HPRCOM have been applied yet. 1: All programmed gains to HPRCOM have been applied.
D0	R/W	0	HPRCOM Power Control 0: HPRCOM is not fully powered up. 1: HPRCOM is fully powered up.

表 8-75. Page 0, Registers 73–78: Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved. Do not write to these registers.

表 8-76. Page 0, Register 79: Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0010	Reserved. Do not write to this register.

表 8-77. Page 0, Register 80: Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved. Do not write to this register.

表 8-78. Page 0, Register 81: PGA_L to LEFT_LOP/M Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_L Output Routing Control 0: PGA_L is not routed to LEFT_LOP/M. 1: PGA_L is routed to LEFT_LOP/M.
D6–D0	R/W	000 0000	PGA_L to LEFT_LOP/M Analog Volume Control For 7-bit register settings versus analog gain values, see 表 8-46.

表 8-79. Page 0, Register 82: DAC_L1 to LEFT_LOP/M Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_L1 Output Routing Control 0: DAC_L1 is not routed to LEFT_LOP/M. 1: DAC_L1 is routed to LEFT_LOP/M.
D6–D0	R/W	000 0000	DAC_L1 to LEFT_LOP/M Analog Volume Control For 7-bit register settings versus analog gain values, see 表 8-46.

表 8-80. Page 0, Register 83: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	Reserved. Do not write to this register.

表 8-81. Page 0, Register 84: PGA_R to LEFT_LOP/M Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_R Output Routing Control 0: PGA_R is not routed to LEFT_LOP/M. 1: PGA_R is routed to LEFT_LOP/M.
D6–D0	R/W	000 0000	PGA_R to LEFT_LOP/M Analog Volume Control For 7-bit register settings versus analog gain values, see 表 8-46.

表 8-82. Page 0, Register 85: DAC_R1 to LEFT_LOP/M Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_R1 Output Routing Control 0: DAC_R1 is not routed to LEFT_LOP/M. 1: DAC_R1 is routed to LEFT_LOP/M.
D6–D0	R/W	000 0000	DAC_R1 to LEFT_LOP/M Analog Volume Control For 7-bit register settings versus analog gain values, see 表 8-46.

表 8-83. Page 0, Register 86: LEFT_LOP/M Output Level Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	0000	LEFT_LOP/M Output Level Control 0000: Output level control = 0 dB 0001: Output level control = 1 dB 0010: Output level control = 2 dB ... 1000: Output level control = 8 dB 1001: Output level control = 9 dB 1010–1111: Reserved. Do not write these sequences to these register bits.
D3	R/W	0	LEFT_LOP/M Mute 0: LEFT_LOP/M is muted. 1: LEFT_LOP/M is not muted.
D2	R	0	Reserved. Do not write to this register bit.
D1	R	1	LEFT_LOP/M Volume Control Status 0: Not all programmed gains to LEFT_LOP/M have been applied yet. 1: All programmed gains to LEFT_LOP/M have been applied.
D0	R/W	0	LEFT_LOP/M Power Status 0: LEFT_LOP/M is not fully powered up. 1: LEFT_LOP/M is fully powered up.

表 8-84. Page 0, Register 87: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	Reserved. Do not write to this register.

表 8-85. Page 0, Register 88: PGA_L to RIGHT_LOP/M Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_L Output Routing Control 0: PGA_L is not routed to RIGHT_LOP/M. 1: PGA_L is routed to RIGHT_LOP/M.
D6–D0	R/W	000 0000	PGA_L to RIGHT_LOP/M Analog Volume Control For 7-bit register settings versus analog gain values, see 表 8-46.

表 8-86. Page 0, Register 89: DAC_L1 to RIGHT_LOP/M Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_L1 Output Routing Control 0: DAC_L1 is not routed to RIGHT_LOP/M. 1: DAC_L1 is routed to RIGHT_LOP/M.
D6–D0	R/W	000 0000	DAC_L1 to RIGHT_LOP/M Analog Volume Control For 7-bit register settings versus analog gain values, see 表 8-46.

表 8-87. Page 0, Register 90: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	Reserved. Do not write to this register.

表 8-88. Page 0, Register 91: PGA_R to RIGHT_LOP/M Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_R Output Routing Control 0: PGA_R is not routed to RIGHT_LOP/M. 1: PGA_R is routed to RIGHT_LOP/M.
D6–D0	R/W	000 0000	PGA_R to RIGHT_LOP/M Analog Volume Control For 7-bit register settings versus analog gain values, see 表 8-46.

表 8-89. Page 0, Register 92: DAC_R1 to RIGHT_LOP/M Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_R1 Output Routing Control 0: DAC_R1 is not routed to RIGHT_LOP/M. 1: DAC_R1 is routed to RIGHT_LOP/M.
D6–D0	R/W	000 0000	DAC_R1 to RIGHT_LOP/M Analog Volume Control For 7-bit register settings versus analog gain values, see 表 8-46.

表 8-90. Page 0, Register 93: RIGHT_LOP/M Output Level Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	0000	RIGHT_LOP/M Output Level Control 0000: Output level control = 0 dB 0001: Output level control = 1 dB 0010: Output level control = 2 dB ... 1000: Output level control = 8 dB 1001: Output level control = 9 dB 1010–1111: Reserved. Do not write these sequences to these bits.
D3	R/W	0	RIGHT_LOP/M Mute 0: RIGHT_LOP/M is muted. 1: RIGHT_LOP/M is not muted.
D2	R	0	Reserved. Do not write to this register bit.
D1	R	1	RIGHT_LOP/M Volume Control Status 0: All programmed gains to RIGHT_LOP/M have been applied. 1: Not all programmed gains to RIGHT_LOP/M have been applied yet
D0	R/W	0	RIGHT_LOP/M Power Status 0: RIGHT_LOP/M is not fully powered up. 1: RIGHT_LOP/M is fully powered up.

表 8-91. Page 0, Register 94: Module Power Status Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Left-DAC Power Status 0: Left DAC is not fully powered up. 1: Left DAC is fully powered up.
D6	R	0	Right-DAC Power Status 0: Right DAC is not fully powered up. 1: Right DAC is fully powered up.
D5	R	0	Reserved. Write only 0 to this bit.
D4	R	0	LEFT_LOP/M Power Status 0: LEFT_LOP/M output driver is powered down. 1: LEFT_LOP/M output driver is powered up.
D3	R	0	RIGHT_LOP/M Power Status 0: RIGHT_LOP/M is not fully powered up. 1: RIGHT_LOP/M is fully powered up.
D2	R	0	HPLOUT Driver Power Status 0: HPLOUT Driver is not fully powered up. 1: HPLOUT Driver is fully powered up.
D1	R	0	HPROUT Driver Power Status 0: HPROUT Driver is not fully powered up. 1: HPROUT Driver is fully powered up.
D0	R	0	Reserved. Do not write to this bit.

表 8-92. Page 0, Register 95: Output Driver Short-Circuit Detection Status Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	HPLOUT Short-Circuit Detection Status 0: No short circuit detected at HPLOUT 1: Short circuit detected at HPLOUT
D6	R	0	HPROUT Short-Circuit Detection Status 0: No short circuit detected at HPROUT 1: Short circuit detected at HPROUT
D5	R	0	HPLCOM Short-Circuit Detection Status 0: No short circuit detected at HPLCOM 1: Short circuit detected at HPLCOM
D4	R	0	HPRCOM Short-Circuit Detection Status 0: No short circuit detected at HPRCOM 1: Short circuit detected at HPRCOM
D3	R	0	HPLCOM Power Status 0: HPLCOM is not fully powered up. 1: HPLCOM is fully powered up.
D2	R	0	HPRCOM Power Status 0: HPRCOM is not fully powered up. 1: HPRCOM is fully powered up.
D1–D0	R	00	Reserved. Do not write to these bits.

表 8-93. Page 0, Register 96: Sticky Interrupt Flags Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	HPLOUT Short-Circuit Detection Status 0: No short circuit detected at HPLOUT driver 1: Short circuit detected at HPLOUT driver
D6	R	0	HPROUT Short-Circuit Detection Status 0: No short circuit detected at HPROUT driver 1: Short circuit detected at HPROUT driver
D5	R	0	HPLCOM Short-Circuit Detection Status 0: No short circuit detected at HPLCOM driver 1: Short circuit detected at HPLCOM driver
D4	R	0	HPRCOM Short-Circuit Detection Status 0: No short circuit detected at HPRCOM driver 1: Short circuit detected at HPRCOM driver
D3	R	0	Reserved. Do not write to this bit.
D2	R	0	Headset Detection Status 0: No headset insertion/removal is detected. 1: Headset insertion/removal is detected.
D1	R	0	Left ADC AGC Noise Gate Status 0: Left ADC signal power is greater than or equal to noise threshold for left AGC. 1: Left ADC signal power is less than noise threshold for left AGC.
D0	R/W	0	Right ADC AGC Noise Gate Status 0: Right ADC signal power is greater than or equal to noise threshold for right AGC. 1: Right ADC signal power is less than noise threshold for right AGC.

表 8-94. Page 0, Register 97: Real-Time Interrupt Flags Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	HPLOUT Short-Circuit Detection Status 0: No short circuit detected at HPLOUT driver 1: Short circuit detected at HPLOUT driver
D6	R	0	HPROUT Short-Circuit Detection Status 0: No short circuit detected at HPROUT driver 1: Short circuit detected at HPROUT driver

表 8-94. Page 0, Register 97: Real-Time Interrupt Flags Register (続き)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5	R	0	HPLCOM Short-Circuit Detection Status 0: No short circuit detected at HPLCOM driver 1: Short circuit detected at HPLCOM driver
D4	R	0	HPRCOM Short-Circuit Detection Status 0: No short circuit detected at HPRCOM driver 1: Short circuit detected at HPRCOM driver
D3	R	0	Reserved. Do not write to this bit.
D2	R	0	Headset Detection Status 0: No headset insertion/removal is detected. 1: Headset insertion/removal is detected.
D1	R	0	Left ADC AGC Noise Gate Status 0: Left ADC signal power is greater than noise threshold for left AGC. 1: Left ADC signal power lower than noise threshold for left AGC.
D0	R	0	Right ADC AGC Noise Gate Status 0: Right ADC signal power is greater than noise threshold for right AGC. 1: Right ADC signal power is lower than noise threshold for right AGC.

表 8-95. Page 0, Register 98–100: Reserved Registers

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved. Do not write to these registers.

表 8-96. Page 0, Register 101: Clock Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D1	R	0000 000	Reserved. Write only zeros to these bits.(1)
D0	R/W	0	CODEC_CLKIN Source Selection 0: CODEC_CLKIN uses PLLDIV_OUT 1: CODEC_CLKIN uses CLKDIV_OUT

(1) Bits D7–D1 in register 101 are only valid in I^2C control mode, when SELECT = 0.

表 8-97. Page 0, Register 102: Clock Generation Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	CLKDIV_IN Source Selection 00: CLKDIV_IN uses MCLK. 01: CLKDIV_IN uses GPIO2. 10: CLKDIV_IN uses BCLK. 11: Reserved. Do not use.
D5–D4	R/W	00	PLLCLK_IN Source Selection 00: PLLCLK_IN uses MCLK. 01: PLLCLK_IN uses GPIO2. 10: PLLCLK _IN uses BCLK. 11: Reserved. Do not use.
D3–D0	R/W	0010	Reserved. Write only 0010 to these bits.

表 8-98. Page 0, Register 103: Left-AGC New Programmable Attack Time Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Attack Time Register Selection 0: Attack time for the left AGC is generated from page 0, register 26. 1: Attack time for the left AGC is generated from this register.

表 8-98. Page 0, Register 103: Left-AGC New Programmable Attack Time Register (続き)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6–D5	R/W	00	Baseline AGC Attack time 00: Left-AGC attack time = 7 ms 01: Left-AGC attack time = 8 ms 10: Left-AGC attack time = 10 ms 11: Left-AGC attack time = 11 ms
D4–D2	R/W	000	Multiplication Factor for Baseline AGC 000: Multiplication factor for the baseline AGC attack time = 1 001: Multiplication factor for the baseline AGC attack time = 2 010: Multiplication factor for the baseline AGC attack time = 4 011: Multiplication factor for the baseline AGC attack time = 8 100: Multiplication factor for the baseline AGC attack time = 16 101: Multiplication factor for the baseline AGC attack time = 32 110: Multiplication factor for the baseline AGC attack time = 64 111: Multiplication factor for the baseline AGC attack time = 128
D1–D0	R/W	00	Reserved. Write only zeros to these bits.

表 8-99. Page 0, Register 104: Left-AGC New Programmable Decay Time Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Decay Time Register Selection (1) 0: Decay time for the left AGC is generated from page 0, register 26. 1: Decay time for the left AGC is generated from this register.
D6–D5	R/W	00	Baseline AGC Decay Time 00: Left-AGC decay time = 50 ms 01: Left-AGC decay time = 150 ms 10: Left-AGC decay time = 250 ms 11: Left-AGC decay time = 350 ms
D4–D2	R/W	000	Multiplication Factor for Baseline AGC 000: Multiplication factor for the baseline AGC decay time = 1 001: Multiplication factor for the baseline AGC decay time = 2 010: Multiplication factor for the baseline AGC decay time = 4 011: Multiplication factor for the baseline AGC decay time = 8 100: Multiplication factor for the baseline AGC decay time = 16 101: Multiplication factor for the baseline AGC decay time = 32 110: Multiplication factor for the baseline AGC decay time = 64 111: Multiplication factor for the baseline AGC decay time = 128
D1–D0	R/W	00	Reserved. Write only zeros to these bits.

(1) Decay time is limited based on NCODEC ratio that is selected. For
NCODEC = 1, Maximum decay time = 4 s
NCODEC = 1.5, Maximum decay time = 5.6 s
NCODEC = 2, Maximum decay time = 8 s
NCODEC = 2.5, Maximum decay time = 9.6 s
NCODEC = 3 or 3.5, Maximum decay time = 11.2 s
NCODEC = 4 or 4.5, Maximum decay time = 16 s
NCODEC = 5, Maximum decay time = 19.2 s
NCODEC = 5.5 or 6, Maximum decay time = 22.4 s

表 8-100. Page 0, Register 105: Right-AGC New Programmable Attack Time Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Attack Time Register Selection 0: Attack time for the right AGC is generated from page 0, register 29. 1: Attack time for the right AGC is generated from this register.
D6–D5	R/W	00	Baseline AGC attack time 00: Right-AGC attack time = 7 ms 01: Right-AGC attack time = 8 ms 10: Right-AGC attack time = 10 ms 11: Right-AGC attack time = 11 ms

表 8-100. Page 0, Register 105: Right-AGC New Programmable Attack Time Register (続き)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D4–D2	R/W	000	Multiplication Factor for Baseline AGC 000: Multiplication factor for the baseline AGC attack time = 1 001: Multiplication factor for the baseline AGC attack time = 2 010: Multiplication factor for the baseline AGC attack time = 4 011: Multiplication factor for the baseline AGC attack time = 8 100: Multiplication factor for the baseline AGC attack time = 16 101: Multiplication factor for the baseline AGC attack time = 32 110: Multiplication factor for the baseline AGC attack time = 64 111: Multiplication factor for the baseline AGC attack time = 128
D1–D0	R/W	00	Reserved. Write only zeros to these bits.

表 8-101. Page 0, Register 106: Right-AGC New Programmable Decay Time Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Decay Time Register Selection (1) 0: Decay time for the right AGC is generated from page 0, register 29. 1: Decay time for the right AGC is generated from this register.
D6–D5	R/W	00	Baseline AGC Decay Time 00: Right-AGC decay time = 50 ms 01: Right-AGC decay time = 150 ms 10: Right-AGC decay time = 250 ms 11: Right-AGC decay time = 350 ms
D4–D2	R/W	000	Multiplication Factor for Baseline AGC 000: Multiplication factor for the baseline AGC decay time = 1 001: Multiplication factor for the baseline AGC decay time = 2 010: Multiplication factor for the baseline AGC decay time = 4 011: Multiplication factor for the baseline AGC decay time = 8 100: Multiplication factor for the baseline AGC decay time = 16 101: Multiplication factor for the baseline AGC decay time = 32 110: Multiplication factor for the baseline AGC decay time = 64 111: Multiplication factor for the baseline AGC decay time = 128
D1–D0	R/W	00	Reserved. Write only zeros to these bits.

(1) Decay time is limited based on NCODEC ratio that is selected. For
NCODEC = 1, Maximum decay time = 4 seconds
NCODEC = 1.5, Maximum decay time = 5.6 seconds
NCODEC = 2, Maximum decay time = 8 seconds
NCODEC = 2.5, Maximum decay time = 9.6 seconds
NCODEC = 3 or 3.5, Maximum decay time = 11.2 seconds
NCODEC = 4 or 4.5, Maximum decay time = 16 seconds
NCODEC = 5, Maximum decay time = 19.2 seconds
NCODEC = 5.5 or 6, Maximum decay time = 22.4 seconds

表 8-102. Page 0, Register 107: New Programmable ADC Digital Path and I^2C Bus Condition Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Left-Channel High-Pass Filter Coefficient Selection 0: Default coefficients are used when ADC high pass is enabled. 1: Programmable coefficients are used when ADC high pass is enabled.
D6	R/W	0	Right-Channel High-Pass Filter Coefficient Selection 0: Default coefficients are used when ADC high pass is enabled. 1: Programmable coefficients are used when ADC high pass is enabled.
D5–D4	R/W	00	ADC Decimation Filter Configuration 00: Left and right digital microphones are used. 01: Left digital microphone and right analog microphone are used. 10: Left analog microphone and right digital microphone are used. 11: Left and right analog microphones are used.
D3	R/W	0	ADC Digital Output to Programmable Filter Path Selection 0: No additional programmable filters other than the HPF are used for the ADC. 1: The programmable filter is connected to ADC output, if both DACs are powered down.

表 8-102. Page 0, Register 107: New Programmable ADC Digital Path and I²C Bus Condition Register (続き)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D2	R/W	0	I²C Bus Condition Detector 0: Internal logic is enabled to detect an I²C bus error, and clears the bus error condition. 1: Internal logic is disabled to detect an I²C bus error.
D1	R	0	Reserved. Write only zero to these register bits.
D0	R	0	I²C Bus Error Detection Status 0: I²C bus error is not detected. 1: I²C bus error is detected. This bit is cleared by reading this register.

表 8-103. Page 0, Register 108: Passive Analog Signal Bypass Selection During Power Down Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Reserved. Write only zero to this bit.
D6	R/W	0	Reserved. Write only zero to these register bits.
D5	R/W	0	LINE1RM Path Selection 0: Normal signal path 1: Signal is routed by a switch to RIGHT_LOM.
D4	R/W	0	LINE1RP Path Selection 0: Normal signal path 1: Signal is routed by a switch to RIGHT_LOP.
D3	R/W	0	Reserved. Write only zero to this bit.
D2	R/W	0	Reserved. Write only zero to these register bits.
D1	R/W	0	LINE1LM Path Selection 0: Normal signal path 1: Signal is routed by a switch to LEFT_LOM.
D0	R/W	0	LINE1LP Path Selection 0: Normal signal path 1: Signal is routed by a switch to LEFT_LOP.

Based on the register 108 settings, if BOTH LINE1 and LINE2 inputs are routed to the output at the same time, then the two switches used for the connection short the two input signals together on the output pins. The shorting resistance between the two input pins is two times the bypass switch resistance (RDS(ON)). In general, this condition of shorting should be avoided, as higher drive currents are likely to occur on the circuitry that feeds these two input pins of this device.

表 8-104. Page 0, Register 109: DAC Quiescent Current Adjustment Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	DAC Current Adjustment 00: Default 01: 50% increase in DAC reference current 10: Reserved 11: 100% increase in DAC reference current
D5–D0	R/W	00 0000	Reserved. Write only zeros to these bits.

表 8-105. Page 0, Register 110–127: Reserved Registers

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved. Do not write to these registers.

表 8-106. Page 1, Register 0: Page Select Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D1	X	0000 000	Reserved, write only zeros to these bits.
D0	R/W	0	Page Select Bit Writing zero to this bit sets page 0 as the active page for following register accesses. Writing a one to this bit sets page 1 as the active page for following register accesses. It is recommended that the user read this register bit back after each write, to ensure that the proper page is being accessed for future register read/writes. This register has the same functionality on page 0 and page 1.

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When programming any coefficient value in Page 1, the MSB register should always be written first, immediately followed by the LSB register. Even if only the MSB or LSB of the coefficient changes, both registers should be written in this sequence.

表 8-107. Page 1, Register 1: Left-Channel Audio Effects Filter N0 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0110 1011	Left-Channel Audio Effects Filter N0 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-108. Page 1, Register 2: Left-Channel Audio Effects Filter N0 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1110 0011	Left-Channel Audio Effects Filter N0 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-109. Page 1, Register 3: Left-Channel Audio Effects Filter N1 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1001 0110	Left-Channel Audio Effects Filter N1 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-110. Page 1, Register 4: Left-Channel Audio Effects Filter N1 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0110 0110	Left-Channel Audio Effects Filter N1 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-111. Page 1, Register 5: Left-Channel Audio Effects Filter N2 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0110 0111	Left-Channel Audio Effects Filter N2 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-112. Page 1, Register 6: Left-Channel Audio Effects Filter N2 Coefficient LSB

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0101 1101	Left-Channel Audio Effects Filter N2 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-113. Page 1, Register 7: Left-Channel Audio Effects Filter N3 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0110 1011	Left-Channel Audio Effects Filter N3 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-114. Page 1, Register 8: Left-Channel Audio Effects Filter N3 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1110 0011	Left-Channel Audio Effects Filter N3 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-115. Page 1, Register 9: Left-Channel Audio Effects Filter N4 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1001 0110	Left-Channel Audio Effects Filter N4 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-116. Page 1, Register 10: Left-Channel Audio Effects Filter N4 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0110 0110	Left-Channel Audio Effects Filter N4 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-117. Page 1, Register 11: Left-Channel Audio Effects Filter N5 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0110 0111	Left-Channel Audio Effects Filter N5 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-118. Page 1, Register 12: Left-Channel Audio Effects Filter N5 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0101 1101	Left-Channel Audio Effects Filter N5 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-119. Page 1, Register 13: Left-Channel Audio Effects Filter D1 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0111 1101	Left-Channel Audio Effects Filter D1 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-120. Page 1, Register 14: Left-Channel Audio Effects Filter D1 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1000 0011	Left-Channel Audio Effects Filter D1 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-121. Page 1, Register 15: Left-Channel Audio Effects Filter D2 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1000 0100	Left-Channel Audio Effects Filter D2 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-122. Page 1, Register 16: Left-Channel Audio Effects Filter D2 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1110 1110	Left-Channel Audio Effects Filter D2 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-123. Page 1, Register 17: Left-Channel Audio Effects Filter D4 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0111 1101	Left-Channel Audio Effects Filter D4 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-124. Page 1, Register 18: Left-Channel Audio Effects Filter D4 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1000 0011	Left-Channel Audio Effects Filter D4 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-125. Page 1, Register 19: Left-Channel Audio Effects Filter D5 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1000 0100	Left-Channel Audio Effects Filter D5 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-126. Page 1, Register 20: Left-Channel Audio Effects Filter D5 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1110 1110	Left-Channel Audio Effects Filter D5 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-127. Page 1, Register 21: Left-Channel De-Emphasis Filter N0 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0011 1001	Left-Channel De-Emphasis Filter N0 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-128. Page 1, Register 22: Left-Channel De-Emphasis Filter N0 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0101 0101	Left-Channel De-Emphasis Filter N0 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-129. Page 1, Register 23: Left-Channel De-Emphasis Filter N1 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1111 0011	Left-Channel De-Emphasis Filter N1 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-130. Page 1, Register 24: Left-Channel De-Emphasis Filter N1 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0010 1101	Left-Channel De-Emphasis Filter N1 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-131. Page 1, Register 25: Left-Channel De-Emphasis Filter D1 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0101 0011	Left-Channel De-Emphasis Filter D1 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-132. Page 1, Register 26: Left-Channel De-Emphasis Filter D1 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0111 1110	Left-Channel De-Emphasis Filter D1 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-133. Page 1, Register 27: Right-Channel Audio Effects Filter N0 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0110 1011	Right-Channel Audio Effects Filter N0 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-134. Page 1, Register 28: Right-Channel Audio Effects Filter N0 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1110 0011	Right-Channel Audio Effects Filter N0 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-135. Page 1, Register 29: Right-Channel Audio Effects Filter N1 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1001 0110	Right-Channel Audio Effects Filter N1 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-136. Page 1, Register 30: Right-Channel Audio Effects Filter N1 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0110 0110	Right-Channel Audio Effects Filter N1 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-137. Page 1, Register 31: Right-Channel Audio Effects Filter N2 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0110 0111	Right-Channel Audio Effects Filter N2 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-138. Page 1, Register 32: Right-Channel Audio Effects Filter N2 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0101 1101	Right-Channel Audio Effects Filter N2 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-139. Page 1, Register 33: Right-Channel Audio Effects Filter N3 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0110 1011	Right-Channel Audio Effects Filter N3 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-140. Page 1, Register 34: Right-Channel Audio Effects Filter N3 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1110 0011	Right-Channel Audio Effects Filter N3 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-141. Page 1, Register 35: Right-Channel Audio Effects Filter N4 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1001 0110	Right-Channel Audio Effects Filter N4 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-142. Page 1, Register 36: Right-Channel Audio Effects Filter N4 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0110 0110	Right-Channel Audio Effects Filter N4 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-143. Page 1, Register 37: Right-Channel Audio Effects Filter N5 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0110 0111	Right-Channel Audio Effects Filter N5 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-144. Page 1, Register 38: Right-Channel Audio Effects Filter N5 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0101 1101	Right-Channel Audio Effects Filter N5 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-145. Page 1, Register 39: Right-Channel Audio Effects Filter D1 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0111 1101	Right-Channel Audio Effects Filter D1 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-146. Page 1, Register 40: Right-Channel Audio Effects Filter D1 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1000 0011	Right-Channel Audio Effects Filter D1 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-147. Page 1, Register 41: Right-Channel Audio Effects Filter D2 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1000 0100	Right-Channel Audio Effects Filter D2 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-148. Page 1, Register 42: Right-Channel Audio Effects Filter D2 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1110 1110	Right-Channel Audio Effects Filter D2 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-149. Page 1 / Register 43: Right-Channel Audio Effects Filter D4 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0111 1101	Right-Channel Audio Effects Filter D4 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-150. Page 1 / Register 44: Right-Channel Audio Effects Filter D4 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1000 0011	Right-Channel Audio Effects Filter D4 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-151. Page 1 / Register 45: Right-Channel Audio Effects Filter D5 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1000 0100	Right-Channel Audio Effects Filter D5 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-152. Page 1 / Register 46: Right-Channel Audio Effects Filter D5 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1110 1110	Right-Channel Audio Effects Filter D5 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-153. Page 1 / Register 47: Right-Channel De-Emphasis Filter N0 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0011 1001	Right-Channel De-Emphasis Filter N0 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-154. Page 1 / Register 48: Right-Channel De-Emphasis Filter N0 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0101 0101	Right-Channel De-Emphasis Filter N0 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-155. Page 1 / Register 49: Right-Channel De-Emphasis Filter N1 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1111 0011	Right-Channel De-Emphasis Filter N1 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-156. Page 1 / Register 50: Right-Channel De-Emphasis Filter N1 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0010 1101	Right-Channel De-Emphasis Filter N1 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-157. Page 1 / Register 51: Right-Channel De-Emphasis Filter D1 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0101 0011	Right-Channel De-Emphasis Filter D1 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-158. Page 1 / Register 52: Right-Channel De-Emphasis Filter D1 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0111 1110	Right-Channel De-Emphasis Filter D1 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-159. Page 1 / Register 53: 3-D Attenuation Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0111 1111	3-D Attenuation Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-160. Page 1 / Register 54: 3-D Attenuation Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1111 1111	3-D Attenuation Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-161. Page 1 / Register 55–64: Reserved Registers

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved. Do not write to these registers.

表 8-162. Page 1 / Register 65: Left-Channel ADC High-Pass Filter N0 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0011 1001	Left-Channel ADC High-Pass Filter N0 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-163. Page 1 / Register 66: Left-Channel ADC High-Pass Filter N0 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0101 0101	Left-Channel ADC High-Pass Filter N0 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-164. Page 1 / Register 67: Left-Channel ADC High-Pass Filter N1 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1111 0011	Left-Channel ADC High-Pass Filter N1 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-165. Page 1 / Register 68: Left-Channel ADC High-Pass Filter N1 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0010 1101	Left-Channel ADC High-Pass Filter N1 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-166. Page 1 / Register 69: Left-Channel ADC High-Pass Filter D1 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0101 0011	Left-Channel ADC High-Pass Filter D1 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-167. Page 1 / Register 70: Left-Channel ADC High-Pass Filter D1 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0111 1110	Left-Channel ADC High-Pass Filter D1 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-168. Page 1 / Register 71: Right-Channel ADC High-Pass Filter N0 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0011 1001	Right-Channel ADC High-Pass Filter N0 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-169. Page 1 / Register 72: Right-Channel ADC High-Pass Filter N0 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0101 0101	Right-Channel ADC High-Pass Filter N0 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-170. Page 1 / Register 73: Right-Channel ADC High-Pass Filter N1 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1111 0011	Right-Channel ADC High-Pass Filter N1 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-171. Page 1 / Register 74: Right-Channel ADC High-Pass Filter N1 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0010 1101	Right-Channel ADC High-Pass Filter N1 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-172. Page 1 / Register 75: Right-Channel ADC High-Pass Filter D1 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0101 0011	Right-Channel ADC High-Pass Filter D1 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-173. Page 1 / Register 76: Right-Channel ADC High-Pass Filter D1 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0111 1110	Right-Channel ADC High-Pass Filter D1 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767.

表 8-174. Page 1 / Registers 77–127: Reserved Registers

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved. Do not write to these registers.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TLV320AIC3104-Q1 is a highly integrated low-power stereo audio codec with integrated stereo headphone/line amplifier, as well as multiple inputs and outputs that are programmable in single-ended or fully differential configurations. All the features of the TLV320AIC3104-Q1 are accessed by programmable registers. External processor with I ^{2}C protocol is required to control the device. It is good practice to perform a hardware reset after initial power up to ensure that all registers are in their default states. Extensive register-based power control is included, enabling stereo 48-kHz DAC playback as low as 14 mW from a 3.3-V analog supply, making it ideal for various car audio applications such as cluster, telematics, emergency call (eCall), navigation systems, and head units.

9.2 Typical Applications

9.2.1 External Speaker Driver in Infotainment and Cluster Applications

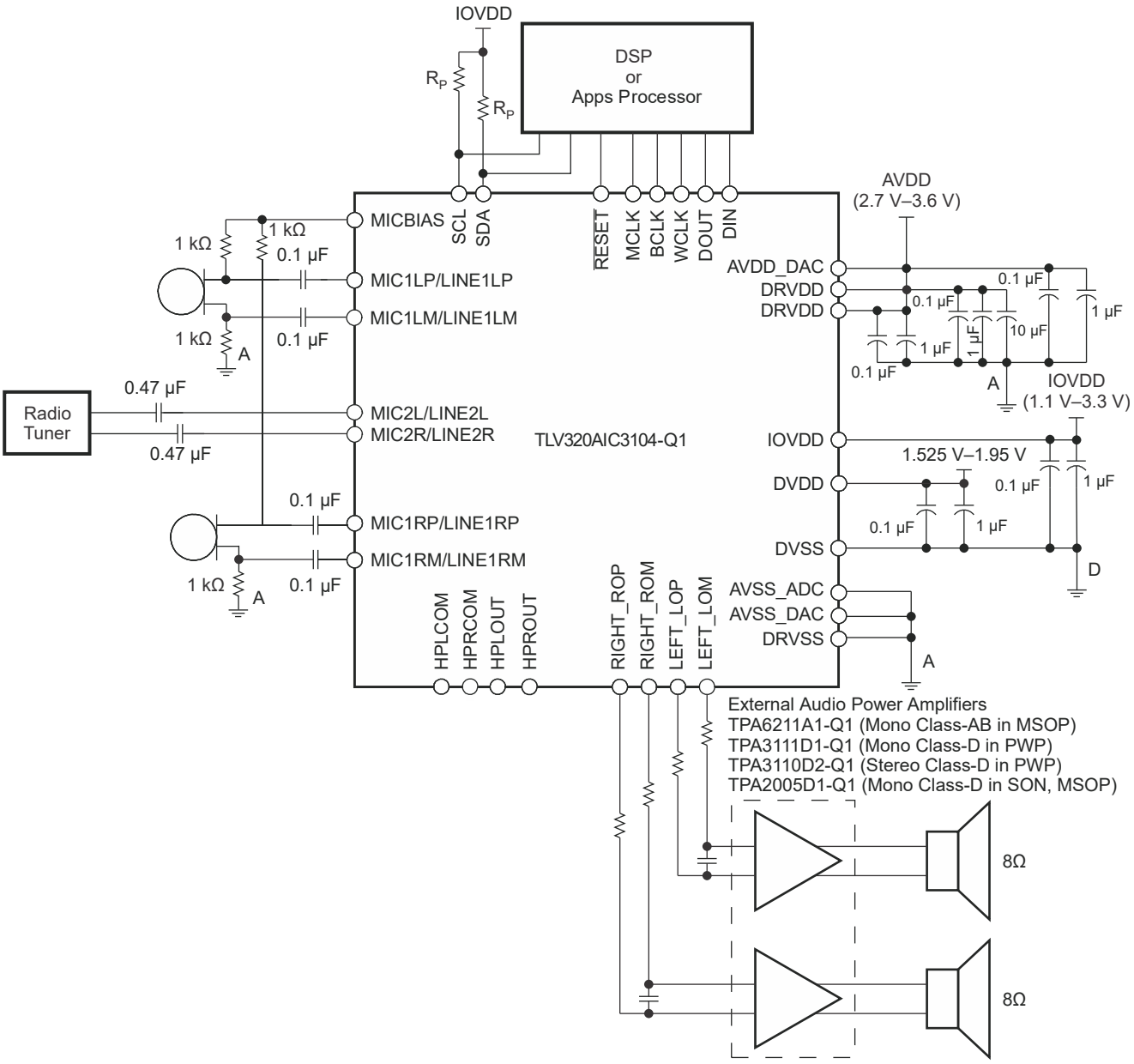

図 9-1. Typical Connections With Differential Inputs for External Speaker Driver

9.2.1.1 Design Requirements

For this design example, use the parameters shown in 表 9-1.

表 9-1. Design Parameters

PARAMETER	VALUE
Supply Voltage (AVDD, DRVDD)	3.3 V
Supply Voltage (DVDD, IOVDD)	1.8 V
Analog Fully Differential Line Output Driver Load	10 kΩ

9.2.1.2 Detailed Design Procedure

- Use 図 9-1as a guide to integrate the hardware into the system.
- Following the recommended component placement, schematic layout and routing given in 図 9-7, integrate the device and its supporting components into the system PCB file.
- Determining sample rate and master clock frequency is required when powering up the device because all internal timing is derived from the master clock. Refer to the Audio Clock Generation section to obtain more information on how to configure correctly the required clocks for the device.
- As the TLV320AIC3104-Q1 is designed for low-power applications, when powered up, the device has several features powered down. A correct routing of the TLV320AIC3104-Q1 signals is achieved by a correct setting of the device registers, powering up the required stages of the device and configuring the internal switches to follow a desired route.

9.2.1.3 Application Curves

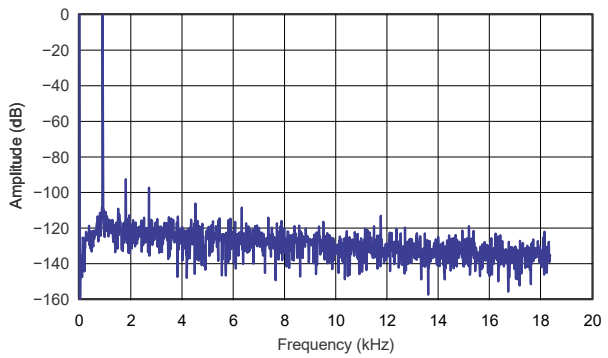

図 9-2. DAC to Line Output FFT at 1-kHz Signal Plot

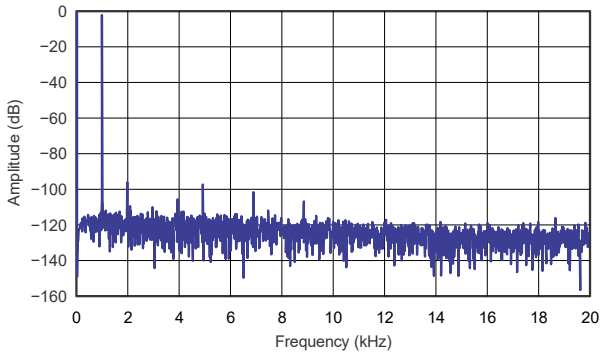

図 9-3. Line Input to ADC FFT at 1-kHz Signal Plot

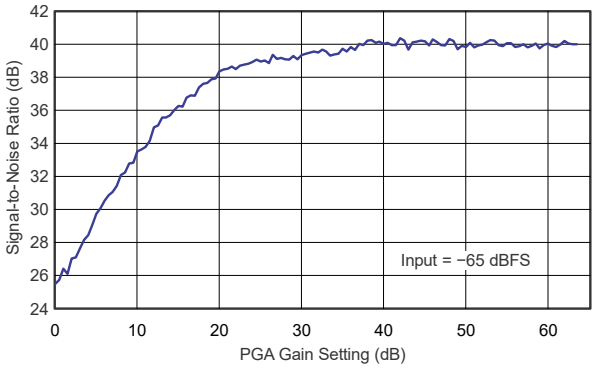

図 9-4. ADC SNR vs PGA Gain Setting, –65-dBfs Input

9.2.2 External Speaker Amplifier With Separate Line Outputs

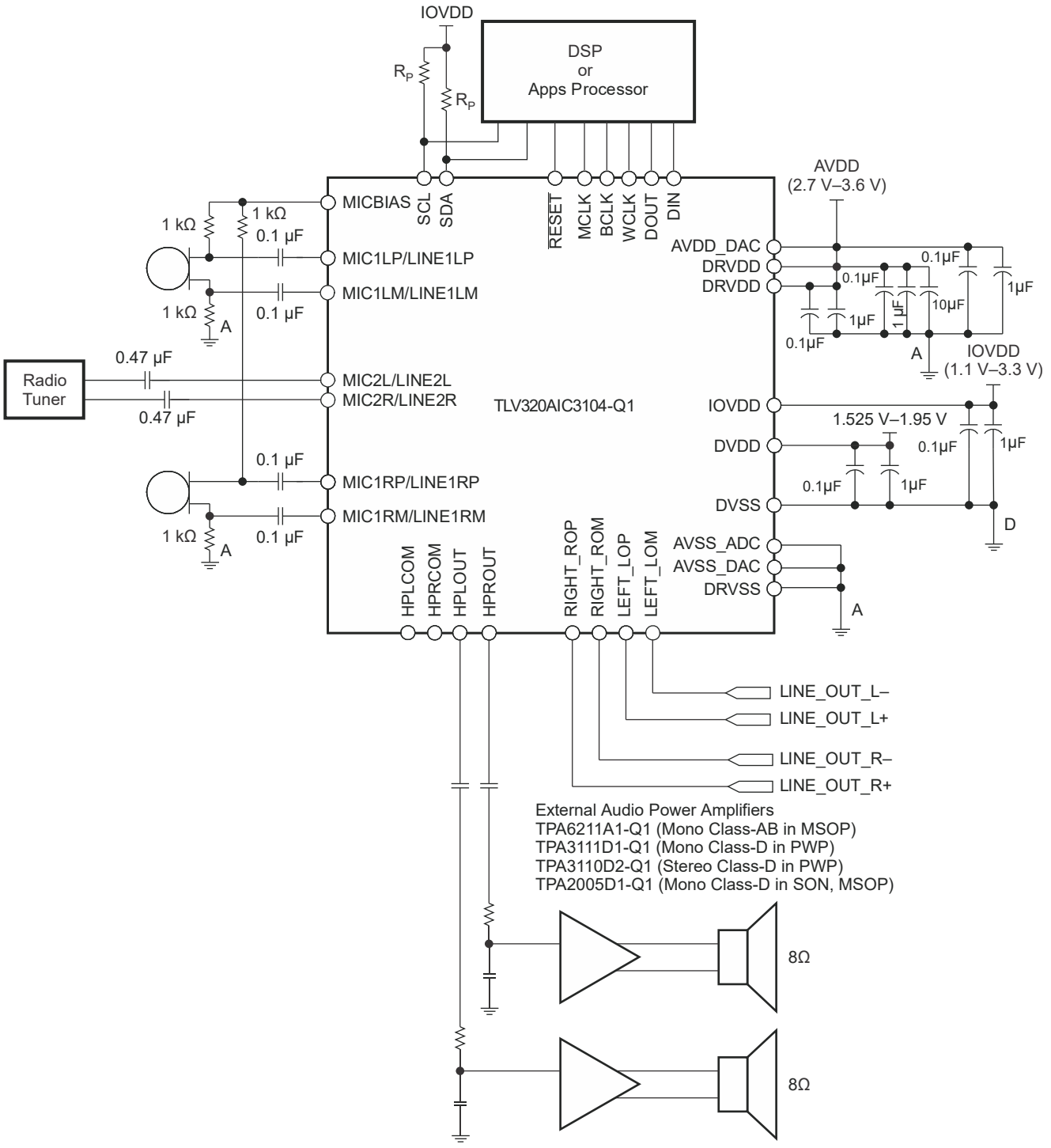

図 9-5. Typical Connections With Single-Ended Outputs for External Amplifier With Separate Line Outputs

9.2.2.1 Design Requirements

Refer to the previous *Design Requirements* section.

9.2.2.2 Detailed Design Procedure

Refer to the previous *Detailed Design Procedure* section.

9.3 Power Supply Recommendations

The TLV320AIC3104-Q1 has been designed to be extremely tolerant of power supply sequencing. However, in some rare instances, unexpected conditions can be attributed to power supply sequencing. The following sequence will provide the most robust operation.

Power up IOVDD first. The analog supplies, which include AVDD and DRVDD, should be powered up second. The digital supply DVDD should be powered up last. Keep RESET low until all supplies are stable. The analog supplies should be greater than or equal to DVDD at all times.

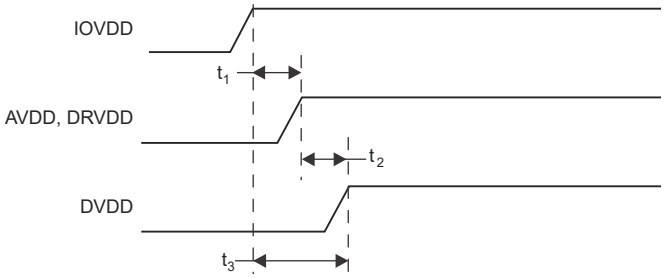

図 9-6. Power-Supply Sequencing

表 9-2. TLV320AIC3104-Q1 Power-Supply Sequencing

		MIN	MAX	UNIT
t1	IOVDD to AVDD, DRVDD	0		ms
t2	AVDD to DVDD	0	5	
t3	IOVDD, to DVDD	0		

9.4 Layout

9.4.1 Layout Guidelines

PCB design is made considering the application, and the review is specific for each system requirements. However, general considerations can optimize the system performance.

- The TLV320AIC3104-Q1 thermal pad should be connected to analog output driver ground.
- Analog and digital grounds should be separated to prevent possible digital noise from affecting the analog performance of the board.
- The TLV320AIC3104-Q1 requires the decoupling capacitors to be placed as close as possible to the device power supply terminals.
- If possible, route the differential audio signals differentially on the PCB. This is recommended to get better noise immunity.

9.4.2 Layout Example

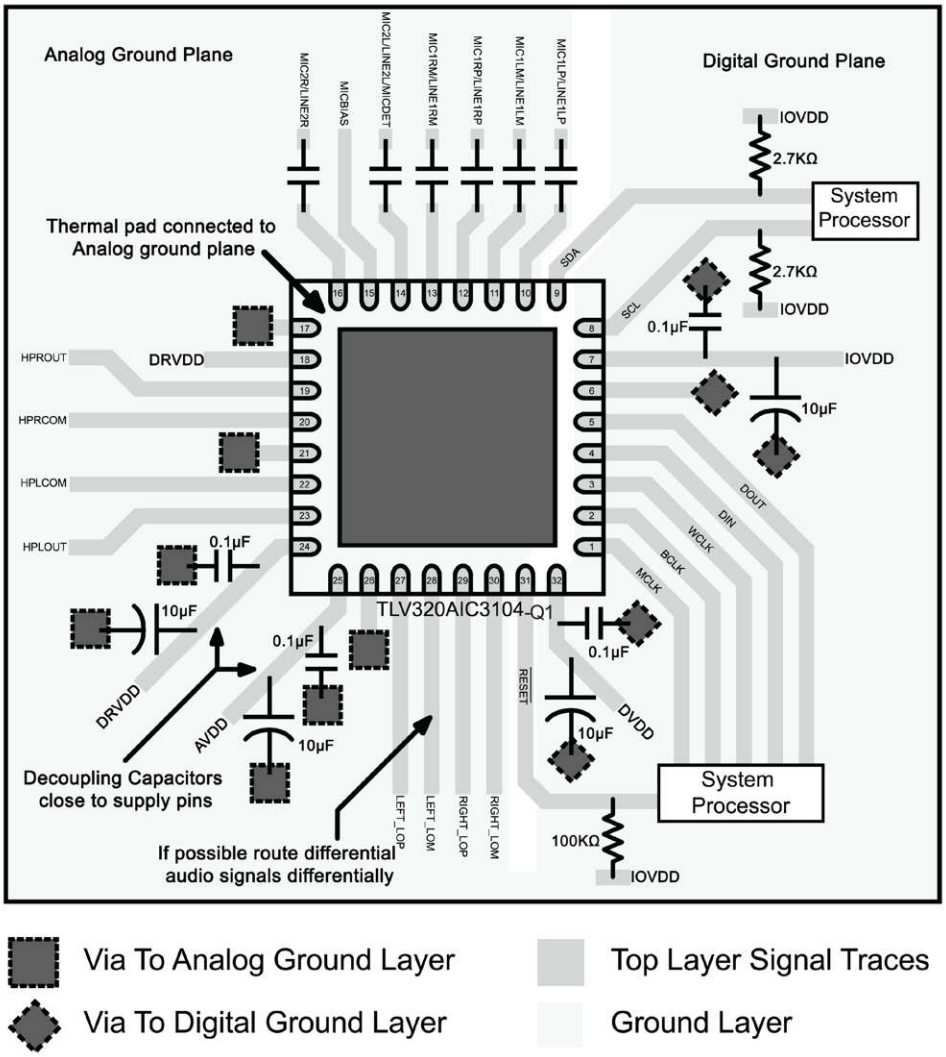

図 9-7. Layout Example

10 Device and Documentation Support

10.1 Device Support

10.1.1 Device Nomenclature

Target level Represents the nominal output level at which the AGC attempts to hold the ADC output signal level.

Attack time Determines how quickly the AGC circuitry reduces the PGA gain when the input signal is too loud. It can be varied from 7 ms to 1,408 ms.

Decay time Determines how quickly the PGA gain is increased when the input signal is too low. It can be varied in the range from 0.05 s to 22.4 s.

Noise gate threshold Determines the level at which the input speech average falls below.

Maximum PGA gain applicable Allows the user to restrict the maximum PGA gain that can be applied by the AGC algorithm.

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation see the following:

- *TIDA-00724 Automotive Emergency Call (eCall) Audio Subsystem Reference Design*
- *TPA3111D1-Q1 10-W Filter-Free Mono Class-D Audio Power Amplifier With SpeakerGuard™*
- *TPA3110D2-Q1 15-W Filter-Free Stereo Class D Audio Power Amplifier with SpeakerGuard™*
- *TPA6211A1-Q1 3.1-W Mono Fully Differential Audio Power Amplifier*
- *TPA2005D1-Q1 1.4-W Mono Filter-Free Class-D Audio Amplifier*

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 Community Resources

10.5 Trademarks

すべての商標は、それぞれの所有者に帰属します。

10.6 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

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11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (January 2023) to Revision D (October 2024)	Page
• データシート全体のフォーマットを更新。	1
• Updated Junction Temperature Max Rating	6

Changes from Revision B (February 2017) to Revision C (January 2023)	Page
• Added TLV320ATC3104-Q1 to orderable table	96

Changes from Revision A (March 2016) to Revision B (February 2017)	Page
• Changed the *Input Impedance and VCM Control* section	30
• Changed the *Hardware Reset* section	39
• Added the *Receiving Notification of Documentation Updates* section	95
• Changed the *Electrostatic Discharge Caution* statement	95

Changes from Revision * (June 2010) to Revision A (March 2016)	Page
• 「製品情報」表、「ピン構成および機能」セクション、「仕様」セクション、「機能説明」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加	1

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
6PAIC3104IRHBRQ1	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	3104I	Samples
6PAIC3104TRHBRQ1	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	3104T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TLV320AIC3104-Q1 :

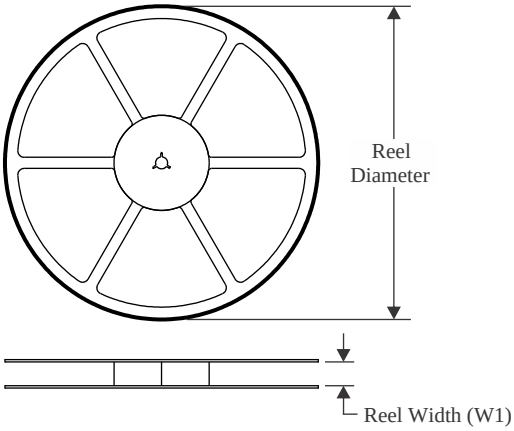
- Catalog : TLV320AIC3104

NOTE: Qualified Version Definitions:

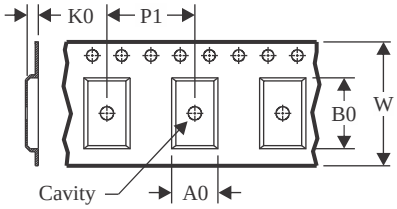
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

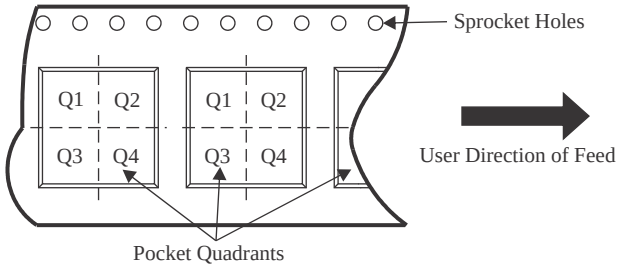


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

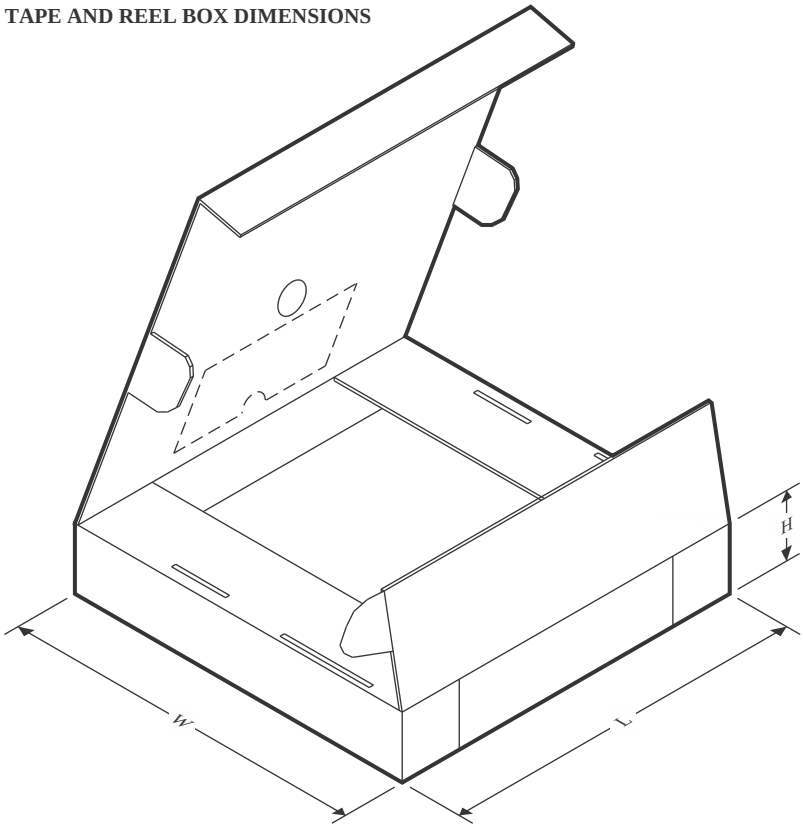
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
6PAIC3104IRHBRQ1	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
6PAIC3104TRHBRQ1	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
6PAIC3104IRHBRQ1	VQFN	RHB	32	3000	367.0	367.0	35.0
6PAIC3104TRHBRQ1	VQFN	RHB	32	3000	367.0	367.0	35.0

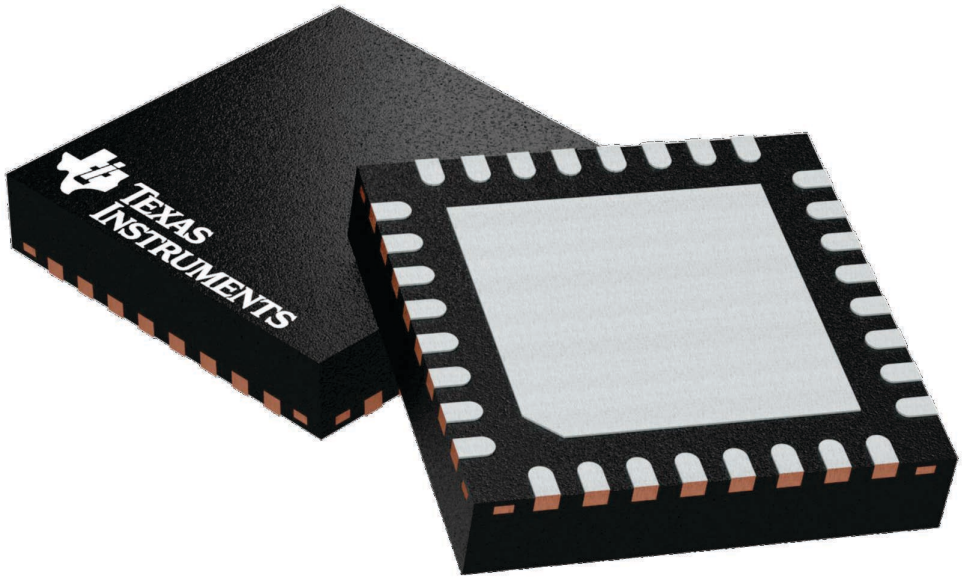
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

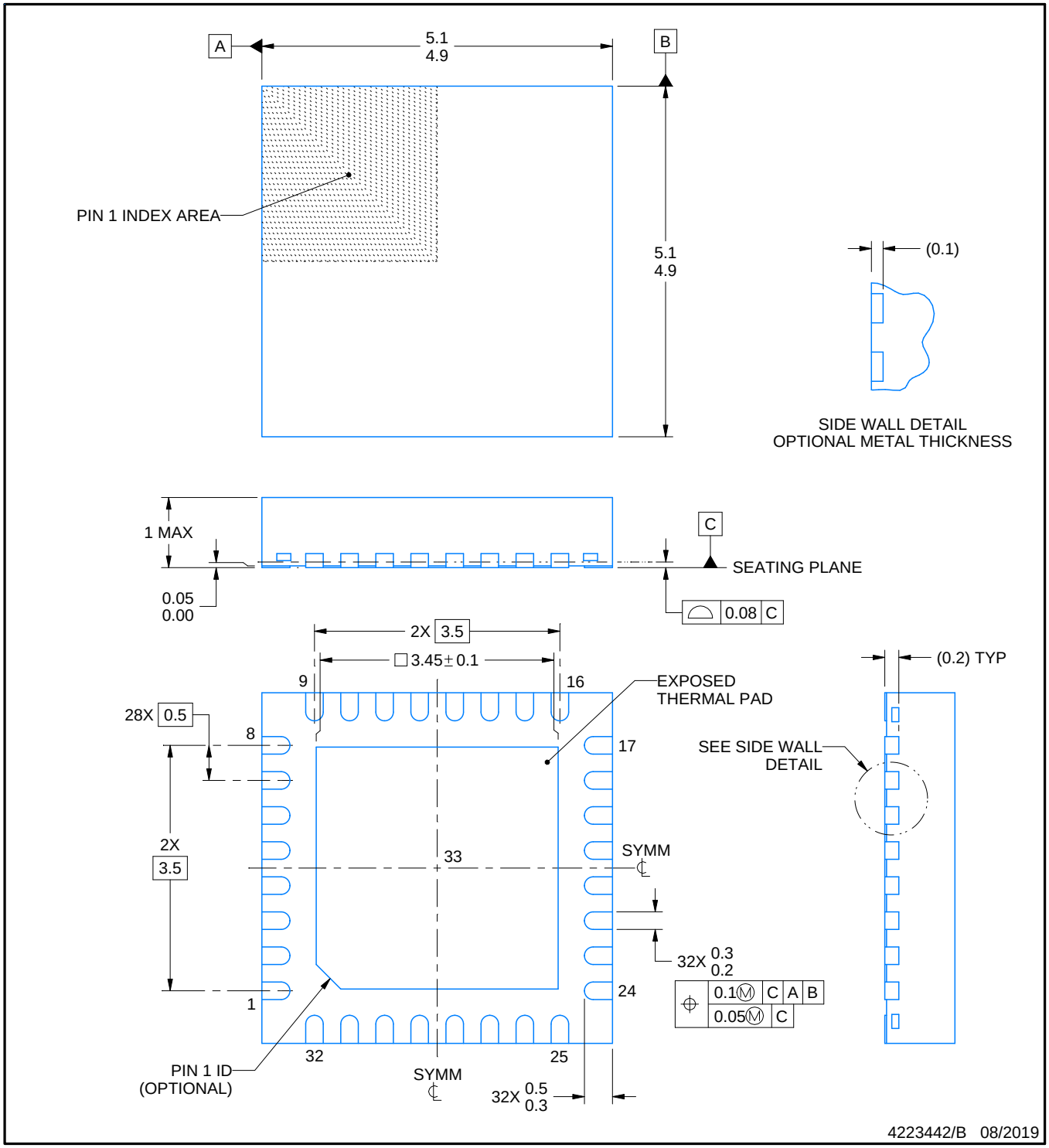
4224745/A

RHB0032E

PACKAGE OUTLINE

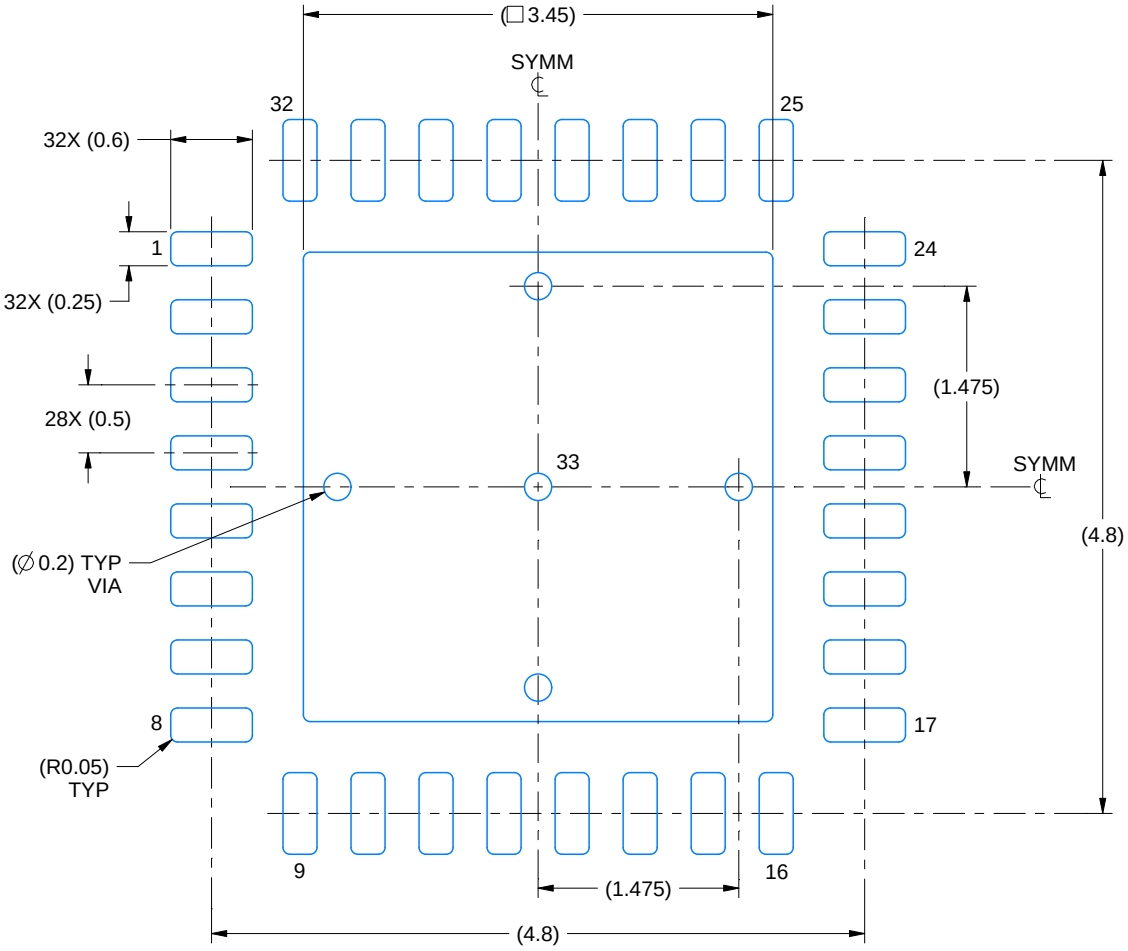
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

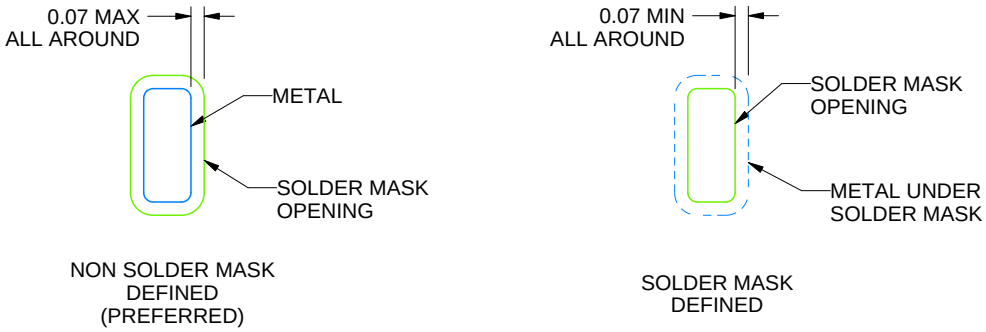


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X



SOLDER MASK DETAILS

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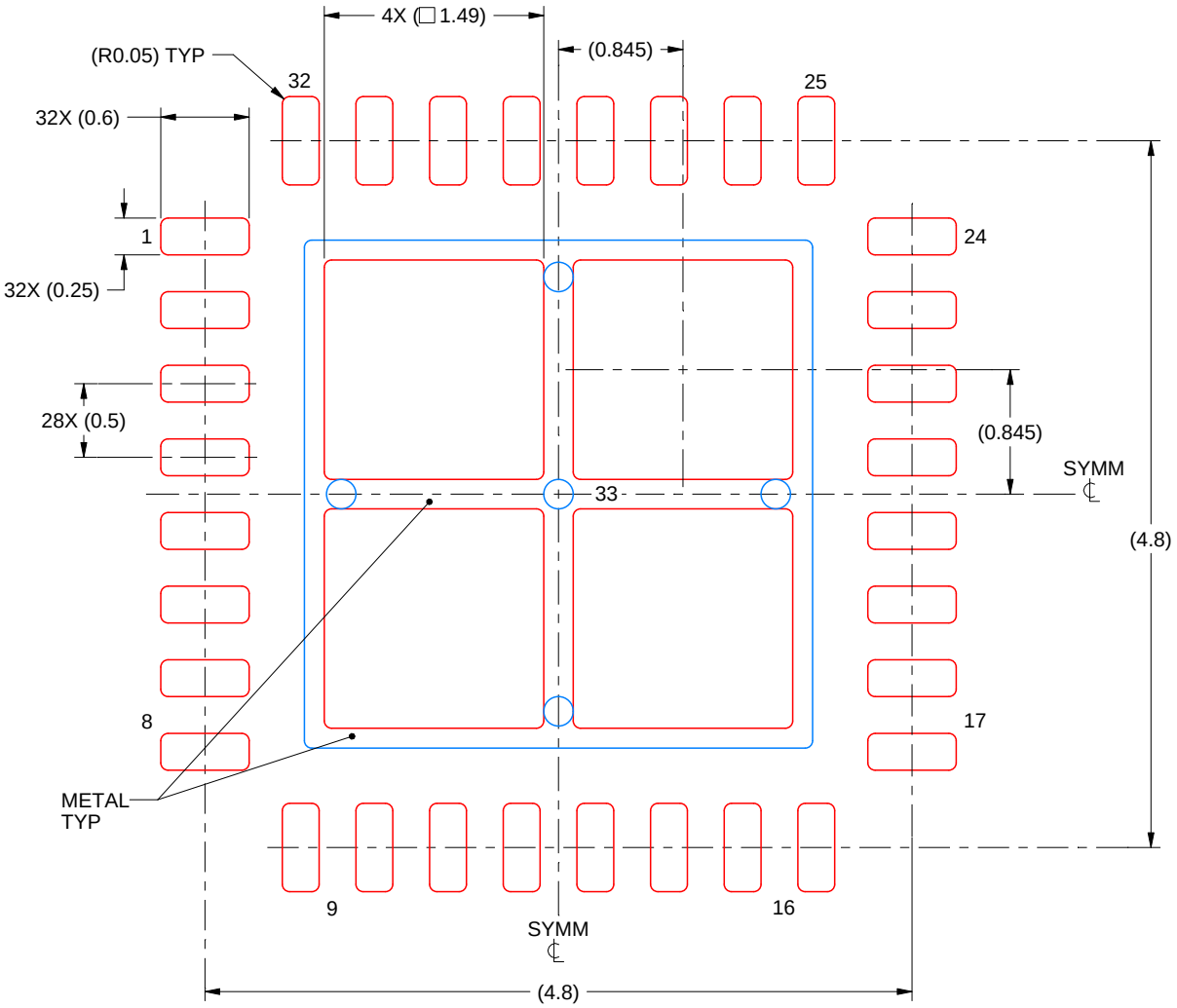
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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