TLV702-Q1 300mA、低I_Q、低ドロップアウトのレギュレータ

1 特長

- 車載アプリケーション用に認定済み
- 下記内容でAEC-Q100認定済み
  - デバイス温度グレード1: 動作時周囲温度範囲 -40℃～125℃
  - デバイスHBM ESD分類レベルH2
  - デバイスCDM ESD分類レベルC4B
- 非常に低いドロップアウト
  - I_{OUT} = 50mA、V_{OUT} = 2.8Vで37mV
  - I_{OUT} = 100mA、V_{OUT} = 2.8Vで75mV
  - I_{OUT} = 300mA、V_{OUT} = 2.8Vで220mV
- 温度範囲全体にわたって2%の精度
- 低い I_Q：35µA
- 1.2V～4.8Vの固定出力電圧の組み合わせが可能
- 高いPSRR: 1kHzにおいて68dB
- 実効容量 0.1µF で安定(1)
- サーマル・シャットダウンおよび過電流保護機能
- パッケージ: 5ピンSOT (DBVおよびDDC)および 1.5mm×1.5mm、6ピンWSON

(1) 「*アプリケーション情報*」の「*入力および出力コンデンサの要件*」を参照してください。

2 アプリケーション

- 車載用カメラ・モジュール
- 画像センサ用電源
- マイクロプロセッサ用レール
- 車載用インフォテインメントのヘッド・ユニット
- 車体用電子機器

3 概要

TLV702-Q1シリーズの低ドロップアウト(LDO)リニア・レギュレータは、低静止電流のデバイスで、ラインおよび負荷過渡性能が非常に優れています。これらのLDOは、電力の制約が厳しいアプリケーション用に設計されています。

高精度のバンドギャップおよびエラー・アンプにより、2%の総合精度を実現しています。低い出力ノイズ、非常に高い電源除去率(PSRR)、低いドロップアウト電圧から、このシリーズのデバイスは広範なバッテリ動作機器に理想的です。デバイスのすべてのバージョンには、安全のためサーマル・シャットダウンと電流制限保護が組み込まれています。

さらに、これらのデバイスはわずか0.1µFの実効出力容量で安定します。この特長により、バイアス電圧が高く温度ディレーティングが大きい、コスト効率の高いコンデンサを使用できます。これらのデバイスは、出力負荷なしでも指定の精度へのレギュレーションを行います。

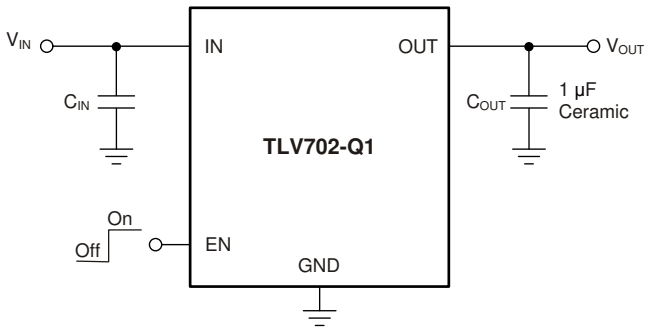
TLV702-Q1シリーズのLDOリニア・レギュレータは、SOTおよびWSONパッケージで供給されます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TLV702-Q1	SOT (5)	2.90mm×1.60mm
	WSON (6)	1.50mm×1.50mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。

代表的なアプリケーション



目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision C (January 2018) から Revision D に変更 **Page**

- Changed OUT pin number from 5 to 3 in DSE column of *Pin Functions* table ... 4
- Added footnote to maximum EN voltage specification ... 5
- Added parameter names to *Recommended Operating Conditions* table ... 5

Revision B (June 2015) から Revision C に変更 **Page**

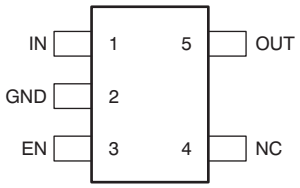
- ドキュメントにDBVパッケージを 追加 ... 1
- DBVパッケージを追加して特長の「パッケージ」箇条書きを 変更 ... 1
- Added DBV package to *Pin Configuration and Functions* section ... 4
- Added DBV column to *Thermal Information* table ... 5
- Changed title of *Layout Example for the DDC and DBV Packages* figure to include DBV package ... 16

Revision A (August 2013) から Revision B に変更 **Page**

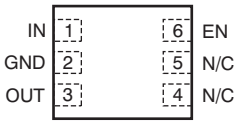
- データシートにDSE (6ピンWSON)パッケージを追加 ... 1
- 「*製品情報*」表、「*ESD定格*」表、「*推奨動作条件*」表、「*詳細説明*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションをデータシートに追加 ... 1
- データシート全体を通して、デバイスのPバージョンへの参照をすべて削除 ... 1
- 「*特長*」の箇条書きで、「2%の精度」項目に「温度範囲全体にわたって」を追加 ... 1
- データシート全体で、DDCパッケージ名をTSOT23からSOTに変更 ... 1
- 「*アプリケーション*」の箇条書きを変更 ... 1
- 「*概要*」セクションのテキストを変更 ... 1
- 「*代表的なアプリケーション*」回路のセラミック・コンデンサの単位をmFからμFに変更(誤植) ... 1
- Changed "free-air temperature" to "junction temperature" in *Absolute Maximum Ratings* condition statement ... 5
- Added T_J to T_A condition in *Electrical Characteristics* condition statement ... 6
- Changed T_A to T_J for typical values in *Electrcial Characteristics* condition statement ... 6

5 Pin Configuration and Functions

DDC and DBV Package
5-pin SOT
Top View



DSE Package
6-Pin WSON
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	DDC, DBV (SOT)	DSE (WSON)		
IN	1	1	I	Input pin. A small, 1-μF ceramic capacitor is recommended from this pin to ground to assure stability and good transient performance. See *Input and Output Capacitor Requirements* in the *Application Information* section for more details.
GND	2	2	—	Ground pin
EN	3	6	I	Enable pin. Driving EN over 0.9 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode and reduces operating current to 1 μA, nominal.
NC	4	4, 5	—	No connection. Tie this pin to ground to improve thermal dissipation.
OUT	5	3	O	Regulated output voltage pin. A small, 1-μF ceramic capacitor is needed from this pin to ground for stability. See *Input and Output Capacitor Requirements* in the *Application Information* section for more details.

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage(2)	IN	–0.3	6	V
	EN	–0.3	6(3)	V
	OUT	–0.3	6	V
Current (source)	OUT	Internally limited		A
Output short-circuit duration		Indefinite		
Temperature	Operating virtual junction, T_J	–55	150	°C
	Storage, T_{stg}	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground terminal.
(3) The absolute maximum rating is V_{IN} + 0.3 V or 6.0 V, whichever is smaller.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2		5.5	V
V_{OUT}	Output voltage	1.2		4.8	V
I_{OUT}	Output current	0		300	mA
T_A	Ambient temperature	–40		125	°C
T_J	Operating virtual junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TLV702-Q1			UNIT
		DDC (SOT)	DBV (SOT)	DSE (WSON)	
		5 PINS	5 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	262.8	249.2	321.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	68.2	136.4	207.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	81.6	85.9	281.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.1	19.5	42.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	80.9	85.3	284.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	142.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

At V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2 V (whichever is greater); I_{OUT} = 10 mA, V_{EN} = 0.9 V, C_{OUT} = 1 µF, and T_J, T_A = –40°C to +125°C, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	DC output accuracy		–2%	0.5%	2%	
$\Delta V_{O(\Delta VI)}$	Line regulation	$V_{OUT(nom)}$ + 0.5 V ≤ V_{IN} ≤ 5.5 V, I_{OUT} = 10 mA		1	5	mV
$\Delta V_{O(\Delta IO)}$	Load regulation	0 mA ≤ I_{OUT} ≤ 300 mA		1	15	mV
V_{DO}	Dropout voltage(1)	V_{IN} = 0.98 × $V_{OUT(nom)}$, I_{OUT} = 300 mA		260	375	mV
I_{CL}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(nom)}$	320	500	860	mA
I_{GND}	Ground pin current	I_{OUT} = 0 mA		35	55	µA
		I_{OUT} = 300 mA, V_{IN} = V_{OUT} + 0.5 V		370		µA
I_{SHDN}	Ground pin current (shutdown)	V_{EN} ≤ 0.4 V, V_{IN} = 2 V		400		nA
		V_{EN} ≤ 0.4 V, 2 V ≤ V_{IN} ≤ 4.5 V		1	2.5	µA
PSRR	Power-supply rejection ratio	V_{IN} = 2.3 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA, f = 1 kHz		68		dB
V_n	Output noise voltage	BW = 100 Hz to 100 kHz, V_{IN} = 2.3 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA		48		μV_{RMS}
t_{STR}	Start-up time(2)	C_{OUT} = 1 µF, I_{OUT} = 300 mA		100		µs
$V_{EN(high)}$	Enable pin high (enabled)		0.9		V_{IN}	V
$V_{EN(low)}$	Enable pin low (disabled)		0		0.4	V
I_{EN}	Enable pin current	V_{IN} = V_{EN} = 5.5 V		0.04		µA
UVLO	Undervoltage lockout	V_{IN} rising		1.9		V
T_{sd}	Thermal shutdown temperature	Shutdown, temperature increasing		165		°C
		Reset, temperature decreasing		145		°C

(1) V_{DO} is measured for devices with $V_{OUT(nom)}$ ≥ 2.35 V.
(2) Start-up time = time from EN assertion to 0.98 × $V_{OUT(nom)}$.

6.6 Typical Characteristics

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2 V, whichever is greater; I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, unless otherwise noted. Typical values are at T_J = 25°C.

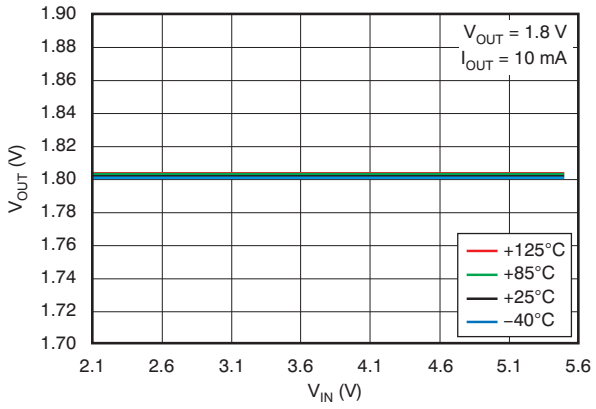


Figure 1. Line Regulation

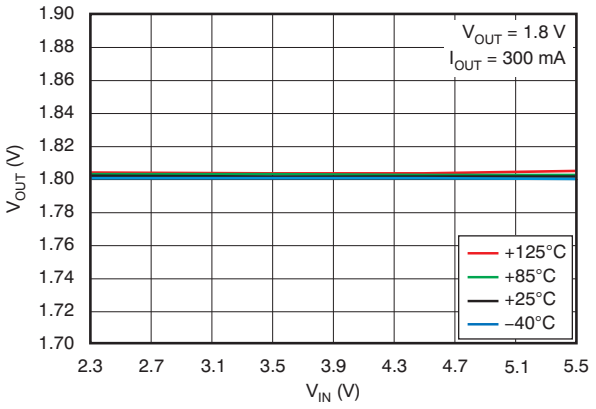


Figure 2. Line Regulation

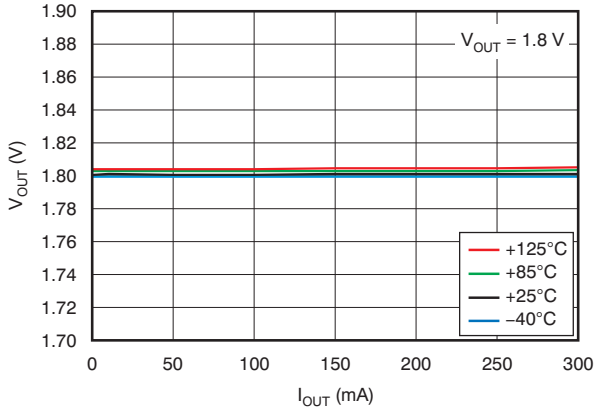


Figure 3. Load Regulation

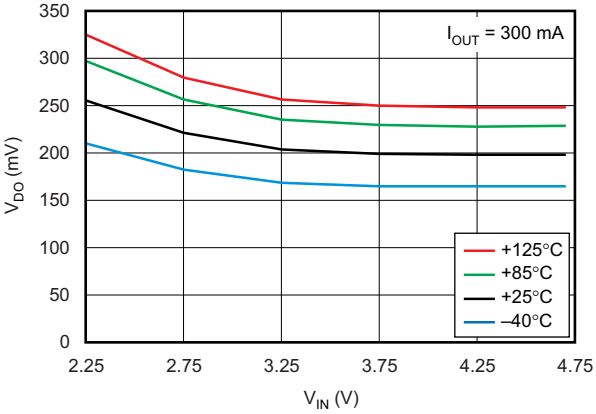


Figure 4. Dropout Voltage vs Input Voltage

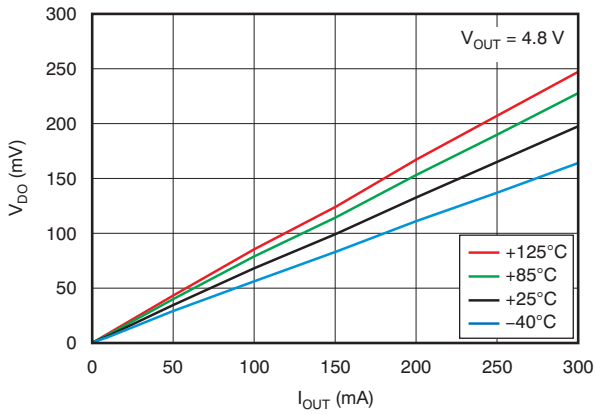


Figure 5. Dropout Voltage vs Output Current

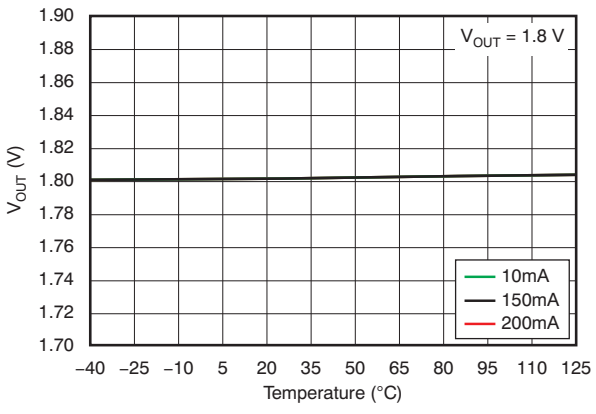


Figure 6. Output Voltage vs Temperature

Typical Characteristics (continued)

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2 V, whichever is greater; I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, unless otherwise noted. Typical values are at T_J = 25°C.

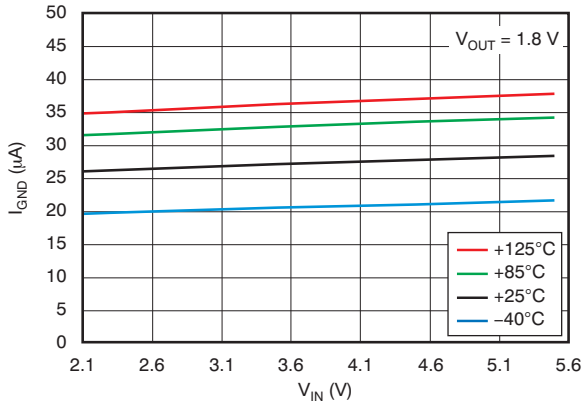


Figure 7. Ground Pin Current vs Input Voltage

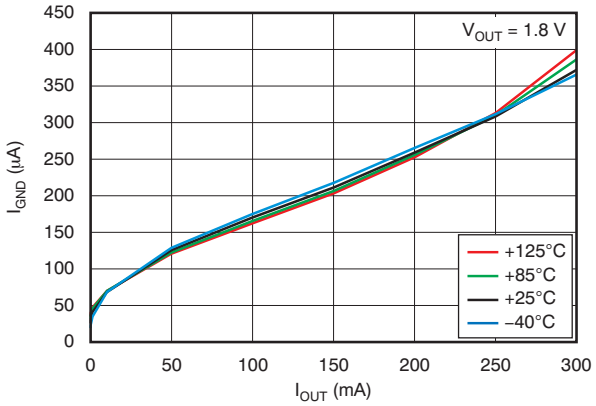


Figure 8. Ground Pin Current vs Load

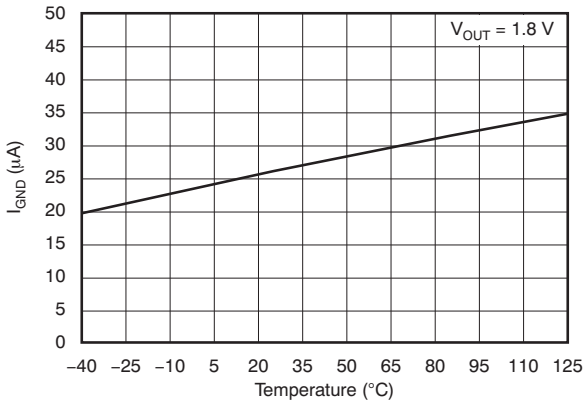


Figure 9. Ground Pin Current vs Temperature

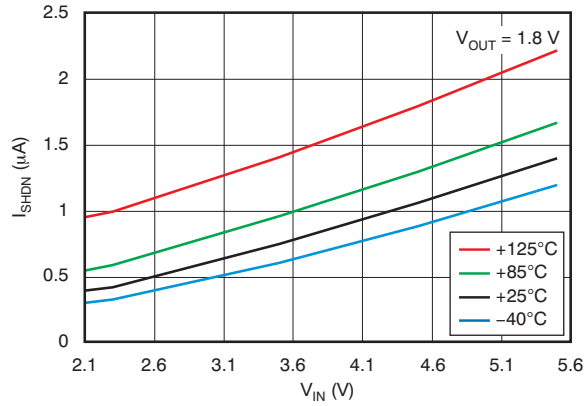


Figure 10. Shutdown Current vs Input Voltage

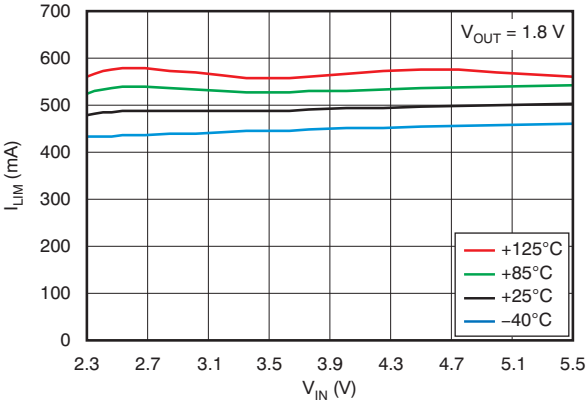


Figure 11. Current Limit vs Input Voltage

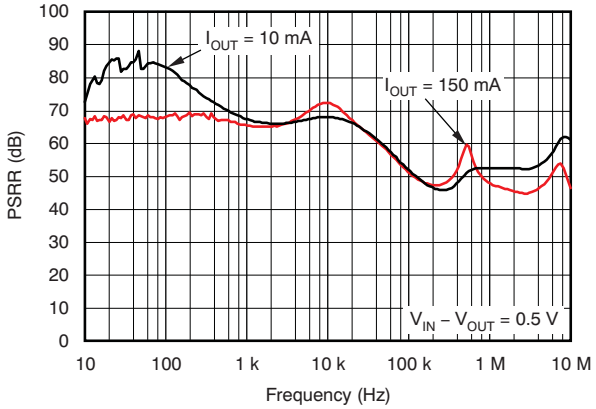


Figure 12. Power-Supply Ripple Rejection vs Frequency

Typical Characteristics (continued)

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2 V, whichever is greater; I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, unless otherwise noted. Typical values are at T_J = 25°C.

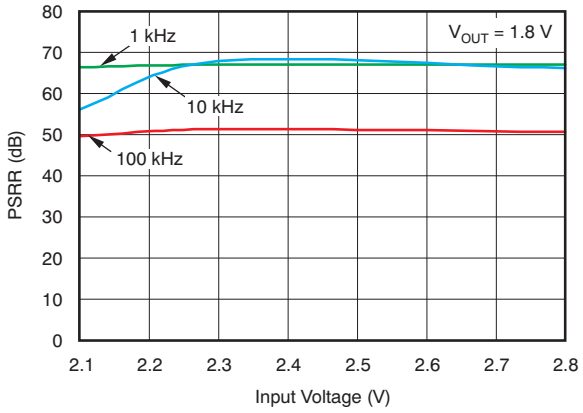


Figure 13. Power-Supply Ripple Rejection vs Input Voltage

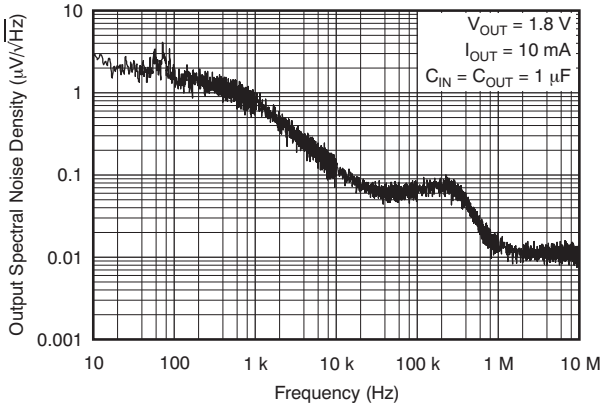


Figure 14. Output Spectral Noise Density vs Frequency

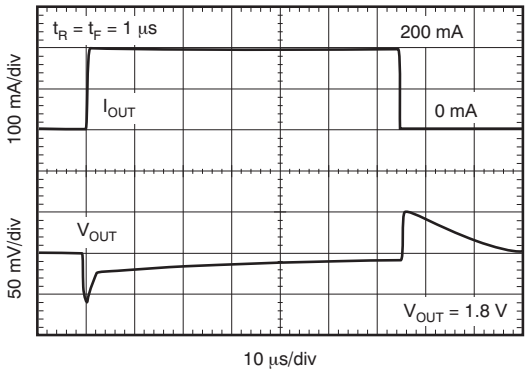


Figure 15. Load Transient Response

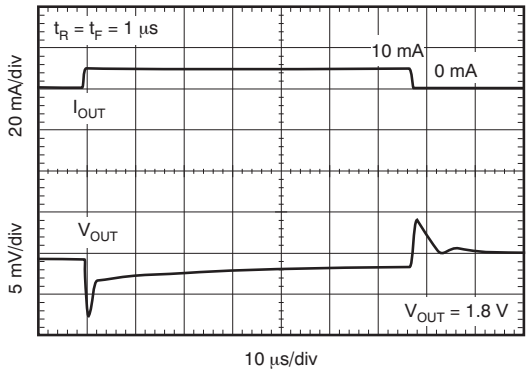


Figure 16. Load Transient Response

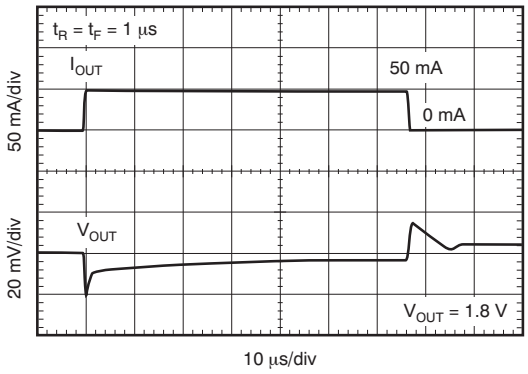


Figure 17. Load Transient Response

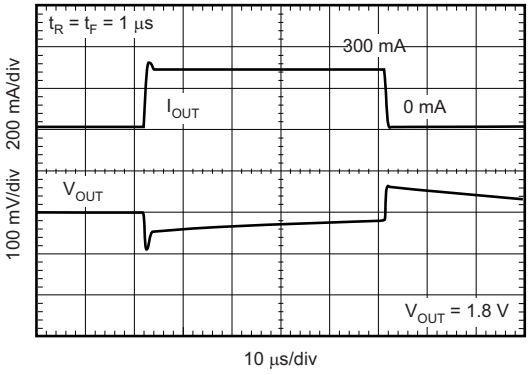


Figure 18. Load Transient Response

Typical Characteristics (continued)

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2 V, whichever is greater; I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, unless otherwise noted. Typical values are at T_J = 25°C.

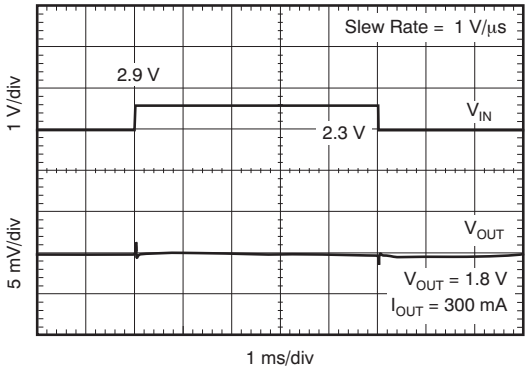


Figure 19. Line Transient Response

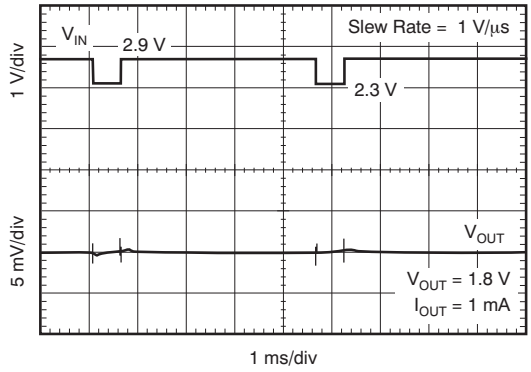


Figure 20. Line Transient Response

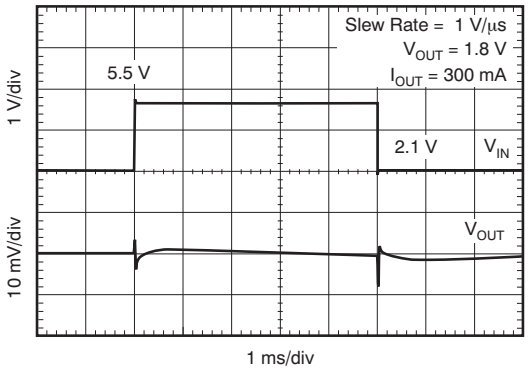


Figure 21. Line Transient Response

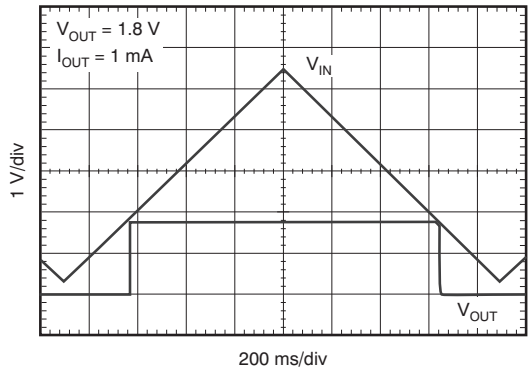


Figure 22. V_{IN} Ramp Up, Ramp Down Response

7 Detailed Description

7.1 Overview

The TLV702-Q1 series of low-dropout (LDO) linear regulators are low quiescent current devices with excellent line and load transient performance. These LDOs are designed for power-sensitive applications. A precision bandgap and error amplifier provides overall 2% accuracy. Low output noise, very high power-supply rejection ratio (PSRR), and low dropout voltage make this series of devices ideal for most battery-operated handheld equipment. All device versions have integrated thermal shutdown, current limit, and undervoltage lockout (UVLO) protections.

7.2 Functional Block Diagrams

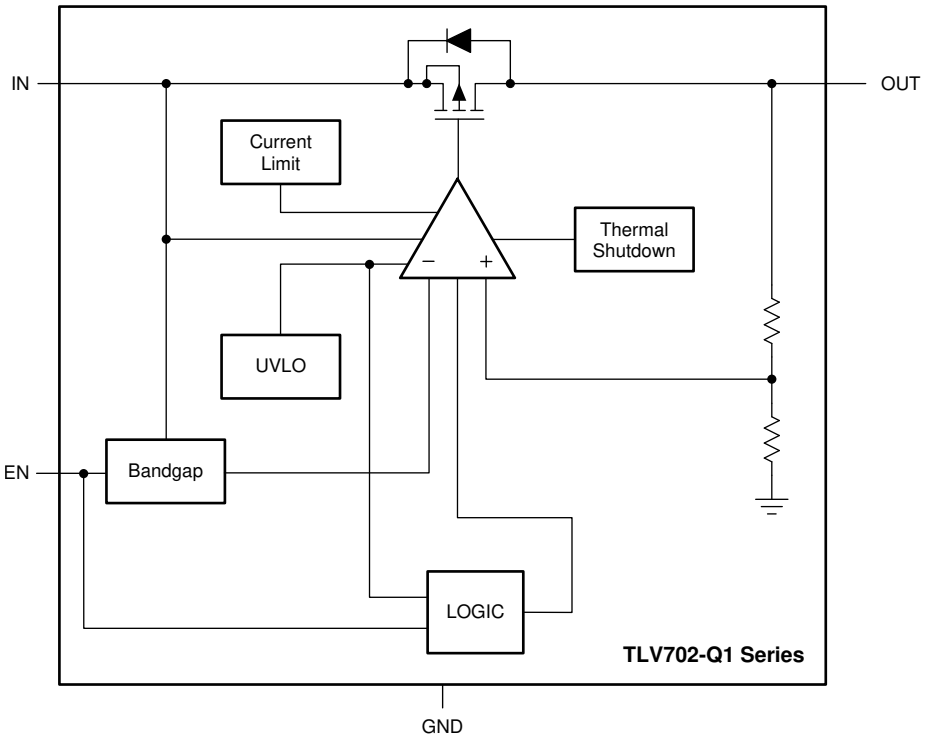


Figure 23. TLV702-Q1 Block Diagram

7.3 Feature Description

7.3.1 Internal Current Limit

The TLV702-Q1 internal current limit protection helps to protect the regulator during fault conditions. During current limit operation, the output sources a fixed amount of current that is largely independent of the output voltage. In such a case, the output voltage is not regulated, and is $V_{OUT} = I_{CL} \times R_{LOAD}$. The PMOS pass transistor dissipates $(V_{IN} – V_{OUT}) \times I_{CL}$ until thermal shutdown is triggered and the device turns off. As the device cools, the device is turned on by the internal thermal shutdown circuit. If the fault condition continues, the device cycles between current limit operation and thermal shutdown. See *Thermal Consideration* for more details.

The PMOS pass element in the TLV702-Q1 has a built-in body diode that conducts current when the voltage at the OUT pin exceeds the voltage at IN. This current is not limited; if extended reverse-voltage operation is anticipated, externally limit the output current to 5% of the rated I_{OUT} specification.

Feature Description (continued)

7.3.2 Shutdown

The enable pin (EN) is active high. The device is enabled when voltage at EN pin exceeds 0.9 V. The device is turned off when the EN pin is held at less than 0.4 V. When shutdown capability is not required, connect the EN pin to the IN pin.

7.3.3 Dropout Voltage

The TLV702-Q1 uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear (triode) region of operation. The input-to-output resistance is equal to the drain-source on-state resistance ($R_{DS(on)}$) of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves as a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded as (V_{IN} – V_{OUT}) approaches dropout. This effect is shown in Figure 13.

7.3.4 Undervoltage Lockout

The TLV702-Q1 uses a UVLO circuit to keep the output shut off until internal circuitry is operating properly.

7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The output current is less than the current limit.
- The input voltage is greater than the UVLO voltage.

7.4.2 Dropout Operation

If the input voltage is less than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this condition, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device is in a triode state and no longer regulates the output voltage of the LDO. Line or load transients in dropout may result in large output voltage deviations.

Table 1 lists the conditions that lead to the different modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER	
	V_{IN}	I_{OUT}
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{DO}$	$I_{OUT} < I_{CL}$
Dropout mode	$V_{IN} < V_{OUT(nom)} + V_{DO}$	$I_{OUT} < I_{CL}$
Current limit	$V_{IN} >$ UVLO	$I_{OUT} > I_{CL}$

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV702-Q1 belongs to a new family of next-generation value LDO regulators. These devices consume low quiescent current and deliver excellent line and load transient performance. These characteristics, combined with low noise and very good PSRR with little (V_{IN} – V_{OUT}) headroom, make this family of devices ideal for portable RF applications. This family of regulators offers current limit and thermal protection, and is specified from –40°C to +125°C.

8.2 Typical Application

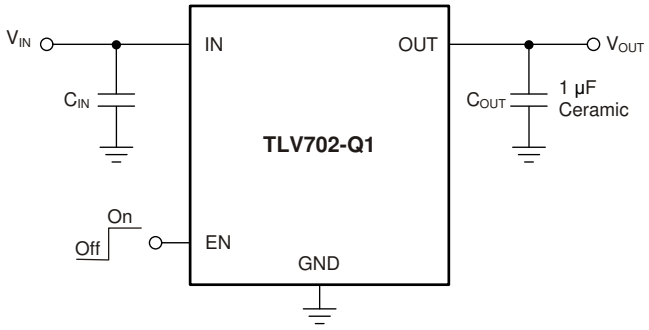


Figure 24. Typical Application Circuit

8.2.1 Design Requirements

Table 2 lists the design parameters.

Table 2. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	2.5 V to 3.3 V
Output voltage	1.8 V
Output current	100 mA

8.2.2 Detailed Design Procedure

8.2.2.1 Input and Output Capacitor Requirements

1-μF X5R- and X7R-type ceramic capacitors are recommended because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature.

However, the TLV702-Q1 is designed to be stable with an *effective capacitance* of 0.1 μF or larger at the output. Thus, the device is stable with capacitors of other dielectric types as well, as long as the effective capacitance under operating bias voltage and temperature is greater than 0.1 μF. This effective capacitance refers to the capacitance that the LDO sees under operating bias voltage and temperature conditions; that is, the capacitance after taking both bias voltage and temperature derating into consideration. In addition to allowing the use of lower-cost dielectrics, this capability of being stable with 0.1-μF effective capacitance also enables the use of smaller footprint capacitors that have higher derating in size- and space-constrained applications.

Using a 0.1-μF rated capacitor at the output of the LDO does not ensure stability because the effective capacitance under the specified operating conditions must not be less than 0.1 μF. Maximum ESR should be less than 200 mΩ.

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1-μF to 1-μF, low ESR capacitor across the IN pin and GND pin of the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located close to the power source. If source impedance is more than 2 Ω, a 0.1-μF input capacitor may be necessary for stability.

8.2.2.2 Transient Response

As with any regulator, increasing the size of the output capacitor reduces overshoot and undershoot magnitude, but increases the duration of the transient response.

8.2.3 Application Curves

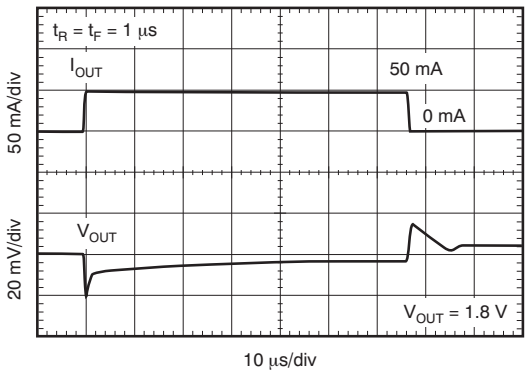


Figure 25. Load Transient Response

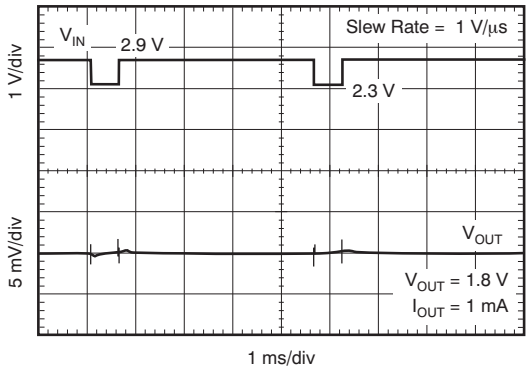


Figure 26. Line Transient Response

9 Power Supply Recommendations

Connect a low output impedance power supply directly to the IN pin of the TLV702-Q1. Inductive impedances between the input supply and the IN pin can create significant voltage excursions at the IN pin during start-up or load transient events.

9.1 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed-circuit-board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air.

Refer to *Thermal Information* for thermal performance on the TLV702-Q1 evaluation module (EVM). The EVM is a two-layer board with two ounces of copper per side.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current and the voltage drop across the output pass element, as shown in Equation 1.

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (1)$$

10 Layout

10.1 Layout Guidelines

Place the input and output capacitors as close to the device pins as possible. To improve ac performance such as PSRR, output noise, and transient response, design the board with separate ground planes for V_{IN} and V_{OUT}, with the ground plane connected only at the GND pin of the device. In addition, connect the ground connection for the output capacitor directly to the GND pin of the device. High-ESR capacitors may degrade PSRR performance.

10.1.1 Thermal Consideration

Thermal protection disables the output when the junction temperature rises to approximately 165°C, allowing the device to cool. When the junction temperature cools to approximately 145°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, limit junction temperature to 125°C maximum.

To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

The internal protection circuitry of the TLV702-Q1 is designed to protect against overload conditions but is not intended to replace proper heatsinking. Continuously running the TLV702-Q1 into thermal shutdown degrades device reliability.

Layout Guidelines (continued)

10.1.2 Package Mounting

Solder pad footprint recommendations for the TLV702-Q1 are available from the TI website at www.ti.com. The recommended layout examples for the DDC and DSE packages are shown in Figure 27 and Figure 28, respectively.

10.2 Layout Examples

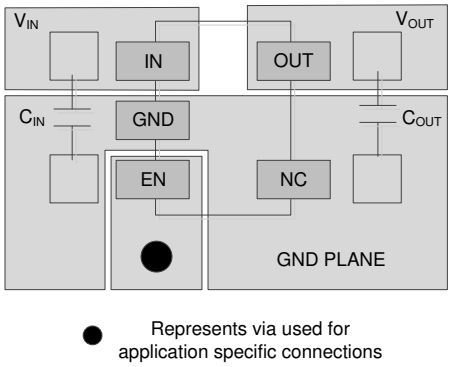


Figure 27. Layout Example for the DDC and DBV Packages

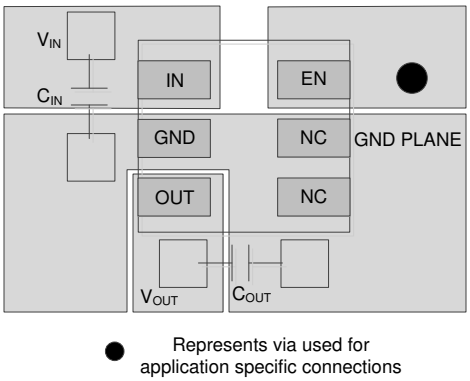


Figure 28. Layout Example for the DSE Package

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 開発サポート

11.1.1.1 SPICEモデル

SPICEを使用した回路パフォーマンスのコンピュータによるシミュレーションは、アナログ回路やシステムのパフォーマンスを分析するため多くの場合に有用です。TLV702用のSPICEモデルは、製品フォルダの「ツールとソフトウェア」から入手できます。

11.1.2 デバイスの項目表記

表 3. 製品情報(1)

製品名	V_{OUT} (2)
TLV702**xx** ***yyyz***	**XX**は公称出力電圧です(例: 28 =2.8V)。 **YYY**はパッケージ指定子です。 **Z**はテープ・アンド・リール数量です(R = 3,000、T = 250)。

(1) 最新のパッケージおよび注文情報については、このドキュメントの最後にあるパッケージ・オプションの付録を参照するか、www.ti.comのデバイス製品フォルダをご覧ください。
(2) 出力電圧は、1.2Vから4.8Vまで、50mV刻みで利用できます。詳細と在庫については、工場にお問い合わせください。

11.2 ドキュメントのサポート

11.2.1 関連資料

関連資料については、以下を参照してください。

テキサス・インスツルメンツ、*『Using the TLV700xxEVM-503』ユーザー・ガイド* (英語)

11.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 商標

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV702125QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1M57	Samples
TLV70212QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1B5H	Samples
TLV70212QDSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	H9	Samples
TLV70213QDSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	H8	Samples
TLV70215QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1B6H	Samples
TLV70215QDSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	HB	Samples
TLV70218QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1B7H	Samples
TLV70218QDSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	HC	Samples
TLV70225QDSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	G7	Samples
TLV70227QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1B8H	Samples
TLV70227QDSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	H7	Samples
TLV70228QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1B9H	Samples
TLV70228QDDCRQ1	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SJV	Samples
TLV70228QDSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HD	Samples
TLV70229QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1BAH	Samples
TLV70229QDSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	H1	Samples
TLV70230QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1MQ7	Samples
TLV70230QDSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	HE	Samples
TLV70231QDSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	HF	Samples
TLV70232QDSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	HG	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV70233QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1BBH	Samples
TLV70233QDSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	H2	Samples
TLV70236QDSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	H3	Samples
TLV70245QDSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	HH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

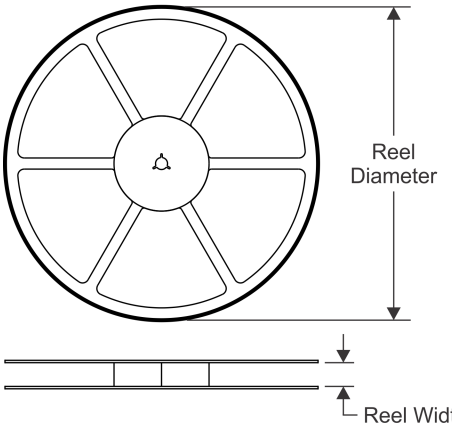
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

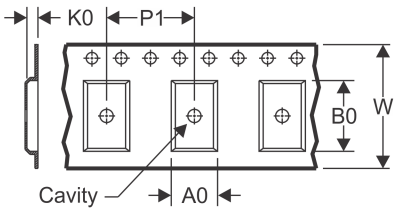
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

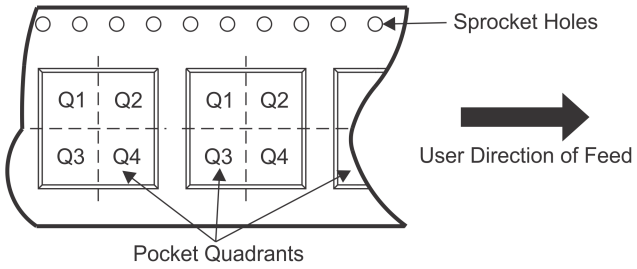


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

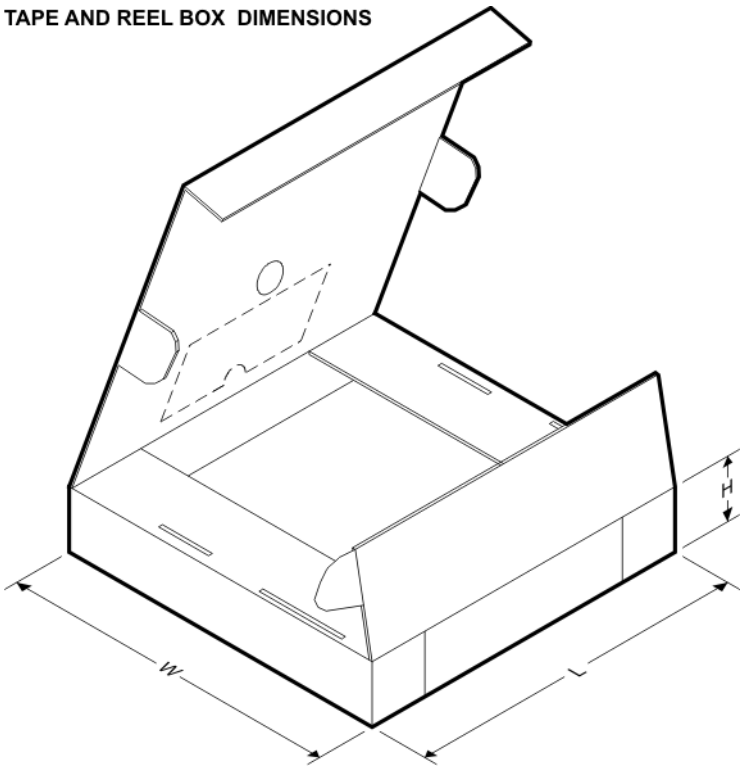


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV702125QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70212QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70212QDSERQ1	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70213QDSERQ1	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70215QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70215QDSERQ1	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70218QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70218QDSERQ1	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70225QDSERQ1	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70227QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70227QDSERQ1	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70228QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70228QDDCRQ1	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70228QDSERQ1	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70229QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70229QDSERQ1	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70230QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV70230QDSERQ1	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70231QDSERQ1	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70232QDSERQ1	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70233QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70233QDSERQ1	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70236QDSERQ1	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70245QDSERQ1	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV702125QDBVRQ1	SOT-23	DBV	5	3000	183.0	183.0	20.0
TLV70212QDBVRQ1	SOT-23	DBV	5	3000	183.0	183.0	20.0
TLV70212QDSERQ1	WSON	DSE	6	3000	200.0	183.0	25.0
TLV70213QDSERQ1	WSON	DSE	6	3000	200.0	183.0	25.0
TLV70215QDBVRQ1	SOT-23	DBV	5	3000	183.0	183.0	20.0
TLV70215QDSERQ1	WSON	DSE	6	3000	200.0	183.0	25.0
TLV70218QDBVRQ1	SOT-23	DBV	5	3000	183.0	183.0	20.0
TLV70218QDSERQ1	WSON	DSE	6	3000	200.0	183.0	25.0
TLV70225QDSERQ1	WSON	DSE	6	3000	200.0	183.0	25.0
TLV70227QDBVRQ1	SOT-23	DBV	5	3000	183.0	183.0	20.0

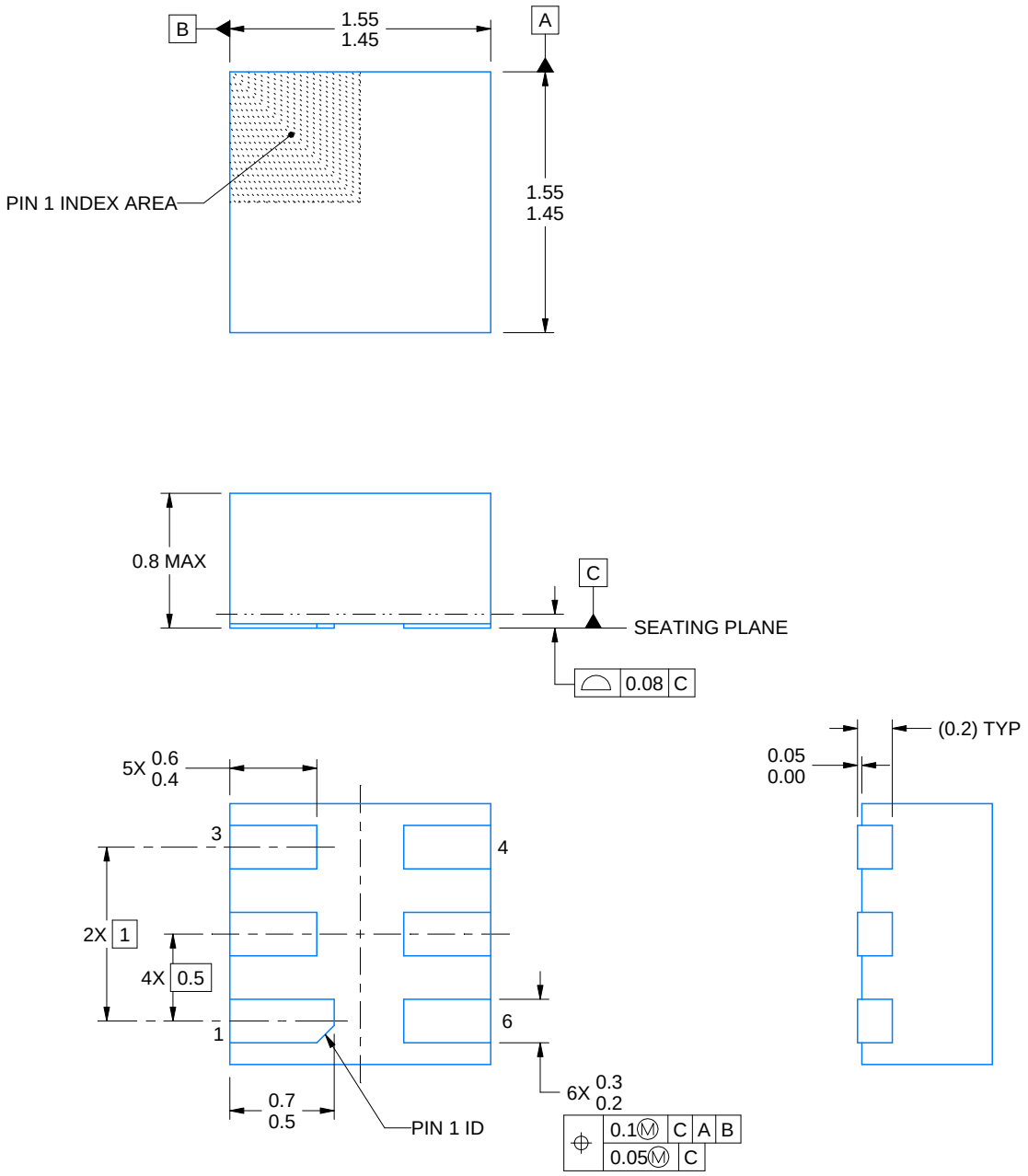
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV70227QDSERQ1	WSON	DSE	6	3000	200.0	183.0	25.0
TLV70228QDBVRQ1	SOT-23	DBV	5	3000	183.0	183.0	20.0
TLV70228QDDCRQ1	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
TLV70228QDSERQ1	WSON	DSE	6	3000	200.0	183.0	25.0
TLV70229QDBVRQ1	SOT-23	DBV	5	3000	183.0	183.0	20.0
TLV70229QDSERQ1	WSON	DSE	6	3000	200.0	183.0	25.0
TLV70230QDBVRQ1	SOT-23	DBV	5	3000	183.0	183.0	20.0
TLV70230QDSERQ1	WSON	DSE	6	3000	200.0	183.0	25.0
TLV70231QDSERQ1	WSON	DSE	6	3000	200.0	183.0	25.0
TLV70232QDSERQ1	WSON	DSE	6	3000	200.0	183.0	25.0
TLV70233QDBVRQ1	SOT-23	DBV	5	3000	183.0	183.0	20.0
TLV70233QDSERQ1	WSON	DSE	6	3000	200.0	183.0	25.0
TLV70236QDSERQ1	WSON	DSE	6	3000	200.0	183.0	25.0
TLV70245QDSERQ1	WSON	DSE	6	3000	200.0	183.0	25.0

DSE0006A

PACKAGE OUTLINE

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4220552/B 01/2024

NOTES:

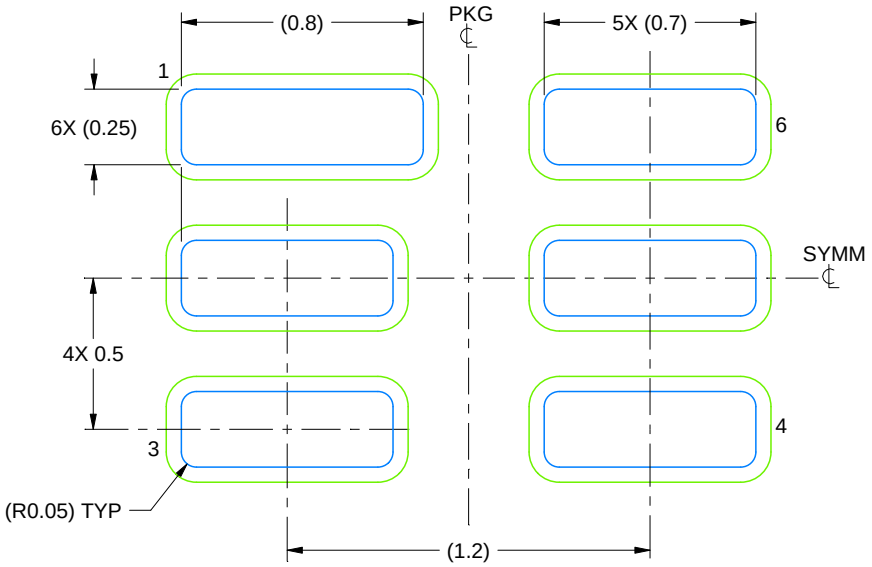
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

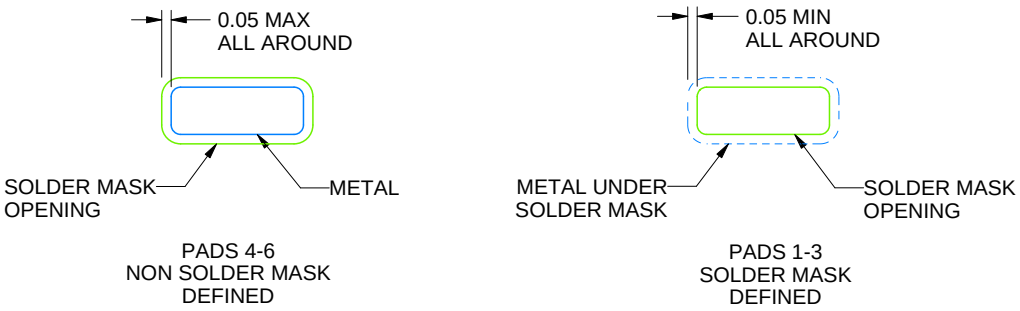
DSE0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS

4220552/B 01/2024

NOTES: (continued)

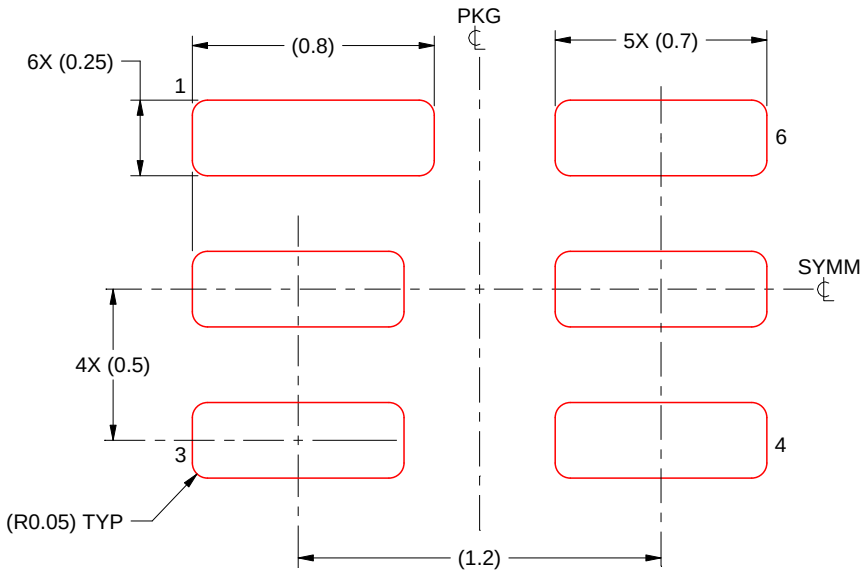
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSE0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:40X

NOTES: (continued)

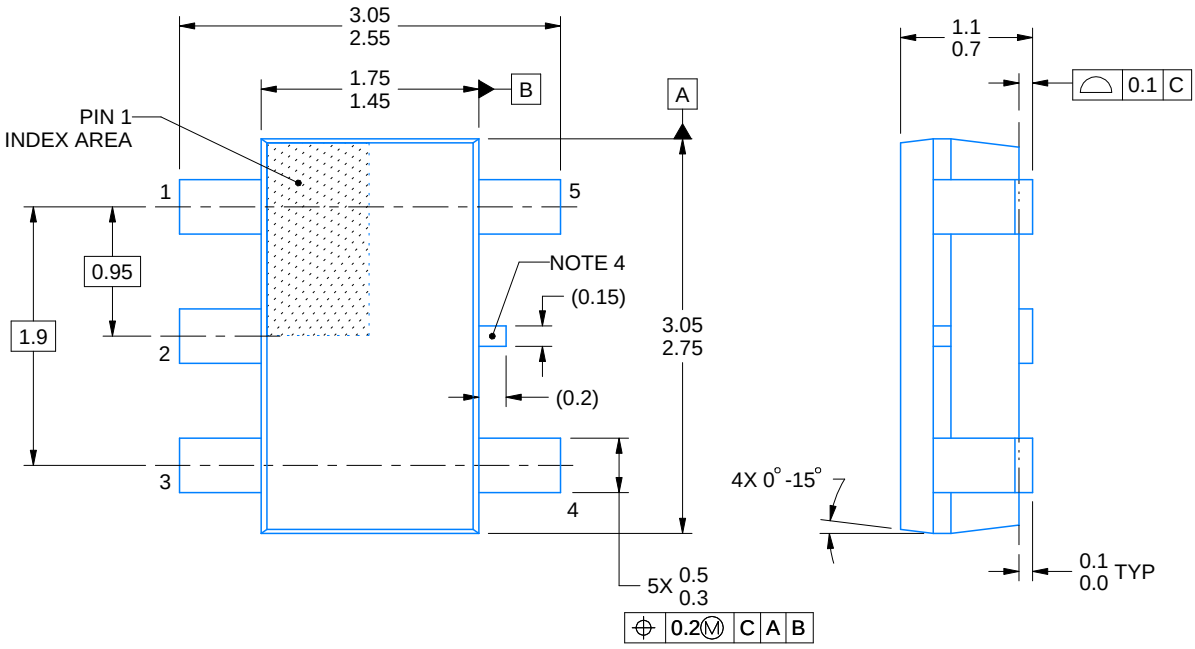
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

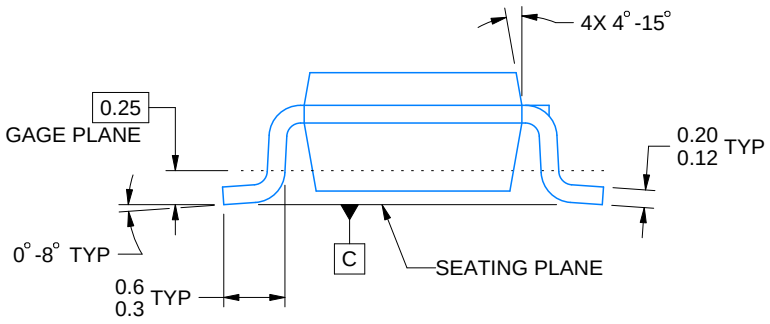
PACKAGE OUTLINE

DDC0005A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR

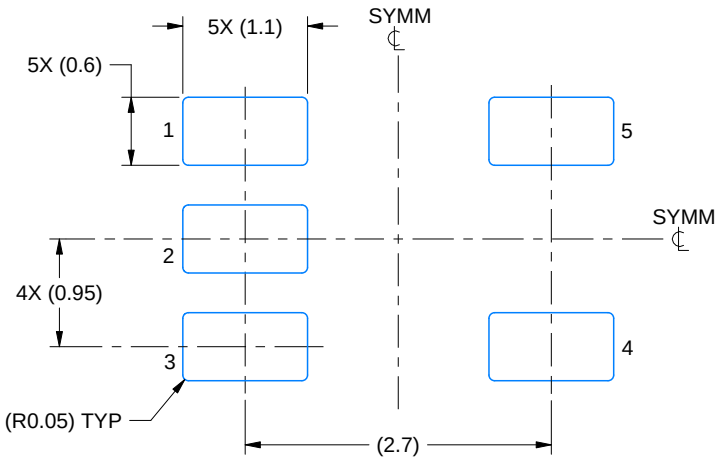




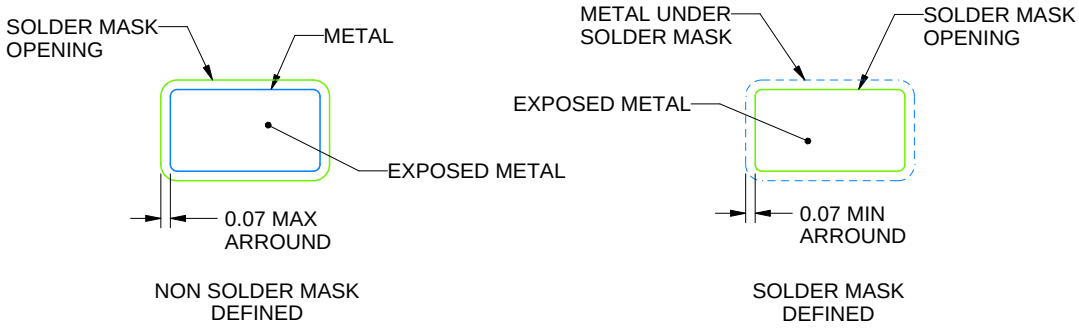
4220752/C 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.
4. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X

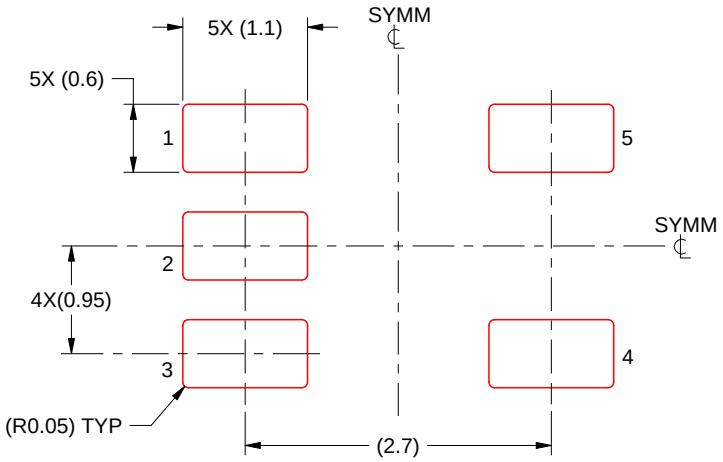


SOLDERMASK DETAILS

4220752/C 08/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4220752/C 08/2024

NOTES: (continued)

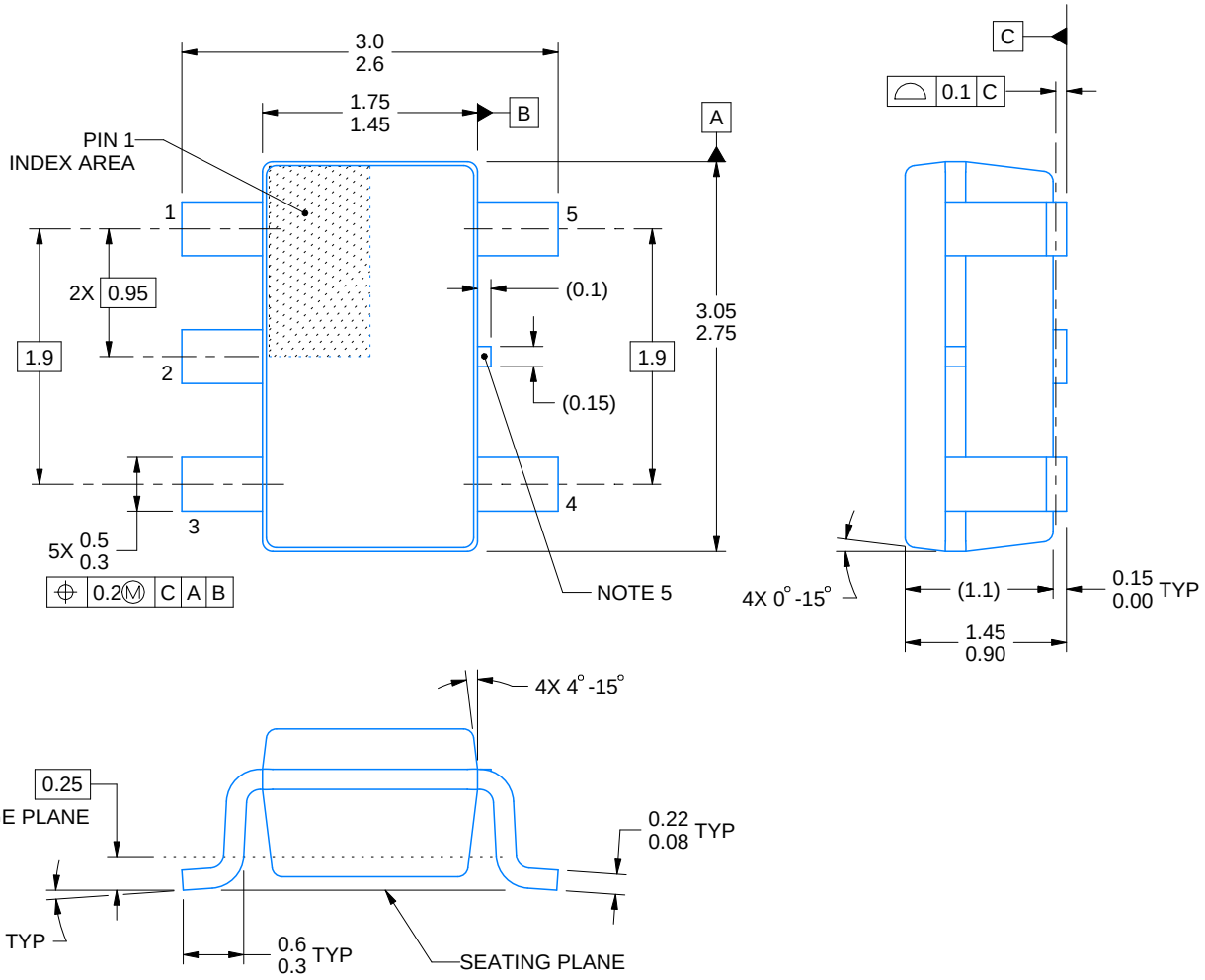
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

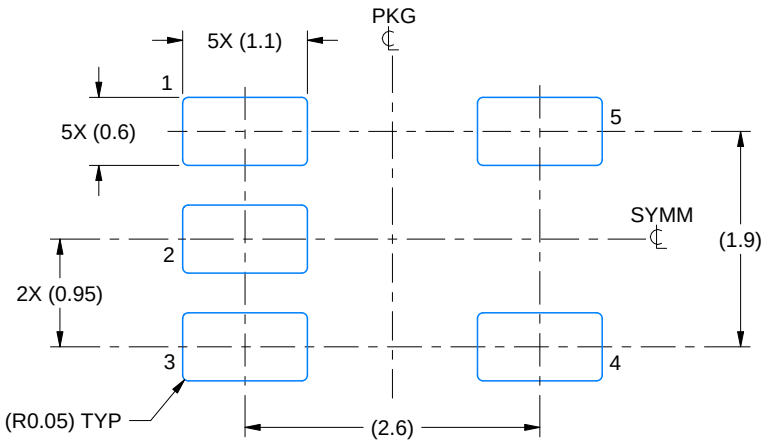
SMALL OUTLINE TRANSISTOR



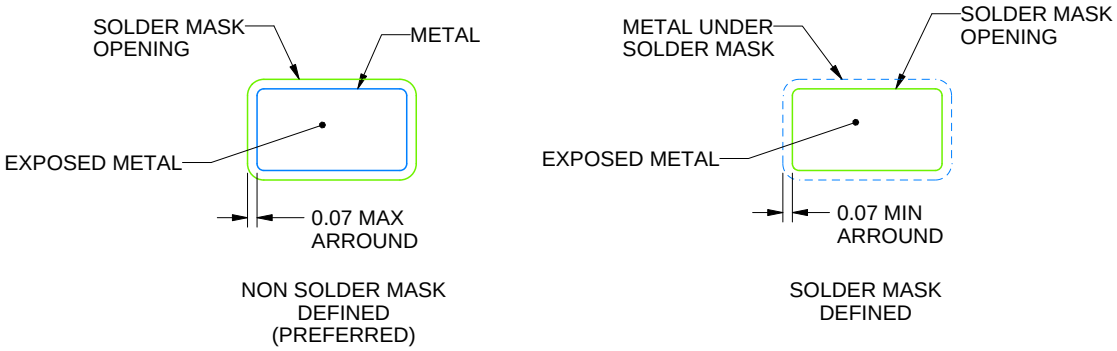
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

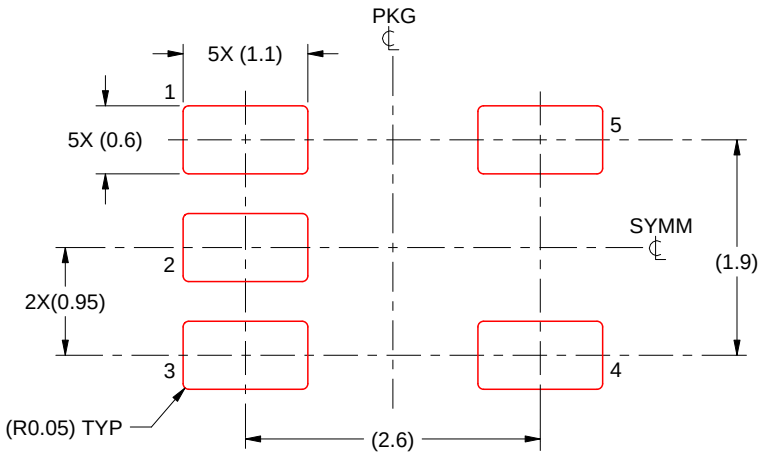


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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