

TLV742P 200mA小型低ドロップアウト・リニア電圧レギュレータ

1 特長

- 入力電圧範囲: 2V~5.5V
- 固定出力電圧: 50mV刻みで0.85V~5V⁽¹⁾
- 精度: 標準値0.5%
- 高PSRR:
 - 1MHz時に55dB
- イネーブル時 I_Q : 25 μ A
- ディセーブル時 I_Q : 1 μ A
- アクティブ出力放電
- サーマル・シャットダウンおよび過電流保護機能
- パッケージ:
 - 1mm \times 1mm DQN (X2SON)

2 アプリケーション

- POS
- カメラおよびマシン・ビジョン・モジュール
- ゲームおよび玩具
- ビル・オートメーションおよびビデオ監視
- テレビおよびセットトップ・ボックス

3 概要

TLV742P低ドロップアウト(LDO)リニア電圧レギュレータは、広い出力電圧範囲のサポートにより、優れた性能を実現しています。LDOは、シングルセル・リチウムイオン・バッテリーの入出力電圧を0.85Vまで直接調整できます。DC-DCコンバータ出力のポストレギュレーションに使用すれば、1MHz時55dBという高いPSRRでリップルを抑制し、安定した低ノイズのよく調整された V_{OUT} を実現します。

TLV742Pはアクティブ出力放電機能を備えているため、システムがディセーブル、スタンバイ・モード、またはスリープ・モードの場合に出力を低い状態に維持することができます。また、過電流保護機能により出力短絡時にデバイスを保護し、サーマル・シャットダウンによって過熱を防止します。

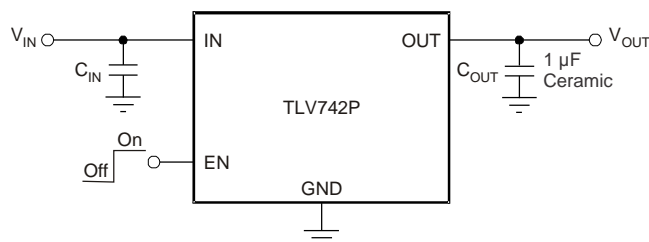
TLV742P電圧レギュレータは1mm \times 1mmのX2SONパッケージで供給されているため、PCB面積を最小限に抑えることができます。

製品情報⁽¹⁾

型番	パッケージ	本体サイズ(公称)
TLV742P	X2SON (4)	1.00mm \times 1.00mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

代表的なアプリケーション回路



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目次

1	特長	1	8	Application and Implementation	15
2	アプリケーション	1	8.1	Application Information.....	15
3	概要	1	8.2	Typical Application	15
4	改訂履歴	2	8.3	Do's and Don'ts.....	18
5	Pin Configuration and Functions	3	9	Power Supply Recommendations	19
6	Specifications	4	10	Layout	19
6.1	Absolute Maximum Ratings	4	10.1	Layout Guidelines	19
6.2	ESD Ratings.....	4	10.2	Layout Example	20
6.3	Recommended Operating Conditions.....	4	10.3	Thermal Considerations	20
6.4	Thermal Information	4	10.4	Power Dissipation	20
6.5	Electrical Characteristics.....	5	11	デバイスおよびドキュメントのサポート	21
6.6	Typical Characteristics	6	11.1	デバイス・サポート	21
7	Detailed Description	13	11.2	ドキュメントの更新通知を受け取る方法.....	21
7.1	Overview	13	11.3	コミュニティ・リソース	21
7.2	Functional Block Diagrams	13	11.4	商標	21
7.3	Feature Description.....	13	11.5	静電気放電に関する注意事項	21
7.4	Device Functional Modes.....	14	11.6	Glossary	21
			12	メカニカル、パッケージ、および注文情報	22

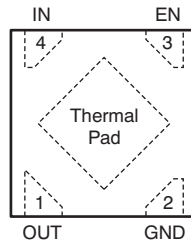
4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

日付	改訂内容	注
2017年9月	*	初版

5 Pin Configuration and Functions

DQN Package
4-Pin X2SON With Exposed Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	3	I	Enable pin. Driving EN over 0.9 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode. For TLV742P, output voltage is discharged through an internal 120-Ω resistor when device is shut down.
GND	2	—	Ground pin
IN	4	I	Input pin. For good transient performance, place a small 1-μF ceramic capacitor from this pin to ground. See Input and Output Capacitor Requirements for more details.
OUT	1	O	Regulated output voltage pin. A small 1-μF ceramic capacitor is required from this pin to ground to ensure stability. See Input and Output Capacitor Requirements for more details.
Thermal pad	—	—	The thermal pad is electrically connected to the GND node. Connect to the GND plane for improved thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Voltage ⁽²⁾	IN	-0.3	6	V
	EN	-0.3	6	V
	OUT	-0.3	6	V
Current (source)	OUT	Internally limited		
Output short-circuit duration		Indefinite		
Operating junction, T _J		-55	150	°C
Storage, T _{stg}		-55	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to GND pin.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human body model (HBM) QSS 009-105 (JESD22-A114A) ⁽¹⁾	±2000	V
	Charged device model (CDM) QSS 009-147 (JESD22-C101B.01) ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{IN}	Input voltage	2		5.5	V
I _{OUT}	Output current	0		200	mA
T _J	Operating junction temperature range	-40		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TLV742P	UNIT
		DQN (X2SON)	
		4 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	180.4	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	152	°C/W
R _{θJB}	Junction-to-board thermal resistance	117.2	°C/W
ψ _{JT}	Junction-to-top characterization parameter	5.1	°C/W
ψ _{JB}	Junction-to-board characterization parameter	117	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	99.7	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

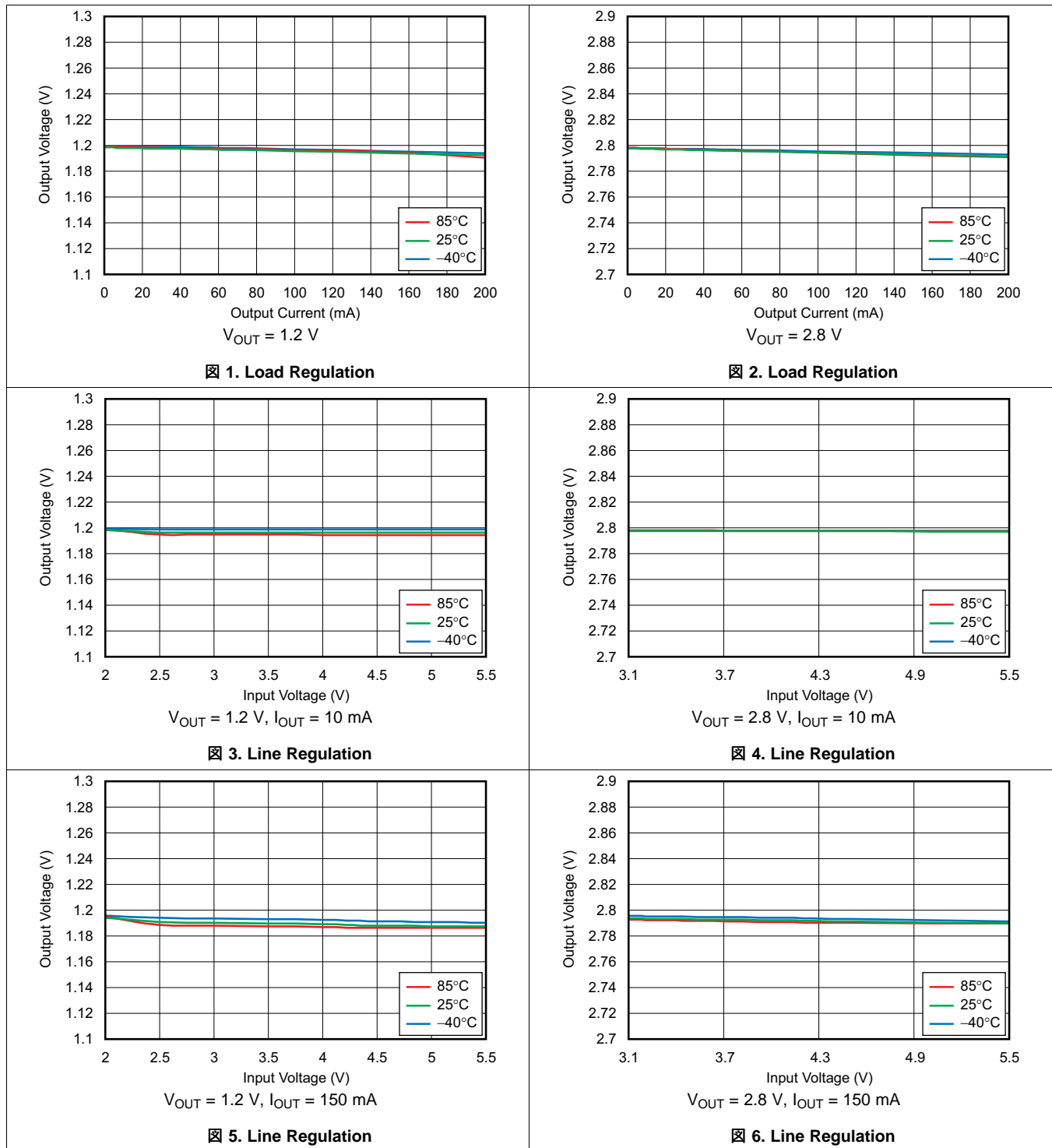
at $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$ or 2 V (whichever is greater); $I_{OUT} = 1\text{ mA}$, $V_{EN} = V_{IN}$, $C_{OUT} = 0.47\text{ }\mu\text{F}$, and $T_J = -40^\circ\text{C}$ to $+85^\circ\text{C}$. Typical values are at $T_J = 25^\circ\text{C}$, (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range			2		5.5	V
V_{OUT}	Output voltage range			0.85		5	V
	DC output accuracy	$V_{OUT} \geq 0.85\text{ V}$			0.5%		
$\Delta V_{O(\Delta V)}$	Line regulation				1	5	mV
$\Delta V_{O(\Delta I)}$	Load regulation	$0\text{ mA} \leq I_{OUT} \leq 150\text{ mA}$			10	20	mV
$V_{(DO)}$	Dropout voltage	$V_{IN} = 0.98 \times V_{OUT(NOM)}$	$2\text{ V} < V_{OUT} \leq 2.4\text{ V}$	$I_{OUT} = 30\text{ mA}$	65		mV
				$I_{OUT} = 150\text{ mA}$	325	360	mV
			$2.4\text{ V} < V_{OUT} \leq 2.8\text{ V}$	$I_{OUT} = 30\text{ mA}$	50		mV
				$I_{OUT} = 150\text{ mA}$	250	300	mV
			$2.8\text{ V} < V_{OUT} \leq 3.3\text{ V}$	$I_{OUT} = 30\text{ mA}$	45		mV
				$I_{OUT} = 150\text{ mA}$	220	270	mV
$3.3\text{ V} < V_{OUT} \leq 5\text{ V}$	$I_{OUT} = 30\text{ mA}$	40		mV			
	$I_{OUT} = 150\text{ mA}$	200	250	mV			
I_{CL}	Output current limit	$V_{OUT} = 0.9 \times V_{OUT(NOM)}$		240	300	450	mA
$I_{(GND)}$	Ground pin current	$I_{OUT} = 0\text{ mA}$			25	50	μA
$I_{(EN)}$	EN pin current	$V_{EN} = 5.5\text{ V}$			0.01		μA
$I_{SHUTDOWN}$	Shutdown current	$V_{EN} \leq 0.4\text{ V}$ $2\text{ V} \leq V_{IN} \leq 4.5\text{ V}$			1		μA
$V_{IL(EN)}$	EN pin low-level input voltage (disable device)			0		0.4	V
$V_{IH(EN)}$	EN pin high-level input voltage (enable device)			0.9		V_{IN}	V
PSRR	Power-supply rejection ratio	$V_{IN} = 3.3\text{ V}$ $V_{OUT} = 2.8\text{ V}$ $I_{OUT} = 30\text{ mA}$	$f = 100\text{ Hz}$		70		dB
			$f = 10\text{ kHz}$		55		
			$f = 1\text{ MHz}$		55		
V_n	Output noise voltage	BW = 100 Hz to 100 kHz, $V_{IN} = 2.3\text{ V}$ $V_{OUT} = 1.8\text{ V}$ $I_{OUT} = 10\text{ mA}$			45		μV_{RMS}
t_{STR}	Startup time ⁽¹⁾	$C_{OUT} = 1\text{ }\mu\text{F}$ $I_{OUT} = 150\text{ mA}$			100		μs
$R_{PULLDOWN}$	Pulldown resistance (TLV742P only)				120		Ω
T_J	Operating junction temperature			-40		125	$^\circ\text{C}$

(1) Start-up time = time from EN assertion to $0.98 \times V_{OUT}$.

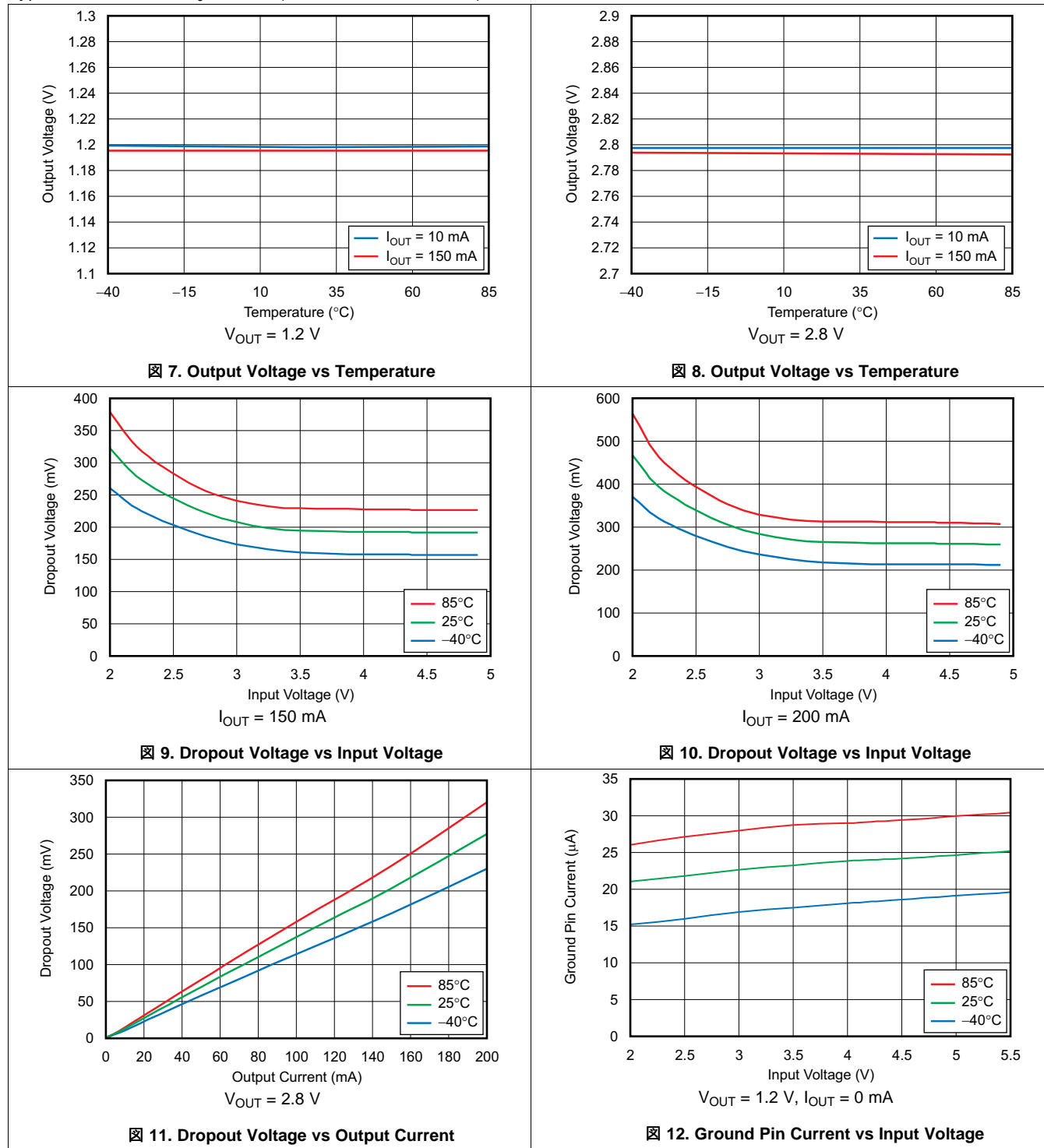
6.6 Typical Characteristics

at $T_J = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$ or 2 V (whichever is greater), $I_{OUT} = 10\text{ mA}$, $V_{EN} = V_{IN}$, and $C_{OUT} = 1\ \mu\text{F}$
 Typical values are at $T_J = 25^{\circ}\text{C}$, (unless otherwise noted)



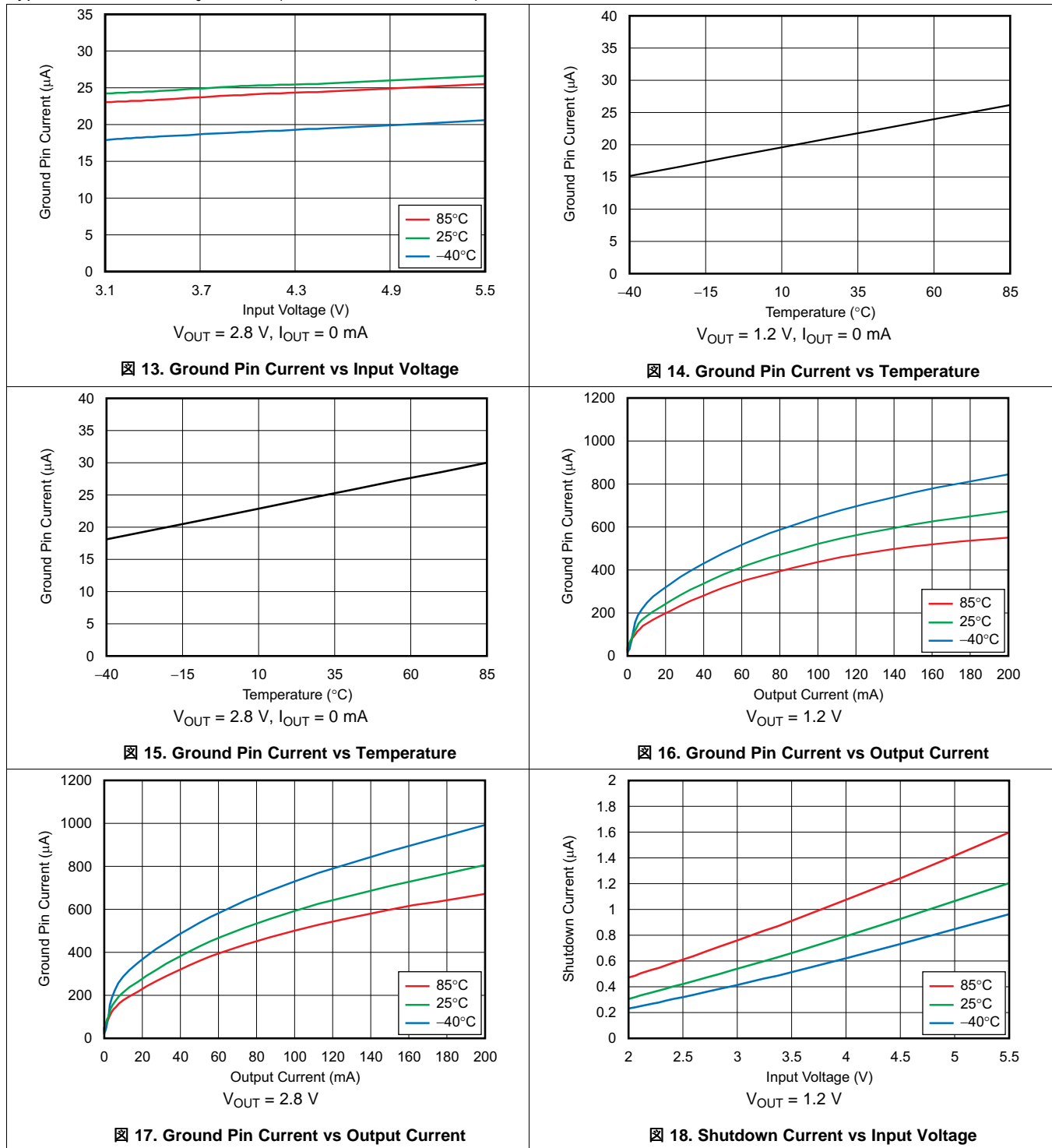
Typical Characteristics (continued)

at $T_J = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$ or 2 V (whichever is greater), $I_{OUT} = 10\text{ mA}$, $V_{EN} = V_{IN}$, and $C_{OUT} = 1\text{ }\mu\text{F}$
 Typical values are at $T_J = 25^{\circ}\text{C}$, (unless otherwise noted)



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 Typical values are at $T_J = 25^\circ\text{C}$, (unless otherwise noted)



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 Typical values are at $T_J = 25^{\circ}\text{C}$, (unless otherwise noted)

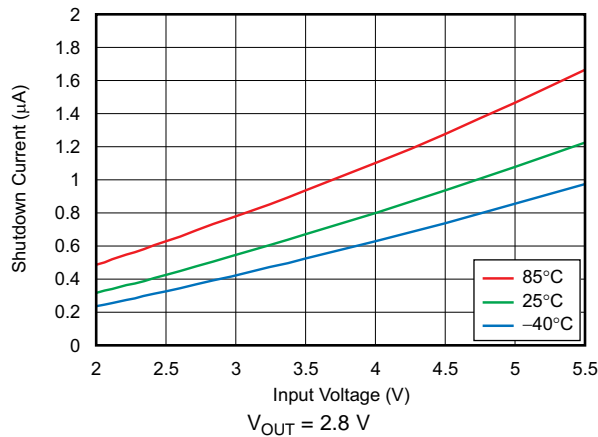


图 19. Shutdown Current vs Input Voltage

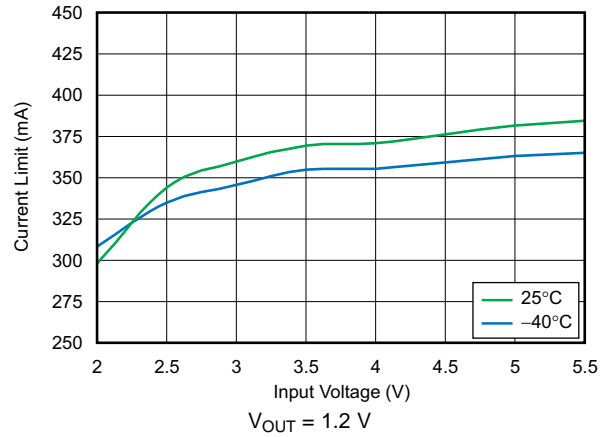


图 20. Current Limit vs Input Voltage

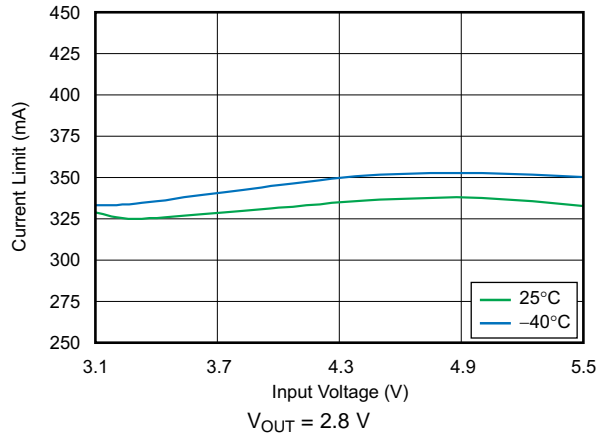


图 21. Current Limit vs Input Voltage

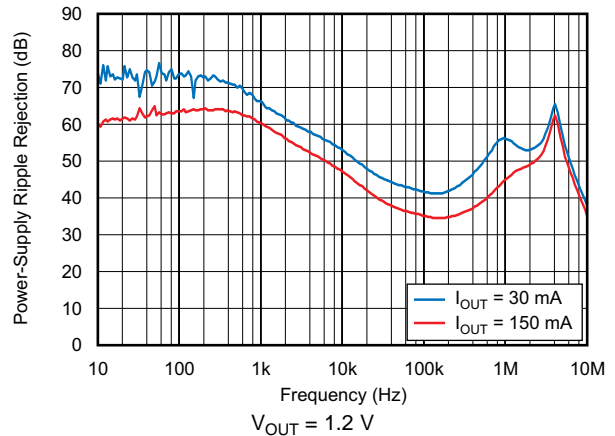


图 22. Power-Supply Ripple Rejection vs Frequency

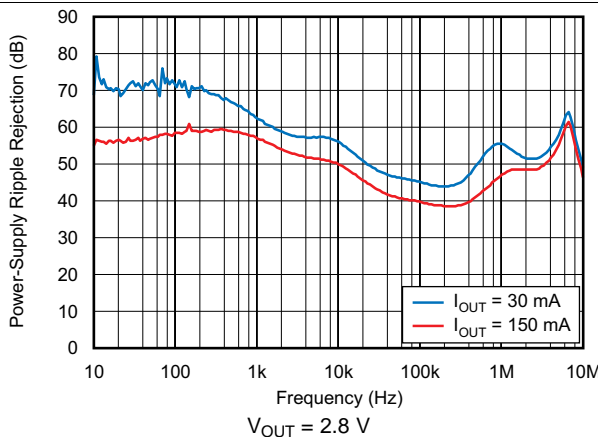


图 23. Power-Supply Ripple Rejection vs Frequency

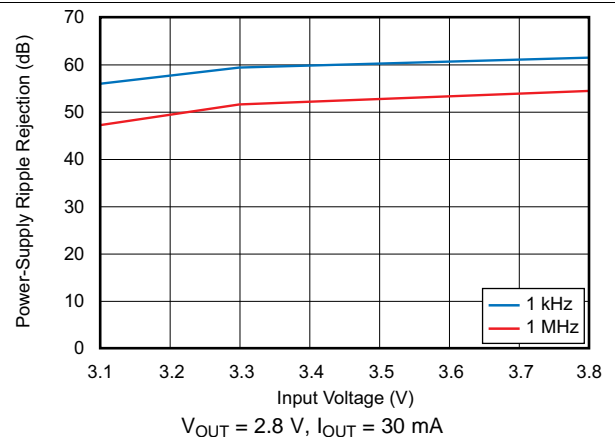
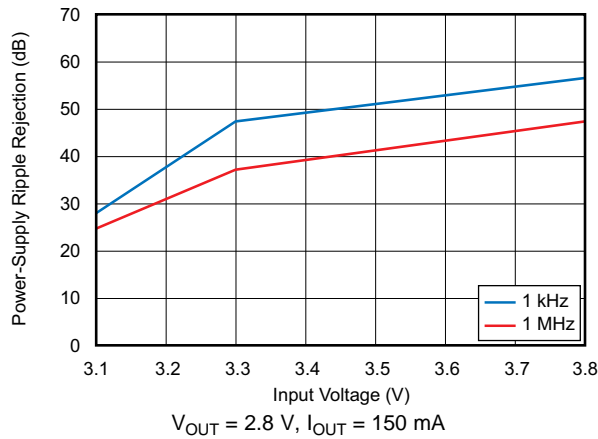


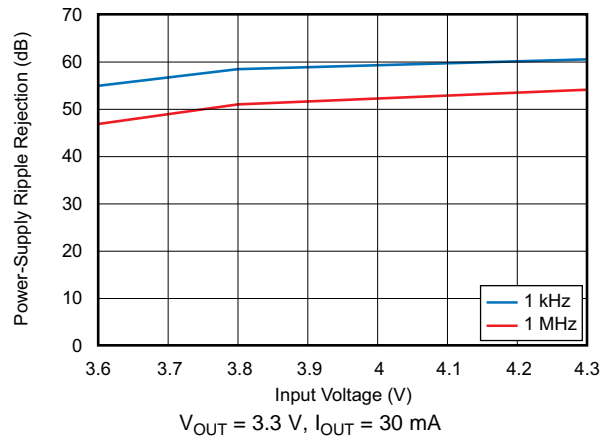
图 24. Power-Supply Ripple Rejection vs Input Voltage

Typical Characteristics (continued)

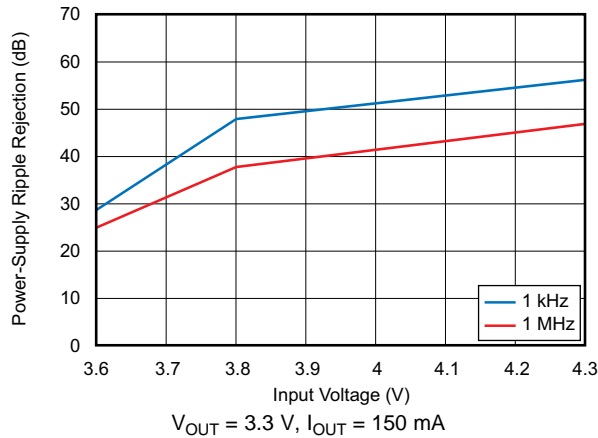
at $T_J = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$ or 2 V (whichever is greater), $I_{OUT} = 10\text{ mA}$, $V_{EN} = V_{IN}$, and $C_{OUT} = 1\ \mu\text{F}$
 Typical values are at $T_J = 25^{\circ}\text{C}$, (unless otherwise noted)



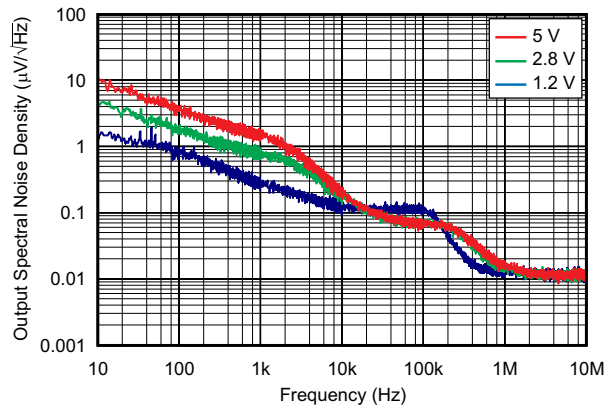
25. Power-Supply Ripple Rejection vs Input Voltage



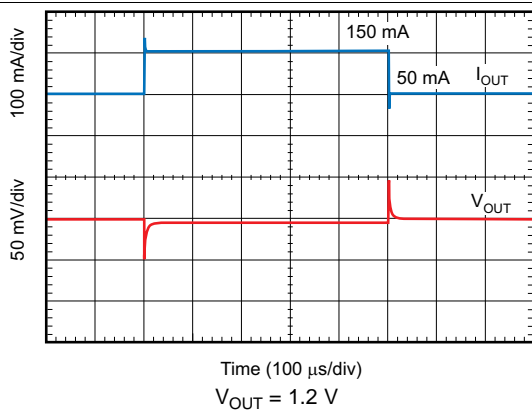
26. Power-Supply Ripple Rejection vs Input Voltage



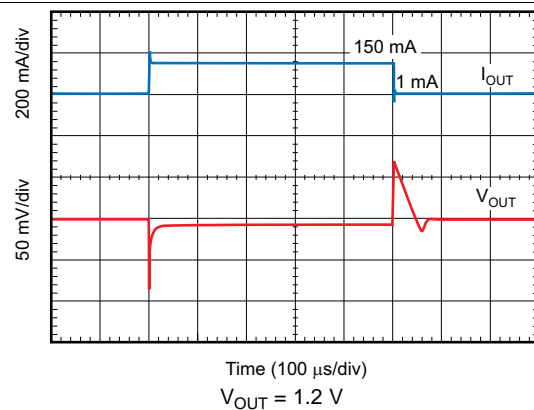
27. Power-Supply Ripple Rejection vs Input Voltage



28. Output Spectral Noise Density vs Frequency



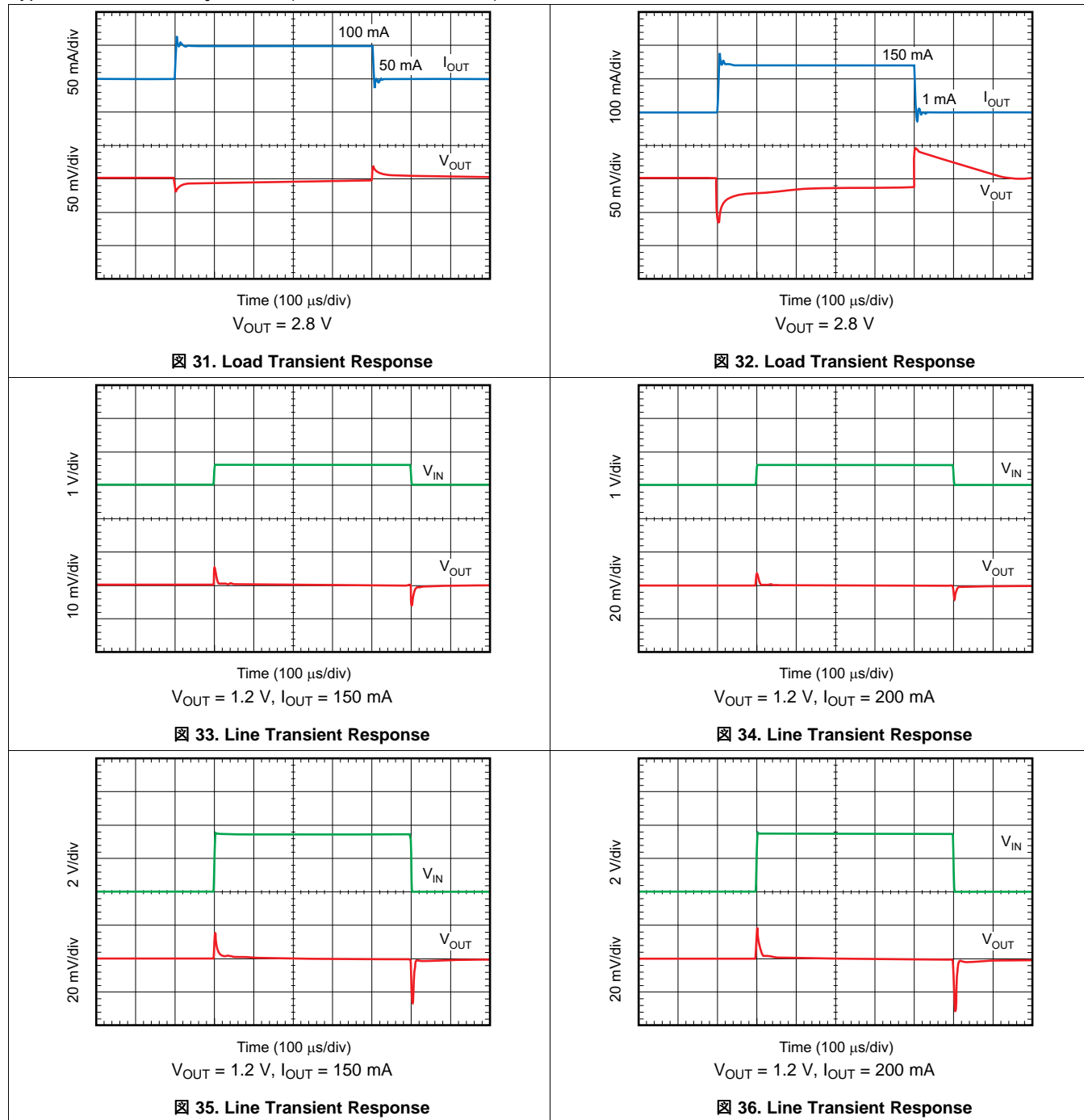
29. Load Transient Response



30. Load Transient Response

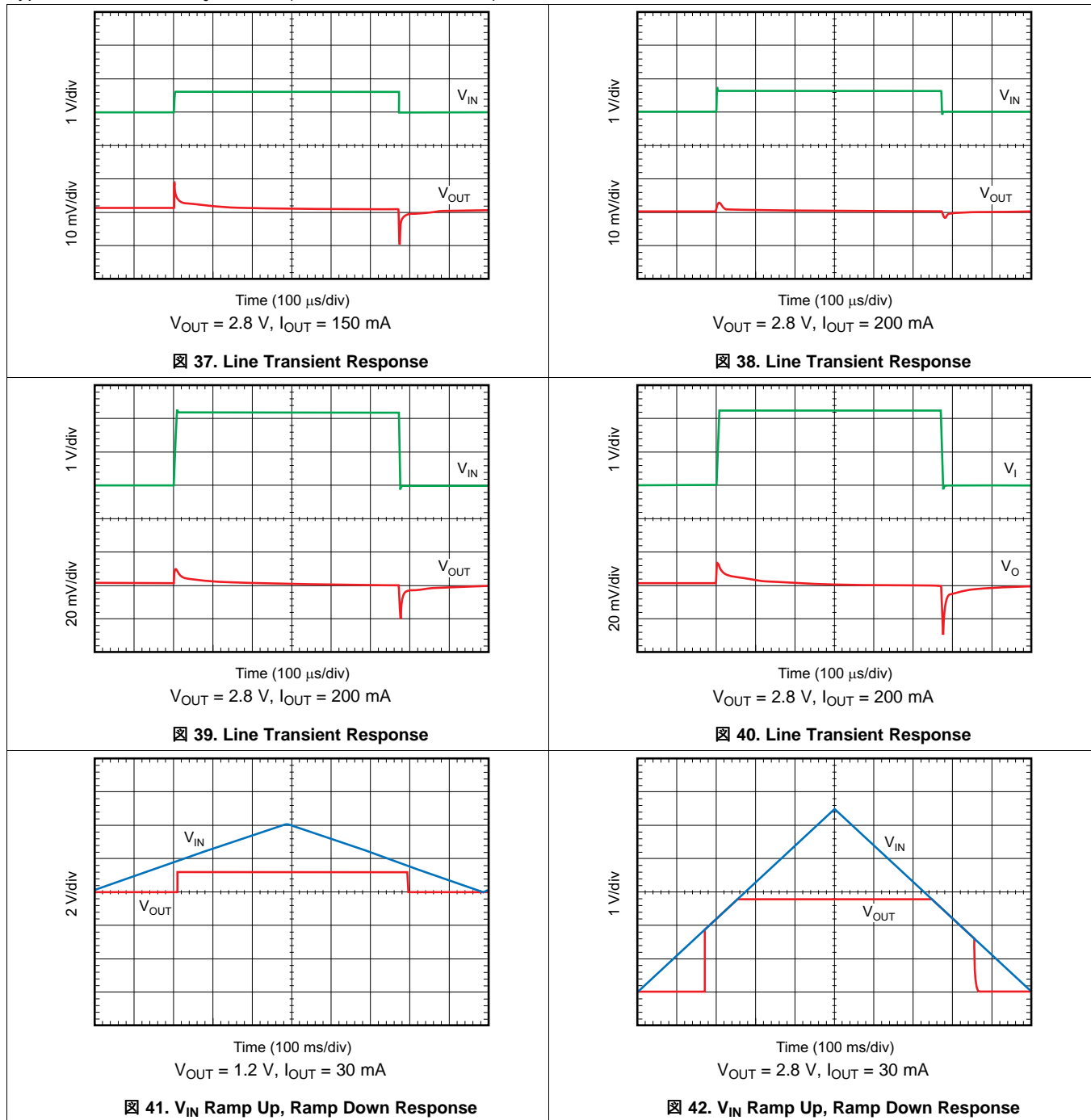
Typical Characteristics (continued)

at $T_J = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$ or 2 V (whichever is greater), $I_{OUT} = 10\text{ mA}$, $V_{EN} = V_{IN}$, and $C_{OUT} = 1\text{ }\mu\text{F}$
 Typical values are at $T_J = 25^{\circ}\text{C}$, (unless otherwise noted)



Typical Characteristics (continued)

at $T_J = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$ or 2 V (whichever is greater), $I_{OUT} = 10\text{ mA}$, $V_{EN} = V_{IN}$, and $C_{OUT} = 1\text{ }\mu\text{F}$
 Typical values are at $T_J = 25^\circ\text{C}$, (unless otherwise noted)

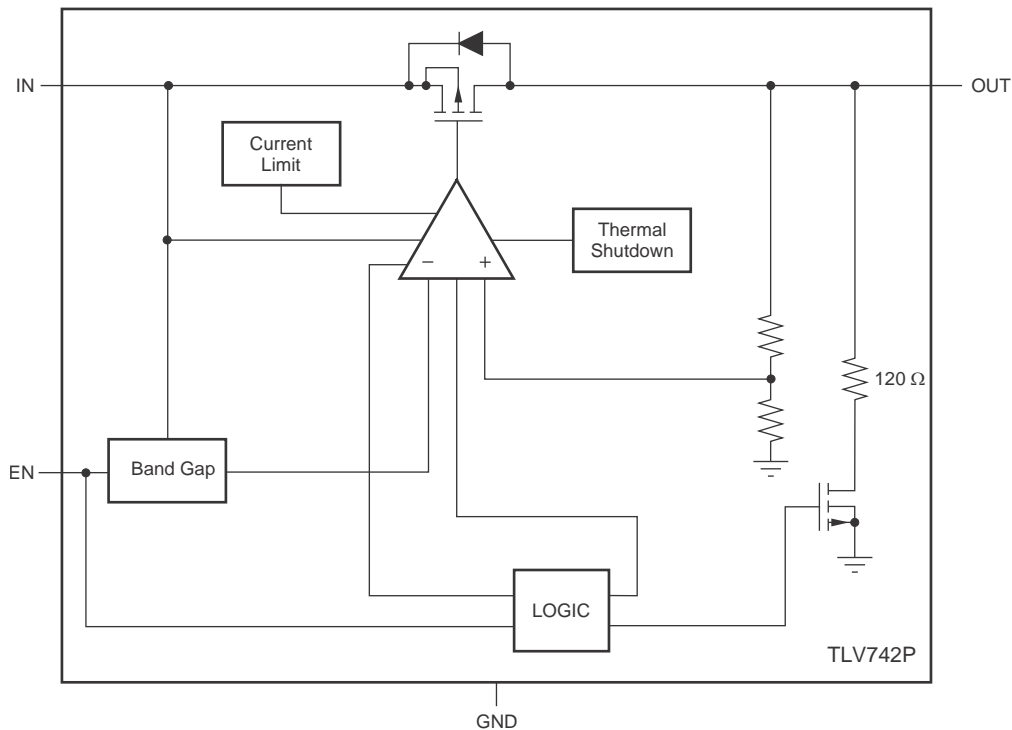


7 Detailed Description

7.1 Overview

The TLV742P device belongs to a family of LDOs. This device consumes low quiescent current and delivers excellent line and load transient performance. These characteristics [combined with low noise and very good PSRR with little ($V_{IN} - V_{OUT}$) headroom] make this device ideal for portable RF applications.

7.2 Functional Block Diagrams



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✶ 43. TLV742P Block Diagram

7.3 Feature Description

This LDO regulator offers current limit and thermal protection. The operating junction temperature of this device is -40°C to $+125^{\circ}\text{C}$.

7.3.1 Internal Current Limit

The internal current limit helps to protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of the output voltage. In such a case, the output voltage is not regulated, and is $V_{OUT} = I_{CL} \times R_L$. The PMOS pass transistor dissipates $(V_{IN} - V_{OUT}) \times I_{LIMIT}$ until thermal shutdown is triggered and the device turns off. When the device cools, the internal thermal shutdown circuit turns the device back on. If the fault condition continues, the device cycles between current limit and thermal shutdown; see [Thermal Information](#) for more details.

The PMOS pass element has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of the rated output current is recommended.

Feature Description (continued)

7.3.2 Shutdown

The enable pin (EN) is active high. The device is enabled when voltage at the EN pin goes above 0.9 V. The device is turned off when the EN pin is held at less than 0.4 V. When shutdown capability is not required, EN can be connected to the IN pin.

The TLV742P version has internal active pulldown circuitry that discharges the output with a time constant as given by 式 1:

$$\tau = \frac{(120 \cdot R_L)}{(120 + R_L)} \cdot C_{OUT}$$

where:

- R_L = Load resistance
- C_{OUT} = Output capacitor

(1)

7.4 Device Functional Modes

The TLV742P series is specified over the recommended operating conditions (see [Recommended Operating Conditions](#)). The specifications may not be met when exposed to conditions outside of the recommended operating range.

To turn on the regulator, the EN pin must be driven over 0.9 V. Driving the EN pin below 0.4 V causes the regulator to enter shutdown mode.

In shutdown, the current consumption of the device typically reduces to 1 μ A.

8 Application and Implementation

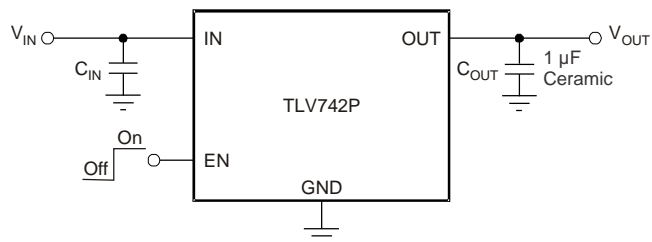
注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV742P is a LDO with low quiescent current that delivers excellent line and load transient performance. This LDO regulator offers current limit and thermal protection. The operating junction temperature of this device series is -40°C to $+125^{\circ}\text{C}$.

8.2 Typical Application



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图 44. Typical Application Circuit

8.2.1 Design Requirements

Provide an input supply with adequate headroom to meet minimum V_{IN} requirements (as listed in 表 1), compensate for the GND pin current, and to power the load.

表 1. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	1.8 V to 3.6 V
Output voltage	1.2 V
Output current	100 mA

8.2.2 Detailed Design Procedure

8.2.2.1 Input and Output Capacitor Requirements

Generally, 1- μ F X5R- and X7R-type ceramic capacitors are recommended because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature.

However, the TLV742P is designed to be stable with an effective capacitance of 0.1 μ F or larger at the output. As a result, the device is stable with capacitors of other dielectric types if the effective capacitance under operating bias voltage and temperature is greater than 0.1 μ F. This effective capacitance refers to the capacitance that the LDO detects under operating bias voltage and temperature conditions; that is, the capacitance after taking bias voltage and temperature derating into consideration. In addition to using less expensive dielectrics, this stability with 0.1- μ F effective capacitance enables the use of smaller footprint capacitors that have higher derating in size- and space-constrained applications.

Using a 0.1- μ F rated capacitor at the output of the LDO does not ensure stability because the effective capacitance under the specified operating conditions is less than 0.1 μ F. Maximum ESR must be less than 200 m Ω .

Although an input capacitor is not required for stability, good analog design practice is to connect a 0.1- μ F to 1- μ F, low ESR capacitor across the IN pin and GND pin of the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be required if large, fast rise-time load transients are anticipated, or if the device is not located close to the power source. If source impedance is more than 2- Ω , a 0.1- μ F input capacitor may be required to ensure stability.

8.2.2.2 Dropout Voltage

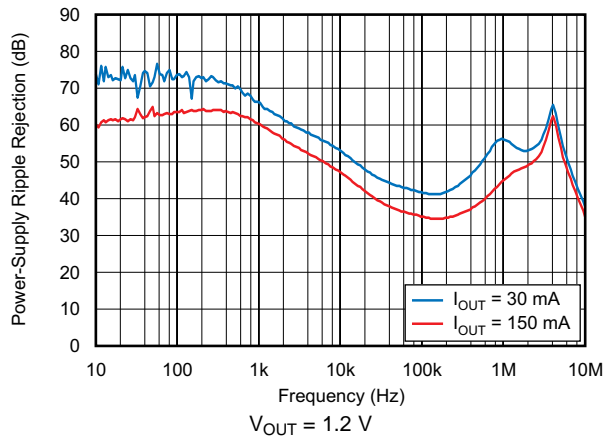
The TLV742P series of LDOs use a PMOS pass transistor to achieve low dropout. When ($V_{IN} - V_{OUT}$) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device functions similar to a resistor in dropout.

PSRR and transient response degrade when ($V_{IN} - V_{OUT}$) approaches dropout.

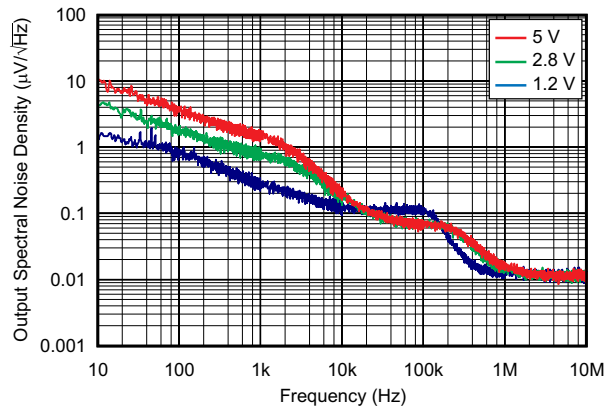
8.2.2.3 Transient Response

Increasing the size of the output capacitor reduces overshoot and undershoot magnitude but increases the duration of the transient response.

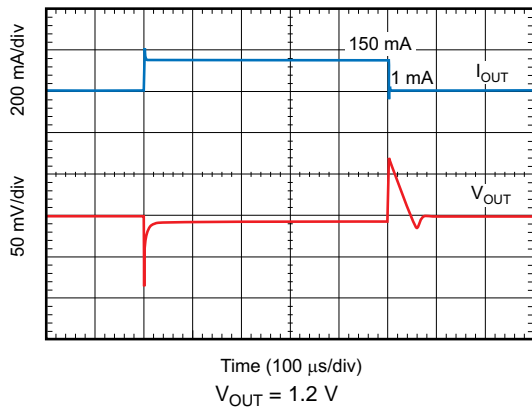
8.2.3 Application Curves



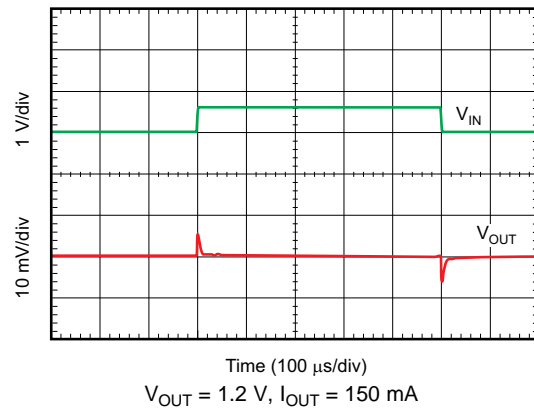
45. Power-Supply Ripple Rejection vs Frequency



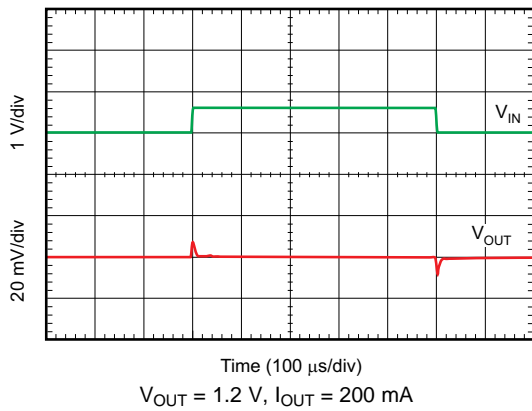
46. Output Spectral Noise Density vs Frequency



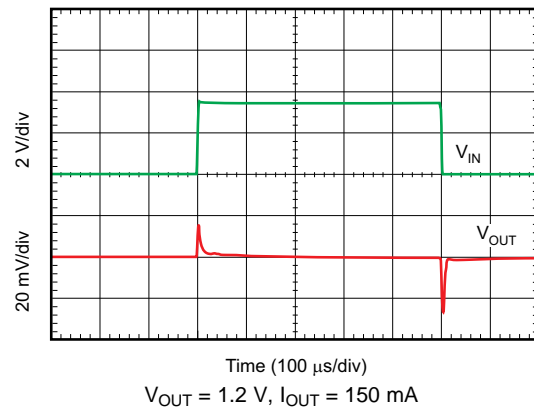
47. Load Transient Response



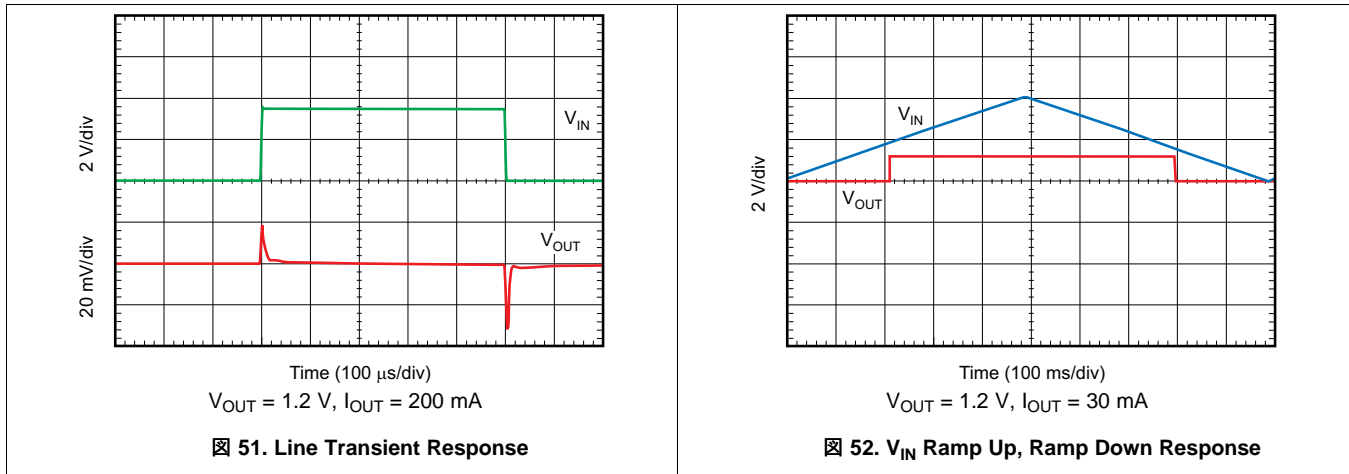
48. Line Transient Response



49. Line Transient Response



50. Line Transient Response



8.3 Do's and Don'ts

Place at least one 1- μ F ceramic capacitor as close as possible to the OUT pin of the regulator.

Do not place the output capacitor more than 10 mm away from the regulator.

Connect a 1- μ F low equivalent series resistance (ESR) capacitor across the IN pin and GND input of the regulator for improved transient performance.

Do not exceed the absolute maximum ratings.

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2 V and 5.5 V. The input voltage range provides adequate headroom for the device to have a regulated output. This input supply must be well-regulated (see [Figure 33](#) through [Figure 40](#)). If the input supply is noisy, additional input capacitors with low ESR help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

10.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

Place input and output capacitors as close to the device pins as possible. To improve ac performance (such as PSRR, output noise, and transient response), TI recommends that the board be designed with separate ground planes for V_{IN} and V_{OUT} , with the ground plane connected only at the GND pin of the device, as shown in [Figure 53](#). Connect the ground connection for the output capacitor directly to the GND pin of the device. High ESR capacitors can degrade PSRR performance.

10.1.2 Package Mounting

Solder pad footprint recommendations are available from the TI website at www.ti.com. The recommended land pattern for the DQN (X2SON-4) package is provided in the [メカニカル、パッケージ、および注文情報](#) section.

10.2 Layout Example

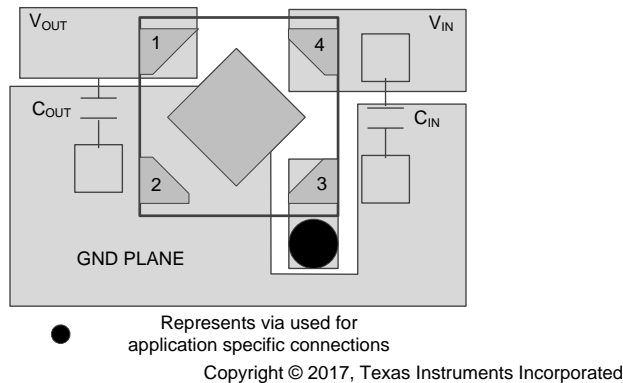


Fig 53. Recommended Layout Example

10.3 Thermal Considerations

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is enabled again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, which protects the regulator from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, limit junction temperature to 125°C (maximum). To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

For good reliability, thermal protection triggers at least 35°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the LDO is designed to protect against overload conditions. This circuitry is not intended to replace proper heat sinking. Continuously running the LDO into thermal shutdown degrades device reliability.

10.4 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed-circuit-board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air.

Performance data for JEDEC low- and high-K boards are shown in [Thermal Information](#). Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers improves heat sink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current and the voltage drop across the output pass element, as shown in [Equation 2](#).

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 開発サポート

11.1.1.1 評価モジュール

TLV742Pを使用する回路の初期性能評価に役立てるため、評価モジュール(EVM)を利用可能です。TLV70728EVM-612の設計キットおよび評価モジュールについては、[TLV70728EVM-612ユーザーズ・ガイド](#)を参照してください。

EVMは、テキサス・インスツルメンツのWebサイトの[TLV742P](#)製品フォルダからご請求されるか、[TI eStore](#)から直接お求めになれます。

11.1.2 デバイスの項目表記

製品情報⁽¹⁾

製品名	V _{OUT} ⁽²⁾
TLV742xx(x)Pyyyz	<p>xx(x)は公称出力電圧です。出力電圧の分解能が100mVの場合、注文番号に2桁が使用されます。それ以外の場合は3桁が使用されます(例: 18=1.8V、285=2.85V)。</p> <p>Pはオプションです。Pの付いたデバイスは、アクティブ出力放電機能付きのLDOレギュレータを備えています。</p> <p>YYYはパッケージ指定子です。</p> <p>Zはパッケージ数量です。Rはリール(3000ピース)、Tはテープ(250ピース)を表します。</p>

- (1) 最新のパッケージおよび注文情報については、このドキュメントの最後にあるパッケージ・オプションの付録を参照するか、www.ti.comのデバイス製品フォルダをご覧ください。
- (2) 出力電圧は、0.85Vから5Vまで、50mV刻みで利用できます。詳細と在庫については、工場にお問い合わせください。

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™オンライン・コミュニティ *TIのE2E (Engineer-to-Engineer) コミュニティ*。エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイデアを検討して、問題解決に役立てることができます。

設計サポート *TIの設計サポート* 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

11.4 商標

E2E is a trademark of Texas Instruments.

11.5 静電気放電に関する注意事項



すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV74211PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8H	Samples
TLV74212PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8G	Samples
TLV74215PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8F	Samples
TLV74218PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8E	Samples
TLV74225PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CS	Samples
TLV74227PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8D	Samples
TLV74228PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8C	Samples
TLV74229PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8B	Samples
TLV74230PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CT	Samples
TLV74233PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7Z	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV74211PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV74212PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV74215PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV74218PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV74225PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV74227PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV74228PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV74229PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV74230PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV74233PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV74211PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV74212PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV74215PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV74218PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV74225PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV74227PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV74228PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV74229PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV74230PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV74233PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

DQN 4

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

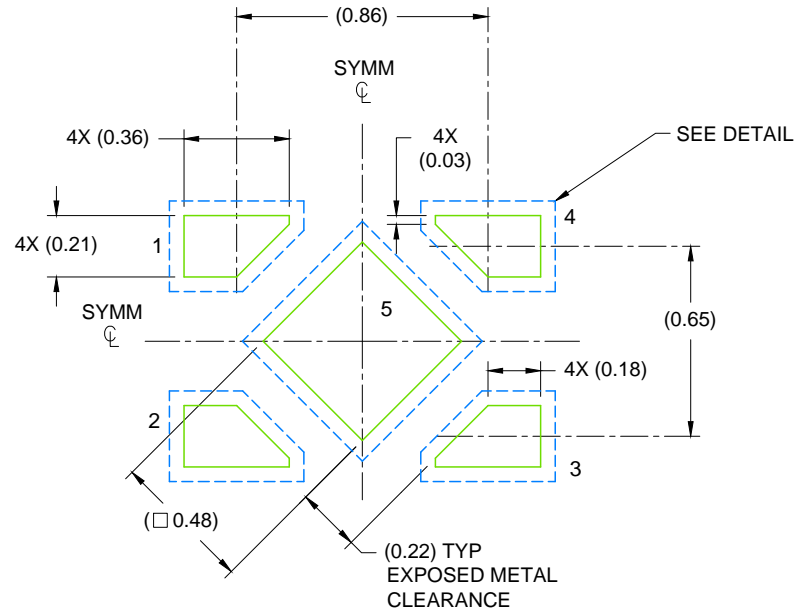
4210367/F



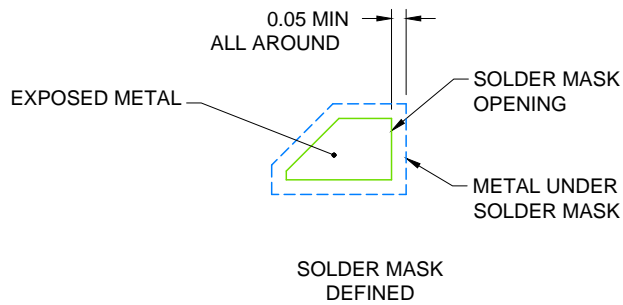
4215302/E 12/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.
5. Shape of exposed side leads may differ.
6. Number and location of exposed tie bars may vary.



LAND PATTERN EXAMPLE
SCALE: 40X

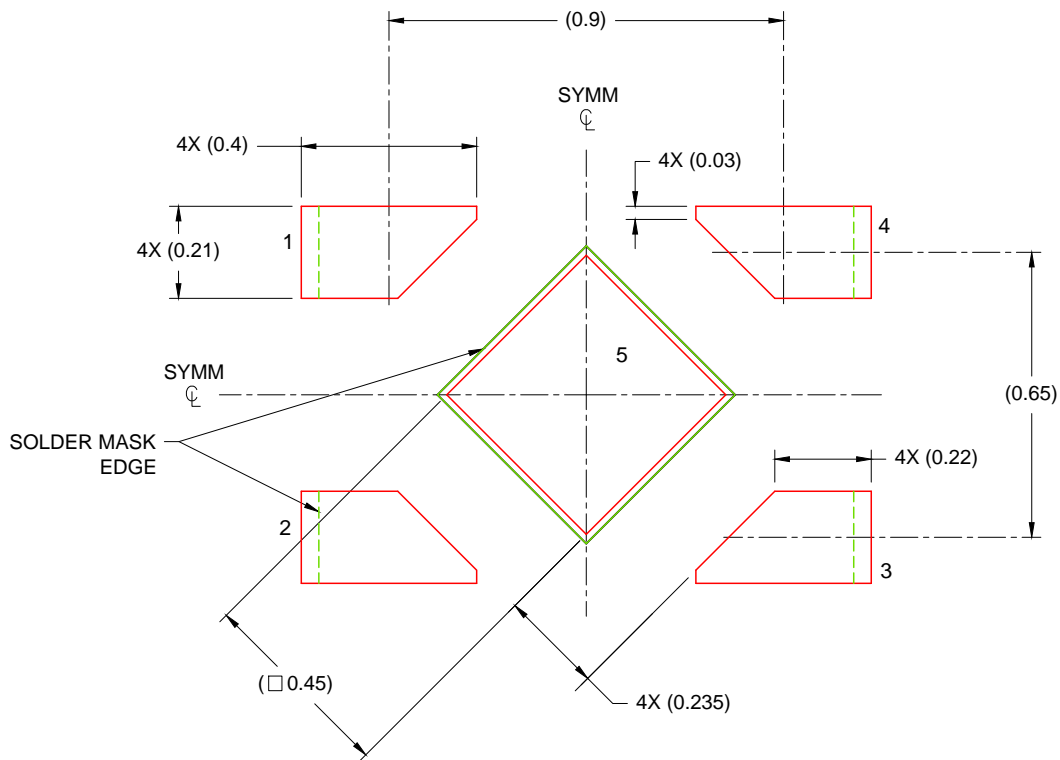


SOLDER MASK DEFINED
SOLDER MASK DETAIL

4215302/E 12/2016

NOTES: (continued)

7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
8. If any vias are implemented, it is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
 BASED ON 0.075 - 0.1mm THICK STENCIL
 EXPOSED PAD
 88% PRINTED SOLDER COVERAGE BY AREA
 SCALE: 60X

4215302/E 12/2016

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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