TPL7407LA 30V、7チャネルのローサイド・ドライバ

1 特長

- 600mAの定格ドレイン電流(チャネルごと)
- 7チャネル・ダーリントン・アレイ(例: ULN2003A)に対するピン互換のCMOS代替品
- 高い電力効率(非常に低いV_{OL})
  - ダーリントン・アレイと比べて100mAで1/4以下のV_{OL}
- 非常に低い出力リーク: チャネルごとに10nA未満
- 拡張周囲温度範囲: T_A = -40℃～+125℃
- 高い電圧出力: 30V
- 1.8V～5Vのマイクロコントローラおよびロジック・インターフェイスと互換
- 誘導性キックバック保護用のフリー・ホイール・ダイオード内蔵
- 入力プルダウン抵抗により入力ドライバをトライステートとすることが可能
- 入力RCスナバーにより、ノイズの多い環境でスプリアス動作を排除
- 誘導性負荷ドライバ・アプリケーション
- JESD 22を超えるESD保護
  - HBM ±2kV、CDM ±500V
- 16ピンのSOICおよびTSSOPパッケージで供給

2 アプリケーション

- 誘導性負荷
  - リレー
  - ユニポーラ・ステッパおよびブラシ付きDCモータ
  - ソレノイドおよびバルブ
- LED
- ロジック・レベルのシフト
- ゲートおよびIGBTドライブ

3 概要

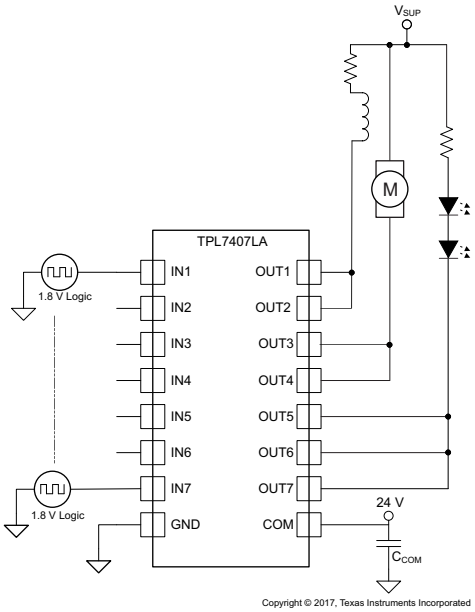
TPL7407LAは高電圧、大電流のNMOSトランジスタ・アレイです。このデバイスは、出力電圧の高い7つのNMOSトランジスタと、誘導性負荷のスイッチングを行う共通カソードのクランプ・ダイオードで構成されます。単一のNMOSチャネルの最大ドレイン電流定格は600mAです。すべてのGPIO範囲(1.8V～5V)にわたって最大の駆動強度を得るため、新しいレギュレーションおよび駆動回路が追加されました。トランジスタを並列接続して、より大電流を使用することもできます。

製品情報(1)

型番	パッケージ(ピン数)	本体サイズ(公称)
TPL7407LAPW	TSSOP (16)	5.00mm×4.40mm
TPL7407LAD	SOIC (16)	9.90mm×3.91mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

単純なアプリケーションの回路図



目次

4 改訂履歴

2017年5月発行のものから更新 **Page**

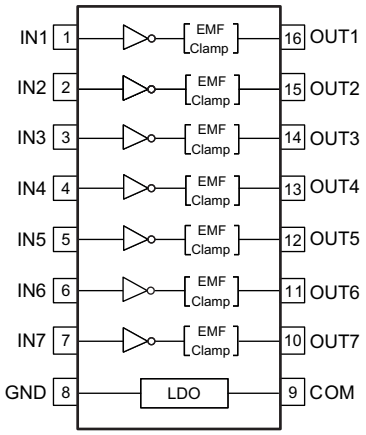
- 「*製品情報*」表、「*ピン構成および機能*」セクション、「*熱に関する情報*」表にDパッケージを 追加 ... 3

5 概要（続き）

TPL7407LAの主要な利点は、バイポーラのダーリントン実装と比べて電力効率が高く、リークが少ないことです。V_{OL}が低いため、従来のリレー・ドライバと比べて消費電力が半分以下で、電流はチャネルごとに250mA未満です。

6 Pin Configuration and Functions

D and PW Package
16-Pin SOIC and TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
COM	9	—	Supply pin that must be tied to 6.5 V or higher for proper operation (see the *Power Supply Recommendations* section for more information)
GND	8	—	Ground pin
IN(X)	1	I	GPIO inputs that drives the outputs "low" (or sink current) when driven "high"
	2		
	3		
	4		
	5		
	6		
	7		
OUT(X)	10	O	Driver output that sinks currents after input is driven "high"
	11		
	12		
	13		
	14		
	15		
	16		

7 Specifications

7.1 Absolute Maximum Ratings

at 25°C free-air temperature (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{OUT}	Pins OUT1-OUT7 to GND voltage	–0.3	32	V
V_{OK}	Output clamp diode reverse voltage (2)	–0.3	32	V
V_{COM}	COM pin voltage (2)	–0.3	32	V
V_{IN}	Pins IN1-IN7 to GND voltage (2)	–0.3	30	V
I_{DS}	Continuous drain current per channel (3) (4)		600	mA
I_{OK}	Output clamp current		500	mA
I_{GND}	Total continuous GND-pin current		–2	A
T_J	Operating virtual junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the GND/substrate pin, unless otherwise noted.
(3) Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

Over operating temperature range

		MIN	MAX	UNIT
V_{OUT}	OUT1 – OUT7 pin voltage for recommended operation	0	30	V
V_{COM}	COM pin voltage range for full output drive	6.5	30	V
V_{IL}	IN1- IN7 input low voltage ("Off" high impedance output)		0.9	V
V_{IH}	IN1- IN7 input high voltage ("Full Drive" low impedance output)	1.5		V
T_A	Operating free-air temperature	–40	125	°C
I_{DS}	Continuous drain current	0	500	mA

7.4 Thermal Information

THERMAL METRIC (1)		TPL7407LA		UNIT
		TSSOP (PW)	SOIC (D)	
		16 PINS	16 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	113.1	88	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	46.5	47.6	°C/W
θ_{JB}	Junction-to-board thermal resistance	58.6	45.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7	14.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	58	45.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

T_J= –40°C to +125°C; Typical Values at T_A= 25°C (1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OL} (V_{DS})	OUT1- OUT7 low-level output voltage	V_{IN} ≥ 1.5 V	I_D = 100 mA		210	450	mV
			I_D = 200 mA		430	900	
V_{IL}	IN1- IN7 low-level input voltage	I_D = 5 µA				0.9	V
V_{IH}	IN1- IN7 high-level input voltage	I_D = 100 mA		1.5			V
$I_{OUT(OFF)}$ (I_{DS_OFF})	OUT1- OUT7 OFF-state leakage current	V_{OUT} = 24V, V_{IN} ≤ 0.9V			10	500	nA
V_F	Clamp forward voltage	I_F = 200 mA				1.4	V
$I_{IN(off)}$	IN1- IN7 Off-state input current	V_{INX} = 0 V	V_{OUT} = 30 V			500	nA
$I_{IN(ON)}$	IN1- IN7 ON state input current	V_{INX} = 1.5 V – 5 V				10	µA
I_{COM}	Static current flowing through COM pin	V_{COM} = 6.5 V – 30 V			17	30	µA

(1) During production testing, device is tested under short duration, therefore $T_A = T_J$.

7.6 Switching Characteristics

Typical Values at T_A= 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	V_{INX} ≥ 1.65 V, Vpull-up = 24 V, Rpull-up = 48 Ω		350		ns
t_{PHL}	Propagation delay time, high- to low-level output	V_{INX} ≥ 1.65 V, Vpull-up = 24 V, Rpull-up = 48 Ω		350		ns
C_i	Input capacitance	V_I = 0, f = 100 kHz		5		pF

7.7 Typical Characteristics

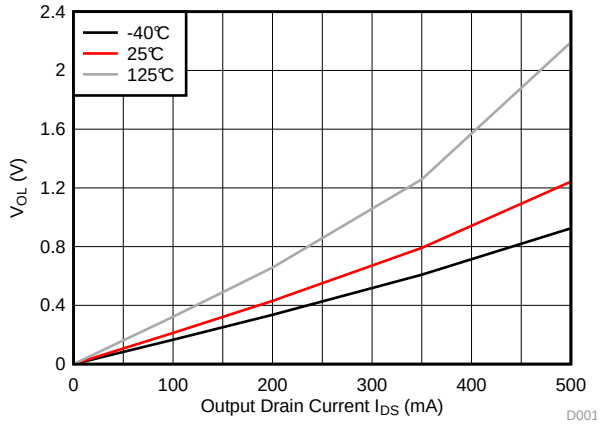


図 1. V_{OL} (V_{DS})

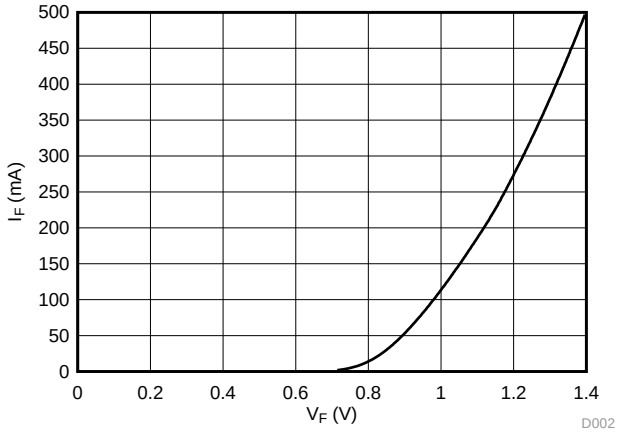


図 2. Flyback Diode Forward Voltage at 25°C

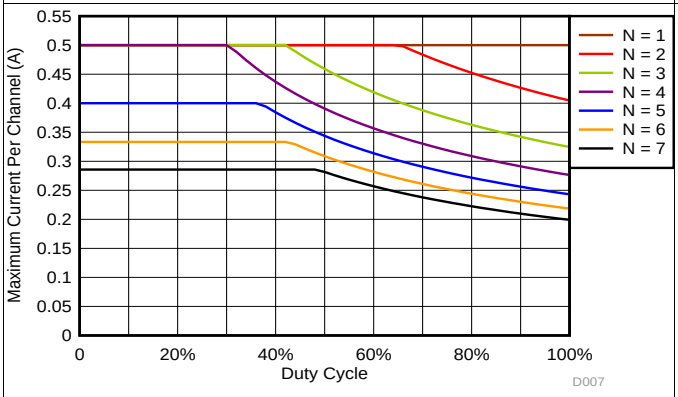


図 3. PW Package Maximum Collector Current vs Duty Cycle at 25°C

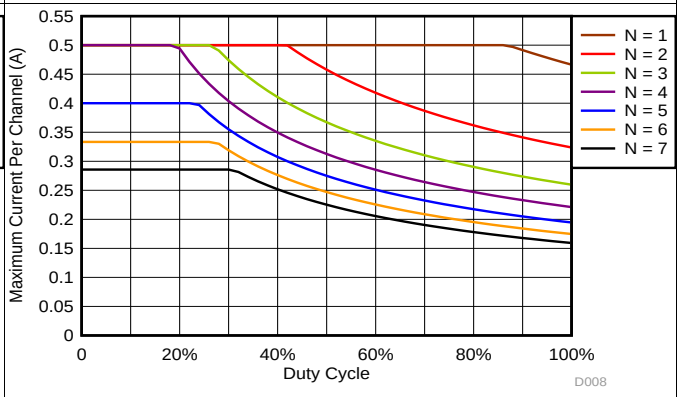


図 4. PW Package Maximum Collector Current vs Duty Cycle at 70°C

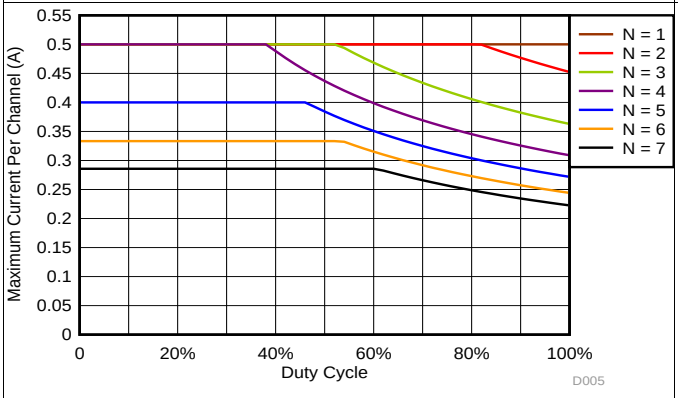


図 5. D Package Maximum Collector Current vs Duty Cycle at 25°C

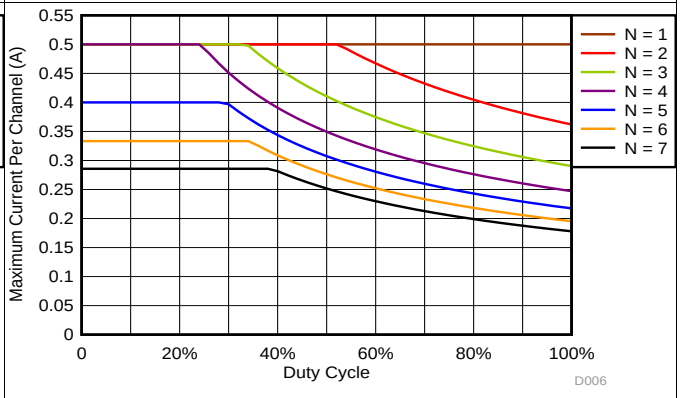


図 6. D Package Maximum Collector Current vs Duty Cycle at 70°C

8 Detailed Description

8.1 Overview

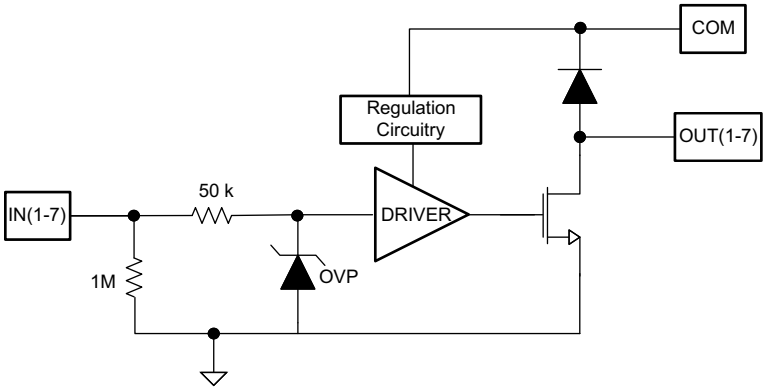
This device has proven ubiquity and versatility across a wide range of applications. This is due to its integration of 7 low side NMOS transistors that are capable of sinking up to 600 mA and wide GPIO range capability.

The TPL7407LA comprises seven high voltage, high current NMOS transistors tied to a common ground driven by internal level shifting and gate drive circuitry. The TPL7407LA offers solutions to many interface needs, including solenoids, relays, lamps, small motors, and LEDs. Applications requiring sink currents beyond the capability of a single output may be accommodated by paralleling the outputs.

The TPL7407LA also enables pin to pin replacement with legacy 7 channel darlington pair implementations.

This device can operate over a wide temperature range (–40°C to +125°C).

8.2 Functional Block Diagram



8.3 Feature Description

Each channel of the TPL7407LA consists of high power low side NMOS transistors driven by level shifting and gate driving circuitry. The gate drivers allow for high output current drive with a very low input voltage, meaning full operation with low GPIO voltages.

In order to enable floating inputs a 1-MΩ pull-down resistor exists on each channel. Another 50-kΩ resistor exists between the input and gate driving circuitry. This exists to limit the input current whenever there is an over voltage and the internal Zener clamps. It also interacts with the inherent capacitance of the gate driving circuitry to behave as an RC snubber to help prevent spurious switching in noisy environment.

In order to power the gate driving circuitry an LDO exists. See the *Power Supply Recommendations* section for further detail on this circuitry.

The diodes connected between the output and COM pin is used to suppress kick-back voltage from an inductive load that is excited when the NMOS drivers are turned off (stop sinking) and the stored energy in the coils causes a reverse current to flow into the coil supply.

8.4 Device Functional Modes

8.4.1 Inductive Load Drive

When the COM pin is tied to the coil supply voltage, the TPL7407LA is able to drive inductive loads and suppress the kick-back voltage via the internal free wheeling diodes.

8.4.2 Resistive Load Drive

When driving a resistive load, a pull-up resistor is needed in order for the TPL7407LA to sink current and for there to be a logic high level. The COM pin must be supplied ≥ 6.5 V for full functionality.

Device Functional Modes (continued)

8.4.3 ON State Input Current

The current into the INx pins is defined in the electrical characteristics table for input voltages from 1.5 V to 5 V. At higher voltages, this leakage increases, and the input current can be estimated using the approximate clamp voltage for the OVP diode, 6.4 V. 式 1 shows how to approximate input current for input voltages greater than 6.4 V:

$$I_{IN(ON)} = V_{IN} / 1M\Omega + (V_{IN} - 6.4V) / 50k\Omega \quad (1)$$

where

- V_{IN} is the input voltage
- 1 MΩ is the input pull-down resistance
- 50 kΩ is the input series resistance
- 6.8 V is the approximate clamp voltage for the OVP diode

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPL7407LA is typically used to drive a high voltage and/or current peripheral from an MCU or logic device that cannot tolerate these conditions. The following design is a common application of the TPL7407LA, driving inductive loads. This includes motors, solenoids & relays. Each load type can be modeled by what's seen in 図 9.

9.1.1 Unipolar Stepper Motor Driver

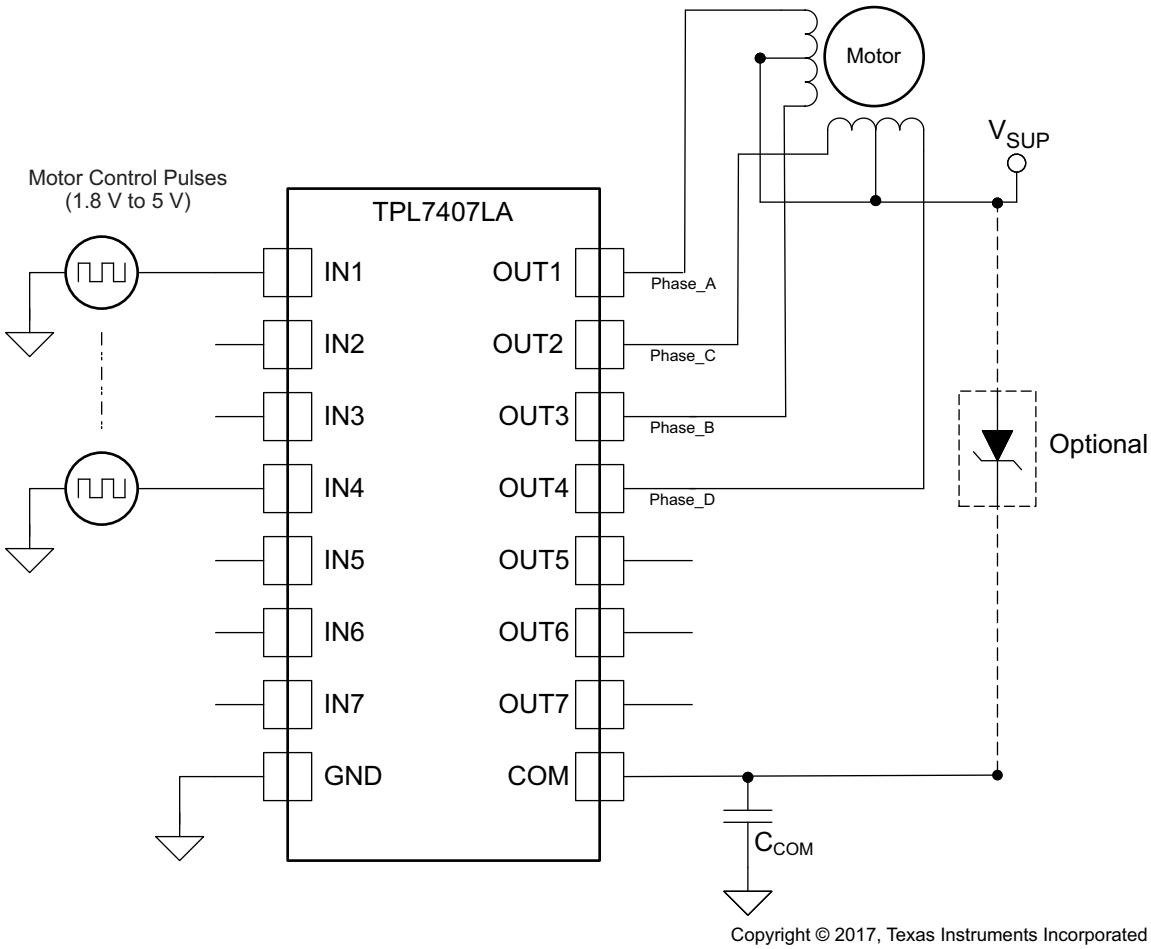


図 7. Stepper Motor Driver Schematic

図 7 shows an implementation of the TPL7407LA for driving a uniploar stepper motor. The unconnected input channels can be used for other functions. When an input pin is left open the internal 1-MΩ pull down resistor pulls the respective input pin to GND potential. For higher noise immunity use an external short across an unconnected input and GND pins. The COM pin must be tied to the supply of whichever inductive load is being driven for the driver to be protected by the free-wheeling diode.

For more information on this application, see the *Stepper Motor Driving With Peripheral Drivers (Driver ICs)* application report.

Application Information (continued)

9.1.2 Multi-Purpose Sink Driver

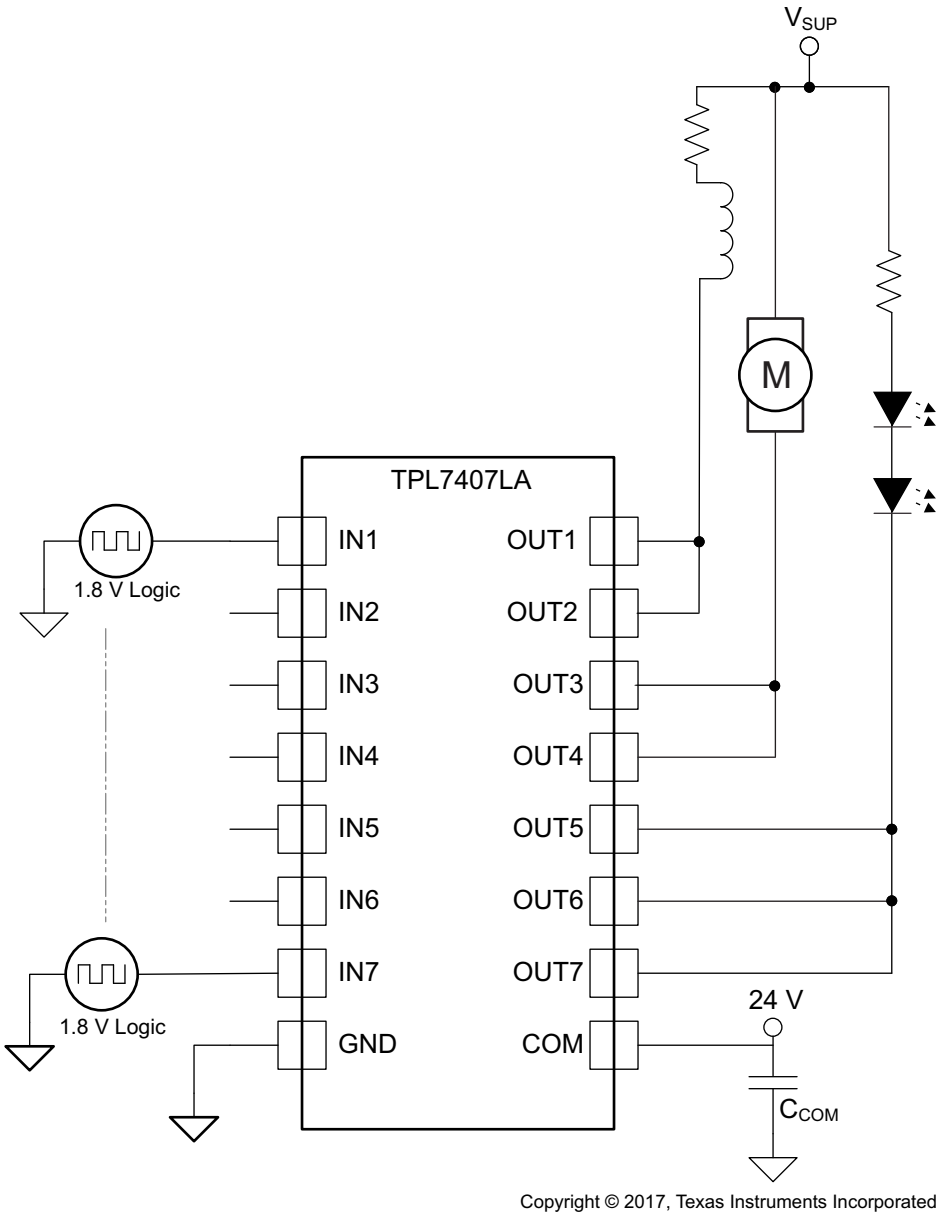


図 8. Multi-Purpose Sink Driver Schematic

When configured as per 図 8, the TPL7407LA may be used as a multi-purpose driver. The output channels may be tied together to sink more current. The TPL7407LA can easily drive motors, relays & LEDs with little power dissipation. COM must be tied to highest load voltage, which may or may not be same as inductive load supply.

9.2 Typical Application

A common application for the TPL7407LA is driving inductive loads such as relays, solenoids, and unipolar stepper motors.

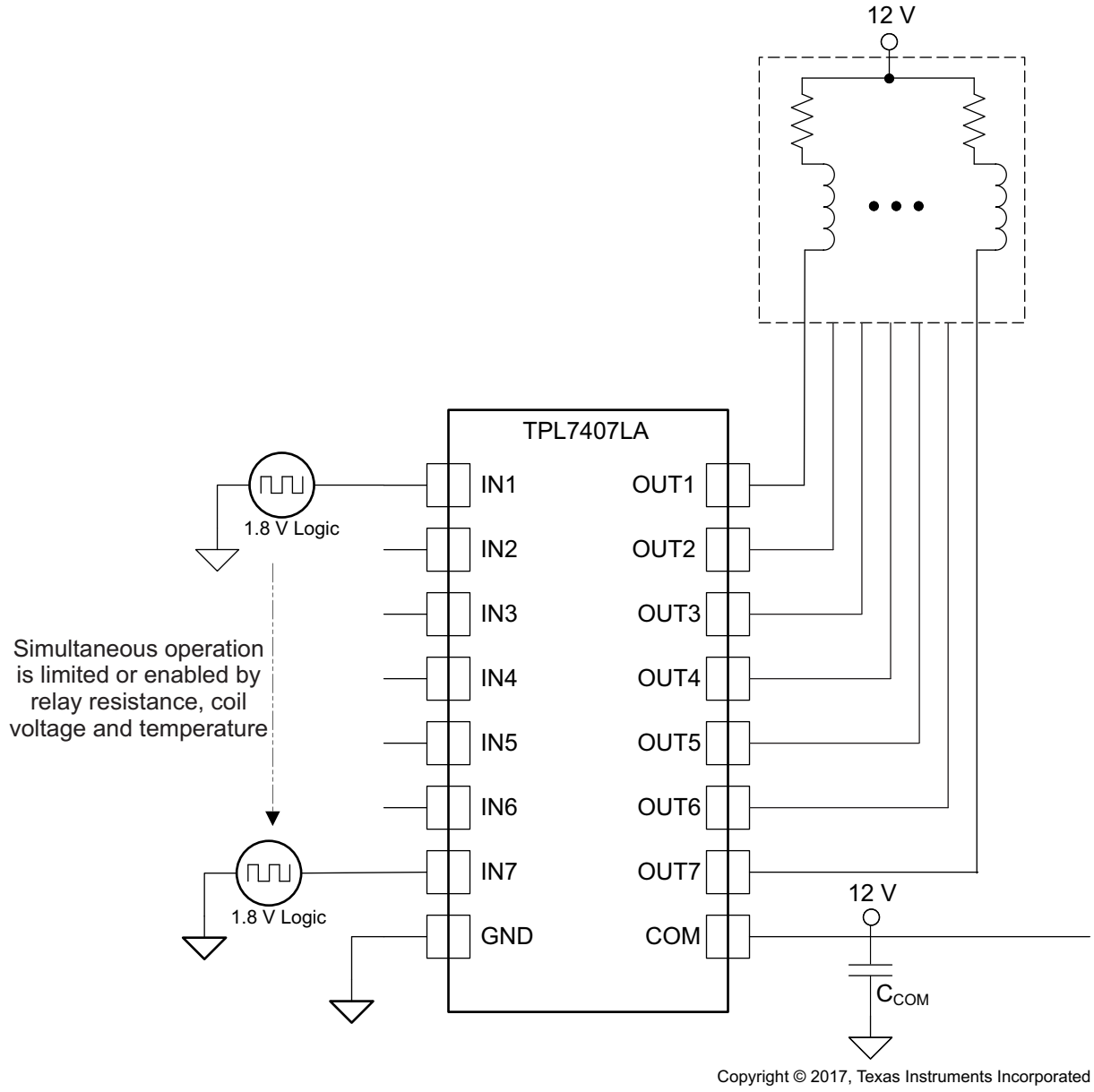


図 9. Inductive Load Driver Schematic

Typical Application (continued)

9.2.1 Design Requirements

For this design example, use the parameters listed in 表 1 as the input parameters.

表 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
GPIO Voltage	1.8 V, 3.3 V or 5 V
Coil supply voltage	6.5 V to 30 V
Number of channels	7
Output current (R_{COIL})	20 mA to 300 mA per channel
C_{COM}	0.1 µF
Duty cycle	100%

9.2.2 Detailed Design Procedure

When using the TPL7407LA in a coil driving application, determine the following:

- Input Voltage Range
- Temperature Range
- Output & Drive Current
- Power Dissipation

9.2.2.1 TTL and other Logic Inputs

The TPL7407LA input interface is specified for standard 1.8 V through 5 V CMOS logic interface and can tolerate up to 30 V. At any input voltage the output drivers is going to be driven at its maximum when Vcom is greater than or equal to 6.5 V.

9.2.2.2 Input RC Snubber

The TPL7407LA features an input RC snubber that helps prevent spurious switching in noisy environments. Connect an external 1 kΩ to 5 kΩ resistor in series with the input to further enhance the TPL7407LA's noise tolerance.

9.2.2.3 High-Impedance Input Drivers

The TPL7407LA features a 1-MΩ input pull-down resistor. The presence of this resistor allows the input drivers to be tri-stated. When a high-impedance driver is connected to a channel input the TPL7407LA detects the channel input as a low level input and remains in the OFF position. The input RC snubber helps improve noise tolerance when input drivers are in the high-impedance state.

9.2.2.4 Drive Current

The coil current is determined by the coil voltage (V_{SUP}), coil resistance & output low voltage (V_{OL}) as shown in 式 2.

$$I_{COIL} = (V_{SUP} - V_{OL})/R_{COIL} \quad (2)$$

9.2.2.5 Output Low Voltage

The output low voltage (V_{OL}) is drain to source (V_{DS}) voltage of the output NMOS transistors when the input is driven high and it is sinking current and can be determined by the *Specifications* section or 図 1.

9.2.3 Application Curve

図 10 was generated with TPL7407LA driving an OMRON G5NB relay -- V_{in} = 5 V; V_{sup} = 12 V & R_{COIL} = 2.8 kΩ

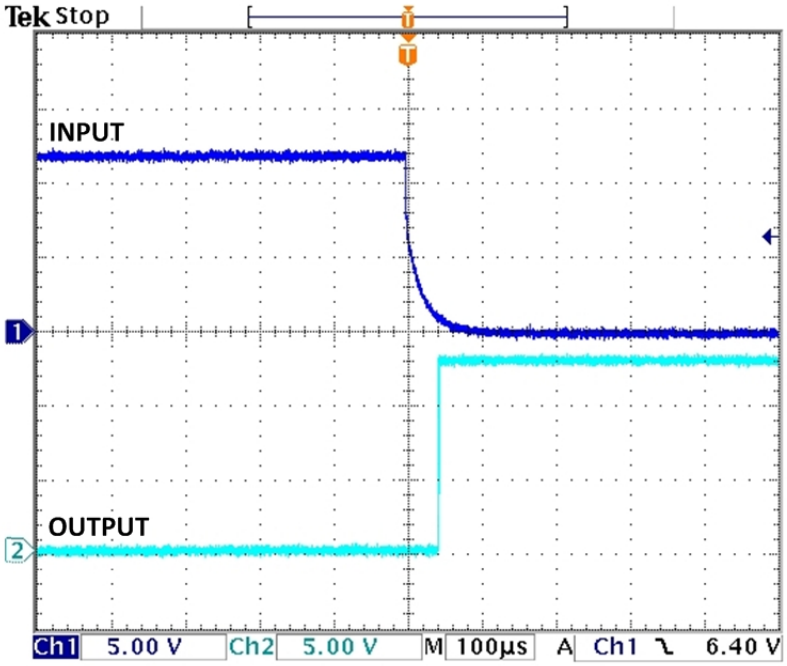


図 10. Output Response With De-Activation of Coil (Turnoff)

10 Power Supply Recommendations

The COM pin is the power supply pin of this device to power the gate drive circuitry. While a bypass capacitor on this pin is recommended for sensitive power supplies, it is not required for proper operation of the device. The COM pin supply ensures full drive potential with any GPIO above 1.5 V. The gate drive circuitry is based on low voltage CMOS transistors that can only handle a max gate voltage of 7 V. An integrated LDO reduces the COM voltage of 6.5 V to 30 V to a regulated voltage of 5.3 V. Though 6.5 V minimum is recommended for Vcom, the part still functions with a reduced COM voltage that has a reduced gate drive voltage and a resulting higher Rdson.

11 Layout

11.1 Layout Guidelines

Thin traces can be used on the input due to the low current logic that is typically used to drive the TPL7407LA. Care must be taken to separate the input channels as much as possible, so as to eliminate cross-talk. Thick traces are recommended for the output, in order to drive whatever high currents that may be needed. Wire thickness can be determined by the trace material's current density and desired drive current.

Since all of the channels currents return to a common ground, it is best to size that trace width to be very wide. Some applications require up to 2 A.

Since the COM pin only draws up to 30 µA, thick traces are not necessary.

11.2 Layout Example

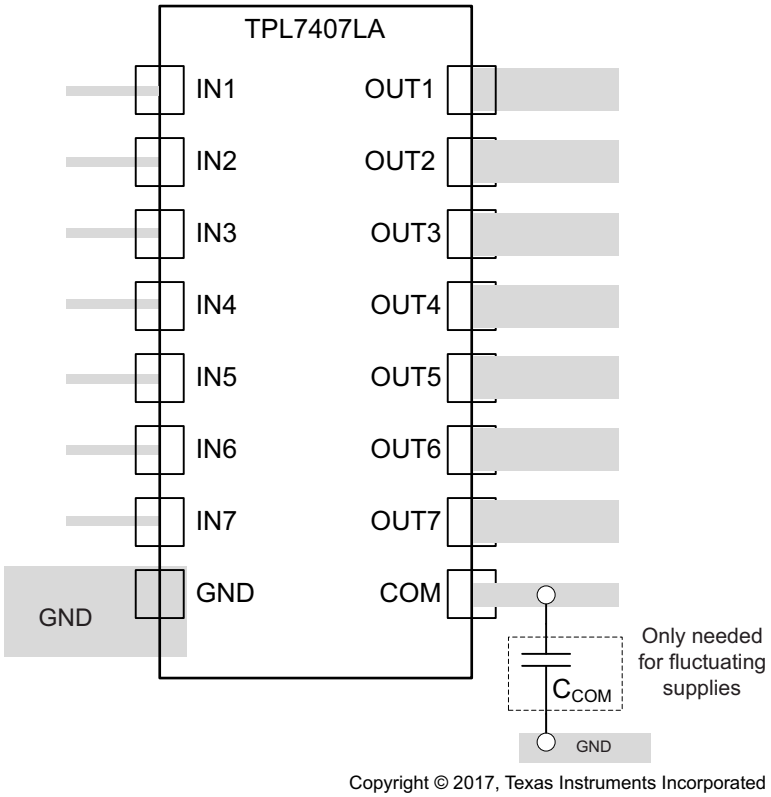


図 11. Package Layout

11.3 Thermal Considerations

The number of coils driven is dependent on the coil current and on-chip power dissipation. The number of coils driven can be determined by 図 3 or 図 4.

For a more accurate determination of number of coils possible, use 式 3 to calculate TPL7407LA on-chip power dissipation P_D:

$$P_D = \sum_{i=1}^{N} V_{OLi} \times I_{Li}$$

where

- N is the number of channels active together
- V_{OLi} is the OUT_i pin voltage for the load current I_{Li}. This is the same as $V_{CE(SAT)}$ (3)

In order to guarantee reliability of TPL7407LA and the system, the on-chip power dissipation must be lower than or equal to the maximum allowable power dissipation ($P_{D(MAX)}$) dictated by below equation 式 4.

$$PD_{(MAX)} = \frac{\left(T_{J(MAX)} - T_A\right)}{\theta_{JA}}$$

where

- $T_{J(MAX)}$ is the target maximum junction temperature
- T_A is the operating ambient temperature
- θ_{JA} is the package junction to ambient thermal resistance (4)

It is recommended to limit rhe TPL7407LA IC's die junction temperature to less than 125°C. The IC junction temperature is directly proportional to the on-chip power dissipation.

11.3.1 Improving Package Thermal Performance

θ_{JA} value depends on the PC board layout. An external heat sink and/or a cooling mechanism, like a cold air fan, can help reduce θ_{JA} and thus improve device thermal capabilities. Refer to TI's design support web page at www.ti.com/thermal for a general guidance on improving device thermal performance.

12 デバイスおよびドキュメントのサポート

12.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E（Engineer-to-Engineer）コミュニティ。*** **エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。**

設計サポート ***TIの設計サポート*** **役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。**

12.3 商標

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

重要なお知らせと免責事項

TI は、技術データと信頼性データ（データシートを含みます）、設計リソース（リファレンス・デザインを含みます）、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションが適用される各種規格や、その他のあらゆる安全性、セキュリティ、またはその他の要件を満たしていることを確実にする責任を、お客様のみが単独で負うものとします。上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件（www.tij.co.jp/ja-jp/legal/termsofsale.html）、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用されるTI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPL7407LADR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	TPL7407LAD	Samples
TPL7407LAPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	TPL747LA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

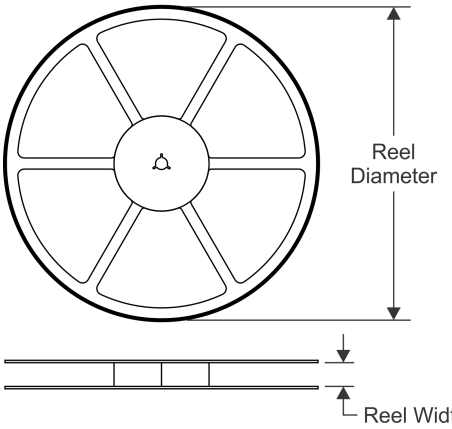
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

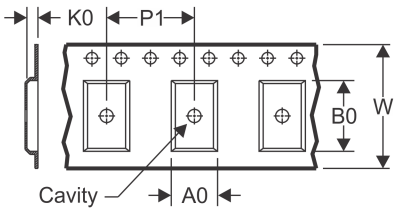
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

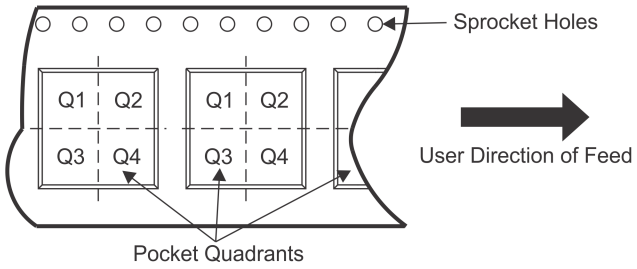


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

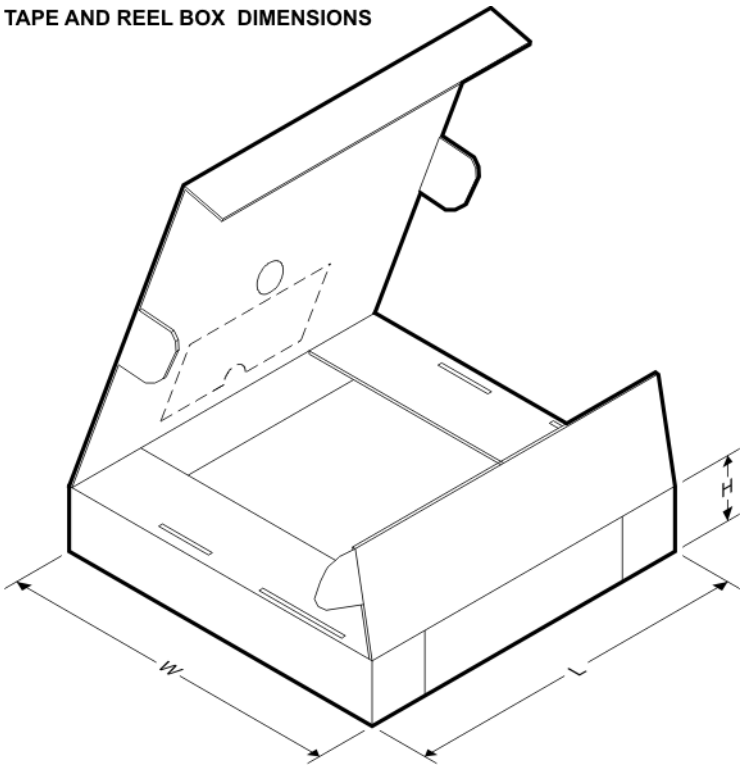
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPL7407LADR	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
TPL7407LAPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

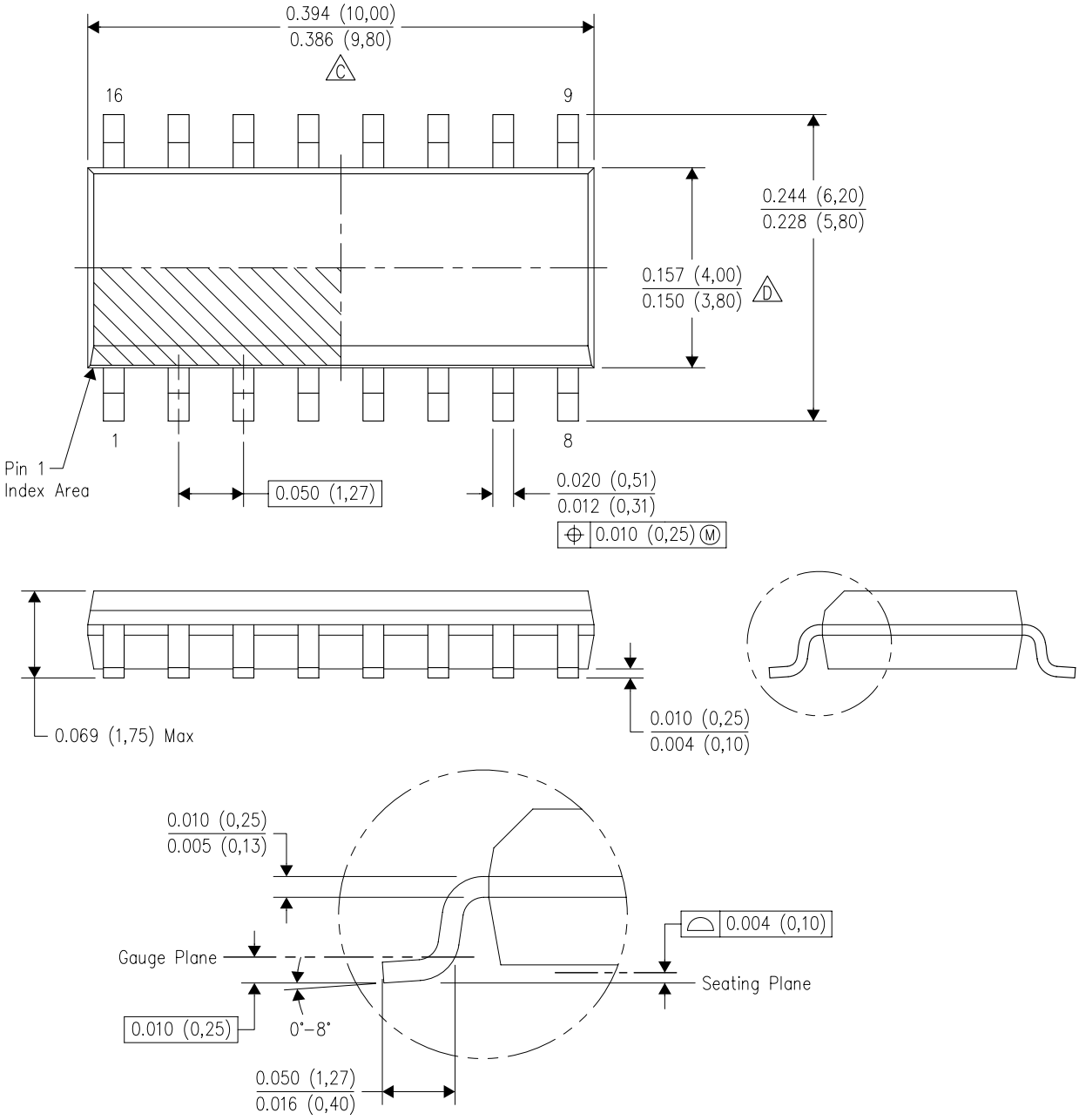
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

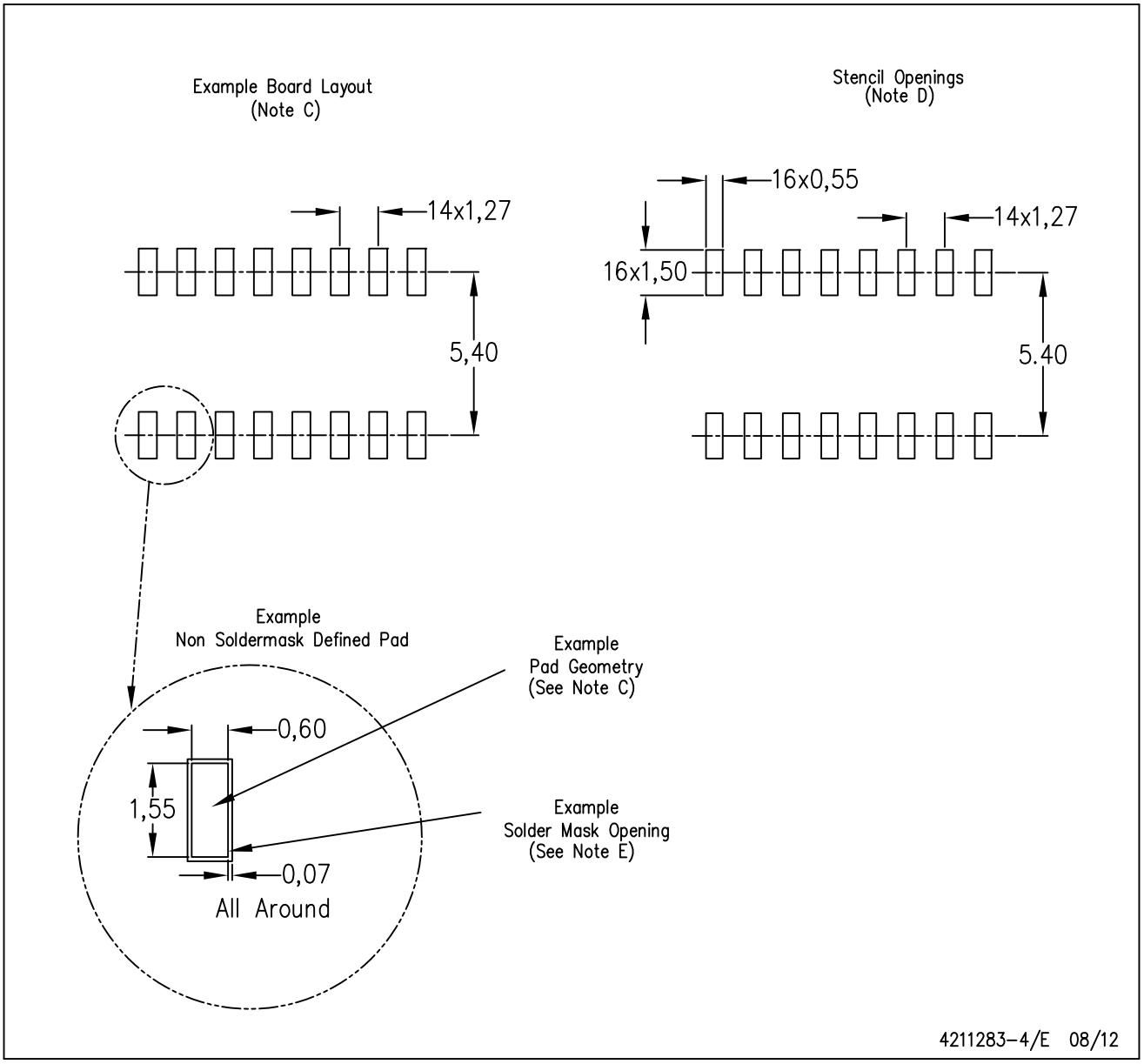
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPL7407LADR	SOIC	D	16	2500	364.0	364.0	27.0
TPL7407LAPWR	TSSOP	PW	16	2000	364.0	364.0	27.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



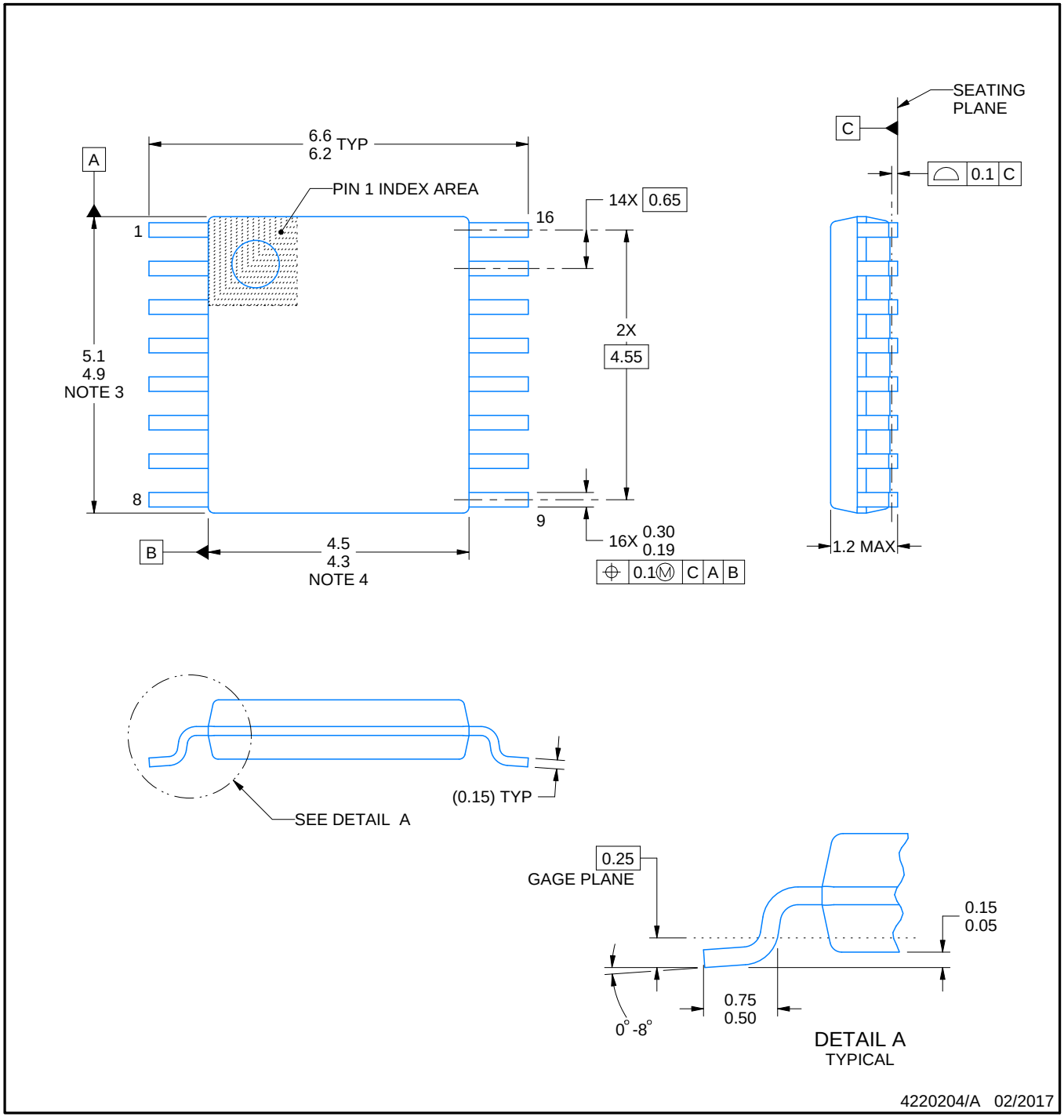
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PW0016A

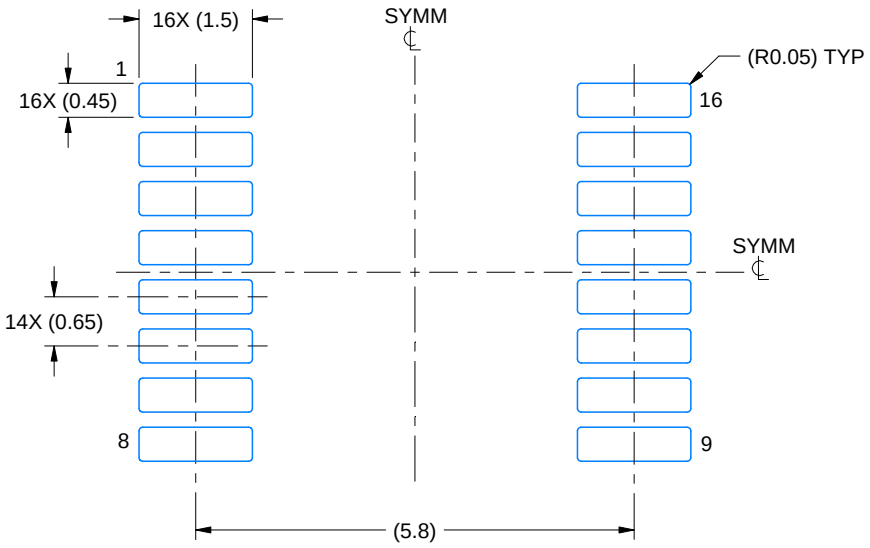
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

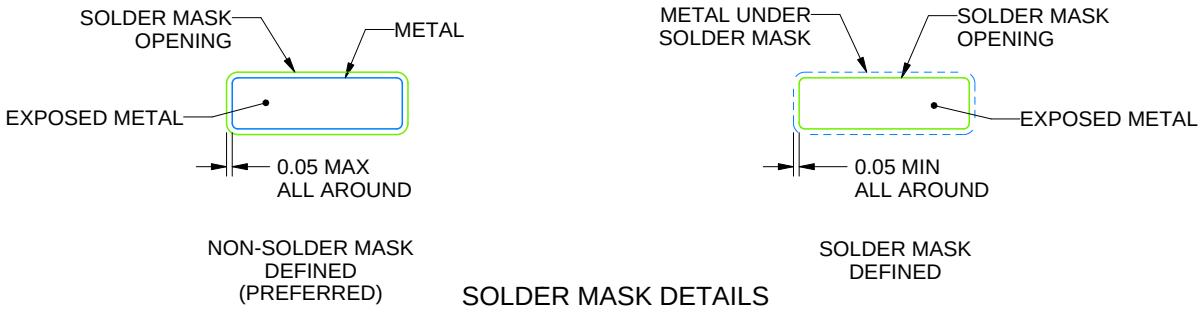


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

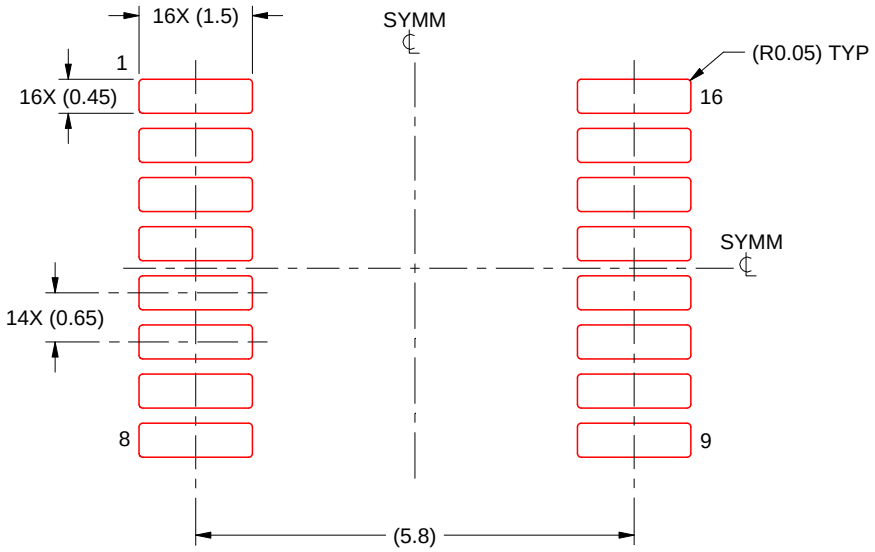


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

TI は、技術データと信頼性データ（データシートを含みます）、設計リソース（リファレンス・デザインを含みます）、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションが適用される各種規格や、その他のあらゆる安全性、セキュリティ、またはその他の要件を満たしていることを確実にする責任を、お客様のみが単独で負うものとします。上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件（www.tij.co.jp/ja-jp/legal/termsofsale.html）、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用されるTI の保証または他の保証の放棄の拡大や変更を意味するものではありません。