TEXAS INSTRUMENTS
TPS2663
JAJSGA2F – SEPTEMBER 2018 – REVISED JUNE 2021

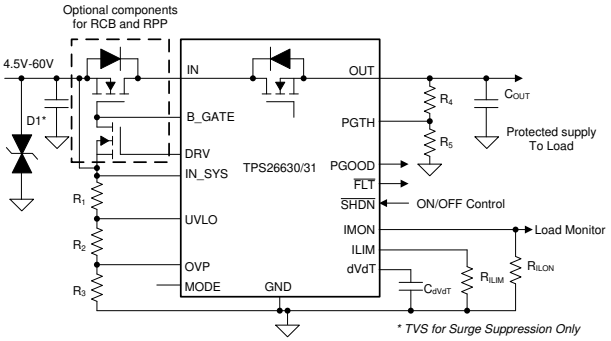
TPS2663x 60V、6A の電力制限、サージ保護の産業用 eFuse

1 特長

- 動作電圧範囲 4.5V～60V、絶対最大定格 67V
- 60V、R_{ON} 31mΩ のホットスワップ FET を内蔵
- 外付けの N チャネル FET で逆極性保護および逆電流ブロックをサポート
- 電流制限を 0.6A～6A に調整可能 (±7%)
- 電気的高速過渡 (IEC61000-4-4) 耐性とサージ時負荷保護 (IEC 61000-4-5) で Class-A のシステム性能
- 高速な逆電流ブロック (0.17µs)
- 可変出力電力制限を備えたバリアント (±6%)
- 可変 UVLO、OVP カットオフ、出力スルー・レート制御による突入電流制限
- デバイス起動中のサーマル・レギュレーションにより大容量および未知の容量性負荷を充電可能
- 35V と 39V の最大過電圧クランプを備えたバリアント
- パワー・グッド出力 (PGOOD)
- 過電流フォルト応答オプションとして、自動再試行とラッチオフを選択可能 (MODE)
- 2 倍のパルス過電流をサポートするバリアント
- アナログ電流モニタ (IMON) 出力 (±6%)
- UL 2367 認定
  - ファイル番号 E169910
  - RILIM ≥ 3kΩ
- IEC 62368-1 認証済み

2 アプリケーション

- ファクトリ・オートメーションおよび制御 - PLC、DCS、HMI、I/O モジュール、センサ・ハブ
- モータ・ドライブ - CNC、エンコーダ電源
- 電子回路ブレーカ



概略回路図

3 概要

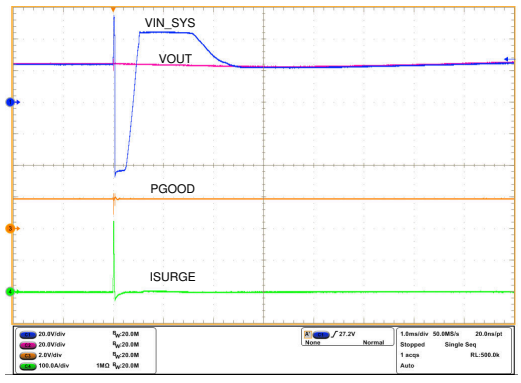
TPS2663x デバイスは、31mΩ の FET を内蔵した使いやすい正の 60V/6A の eFuse です。入力逆極性フォルト保護や逆電流ブロックを必要とするシステム設計において、外付け N チャネル FET を制御するための B-FET ドライバを備えています。このデバイスには堅牢な保護機能が組み込まれ、IEC61000-4-5 産業用サージ・テストなどのシステム・テスト中に保護を必要とするシステム設計を簡素化できます。また、可変出力電力制限 (PLIM) 機能も備え、IEC61010-1 や UL1310 などの規格への準拠を必要とするシステム設計を簡素化できます。それ以外にも、可変の過電流保護、高速な短絡保護、出力スルーレート制御、過電圧保護、低電圧誤動作防止などの保護機能を搭載しています。

システム状態の監視や、下流負荷の制御のため、このデバイスはフォルトおよび高精度の電流監視出力を備えています。PGOOD を使用して、下流の DC-DC コンバータの制御をイネーブル/ディセーブルできます。MODE ピンにより、2 種類の電流制限フォルト応答 (ラッチオフおよび自動再試行) のどちらにもデバイスを柔軟に設定できます。

デバイス情報(1)

部品番号	パッケージ	本体サイズ (公称)
TPS26630 TPS26631 TPS26632 TPS26633 TPS26635	VQFN (24)	4.00mm × 4.00mm
TPS26631 TPS26633 TPS26636	HTSSOP (20)	6.50mm × 4.40mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



24V 電源での IEC61000-4-5 サージ性能

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision E (March 2020) to Revision F (June 2021) — **Page**

- 文書全体にわたって表、図、相互参照の採番方法を更新 ... 1

Changes from Revision D (August 2019) to Revision E (March 2020) — **Page**

- UL 2367 を「認定待ち」から「認定済み」に変更 ... 1
- 「*特長*」セクションに IEC 62368-1 認証を追加 ... 1

Changes from Revision C (March 2019) to Revision D (August 2019) — **Page**

- 「*製品情報*」表の TPS26632 を TPS26636 に置換 ... 1
- Added the TPS26636 device to the *Pin Configuration and Functions* table ... 3
- Added the TPS26636 device to the *Pin Functions* table ... 3
- Updated the Input Voltage in the *Absolute Maximum Ratings* table ... 6
- Updated the PLIM Input and Output Ramp Control in the *Electrical Characteristics* table ... 7

Changes from Revision B (January 2019) to Revision C (March 2019) — **Page**

- 事前情報から量産データに変更 ... 1

Changes from Revision A (December 2018) to Revision B (January 2019) — **Page**

- Updated the *Pin Configuration and Functions* section ... 3
- Updated *Layout Example* ... 40

Changes from Revision * (September 2018) to Revision A (December 2018) — **Page**

- Updated the *Pin Configuration and Functions* section ... 3
- Updated *Functional Block Diagram* ... 17
- Updated *Layout Example* ... 40

5 Device Comparison Table

PART NUMBER	OVERVOLTAGE PROTECTION	OVERLOAD FAULT RESPONSE	ADJUSTABLE OUTPUT POWER LIMITING
TPS26630	Overvoltage cut-off, adjustable	Active Current Limiting (1x)	No
TPS26631	Overvoltage cut-off, adjustable	Active Current Limiting with Pulse current support (2x)	No
TPS26632	Overvoltage clamp, fixed (35-V max)	Active Current Limiting (1x)	Yes
TPS26633	Overvoltage clamp, fixed (35-V max)	Active Current Limiting with Pulse current support (2x)	Yes
TPS26635	Overvoltage clamp, fixed (39-V max)	Active Current Limiting with Pulse current support (2x)	Yes
TPS26636	Overvoltage clamp, fixed (35-V max)	Active Current Limiting with Pulse current support (2x)	Yes

6 Pin Configuration and Functions

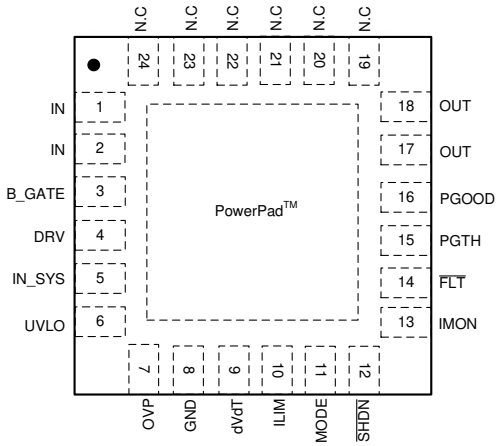


図 6-1. TPS26630, TPS26631 RGE Package 24-Pin VQFN Top View

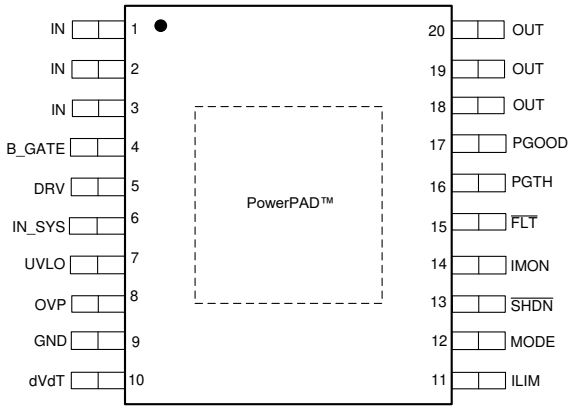


図 6-2. TPS26631 PWP Package 20-Pin HTSSOP Top View

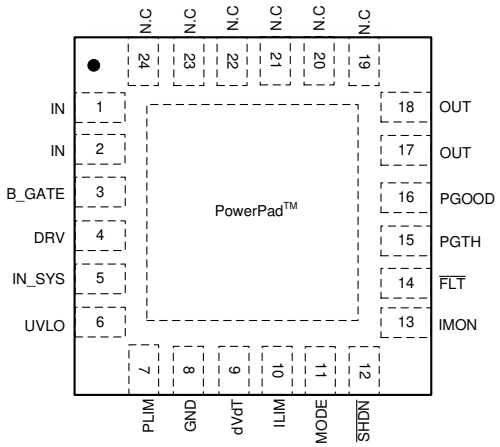


図 6-3. TPS26632, TPS26633, TPS26635 RGE Package 24-Pin VQFN Top View

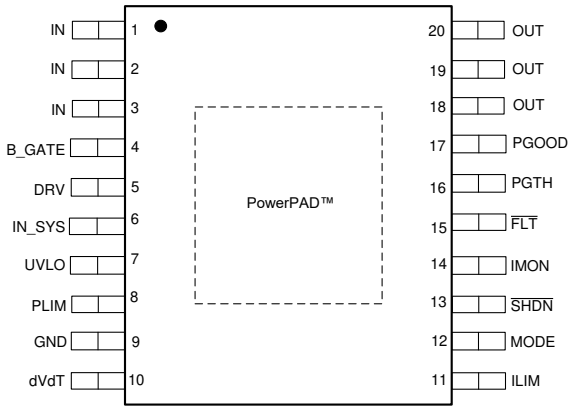


図 6-4. TPS26633, TPS26636 PWP Package 20-Pin HTSSOP Top View

表 6-1. Pin Configuration and Functions

PIN			TYPE	DESCRIPTION
NAME	TPS26630, TPS26631, TPS26632, TPS26633, TPS26635, TPS26636			
	VQFN	HTSSOP		
IN	1	1	P	Power input. Connects to the DRAIN of the internal FET
	2	2		
	—	3		
B_GATE	3	4	O	Blocking FET gate driver output. Connect B_GATE to GATE of the external NFET. If external FET is not used then leave B_GATE pin floating. See the *Input Reverse Polarity Protection (B_GATE, DRV)* section.
DRV	4	5	O	Blocking FET fast pull down switch drive. Connect DRV to the GATE of external pull down switch. Leave this pin floating if external N-FET is not used.
IN_SYS	5	6	P	Power input and supply voltage of the device. When an external Blocking FET is used then connect IN_SYS to source of the FET. Short IN_SYS to IN in case blocking FET is not used.
UVLO	6	7	I	Input for setting the programmable undervoltage lockout threshold. An undervoltage event turns off the internal FET and asserts $\overline{FLT}$ to indicate the power-failure. Connect UVLO pin to GND pin to select the internal default threshold.
OVP	7	8	I	Input for setting the programmable overvoltage protection threshold (For TPS26630 and TPS26631 Only). An overvoltage event turns off the internal FET and asserts $\overline{FLT}$ to indicate the overvoltage fault. Connect OVP pin to GND pin externally to select the internal default threshold.
PLIM	7	8	I	Input for setting the programmable output power limiting threshold (For TPS26632, TPS26633, TPS26635 and TPS26636 Only). Connect a resistor across PLIM to GND to set the output power limit. Connect PLIM to GND if PLIM feature is not used. See the *tput power limit. Connect PLIM to GND if PLIM feature is not used. See the Output Power Limiting, PLIM (TPS26632, TPS26633, TPS26635 and TPS26636 Only)* section.
GND	8	9	—	Connect GND to system ground
dVdT	9	10	I/O	A capacitor from this pin to GND sets output voltage slew rate. See the *Hot Plug-In and In-Rush Current Control* section.
ILIM	10	11	I/O	A resistor from this pin to GND sets the overload and short-circuit current limit. See the *Overload and Short Circuit Protection* section.
MODE	11	12	I	Mode selection pin for overload fault response. See the *Device Functional Modes* section.
$\overline{SHDN}$	12	13	I	Shutdown pin. Pulling $\overline{SHDN}$ low makes the device to enter into low power shutdown mode. Cycling $\overline{SHDN}$ pin voltage resets the device that has latched off due to a fault condition.
IMON	13	14	O	Analog current monitor output. This pin sources a scaled down ratio of current through the internal FET. A resistor from this pin to GND converts current to proportional voltage. If unused, leave it floating.
$\overline{FLT}$	14	15	O	Fault event indicator. It is an open drain output. If unused, leave floating or connect to GND.
PGTH	15	16	I	PGOOD comparator input.
PGOOD	16	17	O	Active High. A high indicates PGTH has crossed the $V_{(PGTHR)}$ threshold and the internal FET is enhanced. PGOOD goes low when $V_{(PGTH)}$ hits $V_{(PGTHF)}$ threshold. If PGOOD is unused then connect to GND or leave it floating.
OUT	17	18	P	Power output of the device
	18	19		
	—	20		

表 6-1. Pin Configuration and Functions (continued)

PIN			TYPE	DESCRIPTION
NAME	TPS26630, TPS26631, TPS26632, TPS26633, TPS26635, TPS26636			
	VQFN	HTSSOP		
N. C	19	—	—	No Connect
	20			
	21			
	22			
	23			
	24			
PowerPad™	—	—	—	Connect PowerPad to GND plane for heat sinking. Do not use PowerPad as the only electrical connection to GND.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
IN_SYS	Input Voltage	–60	67	V
IN_SYS (10ms transient), T_A = 25 ℃		–60	75	V
IN, OUT, UVLO, $\overline{FLT}$, PGOOD, PGTH		–0.3	67	V
IN_SYS – OUT (10ms transient), with a Blocking FET		–85		V
IN (10ms transient), T_A = 25 ℃		–0.3	75	V
BGATE		–60	81	V
BGATE – IN_SYS		–0.3	14	V
DRV		–60	72	V
DRV – IN_SYS		–0.3	20	V
OVP, dVdT, IMON, MODE, $\overline{SHDN}$, ILIM, PLIM		–0.3	5.5	V
$I_{\overline{FLT}}$, I_{dVdT}, I_{PGOOD}	Sink current		10	mA
I_{dVdT}, I_{ILIM}, I_{PLIM}, I_{MODE}, $I_{\overline{SHDN}}$	Source current	Internally limited		
T_J	Operating Junction temperature	–40	150	°C
	Transient junction temperature	–65	$T_{(TSD)}$	
T_{stg}	Storage temperature	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
IN_SYS, IN	Input Voltage	4.5		60	V
OUT, UVLO, PGTH, PGOOD, $\overline{FLT}$		0		60	
OVP, dVdT, IMON, MODE		0		4	
$\overline{SHDN}$		0		5	
ILIM	Resistance	3		30	kΩ
IMON	Resistance	1			
PLIM	Resistance	60.4		150	
IN, IN_SYS, OUT	External Capacitance	0.1			µF
dVdT		10			nF
T_J	Operating Junction temperature	–40	25	125	°C

7.4 Thermal Information

THERMAL METRIC[1]		TPS2663		UNIT
		RGE (VSON)	PWP (HTSSOP)	
		24 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.4	32.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	23.2	23.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	10.2	10	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	10.2	9.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.8	3.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

–40°C ≤ T_A = T_J ≤ +125°C, 4.5 V < $V_{(IN\_SYS)}$ = $V_{(IN)}$ < 60 V, $V_{(\overline{SHDN})}$ = 2 V, $R_{(ILIM)}$ = 30 kΩ, IMON = PGOOD = $\overline{FLT}$ = OPEN, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN. (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
$V_{(IN\_SYS)}$	Operating input voltage		4.5		60	V
$IQ_{(ON)}$	Supply current	Enabled: $V_{(\overline{SHDN})}$ = 2 V		1.38	1.7	mA
$IQ_{(OFF)}$		$V_{(\overline{SHDN})}$ = 0 V		21	60	µA
$I_{(GND)}$	Ground current during reverse polarity	$V_{(IN\_SYS)}$ = –24V, $V_{(IN)}$ = Floating, $V_{(OUT)}$ = 0 V		144	200	µA
$V_{(OVC)}$	Over voltage clamp	TPS26632, TPS26633, TPS26636 Only, $V_{(IN\_SYS)}$ > 35 V, $I_{(OUT)}$ = 1 mA	32	32.8	35	V
		TPS26635 Only, $V_{(IN\_SYS)}$ > 40 V, $I_{(OUT)}$ = 1 mA	35.7	36.6	39	V
UNDERVOLTAGE LOCKOUT (UVLO) INPUT						
$V_{(INSYS\_UVLO)}$	Factory set $V_{(IN\_SYS)}$ undervoltage trip level trip level	$V_{(IN\_SYS)}$ rising, $V_{(UVLO)}$ = 0 V	15.1	15.46	15.9	V
		$V_{(IN\_SYS)}$ falling, $V_{(UVLO)}$ = 0 V	14	14.47	15.1	V
$V_{(SEL\_UVLO)}$	Internal UVLO select threshold		180	210	240	mV
$V_{(UVLOR)}$	UVLO threshold voltage, rising		1.176	1.2	1.224	V
$V_{(UVLOF)}$	UVLO threshold voltage, falling		1.09	1.122	1.15	V
$I_{(UVLO)}$	UVLO Input leakage current	0 V ≤ $V_{(UVLO)}$ ≤ 60 V	–150	8	150	nA
OVERVOLTAGE PROTECTION (OVP) INPUT						
$V_{(IN\_SYS\_OVP)}$	Factory set $V_{(IN\_SYS)}$ overvoltage trip level trip level	$V_{(IN\_SYS)}$ rising, $V_{(OVP)}$ = 0 V	33.2	34.33	35.4	V
		$V_{(IN\_SYS)}$ falling, $V_{(OVP)}$ = 0 V	32.7	33.89	35	V
$V_{(SEL\_OVP)}$	Internal OVP select threshold		180	210	240	mV
$V_{(OVPR)}$	over-voltage threshold voltage, rising		1.176	1.2	1.224	V
$V_{(OVPF)}$	over-voltage threshold voltage, falling		1.09	1.122	1.15	V
$I_{(OVP)}$	OVP Input leakage current	0 V ≤ $V_{(OVP)}$ ≤ 4 V	–150	0	150	nA
CURRENT LIMIT PROGRAMMING (ILIM)						
$I_{(OL)}$	Over Load current limit	$R_{(ILIM)}$ = 30 kΩ, $V_{(IN)}$ – $V_{(OUT)}$ = 1 V	0.54	0.6	0.66	A
		$R_{(ILIM)}$ = 9 kΩ, $V_{(IN)}$ – $V_{(OUT)}$ = 1 V	1.84	2	2.16	A
		$R_{(ILIM)}$ = 4.02 kΩ, $V_{(IN)}$ – $V_{(OUT)}$ = 1 V	4.185	4.5	4.815	A
		$R_{(ILIM)}$ = 3 kΩ, $V_{(IN)}$ – $V_{(OUT)}$ = 1 V	5.58	6	6.42	A
$I_{(OL\_Pulse)}$	Transient Pulse Over current limit	3 kΩ < $R_{(ILIM)}$ < 30 kΩ, TPS26631, TPS26633, TPS26635 and TPS26636 Only		2x$I_{(OL)}$		A

7.5 Electrical Characteristics (continued)

–40°C ≤ T_A = T_J ≤ +125°C, 4.5 V < $V_{(IN\_SYS)}$ = $V_{(IN)}$ < 60 V, $V_{(\overline{SHDN})}$ = 2 V, $R_{(ILIM)}$ = 30 kΩ, IMON = PGOOD = $\overline{FLT}$ = OPEN, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN. (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(FASTRIP)}$	Fast-trip comparator threshold	TPS26630 and TPS26632 Only		2x$I_{(OL)}$		A
$I_{(FASTRIP)}$	Fast-trip comparator threshold	TPS26631, TPS26633,TPS26635 and TPS26636 Only		3x$I_{(OL)}$		A
$I_{(SCP)}$	Short Circuit Protect current			45		A
OUTPUT POWER LIMITING CONTROL (PLIM) INPUT – TPS26632, TPS26633, TPS26635 and TPS26636 ONLY						
$V_{(SEL\_PLIM)}$	Power Limit Feature select threshold		160	217	240	mV
$I_{(PLIM)}$	PLIM sourcing current	$V_{(PLIM)}$ = 0 V	4.4	5.02	5.6	µA
$P_{(PLIM)}$	Max Output power	$R_{(PLIM)}$ = 100 kΩ	94	100	106	W
		$R_{(PLIM)}$ = 150 kΩ (1)	141.9	151	160.1	W
B_GATE (BLOCKING FET GATE DRIVER)						
$V_{(B\_GATE)}$	B_GATE clamp voltage	$V_{(B\_GATE)}$ – $V_{(IN\_SYS)}$	8.3	10.23	14	V
$I_{(B\_GATE)}$	Blocking FET Gate drive current	$V_{(B\_GATE)}$ – $V_{(IN\_SYS)}$ = 1 V	16	19.4	23	µA
Rpd_BGATE	B_GATE Pull down resistance		800	1010	1200	kΩ
$V_{(DRV\_OH)}$	DRV logic high level	$V_{(DRV)}$ – $V_{(IN\_SYS)}$, $C_{(DRV)}$ ≤ 50 pF	3	4.25	5.2	V
PASS FET OUTPUT (OUT)						
R_{ON}	IN to OUT total ON resistance	0.6 A ≤ $I_{(OUT)}$ ≤ 6 A,T_J = 25°C	26	30.44	34.5	mΩ
R_{ON}	IN to OUT total ON resistance	0.6 A ≤ $I_{(OUT)}$ ≤ 6 A,T_J = 85°C	33		45	mΩ
R_{ON}	IN to OUT total ON resistance	0.6 A ≤ $I_{(OUT)}$ ≤ 6 A, –40°C ≤ T_J ≤ +125°C	19	30.44	53	mΩ
$I_{lkg(OUT)}$	OUT leakage during input supply brownout	$V_{(IN\_SYS)}$ = 0 V, $V_{(OUT)}$ = 24 V, $V_{(IN)}$ = Floating, $V_{(\overline{SHDN})}$ = 2V, Sinking	–100			µA
$V_{(REVTH)}$	$V_{(IN\_SYS)}$ – $V_{(OUT)}$ threshold for reverse protection comparator, rising		–20	–15	–9	mV
$V_{(FWDTH)}$	$V_{(IN\_SYS)}$ – $V_{(OUT)}$ threshold for reverse protection comparator, falling		45	57	67	mV
OUTPUT RAMP CONTROL (dVdT)						
$I_{(dVdT)}$	dVdT charging current	$V_{(dVdT)}$ = 0 V	1.775	2	2.225	µA
$GAIN_{(dVdT)}$	dVdT to OUT gain	$V_{(OUT)}$ /$V_{(dVdT)}$	23.5	25	26	V/V
$V_{(dVdTmax)}$	dVdT maximum capacitor voltage		3.8	4.17	4.75	V
$R_{(dVdT)}$	dVdT discharging resistance		10	16.6	26.6	Ω
LOW IQ SHUTDOWN ($\overline{SHDN}$) INPUT						
$V_{(\overline{SHDN})}$	Open circuit voltage	$I_{(\overline{SHDN})}$ = 0.1 µA	2.48	2.7	3.3	V
$V_{(SHUTF)}$	$\overline{SHDN}$ threshold voltage for low IQ shutdown, falling		0.8			V
$V_{(SHUTR)}$	$\overline{SHDN}$ threshold rising				2	V
$I_{(\overline{SHDN})}$	Leakage current	$V_{(\overline{SHDN})}$ = 0 V	–10			µA
CURRENT MONITOR OUTPUT (IMON)						
$GAIN_{(IMON)}$	Gain factor $I_{(IMON)}$:$I_{(OUT)}$	0.6 A ≤ $I_{(OUT)}$ ≤ 2 A	25.66	27.9	30.14	µA/A
		2 A ≤ $I_{(OUT)}$ ≤ 6 A	26.22	27.9	29.58	µA/A
FAULT FLAG ($\overline{FLT}$): ACTIVE LOW						
$R_{(\overline{FLT})}$	$\overline{FLT}$ Pull-down resistance		36	70	130	Ω
$I_{(\overline{FLT})}$	$\overline{FLT}$ Input leakage current	0 V ≤ $V_{(\overline{FLT})}$ ≤ 60 V	–150	6	150	nA
POWER GOOD (PGOOD)						
$R_{(PGOOD)}$	PGOOD Pull-down resistance		36	70	130	Ω
$I_{(PGOOD)}$	PGOOD Input leakage current	0 V ≤ $V_{(PGOOD)}$ ≤ 60 V	–150		150	nA

7.5 Electrical Characteristics (continued)

–40°C ≤ T_A = T_J ≤ +125°C, 4.5 V < $V_{(IN\_SYS)}$ = $V_{(IN)}$ < 60 V, $V_{(\overline{SHDN})}$ = 2 V, $R_{(ILIM)}$ = 30 kΩ, IMON = PGOOD = $\overline{FLT}$ = OPEN, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN. (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POSITIVE INPUT FOR POWER GOOD COMPARATOR (PGTH)						
$V_{(PGTHR)}$	PGTH threshold voltage, rising		1.176	1.2	1.224	V
$V_{(PGTHF)}$	PGTH threshold voltage, falling		1.09	1.123	1.15	V
$I_{(PGOOD)}$	PGTH input leakage current	0 V ≤ $V_{(PGTH)}$ ≤ 60 V	–150		150	nA
THERMAL PROTECTION						
$T_{(J\_REG)}$	Thermal regulation set point		136	145	154	°C
$T_{(TSD)}$	Thermal shutdown (TSD) threshold, rising			165		°C
$T_{(TSDhyst)}$	TSD hysteresis			11		°C
MODE						
MODE_SEL	Mode selection	MODE = Open		Latch		
		MODE = Short to GND		Auto – Retry		

(1) Parameter guaranteed by design and characterization, not tested in production

7.6 Timing Requirements

–40°C ≤ T_A = T_J ≤ +125°C, 4.5 V < $V_{(IN\_SYS)}$ = $V_{(IN)}$ < 60 V, $V_{(\overline{SHDN})}$ = 2 V, $R_{(ILIM)}$ = 30 kΩ, IMON = PGOOD = $\overline{FLT}$ = OPEN, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN. (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
UVLO INPUT (UVLO)						
UVLO_$t_{on(dly)}$	UVLO switch turnon delay	UVLO ↑ (100 mV above $V_{(UVLOR)}$) to $V_{(OUT)}$ = 100 mV with $V_{(PGTH}$ < $V_{(PGTHF)}$, $C_{(dVdT)}$ ≥ 10 nF, [$C_{(dVdT)}$ in nF]		742 + 49.5 x $C_{(dVdT)}$		µs
UVLO_$t_{on(fast_dly)}$	UVLO switch turnon delay (fast)	UVLO ↑ (100 mV above $V_{(UVLOR)}$) to FET ON with $V_{(PGTH)}$ > $V_{(PGTHF)}$	70	150	251	µs
UVLO_$t_{off(dly)}$	UVLO switch turnoff delay	UVLO ↓ (20 mV below $V_{(UVLOF)}$) to $\overline{FLT}$ ↓	9	11	16	µs
$t_{UVLO\_FLTdly)}$	UVLO to fault de-assertion delay	UVLO ↑ to $\overline{FLT}$ ↑ delay	500	617	700	µs
OVER VOLTAGE PROTECTION INPUT (OVP)						
OVP_$t_{OFF(dly)}$	OVP switch turnoff delay	OVP ↑ (20 mV above $V_{(OVPR)}$) to $\overline{FLT}$ ↓	8.5	11	14	µs
OVP_$t_{on(fast_dly)}$	OVP switch turnon delay (fast)	OVP ↓ (100 mV below $V_{(OVPF)}$) to FET ON with $V_{(PGTH\ )}$ > $V_{(PGTHF)}$	58	129	225	µs
OVP_$t_{on(dly)}$	OVP switch disable delay	OVP ↓ (100 mV below $V_{(OVPF)}$) to FET ON with $V_{(PGTH\ )}$ < $V_{(PGTHF)}$, $C_{(dVdT)}$ ≥ 10 nF, [$C_{(dVdT)}$ in nF]		150 + 49.5 x $C_{(dVdT)}$		µs
$t_{OVC(dly)}$	Maximum duration in over voltage clamp operation	TPS26632, TPS26633,TPS26635 and TPS26636 Only		162		ms
OVC_$t_{FLT(dly)}$	$\overline{FLT}$ assertion delay in over voltage clamp operation	TPS26632, TPS26633,TPS26635 and TPS26636 Only		617		µs
SHUTDOWN CONTROL INPUT ($\overline{SHDN}$)						
$t_{SD(dly)}$	SHUTDOWN entry delay	$\overline{SHDN}$ ↓ (below $V_{(SHUTF)}$) to FET OFF	0.8	1	1.5	µs
CURRENT LIMIT						
$t_{FASTTRIP(dly)}$	Hot-short response time	$I_{(OUT)}$ > $I_{(SCP)}$		1		µs
	Soft short response	$I_{(FASTTRIP)}$ < $I_{(OUT)}$ < $I_{(SCP)}$	2.2	3.2	4.5	µs

7.6 Timing Requirements (continued)

–40°C ≤ T_A = T_J ≤ +125°C, 4.5 V < $V_{(IN\_SYS)}$ = $V_{(IN)}$ < 60 V, $V_{(\overline{SHDN})}$ = 2 V, $R_{(ILIM)}$ = 30 kΩ, IMON = PGOOD = $\overline{FLT}$ = OPEN, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN. (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{CL\_PLIM(dly)}$	Maximum duration in current & (power limiting: TPS26632, TPS26633, TPS26635 and TPS26636 Only)		129	162	202	ms
$t_{CB(dly)}$	Maximum duration in 2x current limiting	$I_{(OL)}$ < $I_{(OUT)}$ ≤ $I_{(2xOL)}$	20	25.5	31	ms
$t_{CBRetry(dly)}$	Retry delay in Pulse over current limiting	MODE = GND, TPS26631, TPS26633,TPS26635 and TPS26636 Only	550	670	800	ms
$t_{CL\_PLIM\_FLT(dly)}$	$\overline{FLT}$ delay in current & (power limiting: TPS26632, TPS26633, TPS26635 and TPS26636 Only)		1.09	1.3	1.6	ms
REVERSE CURRENT BLOCKING (RCB) COMPARATOR						
$t_{RCB(fast\_dly)}$	Reverse protection comparator dectection delay (reverse)	($V_{(IN\_SYS)}$ – $V_{(OUT)}$) ↓ (1 V overdrive below $V_{(REVTH)}$) to $V_{(DRV)}$ – $V_{(IN\_SYS)}$ = $V_{(DRV\_OH)}$		0.17	0.37	µs
$t_{RCB(dly)}$		($V_{(IN\_SYS)}$ – $V_{(OUT)}$)) ↓ (10 mV overdrive below $V_{(REVTH)}$) to $V_{(DRV)}$ – $V_{(IN\_SYS)}$ = $V_{(DRV\_OH)}$		0.48	3	µs
$t_{RCB(flt\_dly)}$	Fault assertion Delay	($V_{(IN\_SYS)}$ – $V_{(OUT)}$) ↓ (10 mV overdrive below $V_{(REVTH)}$) to $\overline{FLT}$ ↓	500	617	800	µs
$t_{FWD\_FLT(dly)}$	Reverse protection comparator dectection delay (forward)	($V_{(IN\_SYS)}$ – $V_{(OUT)}$) ↑ (10 mV overdrive above $V_{(FWDTH)}$) to $V_{(BGATE)}$ – $V_{(IN\_SYS)}$ = 5 V, $C_{(BFET\text{-}IN\_SYS)}$ = 4.7 nF		0.87		ms
	Fault de-assertion Delay	($V_{(IN\_SYS)}$ – $V_{(OUT)}$) ↑ (10 mV overdrive above $V_{(FWDTH)}$) to $\overline{FLT}$ ↑	434	605	800	µs
OUTPUT RAMP CONTROL (dVdT)						
$t_{(FASTCHARGE)}$	Output ramp time in fast charging	$C_{(dVdT)}$ = Open, 10% to 90% $V_{(OUT)}$, $C_{(OUT)}$ = 1 µF; $V_{(IN)}$ = 24V	350	495	700	µs
$t_{(dVdT)}$	Output ramp time	$C_{(dVdT)}$ = 22 nF, 10% to 90% $V_{(OUT)}$, $V_{(IN)}$ = 24V		8.35		ms
POWER GOOD (PGOOD)						
t_{PGOODR}	PGOOD delay (deglitch) time	Rising edge	1.07	1.3	1.6	ms
t_{PGOODF}	PGOOD delay (deglitch) time	Falling edge, PGTH ↓ (10mV below $V_{(PGTHF)}$)	1.3	2.12	4	µs
FAULT FLAG ($\overline{FLT}$)						
$t_{CB\_FLT(dly)}$	$\overline{FLT}$ assertion delay in Pulse over current limiting	Delay from $I_{(OUT)}$ > $I_{(OL)}$ to $\overline{FLT}$ ↓ . TPS26631, TPS26633, TPS26635 and TPS26636 Only	22	25.5	30	ms
THERMAL PROTECTION						
$t_{(TSD\_retry)}$	Retry delay in TSD	MODE = GND	500	648	800	ms
$t_{(Treg\_timeout)}$	Thermal Regulation Timeout		2.3	2.54	2.9	s

7.7 Typical Characteristics

–40°C ≤ T_A = T_J ≤ +125°C, $V_{(IN\_SYS)}$ = $V_{(IN)}$ = 24 V, $V_{(\overline{SHDN})}$ = 2 V, $R_{(ILIM)}$ = 30 kΩ, IMON = PGOOD = $\overline{FLT}$ = OPEN, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN. (Unless stated otherwise)

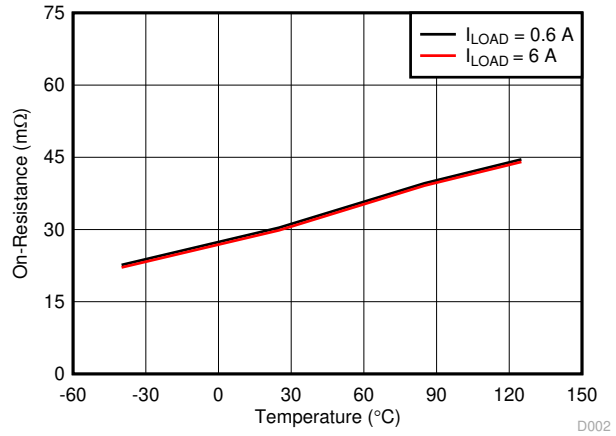


図 7-1. On-Resistance vs Temperature Across Load Current

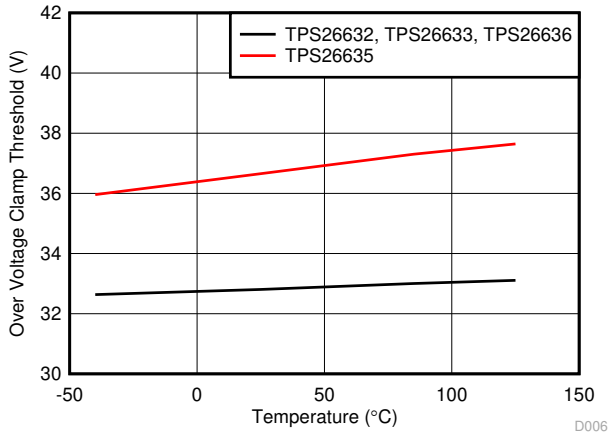


図 7-2. Overvoltage Clamp Threshold vs Temperature

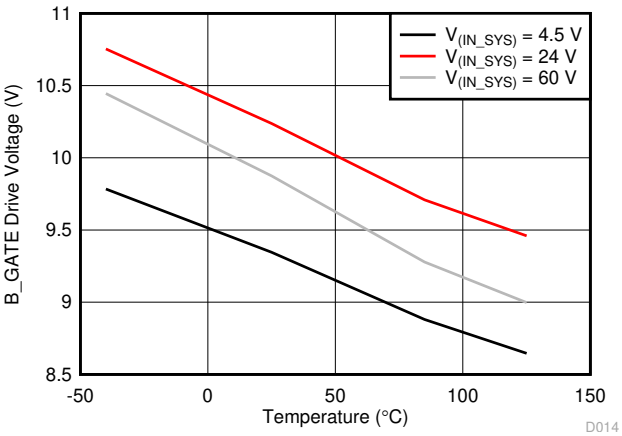


図 7-3. B_GATE Drive Voltage vs Temperature

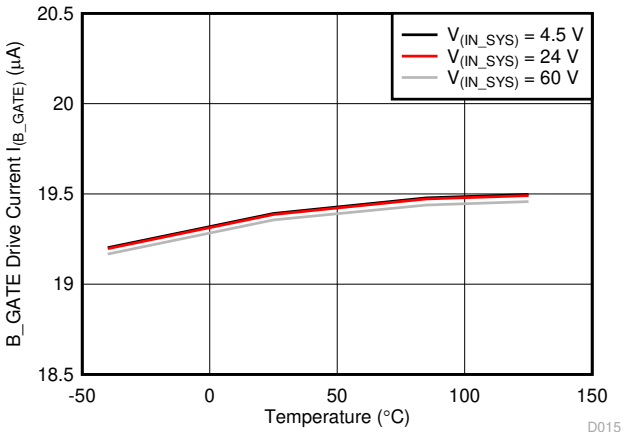


図 7-4. B_GATE Drive Current vs Temperature

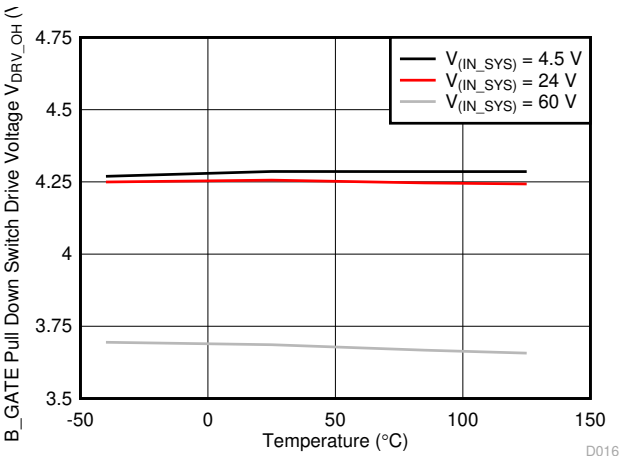


図 7-5. B_GATE Pull Down Drive Voltage vs Temperature

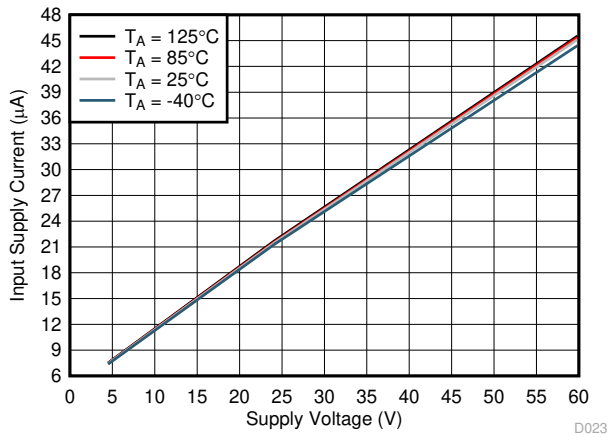


図 7-6. Input Supply Current vs Supply Voltage in Shutdown

7.7 Typical Characteristics (continued)

–40°C ≤ T_A = T_J ≤ +125°C, $V_{(IN\_SYS)}$ = $V_{(IN)}$ = 24 V, $V_{(\overline{SHDN})}$ = 2 V, $R_{(ILIM)}$ = 30 kΩ, IMON = PGOOD = $\overline{FLT}$ = OPEN, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN. (Unless stated otherwise)

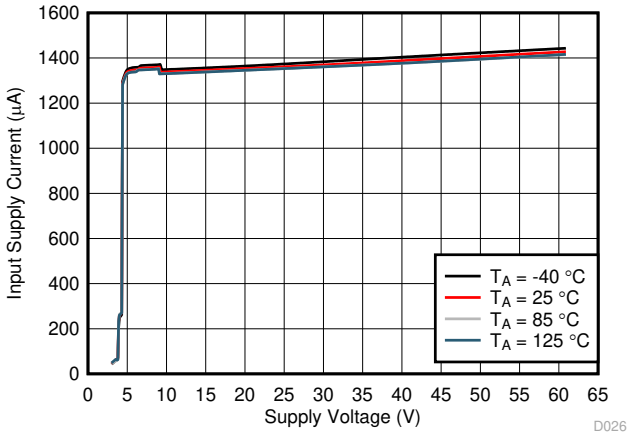
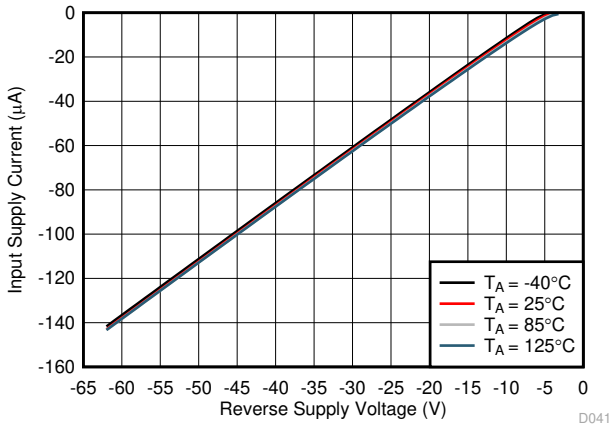


図 7-7. Input Supply Current vs Supply Voltage During Normal Operation



$V_{(OUT)}$ = 0 V

図 7-8. Input Supply Current vs Reverse Supply Voltage, – $V_{(IN\_SYS)}$

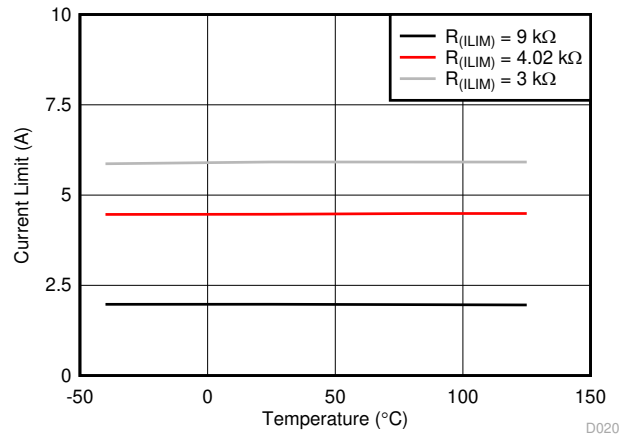


図 7-9. Overload Current Limit vs Temperature

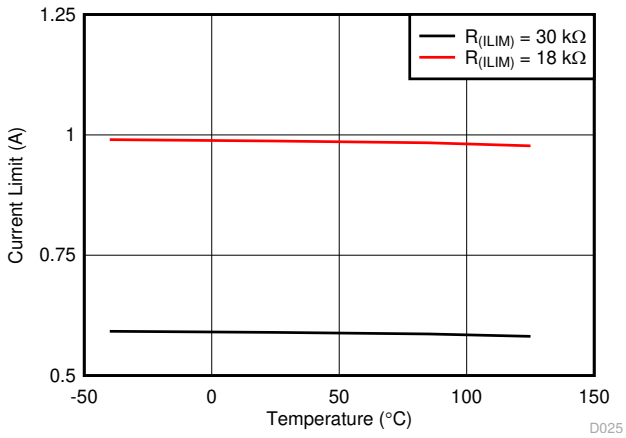


図 7-10. Overload Current Limit vs Temperature

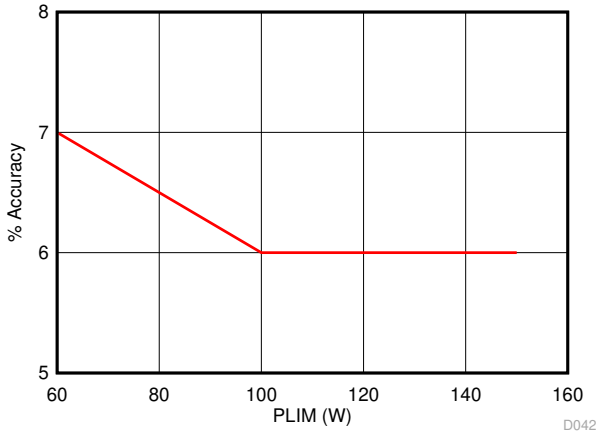
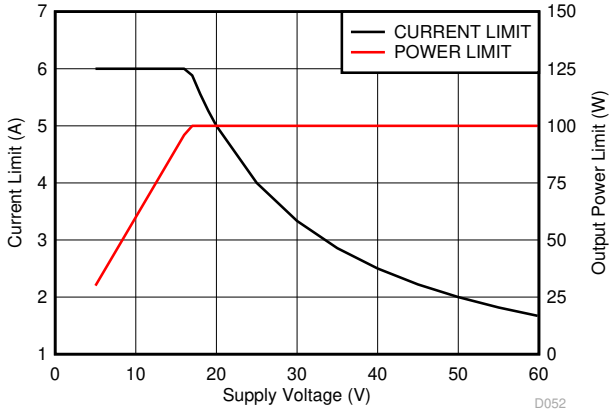


図 7-11. Output Power Limiting Accuracy vs PLIM



TPS26632 $R_{(PLIM)}$ = 100 kΩ $R_{(ILIM)}$ = 3 kΩ

図 7-12. Power Limit, Current limit vs Supply Voltage

7.7 Typical Characteristics (continued)

–40°C ≤ T_A = T_J ≤ +125°C, $V_{(IN\_SYS)}$ = $V_{(IN)}$ = 24 V, $V_{(\overline{SHDN})}$ = 2 V, $R_{(ILIM)}$ = 30 kΩ, IMON = PGOOD = $\overline{FLT}$ = OPEN, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN. (Unless stated otherwise)

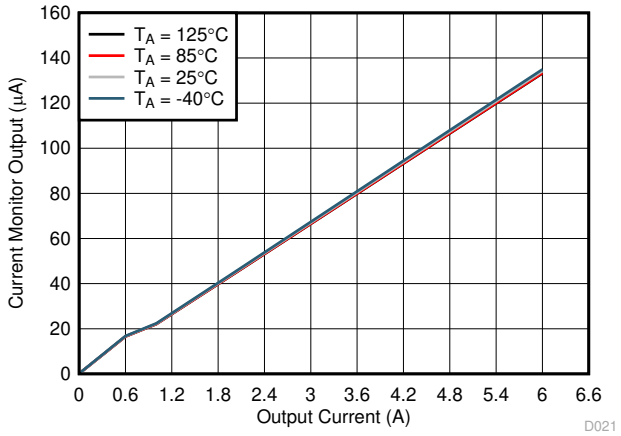


図 7-13. Current Monitor Output vs Output Current

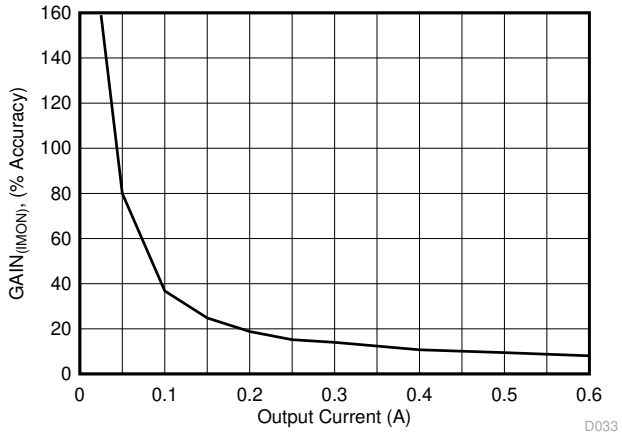
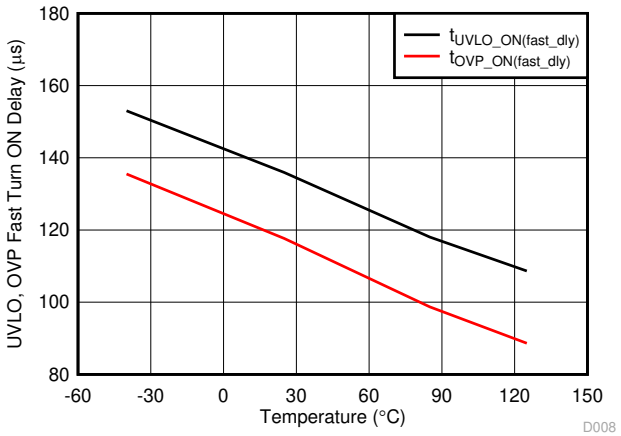


図 7-14. IMON Gain Accuracy at < 0.6-A Output Current



A. $V_{(PGTH)}$ > $V_{(PGTHF)}$

図 7-15. UVLO, OVP Fast Turn ON Delay vs Temperature

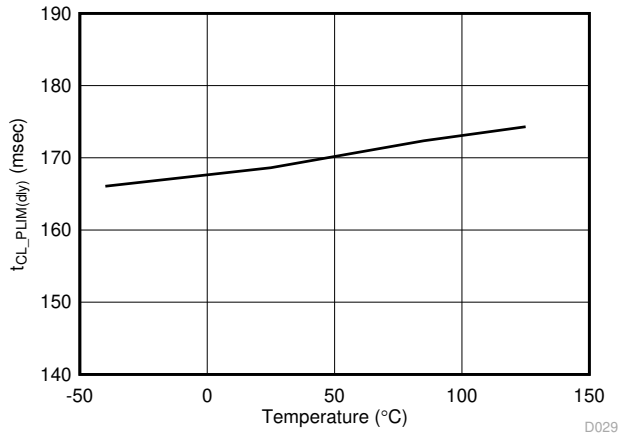


図 7-16. Maximum Duration in Current and Power Limiting vs Temperature

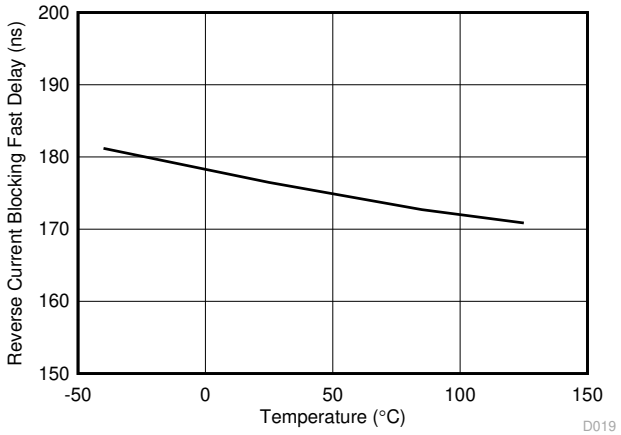
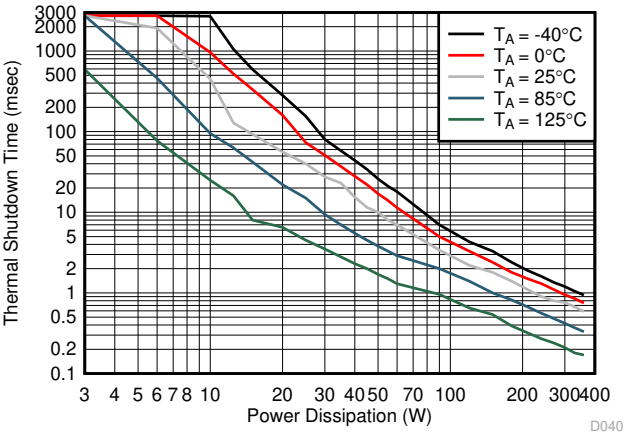


図 7-17. Reverse Current Blocking Response vs Temperature



Taken on VQFN device on EVM Board

図 7-18. Thermal Shutdown Time vs Power Dissipation

8 Parameter Measurement Information

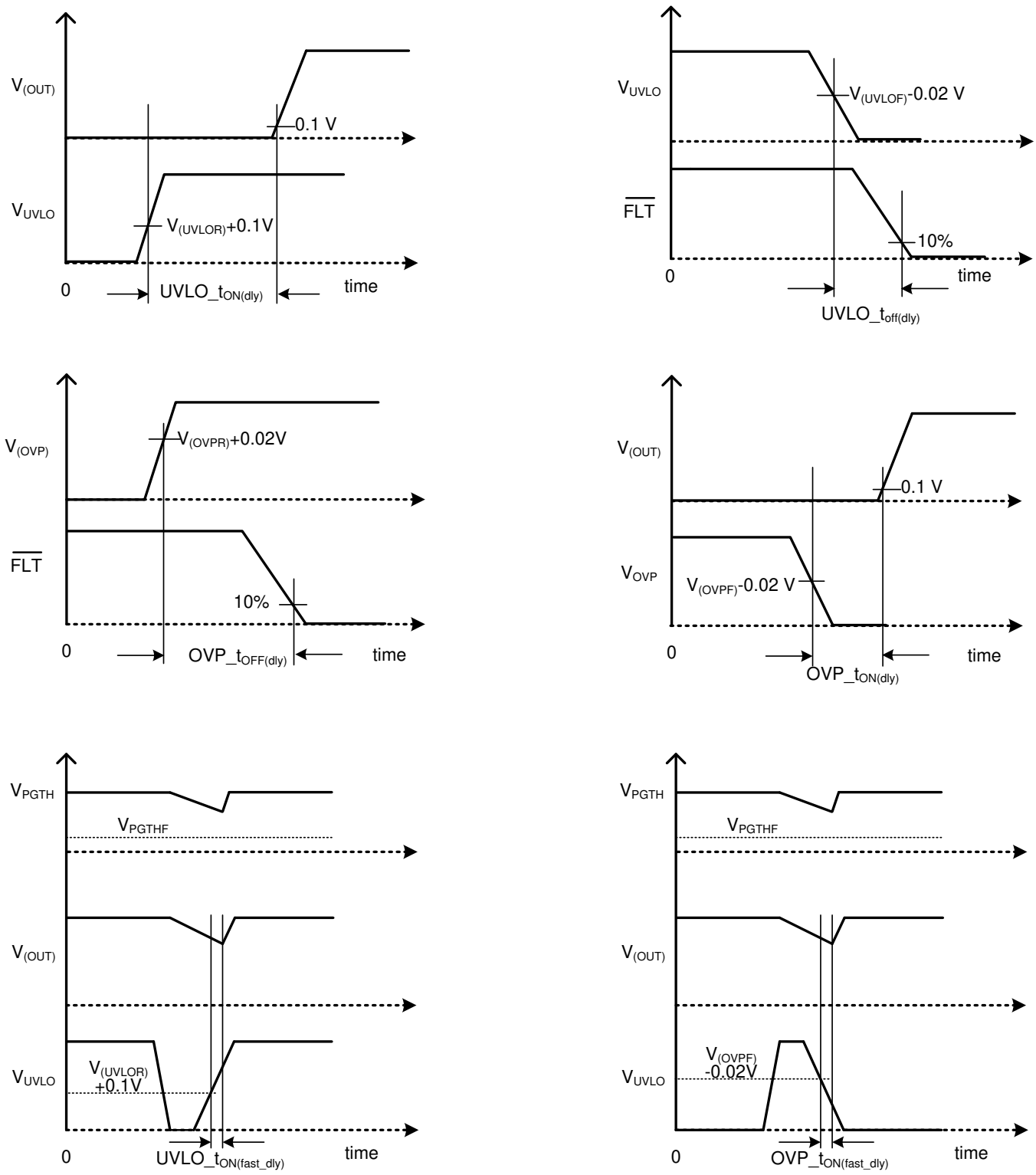


図 8-1. Timing Waveforms

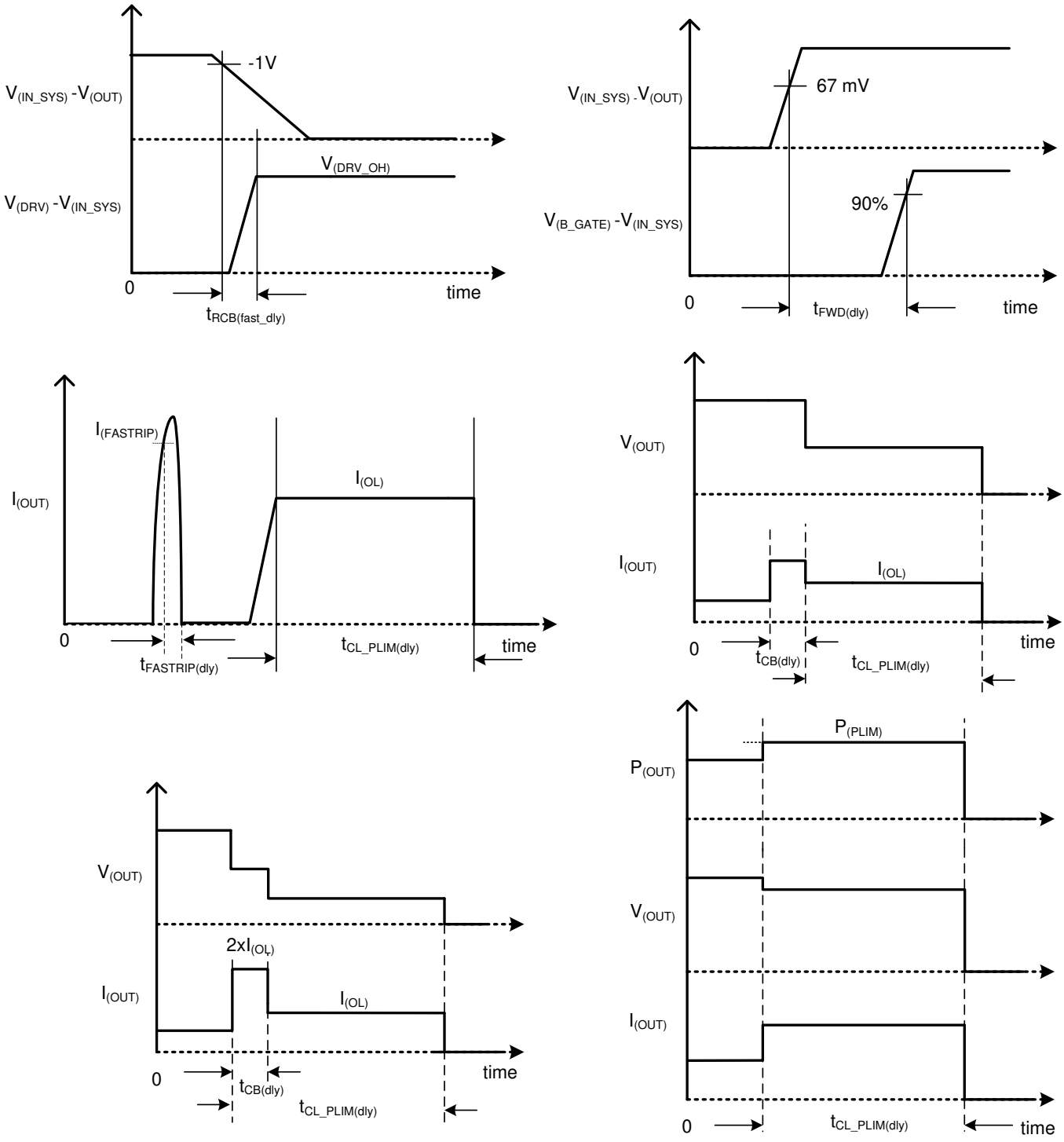


図 8-2. Timing Waveforms

9 Detailed Description

9.1 Overview

The TPS2663x devices are a family of 60-V industrial eFuses. The devices provides robust protection for all systems and applications powered from 4.5 V to 60 V. With an external N-channel FET the devices can be used to protect the loads from negative supply voltages down to –60 V. For hot-pluggable boards, the devices provides hot-swap power management with in-rush current control and programmable output voltage slew rate features using the dVdT pin. Load, source and device protections are provided with many programmable features including overcurrent, overvoltage and undervoltage. The precision overcurrent limit (±7% at 6 A) helps to minimize over design of the input power supply, while the fast response short circuit protection 1-µs (typical) immediately isolates the faulty load from the input supply when a short circuit is detected. The device features fast reverse current blocking response (0.17 µs). The internal robust protection control blocks of the TPS2663x along with its ±60-V rating, helps to simplify the system designs for the industrial surge compliance ensuring complete protection of the load and the device. The 60-V maximum DC operating and 70-V absolute maximum voltage rating enables system protection from 60-V DC input supply faults and from industrial SELV power supplies.

By monitoring the output (Load) voltage through the PGTH pin, the device distinguishes between real system faults and system transients and the turn ON delay during a fault recovery is controlled accordingly. The valid load voltage detection threshold can be adjusted using a resistor ladder network from OUT, PGTH and GND. This scheme ensures fast recovery during system tests like voltage interruption and brown-out tests, EMC testing like Electrical Fast Transients (IEC61000-4-4) and Surge (IEC61000-4-5).

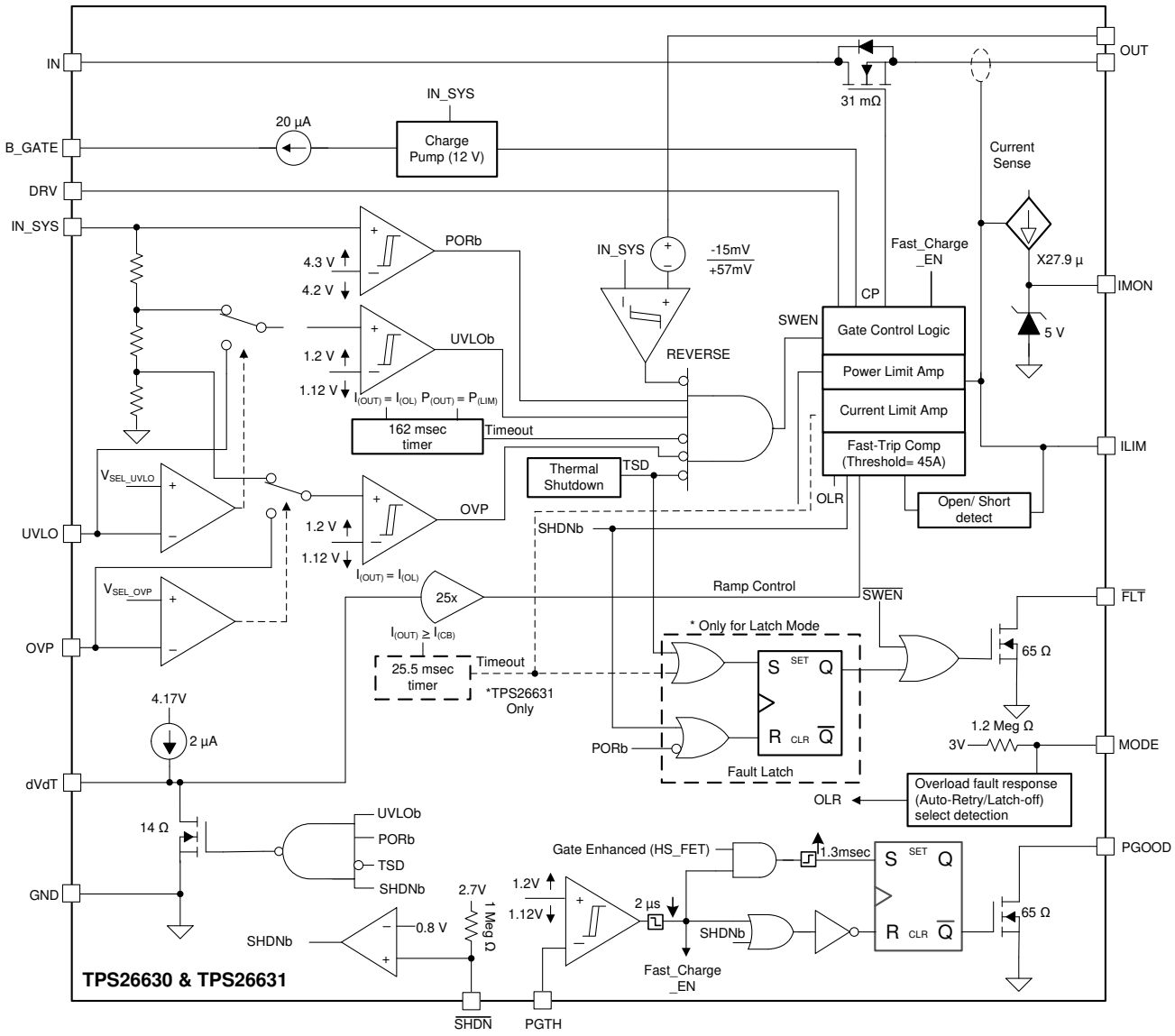
The TPS26632, TPS26633, TPS26635 and TPS26636 devices integrate adjustable output power limiting (PLIM) functionality that simplifies the system design requiring compliance in accordance to standards like IEC61010-1 and UL1310.

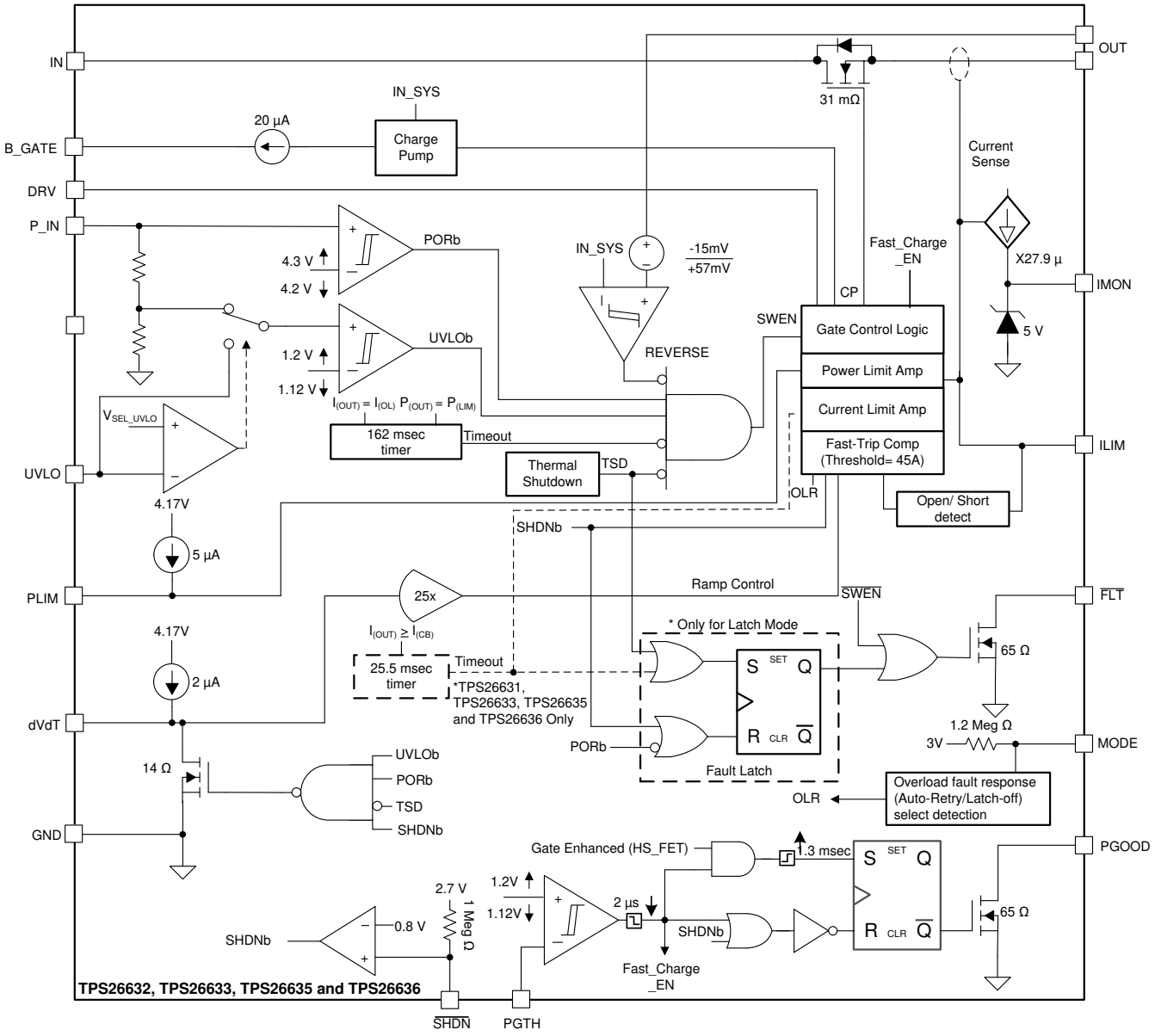
The devices provides precise monitoring of voltage bus for brown-out, overvoltage conditions and asserts fault signal for the downstream system. Its overall threshold accuracy of 2% ensures tight supervision of bus, eliminating the need for a separate supply voltage supervisor chip. The devices monitors $V_{(IN\_SYS)}$ and $V_{(OUT)}$ to provide true reverse current blocking when a reverse condition or input power failure condition is detected.

Additional features of the TPS2663x devices include:

- ±6% Current monitor output (IMON) for health monitoring of the system
- A choice of latch off or automatic restart mode response during current limit, power Limit and thermal fault using MODE pin
- PGOOD indicator output with ±2% accurate adjustable valid load voltage detection threshold (PGTH)
- Over temperature protection to safely shutdown in the event of an overcurrent event
- De-glitched fault reporting for supply brown-out and overvoltage faults
- Enable and disable control from an MCU using $\overline{\text{SHDN}}$ pin

9.2 Functional Block Diagram





9.3 Feature Description

9.3.1 Hot Plug-In and In-Rush Current Control

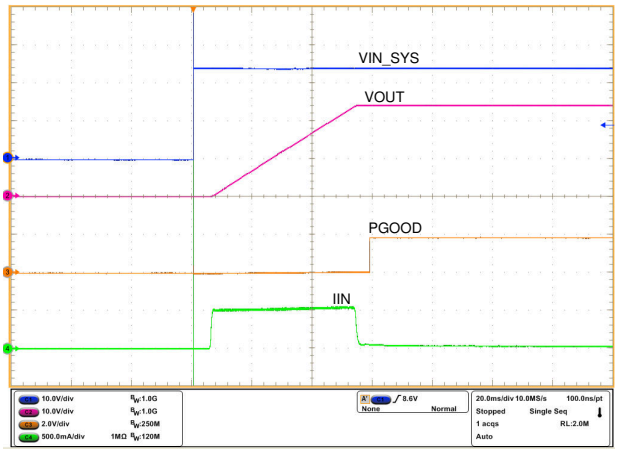
The devices are designed to control the inrush current upon insertion of a card into a live backplane or other "hot" power source. This limits the voltage sag on the backplane's supply voltage and prevents unintended resets of the system power. The controlled start-up also helps to eliminate conductive and radiative interferences. An external capacitor connected from the dVdT pin to GND defines the slew rate of the output voltage at power-on. The fastest output slew rate of 24 V/500 µs can be achieved by leaving dVdT pin floating. The inrush current can be calculated using 式 1.

$$I = C \times \frac{dV}{dT} \geq I_{(INRUSH)} = C_{(OUT)} \times \frac{V_{(IN)}}{t_{dVdT}} \quad (1)$$

where

$$t_{dVdT} = 20.8 \times 10^3 \times V_{(IN)} \times C_{(dVdT)} \quad (2)$$

Figure 8-1 illustrates in-rush current control performance of the device during Hot Plug-In.



C_{dVdT} = 100 nF　　C_{OUT} = 1000 µF　　R_{ILIM} = 4.02 kΩ

図 9-1. Hot Plug In and Inrush Current Control at 24-V Input

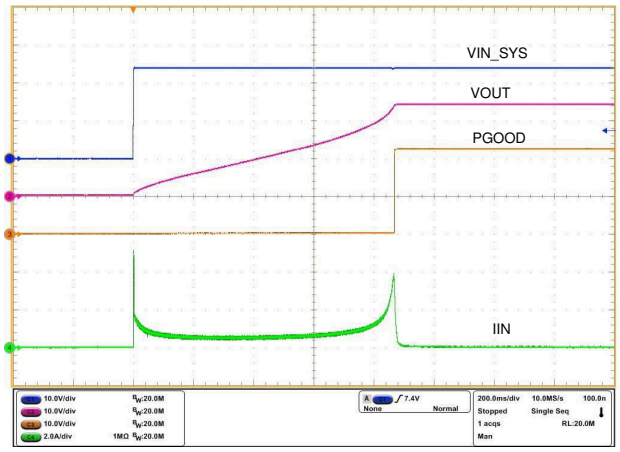
9.3.1.1 Thermal Regulation Loop

The average power dissipation within the eFuse during power up with a capacitive load can be calculated using 式 3.

$$P_{D(INRUSH)} = 0.5 \times V_{(IN)} \times I_{(INRUSH)} \quad (3)$$

System designs requiring to charge large output capacitors rapidly may result in an operating point that exceeds the power dissipation versus time boundary limits of the device defined by 図 7-18 characteristic curve. This may result in increase in junction temperature beyond the device's maximum allowed junction temperature. To keep the junction temperature within the operating range, the thermal regulation control loop regulates the junction temperature at $T_{(J\_REG)}$, 145°C (typical) by controlling the inrush current profile and thereby limiting the power dissipation within the device automatically. An internal 2.5 seconds (typical) timer starts from the instance the thermal regulation operation kicks in. If the output does not power up within this time then the internal FET is turned OFF. Subsequent operation of the device depends on the MODE configuration (Auto-Retry or latch OFF) setting as shown in 表 9-1. The maximum time-out of 1.25 seconds (typical) in thermal regulation loop operation ensures that the device and the system board does not heat up during steady fault conditions such as wake up with output short-circuit. This scheme ensures reliable power up operation.

Thermal regulation control loop is internally enabled during power up by $V_{(IN)}$, UVLO cycling and turn ON using $\overline{SHDN}$ control. Figure 8-2 illustrates performance of the device operating in thermal regulation loop during power up by $V_{(IN)}$ with a large output capacitor. The Thermal regulation loop gets disabled internally after the power up sequence when the internal FET's gate gets fully enhanced or when the $t_{(Treg\_timeout)}$ of 2.5 seconds (typical) time is elapsed.



C_{dVdT} = Open C_{OUT} = 30 mF R_{ILIM} = 4.02 kΩ

図 9-2. Thermal Regulation Loop Response During Power Up with Large Capacitive Load

9.3.2 PGOOD and PGTH

The devices feature an open drain Power good (PGOOD) indicator output. PGOOD can be used for enable and disable of the downstream loads like DC-DC converters. Connect a resistor ladder network from VOUT, PGTH and GND to set the PGOOD threshold level. PGOOD goes high when the internal FET's gate is enhanced and $V_{(PGTH)}$ is above $V_{(PGTHR)}$. PGOOD goes low when $V_{(PGTH)}$ goes below $V_{(PGTHF)}$. There is a deglitch of t_{PGOODR}, 1.2 msec (typical) at the rising edge and t_{PGOODR}, 2.1 µs (typical) deglitch on the falling edge of PGOOD indication. PGOOD is a rated for 60 V and can be pulled to IN_SYS or OUT through a resistor. PGTH can be used for setting downstream's supply UVLO levels and PGOOD as enable and disable control.

9.3.2.1 PGTH as VOUT Sensing Input

The devices use PGTH as the output (Load) voltage monitor input and to set the down stream loads UVLO threshold. To set the input PGTH threshold, connect a resistor divider network from VOUT to PGTH terminal to GND as shown in the *Simplified Schematic*. During a system fault recovery (example: OVP high to low or UVLO low to high) when the internal FET gate control is enabled, the device samples the PGTH information and decides whether to turn ON the FET with fast slew rate or dVdT mode based on the sampled $V_{(PGTH)}$ information.

図 8-1 shows the turn ON behavior based on $V_{(PGTH)}$ information. During the fault recovery instance if the $V_{(PGTH)}$ level is above$_{(PGTHF)}$ then the internal FET turns ON within a delay of $t_{OVP(dly\_fast)}$ with fast slew rate (ignores the capacitance connected at dVdT pin) with thermal regulation loop enabled for a duration of $t_{CL\_PLIM(dly)}$. Maximum current through the device during this operation is limited at $I_{(OL)}$ in TPS26630 and TPS26632 devices and at 2 x $I_{(OL)}$ in TPS26631, TPS26633, TPS26635 and TPS26636 devices for a maximum duration of $t_{CB(dly)}$. During the fault recovery instance if the $V_{(PGTH)}$ level is below $V_{(PGTHF)}$ then the device turns ON the internal FET in dVdT mode and the slew rate will depend on the dVdT capacitor value and maximum current through the devices is limited at $I_{(OL)}$. This way the device distinguishes between real system faults and system transients and the turn ON delay is controlled accordingly. This scheme ensures fast recovery during system tests like voltage interruption and brown-out tests, EMC testing like Electrical Fast Transients (IEC61000-4-4) and Surge (IEC61000-4-5). The fast turn ON during transient recovery feature can be disabled by connecting PGTH to GND. In this case, PGOOD will be pulled low.

9.3.3 Undervoltage Lockout (UVLO)

The TPS2663x devices feature an accurate ± 2% adjustable undervoltage lockout functionality. When the voltage at UVLO pin falls below $V_{(UVLOF)}$ during input undervoltage fault, the internal FET quickly turns off and $\overline{FLT}$ is asserted. The UVLO comparator has a hysteresis of 78 mV (typical). To set the input UVLO threshold, connect a resistor divider network from IN supply to UVLO terminal to GND as shown in the *Simplified Schematic*. The TPS2663x devices also features a factory set 15-V input supply undervoltage lockout

$V_{(IN\_SYS\_UVLO)}$ threshold with 1-V hysteresis. This feature can be enabled by connecting the UVLO terminal directly to the GND terminal. If the Undervoltage Lock-Out function is not needed, the UVLO terminal must be connected to the IN_SYS terminal. UVLO terminal must not be left floating. In the applications where reverse polarity protection is required connect a minimum of 300-kΩ resistor between UVLO and IN_SYS.

図 8-1 shows the turn ON behavior when UVLO pin voltage exceeds $V_{(UVLOR)}$ threshold.

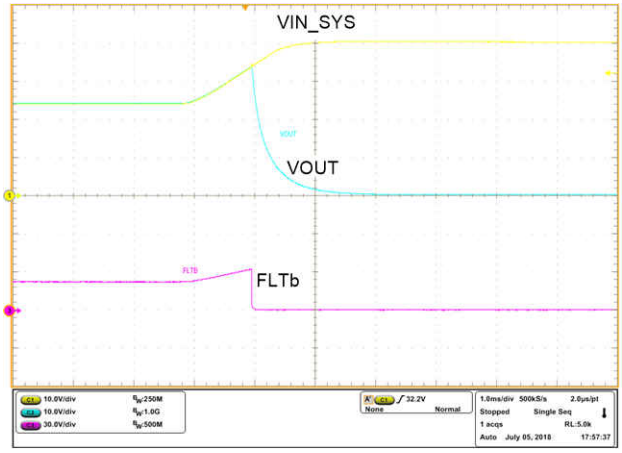
9.3.4 Overvoltage Protection (OVP)

The TPS2663x devices incorporate circuitry to protect the system during overvoltage conditions. The TPS26630 and TPS26631 feature an accurate ± 2% adjustable overvoltage cut off functionality. A voltage more than $V_{(OVPR)}$ on OVP pin turns off the internal FET and protects the downstream load. To program the OVP threshold externally, connect a resistor divider from IN_SYS supply to OVP terminal to GND as shown in the *Simplified Schematic*.

The TPS26630 and TPS26631 also feature a factory set 34.3-V input overvoltage cut off $V_{(IN\_SYS\_OVP)}$ threshold with a 440 mV hysteresis. This feature can be enabled by connecting the OVP terminal directly to the GND terminal. The TPS26632, TPS26633 and TPS26636 feature an internally fixed 35-V maximum overvoltage clamp $V_{(OVC)}$ functionality. The TPS26632 and TPS26633 clamps the output voltage to $V_{(OVC)}$, when the input voltage exceeds 35 V. TPS26635 features a fixed 39-V maximum overvoltage clamp level. During the output voltage clamp operation, the power dissipation in the internal MOSFET is PD = $(V_{(IN\_SYS)} - V_{(OVC)}) \times I_{(OUT)}$. Excess power dissipation for a prolonged period can increase the device temperature. To avoid this, the internal FET is operated in overvoltage clamp for a maximum duration of $t_{OVC(dly)}$, 162 msec (typical). After this duration, the internal FET is turned OFF and the subsequent operation of the device depends on the MODE configuration (Auto-Retry or latch OFF) setting as shown in 表 9-1.

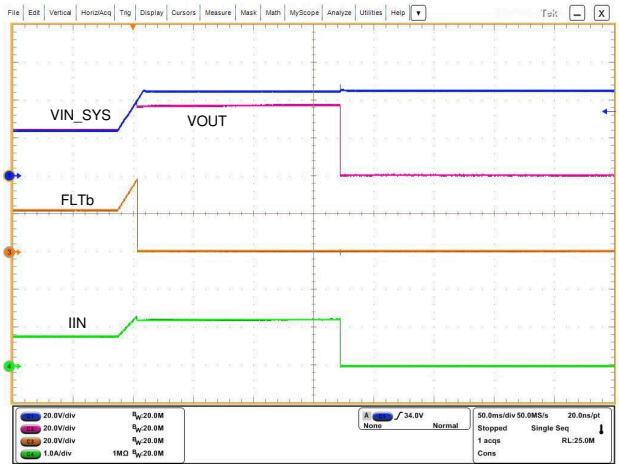
図 8-1 shows the turn ON behavior when OVP pin voltage falls below $V_{(OVPF)}$ threshold.

図 9-3 illustrates the overvoltage cut-off functionality and 図 9-4 illustrates the overvoltage clamp functionality. $\overline{FLT}$ is asserted after a delay of 617 µs (typical) after entering in overvoltage clamp mode and remains asserted until the overvoltage fault is removed.



TPS26630 and TPS26631

図 9-3. Overvoltage Cut-off Response at 33-V Level



TPS26635

R_{LOAD} = 30 Ω, $\overline{FLT}$ connected to VOUT

図 9-4. Overvoltage Clamp Response with TPS26635

9.3.5 Input Reverse Polarity Protection (B_GATE, DRV)

The TPS2663x devices support the reverse input polarity protection feature. Connect an N-channel power FET (Q1) with the source to IN_SYS, drain to IN and GATE to B-GATE as shown in 図 9-5. This forms a back to back FET topology in power path that is required to protect the load from input reverse polarity faults. Connect an

external signal FET (Q2) across BGATE, DRV and IN_SYS. Q2 acts as a pull down gate switch for Q1. In the applications where reverse polarity protection and reverse current blocking is not required then connect IN_SYS and IN together. Leave BGATE and DRV open as shown in 図 9-6.
Figure 8-7 illustrates the reverse input polarity protection functionality.

The TPS2663x devices support a maximum differential voltage across $V_{(IN\_SYS)}$ – $V_{(OUT)}$ upto –85 V. This high voltage transients generally appear during the IEC61000-4-5 surge testing at the $V_{(IN\_SYS)}$. This voltage stress appears across the external N-channel FET. The TPS2663x provides a gate drive (B_GATE) of 10.2 V (typical). The fast pull down gate switch Q2 pulls down the GATE of the Q1 during reverse current and reverse polarity fault events. Q2 should be at least 15-V, VDS rated FET with a maximum VGS rating of 20-V, Ciss ≤ 50 pF and VGTH(min) ≤ 3 V.

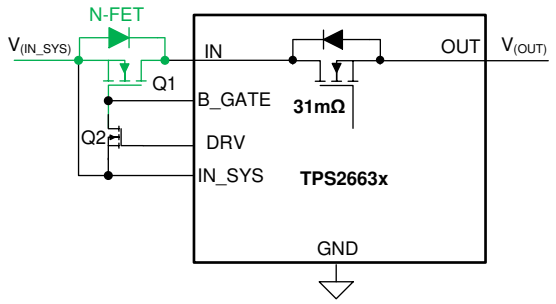


図 9-5. Configuration for Input Reverse Polarity Protection and Reverse Current Blocking

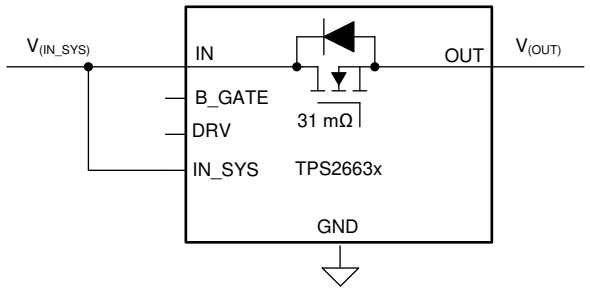


図 9-6. Configuration for Applications Without Input Reverse Polarity Protection and Reverse Current Blocking Requirement

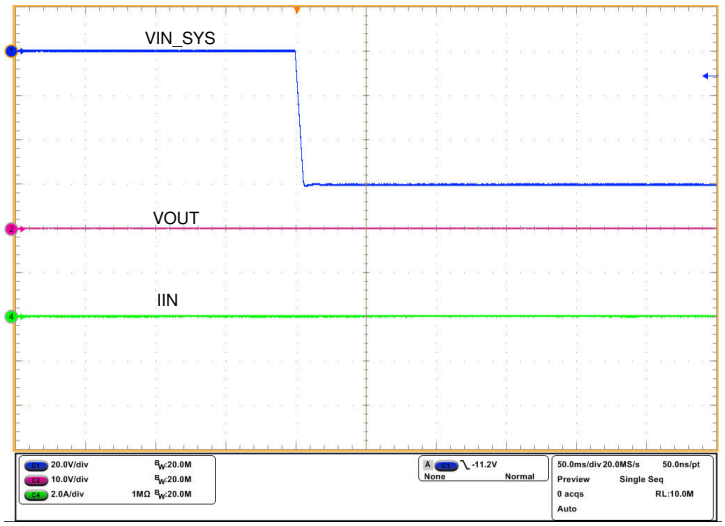


図 9-7. Input Reverse Polarity Response at –60-V Input

9.3.6 Reverse Current Protection

The device monitors $V_{(IN\_SYS)}$ and $V_{(OUT)}$ to provide true reverse current blocking when a reverse condition or input power failure condition is detected. The reverse comparator turns OFF the external blocking FET Q1 quickly as soon as $V_{(IN\_SYS)}$ – $V_{(OUT)}$ falls below –1 V. The total time taken to turn OFF the FET Q1 in this condition is $t_{RCB(fast\_dly)}$ + $t_{(Driver)}$. The delay due to the driver stage $t_{(Driver)}$ can be calculated using 式 4.

$$t_{(Driver)} = -RDSON_{(Q2)} \times Ciss_{(Q1)} \times \ln\left(\frac{VGTH_{(Q1)}}{V_{BGATE}}\right) \quad (4)$$

where

- $RDSON_{(Q2)}$ is the on resistance of the fast pull down switch Q2
- $Ciss_{(Q1)}$ is the input capacitance of the blocking FET Q1
- $VGTH_{(Q1)}$ is the GATE threshold voltage of the blocking FET Q1
- V_{BGATE} = 10.2 V (typical)

In a typical system design, $t_{(Driver)}$ is generally 10% to 20% of $t_{RCB(fast\_dly)}$ of 120 nsec (typical).

図 9-8 and 図 9-9 illustrates the behavior of the system during input hot short circuit condition. The blocking FET Q1 is turned ON within 1.6 ms (typical) once the differential forward voltage $V_{(IN\_SYS)} – V_{(OUT)}$ exceeds 67 mV (typical).

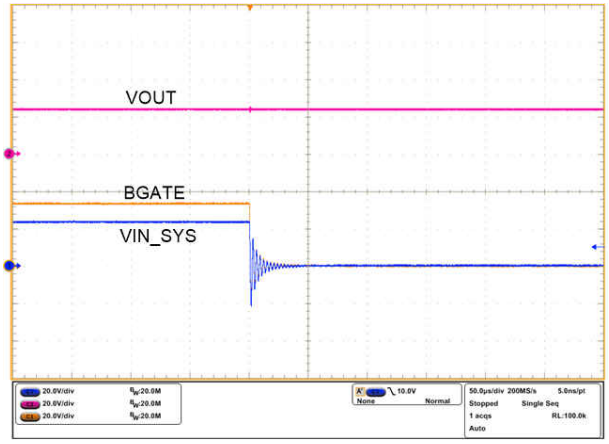


図 9-8. Input Hot Short Functionality at 24-V Supply

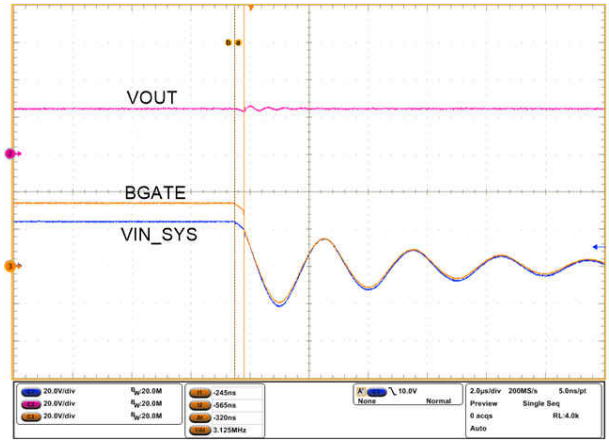


図 9-9. Input Hot-Short: Fast Trip Response (Zoomed)

The reverse comparator architecture has a supply line noise immunity resulting in a robust performance in noisy environments. This is achieved by controlling the turn OFF time of the internal FET based on the over-drive differential voltage $V_{(IN\_SYS)} – V_{(OUT)}$ over $V_{(REVTH)}$. Higher the over-drive, faster the turn OFF time, $t_{RCB(dly)}$.

9.3.7 Overload and Short Circuit Protection

The device monitors the load current by sensing the voltage across the internal sense resistor. The FET current is monitored during start-up and normal operation.

9.3.7.1 Overload Protection

Set the current limit using 式 5

$$I_{OL} = \frac{18}{R_{(ILIM)}} \tag{5}$$

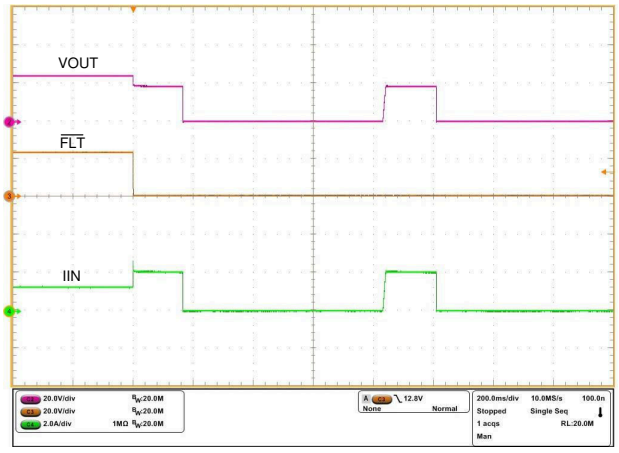
where

- $I_{(OL)}$ is the overload current limit in Ampere
- $R_{(ILIM)}$ is the current limit resistor in kΩ

9.3.7.1.1 Active Current Limiting at 1x I_{OL}, (TPS26630 and TPS26632 Only)

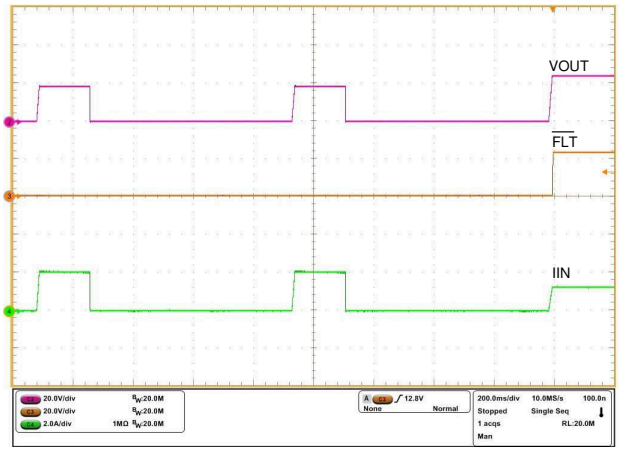
The TPS2663x devices feature accurate overload current limiting and fast short circuit protection feature. With TPS26630 and TPS26632 if the load current exceeds the programmed current limit I_{OL}, the device regulates the current through it at I_{OL} eventually reducing the output voltage. The power dissipation across the device during this operation will be $(V_{IN} – V_{OUT})$ x I_{OL} and this could heat up the device and eventually enter into thermal shutdown. The maximum duration for the overcurrent through the FET $t_{CL\_PLIM(dly)}$, 162 msec (typical). If the thermal shutdown occurs before this time the internal FET turns OFF and the subsequent operation (auto-retry

or latch OFF) will depend on the MODE pin configuration in 表 9-1. Figure 9-10 and Figure 9-11 illustrate overload current limiting performance.



V_{IN_SYS} = 24 V MODE connected to GND (Auto-Retry) R_{ILIM} = 9 kΩ

図 9-10. Overload Performance with TPS26630, TPS26632 during Load Step from 19 Ω to 9 Ω



V_{IN_SYS} = 24 V MODE connected to GND (Auto-Retry) R_{ILIM} = 9 kΩ

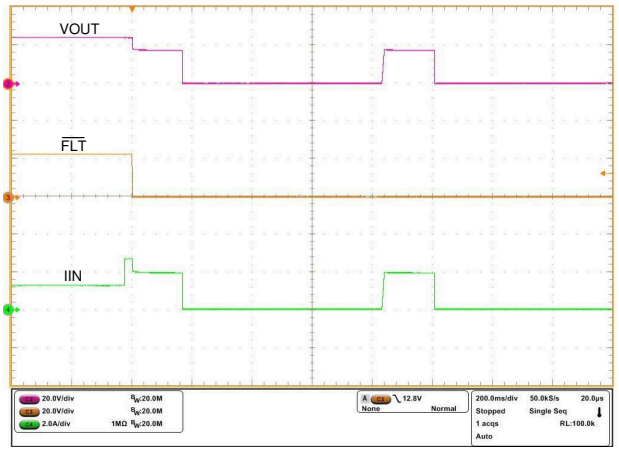
図 9-11. Response During Coming Out of Overload Fault

9.3.7.1.2 Active Current Limiting with 2x I_{OL} Pulse Current Support, (TPS26631, TPS26633, TPS26635 and TPS26636 Only)

TPS26631,TPS26633,TPS26635 and TPS26636 after the start-up and with PGOOD high, if the load current exceeds I_{OL}, then an internal fixed $t_{CB(dly)}$, 25.5 msec (typical) timer starts. During this time the device will pass through the over current demanded by the load not more than 2 x I_{OL} above which the device will regulate at 2 x I_{OL}. After $t_{CB(dly)}$ time, the device regulates the current at I_{OL}. The power dissipation across the device during this operation will be (V_{IN}–V_{OUT}) x I_{OL} and this could heat up the device and eventually enter into thermal shutdown. The maximum duration for the internal FET in current regulation is $t_{CL\_PLIM(dly)}$. The subsequent operation will be based on the MODE setting (either auto-retry or latch OFF) in 表 9-1.

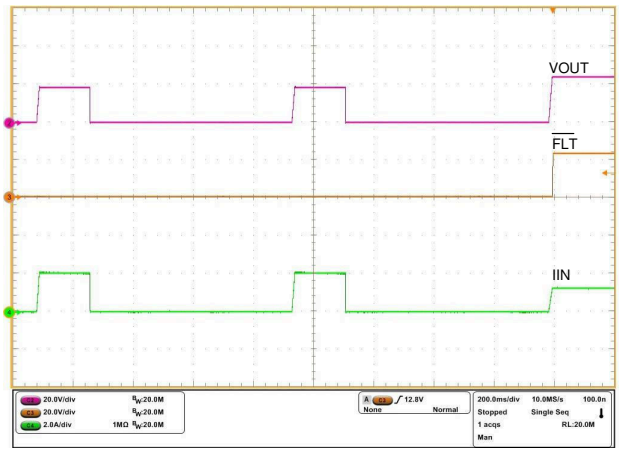
The 2 x $I_{(OL)}$ pulse current support is activated only after PGOOD goes high. If PGOOD is in low state such as during start-up operation or during auto-retry cycles, the 2 x $I_{(OL)}$ pulse current support is not activated and the device limits the current at $I_{(OL)}$ level.

図 9-12 and 図 9-13 illustrate overload current limiting performance.



V_{IN_SYS} = 24 V　MODE connected to GND (Auto-Retry)　R_{ILIM} = 9 kΩ

図 9-12. Overload Performance with TPS26631, TPS26633, TPS26635 and TPS26636 during Load Step from 19 Ω to 9 Ω



V_{IN_SYS} = 24 V　MODE connected to GND (Auto-Retry)　R_{ILIM} = 9 kΩ

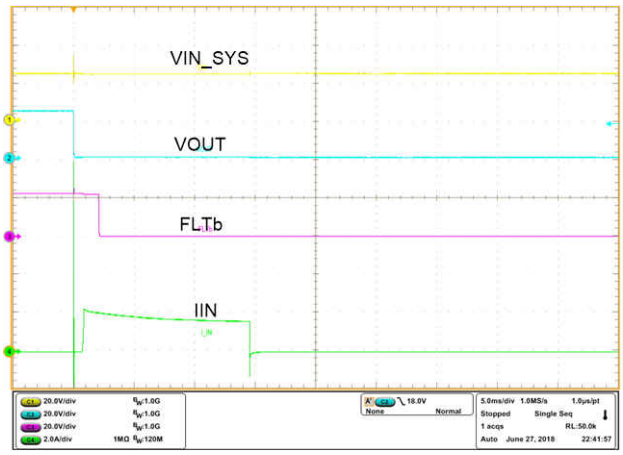
図 9-13. Response during Coming Out of Overload Fault

The TPS2663x devices feature ILIM pin short and open fault detection and protection. The internal FET is turned OFF when ILIM pin is detected short or open to GND and it remains OFF till the ILIM pin fault is removed.

Refer to 図 8-2 for more information on $t_{CB(dly)}$ and $t_{CL\_PLIM(dly)}$ parameter measurement information.

9.3.7.2 Short Circuit Protection

During a transient output short circuit event, the current through the device increases rapidly. As the current-limit amplifier cannot respond quickly to this event due to its limited bandwidth, the device incorporates a fast-trip comparator. The fast-trip comparator architecture is designed for fast turn OFF $t_{FASTTRIP(dly)}$ = 1 µs (typical) with $I_{(SCP)}$ = 45 A of the internal FET during an output short circuit event. The fast-trip threshold is internally set to $I_{(FASTTRIP)}$. The fasttrip circuit holds the internal FET off for only a few microseconds, after which the device turns back on slowly, allowing the current-limit loop to regulate the output current to $I_{(OL)}$. Then the device functions similar to the overload condition. Figure 8-14 illustrates output hot-short performance of the device.



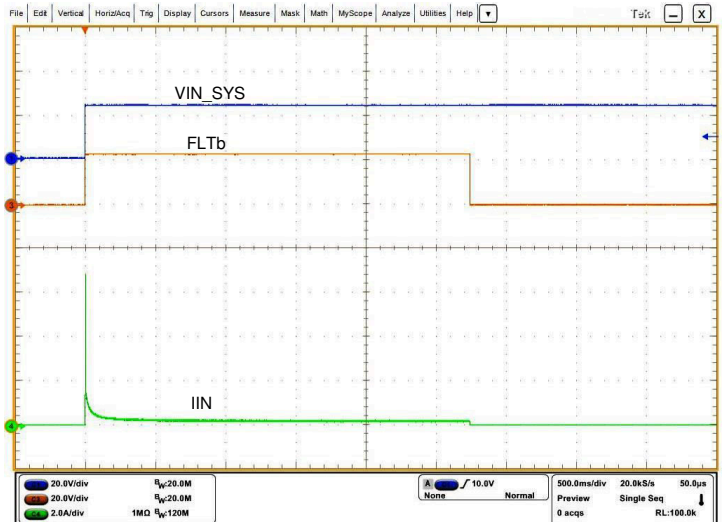
V_{IN_SYS} = 24 V　R_{ILIM} = 9.09 kΩ

図 9-14. Output Hot-Short Response

The fast-trip comparator architecture has a supply line noise immunity resulting in a robust performance in noisy environments. This is achieved by controlling the turn OFF time of the internal FET based on the overcurrent level, $I_{(FASTTRIP)}$ through the device. Higher the overcurrent, faster the turn OFF time, $t_{FASTTRIP(dly)}$. At overload current level in the range of $I_{FASTTRIP} < I_{OUT} < I_{SCP}$ the fast-trip comparator response is 3.2 µs (typical).

9.3.7.2.1 Start-Up With Short-Circuit On Output

When the device is started with short-circuit on the output, the current begins to limit at $I_{(OL)}$. Due to high power dissipation of VIN x $I_{(OL)}$ within the device the junction temperature increases. Subsequently, the thermal regulation control loop limits the load current to regulate the junction temperature at $T_{(J\_REG)}$, 145°C (typical) for a duration of $t_{(Treg\_timeout)}$, 2.5 sec (typical). Subsequent operation of the device depends on the MODE configuration (Auto-Retry or latch OFF) setting as per the 表 9-1. $\overline{FLT}$ gets asserted after $t_{(Treg\_timeout)}$ and remains asserted till the output short-circuit is removed. 図 9-15 illustrates the behavior of the device in this condition.



A. V_{IN} = 24V R_{ILIM} = 3 kΩ

図 9-15. Start-Up With Short on Output

9.3.8 Output Power Limiting, PLIM (TPS26632, TPS26633, TPS26635 and TPS26636 Only)

The TPS26630 and TPS26631 devices with a fixed overcurrent limit threshold the maximum output power limit increases linearly with supply input. Electrical industrial process control equipment such as PLC CPU needs to comply with standards like IEC61010-1 and UL1310 for fire safety, which require limited energy and power circuits. Limiting the output power becomes a challenge in such high power applications where the operating supply voltage range is wide. The TPS26632, TPS26633, TPS26635 and TPS26636 devices integrate adjustable output power limiting functionality that simplifies the system design requiring compliance in accordance to this standard.

Connect a resistor from PLIM to GND as shown in 図 9-16 to set the output power limiting value. If output power limiting is not required then connect PLIM to GND directly. This disables the PLIM functionality.

During an over power load event the TPS26632 limits the output power at the programmed value set by PLIM resistor. This indirectly results in the device operation in current limiting mode with steady state output voltage and current set by the load characteristics and $P_{LIM} = V_{OUT} \times I_{OUT}$. 図 7-12 shows the output power limit and current limit characteristics of TPS26632 with 100 W power limit setting. The maximum duration for the device in power limiting mode is 162 msec (typical), $t_{CL\_PLIM(dly)}$. After this time, the device operates either in auto-retry or latch off mode based on MODE pin configuration in 表 9-1.

During an over power load event the TPS26633, TPS26635 and TPS26636 allows the extra power for a maximum duration of $t_{CB(dly)}$, 25.5 msec (typical). The maximum power during this time is limited to V_{OUT} x 2 x

I_{OL} where I_{OL} is the overload current limit set by the $R_{(ILIM)}$ resistor. After the $t_{CB(dly)}$ time, the output power gets limited to the value programmed by the PLIM resistor. Set the power limit using 式 6.

$$P_{(PLIM)} = 1 \times R_{(PLIM)} \quad (6)$$

Here $P_{(PLIM)}$ is output power limit in watts, $R_{(PLIM)}$ is the power limit setting resistor in kΩ. Figure 9-17 and Figure 9-18 illustrate output power limiting performance of TPS26632 and TPS26633 devices respectively.

Refer to 図 8-2 for more information on $t_{CB(dly)}$ and $t_{CL\_PLIM(dly)}$ parameter measurement information.

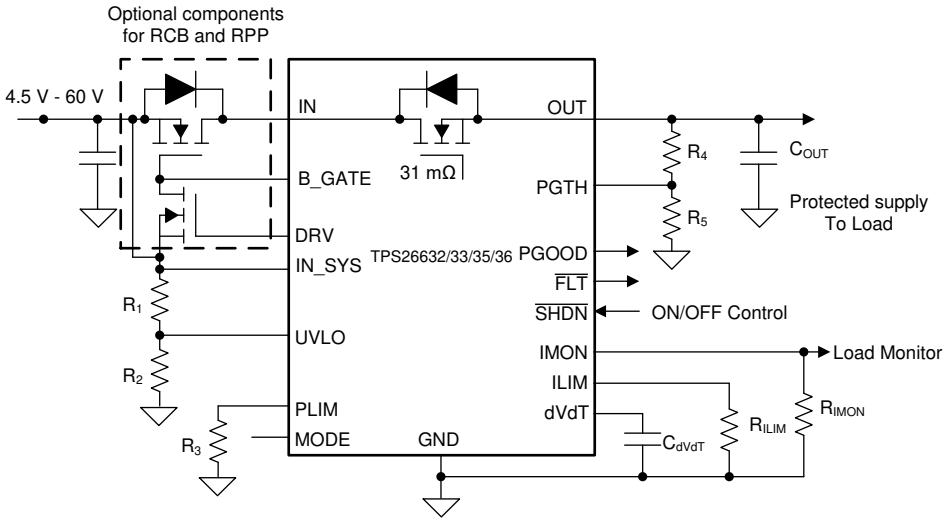
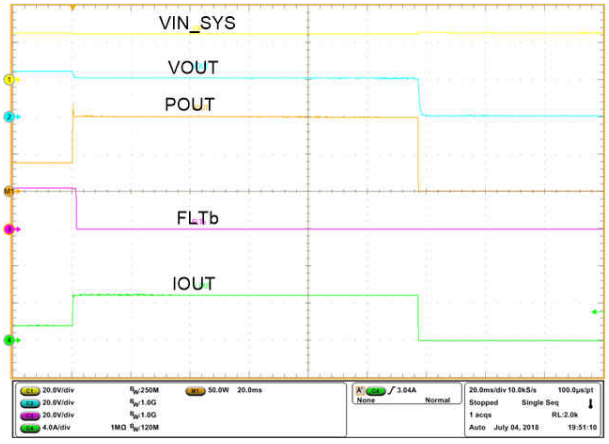
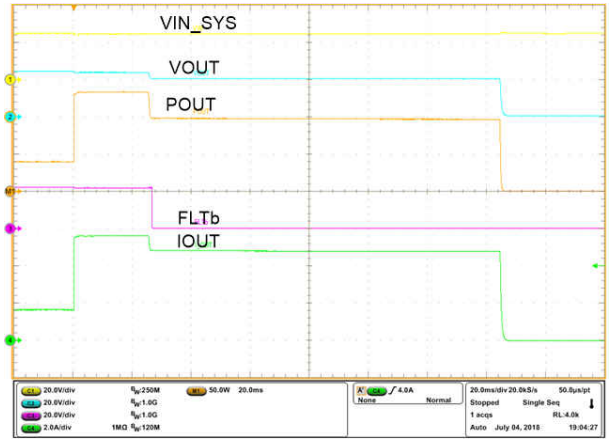


図 9-16. TPS26632, TPS26633, TPS26635 and TPS26636 Typical Application Schematic



R_{PLIM} = 100 kΩ R_{ILIM} = 3 kΩ

図 9-17. 100 W Class 2, Output Power Limiting Response of TPS26632



R_{PLIM} = 100 kΩ R_{ILIM} = 3 kΩ

図 9-18. 100 W Class 2, Output Power Limiting Response of TPS26633

9.3.9 Current Monitoring Output (IMON)

The TPS2663x devices feature an accurate analog current monitoring output. A current source at IMON terminal is internally configured to be proportional to the current flowing from IN to OUT. This current can be converted into a voltage using a resistor $R_{(IMON)}$ from IMON terminal to GND terminal. The IMON voltage can be used as a means of monitoring current flow through the system. The maximum voltage ($V_{(IMONmax)}$) for monitoring the current is limited to 4 V. This puts a limitation on maximum value of $R_{(IMON)}$ resistor and is determined by 式 7.

$$V_{(IMON)} = \left[I_{(OUT)} \times GAIN_{(IMON)}\right] \times R_{(IMON)} \quad (7)$$

Where,

- $GAIN_{(IMON)}$ is the gain factor $I_{(IMON)}$:$I_{(OUT)}$ = 27.9 µA/A (Typical)
- $I_{(OUT)}$ is the load current

Refer to Figure 6-13 for IMON output versus load current plot. 図 9-19 illustrates IMON performance.

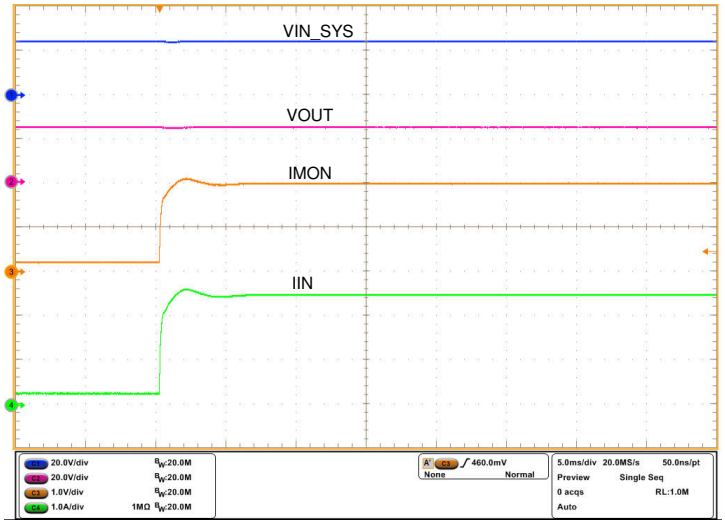


図 9-19. IMON Response During a Load Step

The IMON pin must not have a bypass capacitor to avoid delay in the current monitoring information.

9.3.10 FAULT Response ($\overline{FLT}$)

The $\overline{FLT}$ open-drain output asserts (active low) under the faults events such as undervoltage, overvoltage, overload, power limiting, reverse current, ILIM pin short and thermal shutdown conditions. The device is designed to eliminate false reporting by using an internal "de-glitch" circuit for fault conditions without the need for an external circuitry. $\overline{FLT}$ can be left open or connected to GND when not used.

9.3.11 IN_SYS, IN, OUT and GND Pins

Connect a minimum of 0.1uF capacitor across IN_SYS and GND. For systems and applications where reverse polarity protection and/or reverse current blocking feature is required

- Connect a N-channel FET between IN_SYS and IN with source of the FET connected to IN_SYS, Drain at IN and GATE to B_GATE.
- Connect a N-channel signal FET with GATE to DRV, Drain to B_GATE, Source to IN_SYS

If the external N-channel FET is not used then connect IN_SYS and IN together and leave B_GATE and DRV pins floating as shown in Figure 8-7. Do not leave any of the IN and OUT pins un-connected.

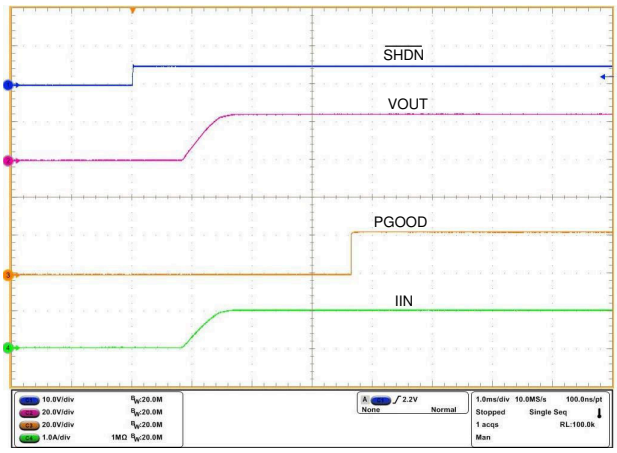
9.3.12 Thermal Shutdown

The device has a built-in overtemperature shutdown circuitry designed to protect the internal FET, if the junction temperature exceeds $T_{(TSD)}$, 165°C (typical). After the thermal shutdown event, depending upon the mode of fault response configured as per the 表 9-1, the device either latches off or commences an auto-retry cycle of 648 msec (typical), $t_{(TSD\_retry)}$ after $T_J < [T_{(TSD)} – 11°C]$. During the thermal shutdown, the fault pin $\overline{FLT}$ pulls low to indicate a fault condition.

9.3.13 Low Current Shutdown Control ($\overline{SHDN}$)

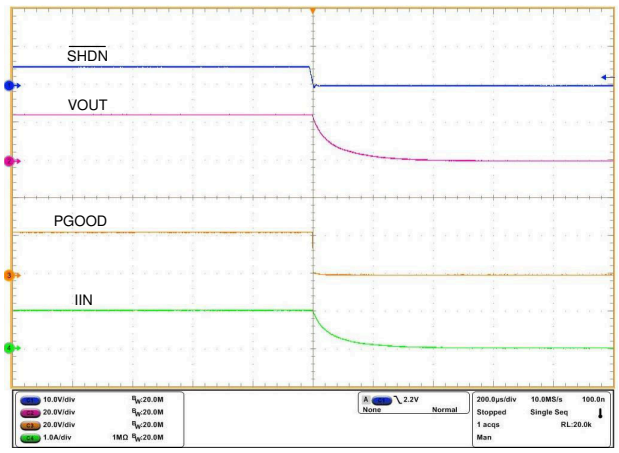
The internal, external FET and hence the load current can be switched off by pulling the $\overline{SHDN}$ pin below 0.8-V threshold with a micro-controller GPIO pin or can be controlled remotely with an opto-isolator device. The device

quiescent current reduces to 21 µA (typical) in shutdown state. To assert $\overline{SHDN}$ low, the pull down must have sinking capability of at least 10 µA. To enable the device, $\overline{SHDN}$ must be pulled up to at least 2 V. Once the device is enabled, the internal FET turns on with dVdT mode. 図 9-20 and 図 9-13 illustrate the performance of $\overline{SHDN}$ control.



V_{IN} = 24 V $C_{(dVdT)}$ = 22 nF R_{LOAD} = 24 Ω

図 9-20. Turnon Control With $\overline{SHDN}$



V_{IN} = 24 V $C_{(dVdT)}$ = 22 nF R_{LOAD} = 24 Ω

図 9-21. Turnoff Control With $\overline{SHDN}$

9.4 Device Functional Modes

The TPS2663x devices respond differently to overload with MODE pin configurations. The operational differences are explained in 表 9-1.

表 9-1. Device Operational Differences Under Different MODE Configurations

MODE Pin Configuration	Overload Protection Operation	Device
Open	Active Current limiting at 1x for a maximum duration of $t_{CL\_PLIM(dly)}$. There after Latches OFF. Latch reset by toggling $\overline{SHDN}$ low to high or UVLO low to high or power cycling IN_SYS.	TPS26630, TPS26632
	Active Current limiting at 2x for $t_{CB(dly)}$ duration followed with 1x current limiting for a maximum duration of $t_{CL\_PLIM(dly)}$. There after Latches OFF. Latch reset by toggling $\overline{SHDN}$ low to high or UVLO low to high or power cycling IN_SYS.	TPS26631, TPS26633, TPS26635, TPS26636
Shorted to GND	Active Current limiting at 1x for a maximum duration of $t_{CL\_PLIM(dly)}$. There after auto-retries after a delay of $t_{(TSD\_retry)}$.	TPS26630, TPS26632
	Active Current limiting at 2x for $t_{CB(dly)}$ duration followed with 1x current limiting for a maximum duration of $t_{CL\_PLIM(dly)}$. There after auto-retries after a delay of $t_{(TSD\_retry)}$.	TPS26631, TPS26633, TPS26635

Refer to 図 8-2 for more information on $t_{CB(dly)}$ and $t_{CL\_PLIM(dly)}$ parameter measurement information.

10 Application and Implementation

注

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10.1 Application Information

The TPS2663x is an industrial eFuse, typically used for Hot-Swap and Power rail protection applications. It operates from 4.5 V to 60 V with adjustable current limit, output power limit, overvoltage, undervoltage and reverse polarity protections. The device aids in controlling in-rush current and provides robust protection against reverse current and filed miss-wiring conditions for systems such as PLCs, Industrial PCs, Control and Automation and Sensors. The device also provides robust protection for multiple faults on the system rail

The *Detailed DesignProcedure* section can be used to select component values for the device. Additionally, a spreadsheet design tool *TPS2663 Design Calculator* is available in the web product folder.

10.2 Typical Application: Power Path Protection in a PLC System

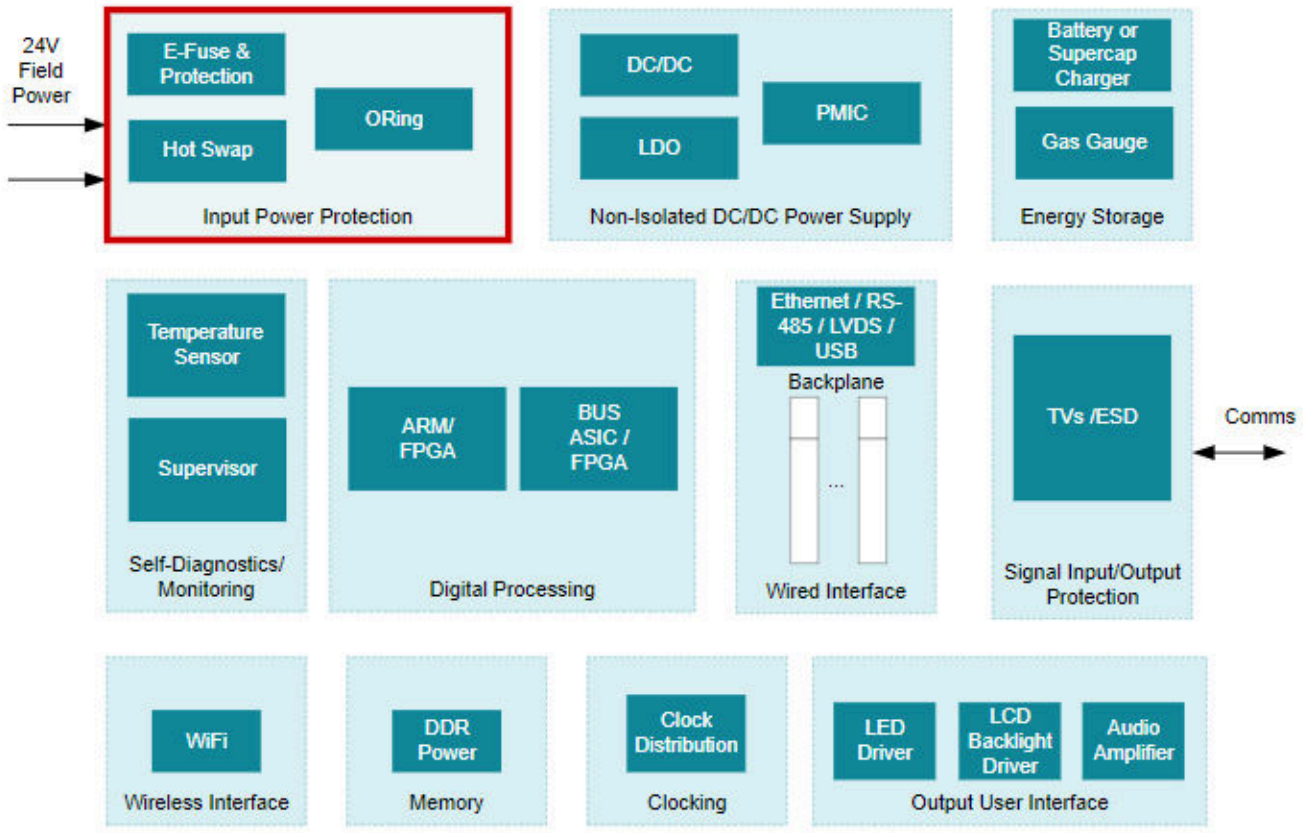


図 10-1. A Typical CPU (PLC Controller) System Block Diagram

The PLC system is usually connected to an external 24-V DC power supply to provide power to the controller unit, backplane, and I/O modules. Input protection circuits are required to protect the PLC from faults such as overvoltage, undervoltage, and overload. Because input supply connectors are screw type, there can always be a possibility of reverse supply connections. Protection circuits should block the reverse polarity to protect the PLC from possible negative voltages. At the same time, every PLC is tested for electrostatic discharge (ESD) according to IEC 61000-4-2, burst pulses (EFT) according to IEC 61000- 4-4, energy single pulse (surge)

according to IEC 61000-4-5, voltage drops and interruptions. 図 10-1 shows a system block diagram of PLC controller unit along with the input protection socket. The TPS2663x devices offer a plug and play input protection solution for such applications. For more information about this end equipment refer to the TI application site on *Programmable Logic Controller (PLC), DCS & PAC: CPU (PLC Controller)*.

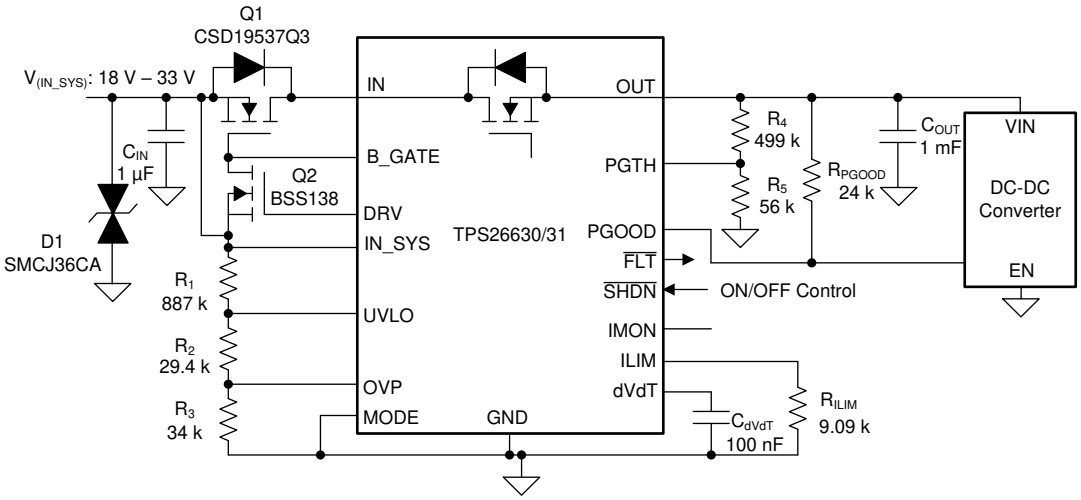


図 10-2. 24-V, 2-A eFuse Input Protection Circuit for Industrial PLC, CNC CPU

10.2.1 Design Requirements

表 10-1 shows the Design Requirements for TPS2663x.

表 10-1. Design Requirements

DESIGN PARAMETER		EXAMPLE VALUE
$V_{(IN)}$	Typical input voltage	24 V
$V_{(UV)}$	Undervoltage lockout set point	18 V
$V_{(OV)}$	Overvoltage cutoff set point	33 V
$I_{(LIM)}$	Overload Current limit	2 A
$I_{(INRUSH)}$	Inrush Current limit	500 mA
$P_{(OUT)}$	Output Load	15 W (DC-DC) with 15 V $VINmin_{DC-DC}$
$T_{(FAIL\_TR)}$	Power Interruption time	10 msec
$P_{(Surge)}$	IEC61000-4-5 Surge test level	± 500 V, 2 Ω generator impedance

10.2.2 Detailed Design Procedure

10.2.2.1 Programming the Current-Limit Threshold—$R_{(ILIM)}$ Selection

The $R_{(ILIM)}$ resistor at the ILIM pin sets the overload current limit, this can be set using 式 8.

$$R_{(ILIM)} = \frac{18}{I_{OL}} = 9k\Omega \quad (8)$$

where

- I_{LIM} = 2 A

Choose the closest standard 1% resistor value : $R_{(ILIM)}$ = 9.09 kΩ

10.2.2.2 Undervoltage Lockout and Overvoltage Set Point

The undervoltage lockout (UVLO) and overvoltage trip point are adjusted using an external voltage divider network of R_1, R_2 and R_3 connected between IN_SYS, UVLO, OVP and GND pins of the device. The values required for setting the undervoltage and overvoltage are calculated by solving 式 9 and 式 10.

$$V_{(OVPR)} = \frac{R3}{R1 + R2 + R3} \times V_{(OV)} \quad (9)$$

$$V_{(UVLOR)} = \frac{R2 + R3}{R1 + R2 + R3} \times V_{(UV)} \quad (10)$$

For minimizing the input current drawn from the power supply {$I_{(R123)} = V_{(IN)} / (R_1 + R_2 + R_3)$}, it is recommended to use higher value resistance for R_1, R_2 and R_3.

However, the leakage current due to external active components connected at resistor string can add error to these calculations. So, the resistor string current, $I(R_{123})$ must be chosen to be 20x greater than the leakage current of UVLO and OVP pins.

From the device electrical specifications, $V_{(OVPR)}$ = 1.2 V and $V_{(UVLOR)}$ = 1.2 V. From the design requirements, $V_{(OV)}$ is 33 V and $V_{(UV)}$ is 18 V. To solve the equation, first choose the value of R_3 = 34 kΩ and use 式 9 to solve for (R_1 + R_2) = 916 kΩ. Use 式 10 and value of (R_1 + R_2) to solve for R_2 = 29.4 kΩ and finally R_1= 887 kΩ.

Choose the closest standard 1% resistor values: R_1 = 887 kΩ, R_2 = 29.4 kΩ, and R_3 = 34 kΩ.

The UVLO and the OVP pins can also be connected to the GND pin to enable the internal default $V_{(OV)}$ = 34.2 V and $V_{(UV)}$ = 15.6 V.

10.2.2.3 Output Buffer Capacitor – C_{OUT}

During the power interruption time T_{FAIL_TR} the output capacitor C_{OUT} of the TPS26630 provides energy to the 15 W DC-DC converter load. Use 式 11 to compute the required buffer capacitor C_{OUT}

$$C_{OUT} = \frac{2 \times P_{(DC-DC)} \times T_{FAIL\_TR}}{V_{(IN\_SYS)}^2 - V_{(UV\_DC-DC)}^2} \quad (11)$$

where

- $P_{(DC-DC)}$ = 15 W/η. Assuming efficiency of 95%, $P_{(DC-DC)}$ = 15.8 W
- T_{FAIL_TR} = 10 msec
- $V_{(IN\_SYS)}$ = 24 V
- $V_{(UV\_DC-DC)}$ = 15 V

C_{OUT} = 0.9 mF. Choose a capacitor with ±10% tolerance, C_{OUT} = 1 mF/35 V electrolytic capacitor. Figure 9-4 and 図 10-5 illustrate the performance during the power interruption tests on TPS26630. Figure 9-8 illustrate the performance on TPS26631.

10.2.2.4 PGTH Set Point

Set the V_{PGTHF} threshold at the down-stream DC-DC converter UVLO falling threshold. VIN minimum operating voltage of the DC-DC converter is at 15 V. Assuming UVLO to be at 20% lower level, V_{UVLO_DC-DC} = 12 V. Use 式 12 to calculate R_4 and R_5.

$$V_{(PGTHF)} = \frac{R_5}{R_4 + R_5} \times V_{UVLO\_DC-DC} \quad (12)$$

$V_{(PGTHF)}$ = 1.14 V. Assuming R_5 = 56 kΩ, R_4 comes out to be approximately 499 kΩ.

10.2.2.5 Setting Output Voltage Ramp Time—(t_{dVdT})

Use 式 1 and 式 2 to calculate required $C_{(dVdT)}$ for achieving an inrush current of 500 mA. $C_{(dVdT)}$ = 0.1 µF. Figure 9-3 illustrates the inrush current limiting performance during 24-V hot-plug in condition.

10.2.2.5.1 Support Component Selections— R_{PGOOD} and $C_{(IN)}$

The R_{PGOOD} serves as pull-up for the open-drain output. The current sink by this pin must not exceed 10 mA (see the *Absolute Maximum Ratings* table). Typical resistance value in the range of 10 kΩ to 100 kΩ is recommended for R_{PGOOD}. Connect PGOOD directly to the EN pin of the DC-DC converter. 図 10-6 and Figure 9-8 illustrate the power up and power down performance of the system respectively. The C_{IN} is a local bypass capacitor to suppress noise at the input. A minimum of 1 µF is recommended for $C_{(IN)}$ for limit the slew rates during the surge test.

10.2.2.6 Selecting Q1, Q2 and TVS Clamp for Surge Protection

For ±500-V, 2-Ω surge, typically a SMC sized TVS like SMCJ36CA clamps the voltage around ±55 V. During the negative surge strike, the input voltage V_{IN_SYS}spikes to –55 V. This results in a voltage stress of –(55 V + 24 V) = –79 V across the external blocking FET Q1. Choose at least a 80-V rated N-channel FET. B_GATE drive is in the range of 10 V to 14 V. Select a suitable FET with the target RDSON specified at this gate drive voltage. The fast pull down gate switch Q2 pulls down the GATE of the Q1 during the reverse current event appearing during the surge test. Q2 should be at least 15-V VDS rated FET with a maximum VGS rating of 20-V , Ciss <= 50 pF and VGTH(min) ≤ 3 V. CSD19537Q3 and BSS138 are selected for Q1 and Q2 respectively. Figure 9-9 and Figure 9-10 illustrate the performance of the system during the surge testing.

10.2.3 Application Curves

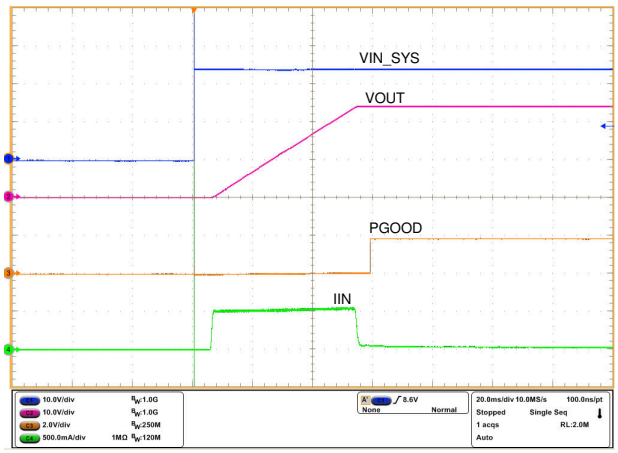


図 10-3. Hot-Plug In at 24-V Supply

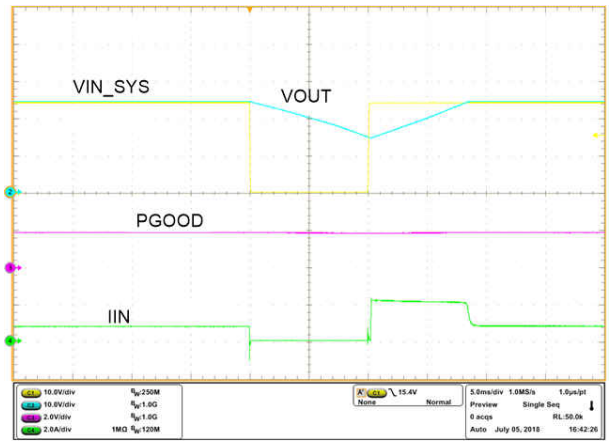


図 10-4. Voltage Interruption Response With TPS26630

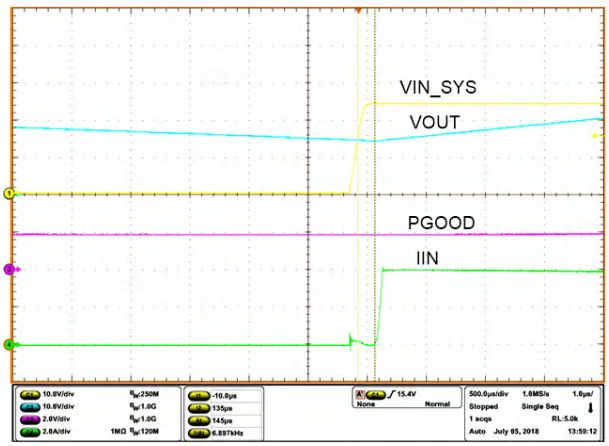


図 10-5. Voltage Interruption Response With TPS26630 (Zoomed)

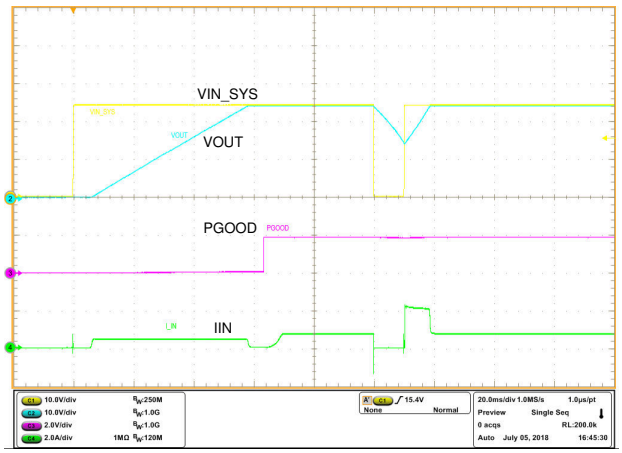


図 10-6. Power Up Followed With Voltage Interruption With TPS26630

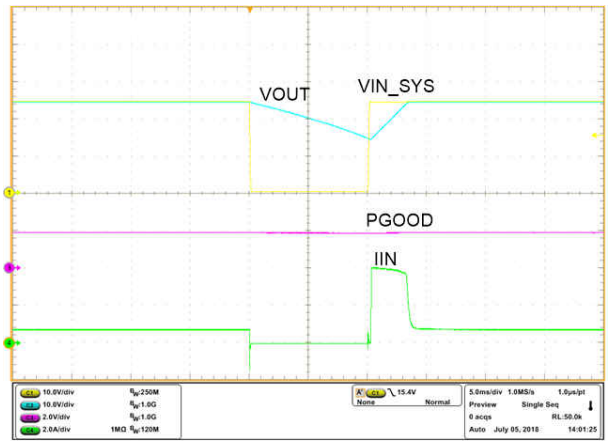


図 10-7. Voltage Interruption Performance With TPS26631

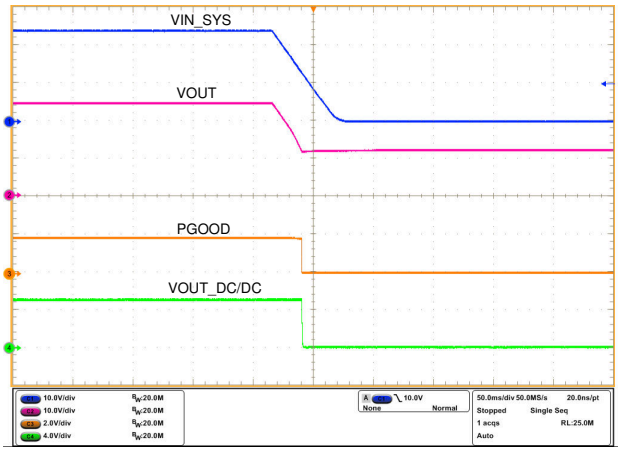


図 10-8. Power Down Response

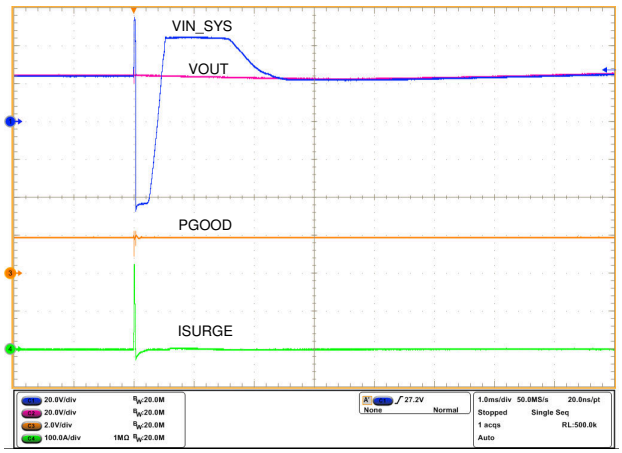


図 10-9. 500-V, 2-Ω Surge Response

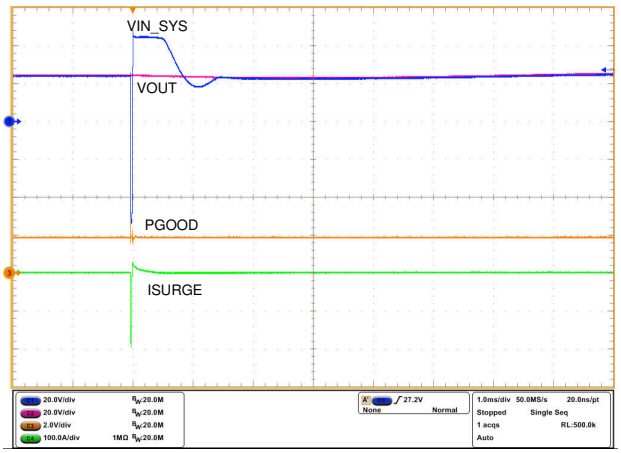


図 10-10. –500-V, 2-Ω Surge Response

10.3 System Examples

10.3.1 Simple 24-V Power Supply Path Protection

With the TPS2663x devices, a simple 24-V power supply path protection can be realized using a minimum of five external components as shown in the schematic diagram in 図 10-11. The external components required are: a N–Channel Power FET Q_1, a N–Channel signal FET Q_2 and a $R_{(ILIM)}$ resistor to program the current limit, $C_{(IN)}$ and $C_{(OUT)}$ capacitors.

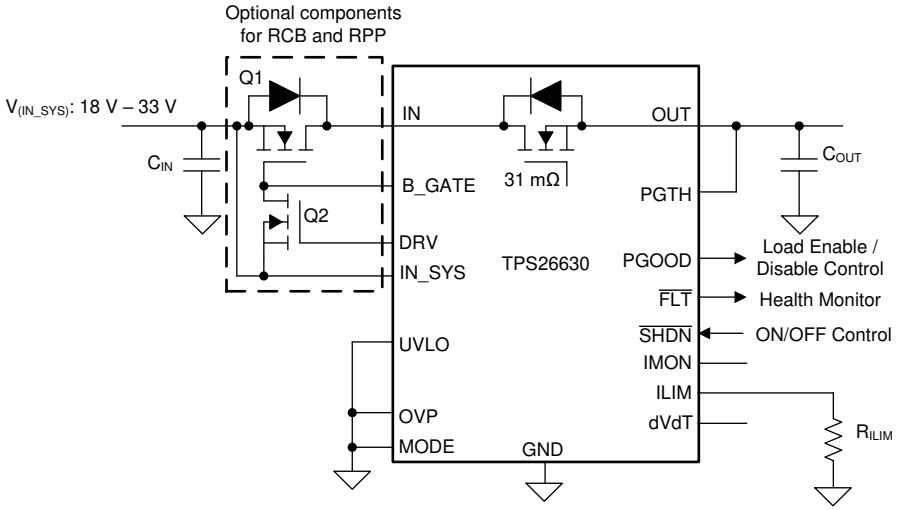


図 10-11. TPS26630 Configured for a Simple 24-V Supply Path Protection

Protection features with this configuration include:

- Load and device protection from reverse input polarity fault down to –60 V (with a 60-V rated Q_1)
- Overvoltage Protection at 34 V
- Inrush current control with 24-V/240-µs output voltage slew rate
- Reverse Current Blocking
- Accurate current limiting with Auto-Retry

10.3.2 Priority Power MUX Operation

Applications having two energy sources such as Portable battery powered equipment require preference of one source to another. For example, mains power (wall-adapter) has the priority over the internal back-up power or auxiliary power. These applications demand for switch over from mains power to backup power only when main input voltage falls below a user defined threshold. The TPS2663x devices provide a simple solution for priority power multiplexing needs.

図 10-12 shows a typical priority power multiplexing implementation using devices. When the MAIN power is present, the device in VIN_MAIN path powers the OUT bus irrespective of whether auxiliary power VIN_AUX is greater than or less than VIN_MAIN. Once the voltage on the VIN_MAIN rail falls below the user-defined threshold, the device VIN_MAIN issues a signal to switch over to auxiliary power VIN_AUX. The transition happens seamlessly in $t_{OVP(dly\_fast)}$, with minimal voltage droop on the output. The voltage droop during transition is a function of load current and output capacitance. See 式 13.

$$V_{(DROOP)} = \frac{I_{(LOAD)} x t_{OVP(fast\_dly)}}{C_{(OUT)}} \quad (13)$$

where

- $V_{(DROOP)}$ is in volts, $I_{(LOAD)}$ is load current in Ampere, $C_{(OUT)}$ is output capacitance in µF, $t_{OVP(fast\_dly)}$ = 140 µs (typical)

Figure 9-13, Figure 9-14, Figure 9-15 and figure 9-16 show typical switch-over waveforms of Priority Muxing implementation using the TPS26630 or TPS26631 for 20-V Primary and 24-V Auxiliary Bus.

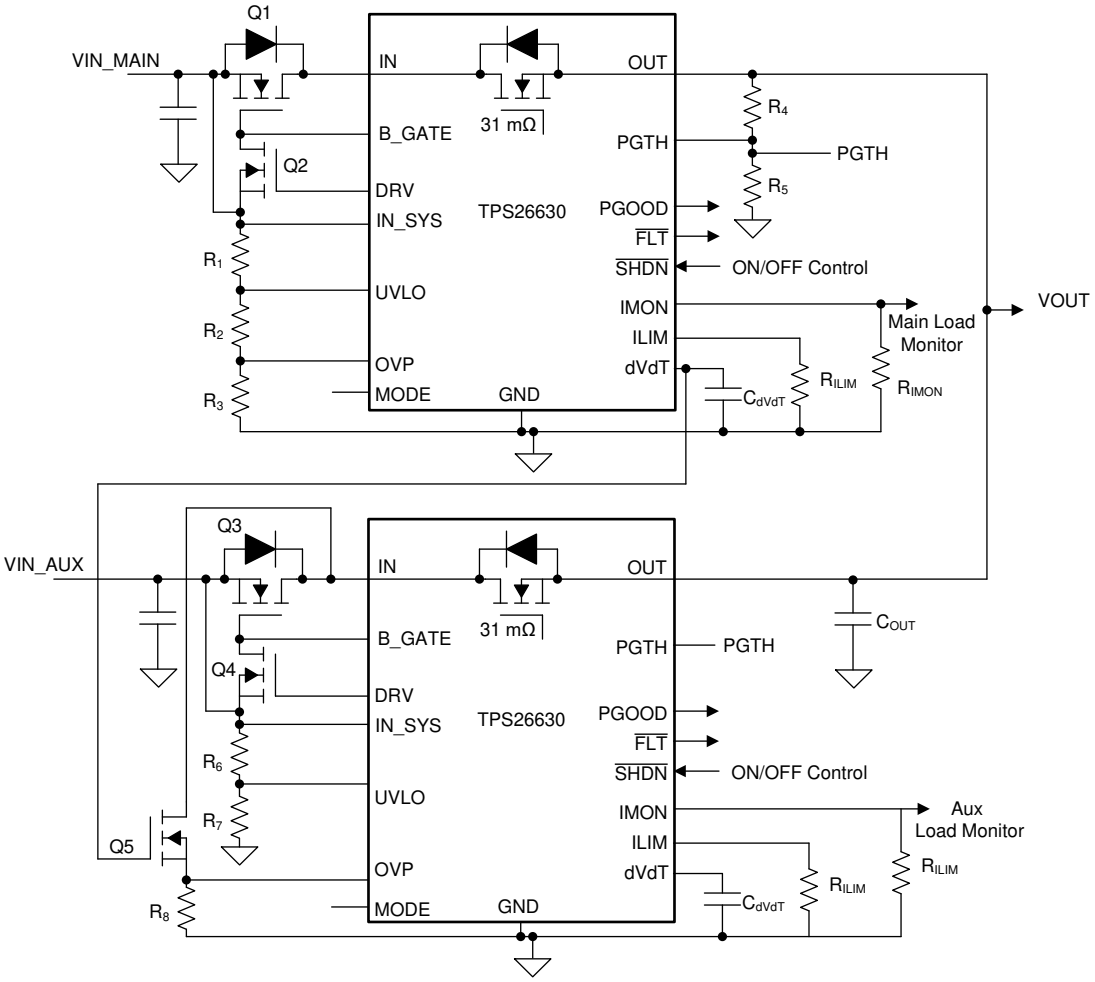


図 10-12. Priority Power Mux Implementation

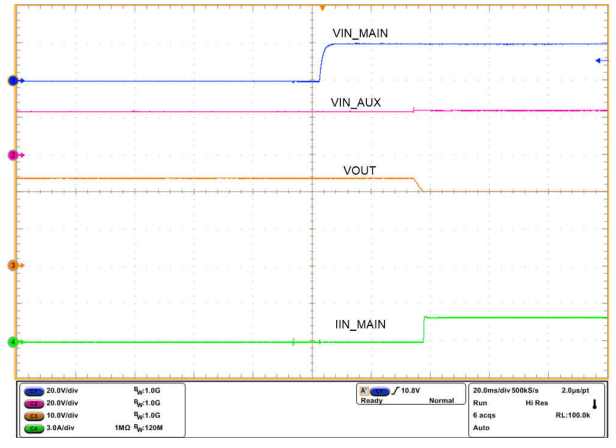


図 10-13. VIN_MAIN Power Recovery: Change Over from Auxiliary VIN_AUX to Primary Power VIN_MAIN

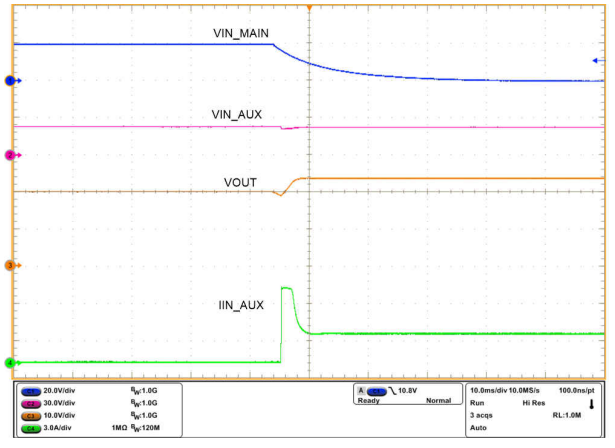


図 10-14. VIN_MAIN Brownout Condition: Change Over from Main VIN_MAIN to Auxiliary Power VIN_AUX

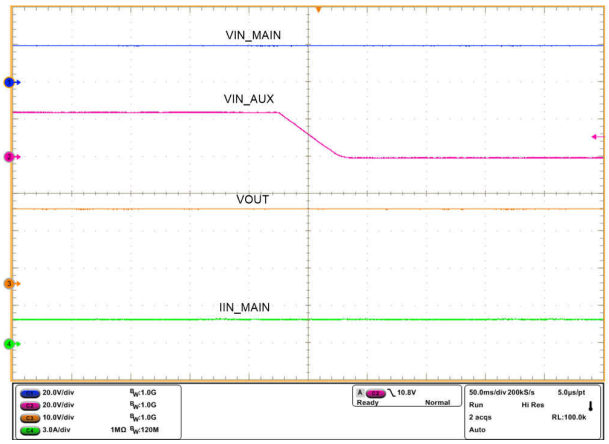


図 10-15. VIN_AUX Brownout Condition

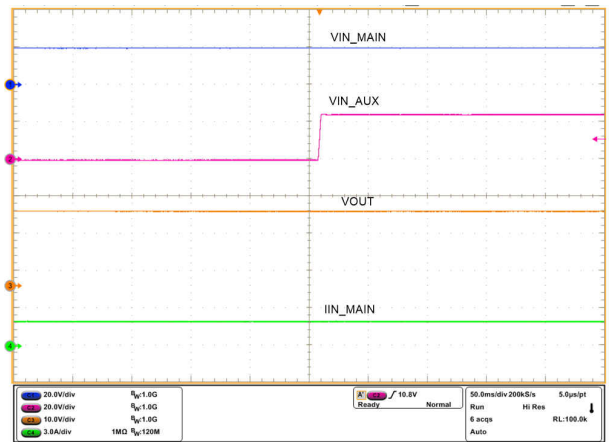


図 10-16. VIN_AUX Power Recovery

10.3.3 Input Protection for a Compact 24-V Auxiliary Power Supply for Servo Drives

TPS2663x eFuse protects the system from common faults such as reverse polarity, reverse power flow, overvoltage, undervoltage and overcurrents along with a robust EMC immunity performance. Refer to, *Compact, efficient, 24-V input auxiliary power supply reference design for servo drives* TI Design Guide for further information.

10.4 Do's and Don'ts

- In the applications where reverse polarity protection is required use external FETs Q1 and Q2.
- Connect at least a 300-kΩ resistor across UVLO and IN_SYS in the applications where reverse polarity protection is required.

11 Power Supply Recommendations

The TPS2663x eFuse is designed for the supply voltage range of 4.5 V ≤ V_{IN} ≤ 60 V. If the input supply is located more than a few inches from the device, an input ceramic bypass capacitor higher than 0.1 µF is recommended. Power supply must be rated higher than the current limit set to avoid voltage droops during overcurrent and short circuit conditions.

11.1 Transient Protection

In case of short circuit and overload current limit, when the device interrupts current flow, input inductance generates a positive voltage spike on the input and output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) depends on the value of inductance in series to the input or output of the device. These transients can exceed the *Absolute Maximum Ratings* of the device if steps are not taken to address the issue.

Typical methods for addressing transients include:

- Minimizing lead length and inductance into and out of the device
- Using large PCB GND plane
- Use of a Schottky diode across the output and GND to absorb negative spikes
- A low value ceramic capacitor ($C_{(IN)}$ to approximately 0.1 µF) to absorb the energy and dampen the transients.

The approximate value of input capacitance can be estimated with 式 14

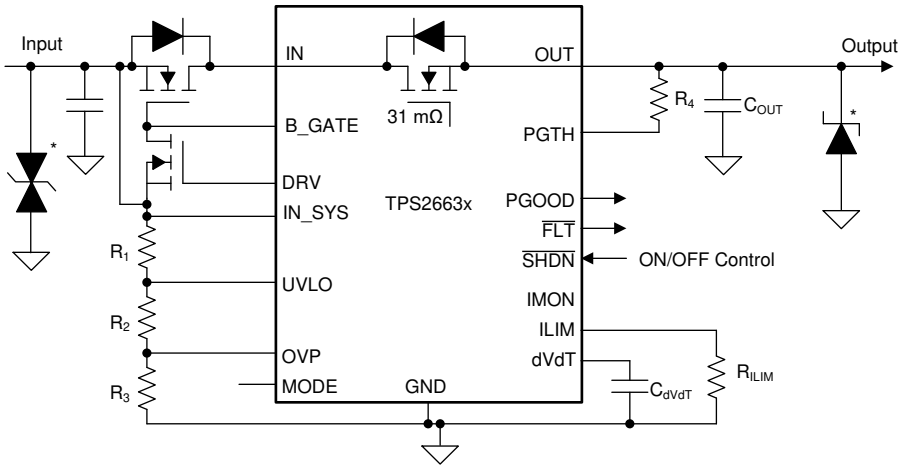
$$V_{spike(Absolute)} = V_{(IN)} + I_{(Load)} \times \sqrt{\frac{L_{(IN)}}{C_{(IN)}}} \quad (14)$$

where

- $V_{(IN)}$ is the nominal supply voltage
- $I_{(LOAD)}$ is the load current
- $L_{(IN)}$ equals the effective inductance seen looking into the source
- $C_{(IN)}$ is the capacitance present at the input

Some applications may require additional Transient Voltage Suppressor (TVS) to prevent transients from exceeding the *Absolute Maximum Ratings* of the device. These transients can occur during positive and negative surge tests on the supply lines. In such applications it is recommended to place at least 1 µF of input capacitor.

The circuit implementation with optional protection components (a ceramic capacitor, TVS and schottky diode) is shown in Figure 10-1.



* Optional components needed for suppression of transients

図 11-1. Circuit Implementation with Optional Protection Components for TPS2663x

12 Layout

12.1 Layout Guidelines

- For all the applications, a 0.1 µF or higher value ceramic decoupling capacitor is recommended between IN_SYS terminal and GND.
- The external FET Q1 should be placed with DRAIN close to the V_{IN} pins of the IC and connected through a plane. The fast pull down switch Q2 DRAIN and SOURCE should be placed very close to the GATE and SOURCE terminals of Q1 with very short loop. See 図 12-1 and 図 12-2 for a typical PCB layout example.
- The optimum placement of decoupling capacitor is closest to the IN_SYS and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN_SYS terminal, and the GND terminal of the IC.
- High current carrying power path connections must be as short as possible and must be sized to carry at least twice the full-load current.
- Locate all the TPS2663x family support components $R_{(ILIM)}$, $C_{(dVdT)}$, $R_{(IMON)}$, UVLO, OVP and PGTH resistors close to their connection pin. Connect the other end of the component to the GND with shortest trace length.
- The trace routing for the R_{ILIM} component to the device must be as short as possible to reduce parasitic effects on the current limit and current monitoring accuracy. These traces must not have any coupling to switching signals on the board.
- Protection devices such as TVS, snubbers, capacitors, or diodes must be placed physically close to the device they are intended to protect, and routed with short traces to reduce inductance. For example, a protection Schottky diode is recommended to address negative transients due to switching of inductive loads, and it must be physically close to the OUT and GND pins.
- Thermal Considerations: When properly mounted, the PowerPAD package provides significantly greater cooling ability. To operate at rated power, the PowerPAD must be soldered directly to the board GND plane directly under the device. Other planes, such as the bottom side of the circuit board can be used to increase heat sinking in higher current applications.

12.2 Layout Example

Top Layer
Bottom layer GND plane
Top Layer GND Plane
Via to Bottom Layer

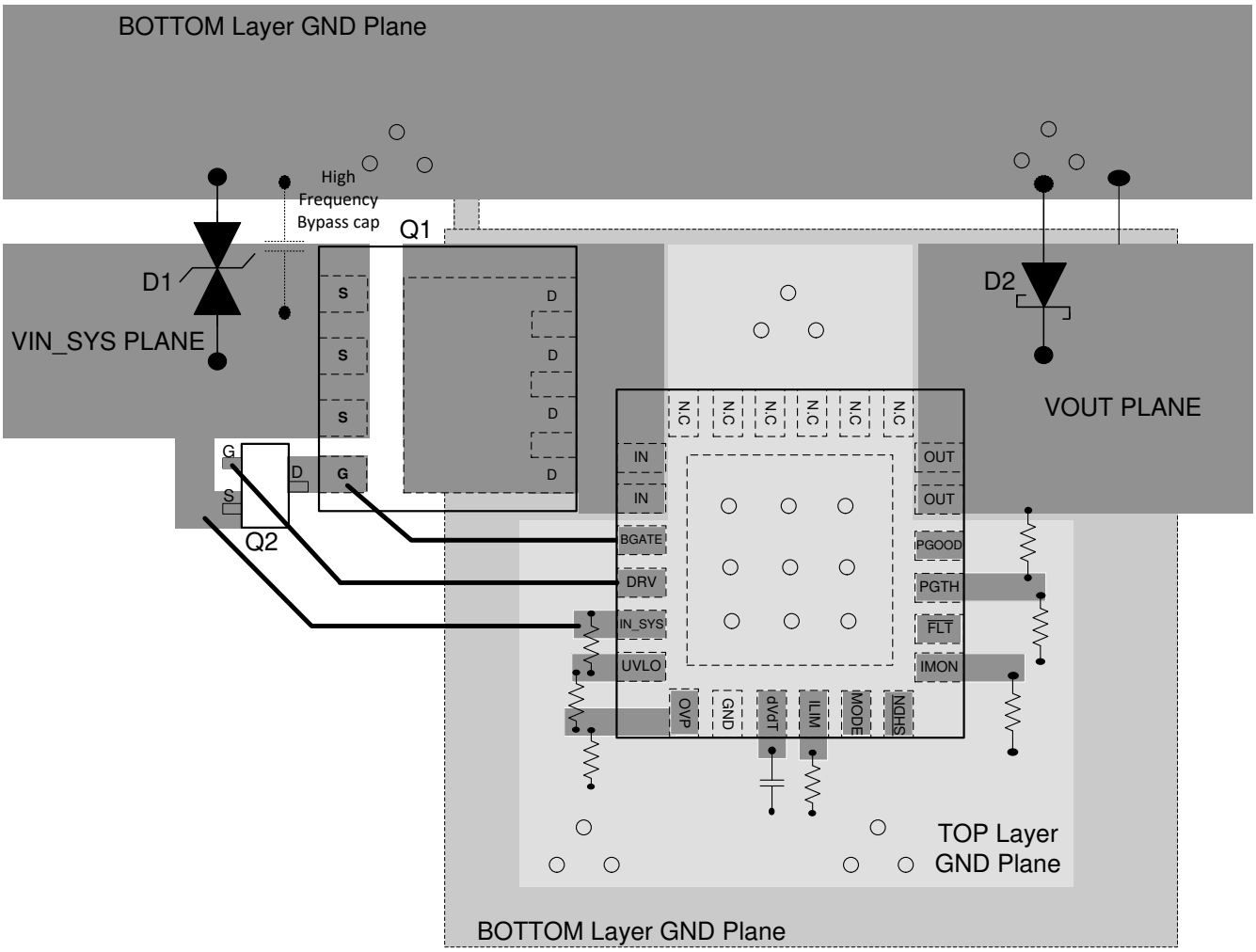


図 12-1. Typical PCB Layout Example With QFN Package With a 2 Layer PCB

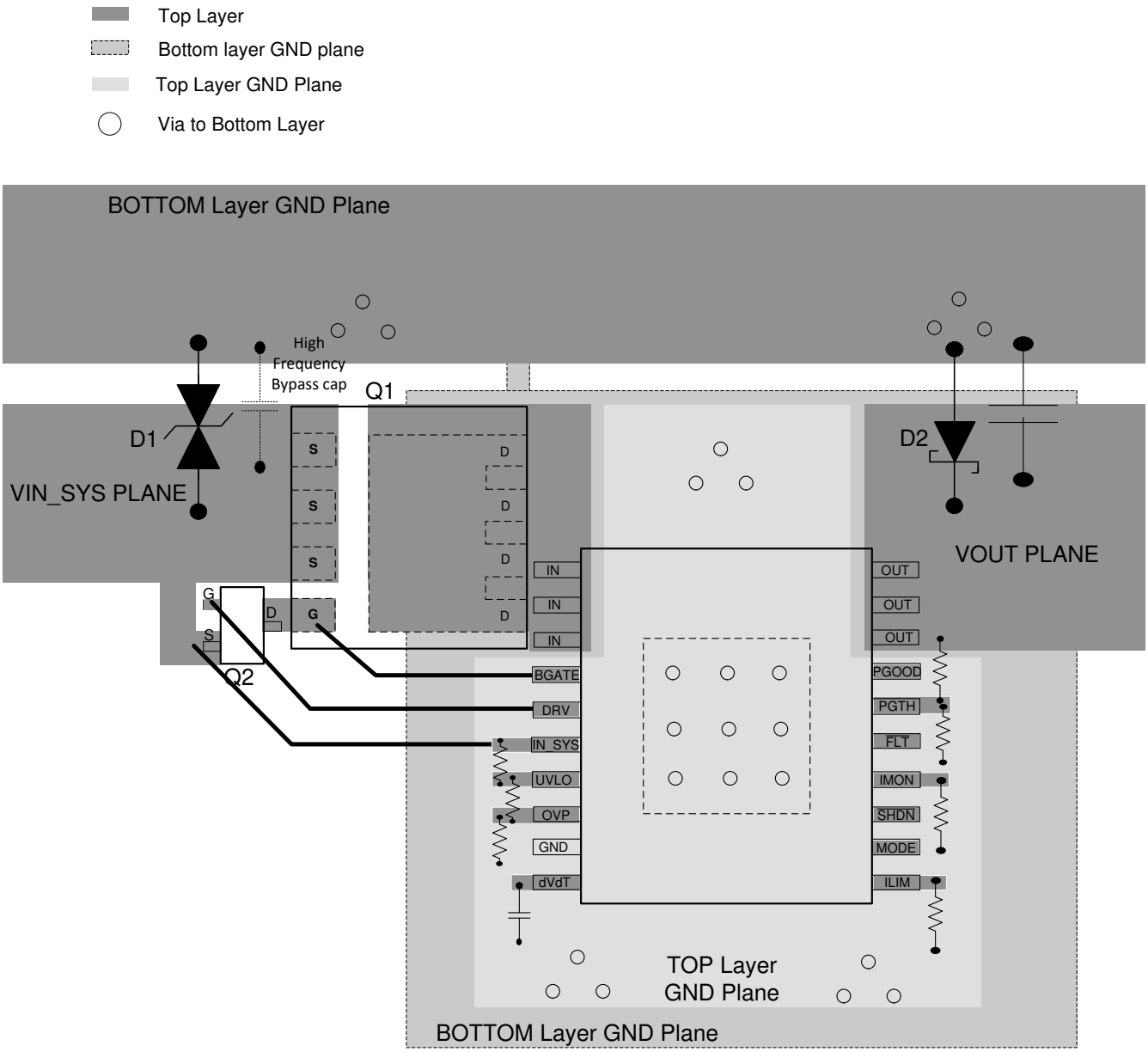


図 12-2. Typical PCB Layout Example With HTSSOP Package With a 2 Layer PCB

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

- *TPS2663 Design Calculator*
- *CPU (PLC Controller)*
- *Compact, efficient, 24-V input auxiliary power supply reference design for servo drives*

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 サポート・リソース

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すべての商標は、それぞれの所有者に帰属します。

13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

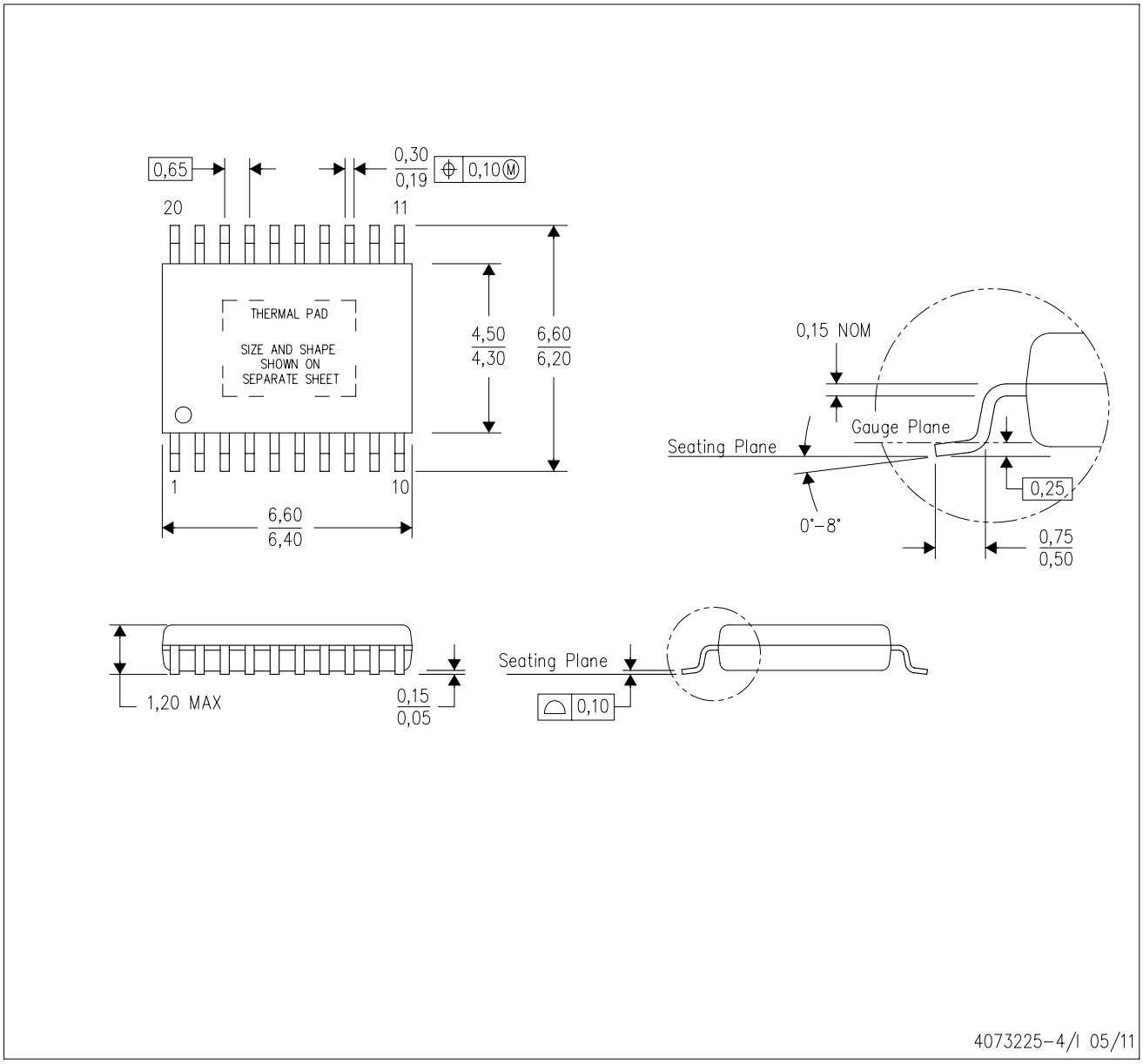
13.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

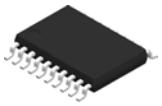
14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

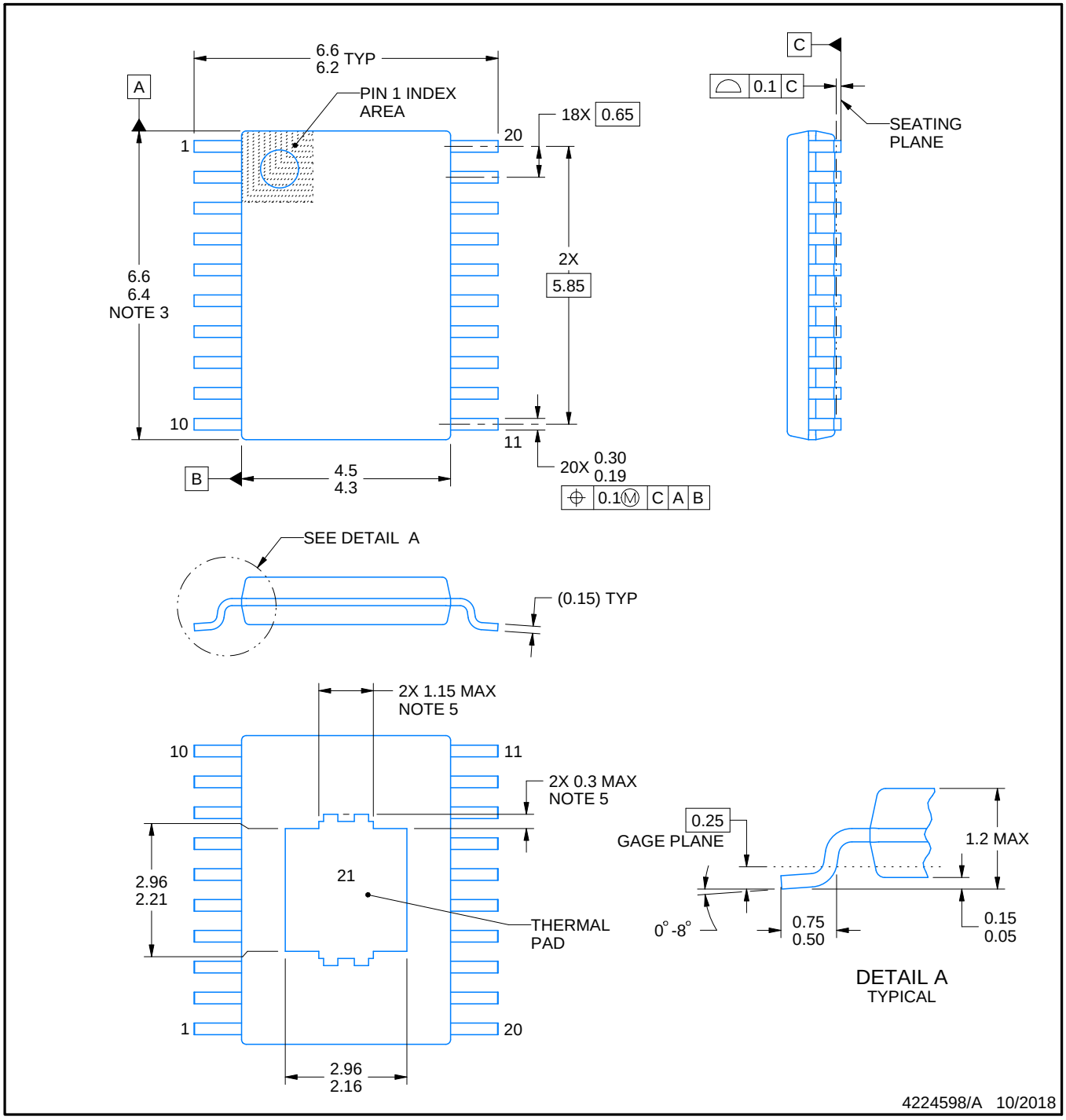


PACKAGE OUTLINE

PWP0020T

PowerPAD™ TSSOP - 1.2 mm max height

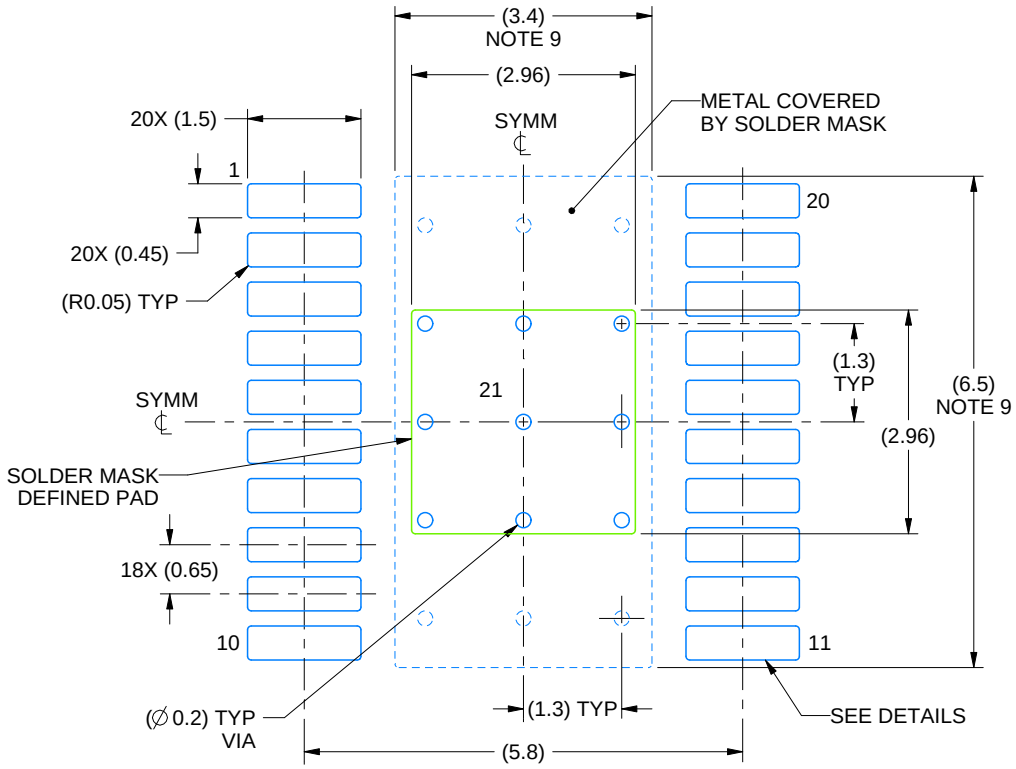
SMALL OUTLINE PACKAGE



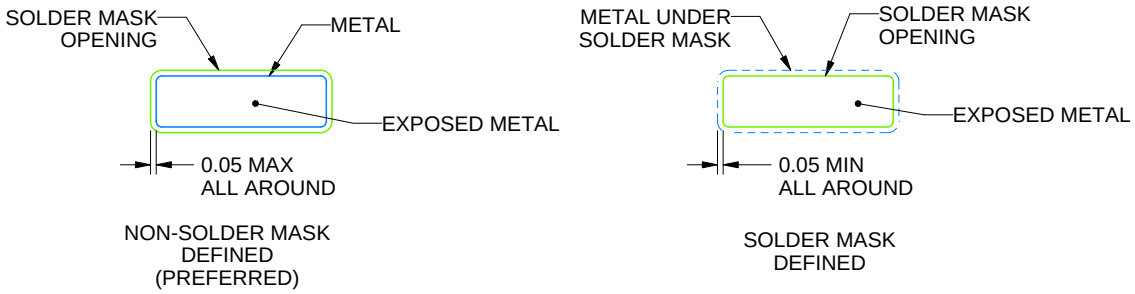
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

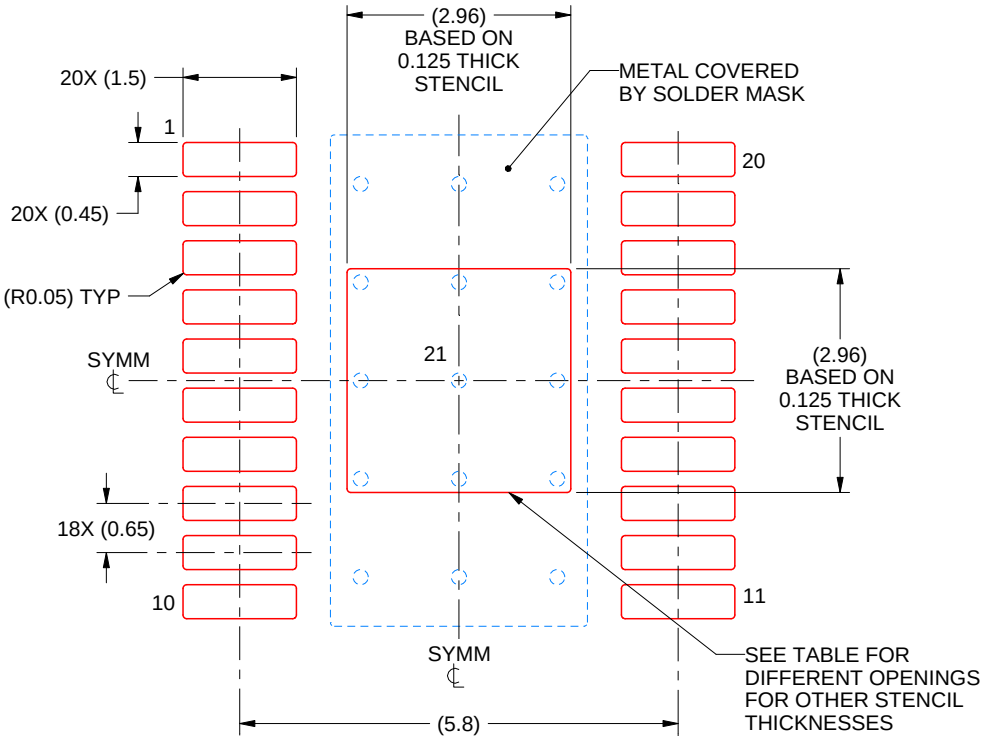


SOLDER MASK DETAILS

4224598/A 10/2018

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.31 X 3.31
0.125	2.96 X 2.96 (SHOWN)
0.15	2.70 X 2.70
0.175	2.50 X 2.50

4224598/A 10/2018

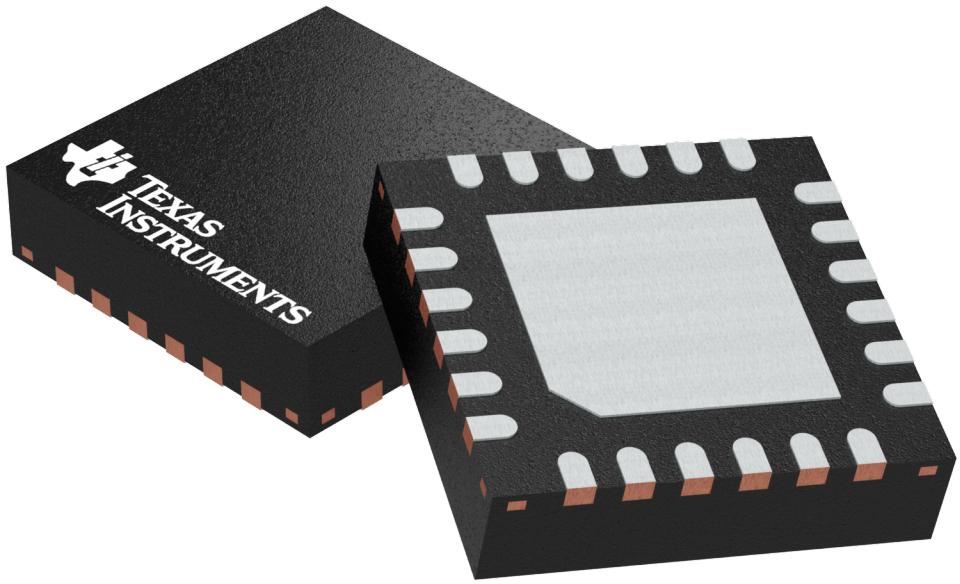
NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

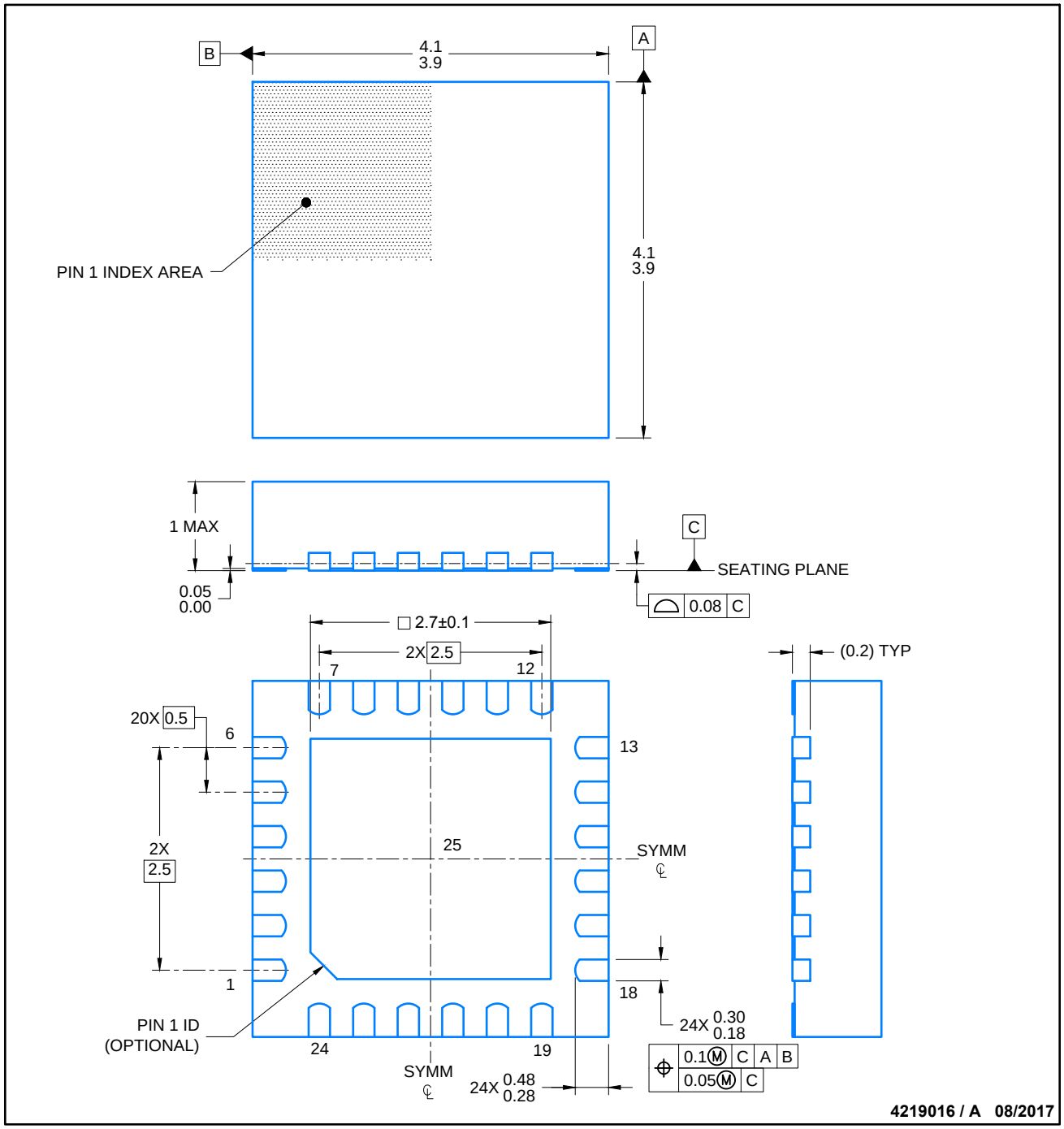
4204104/H

PACKAGE OUTLINE

RGE0024H

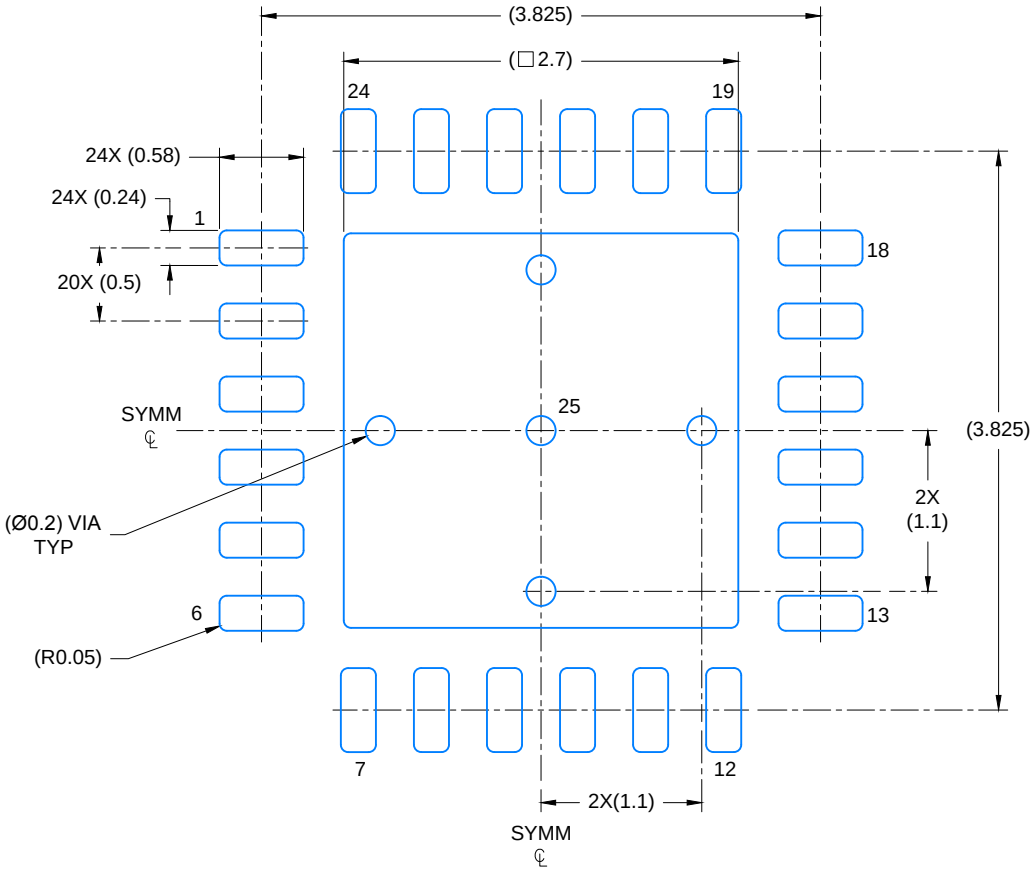
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



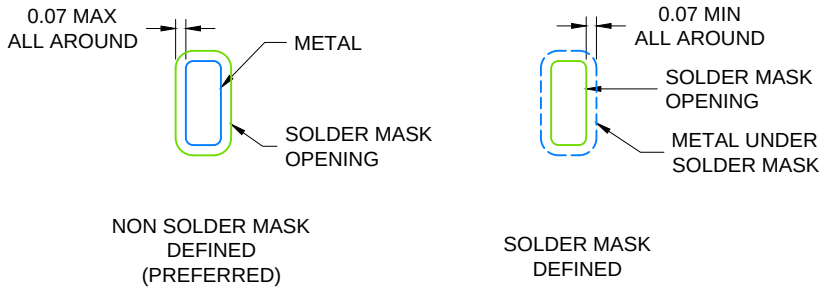
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 20X

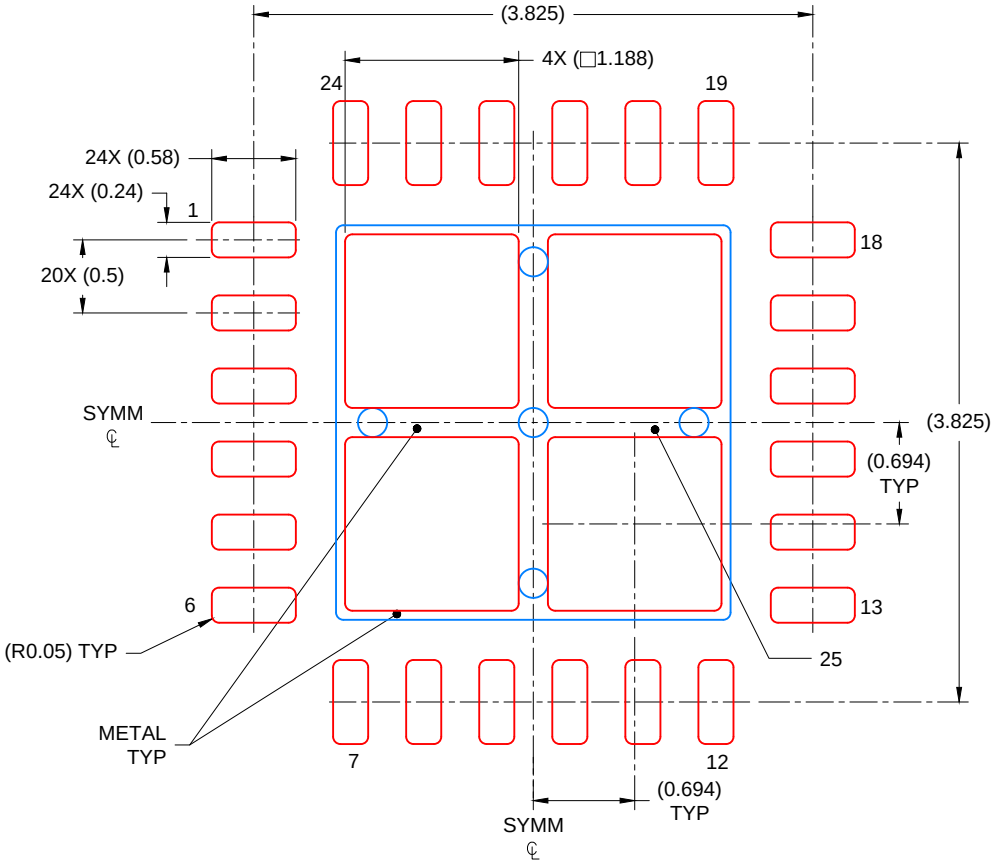


SOLDER MASK DETAILS

4219016 / A 08/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 20X

4219016 / A 08/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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