

# TPS6208x 1.2A高効率降圧型コンバータ、DCS-Control™

## およびスヌーズ・モード搭載

### 1 特長

- DCS-Control™アーキテクチャにより高速の過渡レギュレーションを実現
- スヌーズ・モードでの非常に低い静止電流: 6.5μA
- 入力電圧範囲: 2.3V~6V
- 100%デューティ・サイクル動作により低いドロップアウト電圧を実現
- パワーセーブ・モードによる軽負荷時の効率向上
- 出力放電機能
- 短絡保護
- パワー・グッド出力
- サーマル・シャットダウン
- 2mmx2mmの8ピンWSONパッケージで供給

### 2 アプリケーション

- バッテリー駆動の携帯機器
- ポイント・オブ・ロード・レギュレータ
- システム電源レールの電圧変換

### 3 概要

TPS6208xデバイスは、高周波数の同期整流降圧型コンバータのファミリーです。入力電圧範囲が2.3V~6Vで、一般的なバッテリー・テクノロジーをサポートします。または、このデバイスを低電圧のシステム電源レールとしても使用できます。

TPS6208xは、広い出力電流範囲にわたって高効率の降圧型変換を行うことに特化しています。中負荷から重負荷ではPWMモードで動作し、軽負荷電流時には自動的にパワーセーブ・モードへ移行するため、負荷電流のあらゆる範囲にわたって高効率が維持されます。非常に小さい負荷から無負荷電流時まで高い効率を維持するために、静止電流の非常に低いスヌーズ・モードが実装されています。この機能はMODEピンによって有効化され、バッテリー駆動アプリケーションの稼働時間を延ばし、スタンバイ電流を最低レベルに維持することで、低いスタンバイ電流を目標としたグリーン・エネルギーの基準を満たしています。

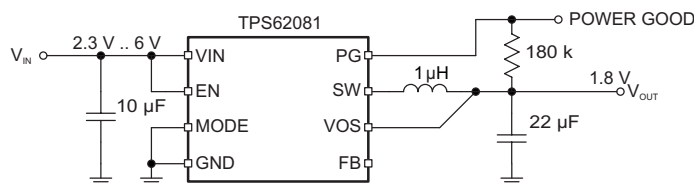
システム電源レールの要件に対応するため、内部のループ補償によって100μFを超える外部出力コンデンサを幅広い選択肢から選ぶことができます。DCS-Control™アーキテクチャにより、優れた負荷過渡性能と出力電圧レギュレーション精度を実現しています。このデバイスは、2mmx2mmのサーマル・パッド付きWSONパッケージで供給されます。

### 製品情報<sup>(1)</sup>

型番	パッケージ	本体サイズ(公称)
TPS62080	WSON (8)	2.00mmx2.00mm
TPS62080A		
TPS62081		
TPS62082		

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

### 代表的なアプリケーションの回路図



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## 4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision E (April 2015) から Revision F に変更	Page
• Changed From: $T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$ To: $T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$ in the <i>Electrical Characteristics</i> condition statement .....	6
• Added a Test Condition to $I_{SD}$ in the <i>Electrical Characteristics</i> .....	6
• Changed the $R_{DS(on)}$ High-side TYP value From: 120 m $\Omega$ To: 95 m $\Omega$ in the <i>Electrical Characteristics</i> .....	6
• Changed the $R_{DS(on)}$ Low-side TYP value From: 90 m $\Omega$ To: 70 m $\Omega$ in the <i>Electrical Characteristics</i> .....	6
• Changed the graphs to include a 125 $^\circ\text{C}$ curve in the <i>Typical Characteristics</i> .....	7
• Added 50 $\Omega$ value to the Power Good block in <a href="#">Figure 5</a> .....	8
• Added 50 $\Omega$ value to the Power Good block in <a href="#">Figure 6</a> .....	9
• Added <a href="#">Table 1</a> .....	9

Revision D (July 2013) から Revision E に変更	Page
• 「ピン構成および機能」セクション、「ESD定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクション 追加.....	1

Revision C (May 2013) から Revision D に変更	Page
• Deleted TPS62080ADGN from ORDERING INFORMATION table .....	4
• Deleted TPS62080A column from the <i>Thermal Information</i> table.....	5

Revision B (March 2012) から Revision C に変更	Page
• Changed the Thermal Information tables values.....	5

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**Revision A (February 2012) から Revision B に変更****Page**

- 
- Changed TPS62080ADSG from Product Preview to Production Data in ORDERING INFORMATION..... 4
- 

**2011年9月発行のものから更新****Page**

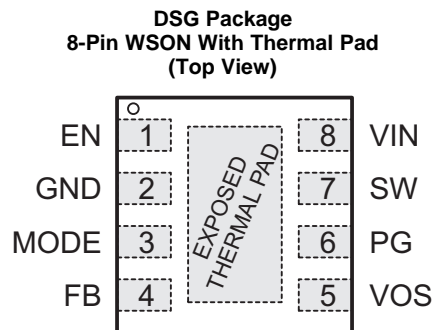
- 
- TPS62080Aデバイス 追加 ..... 1
  - Added TPS62080ADSG (Product Preview) and TPS62080ADGN (Product Preview) to ORDERING INFORMATION ..... 4
  - Added TPS62080A output discharge resistor ..... 6
-

## 5 Device Comparison Table

PART NUMBER <sup>(1)</sup>	OUTPUT VOLTAGE <sup>(2)</sup>	OUTPUT DISCHARGE RESISTOR	PACKAGE MARKING	PACKAGE
TPS62080DSG	Adjustable	1 k $\Omega$	QVR	8-Pin WSON
TPS62081DSG	1.8 V	1 k $\Omega$	QVS	8-Pin WSON
TPS62082DSG	3.3 V	1 k $\Omega$	QVT	8-Pin WSON
TPS62080ADSG	Adjustable	40 $\Omega$	SBN	8-Pin WSON

- (1) For detailed ordering information, see [メカニカル、パッケージ、および注文情報](#).  
 (2) Contact the factory to check availability of other fixed output voltage versions.

## 6 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	1	IN	Device Enable Logic Input. Logic HIGH enables the device, logic LOW disables the device and turns it into shutdown. Do not leave floating.
GND	2	PWR	Power and Signal Ground.
MODE	3	IN	Snooze Mode Enable Logic Input. Logic HIGH enables the Snooze Mode, logic LOW disables the Snooze Mode. Do not leave floating.
FB	4	IN	Feedback Pin for the internal control loop. Connect this pin to the external feedback divider for the adjustable output versions. For the fixed output voltage versions, this pin must be left floating or connected to GND.
VOS	5	IN	Output Voltage Sense Pin for the internal control loop. Must be connected to output voltage.
PG	6	OUT	Power Good open drain output. This pin is pulled to low if the output voltage is below regulation limits. Can be left floating if not used.
SW	7	PWR	Switch Pin connected to the internal MOSFET switches and inductor terminal. Connect the inductor of the output filter here.
VIN	8	PWR	Power Supply Voltage Input.
Exposed Thermal Pad	—	—	Connect it to GND. The thermal pad must be soldered to achieve appropriate power dissipation and mechanical reliability.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

	MIN	MAX	UNIT
Voltage at VIN, PG, VOS <sup>(2)</sup>	-0.3	7	V
Voltage at SW <sup>(2)(3)</sup>	-1	7	V
Voltage at FB <sup>(2)</sup>	-0.3	3.6	V
Voltage at EN, MODE <sup>(2)</sup>	-0.3	VIN + 0.3	V
Sink current at PG	0	0.5	mA
Operating junction temperature, T <sub>J</sub>	-40	150	°C
Storage temperature, T <sub>stg</sub>	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.
- (3) During operation, device switching.

### 7.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions<sup>(1)</sup>

		MIN	NOM	MAX	UNIT
V <sub>IN</sub>	Input voltage	2.3		6	V
V <sub>OUT</sub>	Output voltage	0.5		4	V
I <sub>SNOOZE</sub>	Load current in Snooze Mode			2	mA
T <sub>J</sub>	Operating junction temperature	-40		125	°C

- (1) Refer to the [Application and Implementation](#) section for further information.

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS6208x	UNIT
		DSG (WSON)	
		8 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	59.7	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	70.1	
R <sub>θJB</sub>	Junction-to-board thermal resistance	30.9	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	1.4	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	31.5	
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	8.6	

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.5 Electrical Characteristics

Over recommended free-air temperature range,  $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . Typical values are at  $T_A = 25^{\circ}\text{C}$  (unless otherwise noted),  $V_{IN} = 3.6\text{ V}$ ,  $\text{MODE} = \text{LOW}$ .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY</b>						
$V_{IN}$	Input voltage range		2.3		6	V
$I_Q$	Quiescent current into $V_{IN}$	$I_{OUT} = 0\text{ mA}$ , Device not switching		30		$\mu\text{A}$
	Quiescent current into $V_{IN}$ (SNOOZE MODE)	$I_{OUT} = 0\text{ mA}$ , Device not switching, $\text{MODE} = \text{HIGH}$		6.5		$\mu\text{A}$
$I_{SD}$	Shutdown current into $V_{IN}$	EN = LOW $T_A = -40^{\circ}\text{C}$ to $85^{\circ}\text{C}$			7	$\mu\text{A}$
					1	
$V_{UVLO}$	Undervoltage lockout	Input voltage falling		1.8	2	V
	Undervoltage lockout hysteresis	Rising above $V_{UVLO}$		120		mV
$T_{JSD}$	Thermal shutdown	Temperature rising		150		$^{\circ}\text{C}$
	Thermal shutdown hysteresis	Temperature falling below $T_{JSD}$		20		$^{\circ}\text{C}$
<b>LOGIC INTERFACE (EN MODE)</b>						
$V_{IH}$	High level input voltage	$2.3\text{ V} \leq V_{IN} \leq 6\text{ V}$	1			V
$V_{IL}$	Low level input voltage	$2.3\text{ V} \leq V_{IN} \leq 6\text{ V}$			0.4	V
$I_{LKG}$	Input leakage current			0.01	0.5	$\mu\text{A}$
<b>POWER GOOD</b>						
$V_{PG}$	Power good threshold	$V_{OUT}$ falling referenced to $V_{OUT}$ nominal	-15%	-10%	-5%	
	Power good hysteresis			5%		
$V_{OL}$	Low level voltage	$I_{sink} = 500\ \mu\text{A}$			0.3	V
$I_{PG,LKG}$	PG Leakage current	$V_{PG} = 5.0\text{ V}$		0.01	0.1	$\mu\text{A}$
<b>OUTPUT</b>						
$V_{OUT}$	Output voltage range TPS62080, TPS62080A		0.5		4.0	V
	Output voltage accuracy TPS62081	$I_{OUT} = 0\text{ mA}$ ; $V_{IN} \geq 2.3\text{ V}$	-2.5%		2.5%	
	Output voltage accuracy TPS62082	$I_{OUT} = 0\text{ mA}$ ; $V_{IN} \geq 3.6\text{ V}$	-2.5%		2.5%	
	Snooze Mode output voltage accuracy	$\text{MODE} = \text{HIGH}$ ; $V_{IN} \geq 2.3\text{ V}$ and $V_{IN} \geq V_{OUT} + 1\text{ V}$	-5%		5%	
$V_{FB}$	Feedback regulation voltage TPS62080, TPS62080A	$V_{IN} \geq 2.3\text{ V}$ and $V_{IN} \geq V_{OUT} + 1\text{ V}$	0.438	0.45	0.462	V
$I_{FB}$	Feedback input bias current TPS62080, TPS62080A	$V_{FB} = 0.45\text{ V}$		10	100	nA
$R_{DIS}$	Output discharge resistor	EN = LOW, $V_{OUT} = 1.8\text{ V}$		1		k $\Omega$
		TPS62080A, EN = LOW, $V_{OUT} = 1.2\text{ V}$	25	40	65	$\Omega$
	Line Regulation			0		%/V
	Load Regulation	TPS62081, TPS62082		-0.25		%/A
$R_{DS(on)}$	High-side FET ON-resistance	$I_{SW} = 500\text{ mA}$		95		m $\Omega$
	Low-side FET ON-resistance	$I_{SW} = 500\text{ mA}$		70		m $\Omega$
$I_{LIM}$	High-side FET switch current limit	Rising inductor current	1.6	2.8	4	A

## 7.6 Typical Characteristics

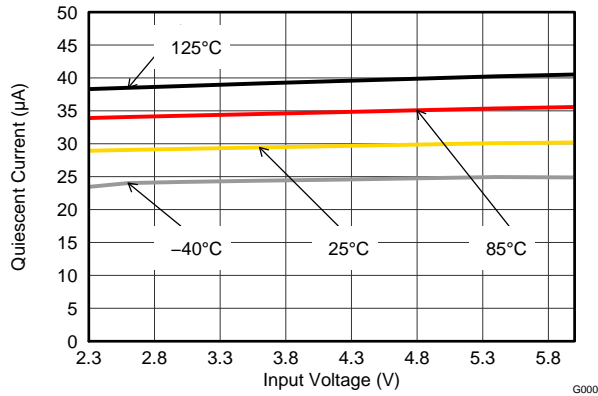


Figure 1. Quiescent Current vs Input Voltage in Normal Mode

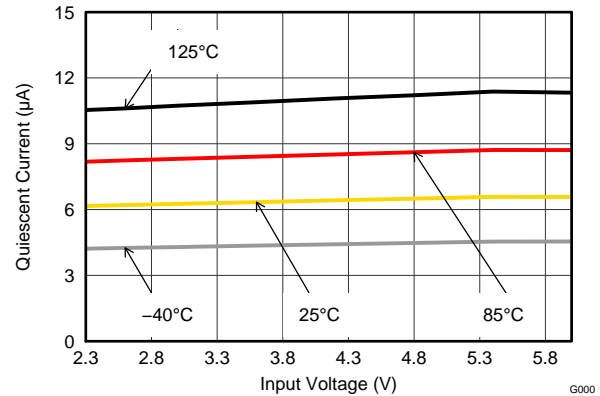


Figure 2. Quiescent Current vs Input Voltage in Snooze Mode

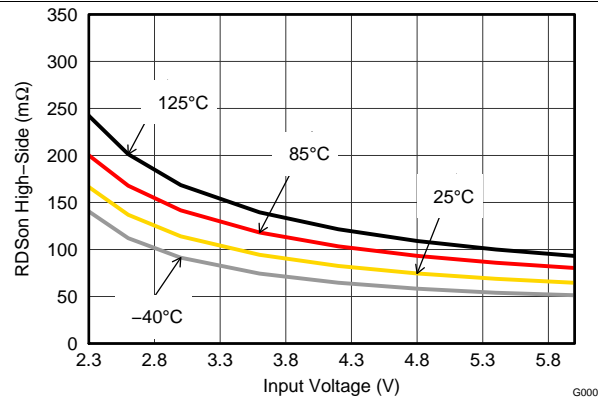


Figure 3. High-Side FET R<sub>DS(on)</sub> vs Input Voltage

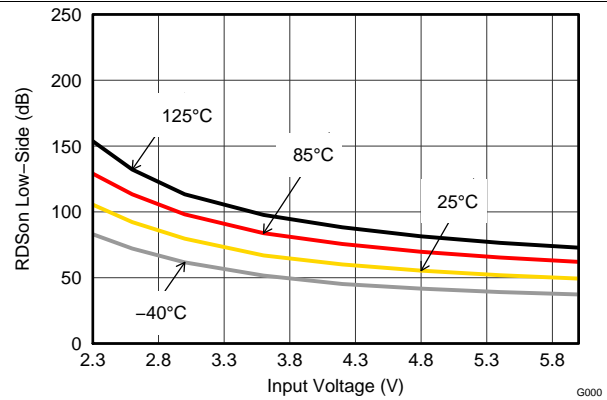


Figure 4. Low-Side FET R<sub>DS(on)</sub> vs Input Voltage

## 8 Detailed Description

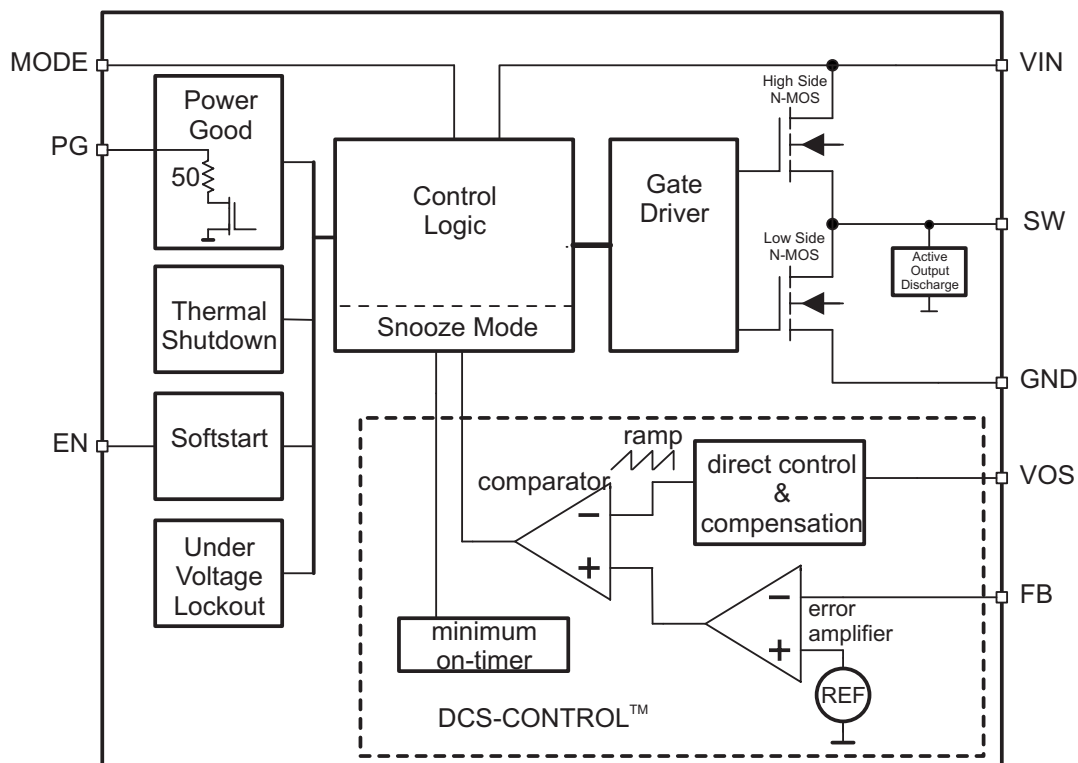
### 8.1 Overview

The TPS6208x synchronous switched mode converters are based on DCS-Control™ (Direct Control with Seamless transition into Power Save Mode). This is an advanced regulation topology that combines the advantages of hysteretic, voltage and current mode control.

The DCS-Control topology operates in pulse width modulation (PWM) mode for medium to heavy load conditions and in Power Save Mode at light load currents. In PWM mode, the converter operates with its nominal switching frequency of 2 MHz having a controlled frequency variation over the input voltage range. As the load current decreases, the converter enters Power Save Mode, reducing the switching frequency and minimizing the IC quiescent current to achieve high efficiency over the entire load current range. DCS-Control supports both operation modes (PWM and PFM) using a single building block having a seamless transition from PWM to Power Save Mode without effects on the output voltage. Fixed output voltage versions provide smallest solution size combined with lowest no load current consumption. The TPS6208x offers both excellent DC voltage and superior load transient regulation, combined with very low output voltage ripple, minimizing interference with RF circuits.

The device is equipped with Snooze Mode functionality, which is enabled with the MODE pin. Snooze Mode supports high efficiency conversion at lowest output currents below 2 mA. If no load current is drawn, the ultra low quiescent current of 6.5  $\mu\text{A}$  is sufficient to maintain the output voltage. This extends battery run time by reducing the quiescent current during lowest or no load conditions in battery-driven applications. For mains-operated voltage supplies, Snooze Mode reduces the system's stand-by energy consumption. During shutdown (EN = LOW), the device reduces energy consumption to less than 1  $\mu\text{A}$ .

### 8.2 Functional Block Diagrams

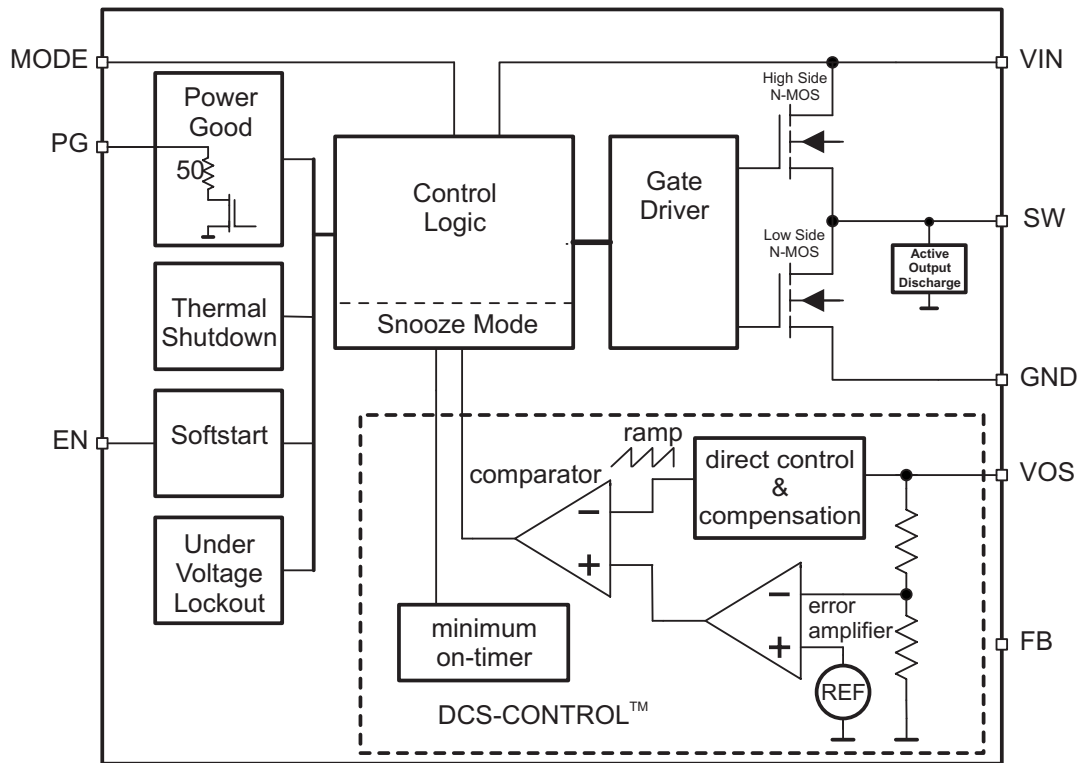


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**Figure 5. Functional Block Diagram (Adjustable Output Voltage Version)**



Functional Block Diagrams (continued)



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Figure 6. Functional Block Diagram (Fixed Output Voltage Version)

8.3 Feature Description

8.3.1 Power Good

The TPS6208x has a power good output which goes low when the output voltage is below its nominal value. The power good is high impedance once the output is above 95% of the regulated voltage, and is driven to low once the output voltage falls below typically 90% of the regulated voltage. The PG pin is an open drain output and can sink up to 0.5 mA. The power good output requires a pull-up resistor. When the device is off due to disable, UVLO or thermal shutdown, the PG pin is high impedance (see Table 1). The PG signal can be used for sequencing of multiple rails by connecting to the EN pin of other converters. Leave the PG pin unconnected when not used.

Table 1. Power Good Pin Logic Table

Device Information		PG Logic Status	
		High Z	Low
Enable (EN=High)	$V_{FB} \geq V_{PG}$	√	
	$V_{FB} \leq V_{PG}$		√
Shutdown (EN=Low)		√	
UVLO	$0.7V < V_{IN} < V_{UVLO}$	√	
Thermal Shutdown	$T_J > T_{JSD}$	√	
Power Supply Removal	$V_{IN} < 0.7V$	√	

### 8.3.2 100% Duty Cycle Low Dropout Operation

The device offers low input to output voltage difference by entering 100% duty cycle mode. In this mode, the high-side MOSFET switch is constantly turned on and the low-side MOSFET is switched off. This is particularly useful in battery powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage to maintain an output voltage is calculated as:

$$V_{IN,MIN} = V_{OUT} + I_{OUT,MAX} \times (R_{DS(on)} + R_L)$$

where

- $V_{IN,MIN}$  = Minimum input voltage
- $I_{OUT,MAX}$  = Maximum output current
- $R_{DS(on)}$  = High-side FET ON-resistance
- $R_L$  = Inductor ohmic resistance

(1)

### 8.3.3 Output Discharge

The output gets discharged by the SW pin with a typical discharge resistor of  $R_{DIS}$  whenever the device shuts down. This is the case when the device gets disabled by enable, thermal shutdown, or undervoltage lockout. The TPS6208A differs from the TPS62080 only in its stronger discharge.

### 8.3.4 Soft-Start

When EN is set to start device operation, the device starts switching after a delay of about 40  $\mu$ s and VOUT rises with a slope of about 10mV/ $\mu$ s (See [Figure 27](#) and [Figure 29](#) for typical startup operation). This avoids excessive inrush current and creates a smooth output voltage rise slope. It also prevents excessive voltage drops of primary cells and rechargeable batteries with high internal impedance.

If the output voltage is not reached within the soft start time, such as in the case of heavy load, the converter enters regular operation. Consequently, the inductor current limit operates as described below. The TPS6208x is able to start into a pre-biased output capacitor. The converter starts with the applied bias voltage and ramps up the output voltage to its nominal value.

### 8.3.5 Undervoltage Lockout

To avoid mis-operation of the device at low input voltages, an undervoltage lockout is implemented that shuts down the device at voltages lower than  $V_{UVLO}$  with a 120 mV typical hysteresis.

### 8.3.6 Thermal Shutdown

The device goes into thermal shutdown once the junction temperature exceeds typically  $T_{JSD}$ . Once the device temperature falls below the threshold minus hysteresis, the device returns to normal operation automatically.

### 8.3.7 Inductor Current Limit

The Inductor Current Limit prevents the device from high inductor current and drawing excessive current from the battery or input voltage rail. Excessive current might occur with a shorted/saturated inductor or a heavy load/shorted output circuit condition.

The incorporated inductor peak current limit measures the current in the high-side and low-side power MOSFET. Once the high-side switch current limit is tripped, the high-side MOSFET is turned off and the low-side MOSFET is turned on to reduce the inductor current. When the inductor current drops down to the low-side switch current limit, the low-side MOSFET is turned off and the high-side switch is turned on again. This operation repeats until the inductor current does not reach the high-side switch current limit. Due to internal propagation delays, the real current limit value can exceed the static current limit in [Electrical Characteristics](#).

## 8.4 Device Functional Modes

### 8.4.1 Enabling and Disabling the Device

The device is enabled by setting the EN input to a logic HIGH. Accordingly, a logic LOW disables the device. If the device is enabled, the internal power stage starts switching and regulates the output voltage to the programmed threshold. The EN input must be terminated and not left floating.

### 8.4.2 Power Save Mode

As the load current decreases, the TPS6208x enters Power Save Mode operation. During Power Save Mode, the converter operates with reduced switching frequency in PFM mode and with a minimum quiescent current maintaining high efficiency. Power Save Mode occurs when the inductor current becomes discontinuous. It is based on a fixed on time architecture. The typical on time is given by  $t_{on} = 500 \text{ ns} \times (V_{OUT}/V_{IN})$ . The switching frequency over the whole load current range is shown in [Figure 21](#) and [Figure 22](#).

### 8.4.3 Snooze Mode

The TPS6208x offers a Snooze Mode function. If Snooze Mode is enabled by an external logic signal setting the MODE pin to HIGH, the device's quiescent current consumption is reduced to typically 6.5  $\mu\text{A}$ . As a result, the high efficiency range is extended towards the range of lowest output currents below 2 mA. See the efficiency figures in [Application Curves](#).

If the device is operating in Snooze Mode, a dedicated, low power consuming block monitors the output voltage. All other control blocks are snoozing during that time. If the output voltage falls below the programmed output voltage by 3.5% (typ), the control blocks wake up, regulate the output voltage and allow themselves to snooze again until the output voltage drops again. Snooze Mode operation provides a clear efficiency improvement at lowest output currents. If the load current increases, the advantage of efficiency in Snooze mode is reduced. Because the dynamic load regulation operates best if Snooze Mode is disabled, it is recommended to turn off Snooze Mode when the load current exceeds 2 mA. Generally, a microcontroller operates the MODE pin.

## 9 Application and Implementation

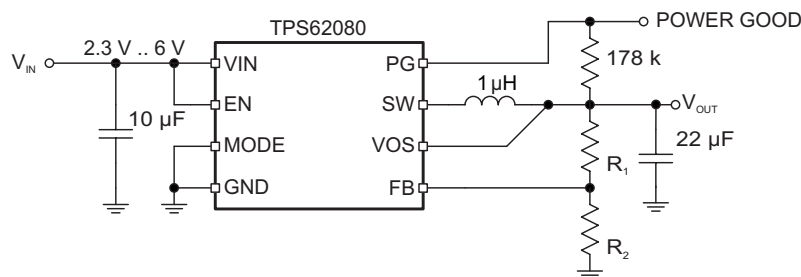
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The TPS62080 and TPS62080A are synchronous step-down converter whose output voltage is adjusted by component selection. The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference. The TPS62081 and TPS62082 provide a fixed output voltage which do not need an external resistor divider.

### 9.2 Typical Application



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**Figure 7. Typical Application Schematic**

#### 9.2.1 Design Requirements

For this design example, use [Table 2](#) as the input parameters.

**Table 2. Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	2.3 V to 6 V
Output voltage	1.2 V
Output ripple voltage	< 20 mV
Maximum output current	1.2 A

#### 9.2.2 Detailed Design Procedure

[Table 3](#) lists the components used for the example.

**Table 3. List of Components**

REFERENCE	DESCRIPTION	MANUFACTURER
C1	10 uF, Ceramic Capacitor, 6.3 V, X5R, size 0603	Std
C2	22 uF, Ceramic Capacitor, 6.3 V, X5R, size 0805, GRM21BR60J226ME39L	Murata
L1	1.0 µH, Power Inductor, 2.2 A, size 3 × 3 × 1.2 mm, XFL3012-102MEB	Coilcraft
R1	Depending on the output voltage of TPS62080, 1%; Not populated for TPS62081, TPS62082;	Std
R2	39.2k, Chip Resistor, 1/16W, 1%, size 0603	Std
R3	178k, Chip Resistor, 1/16W, 1%, size 0603	Std

### 9.2.2.1 Setting the Output Voltage

The TPS608x devices are available as fixed and adjustable output voltage versions. The fixed voltage versions are internally programmed to a fixed output voltage, whereas the adjustable output voltage version needs to be programmed via an external voltage divider to set the desired output voltage.

#### 9.2.2.1.1 Adjustable Output Voltage Version

For the adjustable output voltage version, an external resistor divider is used. By selecting  $R_1$  and  $R_2$ , the output voltage is programmed to the desired value.

When the output voltage is regulated, the typical voltage at the FB pin is  $V_{FB}$  for the adjustable devices. The following equation can be used to calculate  $R_1$  and  $R_2$ .

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right) = 0.45V \times \left(1 + \frac{R_1}{R_2}\right) \quad (2)$$

For best accuracy,  $R_2$  should be kept smaller than  $40k\Omega$  to ensure that the current flowing through  $R_2$  is at least 100 times larger than  $I_{FB}$ . Changing towards a lower value increases the robustness against noise injection. Changing towards higher values reduces the input current. For lowest input current during Snooze Mode, it is recommended to use a fixed output voltage version such as TPS62081 and TPS62082.

#### 9.2.2.2 Output Filter Design

The inductor and the output capacitor together provide a low pass filter. To simplify this process, [Table 4](#) outlines possible inductor and capacitor value combinations for most applications. Checked cells represent combinations that are proven for stability by simulation and lab test. Further combinations should be checked for each individual application.

**Table 4. Matrix of Output Capacitor and Inductor Combinations**

L [ $\mu$ H] <sup>(1)</sup>	C <sub>OUT</sub> [ $\mu$ F] <sup>(1)</sup>				
	10	22	47	100	150
0.47					
1	+	+(2)(3)	+	+	
2.2	+	+	+	+	
4.7					

- (1) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance can vary by +20% and –50%. Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by +20% and –30%.
- (2) Plus mark indicates recommended filter combinations.
- (3) Filter combination in typical application.

#### 9.2.2.3 Inductor Selection

The main parameters for the inductor selection are the inductor value and then the saturation current of the inductor. To calculate the maximum inductor current under static load conditions, [Equation 3](#) is given.

$$I_{L,MAX} = I_{OUT,MAX} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}}$$

where

- $I_{OUT,MAX}$  = Maximum output current
- $\Delta I_L$  = Inductor current ripple
- $f_{SW}$  = Switching frequency
- $L$  = Inductor value

(3)

TI recommends to choose the saturation current for the inductor 20%–30% higher than the  $I_{L,MAX}$ , out of [Equation 3](#). A higher inductor value is also useful to lower ripple current, but increases the transient response time as well. The following inductors are recommended for use.

**Table 5. List of Recommended Inductors**

INDUCTANCE [ $\mu$ H]	CURRENT RATING [mA]	DIMENSIONS L x W x H [ $\text{mm}^3$ ]	DC RESISTANCE [ $\text{m}\Omega$ typ]	TYPE	MANUFACTURER
1.0	2500	3 x 3 x 1.2	35	XFL3012-102ME	Coilcraft
1.0	1650	3 x 3 x 1.2	40	LQH3NPN1R0NJ0	Murata
2.2	2500	4 x 3.7 x 1.65	49	LQH44PN2R2MP0	Murata
2.2	1600	3 x 3 x 1.2	81	XFL3012-222ME	Coilcraft

#### 9.2.2.4 Capacitor Selection

The input capacitor is the low impedance energy source for the converter which helps to provide stable operation. A low ESR multilayer ceramic capacitor is recommended for best filtering and should be placed between VIN and GND as close as possible to those pins. For most applications 10  $\mu$ F is sufficient, though a larger value reduces input current ripple.

The architecture of the TPS6208X allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its resistance up to high frequencies and to get narrow capacitance variation with temperature, it's recommended to use X7R or X5R dielectric. The TPS6208x is designed to operate with an output capacitance of 10  $\mu$ F to 100  $\mu$ F and beyond, as outlined in [Table 4](#). Load transient testing and measuring the bode plot are good ways to verify stability with larger capacitor values.

**Table 6. List of Recommended Capacitors**

CAPACITANCE [ $\mu$ F]	TYPE	DIMENSIONS L x W x H [ $\text{mm}^3$ ]	MANUFACTURER
10	GRM188R60J106M	0603: 1.6 x 0.8 x 0.8	Murata
22	GRM188R60G226M	0603: 1.6 x 0.8 x 0.8	Murata
22	GRM21BR60J226M	0805: 2.0 x 1.2 x 1.25	Murata

9.2.3 Application Curves

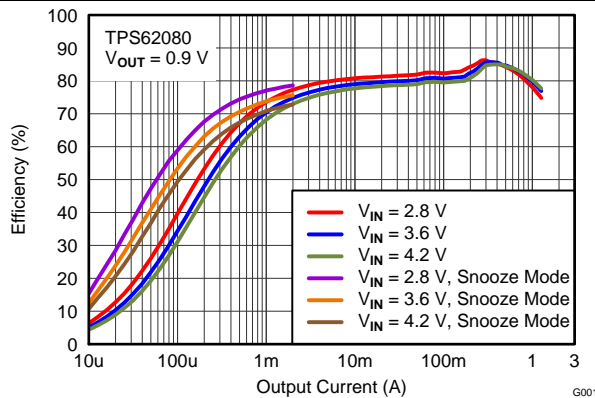


Figure 8. Efficiency vs Load Current

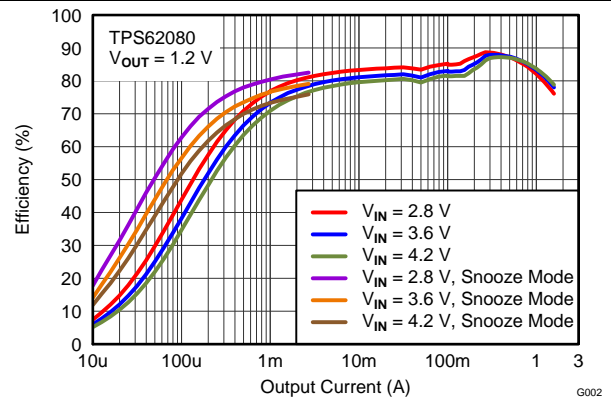


Figure 9. Efficiency vs Load Current

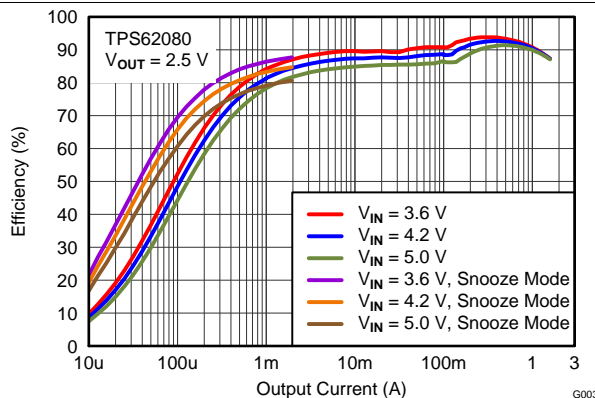


Figure 10. Efficiency vs Load Current

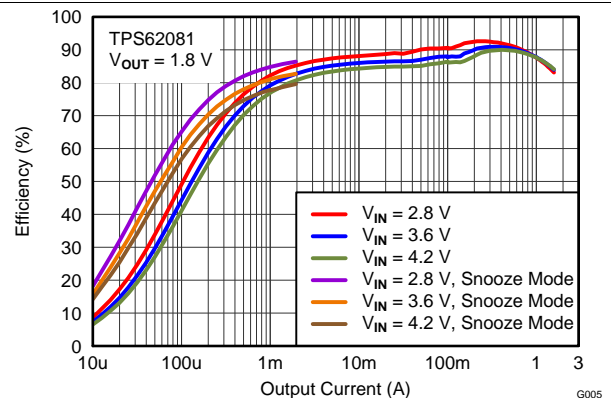


Figure 11. Efficiency vs Load Current

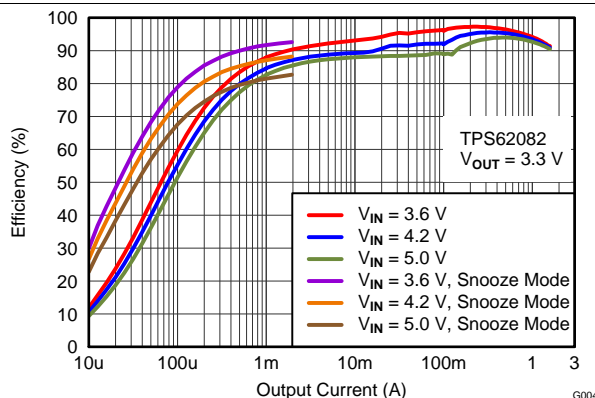


Figure 12. Efficiency vs Load Current

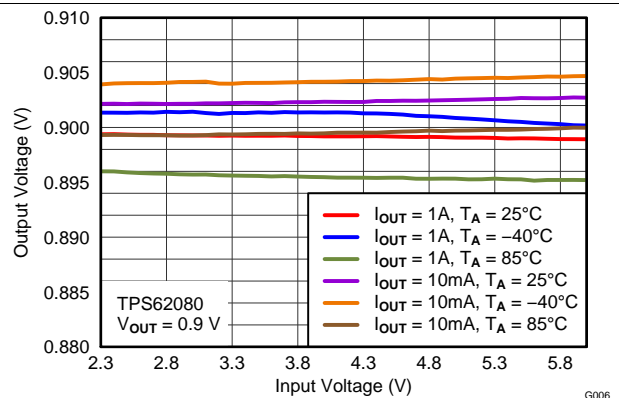


Figure 13. Output Voltage vs Input Voltage

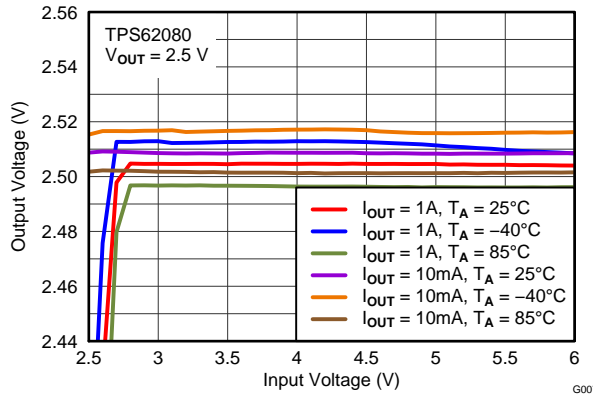


Figure 14. Output Voltage vs Input Voltage

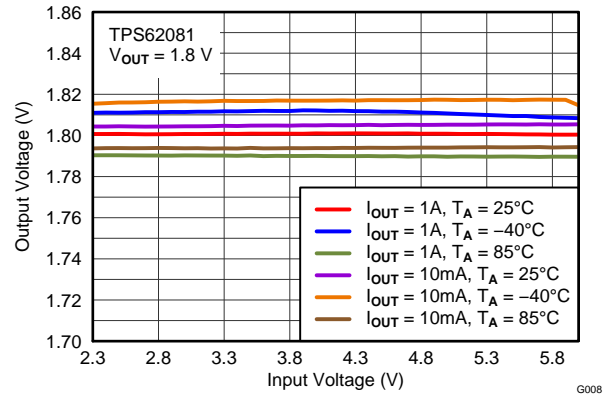


Figure 15. Output Voltage vs Input Voltage

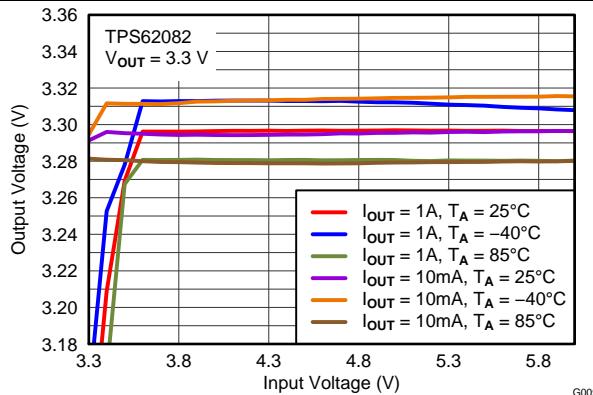


Figure 16. Output Voltage vs Input Voltage

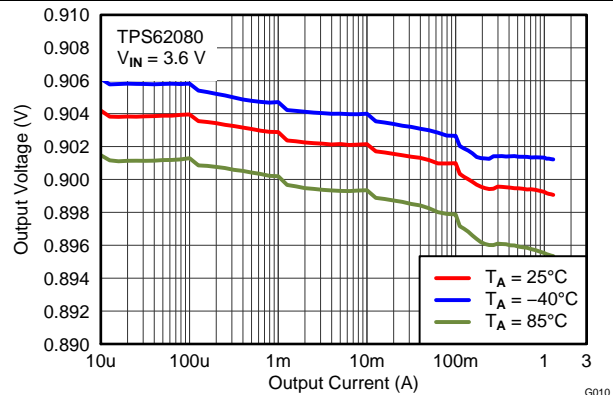


Figure 17. Output Voltage vs Load Current

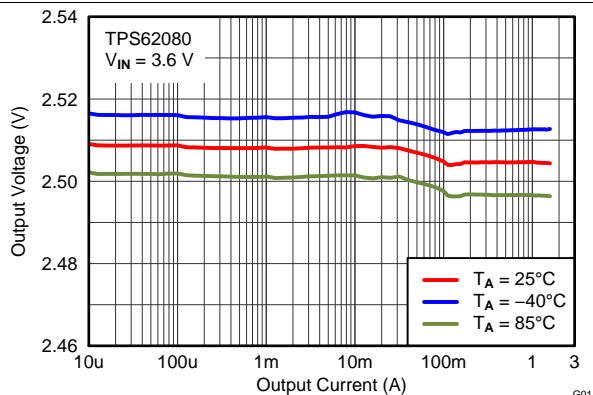


Figure 18. Output Voltage vs Load Current

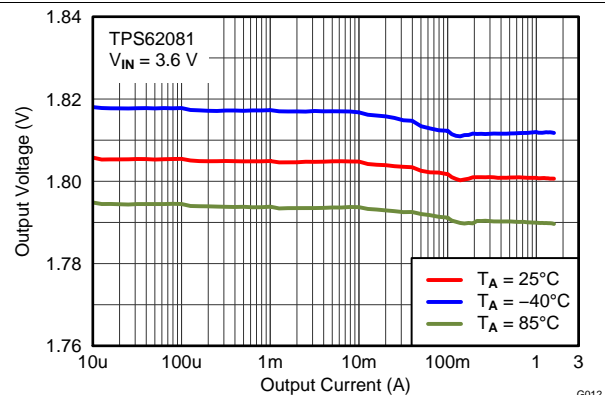


Figure 19. Output Voltage vs Load Current



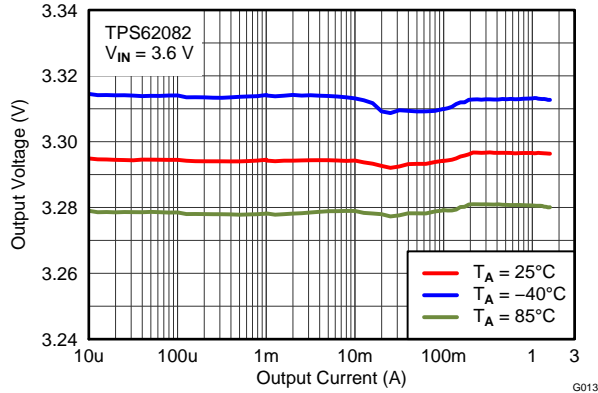


Figure 20. Output Voltage vs Load Current

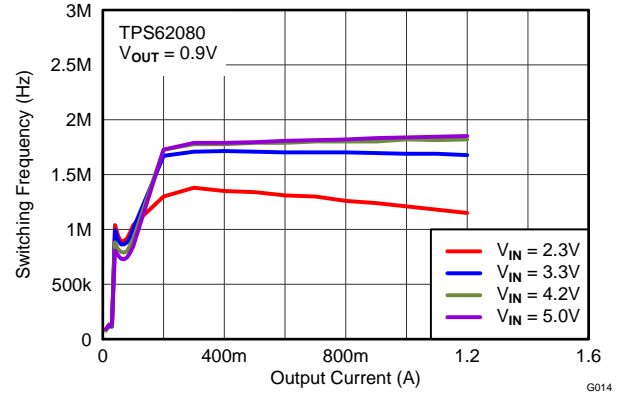


Figure 21. Switching Frequency vs Load Current

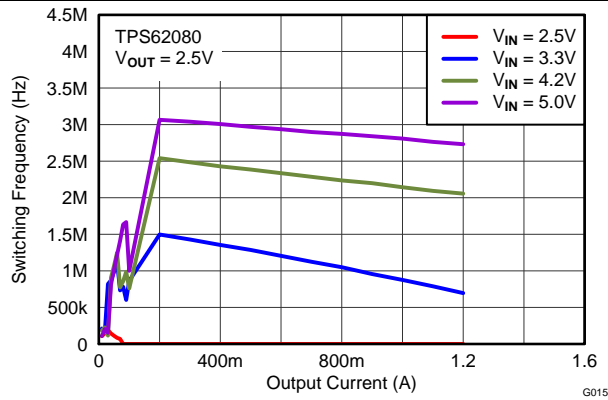


Figure 22. Switching Frequency vs Load Current

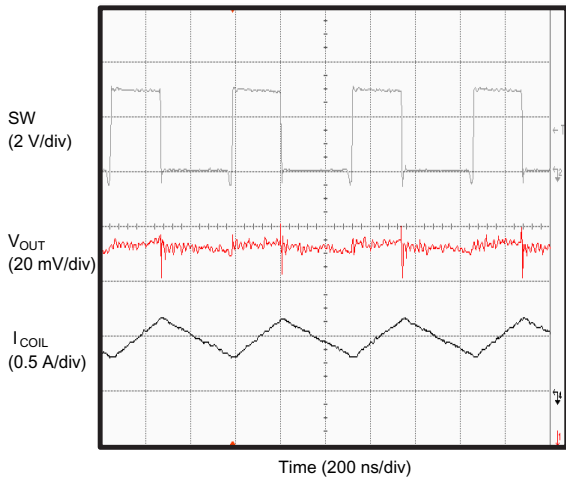


Figure 23. Typical Application (PWM Mode)

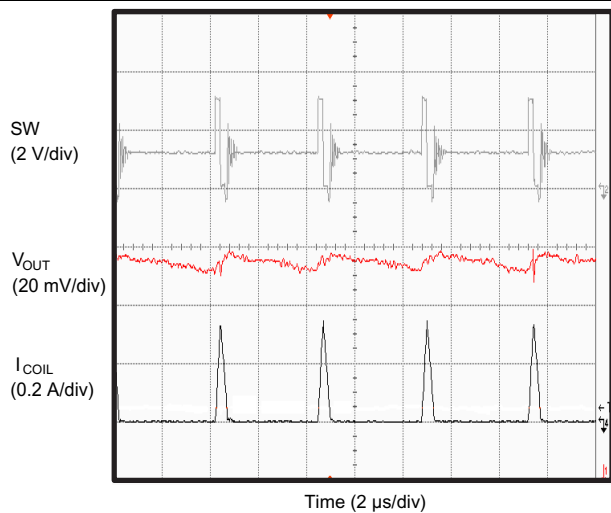


Figure 24. Typical Application (PFM Mode)

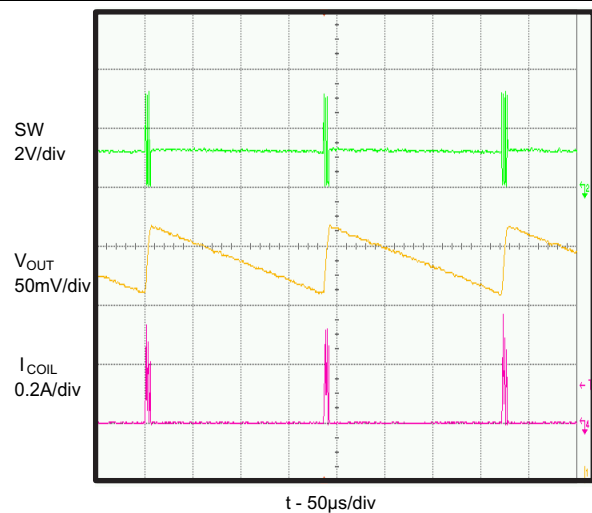
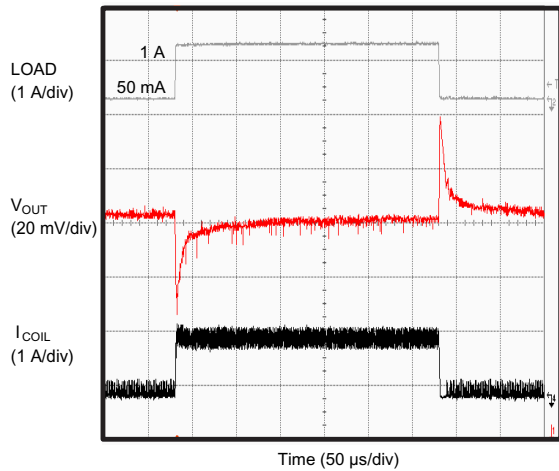
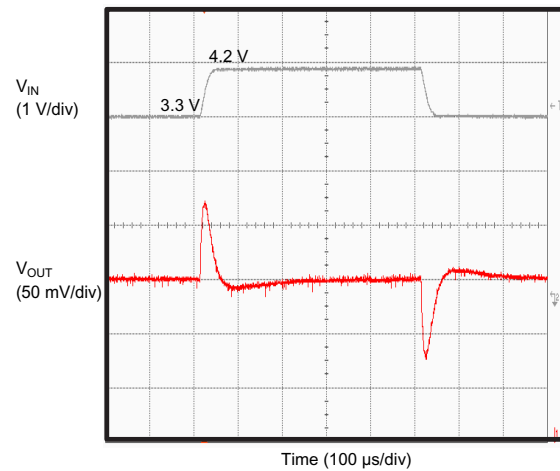


Figure 25. Typical Application (Snooze Mode)



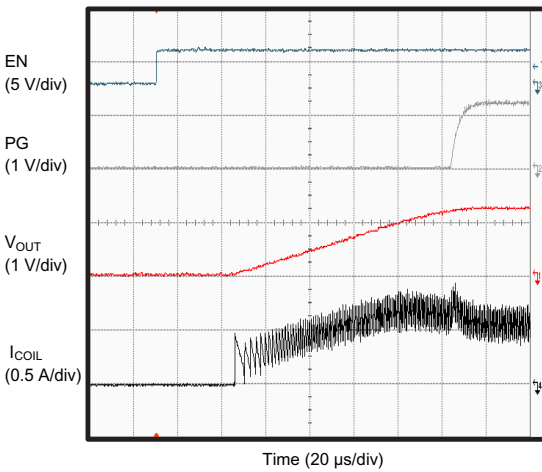
Time (50  $\mu$ s/div)  
 $V_{IN} = 3.3$  V,  $V_{OUT} = 1.2$  V, Load Current = 50 mA to 1 A

**Figure 26. Load Transient**



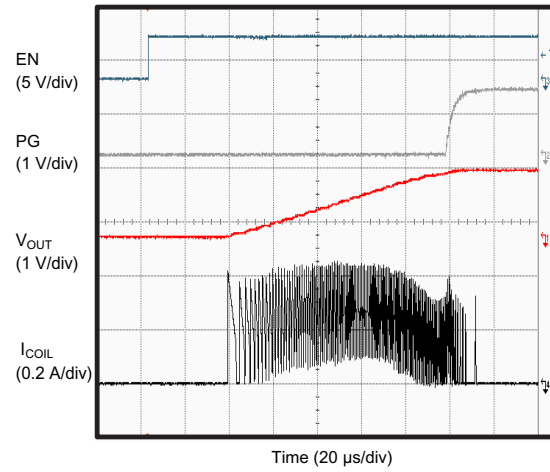
Time (100  $\mu$ s/div)  
 $V_{IN} = 3.3$  V to 4.2 V,  $V_{OUT} = 1.2$  V, Load = 2.2  $\Omega$

**Figure 27. Line Transient**



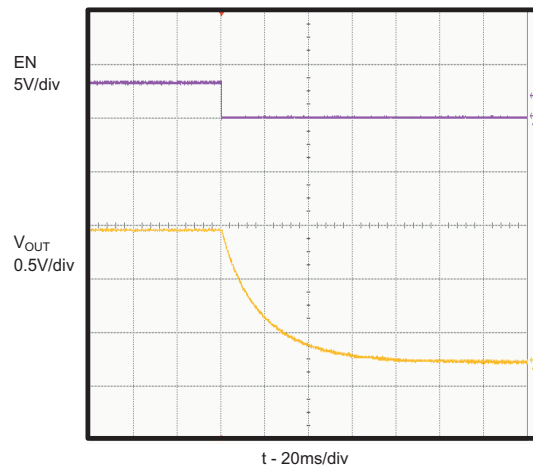
Time (20  $\mu$ s/div)  
 $V_{IN} = 3.3$  V,  $V_{OUT} = 1.2$  V, Load = 2.2  $\Omega$

**Figure 28. Start Up**



Time (20  $\mu$ s/div)  
 $V_{IN} = 3.3$  V,  $V_{OUT} = 1.2$  V, No Load

**Figure 29. Start Up (Without Load)**



t - 20ms/div  
 $V_{IN} = 3.3$  V,  $V_{OUT} = 1.2$  V, No Load

**Figure 30. Shutdown**

## 10 Power Supply Recommendations

The device is designed to operate from an input supply voltage range between 2.3 V and 6 V. Ensure that the input power supply has a sufficient current rating for the application.

## 11 Layout

### 11.1 Layout Guidelines

The PCB layout is an important step to maintain the high performance of the TPS6208x devices.

The input/output capacitors and the inductor should be placed as close as possible to the IC. This keeps the traces short. Routing these traces direct and wide results in low trace resistance and low parasitic inductance. A common power GND should be used. The low-side of the input and output capacitors must be connected properly to the power GND to avoid a GND potential shift.

The sense traces connected to the FB and VOS pins are signal traces. Special care should be taken to avoid noise being induced. By a direct routing, parasitic inductance can be kept small. GND layers might be used for shielding. Keep these traces away from SW nodes.

### 11.2 Layout Example

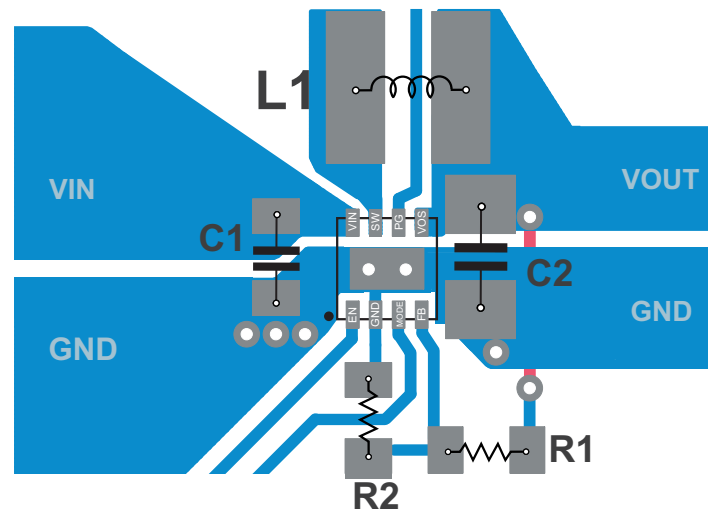


Figure 31. PCB Layout Suggestion

### 11.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB by soldering Exposed Thermal Pad
- Introducing airflow in the system

For more details on how to use the thermal parameters, see the application notes: *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* (SZZA017) and *Semiconductor and IC Package Thermal Metrics* (SPRA953).

## 12 デバイスおよびドキュメントのサポート

### 12.1 デバイス・サポート

#### 12.1.1 デベロッパー・ネットワークの製品に関する免責事項

デベロッパー・ネットワークの製品またはサービスに関するTIの出版物は、単独またはTIの製品、サービスと一緒に提供される場合に関係なく、デベロッパー・ネットワークの製品またはサービスの適合性に関する是認、デベロッパー・ネットワークの製品またはサービスの是認の表明を意味するものではありません。

### 12.2 ドキュメントのサポート

#### 12.2.1 関連資料

関連資料については、以下を参照してください。

『JEDEC PCB設計を使用するリニアおよびロジック・パッケージの熱特性』(SZZA017)

### 12.3 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 7. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
TPS62080	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>
TPS62080A	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>
TPS62081	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>
TPS62082	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>

### 12.4 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](http://ti.com)のデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

### 12.5 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™オンライン・コミュニティ** *TIのE2E ( Engineer-to-Engineer )* コミュニティ。エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイデアを検討して、問題解決に役立てることができます。

**設計サポート** *TIの設計サポート* 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

### 12.6 商標

DCS-Control, E2E are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.7 静電気放電に関する注意事項



これらのデバイスは、限定的なESD(静電破壊)保護機能を内蔵しています。保存時または取り扱い時は、MOSゲートに対する静電破壊を防止するために、リード線同士をショートさせておくか、デバイスを導電フォームに入れる必要があります。

## 12.8 用語集

### SLYZ022 — TI用語集.

この用語集には、用語や略語の一覧および定義が記載されています。

## 13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62080ADSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	Call TI   NIPDAUAG   NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SBN	<a href="#">Samples</a>
TPS62080ADSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	Call TI   NIPDAUAG   NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SBN	<a href="#">Samples</a>
TPS62080DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	Call TI   NIPDAUAG   NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QVR	<a href="#">Samples</a>
TPS62080DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	Call TI   NIPDAUAG   NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QVR	<a href="#">Samples</a>
TPS62081DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	Call TI   NIPDAUAG   NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QVS	<a href="#">Samples</a>
TPS62081DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	Call TI   NIPDAUAG   NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QVS	<a href="#">Samples</a>
TPS62082DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	Call TI   NIPDAUAG   NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QVT	<a href="#">Samples</a>
TPS62082DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	Call TI   NIPDAUAG   NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QVT	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62080ADSGR	WSON	DSG	8	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS62080ADSGT	WSON	DSG	8	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS62080DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62080DSGR	WSON	DSG	8	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS62080DSGT	WSON	DSG	8	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS62080DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62080DSGT	WSON	DSG	8	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS62081DSGR	WSON	DSG	8	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS62081DSGT	WSON	DSG	8	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS62082DSGR	WSON	DSG	8	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS62082DSGT	WSON	DSG	8	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62080ADSGR	WSON	DSG	8	3000	205.0	200.0	33.0
TPS62080ADSGT	WSON	DSG	8	250	205.0	200.0	33.0
TPS62080DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS62080DSGR	WSON	DSG	8	3000	205.0	200.0	33.0
TPS62080DSGT	WSON	DSG	8	250	205.0	200.0	33.0
TPS62080DSGT	WSON	DSG	8	250	210.0	185.0	35.0
TPS62080DSGT	WSON	DSG	8	250	213.0	191.0	35.0
TPS62081DSGR	WSON	DSG	8	3000	205.0	200.0	33.0
TPS62081DSGT	WSON	DSG	8	250	205.0	200.0	33.0
TPS62082DSGR	WSON	DSG	8	3000	205.0	200.0	33.0
TPS62082DSGT	WSON	DSG	8	250	205.0	200.0	33.0

## GENERIC PACKAGE VIEW

**DSG 8**

**WSON - 0.8 mm max height**

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



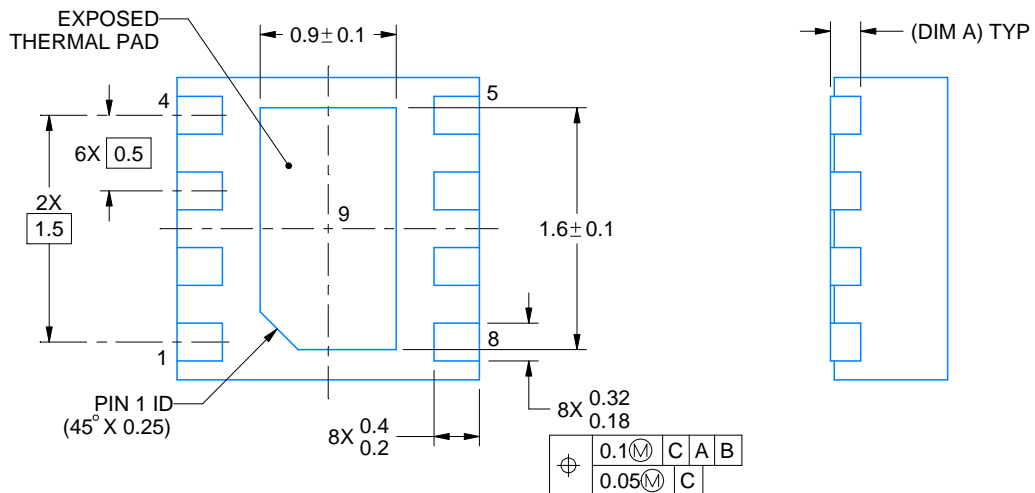
4224783/A



ALTERNATIVE TERMINAL SHAPE TYPICAL



SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2



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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:  
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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