

TPS737 逆電流保護機能付き、1A、低ドロップアウトレギュレータ

1 特長

- 1 μ F 以上のセラミック出力コンデンサにより安定
- 入力電圧範囲: 2.2V~5.5V
- 非常に低いドロップアウト電圧
 - レガシー シリコン: 1A において 130mV (標準値)
 - 新しいシリコン: 1A において 122mV (標準値)
- わずか 1 μ F の出力コンデンサでも優れた負荷過渡応答
- NMOS トポロジにより、低い逆リーク電流を実現
- 初期精度: 1%
- ライン、負荷、温度にわたる全体の精度
 - レガシー シリコン: 3%
 - 新しいシリコン: 1.5%
- シャットダウン モード時の I_Q : 20nA 未満 (標準値)
- サーマル シャットダウンおよび電流制限によるフォルト保護
- 複数の出力電圧バージョンが利用可能:
 - 調整可能な出力: 1.20V~5.5V
 - 工場でのパッケージ工程のプログラミングによりカスタム出力を提供可能

2 アプリケーション

- DSP、FPGA、ASIC、マイクロプロセッサのポイント オブロードレギュレーション
- スイッチング電源のポストレギュレーション
- 携帯型およびバッテリー駆動の機器

3 概要

TPS737 リニア低ドロップアウト (LDO) 電圧レギュレータは、電圧フォロワ構成で NMOS パストランジスタを使用します。このトポロジは出力コンデンサの値と ESR の影響を比較的受けにくいいため、広範な負荷構成に対応できます。わずか 1 μ F のセラミック出力コンデンサを使用した場合でも、負荷過渡応答が非常に優れています。また、NMOS トポロジにより、ドロップアウトも非常に小さくなります。

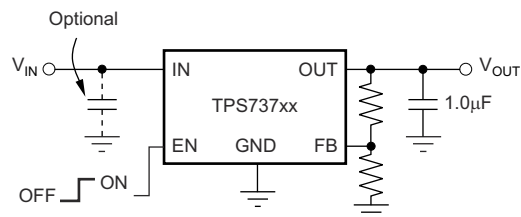
TPS737 は、非常に低いドロップアウト電圧と小さいグラウンドピン電流を実現すると同時に、先進の BiCMOS プロセスを使用することで高い精度を達成しています。最新の製造フローを使用するデバイスは、テキサス・インスツルメンツの最新プロセステクノロジーに基づく新しいシリコンにより設計を更新しています。ディセーブル時の消費電流は 20nA 未満であり、携帯型アプリケーション向けに設計されています。このデバイスは、サーマル シャットダウンとフォールドバック電流制限によって保護されています。

より高い出力電圧精度が必要なアプリケーションに対しては、全体精度 1% のテキサス・インスツルメンツ製 1A 低ドロップアウト電圧レギュレータ、TPS7A37 をご検討ください。

パッケージ情報

部品番号	パッケージ ⁽¹⁾	パッケージサイズ ⁽²⁾
TPS737	DRB (VSON, 8)	3mm × 3mm
	DCQ (SOT-223, 6)	6.5mm × 7.06 mm
	DRV (WSON, 6)	2mm × 2mm

- (1) 詳細については、「[セクション 10](#)」セクションを参照してください。
- (2) パッケージサイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



代表的なアプリケーション回路



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4 Pin Configuration and Functions

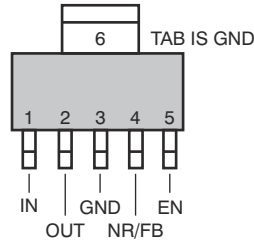


図 4-1. DCQ Package, 6-Pin SOT-223 (Top View)

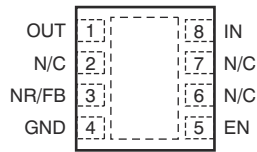


図 4-2. DRB Package, 8-Pin VSON (Top View)

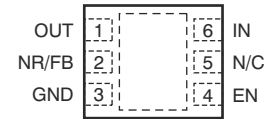


図 4-3. DRV Package^(A), 6-Pin WSON (Top View)

A. Power dissipation can limit operating range. Check the *Thermal Information* table.

表 4-1. Pin Functions

NAME	PIN			Type ⁽¹⁾	DESCRIPTION
	SOT-223	VSON	WSON		
IN	1	8	6	I	Unregulated input supply
GND	3, 6	4, Pad	3, Pad	—	Ground
EN	5	5	4	I	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. See the セクション 6.3.3 section for more details. EN must not be left floating and can be connected to IN if not used.
NR	4	3	2	—	Fixed voltage versions only—connecting an external capacitor to this pin bypasses noise generated by the internal band gap, reducing output noise to very low levels.
FB	4	3	2	I	Adjustable voltage version only—this is the input to the control loop error amplifier, and is used to set the output voltage of the device.
OUT	2	1	1	O	Regulator output. A 1.0- μ F or larger capacitor of any type is required for stability.
NC	—	2, 6, 7	5	—	Not connected

(1) I = Input; O = Output

5 Specifications

5.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Voltage	Input, V_{IN}	-0.3	6	V
	Enable, V_{EN}	-0.3	6	
	Output, V_{OUT}	-0.3	5.5	
	V_{NR} , V_{FB}	-0.3	6	
Current	Maximum output, I_{OUT}	Internally limited		
Output short-circuit duration		Indefinite		
Continuous total power dissipation	P_{DISS}	See <i>Thermal Information</i>		
Temperature	Operating junction, T_J	-55	150	°C
	Storage, T_{stg}	-65	150	

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	2.2		5.5	V
I_{OUT}	Output current	0		1	A
T_J	Operating junction temperature	-40		125	°C

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS737 New silicon		UNIT
		DRB (VSON)	DCQ (SOT-223)	
		8 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.7	76	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	68.9	46.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20.6	18.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.4	8.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	20.6	17.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.5	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

5.5 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS737 Legacy silicon ⁽²⁾			UNIT
		DRB (VSON)	DCQ (SOT-223)	DRV (WSON) ⁽³⁾	
		8 PINS	6 PINS	5 PINS	
R _{θJA}	Junction-to-ambient thermal resistance ⁽⁴⁾	49.5	53.1	67.2	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance ⁽⁵⁾	58.9	35.2	87.6	°C/W
R _{θJB}	Junction-to-board thermal resistance ⁽⁶⁾	25.1	7.8	36.8	°C/W
ψ _{JT}	Junction-to-top characterization parameter ⁽⁷⁾	1.7	2.9	1.8	°C/W
ψ _{JB}	Junction-to-board characterization parameter ⁽⁸⁾	25.2	7.7	37.2	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance ⁽⁹⁾	8.6	N/A	7.7	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.
- (2) Thermal data for the DRB, DCQ, and DRV packages are derived by thermal simulations based on JEDEC-standard methodology as specified in the JESD51 series. The following assumptions are used in the simulations:
 - (a) i. DRB: The exposed pad is connected to the PCB ground layer through a 2x2 thermal via array.
 - ii. DCQ: The exposed pad is connected to the PCB ground layer through a 3x2 thermal via array.
 - iii. DRV: The exposed pad is connected to the PCB ground layer through a 2x2 thermal via array. Due to size limitation of thermal pad, 0.8mm pitch array is used which is off the JEDEC standard.
 - (b) The top copper layer has a detailed copper trace pattern. The bottom copper layer is assumed to have a 20% thermal conductivity of copper, representing a 20% copper coverage.
 - (c) These data were generated with only a single device at the center of a JEDEC high-K (2s2p) board with 3inch × 3inch copper area. To understand the effects of the copper area on thermal performance, see the *Power Dissipation and Estimating Junction Temperature* sections of this data sheet.
- (3) Power dissipation can limit operating range.
- (4) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (5) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the top of the package. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (6) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (7) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain R_{θJA} using a procedure described in JESD51-2a (sections 6 and 7).
- (8) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain R_{θJA} using a procedure described in JESD51-2a (sections 6 and 7).
- (9) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

5.6 Electrical Characteristics

Over operating temperature range ($T_J = -40^\circ\text{C}$ to 125°C), $V_{IN} = V_{OUT(nom)} + 1V^{(1)}$, $I_{OUT} = 10\text{mA}$, $V_{EN} = 2.2\text{V}$, and $C_{OUT} = 2.2\mu\text{F}$ (unless otherwise noted). Typical values are at $T_J = 25^\circ\text{C}$

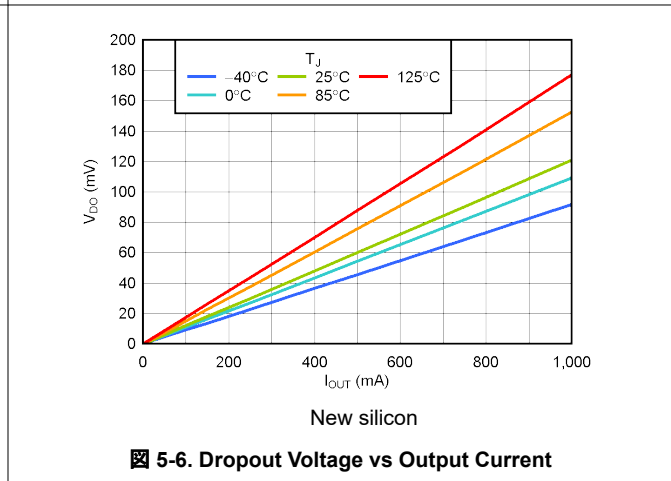
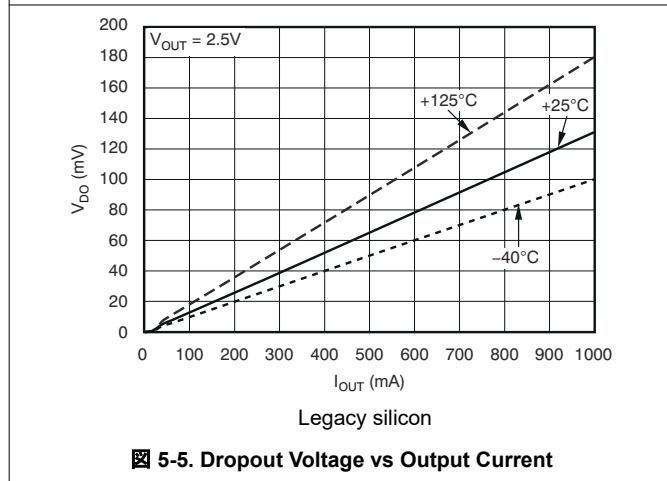
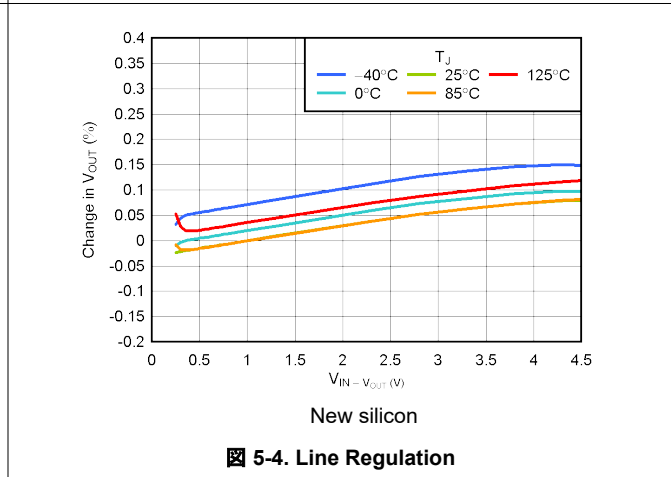
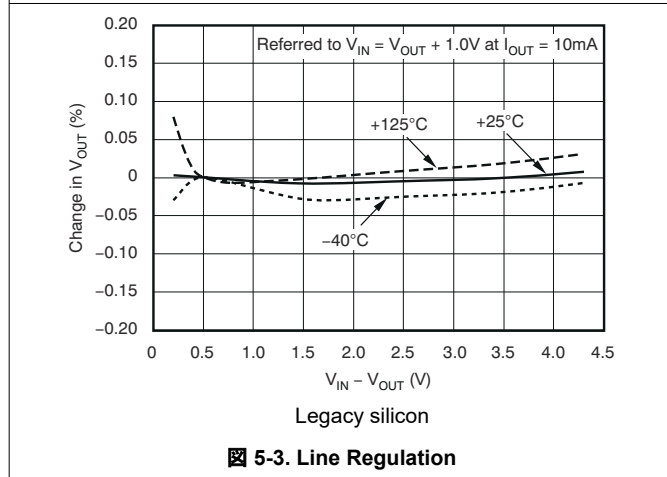
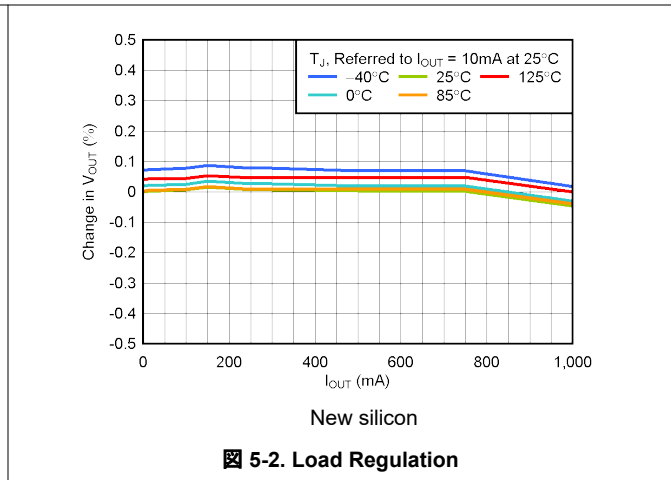
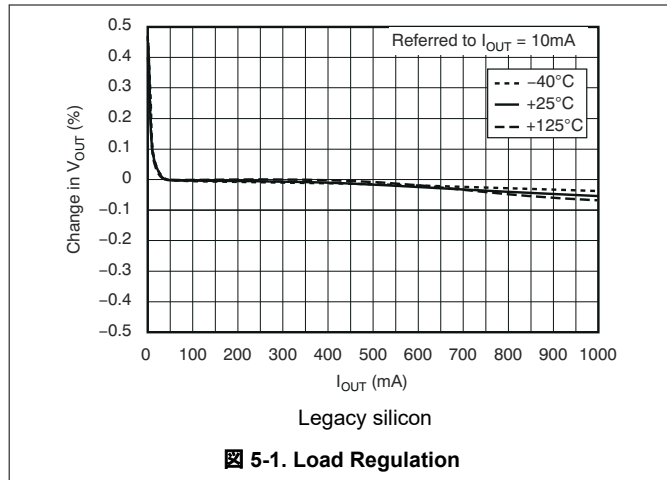
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
V_{IN}	Input voltage range ^{(1) (2)}			2.2		5.5	V	
V_{FB}	Internal reference (DCQ package)	$T_J = 25^\circ\text{C}$		1.198	1.204	1.21	V	
V_{FB}	Internal reference (DRB and DRV packages)	$T_J = 25^\circ\text{C}$		1.192	1.204	1.216	V	
V_{OUT}	Output voltage range (TPS73701) ⁽³⁾			V_{FB}		5.5 - V_{DO}	V	
	Accuracy ^{(1) (4)}	Nominal	$T_J = 25^\circ\text{C}$	-1		1	%	
			$5.36\text{V} < V_{IN} < 5.5\text{V}$, $V_{OUT} = 5.08\text{V}$, $10\text{mA} < I_{OUT} < 800\text{mA}$, $-40^\circ\text{C} < T_J < 85^\circ\text{C}$, TPS73701 (DCQ)		-2			2
		over V_{IN} , I_{OUT} , and T	$V_{OUT} + 0.5\text{V} \leq V_{IN} \leq 5.5\text{V}$; $10\text{mA} \leq I_{OUT} \leq 1\text{A}$, legacy silicon		-3	± 0.5		3
		$V_{OUT} + 0.5\text{V} \leq V_{IN} \leq 5.5\text{V}$; $10\text{mA} \leq I_{OUT} \leq 1\text{A}$, new silicon		-1.5	± 0.5	1.5		
$\Delta V_{OUT(\Delta V_{IN})}$	Line regulation ⁽¹⁾	$V_{OUT(nom)} + 0.5\text{V} \leq V_{IN} \leq 5.5\text{V}$			0.01		%/V	
$\Delta V_{OUT(\Delta I_{OUT})}$	Load regulation	$1\text{mA} \leq I_{OUT} \leq 1\text{A}$			0.002		%/mA	
$\Delta V_{OUT(\Delta I_{OUT})}$	Load regulation	$10\text{mA} \leq I_{OUT} \leq 1\text{A}$			0.0005		%/mA	
V_{DO}	Dropout voltage ⁽⁵⁾ ($V_{IN} = V_{OUT(nom)} - 0.1\text{V}$)	$I_{OUT} = 1\text{A}$, legacy silicon			130	500	mV	
V_{DO}	Dropout voltage ⁽⁵⁾ ($V_{IN} = V_{OUT(nom)} - 0.1\text{V}$)	$I_{OUT} = 1\text{A}$, new silicon			122	250	mV	
$Z_{O(DO)}$	Output impedance in dropout	$2.2\text{V} \leq V_{IN} \leq V_{OUT} + V_{DO}$			0.25		Ω	
I_{CL}	Output current limit	$V_{OUT} = 0.9 \times V_{OUT(nom)}$		1.05	1.6	2.2	A	
I_{SC}	Short-circuit current	$V_{OUT} = 0\text{V}$, legacy silicon			450		mA	
I_{SC}	Short-circuit current	$V_{OUT} = 0\text{V}$, new silicon			510		mA	
I_{REV}	Reverse leakage current ⁽⁶⁾ ($-I_{IN}$)	$V_{EN} \leq 0.5\text{V}$, $0\text{V} \leq V_{IN} \leq V_{OUT}$			0.1		μA	
I_{GND}	Ground pin current	$I_{OUT} = 10\text{mA}$ (I_Q)			400		μA	
I_{GND}	Ground pin current	$I_{OUT} = 1\text{A}$, legacy silicon			1300		μA	
I_{GND}	Ground pin current	$I_{OUT} = 1\text{A}$, new silicon			880		μA	
I_{SHDN}	Shutdown current (I_{GND})	$V_{EN} \leq 0.5\text{V}$, $V_{OUT} \leq V_{IN} \leq 5.5\text{V}$			20		nA	
I_{FB}	Feedback pin current (TPS73701)				0.1	0.6	μA	
PSRR	Power-supply rejection ratio (ripple rejection)	$f = 100\text{Hz}$, $I_{OUT} = 1\text{A}$			58		dB	
		$f = 10\text{kHz}$, $I_{OUT} = 1\text{A}$			37			
V_N	Output noise voltage, BW = 10Hz to 100kHz	$C_{OUT} = 10\mu\text{F}$			$27 \times V_{OUT}$		μV_{RMS}	
t_{STR}	Startup time	$V_{OUT} = 3\text{V}$, $R_L = 30\Omega$, $C_{OUT} = 1\mu\text{F}$, legacy silicon			600		μs	
t_{STR}	Startup time	$V_{OUT} = 3\text{V}$, $R_L = 30\Omega$, $C_{OUT} = 1\mu\text{F}$, new silicon			431		μs	
$V_{EN(high)}$	EN pin high (enabled)			1.7		V_{IN}	V	
$V_{EN(low)}$	EN pin low (shutdown)			0		0.5	V	
I_{EN}	Enable pin current (enabled)	$V_{EN} = 5.5\text{V}$			20		nA	
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing			160		$^\circ\text{C}$	
		Reset, temperature decreasing			140			
T_J	Operating junction temperature			-40		125	$^\circ\text{C}$	

(1) Minimum $V_{IN} = V_{OUT} + V_{DO}$ or 2.2V, whichever is greater.

- (2) For $V_{OUT(nom)} < 1.6V$, when $V_{IN} \leq 1.6V$, the output locks to V_{IN} and may result in a damaging over-voltage condition on the output. To avoid this situation, disable the device before powering down V_{IN} . (Legacy silicon only)
- (3) TPS73701 is tested at $V_{OUT} = 1.2V$.
- (4) Tolerance of external resistors not included in this specification.
- (5) V_{DO} is not measured for output versions with $V_{OUT(nom)} < 2.3V$, because minimum $V_{IN} = 2.2V$.
- (6) Fixed-voltage versions only; refer to *Application Information* section for more information.

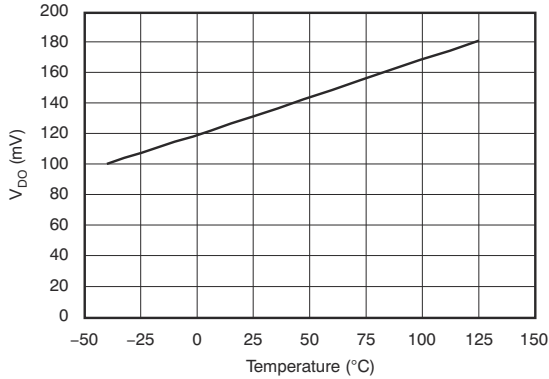
5.7 Typical Characteristics

for all voltage versions at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 1\text{ V}$, $I_{OUT} = 10\text{ mA}$, $V_{EN} = 2.2\text{ V}$, and $C_{OUT} = 2.2\text{ }\mu\text{F}$ (unless otherwise noted)



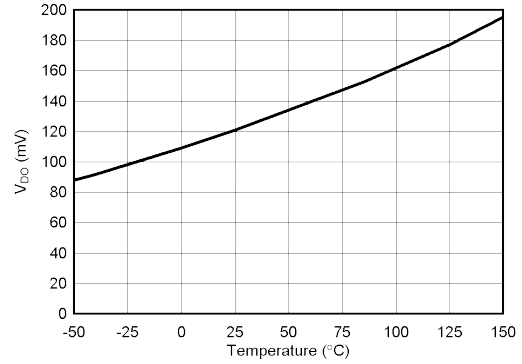
5.7 Typical Characteristics (continued)

for all voltage versions at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(\text{nom})} + 1\text{ V}$, $I_{OUT} = 10\text{ mA}$, $V_{EN} = 2.2\text{ V}$, and $C_{OUT} = 2.2\text{ }\mu\text{F}$ (unless otherwise noted)



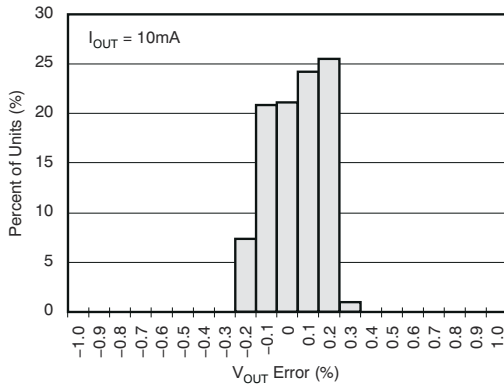
Legacy silicon

5-7. Dropout Voltage vs Temperature



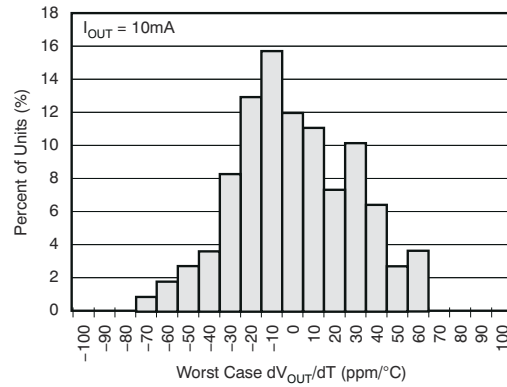
New silicon

5-8. Dropout Voltage vs Temperature



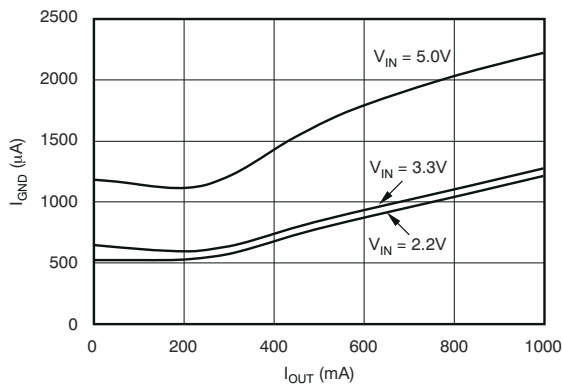
Legacy silicon

5-9. Output Voltage Histogram



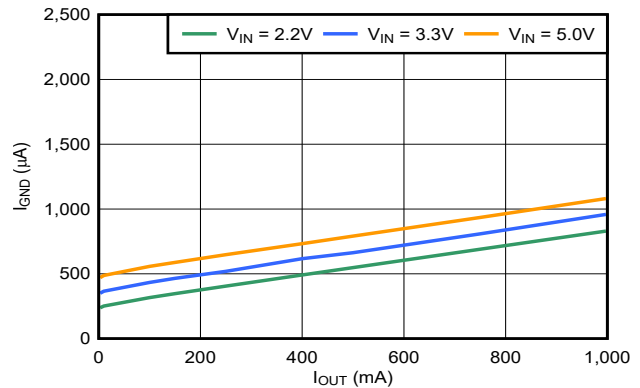
Legacy silicon

5-10. Output Voltage Drift Histogram



Legacy silicon

5-11. Ground Pin Current vs Output Current



New silicon

5-12. Ground Pin Current vs Output Current

5.7 Typical Characteristics (continued)

for all voltage versions at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 1\text{ V}$, $I_{OUT} = 10\text{ mA}$, $V_{EN} = 2.2\text{ V}$, and $C_{OUT} = 2.2\text{ }\mu\text{F}$ (unless otherwise noted)

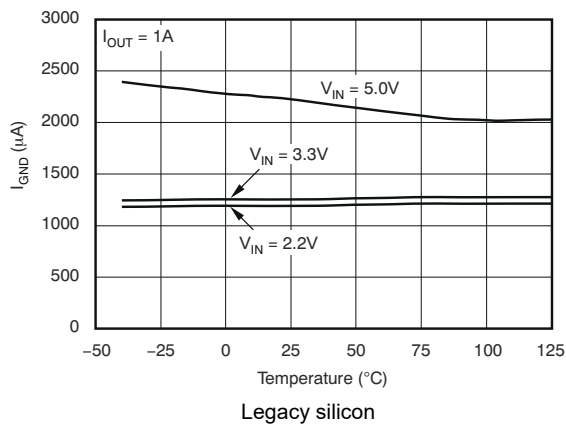


Figure 5-13. Ground Pin Current vs Temperature

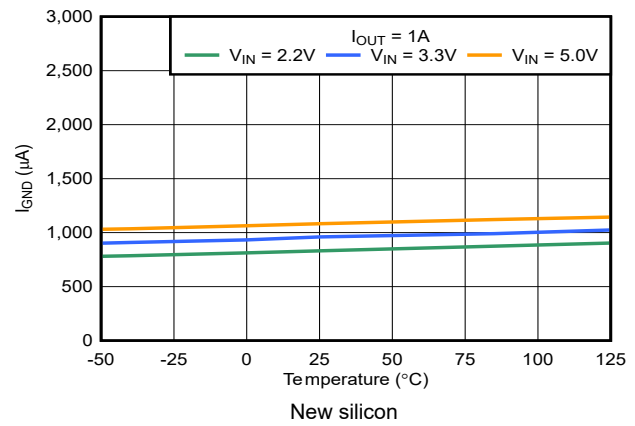


Figure 5-14. Ground Pin Current vs Temperature

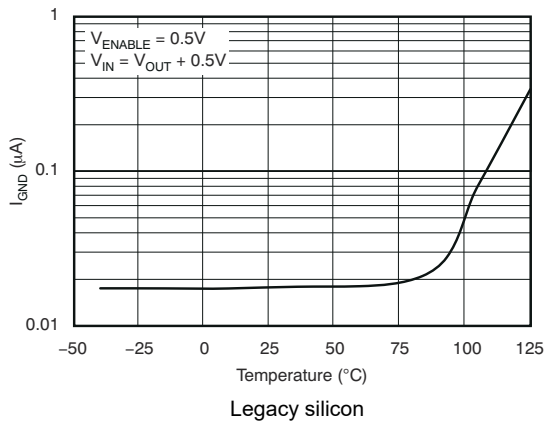


Figure 5-15. Ground Pin Current in Shutdown vs Temperature

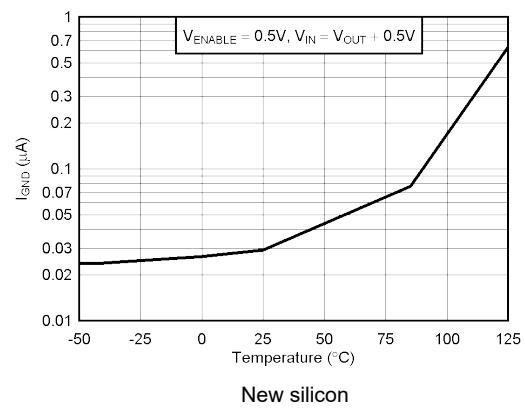


Figure 5-16. Ground Pin Current in Shutdown vs Temperature

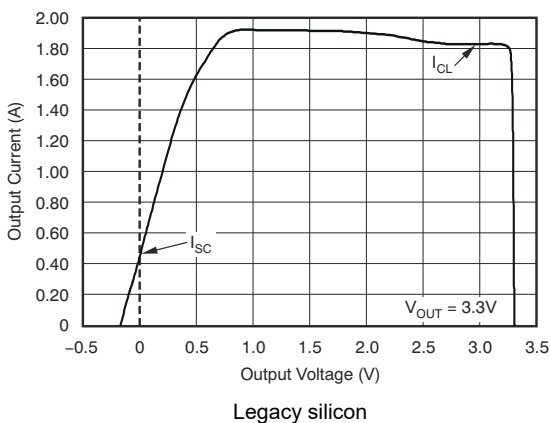


Figure 5-17. Current Limit vs V_{OUT} (Foldback)

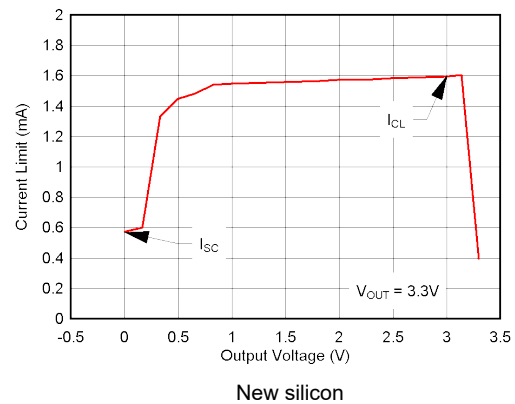
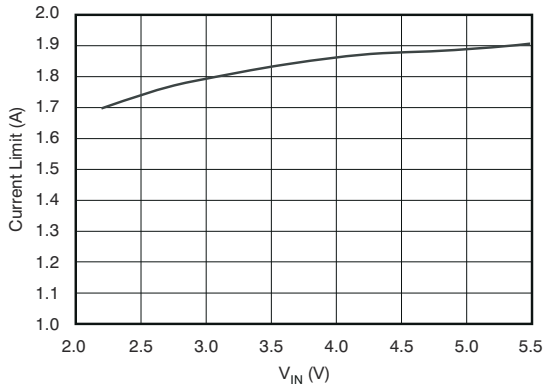


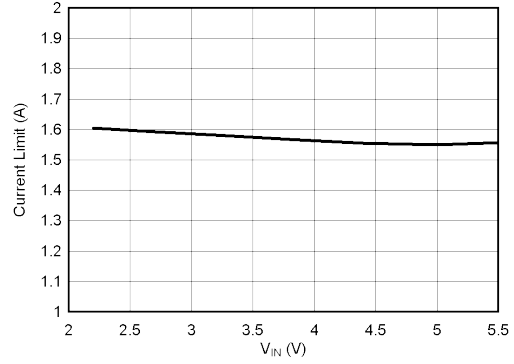
Figure 5-18. Current Limit vs V_{OUT} (Foldback)

5.7 Typical Characteristics (continued)

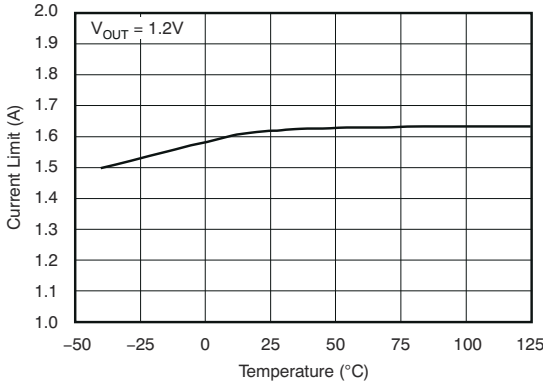
for all voltage versions at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 1\text{ V}$, $I_{OUT} = 10\text{ mA}$, $V_{EN} = 2.2\text{ V}$, and $C_{OUT} = 2.2\text{ }\mu\text{F}$ (unless otherwise noted)



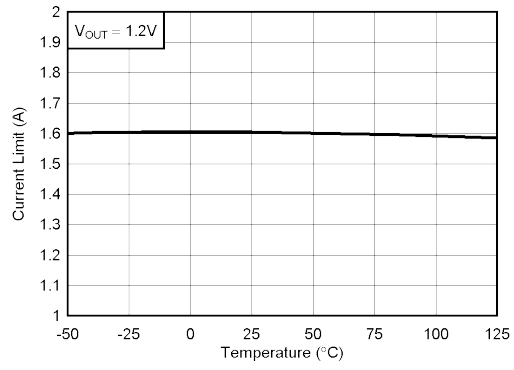
5-19. Current Limit vs V_{IN}



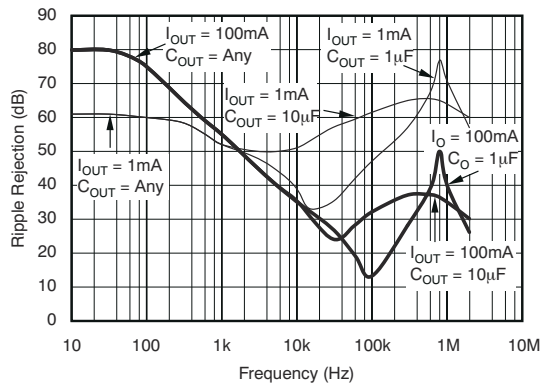
5-20. Current Limit vs V_{IN}



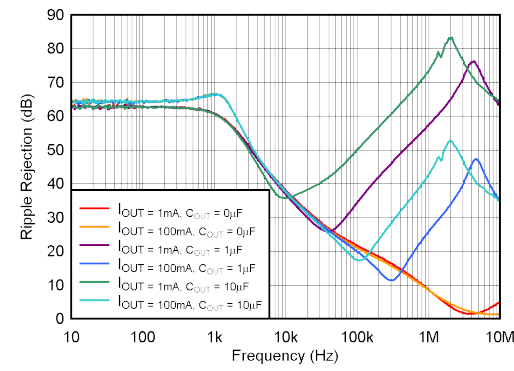
5-21. Current Limit vs Temperature



5-22. Current Limit vs Temperature



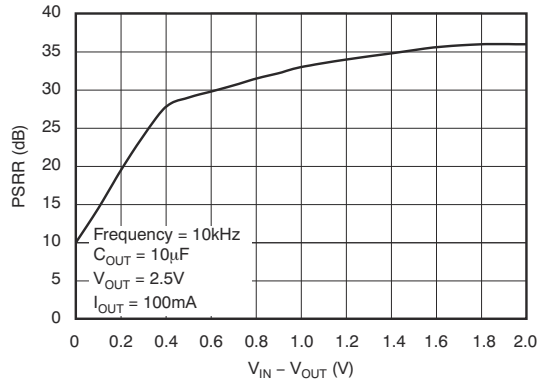
5-23. PSRR (Ripple Rejection) vs Frequency



5-24. PSRR (Ripple Rejection) vs Frequency

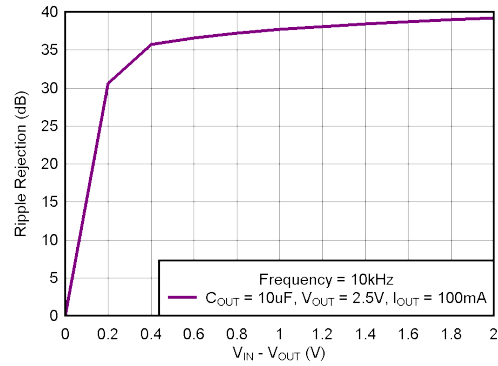
5.7 Typical Characteristics (continued)

for all voltage versions at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 1\text{ V}$, $I_{OUT} = 10\text{ mA}$, $V_{EN} = 2.2\text{ V}$, and $C_{OUT} = 2.2\text{ }\mu\text{F}$ (unless otherwise noted)



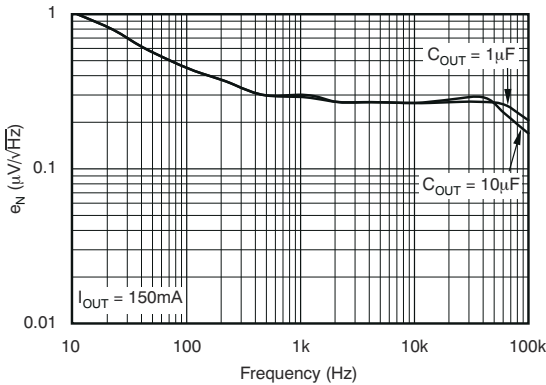
Legacy silicon

5-25. PSRR (Ripple Rejection) vs ($V_{IN} - V_{OUT}$)



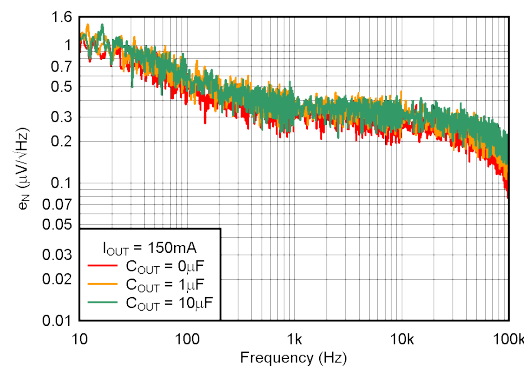
New silicon

5-26. PSRR (Ripple Rejection) vs ($V_{IN} - V_{OUT}$)



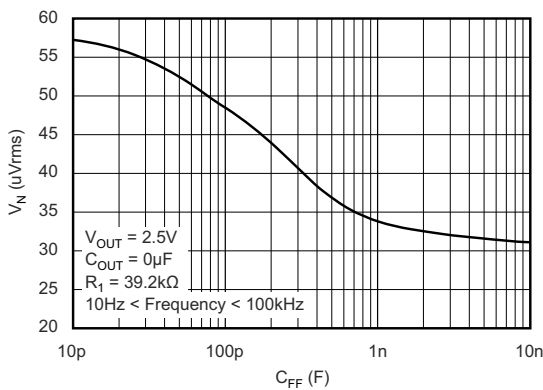
Legacy silicon

5-27. Noise Spectral Density



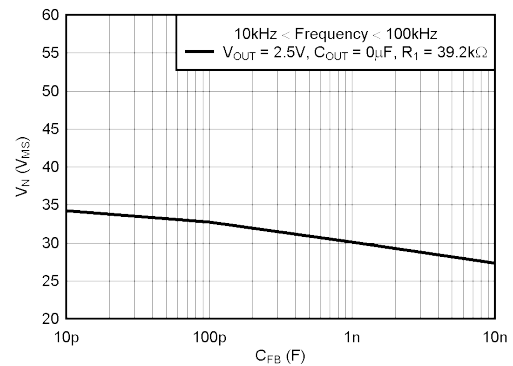
New silicon

5-28. Noise Spectral Density



Legacy silicon

5-29. TPS73701 RMS Noise Voltage vs C_{FB}

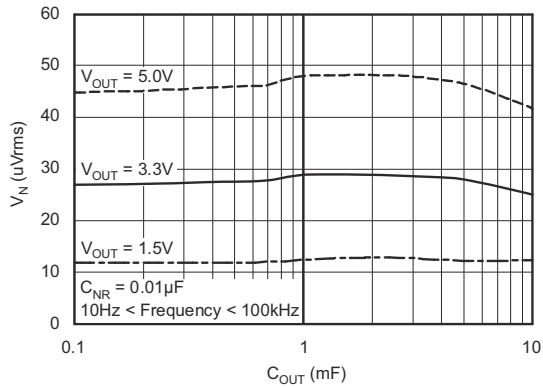


New silicon

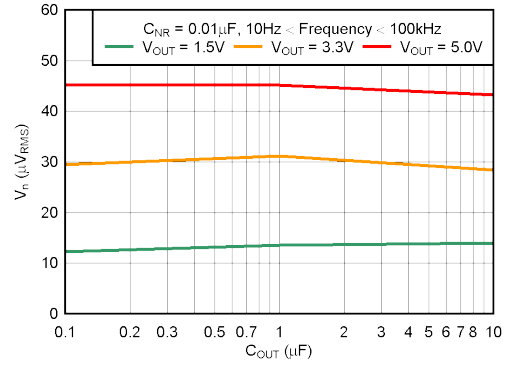
5-30. TPS73701 RMS Noise Voltage vs C_{FB}

5.7 Typical Characteristics (continued)

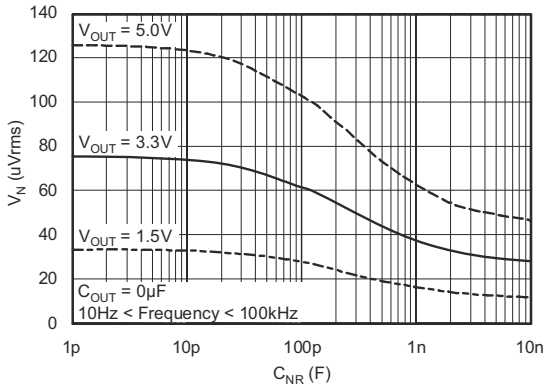
for all voltage versions at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 1\text{ V}$, $I_{OUT} = 10\text{ mA}$, $V_{EN} = 2.2\text{ V}$, and $C_{OUT} = 2.2\text{ }\mu\text{F}$ (unless otherwise noted)



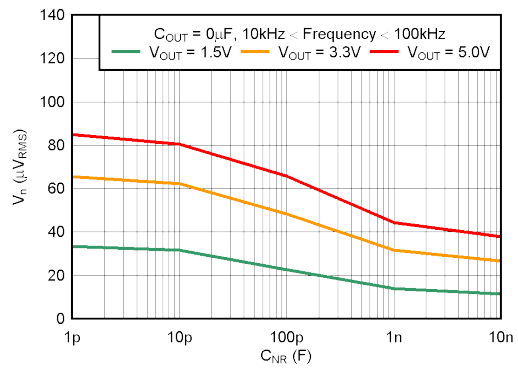
5-31. RMS Noise Voltage vs C_{OUT}



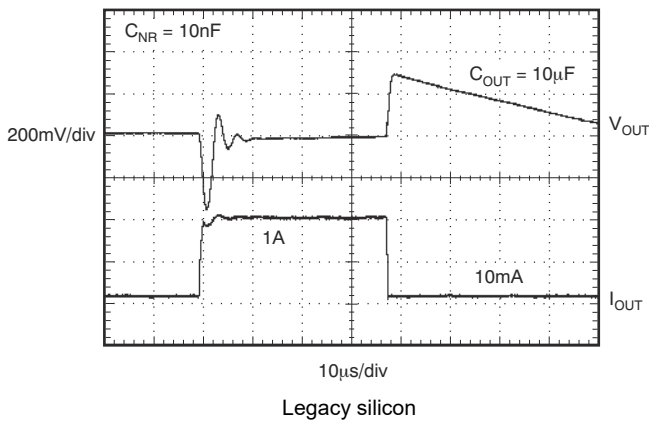
5-32. RMS Noise Voltage vs C_{OUT}



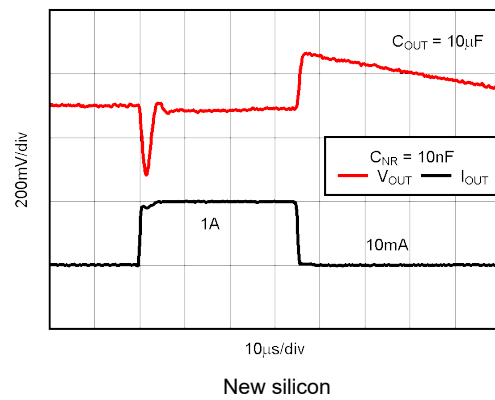
5-33. RMS Noise Voltage vs C_{NR}



5-34. RMS Noise Voltage vs C_{NR}



5-35. TPS73733 Load Transient Response



5-36. TPS73733 Load Transient Response

5.7 Typical Characteristics (continued)

for all voltage versions at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 1\text{ V}$, $I_{OUT} = 10\text{ mA}$, $V_{EN} = 2.2\text{ V}$, and $C_{OUT} = 2.2\text{ }\mu\text{F}$ (unless otherwise noted)

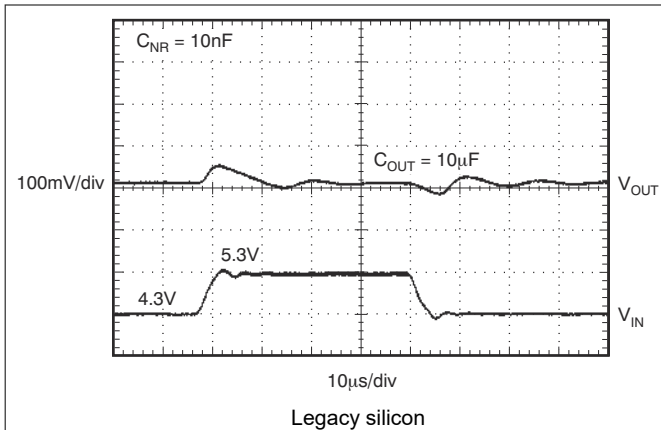


Figure 5-37. TPS73733 Line Transient Response

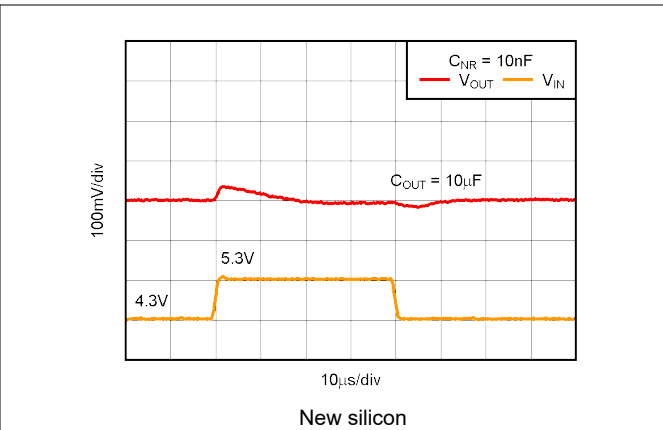


Figure 5-38. TPS73733 Line Transient Response

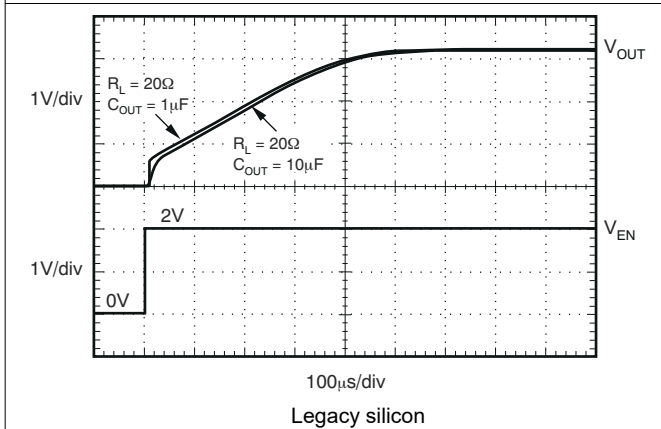


Figure 5-39. TPS73701 Turn-On Response

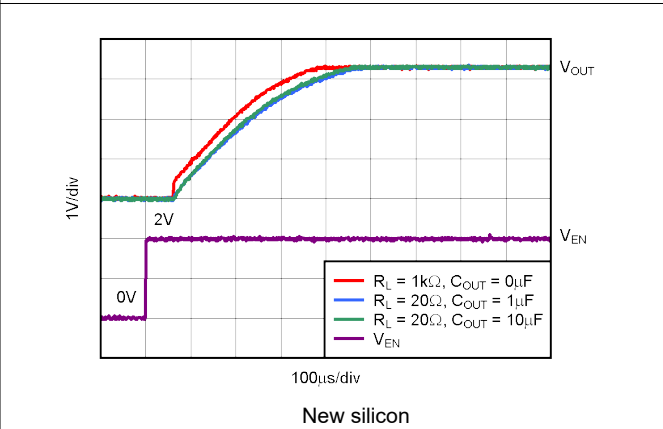


Figure 5-40. TPS73701 Turn-On Response

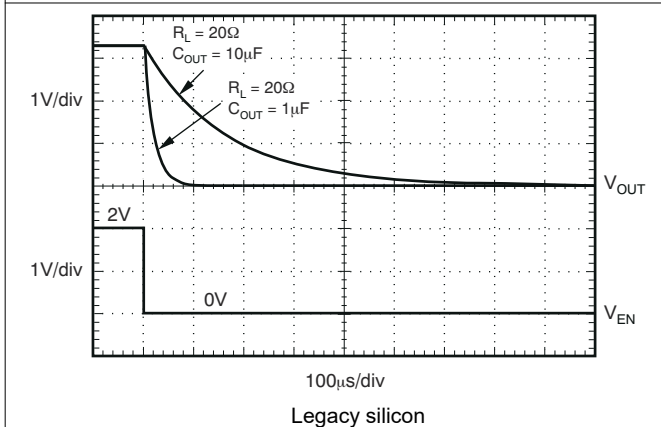


Figure 5-41. TPS73701 Turn-Off Response

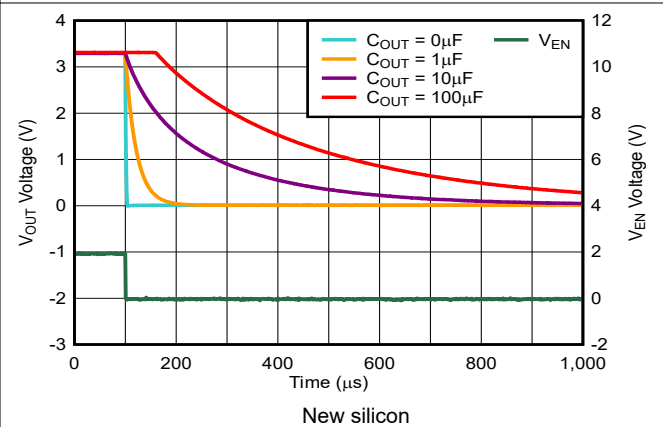


Figure 5-42. TPS73701 Turn-Off Response

5.7 Typical Characteristics (continued)

for all voltage versions at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 1\text{ V}$, $I_{OUT} = 10\text{ mA}$, $V_{EN} = 2.2\text{ V}$, and $C_{OUT} = 2.2\text{ }\mu\text{F}$ (unless otherwise noted)

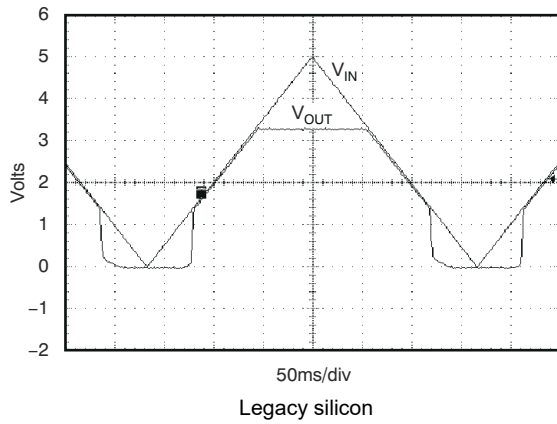


图 5-43. TPS73701, $V_{OUT} = 3.3\text{-V}$ Power-Up and Power-Down

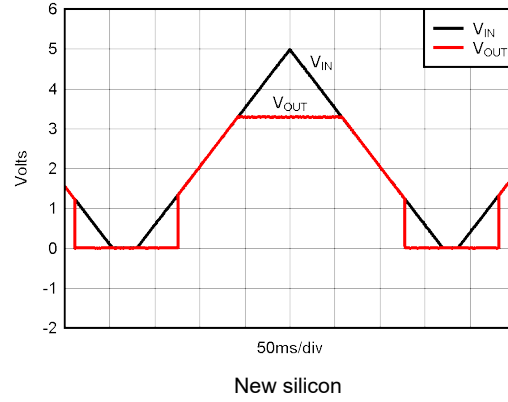


图 5-44. TPS73701, $V_{OUT} = 3.3\text{-V}$ Power-Up and Power-Down

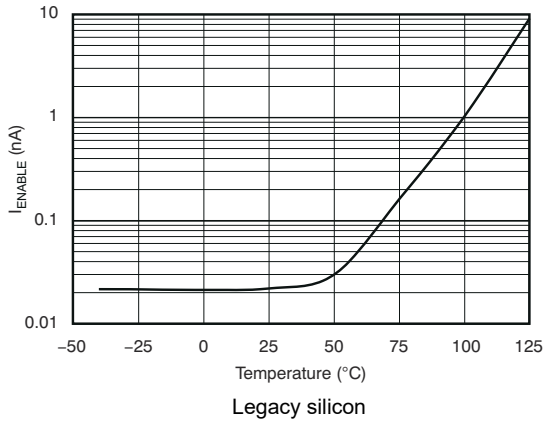


图 5-45. I_{EN} vs Temperature

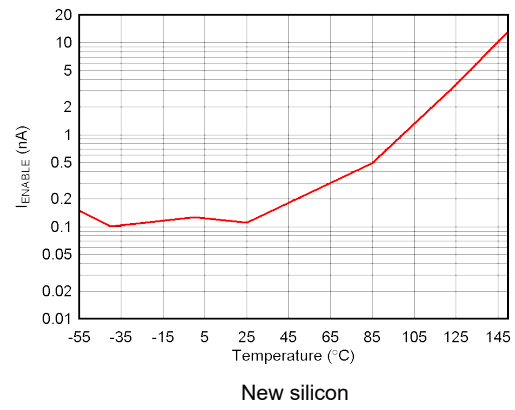


图 5-46. I_{EN} vs Temperature

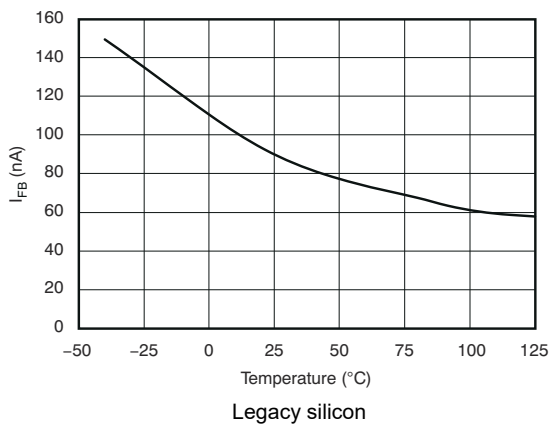


图 5-47. TPS73701 I_{FB} vs Temperature

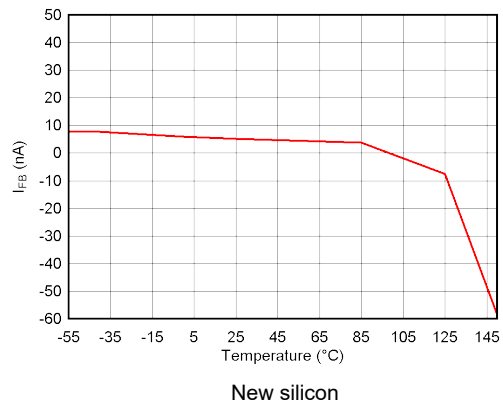
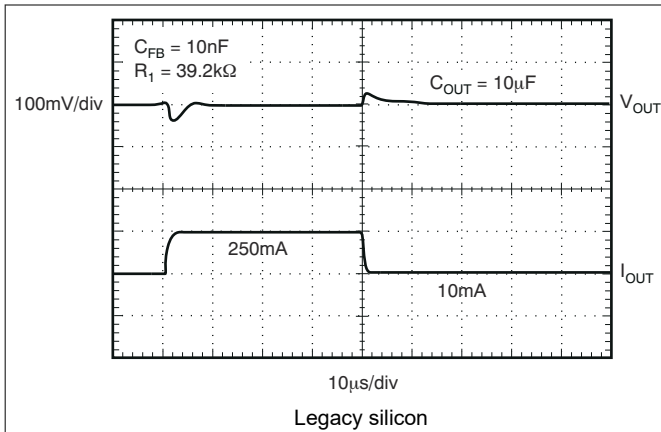


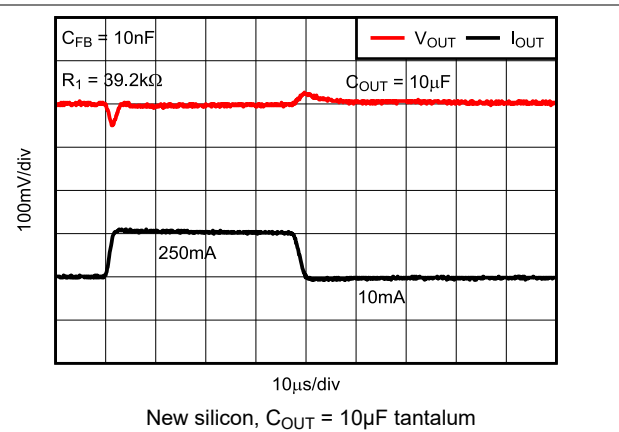
图 5-48. TPS73701 I_{FB} vs Temperature

5.7 Typical Characteristics (continued)

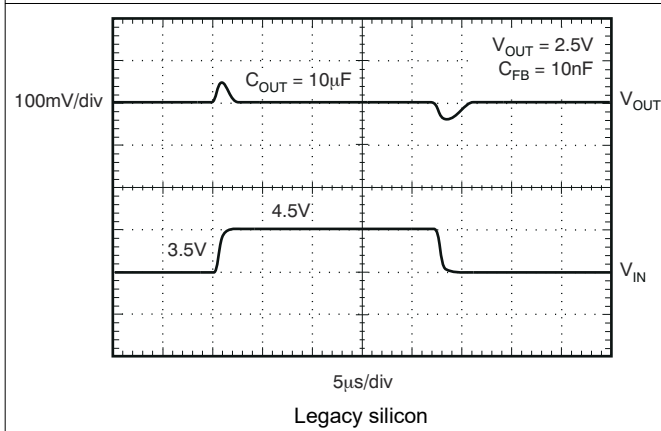
for all voltage versions at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(\text{nom})} + 1\text{ V}$, $I_{OUT} = 10\text{ mA}$, $V_{EN} = 2.2\text{ V}$, and $C_{OUT} = 2.2\text{ }\mu\text{F}$ (unless otherwise noted)



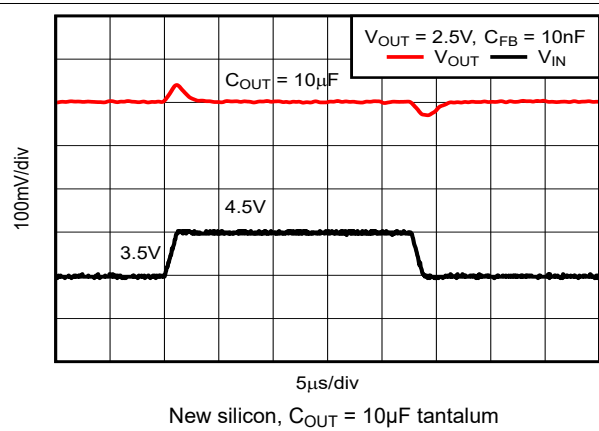
5-49. TPS73701 Load Transient, Adjustable Version



5-50. TPS73701 Load Transient, Adjustable Version



5-51. TPS73701 Line Transient, Adjustable Version



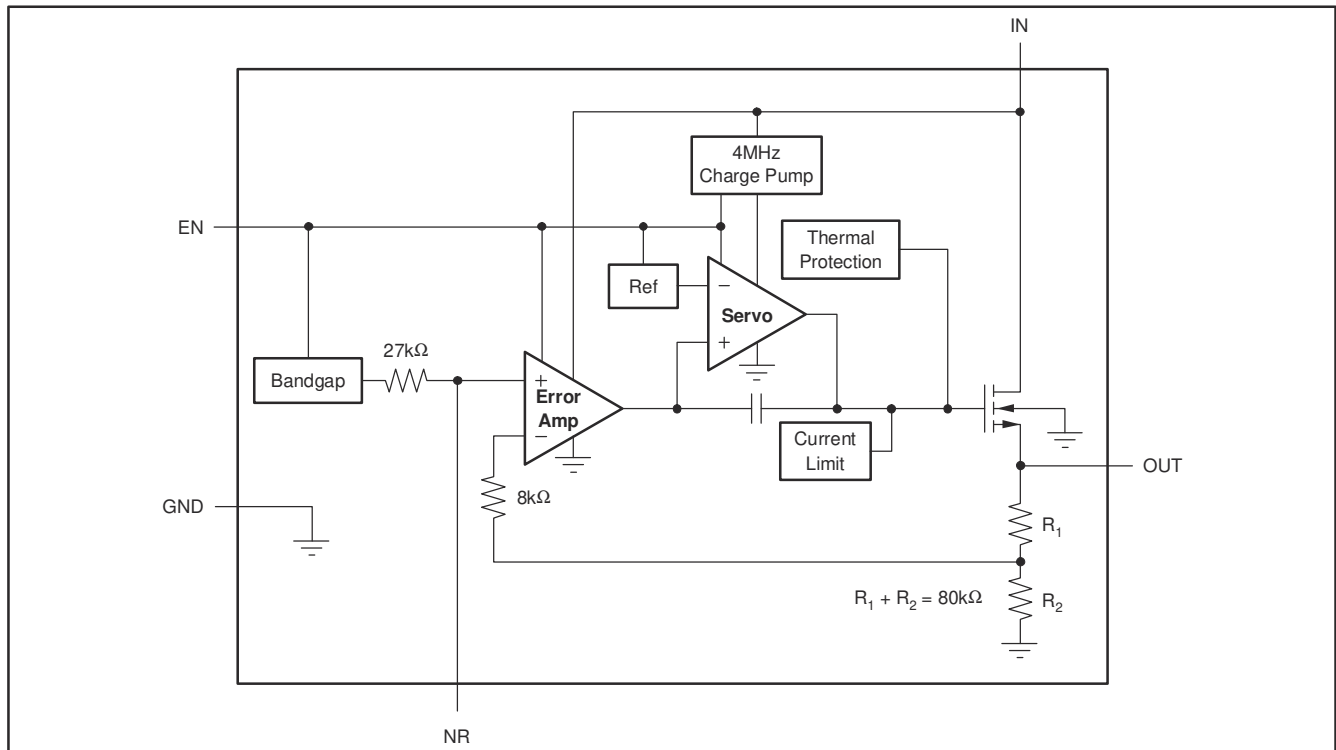
5-52. TPS73701 Line Transient, Adjustable Version

6 Detailed Description

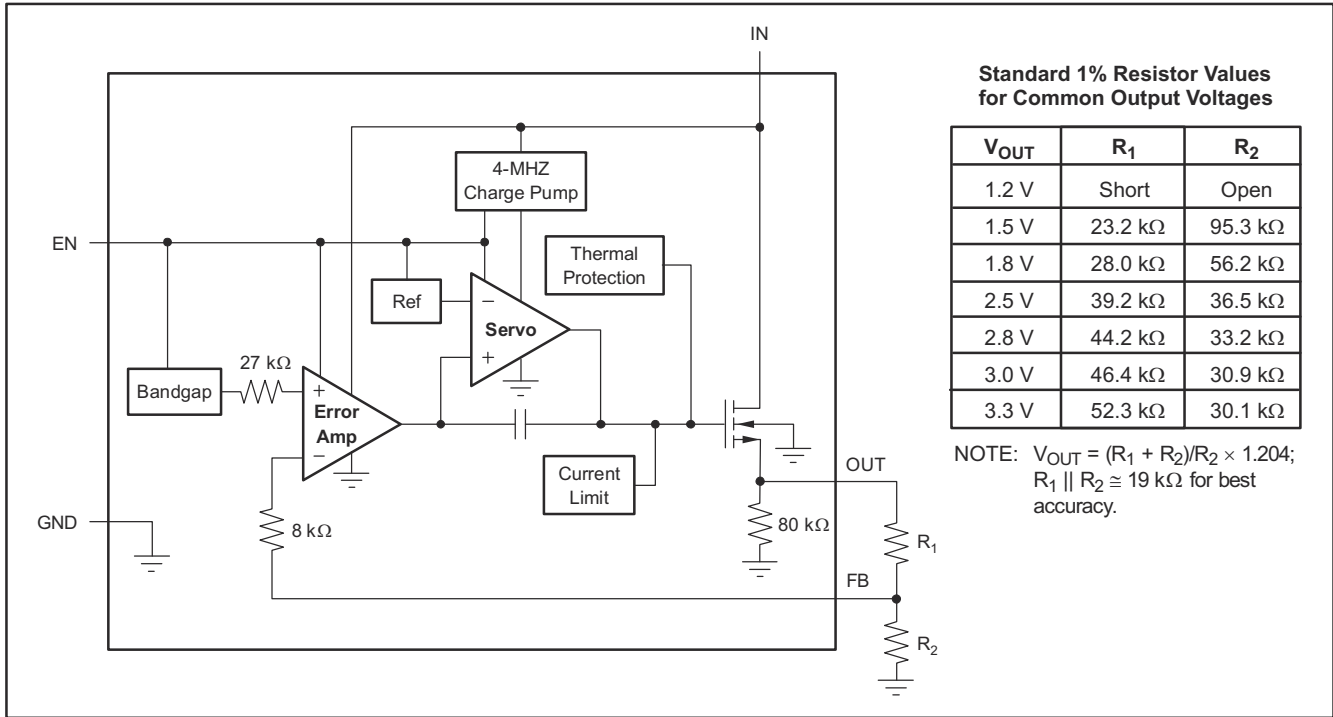
6.1 Overview

The TPS737 is a low-dropout (LDO) regulator that uses an n-type field effect (NMOS) pass transistor to achieve ultra-low dropout performance, reverse current blockage, and freedom from output capacitor constraints. These features combined with an enable input make the TPS737 designed for portable applications. This regulator offers a wide selection of fixed-output voltage versions and an adjustable-output version. All versions have thermal and overcurrent protection, including foldback current limit.

6.2 Functional Block Diagrams



☒ 6-1. Fixed-Voltage Version



6-2. Adjustable-Voltage Version

6.3 Feature Description

6.3.1 Output Noise

A precision band-gap reference is used to generate the internal reference voltage, V_{ref} . This reference is the dominant noise source within the TPS737xx and generates approximately $32 \mu V_{RMS}$ (10 Hz to 100 kHz) at the reference output (NR). The regulator control loop gains up the reference noise with the same gain as the reference voltage, so that the noise voltage of the regulator is approximately given by:

$$V_N = 32 \mu V_{RMS} \times \frac{(R_1 + R_2)}{R_2} = 32 \mu V_{RMS} \times \frac{V_{OUT}}{V_{REF}} \tag{1}$$

Because the value of V_R is 1.2 V, this relationship reduces to:

$$V_N (\mu V_{RMS}) = 27 \left(\frac{\mu V_{RMS}}{V} \right) \times V_{OUT} (V) \tag{2}$$

for the case of no C_{NR} .

An internal 27-kΩ resistor in series with the noise-reduction pin (NR) forms a low-pass filter for the voltage reference when an external noise-reduction capacitor, C_{NR} , is connected from NR to ground. For $C_{NR} = 10 \text{ nF}$, the total noise in the 10-Hz to 100-kHz bandwidth is reduced by a factor of approximately 3.2, giving the approximate relationship:

$$V_N (\mu V_{RMS}) = 8.5 \left(\frac{\mu V_{RMS}}{V} \right) \times V_{OUT} (V) \tag{3}$$

for $C_{NR} = 10 \text{ nF}$.

This noise reduction effect is shown as *RMS Noise Voltage vs C_{NR}* in the *Typical Characteristics* section.

The TPS73701 adjustable version does not have the NR pin available. However, connecting a feedback capacitor, C_{FB} , from the output to the feedback pin (FB) reduces output noise and improves load transient performance. Limit this capacitor to 0.1 μ F.

The TPS737 uses an internal charge pump to develop an internal supply voltage sufficient to drive the gate of the NMOS pass transistor above V_{OUT} . The charge pump generates approximately 250 μ V of switching noise at approximately 4 MHz; however, charge-pump noise contribution is negligible at the output of the regulator for most values of I_{OUT} and C_{OUT} .

6.3.2 Internal Current Limit

The TPS737 internal current limit helps protect the regulator during fault conditions. Foldback current limit helps protect the regulator from damage during output short-circuit conditions by reducing current limit when V_{OUT} drops below 0.5 V. See [Figure 5-17](#) in the *Typical Characteristics* section.

From [Figure 5-17](#), approximately -0.2 V of V_{OUT} results in a current-limit of 0 mA. Therefore, if OUT is forced below -0.2 V before EN goes high, the device can possibly not start up. In applications that work with both a positive and negative voltage supply, the TPS737 must be enabled first.

6.3.3 Enable Pin and Shutdown

The enable pin (EN) is active high and compatible with standard TTL-CMOS levels. V_{EN} below 0.5 V (maximum) turns the regulator off and drops the GND pin current to approximately 10 nA. When EN is used to shutdown the regulator, all charge is removed from the pass transistor gate. A V_{IN} above 1.7 V (minimum) turns the regulator on and the output ramps back up to a regulated V_{OUT} (see [Figure 5-39](#)).

When shutdown capability is not required, EN can be connected to V_{IN} . However, the pass transistor can possibly not be discharged using this configuration, and the pass transistor can be left on (enhanced) for a significant time after V_{IN} is removed. This scenario can result in reverse current flow (if the IN pin is low impedance) and faster ramp times upon power up. In addition, for V_{IN} ramp times slower than a few milliseconds, the output can overshoot upon power up.

Current limit foldback can prevent device start-up under some conditions. See the *Internal Current Limit* section for more information.

6.3.4 Reverse Current

The NMOS pass transistor of the TPS737 provides inherent protection against current flow from the output of the regulator to the input when the gate of the pass transistor is pulled low. To make sure that all charge is removed from the gate of the pass transistor, the EN pin must be driven low before the input voltage is removed. If the EN pin is not driven low, the pass transistor can be left on because of stored charge on the gate.

After the EN pin is driven low, no bias voltage is needed on any pin for reverse current blocking. Reverse current is specified as the current flowing out of the IN pin because of voltage applied on the OUT pin. There is additional current flowing into the OUT pin as a result of the 80-k Ω internal resistor divider to ground (see [Figure 6-1](#) and [Figure 6-2](#)).

For the TPS73701, reverse current can flow when V_{FB} is more than 1.0 V above V_{IN} .

6.4 Device Functional Modes

Driving the EN pin over 1.7 V turns on the regulator. Driving the EN pin below 0.5 V causes the regulator to enter shutdown mode. In shutdown, the current consumption of the device is reduced to 20 nA, typically.

7 Application and Implementation

注

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7.1 Application Information

The TPS737 low-dropout (LDO) regulator uses an NMOS pass transistor to achieve ultra-low-dropout performance, reverse current blockage, and freedom from output capacitor constraints. These features, combined with low noise and an enable input, make the TPS737 designed for portable applications. This regulator offers a wide selection of fixed-output voltage versions and an adjustable-output version. All versions have thermal and overcurrent protection, including foldback current-limit.

7.2 Typical Application

図 7-1 shows the basic circuit connections for the fixed-voltage models. 図 7-2 gives the connections for the adjustable output version (TPS73701).

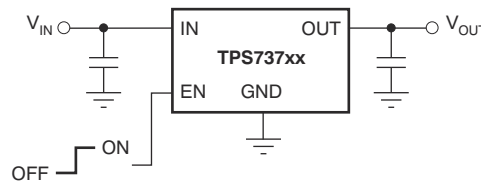


図 7-1. Typical Application Circuit for Fixed-Voltage Versions

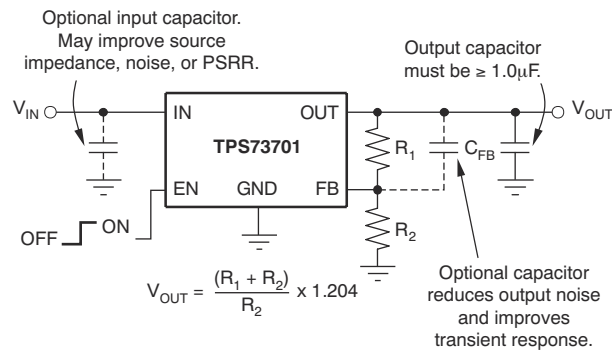


図 7-2. Typical Application Circuit for Adjustable-Voltage Version

7.2.1 Design Requirements

R_1 and R_2 can be calculated for any output voltage using the formula shown in 図 7-2. Sample resistor values for common output voltages are given in 図 6-2.

For best accuracy, make the parallel combination of R_1 and R_2 approximately equal to 19 k Ω . This 19 k Ω , in addition to the internal 8-k Ω resistor, presents the same impedance to the error amp as the 27-k Ω band-gap reference output. This impedance helps compensate for leakages into the error amplifier terminals.

7.2.2 Detailed Design Procedure

Provide an input supply with adequate headroom to account for dropout and output current to compensate for the GND pin current and to power the load. Further, select adequate input and output capacitors as discussed in the [Input and Output Capacitor Requirements](#) section.

7.2.2.1 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability if input impedance is very low, good analog design practice is to connect a 0.1- μF to 1- μF low equivalent series resistance (ESR) capacitor across the input supply near the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor can be necessary if large, fast rise-time load transients are anticipated or the device is located several inches from the power source.

The TPS737 requires a 1- μF output capacitor for stability. The device is designed to be stable for all available types and values of capacitors. In applications where multiple low-ESR capacitors are in parallel, ringing can occur when the product of C_{OUT} and total ESR drops below 50 nF $\cdot\Omega$. Total ESR includes all parasitic resistances, including capacitor ESR and board, socket, and solder joint resistance. In most applications, the sum of capacitor ESR and trace resistance meets this requirement.

7.2.2.2 Dropout Voltage

The TPS737 uses an NMOS pass transistor to achieve extremely low dropout. When $(V_{\text{IN}} - V_{\text{OUT}})$ is less than the dropout voltage (V_{DO}), the NMOS pass transistor is in the linear region of operation and the input-to-output resistance is the $R_{\text{DS(on)}}$ of the NMOS pass transistor.

For large step changes in load current, the TPS737 requires a larger voltage drop from V_{IN} to V_{OUT} to avoid degraded transient response. The boundary of this transient dropout region is approximately twice the DC dropout. Values of $(V_{\text{IN}} - V_{\text{OUT}})$ above this line provide normal transient response.

Operating in the transient dropout region can cause an increase in recovery time. The time required to recover from a load transient is a function of the magnitude of the change in load current rate, the rate of change in load current, and the available headroom ($V_{\text{IN-to-}V_{\text{OUT}}}$ voltage drop). Under worst-case conditions [full-scale instantaneous load change with $(V_{\text{IN}} - V_{\text{OUT}})$ close to DC dropout levels], the TPS737 can take a couple of hundred microseconds to return to the specified regulation accuracy.

7.2.2.3 Transient Response

The low open-loop output impedance provided by the NMOS pass transistor in a voltage-follower configuration allows operation without a 1- μF output capacitor. As with any regulator, the addition of additional capacitance from the OUT pin to ground reduces undershoot magnitude but increases undershoot duration. In the adjustable version, the addition of a capacitor, C_{FB} , from the OUT pin to the FB pin also improves the transient response.

The TPS737 does not have an active pulldown when the output is overvoltage. This architecture allows applications that connect higher voltage sources, such as alternate power supplies, to the output. This architecture also results in an output overshoot of several percent if the load current quickly drops to zero when a capacitor is connected to the output. The duration of overshoot can be reduced by adding a load resistor. The overshoot decays at a rate determined by output capacitor C_{OUT} and the internal and external load resistance. The rate of decay is given by:

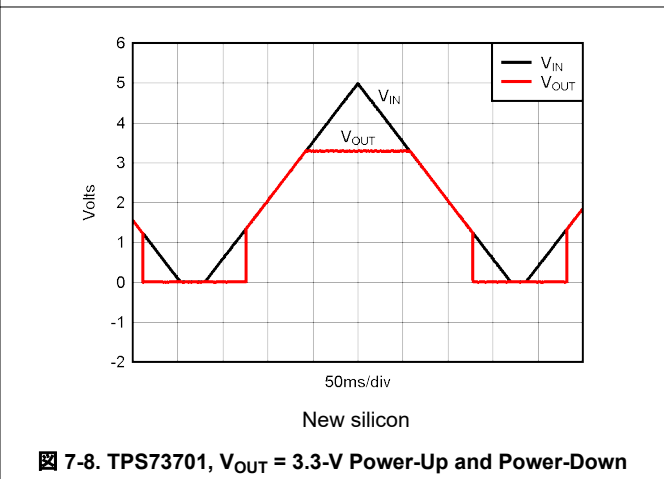
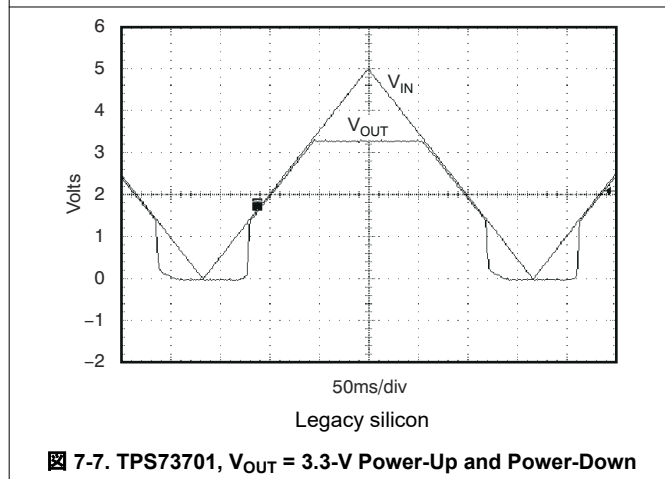
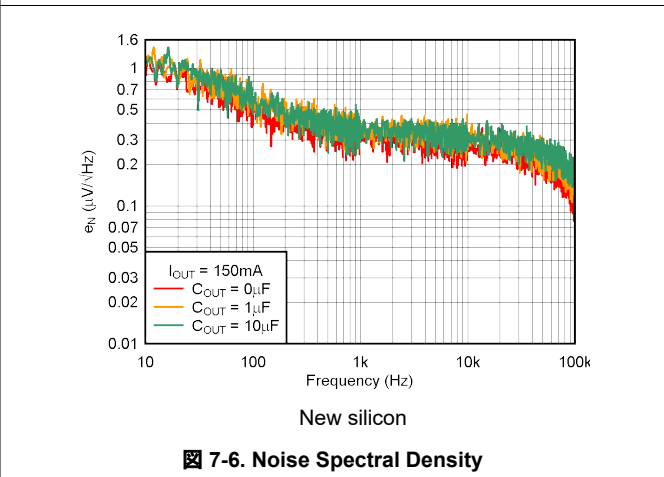
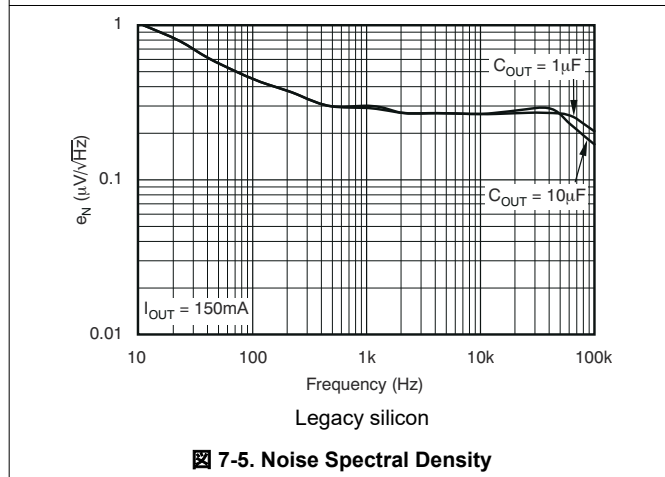
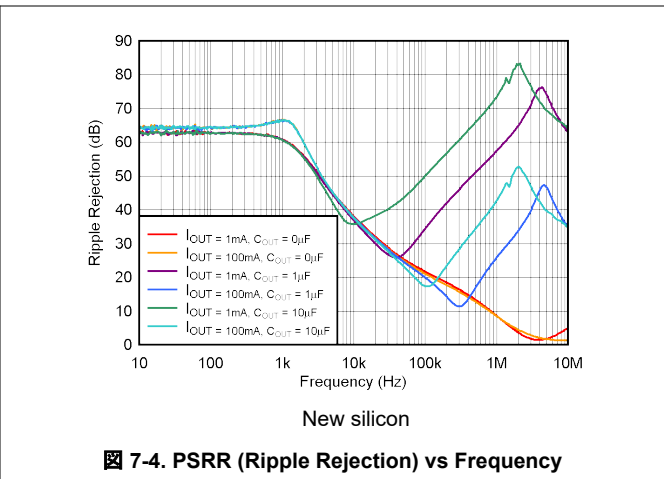
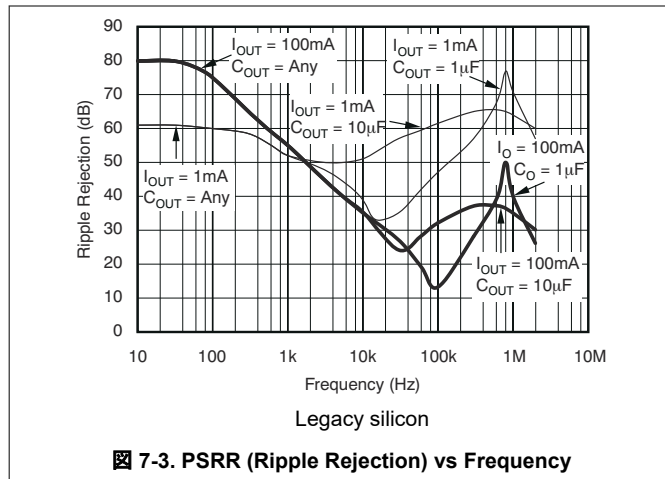
(Fixed voltage version)

$$\frac{dV}{dT} = \frac{V_{\text{OUT}}}{C_{\text{OUT}} \times 80\text{k}\Omega \parallel R_{\text{LOAD}}} \quad (4)$$

(Adjustable voltage version)

$$\frac{dV}{dT} = \frac{V_{\text{OUT}}}{C_{\text{OUT}} \times 80\text{k}\Omega \parallel (R_1 + R_2) \parallel R_{\text{LOAD}}} \quad (5)$$

7.2.3 Application Curves



7.3 Best Design Practices

Place at least one 1- μ F ceramic capacitor as close as possible to the OUT pin of the regulator.

Do not place the output capacitor more than 10-mm away from the regulator.

Connect a 1- μ F low equivalent series resistance (ESR) capacitor across the IN pin and GND input of the regulator for improved transient performance.

Do not exceed the absolute maximum ratings.

7.4 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.2 V and 5.5 V. The input voltage range provides adequate headroom for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR help improve the output noise performance.

7.5 Layout

7.5.1 Layout Guidelines

To improve AC performance such as PSRR, output noise, and transient response, design the printed-circuit-board (PCB) with ground plane connections for the V_{IN} and V_{OUT} capacitors. Furthermore, make sure the ground plane is connected at the GND pin of the device. In addition, the ground connection for the bypass capacitor must connect directly to the GND pin of the device.

7.5.1.1 Power Dissipation

Knowing the device power dissipation and proper sizing of the thermal plane that is connected to the tab or pad is critical to avoiding thermal shutdown and to provide reliable operation.

Power dissipation of the device depends on input voltage and load conditions and can be calculated using 式 6:

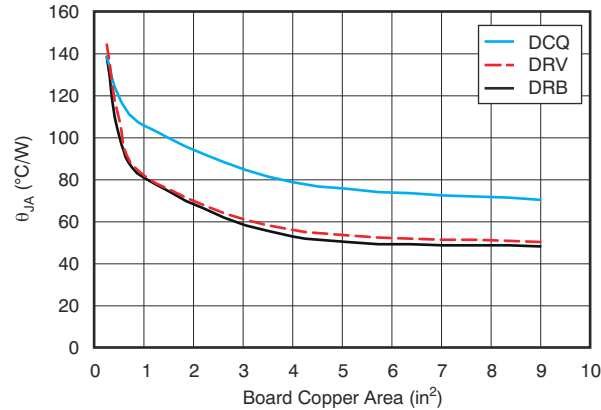
$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (6)$$

Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

On both the VSON (DRB) and WSON (DRV) packages, the primary conduction path for heat is through the exposed pad to the printed circuit board (PCB). The pad can be connected to ground or left floating; however, the pad must be attached to an appropriate amount of copper PCB area to make sure the device does not overheat. On the SOT-223 (DCQ) package, the primary conduction path for heat is through the tab to the PCB. That tab must be connected to ground. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device and can be calculated using 式 7:

$$R_{\theta JA} = \frac{(+125^{\circ}\text{C} - T_A)}{P_D} \quad (7)$$

Knowing the maximum $R_{\theta JA}$, the minimum amount of PCB copper area needed for appropriate heat sinking can be estimated using 図 7-9.



$R_{\theta JA}$ value at board size of 9 in² (that is, 3 in × 3 in) is a JEDEC standard.

図 7-9. $R_{\theta JA}$ vs Board Size

図 7-9 shows the variation of $R_{\theta JA}$ as a function of ground plane copper area in the board. 図 7-9 is intended only as a guideline to demonstrate the effects of heat spreading in the ground plane and is not intended to be used to estimate actual thermal performance in real application environments.

注

When the device is mounted on an application PCB, use Ψ_{JT} and Ψ_{JB} , as explained in the *Thermal Information* table.

7.5.1.2 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle on and off. This cycling limits the dissipation of the regulator, protecting the regulator from damage caused by overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, limit junction temperature to 125°C maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection must trigger at least 35°C above the maximum expected ambient condition of the application. This buffer produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS737 is designed to protect against overload conditions. This circuitry is not intended to replace proper heat sinking. Continuously running the TPS737 into thermal shutdown degrades device reliability.

7.5.1.3 Estimating Junction Temperature

Using the thermal metrics Ψ_{JT} and Ψ_{JB} , as shown in the *Thermal Information* table, the junction temperature can be estimated with corresponding formulas (given in 式 8). For backward compatibility, an older $\theta_{JC, Top}$ parameter is listed as well.

$$\begin{aligned} \Psi_{JT}: T_J &= T_T + \Psi_{JT} \cdot P_D \\ \Psi_{JB}: T_J &= T_B + \Psi_{JB} \cdot P_D \end{aligned} \quad (8)$$

where:

- P_D is the power dissipation shown by 式 6

- T_T is the temperature at the center-top of the device package
- T_B is the PCB temperature measured 1-mm away from the device package *on the PCB surface* (as 図 7-11 shows)

注

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B , see the [Using New Thermal Metrics application note](#), available for download at www.ti.com.

As 図 7-10 shows, the new thermal metrics (Ψ_{JT} and Ψ_{JB}) have very little dependency on board size. That is, using Ψ_{JT} or Ψ_{JB} with 式 8 is a good way to estimate T_J by simply measuring T_T or T_B , regardless of the application board size.

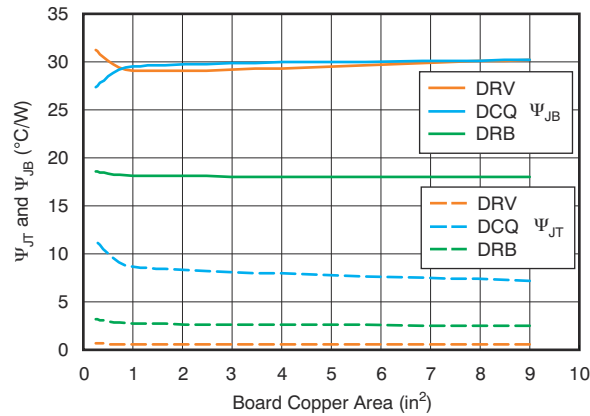
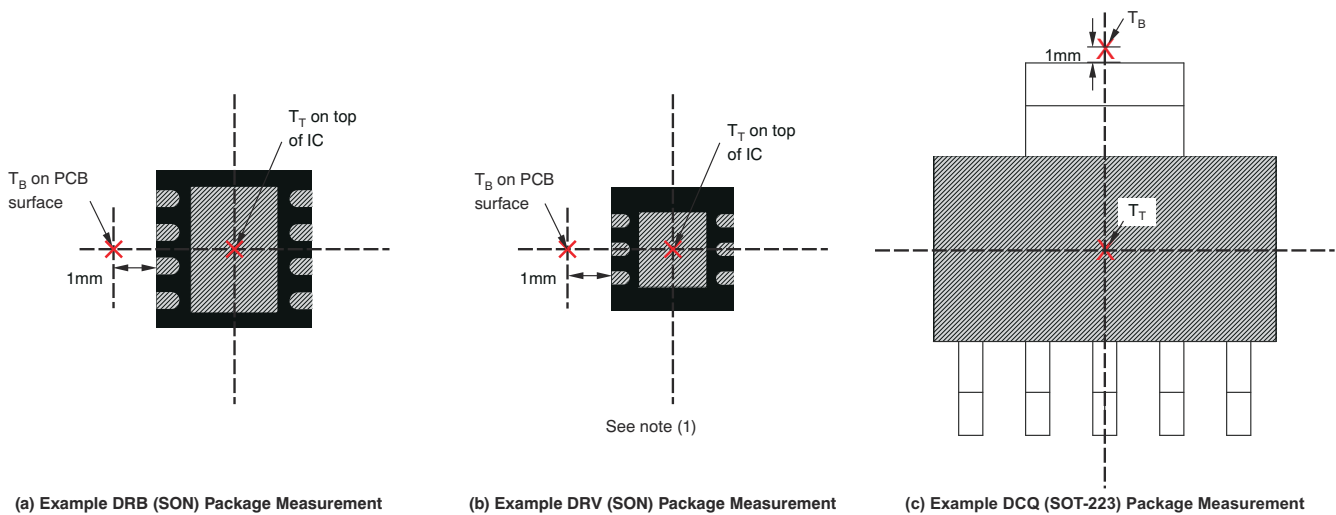


図 7-10. Ψ_{JT} and Ψ_{JB} vs Board Size

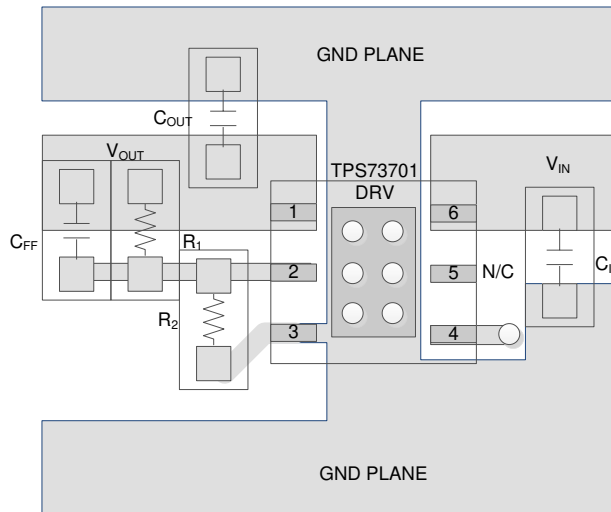
For a more detailed discussion of why TI does not recommend using $\theta_{JC(top)}$ to determine thermal characteristics, see the [Using New Thermal Metrics application note](#), available for download at www.ti.com. For further information, see the [Semiconductor and IC Package Thermal Metrics application note](#), also available on the TI website. 図 7-11 shows the measuring points for DRB, DRV, and DCQ packages.



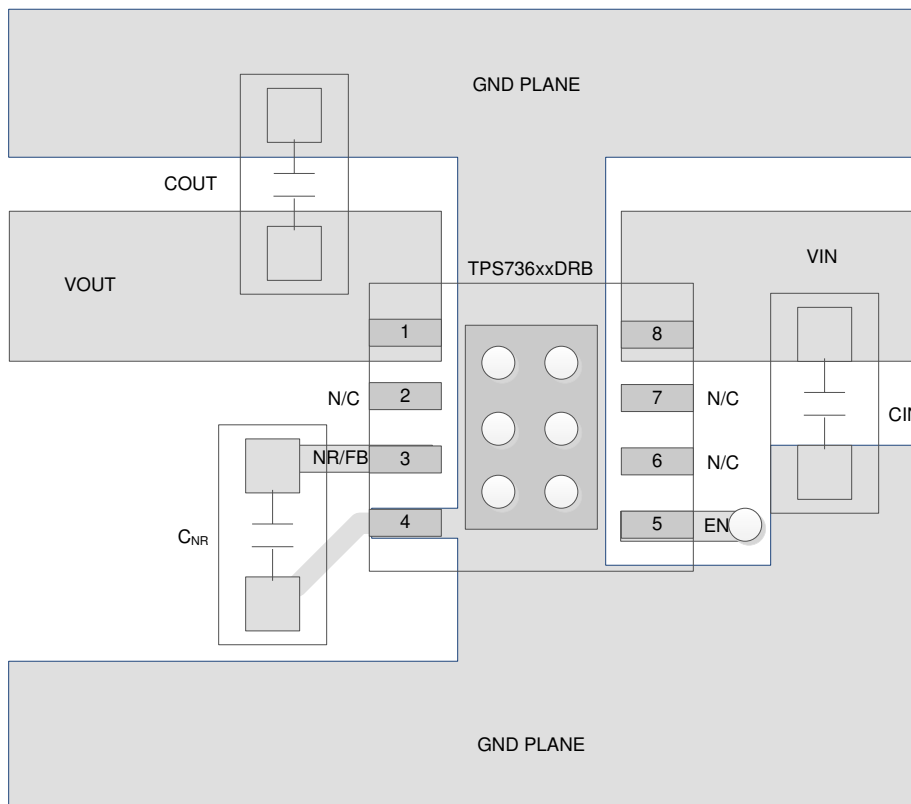
A. Power dissipation can limit operating range. Check the *Thermal Information* table.

図 7-11. Measuring Points for T_T and T_B

7.5.2 Layout Example



7-12. Layout Example



7-13. Fixed Output Voltage Option Layout (DRB Package)

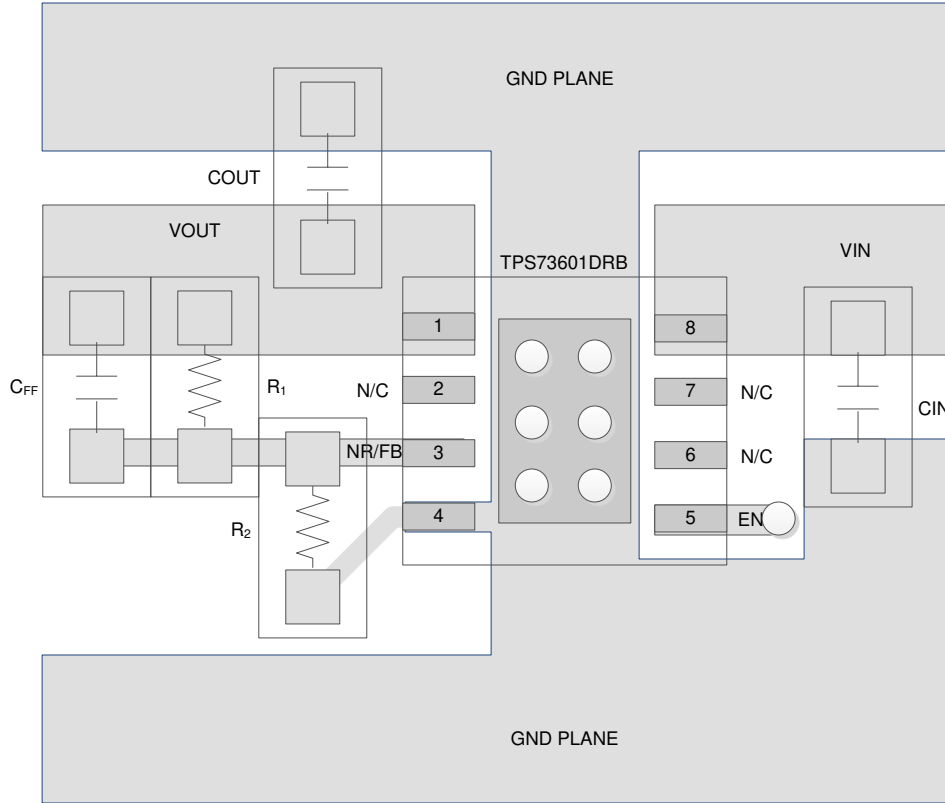


図 7-14. Adjustable Output Voltage Option Layout (DRB Package)

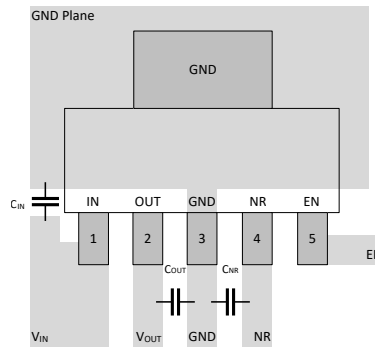
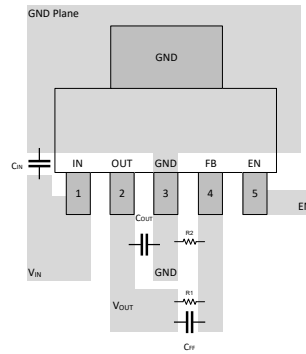


図 7-15. Layout Example for the DCQ Package Fixed Version



☒ 7-16. Layout Example for the DCQ Package Adjustable Version

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS737. The [TPS73701DRVEVM-529 evaluation module](#) (and related [user's guide](#)) can be requested at the Texas Instruments website through the product folders or purchased directly from the [TI eStore](#).

8.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS737 is available through the product folders under *Tools & Software*.

8.1.2 Device Nomenclature

表 8-1. Ordering Information ⁽¹⁾

PRODUCT	DESCRIPTION ⁽¹⁾
TPS737xxyyyz(M3)	<p>xx is the nominal output voltage (for example, 25 = 2.5 V, 01 = Adjustable ⁽²⁾).</p> <p>yyy is the package designator.</p> <p>z is the package quantity.</p> <p>M3 is a suffix designator for devices that only use the latest manufacturing flow (CSO: RFB). Devices without this suffix can ship with the <i>legacy silicon</i> (CSO: DLN) or the <i>new silicon</i> (CSO: RFB). The reel packaging label provides CSO information to distinguish which silicon is being used. Device performance for new and legacy silicon is denoted throughout the document.</p>

- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the device product folder at www.ti.com.
- (2) For fixed 1.20-V operation, tie FB to OUT.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [Using New Thermal Metrics application note](#)
- Texas Instruments, [TPS73701DRVEVM-529 User's Guide user guide](#)
- Texas Instruments, [TMS320DM644x Power Reference Design application note](#)
- Texas Instruments, [TPS73x01DRBEVM-518 User's Guide user guide](#)

8.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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8.7 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision T (December 2023) to Revision U (September 2024)	Page
ドキュメント全体を通して「M3 デバイス」の名称を「新しいシリコン」に変更	1
「従来のシリコン」と「新しいシリコン」の情報を区別するため、ドキュメント全体にデバイスの言い回しを追加	1
ドキュメント全体にわたって表、図、相互参照の採番方法を更新.....	1
Changed <i>Typical Characteristics</i> section.....	8
Changed 50 nF to 50 nF·Ω in <i>Input and Output Capacitor Requirements</i> section.....	21
Added new silicon curves to <i>Application Curves</i> section.....	22
Changed ground plane discussion for clarity in <i>Layout Guidelines</i> section.....	23

Changes from Revision S (November 2023) to Revision T (December 2023)	Page
M3 デバイスのステータスを「事前情報」から「量産データ」に変更	1
Added M3 suffix curves to <i>Typical Characteristics</i> section.....	8

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS73701DCQ	ACTIVE	SOT-223	DCQ	6	78	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	TPS73701	Samples
TPS73701DCQG4	ACTIVE	SOT-223	DCQ	6	78	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS73701	Samples
TPS73701DCQR	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	TPS73701	Samples
TPS73701DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS73701	Samples
TPS73701DRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BZN	Samples
TPS73701DRBRG4	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BZN	Samples
TPS73701DRBRM3	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BZN	Samples
TPS73701DRBT	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BZN	Samples
TPS73701DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QTN	Samples
TPS73701DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QTN	Samples
TPS73718DCQ	ACTIVE	SOT-223	DCQ	6	78	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	TPS73718	Samples
TPS73718DCQR	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	TPS73718	Samples
TPS73718DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS73718	Samples
TPS73718DRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	RAL	Samples
TPS73718DRBRM3	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	RAL	Samples
TPS73718DRBT	OBSOLETE	SON	DRB	8		TBD	Call TI	Call TI	-40 to 125	RAL	
TPS73725DCQ	OBSOLETE	SOT-223	DCQ	6		TBD	Call TI	Call TI	-40 to 125	TPS73725	
TPS73725DCQR	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	TPS73725	Samples
TPS73730DRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CVT	Samples
TPS73730DRBRM3	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CVT	Samples
TPS73730DRBT	OBSOLETE	SON	DRB	8		TBD	Call TI	Call TI	-40 to 125	CVT	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS73733DCQ	ACTIVE	SOT-223	DCQ	6	78	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	TPS73733	Samples
TPS73733DCQG4	ACTIVE	SOT-223	DCQ	6	78	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS73733	Samples
TPS73733DCQR	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	TPS73733	Samples
TPS73733DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS73733	Samples
TPS73733DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SIJ	Samples
TPS73733DRVT	OBSOLETE	WSON	DRV	6		TBD	Call TI	Call TI	-40 to 125	SIJ	
TPS73734DCQ	ACTIVE	SOT-223	DCQ	6	78	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OCH	Samples
TPS73734DCQR	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OCH	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TPS737 :

- Automotive : [TPS737-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

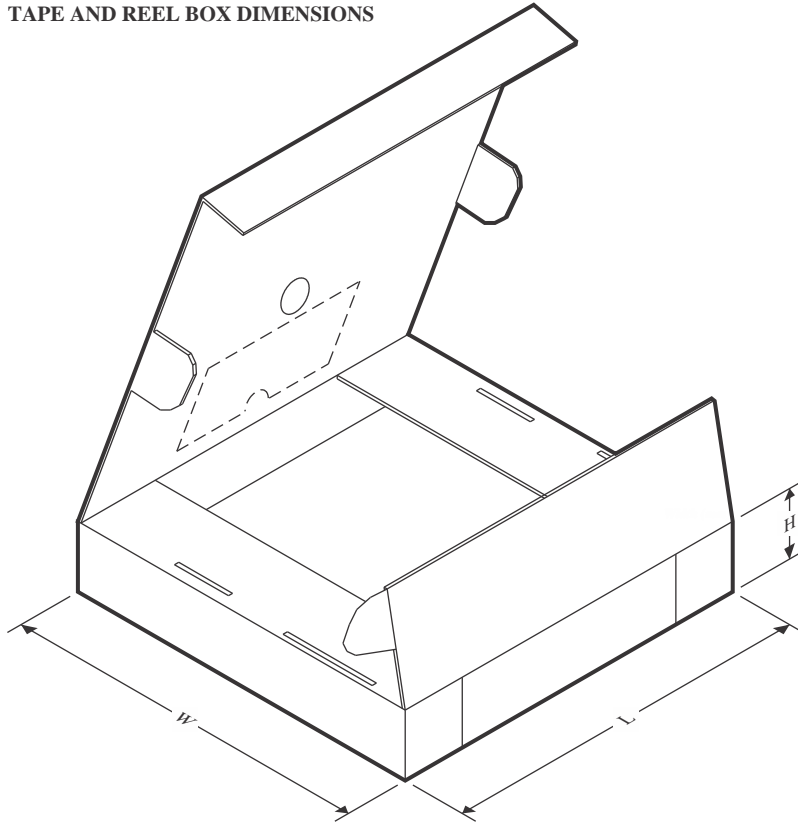
TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73701DCQR	SOT-223	DCQ	6	2500	330.0	12.4	6.85	7.3	1.88	8.0	12.0	Q3
TPS73701DCQRG4	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS73701DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73701DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73701DRBRM3	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73701DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73701DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS73701DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS73718DCQR	SOT-223	DCQ	6	2500	330.0	12.4	6.85	7.3	1.88	8.0	12.0	Q3
TPS73718DCQRG4	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS73718DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73718DRBRM3	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73725DCQR	SOT-223	DCQ	6	2500	330.0	12.4	6.85	7.3	1.88	8.0	12.0	Q3
TPS73730DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73730DRBRM3	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73733DCQR	SOT-223	DCQ	6	2500	330.0	12.4	6.85	7.3	1.88	8.0	12.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73733DCQRG4	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS73733DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS73734DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73701DCQR	SOT-223	DCQ	6	2500	356.0	356.0	36.0
TPS73701DCQRG4	SOT-223	DCQ	6	2500	346.0	346.0	29.0
TPS73701DRBR	SON	DRB	8	3000	552.0	346.0	36.0
TPS73701DRBR	SON	DRB	8	3000	356.0	356.0	35.0
TPS73701DRBRM3	SON	DRB	8	3000	367.0	367.0	35.0
TPS73701DRBT	SON	DRB	8	250	552.0	185.0	36.0
TPS73701DRVR	WSON	DRV	6	3000	213.0	191.0	35.0
TPS73701DRVT	WSON	DRV	6	250	213.0	191.0	35.0
TPS73718DCQR	SOT-223	DCQ	6	2500	356.0	356.0	36.0
TPS73718DCQRG4	SOT-223	DCQ	6	2500	346.0	346.0	29.0
TPS73718DRBR	SON	DRB	8	3000	356.0	356.0	35.0
TPS73718DRBRM3	SON	DRB	8	3000	367.0	367.0	35.0
TPS73725DCQR	SOT-223	DCQ	6	2500	356.0	356.0	36.0
TPS73730DRBR	SON	DRB	8	3000	356.0	356.0	35.0
TPS73730DRBRM3	SON	DRB	8	3000	367.0	367.0	35.0
TPS73733DCQR	SOT-223	DCQ	6	2500	356.0	356.0	36.0
TPS73733DCQRG4	SOT-223	DCQ	6	2500	346.0	346.0	41.0
TPS73733DRVR	WSON	DRV	6	3000	213.0	191.0	35.0

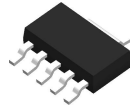
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73734DCQR	SOT-223	DCQ	6	2500	346.0	346.0	41.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TPS73701DCQ	DCQ	SOT-223	6	78	543	8.6	3606.8	2.67
TPS73701DCQG4	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
TPS73701DRBR	DRB	VSON	8	3000	381	4.83	2286	0
TPS73701DRBRG4	DRB	VSON	8	3000	381	4.83	2286	0
TPS73701DRBT	DRB	VSON	8	250	381	4.83	2286	0
TPS73718DCQ	DCQ	SOT-223	6	78	543	8.6	3606.8	2.67
TPS73733DCQ	DCQ	SOT-223	6	78	543	8.6	3606.8	2.67
TPS73733DCQG4	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
TPS73734DCQ	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68

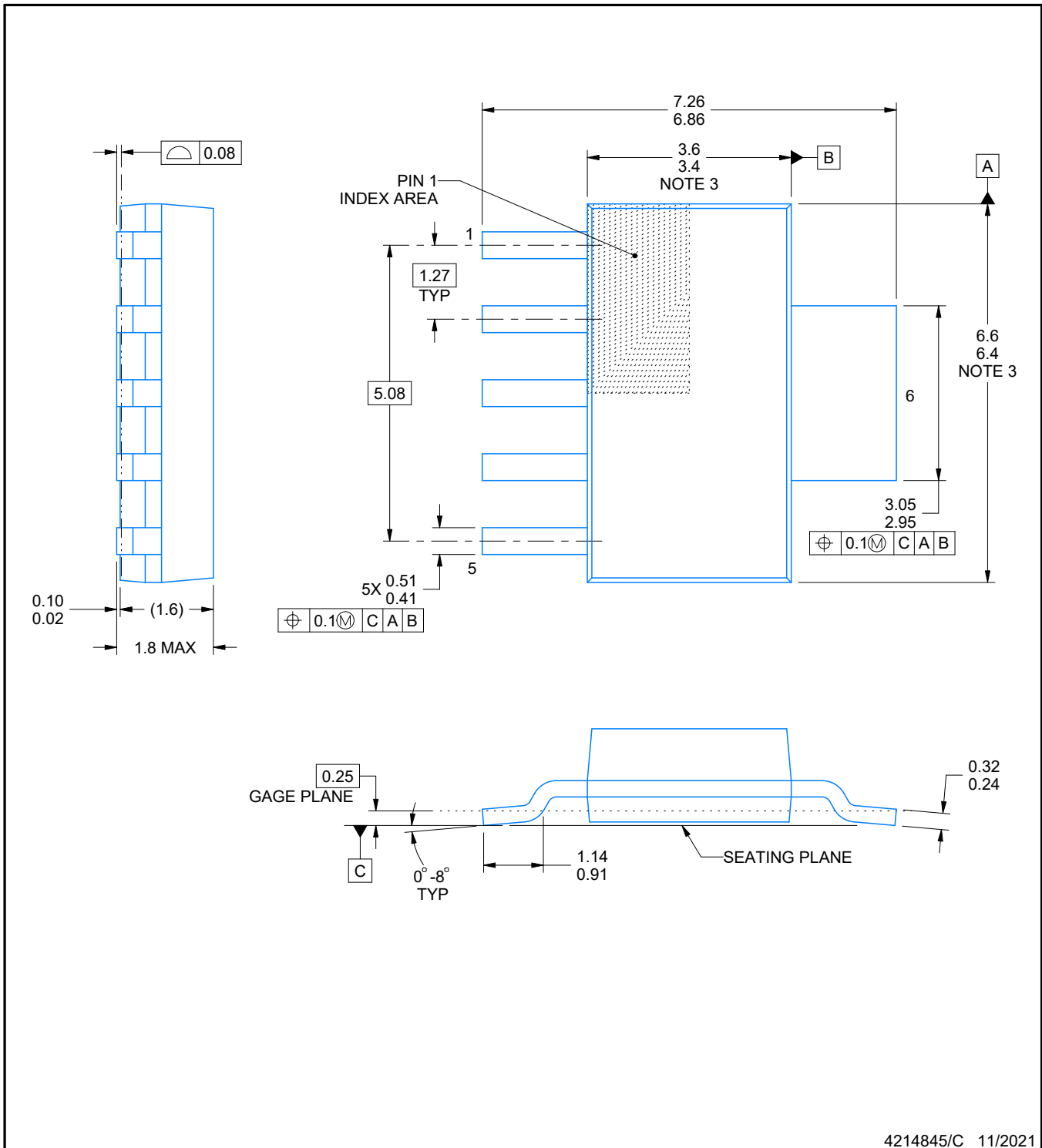
DCQ0006A



PACKAGE OUTLINE

SOT - 1.8 mm max height

PLASTIC SMALL OUTLINE



4214845/C 11/2021

NOTES:

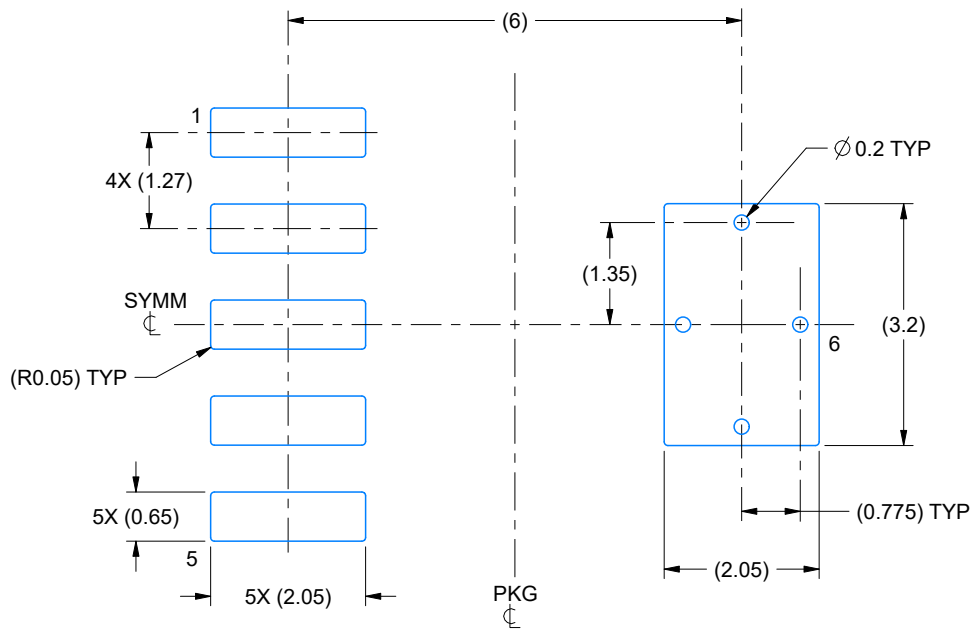
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

EXAMPLE BOARD LAYOUT

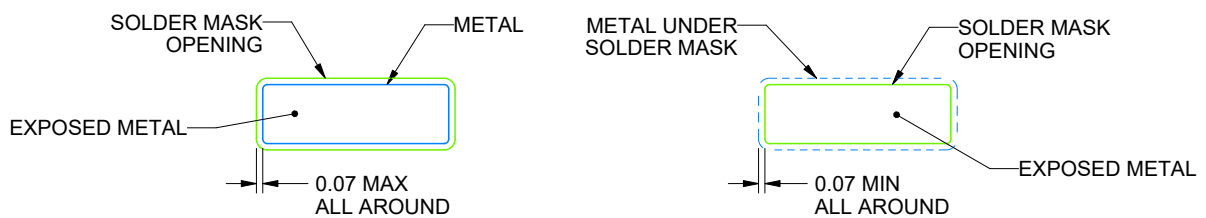
DCQ0006A

SOT - 1.8 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214845/C 11/2021

NOTES: (continued)

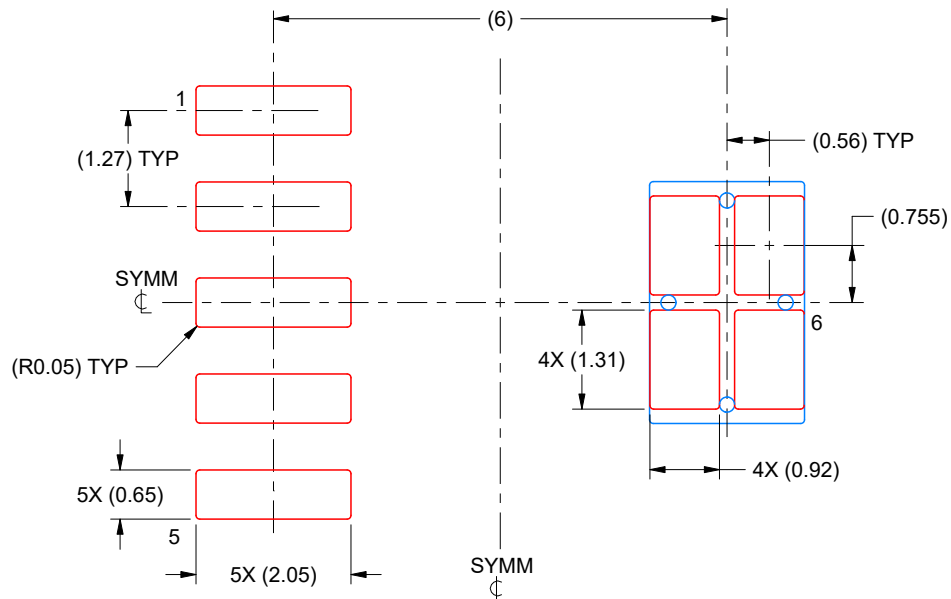
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DCQ0006A

SOT - 1.8 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214845/C 11/2021

NOTES: (continued)

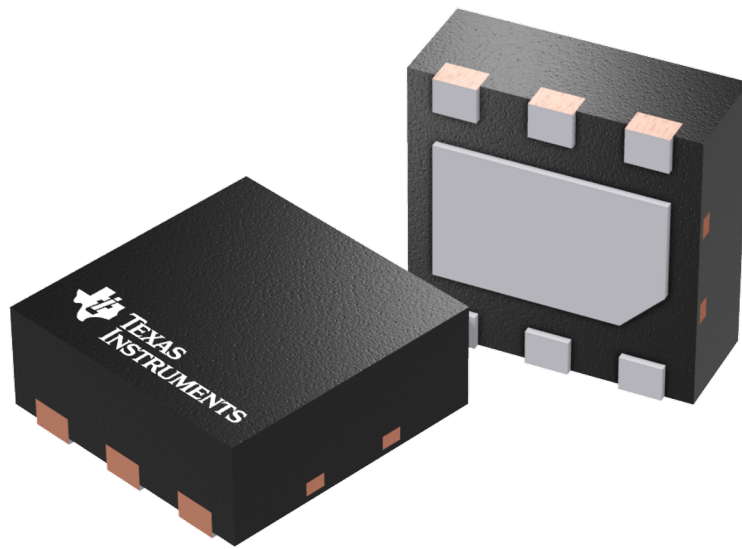
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DRV 6

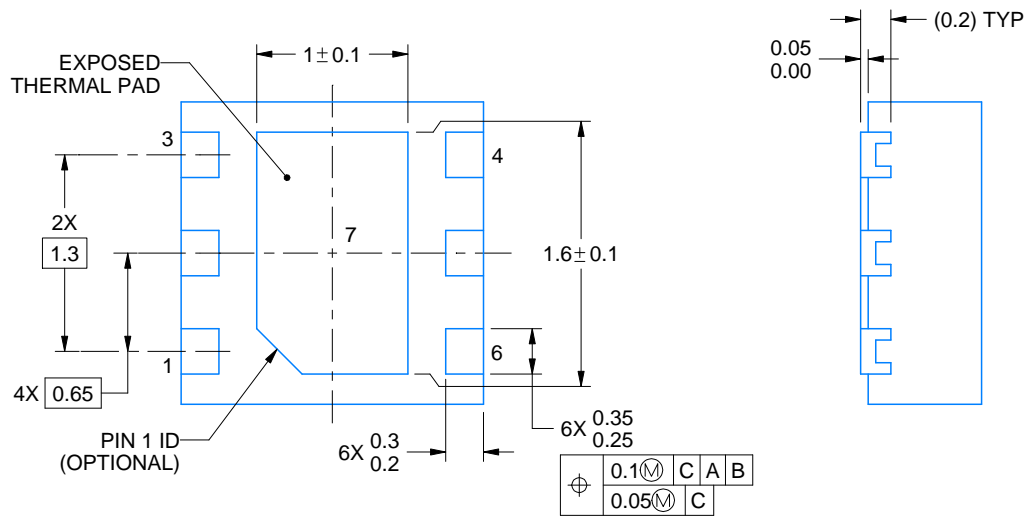
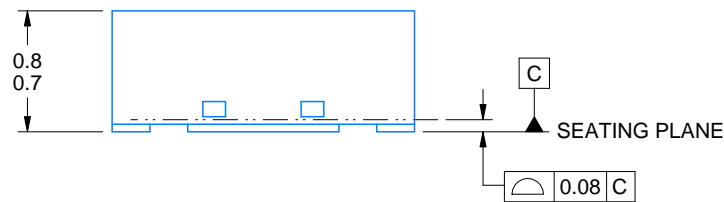
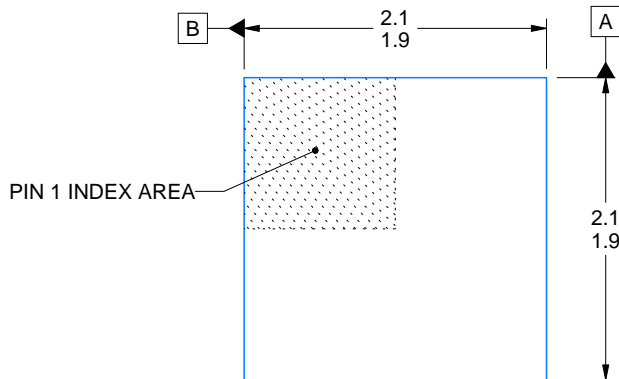
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4206925/F



4225563/A 12/2019

NOTES:

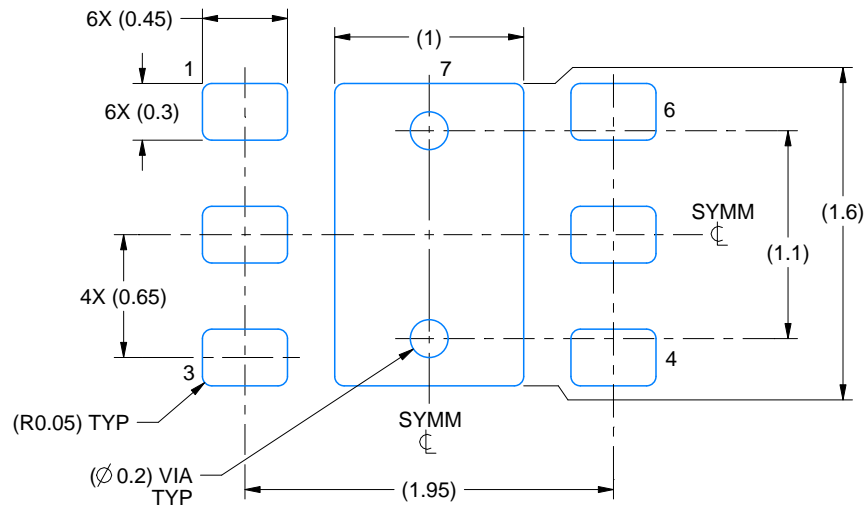
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

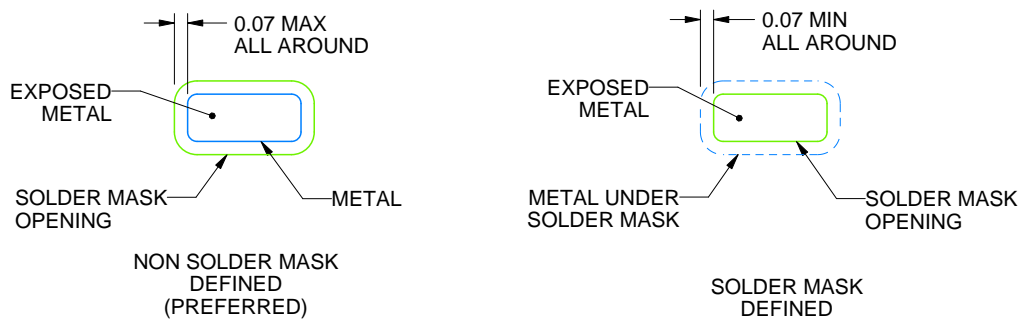
DRV0006D

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X



SOLDER MASK DETAILS

4225563/A 12/2019

NOTES: (continued)

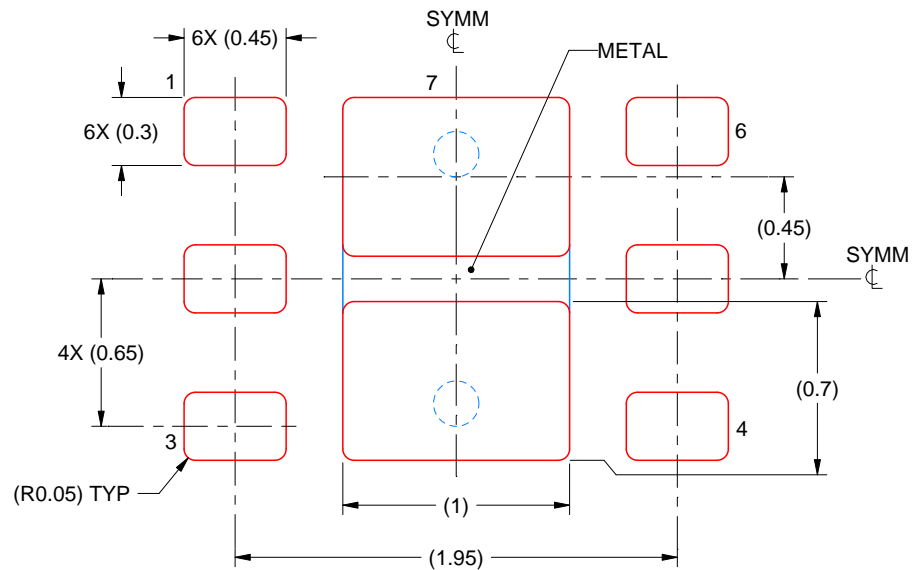
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DRV0006D

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4225563/A 12/2019

NOTES: (continued)

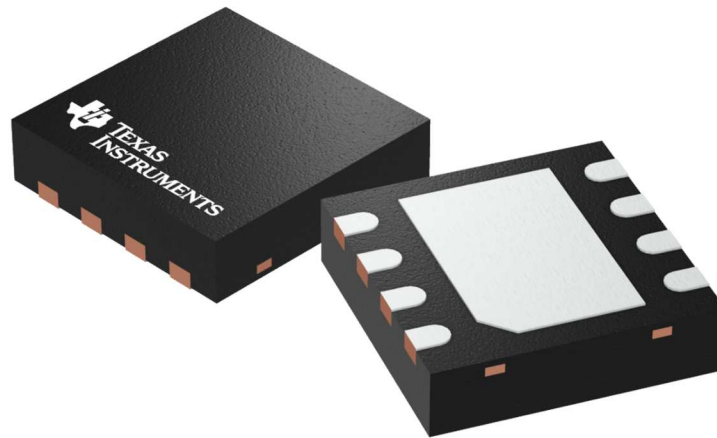
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DRB 8

GENERIC PACKAGE VIEW

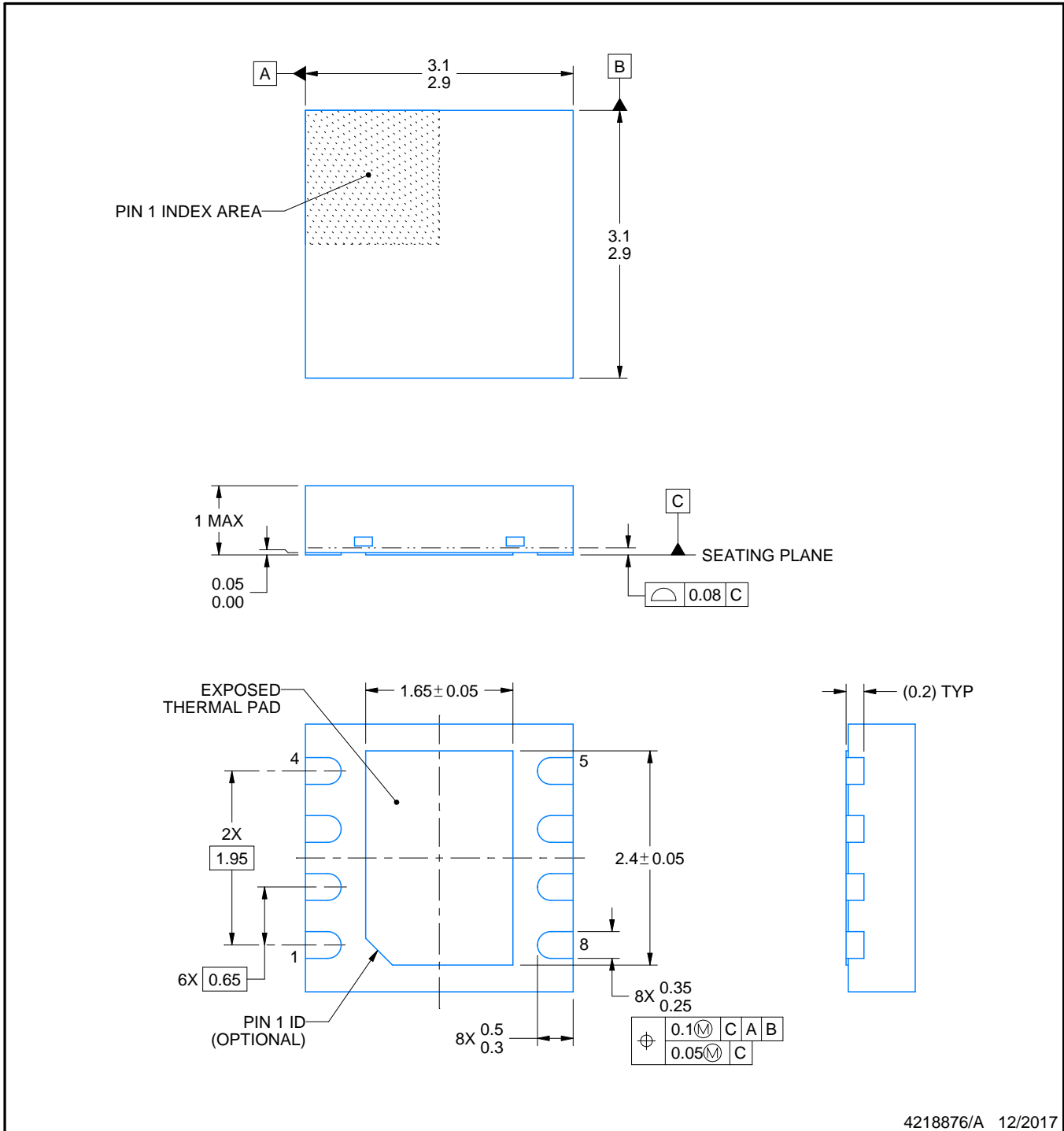
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203482/L



4218876/A 12/2017

NOTES:

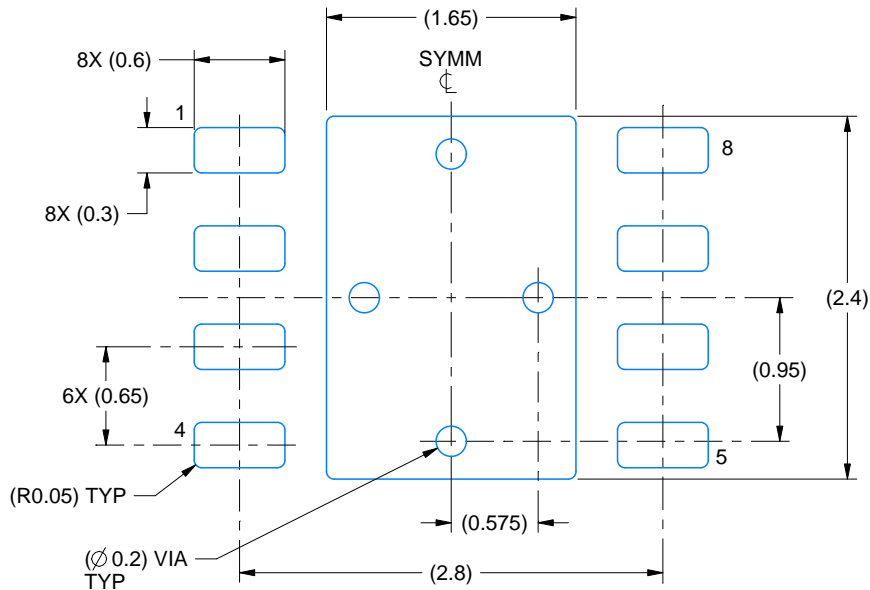
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

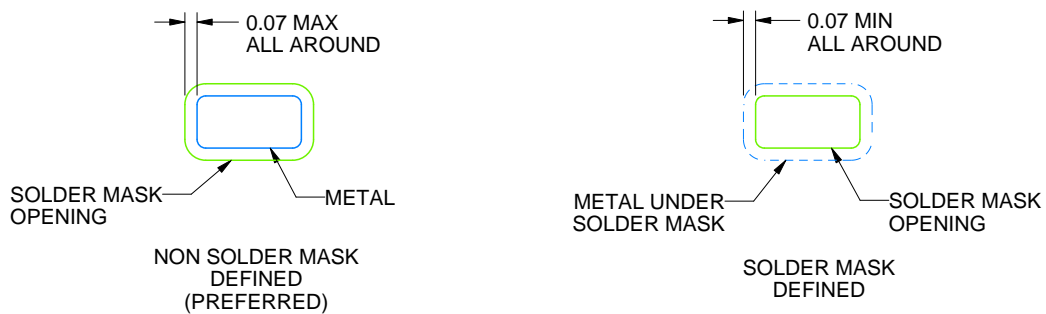
DRB0008B

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4218876/A 12/2017

NOTES: (continued)

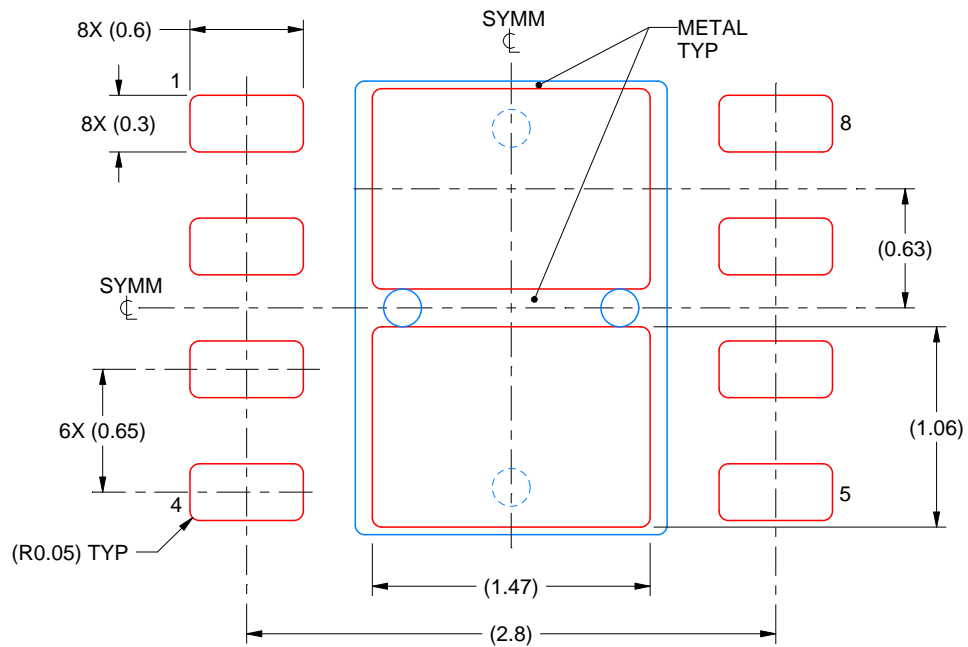
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRB0008B

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218876/A 12/2017

NOTES: (continued)

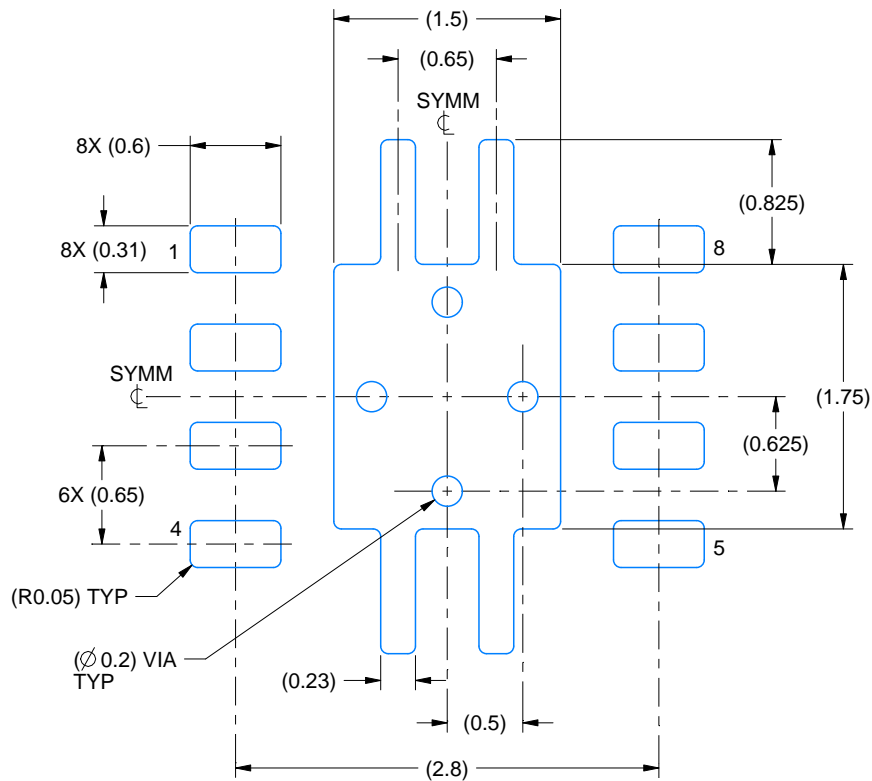
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

EXAMPLE BOARD LAYOUT

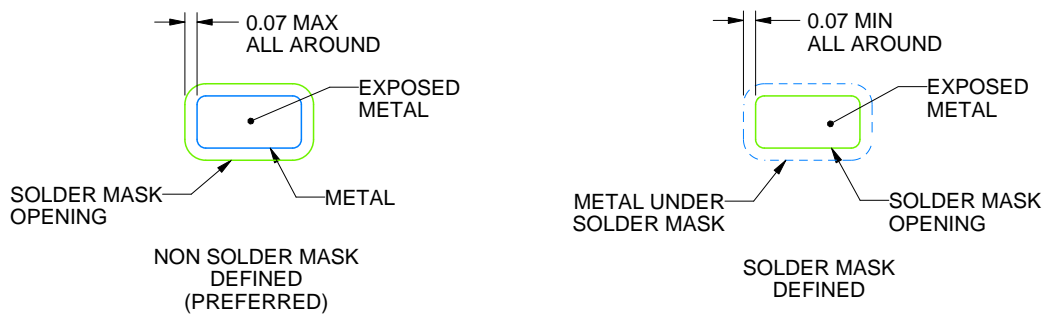
DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4218875/A 01/2018

NOTES: (continued)

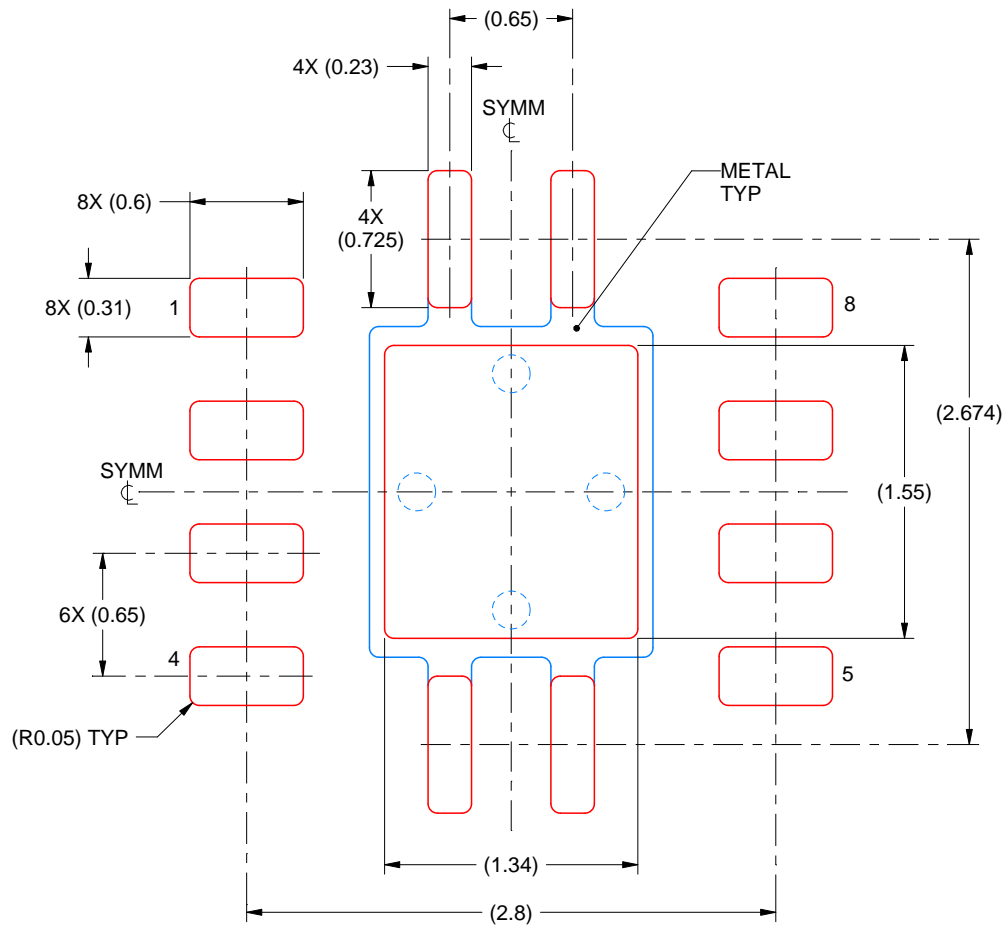
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slue271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218875/A 01/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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