

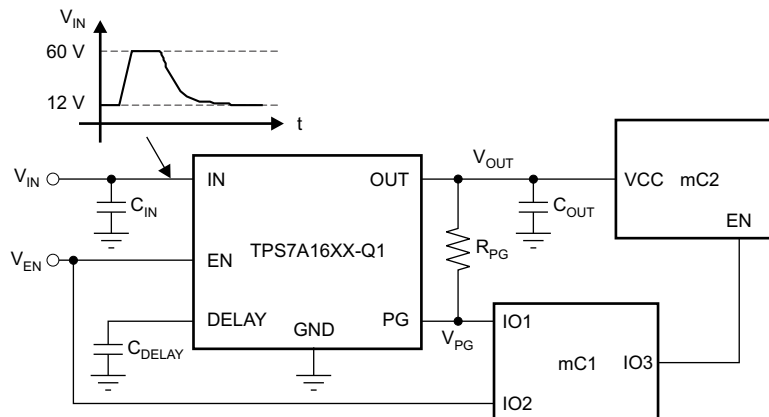
TPS7A16-Q1 60V、5 μ A I_Q、100mA、低ドロップアウト電圧レギュレータ、イネーブルおよびパワー・グッド搭載

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
 - 温度グレード 1: -40°C ~ +125°C、T_A
 - デバイス HBM ESD 分類レベル H2
 - デバイス CDM ESD 分類レベル C3B
- 広い入力電圧範囲: 3V ~ 60V
- 超低静置電流: 5 μ A
- 静置電流 (シャットダウン時): 1 μ A
- 出力電流: 100mA
- 低いドロップアウト電圧: 60mV (20mA の場合)
- 精度: 2%
- 利用可能なバージョン:
 - 固定出力電圧: 3.3V、5V
 - 可変バージョン: 約 1.2 ~ 18.5V
- 遅延時間をプログラム可能なパワー・グッド
- 電流制限およびサーマル・シャットダウン保護機能
- セラミック出力コンデンサで安定動作: 2.2 μ F 以上
- 機能安全対応
 - 機能安全システムの設計に役立つ資料を利用可能
- パッケージ: 熱特性の高い 8 ピン HVSSOP サーマル・パッド・パッケージ

2 アプリケーション

- 緊急通話 (eCall)
- バッテリー管理システム (BMS)
- オンボード・チャージャ (OBC) とワイヤレス・チャージャ
- DC/DC コンバータ



代表的なアプリケーション回路図

3 説明

TPS7A16-Q1 超低消費電力、低ドロップアウト (LDO) 電圧レギュレータは、非常に低い静置電流、高い入力電圧、および熱特性の優れた小型パッケージが特長です。

TPS7A16-Q1 は、連続的または散発的 (電源バックアップ) に使用するバッテリー駆動アプリケーション向けに設計されています。こうした用途では、システムのバッテリー駆動時間を伸ばすために超低静置電流が不可欠です。

TPS7A16-Q1 は標準 CMOS ロジック互換のイネーブル・ピン (EN) と、遅延時間をユーザーがプログラム可能なオープンドレインのアクティブ High パワー・グッド出力 (PG) を備えています。これらのピンは、電源レールのシーケンシングを必要とするマイクロコントローラ・ベースのバッテリー駆動アプリケーションで使うことを目的としています。

さらに TPS7A16-Q1 は、セル数の多い電動工具パックから車載アプリケーションに至るまで、各種のマルチセル・ソリューションから低電圧電源を生成する用途で設計されています。適切にレギュレーションされた電圧レールを提供できるだけでなく、過渡電圧時にもレギュレーションを維持できます。これらの機能により、よりシンプルでコスト効率の優れた電氣的サージ保護回路が実現できます。

パッケージ情報

部品番号	パッケージ (1)	本体サイズ (公称)
TPS7A16-Q1	DGN (HVSSOP, 8)	3.00mm x 3.00mm

- (1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



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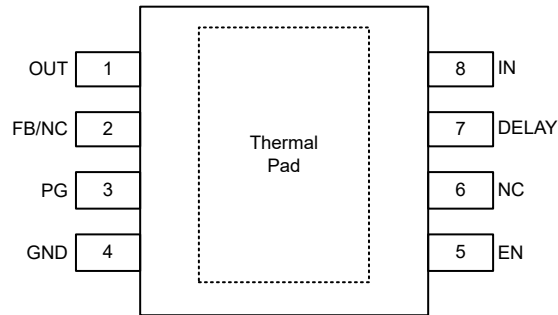
4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (August 2014) to Revision E (May 2023)	Page
• 「特長」セクションに機能安全とパッケージの箇条書き項目を追加.....	1
• 「アプリケーション」セクションにリンクを追加.....	1
• Changed pinout drawing to show pin 2 as FB/NC instead of FB/DNC and changed description of pin 2 in <i>Pin Functions</i> table.....	3

Changes from Revision C (August 2014) to Revision D (May 2016)	Page
• データシートのタイトルを変更.....	1
• Changed <i>Handling Ratings</i> table to <i>ESD Ratings</i> ; moved storage temperature to <i>Absolute Maximum Ratings</i>	4
• Changed maximum EN pin voltage and added a row for EN slew rate.....	5
• Changed UNIT for accuracy on V_{OUT}	6
• Changed <i>Ground current</i> to <i>Quiescent current</i>	6
• Changed 図 6-2	7
• Changed caption of 図 6-3	7
• Changed and added text in <i>Enable (EN)</i> section.....	10
• Moved three paragraphs of text from <i>Layout Examples</i> to <i>Layout Guidelines</i>	18

5 Pin Configuration and Functions



NC – No internal connection

图 5-1. DGN Package, 8-Pin HVSSOP With Exposed Thermal Pad (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
DELAY	7	O	Delay pin. Connect a capacitor to GND to adjust the PG delay time; leave open if the reset function is not needed.
EN	5	I	Enable pin. This pin turns the regulator on or off. If $V_{EN} \geq V_{EN_HI}$, the regulator is enabled. If $V_{EN} \leq V_{EN_LO}$, the regulator is disabled. If not used, the EN pin can be connected to IN. Make sure that $V_{EN} \leq V_{IN}$ at all times.
FB/NC	2	I	This pin is a feedback pin when using an external resistor divider or an NC pin when using the device with a fixed output voltage. When using the adjustable device, this pin must be connected through a resistor divider to the output for the device to function. If using a fixed output this pin can either be left floating or connected to GND.
GND	4	—	Ground pin
IN	8	I	Regulator input supply pin. A capacitor > 0.1 μ F must be tied from this pin to ground to assure stability. Connect a 10- μ F ceramic capacitor from IN to GND (as close to the device as possible) to reduce circuit sensitivity to printed-circuit-board (PCB) layout, especially when long input tracer or high source impedances are encountered.
NC	6	—	This pin can be left open or tied to any voltage between GND and IN.
OUT	1	O	Regulator output pin. A capacitor > 2.2 μ F must be tied from this pin to ground to assure stability. Connect a 10- μ F ceramic capacitor from OUT to GND (as close to the device as possible) to maximize ac performance.
PG	3	O	Power-good pin. Open-collector output; leave open or connect to GND if the power-good function is not needed.
Thermal pad		—	Solder to printed circuit board (PCB) to enhance thermal performance. Although the thermal pad can be left floating, connecting the thermal pad to the GND plane is highly recommended.

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
Voltage	IN pin to GND pin	-0.3	62	V
	OUT pin to GND pin	-0.3	20	
	OUT pin to IN pin	-62	0.3	
	FB pin to GND pin	-0.3	3	
	FB pin to IN pin	-62	0.3	
	EN pin to IN pin	-62	0.3	
	EN pin to GND pin	-0.3	62	
	PG pin to GND pin	-0.3	5.5	
	DELAY pin to GND pin	-0.3	5.5	
Current	Peak output	Internally limited		
Temperature	Operating virtual junction, T _J , absolute maximum range ⁽²⁾	-40	150	°C
	Storage temperature range	-65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Permanent damage does not occur to the part operating within this range, though electrical performance is not guaranteed outside the operating ambient temperature range.

6.2 ESD Ratings

		MIN	MAX	UNIT		
V _(ESD)	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾	-2	2	kV	
		Charged device model (CDM), per AEC Q100-011	Corner pins (OUT, GND, IN, and EN)	-750	750	V
			Other pins	-500	500	

- (1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{IN}	Unregulated input	3		60	V
V _{OUT}	Regulated output	1.2		18	V
EN	Voltage	0		V _{IN}	V
	Slew rate, voltage ramp-up			1.5	V/μs
DELAY	Delay pin voltage	0		5	V
PG	Power-good pin voltage	0		5	V
T _J	Operating junction temperature range	–40		150	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS7A16-Q1	UNIT
		DGN (HVSSOP)	
		8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	66.2	°C/W
R _{θJC(top)}	Junction-to-case(top) thermal resistance	45.9	°C/W
R _{θJB}	Junction-to-board thermal resistance	34.6	°C/W
ψ _{JT}	Junction-to-top characterization parameter	1.9	°C/W
ψ _{JB}	Junction-to-board characterization parameter	34.3	°C/W
R _{θJC(bot)}	Junction-to-case(bottom) thermal resistance	14.9	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application note](#).

6.5 Electrical Characteristics

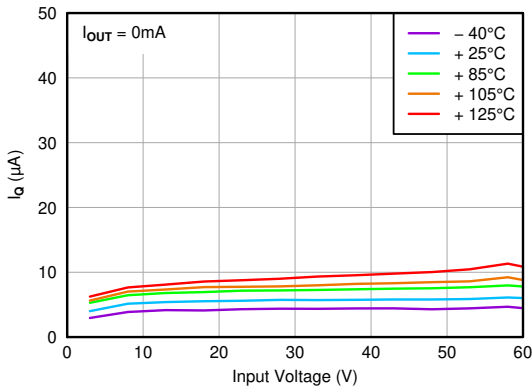
at $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$ or $V_{IN} = 3\text{ V}$ (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT} = 10\ \mu\text{A}$, $C_{IN} = 1\ \mu\text{F}$, $C_{OUT} = 2.2\ \mu\text{F}$, and FB tied to OUT (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		3		60	V
V_{REF}	Internal reference	$T_A = 25^\circ\text{C}$, $V_{FB} = V_{REF}$, $V_{IN} = 3\text{ V}$, $I_{OUT} = 10\ \mu\text{A}$	1.169	1.193	1.217	V
V_{UVLO}	Undervoltage lockout threshold			2.7		V
V_{OUT}	Output voltage range	$V_{IN} \geq V_{OUT(NOM)} + 0.5\text{ V}$		V_{REF}	18.5	V
	Nominal accuracy	$T_A = 25^\circ\text{C}$, $V_{IN} = 3\text{ V}$, $I_{OUT} = 10\ \mu\text{A}$	-2%		2%	
	Overall accuracy	$V_{OUT(NOM)} + 0.5\text{ V} \leq V_{IN} \leq 60\text{ V}^{(1)}$ $10\ \mu\text{A} \leq I_{OUT} \leq 100\text{ mA}$	-2%		2%	
$\Delta V_{O(\Delta VI)}$	Line regulation	$3\text{ V} \leq V_{IN} \leq 60\text{ V}$		± 1		% V_{OUT}
$\Delta V_{O(\Delta IO)}$	Load regulation	$10\ \mu\text{A} \leq I_{OUT} \leq 100\text{ mA}$		± 1		% V_{OUT}
V_{DO}	Dropout voltage	$V_{IN} = 4.5\text{ V}$, $V_{OUT(NOM)} = 5\text{ V}$, $I_{OUT} = 20\text{ mA}$		60		mV
		$V_{IN} = 4.5\text{ V}$, $V_{OUT(NOM)} = 5\text{ V}$, $I_{OUT} = 100\text{ mA}$		265	500	mV
I_{LIM}	Current limit	$V_{OUT} = 90\% V_{OUT(NOM)}$, $V_{IN} = 3.0\text{ V}$	101	225	400	mA
I_Q	Quiescent current	$3\text{ V} \leq V_{IN} \leq 60\text{ V}$, $I_{OUT} = 10\ \mu\text{A}$		5	15	μA
		$I_{OUT} = 100\text{ mA}$		5		μA
I_{SHDN}	Shutdown supply current	$V_{EN} = 0.4\text{ V}$		0.59	5.0	μA
I_{FB}	Feedback current ⁽²⁾		-1	0.0	1	μA
I_{EN}	Enable current	$3\text{ V} \leq V_{IN} \leq 12\text{ V}$, $V_{IN} = V_{EN}$	-1	0.01	1	μA
V_{EN_HI}	Enable high-level voltage		1.2			V
V_{EN_LO}	Enable low-level voltage				0.3	V
V_{IT}	PG trip threshold	OUT pin floating, V_{FB} increasing, $V_{IN} \geq V_{IN_MIN}$	85		95	% V_{OUT}
		OUT pin floating, V_{FB} decreasing, $V_{IN} \geq V_{IN_MIN}$	83		93	% V_{OUT}
V_{HYS}	PG trip hysteresis			2.3	4	% V_{OUT}
V_{PG_LO}	PG output low voltage	OUT pin floating, $V_{FB} = 80\% V_{REF}$, $I_{PG} = 1\text{ mA}$			0.4	V
I_{PG_LKG}	PG leakage current	$V_{PG} = V_{OUT(NOM)}$	-1		1	μA
I_{DELAY}	DELAY pin current			1	2	μA
PSRR	Power-supply rejection ratio	$V_{IN} = 3\text{ V}$, $V_{OUT(NOM)} = V_{REF}$, $C_{OUT} = 10\ \mu\text{F}$, $f = 100\text{ Hz}$		50		dB
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		170		$^\circ\text{C}$
		Reset, temperature decreasing		150		$^\circ\text{C}$
T_A	Operating ambient temperature range		-40		125	$^\circ\text{C}$

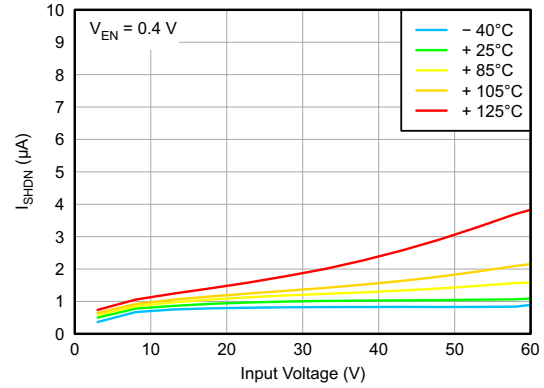
- (1) Maximum input voltage is limited to 24 V because of the package power dissipation limitations at full load ($P \approx (V_{IN} - V_{OUT}) \times I_{OUT} = (24\text{ V} - V_{REF}) \times 50\text{ mA} \approx 1.14\text{ W}$). The device is capable of sourcing a maximum current of 50 mA at higher input voltages as long as the power dissipated is within the thermal limits of the package plus any external heat sinking.
- (2) $I_{FB} > 0$ flows out of the device.

6.6 Typical Characteristics

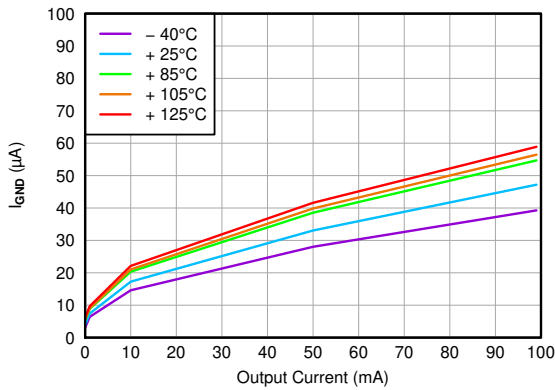
at $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$ or $V_{IN} = 3\text{ V}$ (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT} = 10\ \mu\text{A}$, $C_{IN} = 1\ \mu\text{F}$, $C_{OUT} = 2.2\ \mu\text{F}$, and FB tied to OUT (unless otherwise noted)



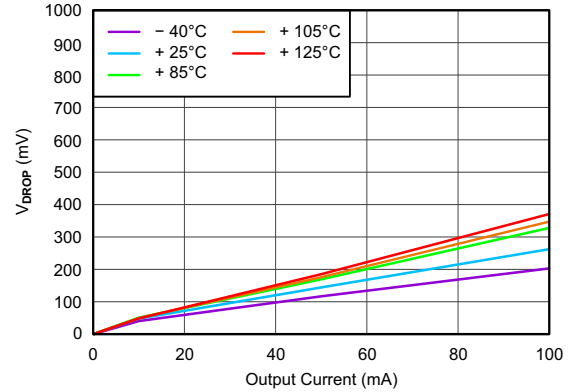
6-1. Quiescent Current vs Input Voltage



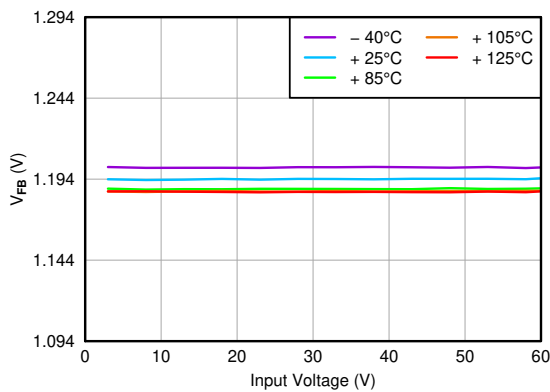
6-2. Shutdown Current vs Input Voltage



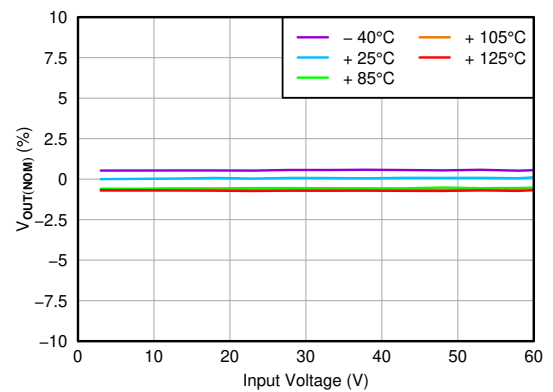
6-3. Quiescent Current vs Output Current



6-4. Dropout Voltage vs Output Current



6-5. Feedback Voltage vs Input Voltage



6-6. Line Regulation

6.6 Typical Characteristics (continued)

at $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$ or $V_{IN} = 3\text{ V}$ (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT} = 10\ \mu\text{A}$, $C_{IN} = 1\ \mu\text{F}$, $C_{OUT} = 2.2\ \mu\text{F}$, and FB tied to OUT (unless otherwise noted)

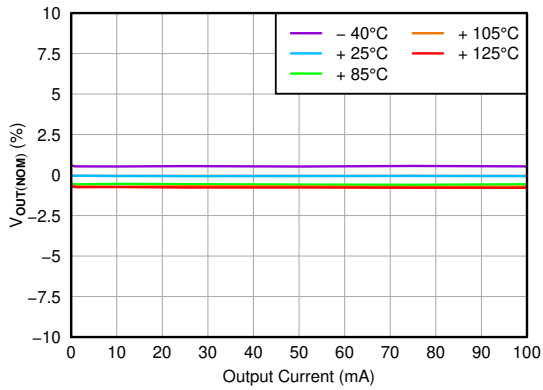


Figure 6-7. Load Regulation

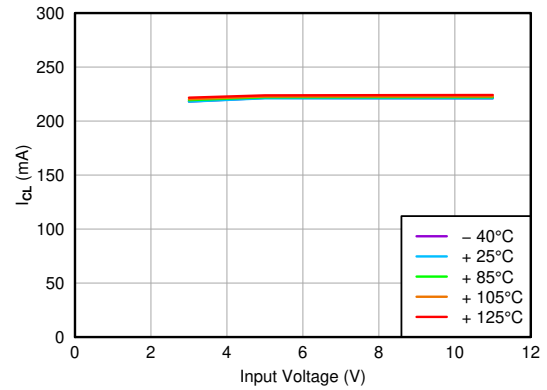


Figure 6-8. Current Limit vs Input Voltage

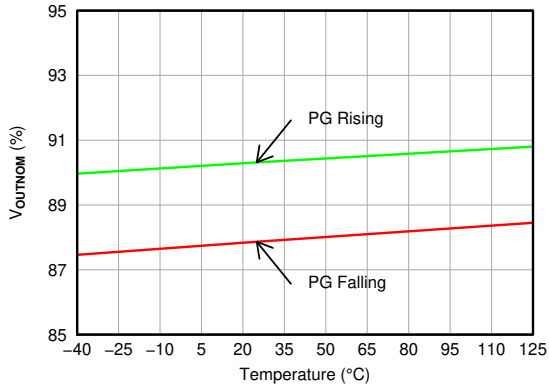


Figure 6-9. Power-Good Threshold Voltage vs Temperature

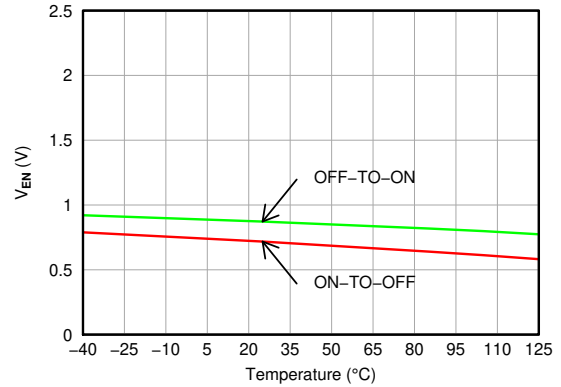


Figure 6-10. Enable Threshold Voltage vs Temperature

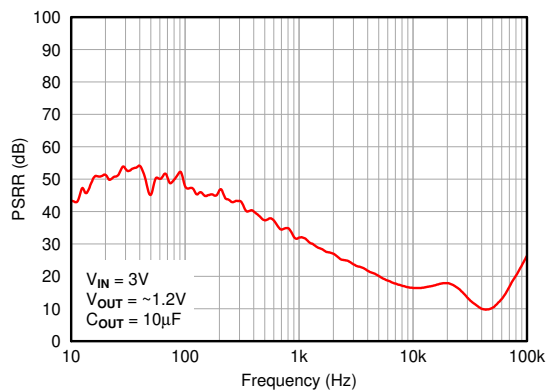


Figure 6-11. Power-Supply Rejection Ratio

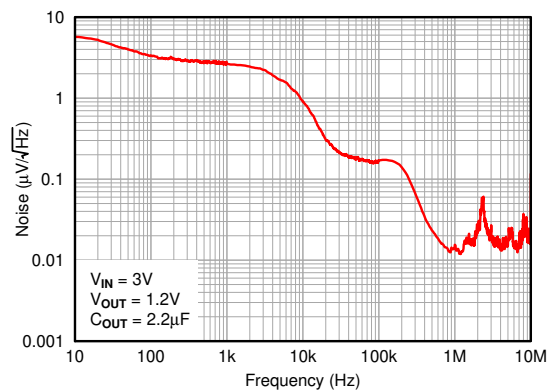
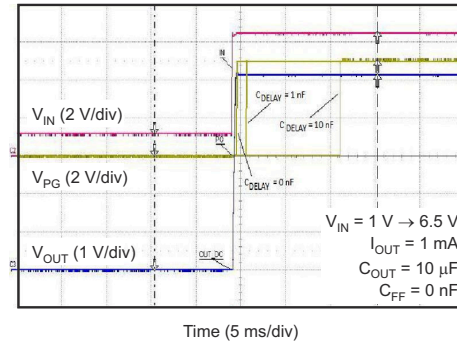


Figure 6-12. Output Spectral Noise Density

6.6 Typical Characteristics (continued)

at $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$ or $V_{IN} = 3\text{ V}$ (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT} = 10\ \mu\text{A}$, $C_{IN} = 1\ \mu\text{F}$, $C_{OUT} = 2.2\ \mu\text{F}$, and FB tied to OUT (unless otherwise noted)



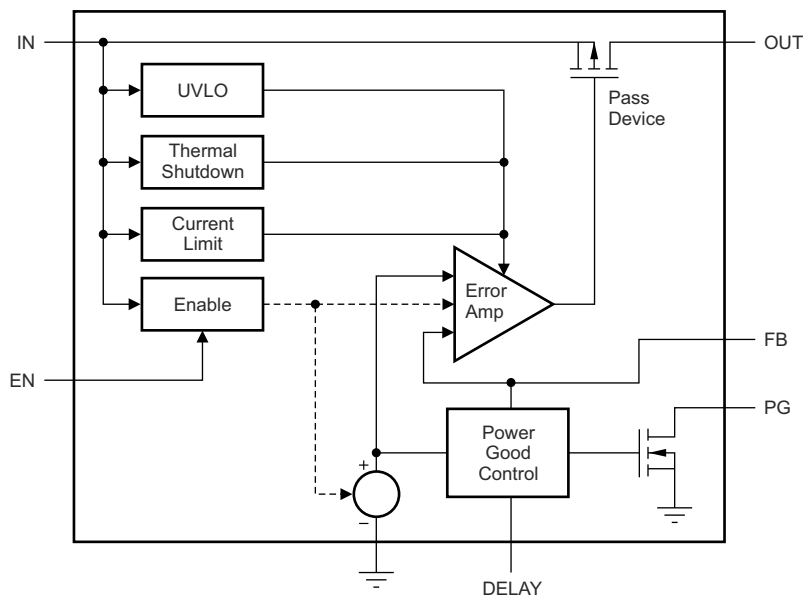
6-13. Power-Good Delay

7 Detailed Description

7.1 Overview

The TPS7A16-Q1 is an ultra low power, low-dropout (LDO) voltage regulator that offers the benefits of ultra-low quiescent current, high input voltage, and miniaturized, high thermal-performance packaging. The TPS7A16-Q1 also offers an enable pin (EN) and integrated open-drain, active-high, power-good output (PG) with a user-programmable delay.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable (EN)

The enable pin is a high-voltage-tolerant pin. A high input on EN activates the device and turns on the regulator. For self-bias applications, connect this input to the V_{IN} pin. Make sure that $V_{EN} \leq V_{IN}$ at all times.

When the enable signal is PWM pulses, the slew rate of the rising and falling edges must be less than $1.5 \text{ V}/\mu\text{s}$. Adding a $0.1\text{-}\mu\text{F}$ capacitor from the EN pin to GND is recommended.

7.3.2 Regulated Output (V_{OUT})

The V_{OUT} pin is the regulated output based on the required voltage. The output has current limitation. During initial power-up, the regulator has a soft-start incorporated to control the initial current through the pass transistor. In the event that the regulator drops out of regulation, the output tracks the input minus a drop based on the load current. When the input voltage drops below the undervoltage lockout (UVLO) threshold, the regulator shuts down until the input voltage recovers above the minimum start-up level.

7.3.3 PG Delay Timer (DELAY)

The power-good delay time (t_{DELAY}) is defined as the time period from when V_{OUT} exceeds the PG trip threshold voltage (V_{IT}) to when the PG output is high. This power-good delay time is set by an external capacitor (C_{DELAY}) connected from the DELAY pin to GND; this capacitor is charged from 0 V to approximately 1.8 V by the DELAY pin current (I_{DELAY}) when V_{OUT} exceeds the PG trip threshold (V_{IT}).

7.4 Device Functional Modes

7.4.1 Power-Good

The power-good (PG) pin is an open-drain output and can be connected to any 5.5-V or lower rail through an external pullup resistor. When no C_{DELAY} is used, the PG output is high-impedance when V_{OUT} is greater than the PG trip threshold (V_{IT}). If V_{OUT} drops below V_{IT} , the open-drain output turns on and pulls the PG output low. If output voltage monitoring is not needed, the PG pin can be left floating or connected to GND.

To provide proper operation of the power-good feature, maintain $V_{IN} \geq 3\text{ V}$ (V_{IN_MIN}).

7.4.2 Power-Good Delay and Delay Capacitor

The power-good delay time (t_{DELAY}) is defined as the time period from when V_{OUT} exceeds the PG trip threshold voltage (V_{IT}) to when the PG output is high. This power-good delay time is set by an external capacitor (C_{DELAY}) connected from the DELAY pin to GND; this capacitor is charged from 0 V to approximately 1.8 V by the DELAY pin current (I_{DELAY}) when V_{OUT} exceeds the PG trip threshold (V_{IT}).

When C_{DELAY} is used, the PG output is high-impedance when V_{OUT} exceeds V_{IT} , and V_{DELAY} exceeds V_{REF} .

The power-good delay time can be calculated using: $t_{DELAY} = (C_{DELAY} \times V_{REF}) / I_{DELAY}$. For example, when $C_{DELAY} = 10\text{ nF}$, the PG delay time is approximately 12 ms; that is, $(10\text{ nF} \times 1.193\text{ V}) / 1\text{ }\mu\text{A} = 11.93\text{ ms}$.

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The TPS7A16-Q1 ultra-low-power voltage regulator offers the benefit of ultra-low quiescent current, high input voltage, and miniaturized, high-thermal-performance packaging.

The TPS7A16-Q1 is designed for continuous or sporadic (power backup) battery-operated applications where ultra-low quiescent current is critical to extending system battery life.

8.2 Typical Applications

8.2.1 TPS7A1601-Q1 Circuit as an Adjustable Regulator

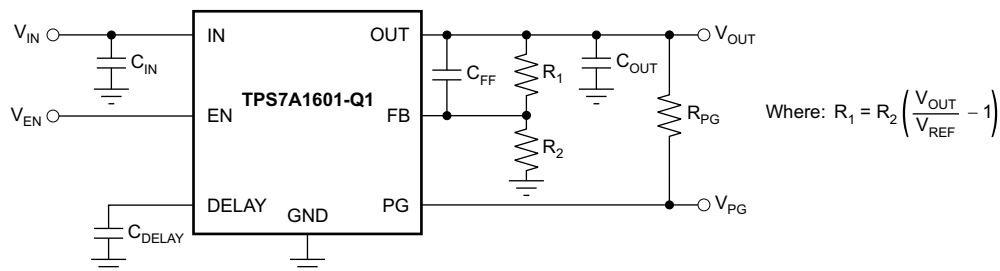


図 8-1. TPS7A1601-Q1 Circuit as an Adjustable Regulator Schematic

8.2.1.1 Design Requirements

表 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	5.5 V to 40 V
Output voltage	5 V
Output current rating	100 mA
Output capacitor range	2.2 μ F to 100 μ F
Delay capacitor range	100 pF to 100 nF

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Adjustable Voltage Operation

The TPS7A1601-Q1 has an output voltage range from 1.194 V to 20 V. The nominal output of the device is set by two external resistors, as shown in [Figure 8-2](#):

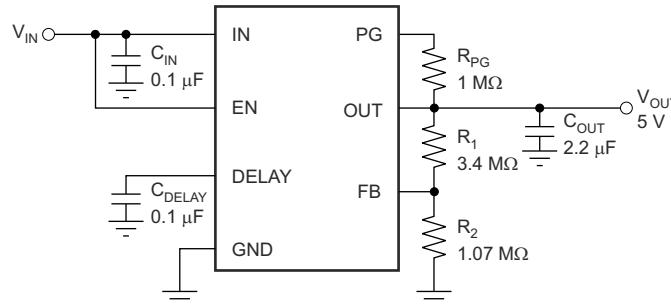


Figure 8-2. Adjustable Operation

R_1 and R_2 can be calculated for any output voltage range using the formula shown in [Equation 1](#):

$$R_1 = R_2 \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \quad (1)$$

8.2.1.2.2 Resistor Selection

Use resistors in the order of megaohms (MΩ) to keep the overall quiescent current of the system as low as possible (by making the current used by the resistor divider negligible compared to the quiescent current of the device).

If greater voltage accuracy is required, take into account the voltage offset contributions as a result of feedback current and use 0.1% tolerance resistors.

[Table 8-2](#) shows the resistor combination to achieve an output for a few of the most common rails using commercially available 0.1% tolerance resistors to maximize nominal voltage accuracy, while adhering to the formula shown in [Equation 1](#).

Table 8-2. Selected Resistor Combinations

V _{OUT}	R ₁	R ₂	V _{OUT} /(R ₁ + R ₂) « I _Q	NOMINAL ACCURACY
1.194 V	0 Ω	∞	0 μA	±2%
1.8 V	1.18 MΩ	2.32 MΩ	514 nA	±(2% + 0.14%)
2.5 V	1.5 MΩ	1.37 MΩ	871 nA	±(2% + 0.16%)
3.3 V	2 MΩ	1.13 MΩ	1056 nA	±(2% + 0.35%)
5 V	3.4 MΩ	1.07 MΩ	1115 nA	±(2% + 0.39%)
10 V	7.87 MΩ	1.07 MΩ	1115 nA	±(2% + 0.42%)
12 V	14.3 MΩ	1.58 MΩ	755 nA	±(2% + 0.18%)
15 V	42.2 MΩ	3.65 MΩ	327 nA	±(2% + 0.19%)
18 V	16.2 MΩ	1.15 MΩ	1038 nA	±(2% + 0.26%)

Close attention must be paid to board contamination when using high-value resistors; board contaminants can significantly impact voltage accuracy. If board cleaning measures cannot be ensured, consider using a fixed-voltage version of the TPS7A16 or using resistors in the order of hundreds or tens of kilohms (kΩ).

8.2.1.2.3 Capacitor Recommendations

Use low equivalent-series-resistance (ESR) capacitors for the input, output, and feed-forward capacitors. Ceramic capacitors with X7R and X5R dielectrics are preferred. These dielectrics offer more stable

characteristics. Ceramic X7R capacitors offer improved overtemperature performance, whereas ceramic X5R capacitors are the most cost-effective and are available in higher values.

However, high-ESR capacitors can degrade PSRR.

8.2.1.2.4 Input and Output Capacitor Requirements

The TPS7A16-Q1 ultra-low-power, high-voltage linear regulators achieve stability with a minimum input capacitance of 0.1 μF and output capacitance of 2.2 μF ; however, use a 10- μF ceramic capacitor to maximize ac performance.

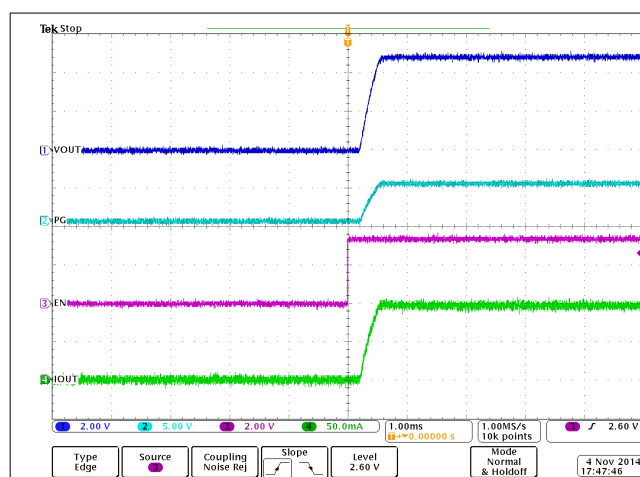
8.2.1.2.5 Feed-Forward Capacitor (Only for Adjustable Version)

Although a feed-forward capacitor (C_{FF}) from OUT to FB is not needed to achieve stability, using a 0.01- μF feed-forward capacitor to maximizes ac performance.

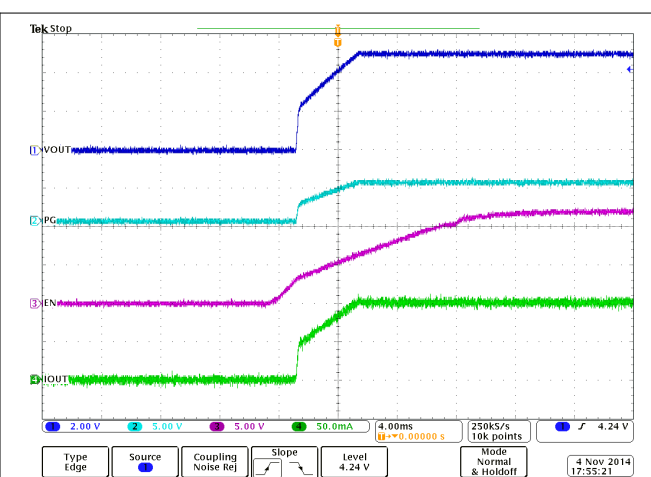
8.2.1.2.6 Transient Response

As with any regulator, increasing the size of the output capacitor reduces over- and undershoot magnitude but increases the duration of the transient response.

8.2.1.3 Application Curves



8-3. CH1 is VOUT, CH2 is PG, CH4 is Iout, VIN is 12 V and Ready Before EN



8-4. CH1 is VOUT, CH2 is PG, CH3 is EN, CH4 is Iout, VIN is 12 V Connected to EN

8.2.2 Automotive Applications

The TPS7A16-Q1 maximum input voltage of 60 V makes the device designed for use in automotive applications where high-voltage transients are present.

Events such as load-dump overvoltage (where the battery is disconnected while the alternator is providing current to a load) can cause voltage spikes from 25 V to 60 V. To prevent any damage to sensitive circuitry, local transient voltage suppressors can be used to cap voltage spikes to lower, more manageable voltages.

The TPS7A16-Q1 can be used to simplify and lower costs in such cases. The very high voltage range allows this regulator not only to withstand the voltages coming out of these local transient voltage suppressors, but even replace them, thus lowering system cost and complexity.

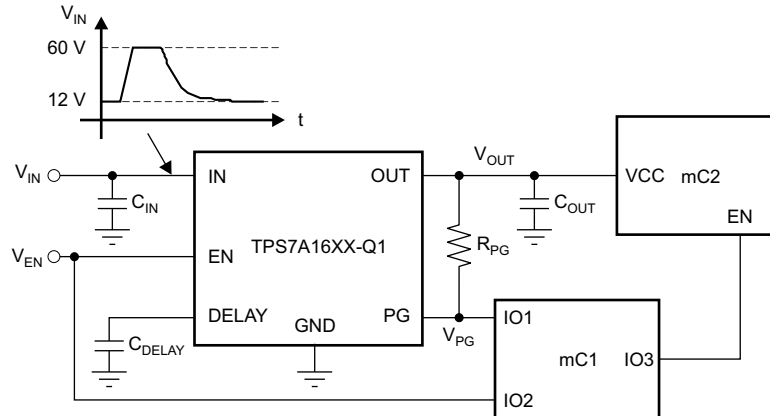


图 8-5. Low-Power Microcontroller Rail Sequencing in Automotive Applications Subjected to Load-Dump Transients

8.2.2.1 Design Requirements

表 8-3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	5.5 V to 60 V
Output voltage	5 V
Output current rating	100 mA
Output capacitor range	2.2 μ F to 100 μ F
Delay capacitor range	100 pF to 100 nF

8.2.2.2 Detailed Design Procedure

See the [Capacitor Recommendations](#) and [Input and Output Capacitor Requirements](#) sections.

8.2.2.2.1 Device Recommendations

The output is fixed, so choose the TPS7A1650-Q1.

8.2.2.3 Application Curves

See 图 8-3 and 图 8-4.

8.2.3 Multicell Battery Packs

Currently, battery packs can employ up to a dozen cells in series that, when fully charged, can have voltages of up to 55 V. Internal circuitry in these battery packs is used to prevent overcurrent and overvoltage conditions that can degrade battery life or even pose a safety risk; this internal circuitry is often managed by a low-power microcontroller, such as TI's MSP430™. See the overview for microcontrollers (MCU) for more information.

The microcontroller continuously monitors the battery, whether the battery is in use or not. Although this microcontroller can be powered by an intermediate voltage taken from the multicell array, this approach unbalances the battery pack, degrading the battery life or adding cost to implement more complex cell-balancing topologies.

The best approach to power this microcontroller is to regulate down the voltage from the entire array to discharge every cell equally and prevent any balancing issues. This approach reduces system complexity and cost.

The TPS7A16-Q1 can be used for this application because this device can handle very high voltages (from the entire multicell array) and has very low quiescent current (to maximize battery life).

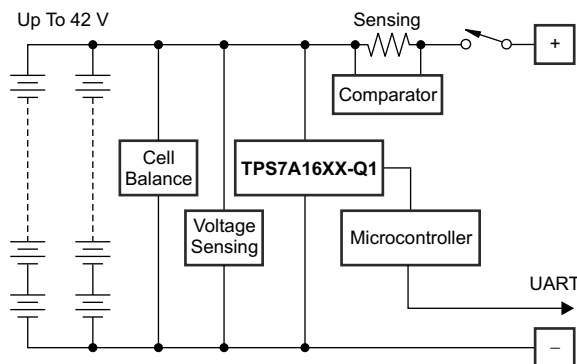


图 8-6. Protection Based on Low-Power Microcontroller Power From Multicell Battery Packs

8.2.3.1 Design Requirements

表 8-4. Device Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	5.5 V to 55 V
Output voltage	5 V
Output current rating	100 mA
Output capacitor range	2.2 μ F to 100 μ F
Delay capacitor range	100 pF to 100 nF

8.2.3.2 Detailed Design Procedure

See the [Device Recommendations](#), [Capacitor Recommendations](#), and [Input and Output Capacitor Requirements](#) sections.

8.2.3.3 Application Curves

See 图 8-3 and 图 8-4.

8.2.4 Battery-Operated Power Tools

High-voltage multicell battery packs support high-power applications (such as power tools) with high current drain when in use, highly intermittent use cycles, and physical separation between battery and motor.

In these applications, a microcontroller or microprocessor controls the motor. This microcontroller must be powered with a low-voltage rail coming from the high-voltage, multicell battery pack; as mentioned previously, powering this microcontroller or microprocessor from an intermediate voltage from the multicell array causes battery-pack life degradation or added system complexity because of cell balancing issues. In addition, this microcontroller or microprocessor must be protected from the high-voltage transients because of the motor inductance.

The TPS7A16-Q1 can be used to power the motor-controlled microcontroller or microprocessor; the device low quiescent current maximizes battery shelf life, and very high-voltage capabilities simplify system complexity by replacing voltage suppression filters, thus lowering system cost.

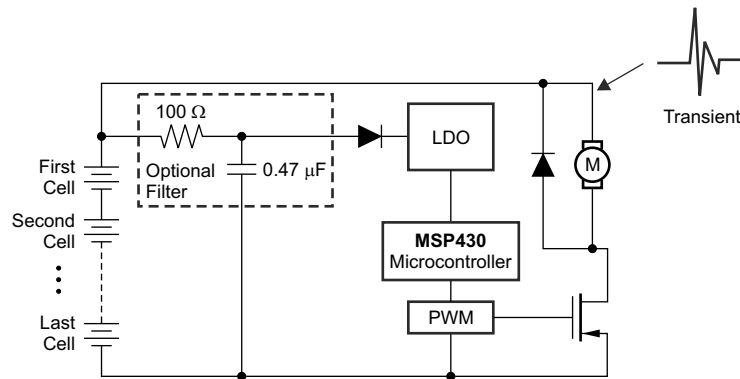


图 8-7. Low Power Microcontroller Power From Multicell Battery Packs in Power Tools

8.2.4.1 Design Requirements

表 8-5. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	5.5 V to 60 V
Output voltage	5 V
Output current rating	100 mA
Output capacitor range	2.2 μ F to 100 μ F
Delay capacitor range	100 pF to 100 nF

8.2.4.2 Detailed Design Procedure

See the [Device Recommendations](#), [Capacitor Recommendations](#), and [Input and Output Capacitor Requirements](#) sections.

8.2.4.3 Application Curves

See 图 8-3 and 图 8-4.

8.3 Power Supply Recommendations

Design of the device is for operation from an input voltage supply with a range between 3 V and 60 V. This input supply must be well regulated. The TPS7A16-Q1 ultra-low-power, high-voltage linear regulator achieves stability with a minimum input capacitance of 0.1 μ F and output capacitance of 2.2 μ F; however, the use of a 10- μ F ceramic capacitor to maximize ac performance is highly recommended.

8.4 Layout

8.4.1 Layout Guidelines

To improve ac performance such as PSRR, output noise, and transient response, design the board with separate ground planes for IN and OUT, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor must connect directly to the GND pin of the device.

Equivalent series inductance (ESL) and ESR must be minimized in order to maximize performance and provide stability. Every capacitor must be placed as close as possible to the device and on the same side of the PCB as the regulator.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. Using vias and long traces is strongly discouraged because these components can impact system performance negatively and even cause instability.

If possible, and to provide the maximum performance denoted in this product data sheet, use the same layout pattern used for the TPS7A16-Q1 evaluation board, available at www.ti.com.

Layout is a critical part of good power-supply design. There are several signal paths that conduct fast-changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power-supply performance. To help eliminate these problems, bypass the IN pin to ground with a low-ESR ceramic bypass capacitor with X5R or X7R dielectric.

Acceptable performance can possibly be obtained with alternative PCB layouts; however, the layout and schematic herein have been shown to produce good results and are meant as a guideline.

☒ 8-8 shows the schematic for the suggested layout. ☒ 8-9 and ☒ 8-10 show the top and bottom printed circuit board (PCB) layers for the suggested layout.

8.4.1.1 Additional Layout Considerations

The high impedance of the FB pin makes the regulator sensitive to parasitic capacitances that can couple undesirable signals from nearby components (especially from logic and digital devices, such as microcontrollers and microprocessors); these capacitively-coupled signals can produce undesirable output voltage transients. In these cases, use a fixed-voltage version of the TPS7A16-Q1, or isolate the FB node by flooding the local PCB area with ground-plane copper to minimize any undesirable signal coupling.

8.4.1.2 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Using heavier copper increases the effectiveness of removing heat from the device. The addition of plated through-holes to heat dissipating layers also improves the heat sink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current times the voltage drop across the output pass element, as shown in 式 2:

$$P_D = (V_{IN} - V_{OUT}) I_{OUT} \quad (2)$$

8.4.1.3 Thermal Considerations

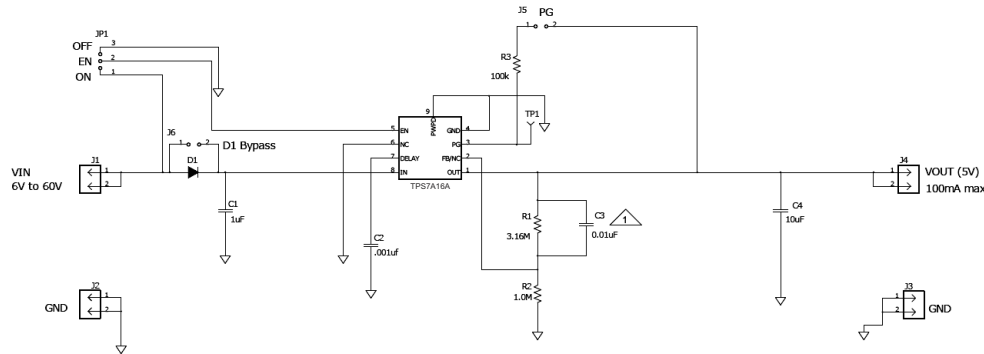
Thermal protection disables the output when the junction temperature rises to approximately 170°C, allowing the device to cool. When the junction temperature cools to approximately 150°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle on and off. This cycling limits the dissipation of the regulator, protecting the regulator from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat-spreading area. For reliable operation, limit junction temperature to a maximum of 125°C at the worst-case ambient temperature for a given application. To estimate the margin of safety in a complete design (including the copper heat-spreading area), increase the ambient temperature until the thermal protection is triggered; use

worst-case loads and signal conditions. For good reliability, thermal protection must trigger at least 45°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

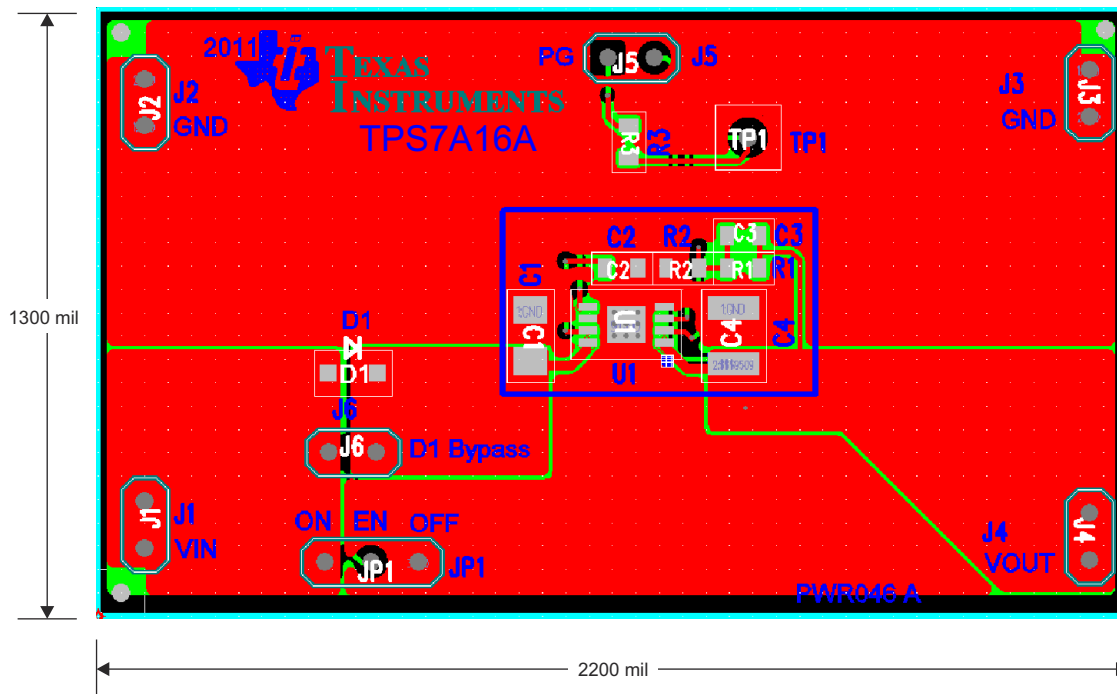
The internal protection circuitry of the TPS7A16-Q1 is designed to protect against overload conditions. This circuitry is not intended to replace proper heat sinking. Continuously running the TPS7A16-Q1 into thermal shutdown degrades device reliability.

8.4.2 Layout Examples

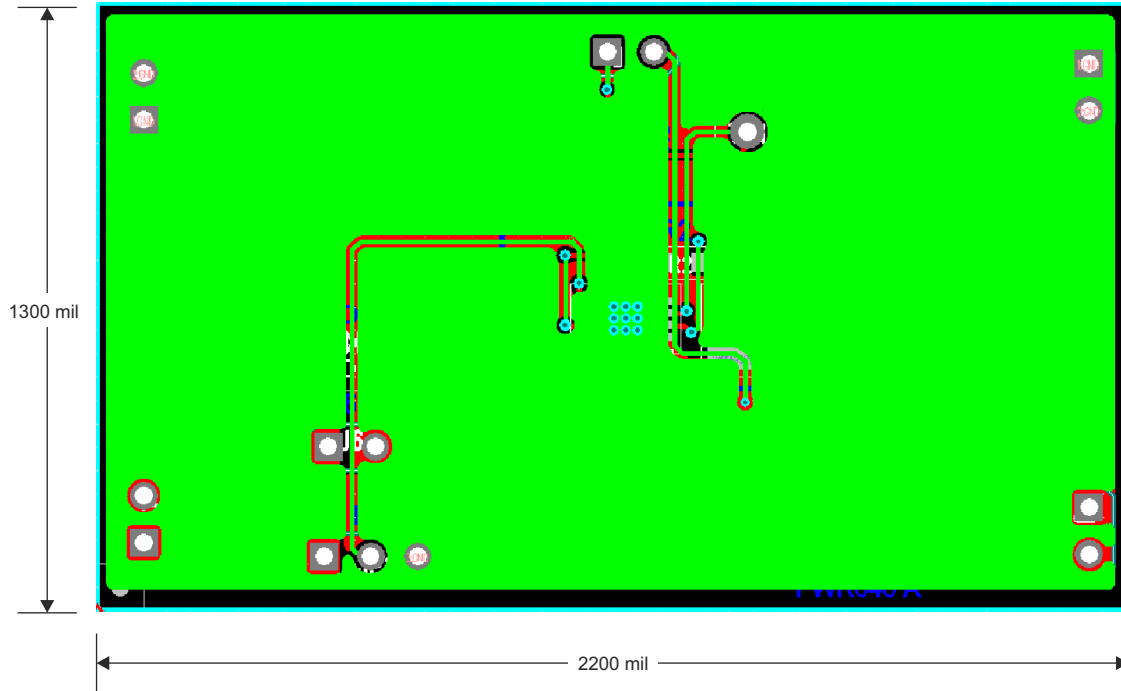


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8-8. Schematic for Suggested Layout



8-9. Suggested Layout: Top Layer



8-10. Suggested Layout: Bottom Layer

9 Device and Documentation Support

9.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

9.2 サポート・リソース

[TI E2E™ サポート・フォーラム](#)は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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9.4 静電気放電に関する注意事項



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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.5 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A1601QDGNRQ1	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PXZQ	Samples
TPS7A1633QDGNRQ1	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PXYQ	Samples
TPS7A1650QDGNRQ1	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PYAQ	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS7A16-Q1 :

- Catalog : [TPS7A16](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A1601QDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS7A1633QDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS7A1650QDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A1601QDGNRQ1	HVSSOP	DGN	8	2500	367.0	367.0	38.0
TPS7A1633QDGNRQ1	HVSSOP	DGN	8	2500	367.0	367.0	38.0
TPS7A1650QDGNRQ1	HVSSOP	DGN	8	2500	367.0	367.0	38.0

GENERIC PACKAGE VIEW

DGN 8

PowerPAD VSSOP - 1.1 mm max height

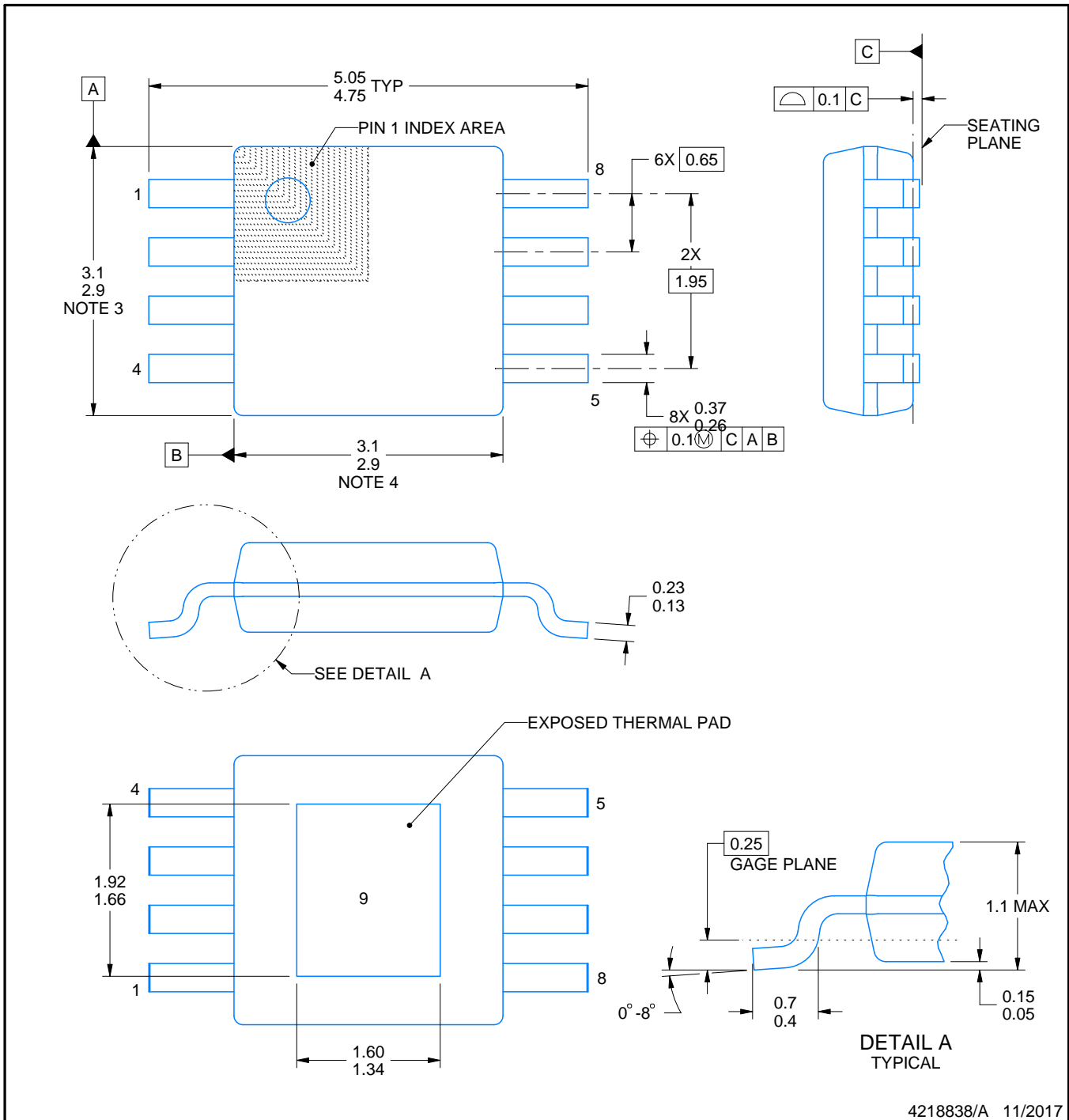
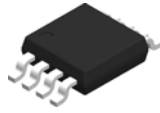
3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/A



4218838/A 11/2017

NOTES:

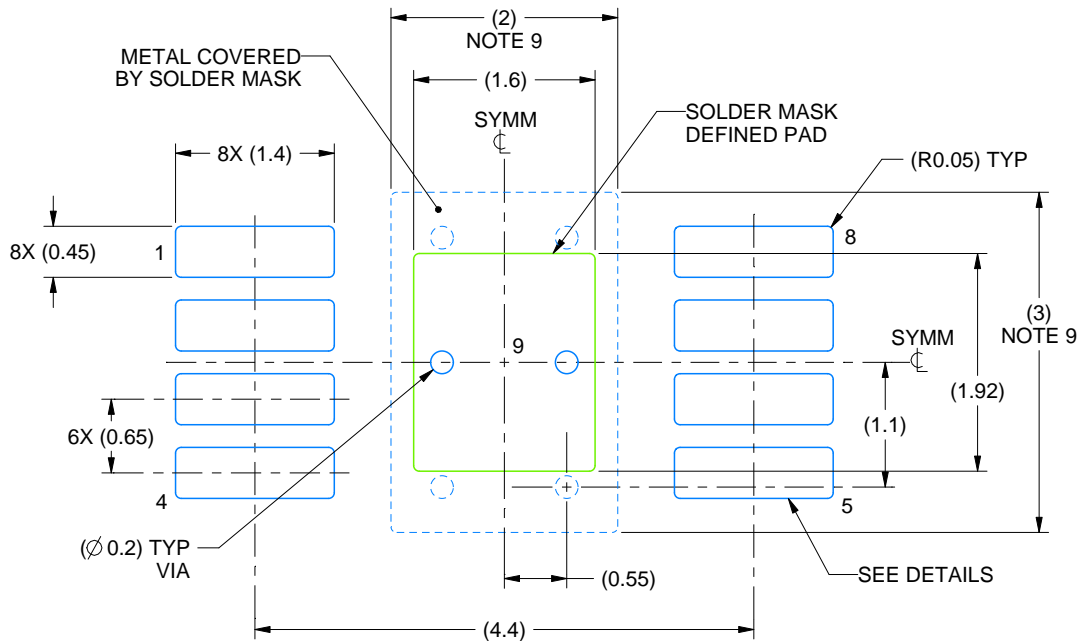
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

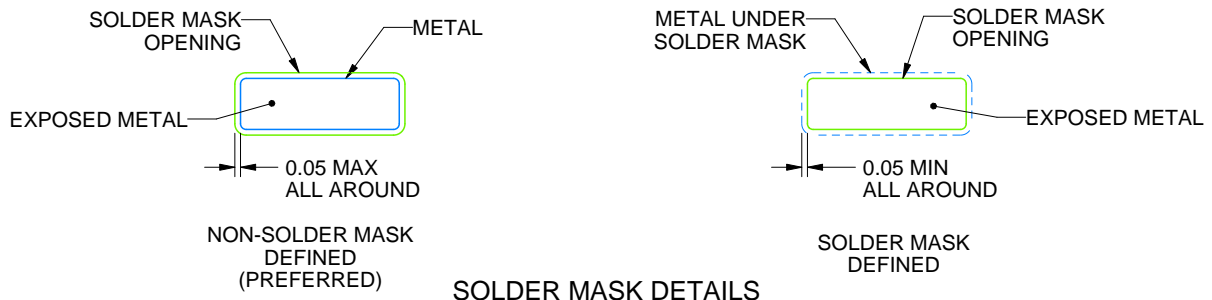
DGN0008C

HVSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



4218838/A 11/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGN0008C

HVSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



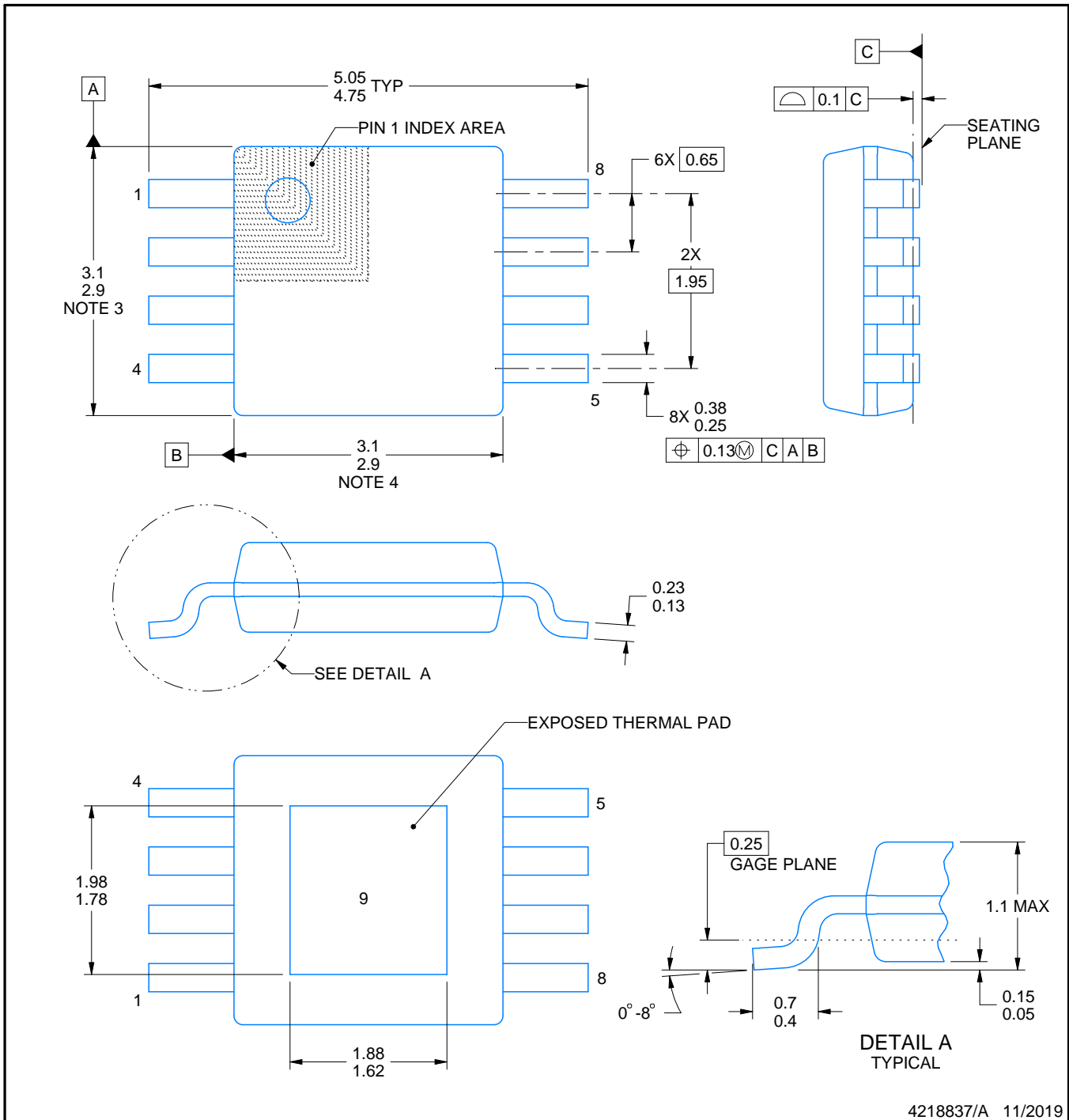
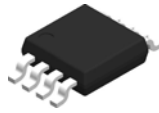
SOLDER PASTE EXAMPLE
 EXPOSED PAD 9:
 100% PRINTED SOLDER COVERAGE BY AREA
 SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.79 X 2.15
0.125	1.60 X 1.92 (SHOWN)
0.15	1.46 X 1.75
0.175	1.35 X 1.62

4218838/A 11/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.



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NOTES:

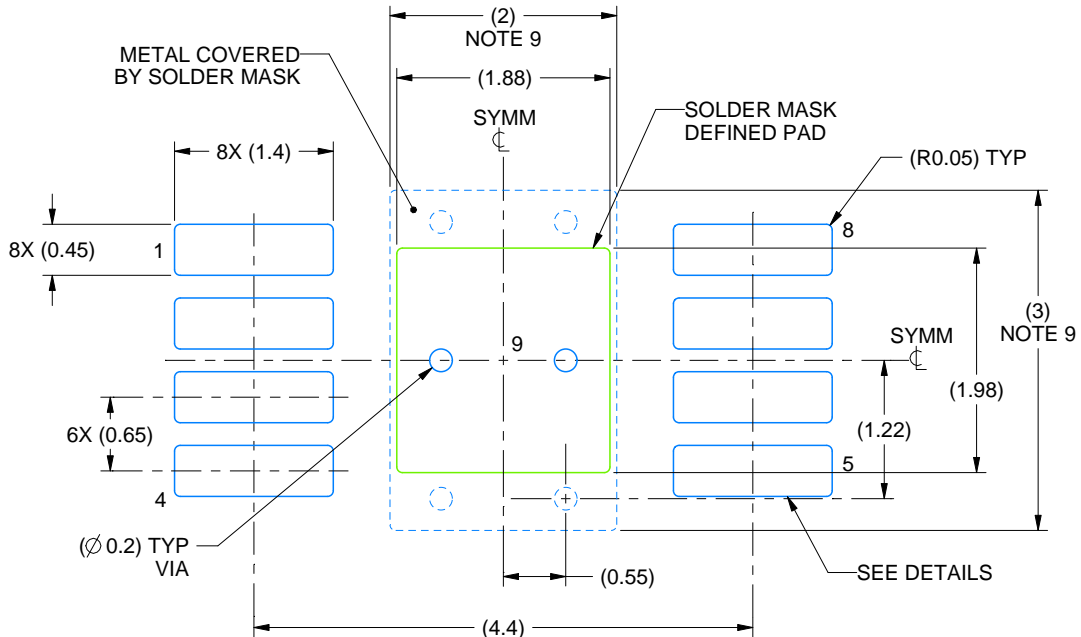
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

DGN0008B

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



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NOTES: (continued)

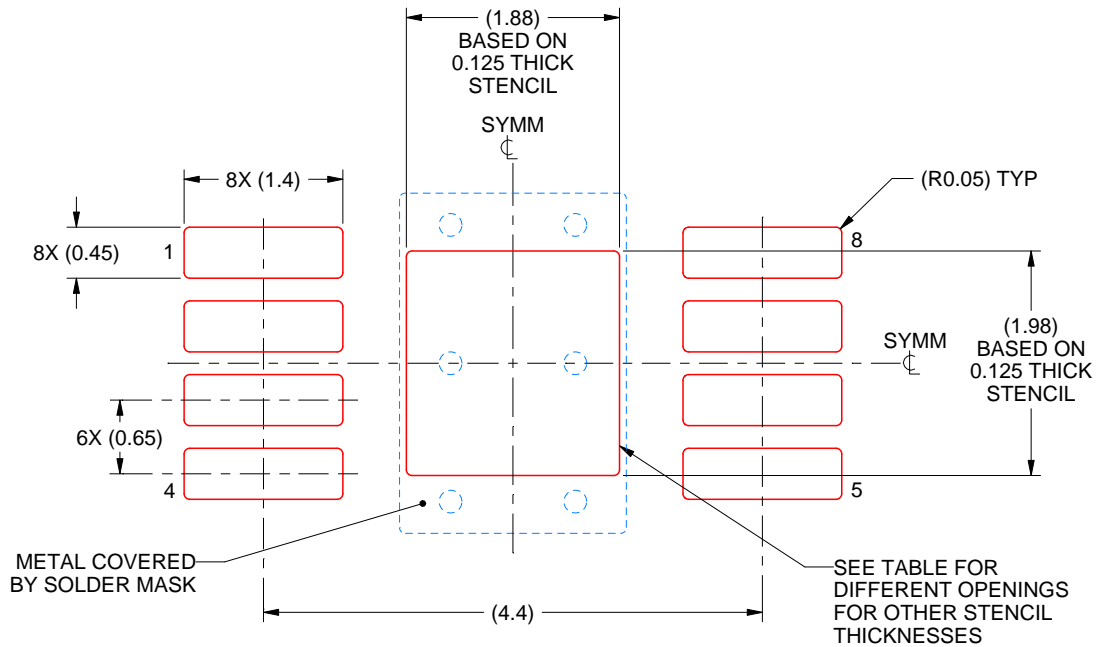
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
- 8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
- 9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGN0008B

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.10 X 2.21
0.125	1.88 X 1.98 (SHOWN)
0.15	1.72 X 1.81
0.175	1.59 X 1.67

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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