Ordering & quality
Technical documentation
Design & development
Support & training

参考資料

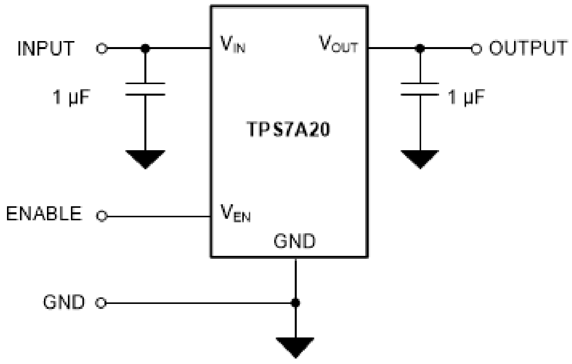
TPS7A20 300mA、超低ノイズ、低 I_Q、高 PSRR LDO

1 特長

- 低い出力電圧ノイズ:$7\mu V_{RMS}$
  - ノイズ・バイパス・コンデンサが不要
- 高い PSRR:1kHz 時に 95dB
- 超低 I_Q:6.5μA
- 入力電圧範囲:1.6V～6.0V
- 出力電圧範囲:0.8V～5.5V
- 出力電圧許容誤差:±1.5% (最大値)
- 非常に低いドロップアウト:
  - 300mA で 140mV 以下 (V_{OUT} = 3.3V)
  - 300mA で 145mV 以下 (V_{OUT} = 3.3V、DBV)
- 小さい突入電流
- スマート・イネーブルのプルダウン
- 最小 1μF のセラミック出力コンデンサで安定に動作
- パッケージ:
  - 1mm × 1mm の X2SON
  - 0.616mm × 0.616mm の DSBGA
  - 2.90mm × 1.60mm の SOT23-5

2 アプリケーション

- スマートフォンとタブレット
- IP ネットワーク・カメラ
- 携帯医療機器
- スマート・メータとフィールド・トランスミッタ
- モータ・ドライブ
- ウェアラブル



概略回路図

3 概要

TPS7A20 は、300mA の出力電流を供給できる超小型の低ドロップアウト (LDO) リニア・レギュレータです。TPS7A20 は、RF やその他の敏感なアナログ回路の要件を満たすため、低ノイズ、高 PSRR、および非常に優れた負荷およびライン過渡性能を実現できるよう設計されています。革新的な設計手法を採用した TPS7A20 は、ノイズ・バイパス・コンデンサを追加しなくても超低ノイズ性能を発揮します。TPS7A20 は、静止電流が小さいという利点も備えているため、バッテリ駆動のアプリケーションに理想的です。1.6V～6.0V の入力電圧範囲と 0.8V～5.5V の出力電圧範囲を持つ TPS7A20 は幅広いアプリケーションに使用できます。本デバイスは、負荷、ライン、温度の変化に対して誤差 1.5% 以下の精度を達成するために高精度の基準電圧回路を使用しています。

TPS7A20 は、突入電流を低減させるための内部ソフトスタートを備えているため、起動時の入力電圧降下を最小限に抑えることができます。このデバイスは小さなセラミック・コンデンサでも安定に動作するため、ソリューション全体を小型化できます。

TPS7A20 は、内部的に制御されるプルダウン抵抗を持つスマート・イネーブル入力回路を備えています。EN ピンをフローティング状態のままにしていても、このプルダウン抵抗が LDO をディセーブル状態に維持するため、EN ピンをプルダウンするために使用する外付け部品は不要です。

製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
TPS7A20	X2SON (4)	1.00mm × 1.00mm
	DSBGA (4)	0.616mm × 0.616mm
	SOT-23 (5)	2.90mm × 1.60mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

English Data Sheet: SBVS338

Table of Contents

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision F (April 2022) to Revision G (May 2022)	Page
• Changed UVLO condition from rising to falling for YCJ and YCK packages	6

Changes from Revision E (December 2021) to Revision F (April 2022)	Page
• 「特長」および「概要」セクションで DSBGA の寸法を 0.603mm × 0.603mm から 0.616mm × 0.616mm に変更	1

5 Pin Configuration and Functions

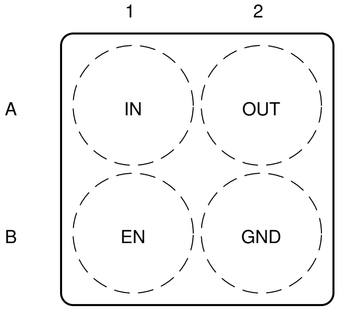


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図 5-1. YCJ and YCK Packages, 4-Pin DSBGA (Top View)

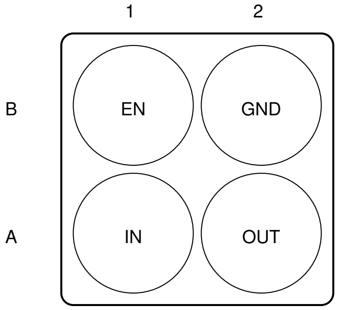

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図 5-2. YCJ and YCK Packages, 4-Pin DSBGA (Bottom View)

Pin Functions: DSBGA

PIN		I/O	DESCRIPTION
NO.	NAME		
A1	IN	I	Input voltage supply. For best transient response and to minimize input impedance, use the nominal value or larger capacitor from IN to ground as listed in the *Recommended Operating Conditions* table. Place the input capacitor as close to the IN and GND pins of the device as possible.
A2	OUT	O	Regulated output voltage. A low equivalent series resistance (ESR) capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger capacitor listed in the *Recommended Operating Conditions* table. Place the output capacitor as close to the OUT and GND pins of the device as possible. An internal 150-Ω (typical) pulldown resistor prevents a charge from remaining on V_{OUT} when the regulator is in shutdown mode ($V_{EN} < V_{EN(LOW)}$).
B1	EN	I	Enable input. A low voltage (< $V_{EN(LOW)}$) on this input turns the regulator off and discharges the output pin to GND. A high voltage (> $V_{EN(HI)}$) on this pin enables the regulator output. This pin has an internal 500-kΩ pulldown resistor to hold the regulator off by default. When $V_{EN} > V_{EN(HI)}$, the 500-kΩ pulldown is disconnected to reduce input current.
B2	GND	—	Common ground.

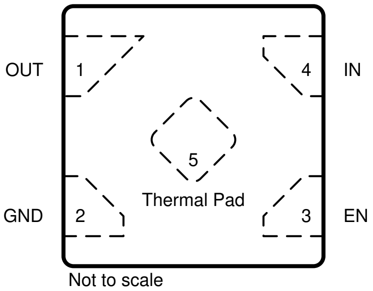


図 5-3. DQN Package, 4-Pin X2SON (Top View)

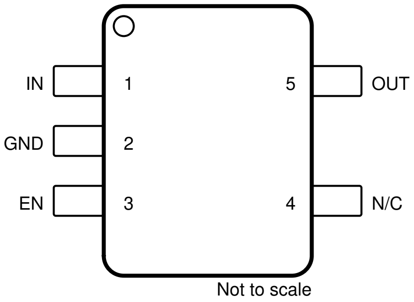


図 5-4. DBV Package, 5-Pin SOT-23 (Top View)

Pin Functions: X2SON, SOT-23

PIN			I/O	DESCRIPTION
NAME	X2SON	SOT-23		
IN	4	1	I	Input voltage supply. For best transient response and to minimize input impedance, use the nominal value or larger capacitor from IN to ground as listed in the *Recommended Operating Conditions* table. Place the input capacitor as close to the IN and GND pins of the device as possible.
OUT	1	5	O	Regulated output voltage. A low equivalent series resistance (ESR) capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger capacitor listed in the *Recommended Operating Conditions* table. Place the output capacitor as close to the OUT and GND pins of the device as possible. An internal 150-Ω (typical) pulldown resistor prevents a charge from remaining on V_{OUT} when the regulator is in shutdown mode ($V_{EN}< V_{EN(LOW)}$).
EN	3	3	I	Enable input. A low voltage (< $V_{EN(LOW)}$) on this pin turns the regulator off and discharges the output pin to GND. A high voltage (> $V_{EN(HI)}$) on this pin enables the regulator output. This pin has an internal 500-kΩ pulldown resistor to hold the regulator off by default. When V_{EN} > $V_{EN(HI)}$, the 500-kΩ pulldown is disconnected to reduce input current.
GND	2	2	—	Common ground.
N/C	—	4	—	No internal electrical connection.
Thermal Pad	5	—	—	Thermal pad for the X2SON package. Connect this pad to GND or leave floating. Do not connect to any potential other than GND. Connect the thermal pad to a large-area ground plane for best thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (3)

		MIN	MAX	UNIT
Voltage	V_{IN}	–0.3	6.5	V
	V_{OUT}	–0.3	6.5 or V_{IN} + 0.3 (2)	
	V_{EN}	–0.3	6.5	
Current	Maximum output(4)	Internally limited		A
Temperature	Operating junction, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The maximum value of V_{OUT} is the lesser of 6.5 V or (V_{IN} + 0.3 V).
(3) All voltages are with respect to the GND pin.
(4) Internal thermal shutdown circuitry protects the device from permanent damage.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safemanufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safemanufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	1.6		6.0	V
V_{EN}	Enable input voltage	0		6.0	V
V_{OUT}	Nominal output voltage range	0.8		5.5	V
I_{OUT}	Output current	0		300	mA
C_{IN}	Input capacitor(2)		1		µF
C_{OUT}	Output capacitor(3)	1		200	µF
ESR	Output capacitor effective series resistance			100	mΩ
T_J	Operating junction temperature	–40		125	°C

(1) All voltages are with respect to GND.
(2) An input capacitor is not required for LDO stability. However, an input capacitor with an effective value of 0.47 µF minimum is recommended to counteract the effect of source resistance and inductance, which may in some cases cause symptoms of system-level instability such as ringing or oscillation, especially in the presence of load transients.
(3) Effective output capacitance of 0.47 µF minimum and 200 µF maximum is required for stability.

6.4 Thermal Information

THERMAL METRIC[1]		TPS7A20				UNIT
		DBV (SOT-23)	DQN (X2SON)	YCJ (DSBGA)	YCK (DSBGA)	
		5 PINS	4 PINS	4 PINS	4 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	187.1	166.1	199.6	201.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	85.5	103.6	2.8	2.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.4	110.6	67.5	69.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	27.1	3.0	1.4	1.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	54.1	103.3	67.4	69.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	98.8	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at operating temperature range (T_J = –40℃ to +125℃), $V_{IN} = V_{OUT(NOM)}$ + 0.3 V or 1.6V, whichever is greater, V_{EN} = 1.0 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF (unless otherwise noted); all typical values are at T_J = 25℃

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ΔV_{OUT}	Output voltage tolerance	V_{IN} = ($V_{OUT(NOM)}$ + 0.3 V) to 6.0 V, I_{OUT} = 1 mA to 300 mA, $V_{OUT} \geq$ 1.85 V (DQN, YCJ, YCK packages)		–1.5		1.5	%
		V_{IN} = ($V_{OUT(NOM)}$ + 0.3 V) to 6.0 V, I_{OUT} = 1 mA to 300 mA, $V_{OUT} \geq$ 2.8 V (DBV package)		-1.5		1.5	
		V_{IN} = ($V_{OUT(NOM)}$ + 0.5 V) to 6.0 V, I_{OUT} = 1 mA to 300 mA V_{OUT} < 1.85 V (DQN, YCJ, YCK packages)		–30		30	mV
		V_{IN} = ($V_{OUT(NOM)}$ + 0.3 V) to 6.0 V, I_{OUT} = 1 mA to 300 mA, V_{OUT} < 2.8 V (DBV package)		-40		40	
ΔV_{OUT}	Line regulation	V_{IN} = ($V_{OUT(NOM)}$ + 0.3 V) to 6.0 V, I_{OUT} = 1 mA			0.03		%/V
ΔV_{OUT}	Load regulation	I_{OUT} = 1 mA to 300 mA (DQN, YCJ, YCK packages)			13		mV
		I_{OUT} = 1 mA to 300 mA (DBV package)			19		
I_{GND}	Quiescent ground current	$V_{EN} = V_{IN}$ = 6 V, I_{OUT} = 0 mA	T_J = 25°C		6.5	8.5	µA
			T_J = –40°C to 85°C			10	
			T_J = –40°C to 125°C			15	
		$V_{EN} = V_{IN}$ = 6 V, I_{OUT} = 300 mA			2000		
I_{SHDN}	Shutdown ground current	V_{EN} = 0 V (disabled), V_{IN} = 6.0 V, T_J = 25°C			0.07	0.2	µA
$I_{GND(DO)}$	I_{GND} in dropout	$V_{IN} \leq V_{OUT(NOM)}$, I_{OUT} = 0 mA, $V_{EN} = V_{IN}$			6.5	15	µA
V_{DO}	Dropout voltage	I_{OUT} = 300 mA, V_{OUT} = 95% x $V_{OUT(NOM)}$, (DQN, YCJ, YCK packages unless otherwise noted)	0.8 V ≤ V_{OUT} < 1.0 V[1]			690	mV
			1.0 V ≤ V_{OUT} < 1.2 V[1]			490	
			1.2 V ≤ V_{OUT} < 1.5 V[1]			355	
			1.5 V ≤ V_{OUT} < 2.5 V			200	
			1.5 V ≤ V_{OUT} < 2.5 V (DBV)			205	
			2.5 V ≤ V_{OUT} < 5.5 V			140	
			2.5 V ≤ V_{OUT} < 5.5 V (DBV)			145	

6.5 Electrical Characteristics (continued)

at operating temperature range (T_J = –40℃ to +125℃), V_{IN} = $V_{OUT(NOM)}$ + 0.3 V or 1.6V, whichever is greater, V_{EN} = 1.0 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF (unless otherwise noted); all typical values are at T_J = 25℃

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CL}	Output current limit	V_{OUT} = 0.9 x $V_{OUT(NOM)}$, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V	V_{OUT} < 1.5 V (YCJ, YCK packages)	360	520	770	mA
		V_{OUT} = 0.9 x $V_{OUT(NOM)}$, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V	V_{OUT} < 1.5 V (DQN package)	360	520	730	
		V_{OUT} = $V_{OUT(NOM)}$ - 150 mV, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V	V_{OUT} < 1.5 V (DBV package)	360	520	730	
		V_{OUT} = 0.9 x $V_{OUT(NOM)}$, V_{IN} = $V_{OUT(NOM)}$ + 0.3 V	V_{OUT} ≥ 1.5 V (YCJ, YCK packages)	360	520	770	
		V_{OUT} = 0.9 x $V_{OUT(NOM)}$, V_{IN} = $V_{OUT(NOM)}$ + 0.3 V	V_{OUT} ≥ 1.5 V (DQN package)	360	520	730	
I_{SC}	Short-circuit current limit	V_{OUT} = 0 V			160		mA
PSRR	Power-supply rejection ratio	I_{OUT} = 20 mA, V_{IN} = V_{OUT} + 1.0 V	f = 100 Hz		95		dB
			f = 1 kHz		95		
			f = 10 kHz		75		
			f = 100 kHz		75		
			f = 1 MHz		45		
		I_{OUT} = 300 mA, V_{IN} = V_{OUT} + 1.0 V	f = 100 Hz		65		
			f = 1 kHz		92		
			f = 10 kHz		75		
			f = 100 kHz		60		
			f = 1 MHz		40		
V_N	Output noise voltage	BW = 10 Hz to 100 kHz, V_{OUT} = 2.8 V	I_{OUT} = 300 mA		7		μV_{RMS}
			I_{OUT} = 1 mA		10		
$R_{PULLDOWN}$	Output automatic discharge pulldown resistance	V_{EN} < $V_{EN(LOW)}$ (output disabled), V_{IN} = 3.1 V			150		Ω
T_{SD}	Thermal shutdown	T_J rising			165		°C
		T_J falling			140		
$V_{EN(LOW)}$	Low input threshold	V_{IN} = 1.6 V to 6.0 V, V_{EN} falling until the output is disabled				0.3	V
$V_{EN(HI)}$	High input threshold	V_{IN} = 1.6 V to 6.0 V V_{EN} rising until the output is enabled		0.9			V
V_{UVLO}	UVLO threshold	V_{IN} rising (YCJ and YCK packages)		1.11	1.35	1.59	V
		V_{IN} rising (DBV and DQN packages)		1.17	1.35	1.59	
		V_{IN} falling (YCJ and YCK packages)		1.05	1.3	1.55	
		V_{IN} falling (DBV and DQN packages)		1.11	1.3	1.55	
$V_{UVLO(HYST)}$	UVLO hysteresis				50		mV
I_{EN}	EN input leakage current	V_{EN} = 6.0 V and V_{IN} = 6.0 V			90	250	nA
$R_{EN(PULL-DOWN)}$	Smart enable pulldown resistor	V_{EN} = 0.25 V			500		KΩ

(1) Design simulation data only

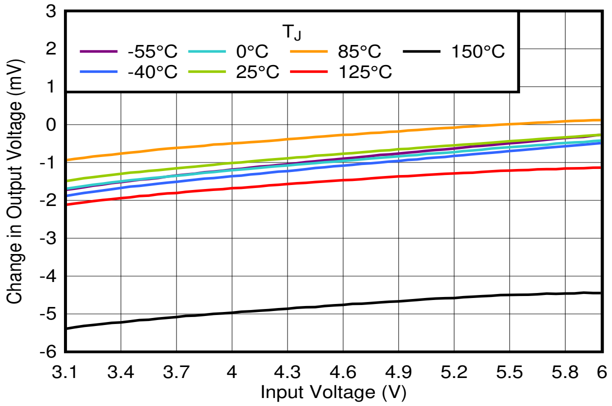
6.6 Switching Characteristics

at operating temperature range (T_J = –40℃ to +125℃), V_{IN} = $V_{OUT(NOM)}$ + 0.3 V or 1.6V, whichever is greater, V_{EN} = 1.0 V, I_{OUT} = 1 mA, C_{IN}= 1 µF, C_{OUT} = 1 µF (unless otherwise noted); all typical values are at T_J = 25℃

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{STR}	Start-up time	From V_{EN} > $V_{EN(HI)}$ to V_{OUT} = 95% of $V_{OUT(NOM)}$,		750	1150	µs

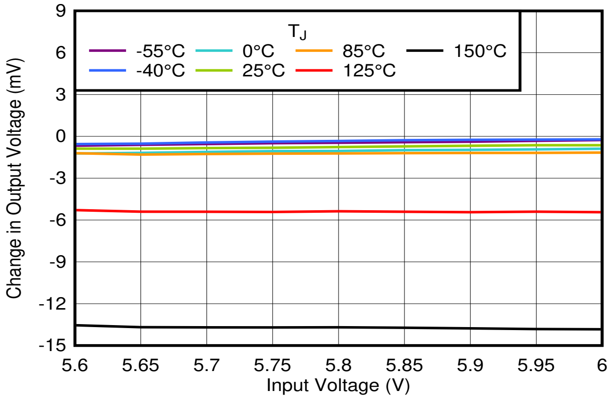
6.7 Typical Characteristics

V_{IN} = $V_{OUT(NOM)}$ + 0.3 V or 1.6 V (whichever is greater), V_{OUT} = 2.8 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, and T_A = 25°C (unless otherwise noted)



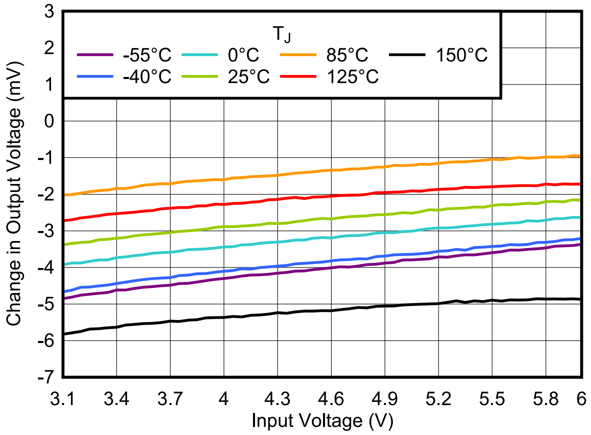
V_{EN} = 1 V, DQN, YCJ, and YCK packages

図 6-1. Line Regulation vs V_{IN}



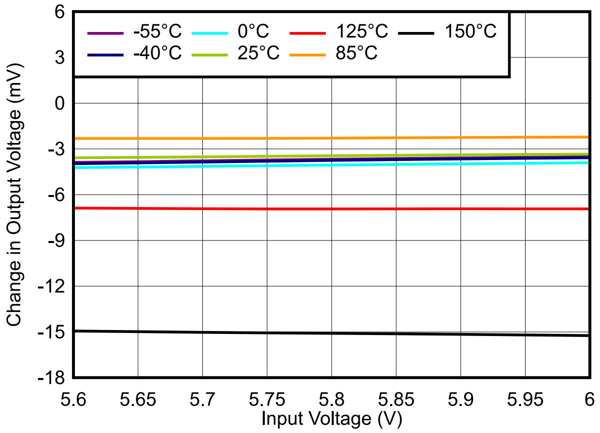
V_{OUT} = 5.5 V, V_{EN} = 1 V, DQN, YCJ, and YCK packages

図 6-2. Line Regulation vs V_{IN}



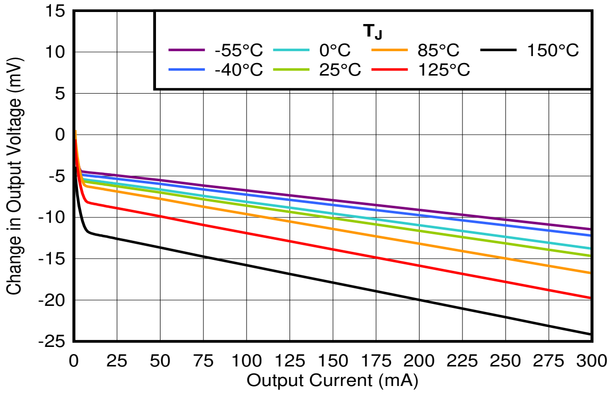
V_{EN} = 1 V, DBV package

図 6-3. Line Regulation vs V_{IN}



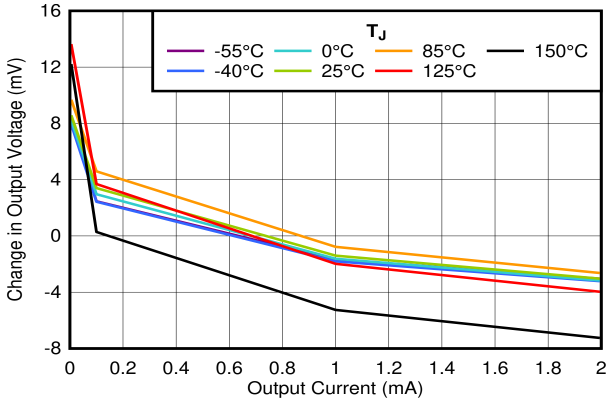
V_{OUT} = 5.5 V, V_{EN} = 1 V, DBV package

図 6-4. Line Regulation vs V_{IN}



V_{IN} = 3.1 V, V_{EN} = 1 V, DQN, YCJ, and YCK packages

図 6-5. Load Regulation vs I_{OUT}

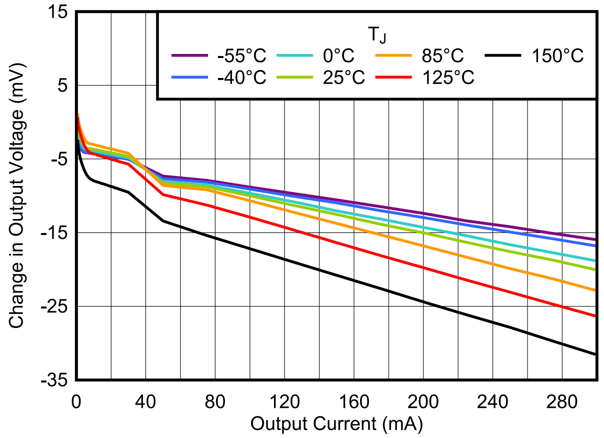


V_{IN} = 3.1 V, V_{EN} = 1 V, DQN, YCJ, and YCK packages

図 6-6. Load Regulation vs I_{OUT}

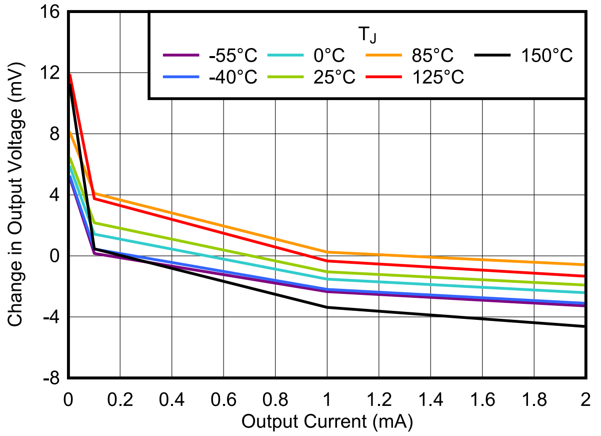
6.7 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.3 V or 1.6 V (whichever is greater), V_{OUT} = 2.8 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, and T_A = 25°C (unless otherwise noted)



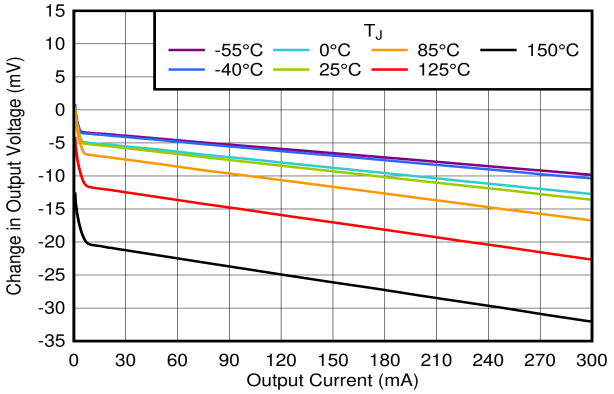
V_{IN} = 2.8 V, V_{EN} = 1 V, DBV package

図 6-7. Load Regulation vs I_{OUT}



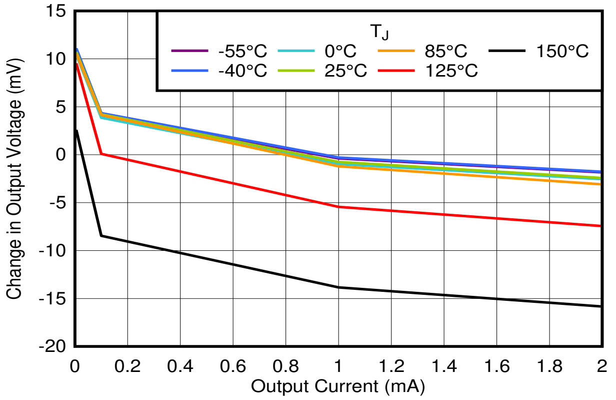
V_{IN} = 2.8 V, V_{EN} = 1 V, DBV package

図 6-8. Load Regulation vs I_{OUT}



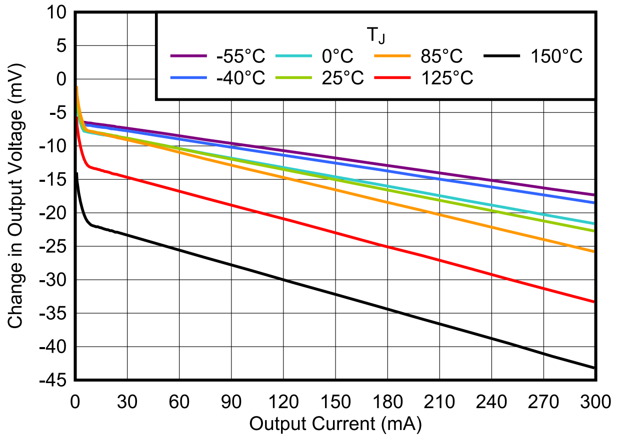
V_{OUT} = 5.5 V, V_{EN} = 1 V, DQN, YCJ, and YCK packages

図 6-9. Load Regulation vs I_{OUT}



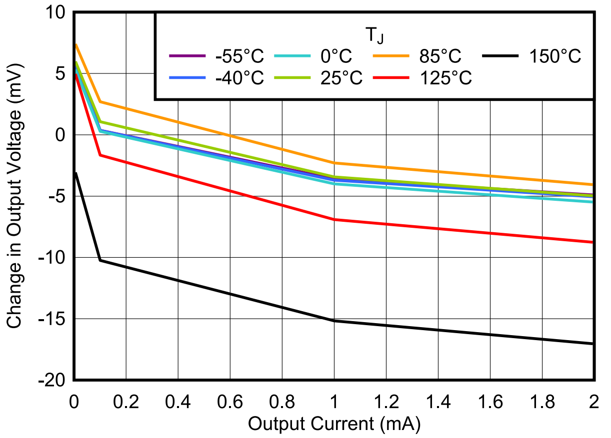
V_{OUT} = 5.5 V, V_{EN} = 1 V, DQN, YCJ, and YCK packages

図 6-10. Load Regulation vs I_{OUT}



V_{OUT} = 5.5 V, V_{EN} = 1 V, DBV package

図 6-11. Load Regulation vs I_{OUT}

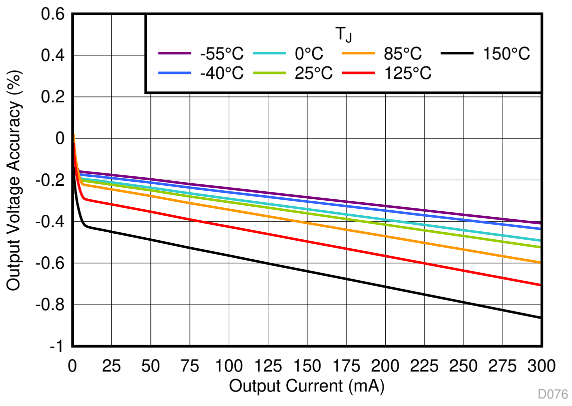


V_{OUT} = 5.5 V, V_{EN} = 1 V, DBV package

図 6-12. Load Regulation vs I_{OUT}

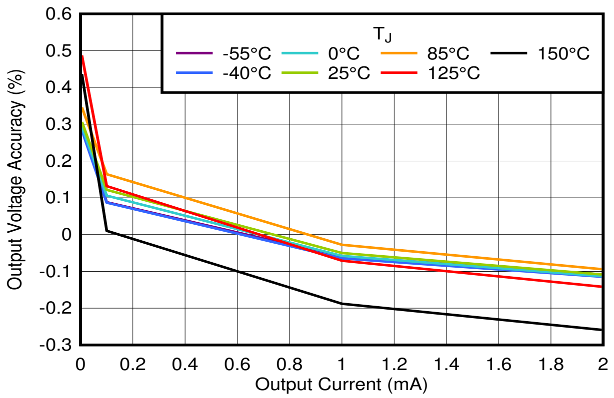
6.7 Typical Characteristics (continued)

$V_{IN} = V_{OUT(NOM)} + 0.3$ V or 1.6 V (whichever is greater), $V_{OUT} = 2.8$ V, $I_{OUT} = 1$ mA, $C_{IN} = 1$ µF, $C_{OUT} = 1$ µF, and $T_A = 25$°C (unless otherwise noted)



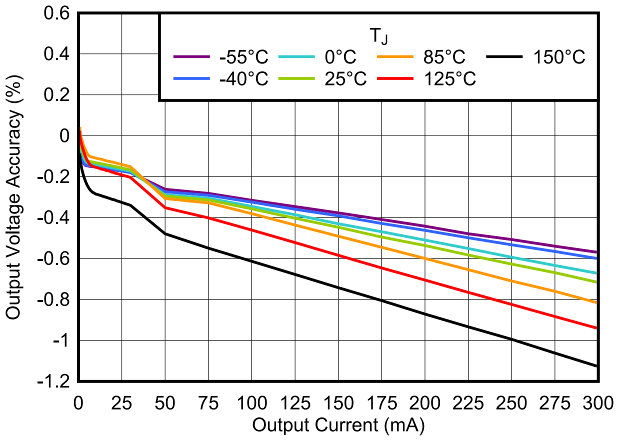
$V_{EN} = 1$ V, DQN, YCJ, and YCK packages

図 6-13. Output Voltage Accuracy vs I_{OUT}



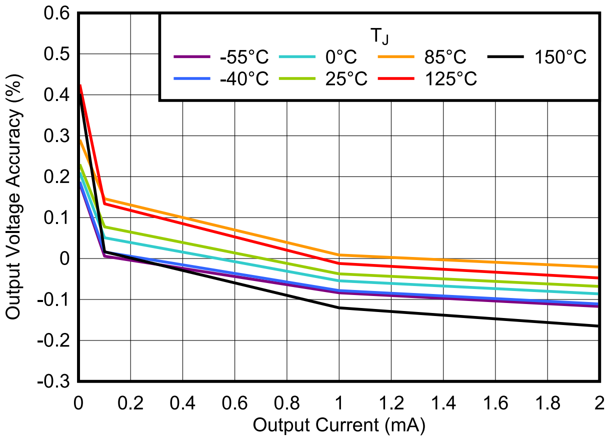
$V_{EN} = 1$ V, DQN, YCJ, and YCK packages

図 6-14. Output Voltage Accuracy vs I_{OUT}



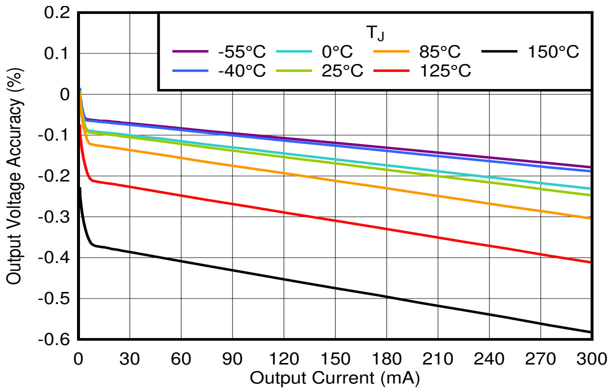
$V_{EN} = 1$ V, DBV package

図 6-15. Output Voltage Accuracy vs I_{OUT}



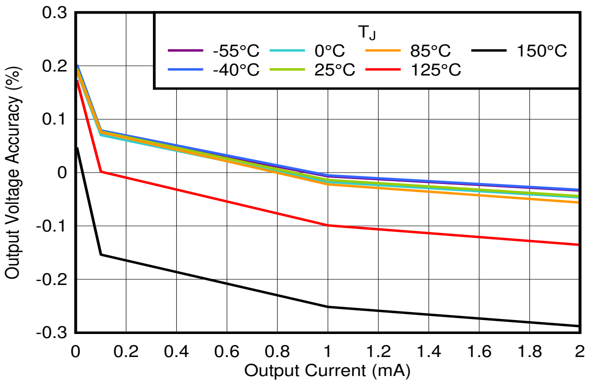
$V_{EN} = 1$ V, DBV package

図 6-16. Output Voltage Accuracy vs I_{OUT}



$V_{OUT} = 5.5$ V, $V_{EN} = 1$ V, DQN, YCJ, and YCK packages

図 6-17. Output Voltage Accuracy vs I_{OUT}

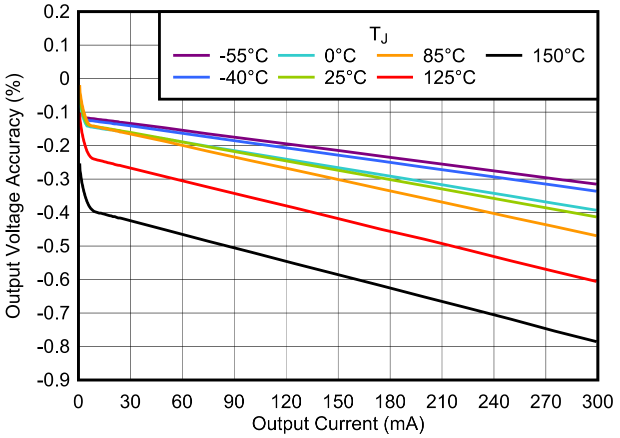


$V_{OUT} = 5.5$ V, $V_{EN} = 1$ V, DQN, YCJ, and YCK packages

図 6-18. Output Voltage Accuracy vs I_{OUT}

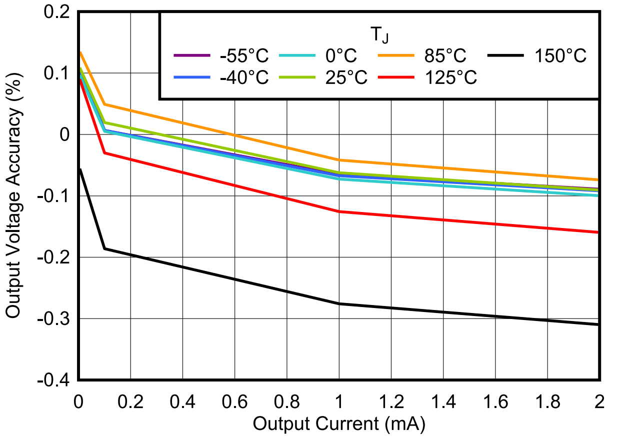
6.7 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.3 V or 1.6 V (whichever is greater), V_{OUT} = 2.8 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, and T_A = 25°C (unless otherwise noted)



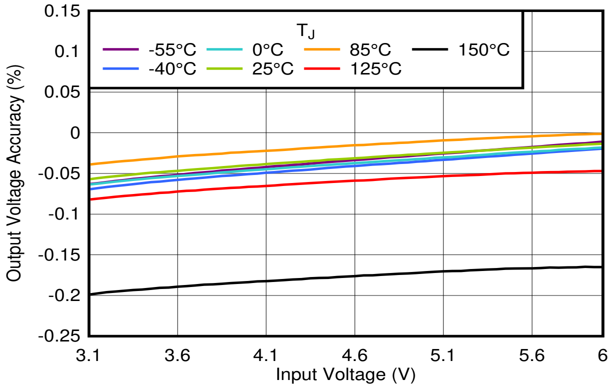
V_{OUT} = 5.5 V, V_{EN} = 1 V, DBV package

図 6-19. Output Voltage Accuracy vs I_{OUT}



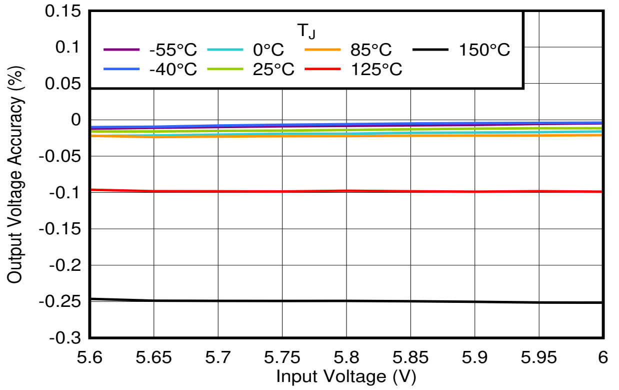
V_{OUT} = 5.5 V, V_{EN} = 1 V, DBV package

図 6-20. Output Voltage Accuracy vs I_{OUT}



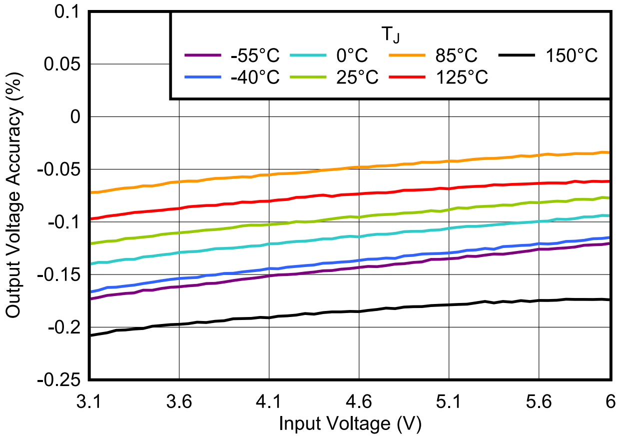
V_{EN} = 1 V, I_{OUT} = 1 mA, DQN, YCJ, and YCK packages

図 6-21. Output Voltage Accuracy vs V_{IN}



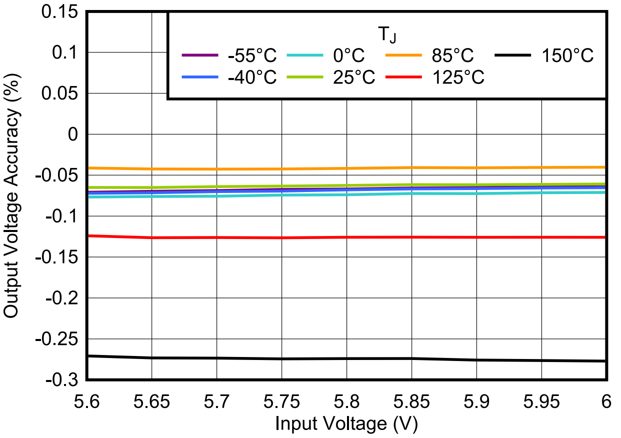
V_{OUT} = 5.5 V, V_{EN} = 1 V, DQN, YCJ, and YCK packages

図 6-22. Output Voltage Accuracy vs V_{IN}



V_{EN} = 1 V, I_{OUT} = 1 mA, DBV package

図 6-23. Output Voltage Accuracy vs V_{IN}

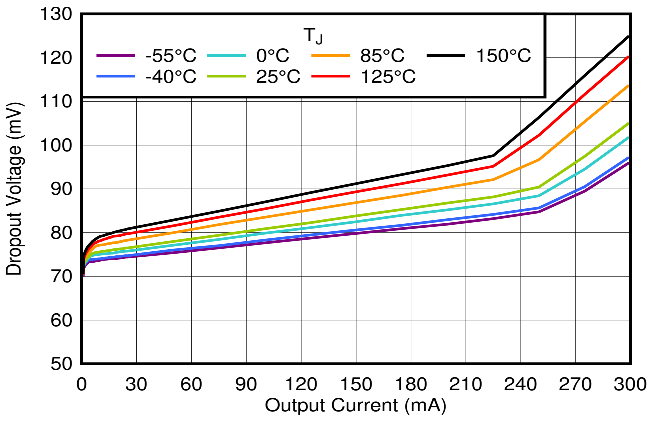


V_{OUT} = 5.5 V, V_{EN} = 1 V, DBV package

図 6-24. Output Voltage Accuracy vs V_{IN}

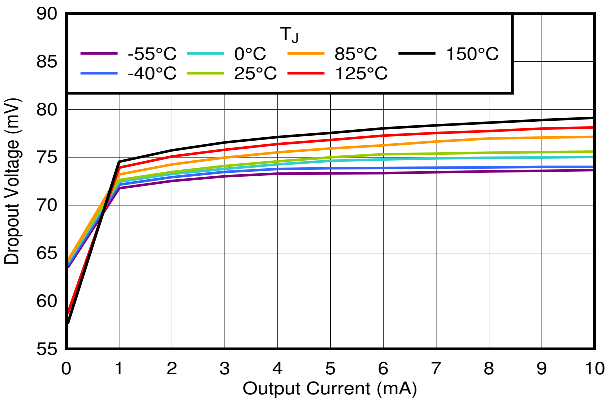
6.7 Typical Characteristics (continued)

$V_{IN} = V_{OUT(NOM)} + 0.3$ V or 1.6 V (whichever is greater), $V_{OUT} = 2.8$ V, $I_{OUT} = 1$ mA, $C_{IN} = 1$ µF, $C_{OUT} = 1$ µF, and $T_A = 25°C$ (unless otherwise noted)



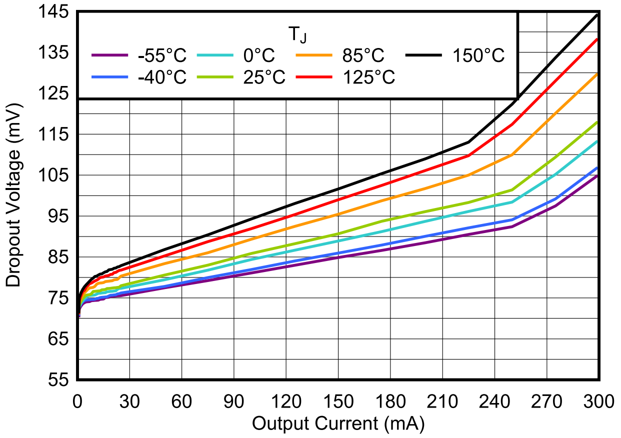
$V_{EN} = 1$ V, DQN, YCJ, and YCK packages

図 6-25. Dropout Voltage vs I_{OUT}



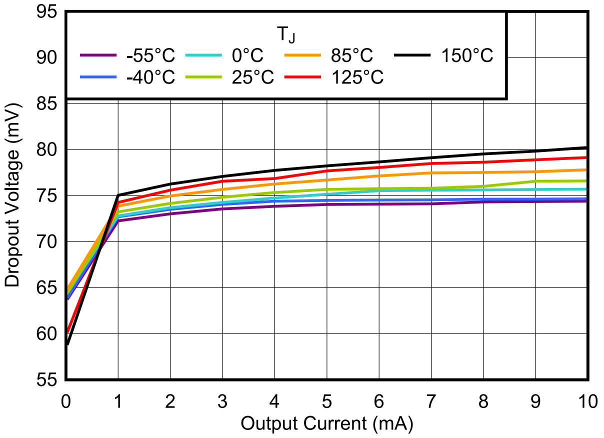
$V_{EN} = 1$ V, DQN, YCJ, and YCK packages

図 6-26. Dropout Voltage vs I_{OUT}



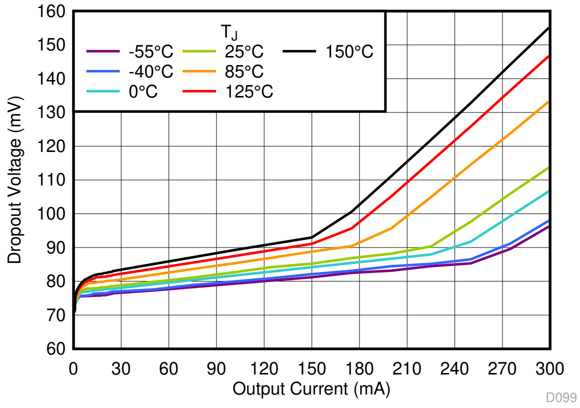
$V_{EN} = 1$ V, DBV package

図 6-27. Dropout Voltage vs I_{OUT}



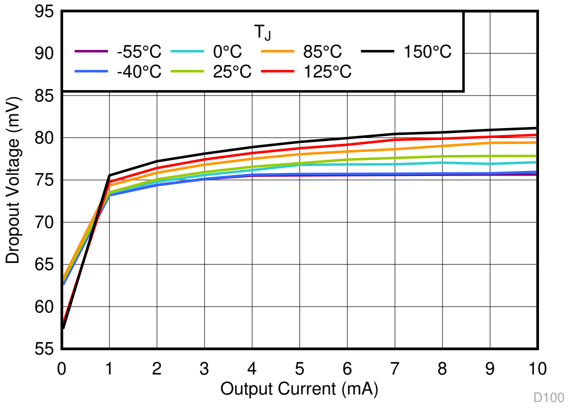
$V_{EN} = 1$ V, DBV package

図 6-28. Dropout Voltage vs I_{OUT}



$V_{OUT} = 1.8$ V, $V_{EN} = 1$ V, DQN, YCJ, and YCK packages

図 6-29. Dropout Voltage vs I_{OUT}

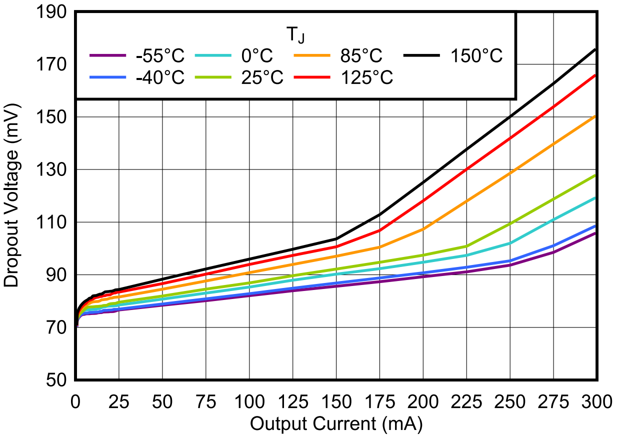


$V_{OUT} = 1.8$ V, $V_{EN} = 1$ V, DQN, YCJ, and YCK packages

図 6-30. Dropout Voltage vs I_{OUT}

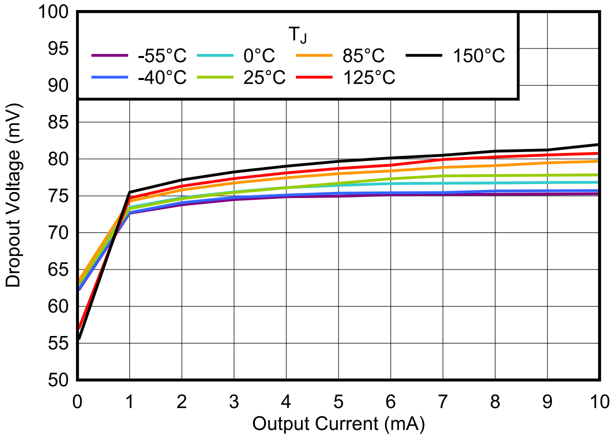
6.7 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.3 V or 1.6 V (whichever is greater), V_{OUT} = 2.8 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, and T_A = 25°C (unless otherwise noted)



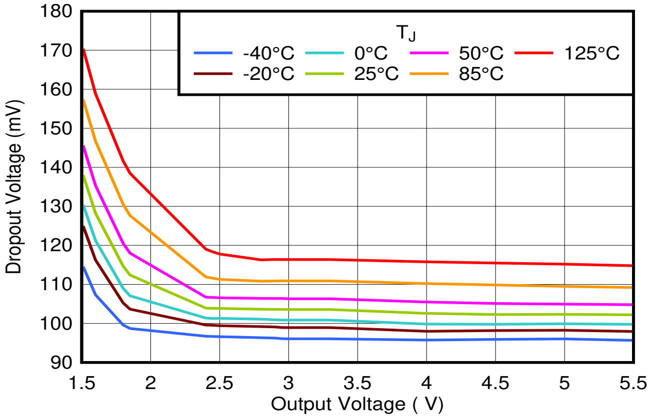
V_{OUT} = 1.8 V, V_{EN} = 1 V, DBV package

図 6-31. Dropout Voltage vs I_{OUT}



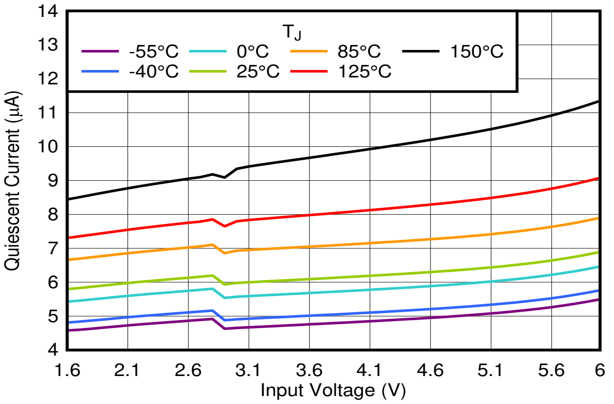
V_{OUT} = 1.8 V, V_{EN} = 1 V, DBV package

図 6-32. Dropout Voltage vs I_{OUT}



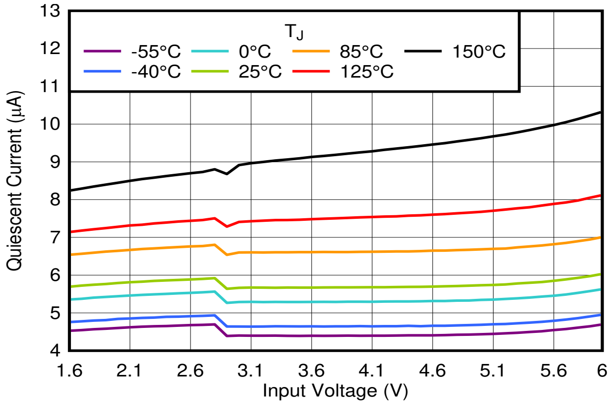
I_{OUT} = 300 mA

図 6-33. Dropout Voltage vs V_{OUT}



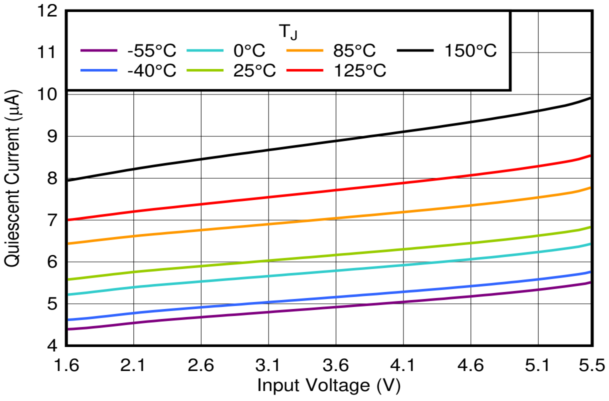
V_{EN} = 1 V, I_{OUT} = 0 mA

図 6-34. I $_{GND}$ vs V_{IN}



V_{EN} = V_{IN}, I_{OUT} = 0 mA

図 6-35. I_{GND} vs V_{IN}

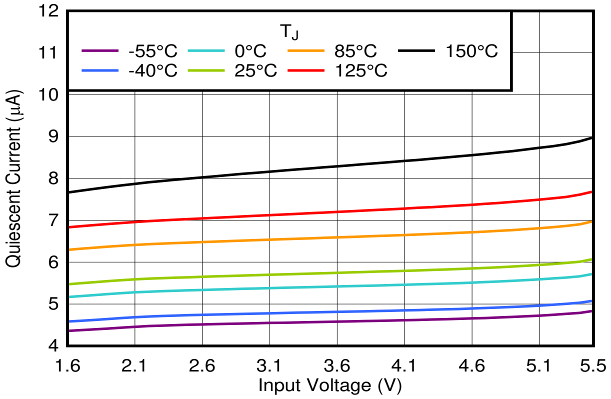


$V_{OUT(NOM)}$ = 5.5 V, V_{EN} = 1 V, I_{OUT} = 0 mA

図 6-36. I_{GND} vs V_{IN} in the Dropout Region

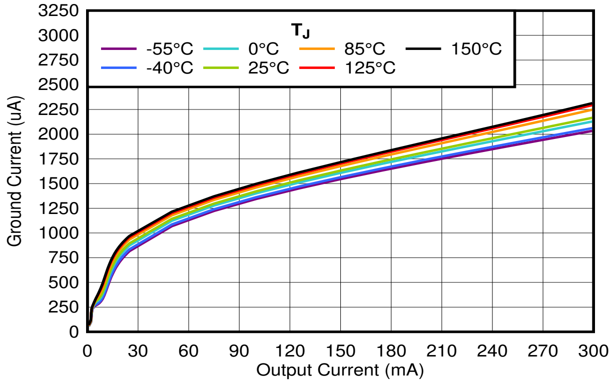
6.7 Typical Characteristics (continued)

$V_{IN} = V_{OUT(NOM)} + 0.3$ V or 1.6 V (whichever is greater), $V_{OUT} = 2.8$ V, $I_{OUT} = 1$ mA, $C_{IN} = 1$ µF, $C_{OUT} = 1$ µF, and $T_A = 25$°C (unless otherwise noted)



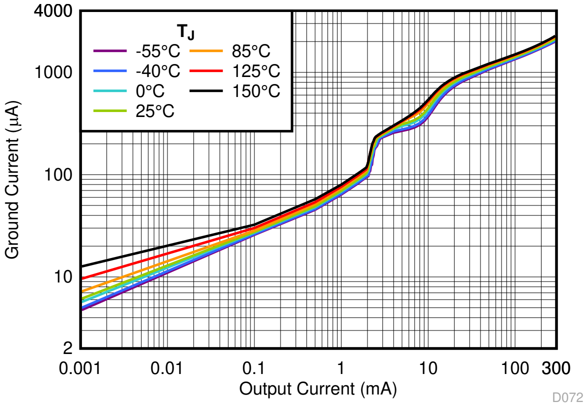
$V_{OUT(NOM)} = 5.5$ V, $V_{EN} = V_{IN}$, $I_{OUT} = 0$ mA

図 6-37. I_{GND} vs V_{IN} in the Dropout Region



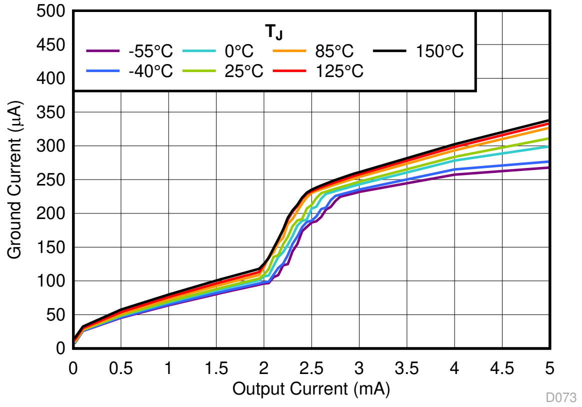
$V_{EN} = 1$ V

図 6-38. I_{GND} vs I_{OUT}



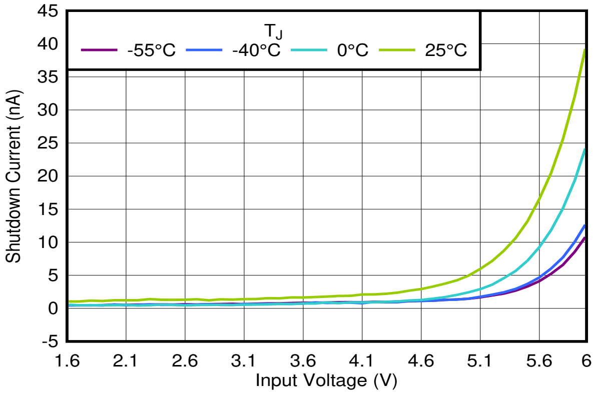
$V_{EN} = 1$ V

図 6-39. I_{GND} vs I_{OUT}



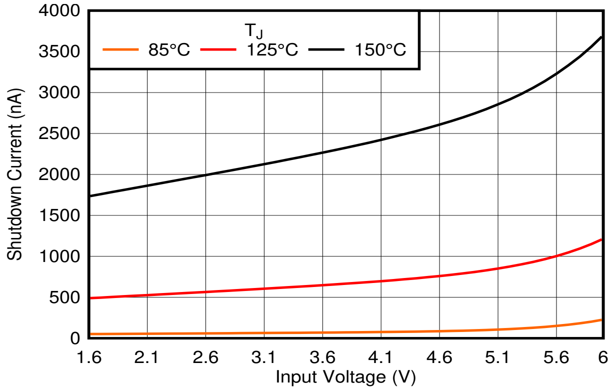
$V_{EN} = 1$ V

図 6-40. I_{GND} vs I_{OUT}



$V_{EN} = 0$ V

図 6-41. Shutdown Current vs V_{IN}

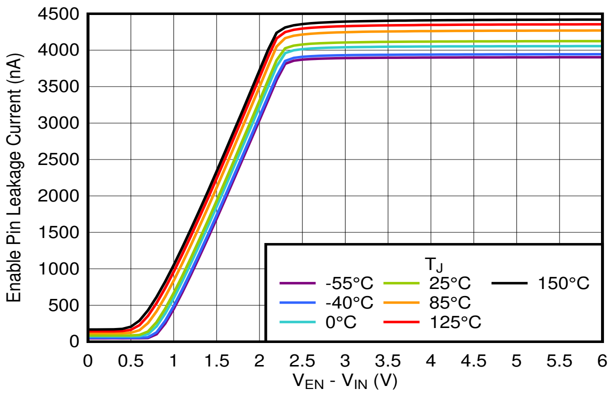


$V_{EN} = 0$ V

図 6-42. Shutdown Current vs V_{IN}

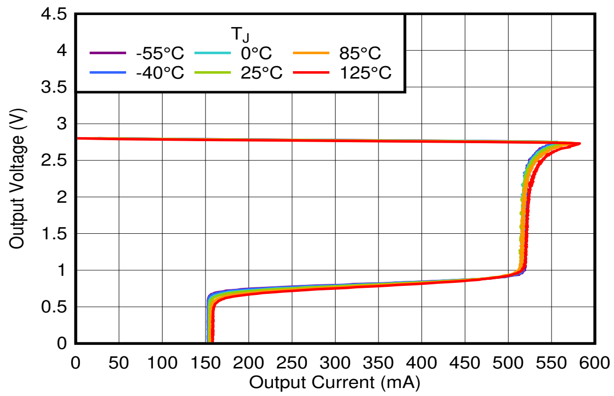
6.7 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.3 V or 1.6 V (whichever is greater), V_{OUT} = 2.8 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, and T_A = 25°C (unless otherwise noted)



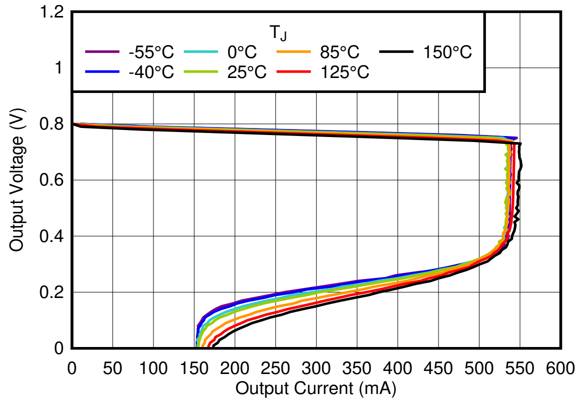
V_{EN} = 6 V, I_{OUT} = 0 mA

図 6-43. Enable Pin Leakage Current vs V_{EN} – V_{IN}



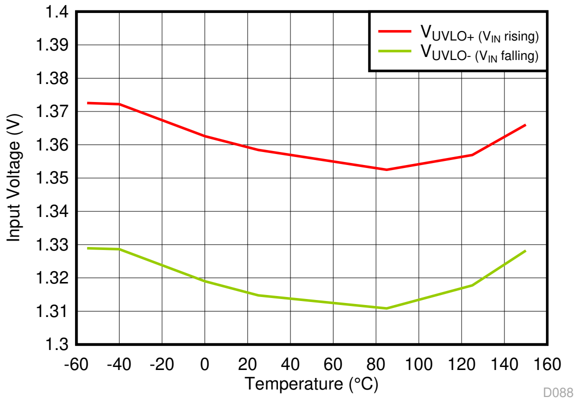
V_{EN} = 1 V

図 6-44. Current Limit



V_{OUT} = 0.8 V, V_{EN} = 1 V

図 6-45. Current Limit



V_{EN} = 1 V

図 6-46. UVLO Threshold vs Temperature

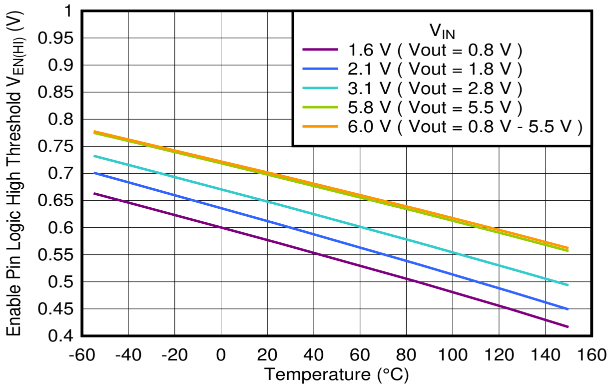


図 6-47. Enable Logic High Threshold vs Temperature

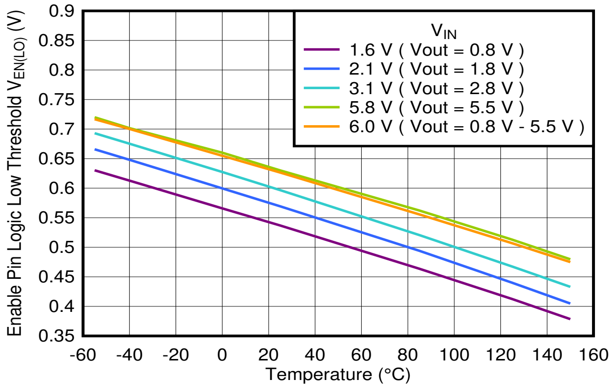
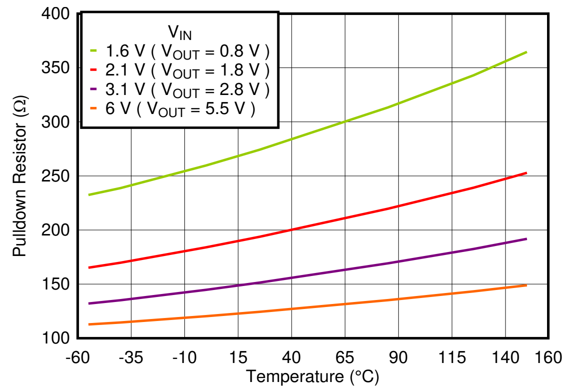


図 6-48. Enable Logic Low Threshold Low vs Temperature

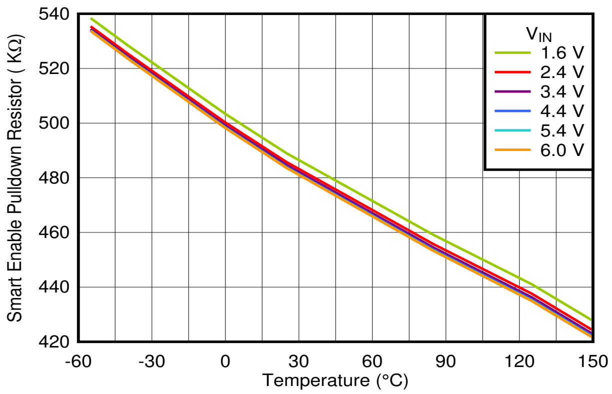
6.7 Typical Characteristics (continued)

$V_{IN} = V_{OUT(NOM)} + 0.3$ V or 1.6 V (whichever is greater), $V_{OUT} = 2.8$ V, $I_{OUT} = 1$ mA, $C_{IN} = 1$ µF, $C_{OUT} = 1$ µF, and $T_A = 25$°C (unless otherwise noted)



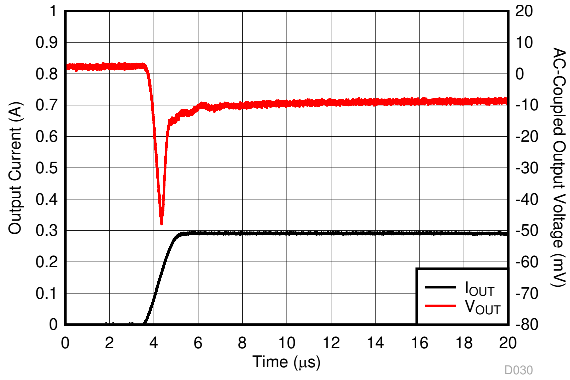
$V_{EN} = 0.25$ V

図 6-49. Output Pulldown Resistor vs Temperature



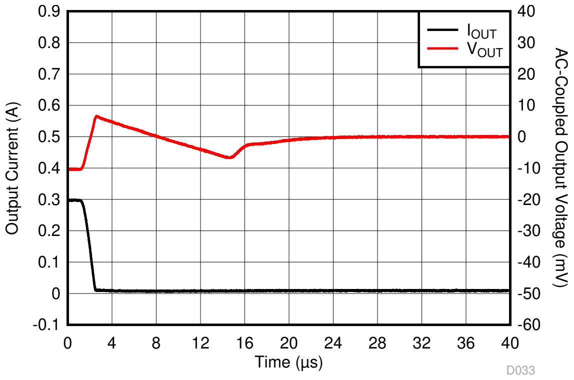
$V_{EN} = 0.25$ V

図 6-50. Smart Enable Pulldown Resistor vs Temperature and V_{IN}



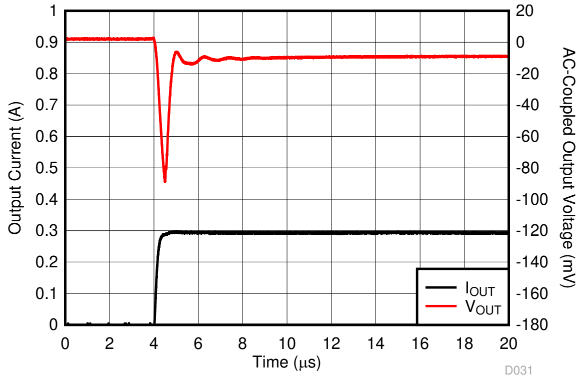
$I_{OUT} = 1$ mA to 300 mA, $t_{RISING} = 1$ µs

図 6-51. Load Transient



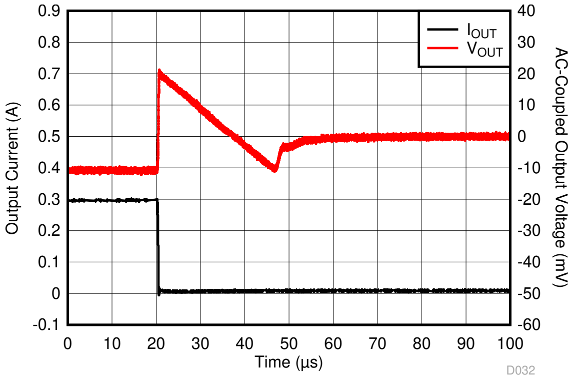
$I_{OUT} = 300$ mA to 1 mA, $t_{FALLING} = 1$ µs

図 6-52. Load Transient



$I_{OUT} = 1$ mA to 300 mA, $t_{RISING} = 200$ ns

図 6-53. Load Transient

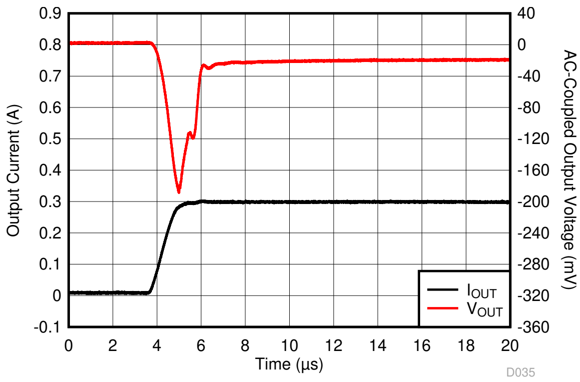


$I_{OUT} = 300$ mA to 1 mA, $t_{FALLING} = 200$ ns

図 6-54. Load Transient

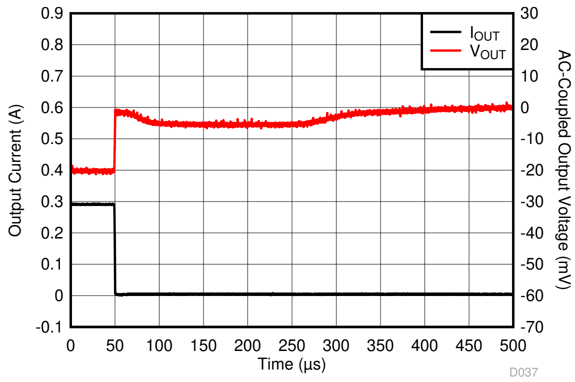
6.7 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.3 V or 1.6 V (whichever is greater), V_{OUT} = 2.8 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, and T_A = 25°C (unless otherwise noted)



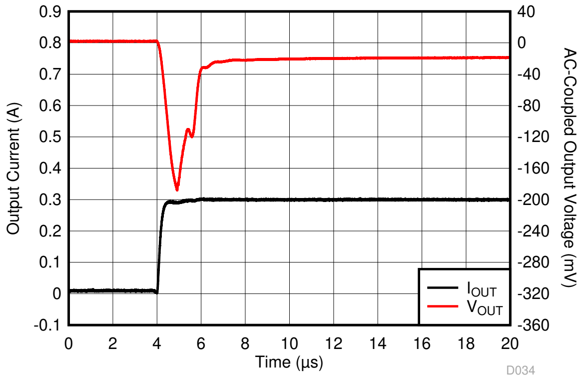
I_{OUT} = 0 mA to 300 mA, t_{RISING} = 1 µs

図 6-55. Load Transient



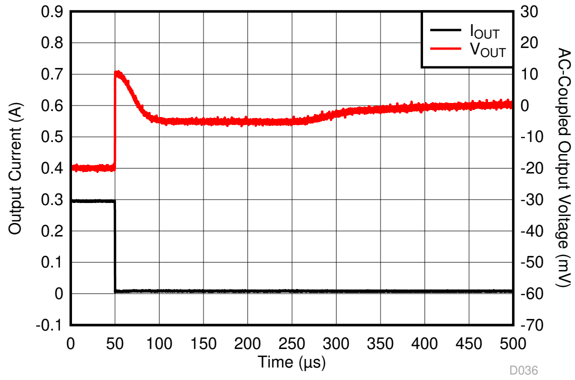
I_{OUT} = 300 mA to 0 mA, $t_{FALLING}$ = 1 µs

図 6-56. Load Transient



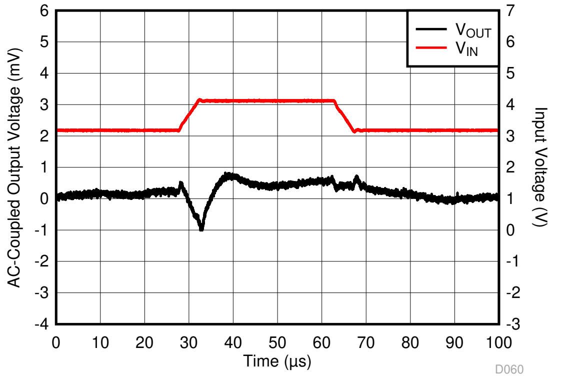
I_{OUT} = 0 mA to 300 mA, t_{RISING} = 200 ns

図 6-57. Load Transient



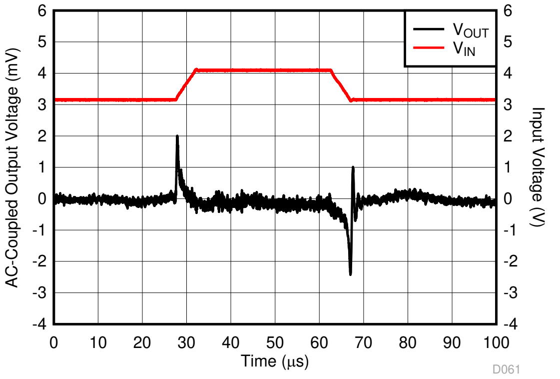
I_{OUT} = 300 mA to 0 mA, $t_{FALLING}$ = 200 ns

図 6-58. Load Transient



V_{IN} = 3.1 V → 4.1 V → 3.1 V, V_{IN} t_{RISING} = 5 µs, I_{OUT} = 1 mA

図 6-59. Line Transient

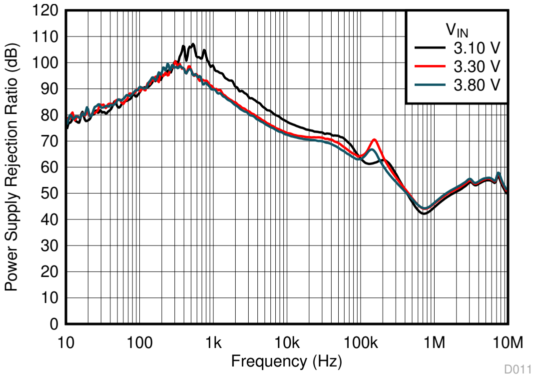


V_{IN} = 3.1 V → 4.1 V → 3.1 V, V_{IN} t_{RISING} = 5 µs, I_{OUT} = 300 mA

図 6-60. Line Transient

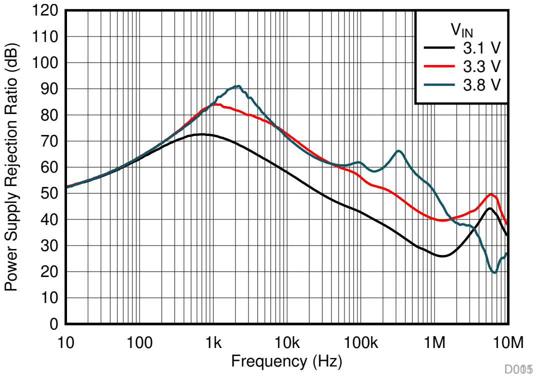
6.7 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.3 V or 1.6 V (whichever is greater), V_{OUT} = 2.8 V, I_{OUT} = 1 mA, C_{IN} = 1 μF, C_{OUT} = 1 μF, and T_A = 25°C (unless otherwise noted)



I_{OUT} = 20 mA

図 6-61. PSRR vs V_{IN} vs Frequency and V_{IN}



I_{OUT} = 300 mA

図 6-62. PSRR vs Frequency and V_{IN}

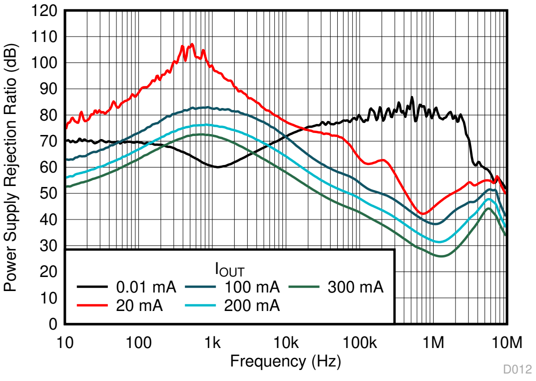
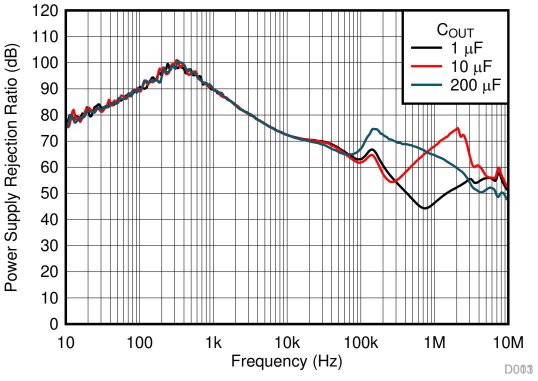
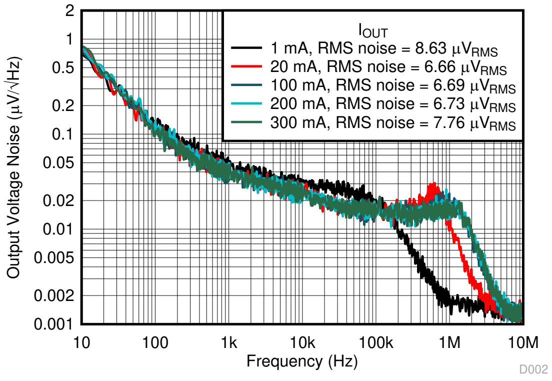


図 6-63. PSRR vs Frequency and I_{OUT}



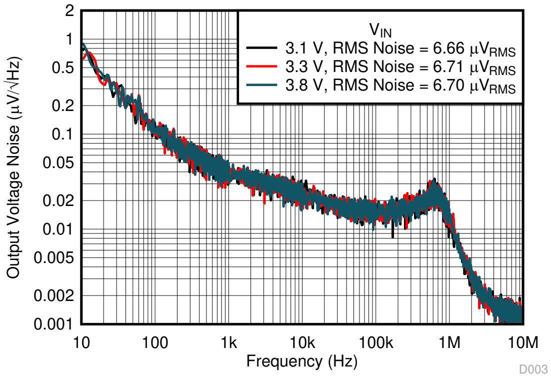
I_{OUT} = 20 mA

図 6-64. PSRR vs Frequency and C_{OUT}



V_{RMS} BW = 10 Hz to 100 kHz

図 6-65. Noise vs Frequency and I_{OUT}

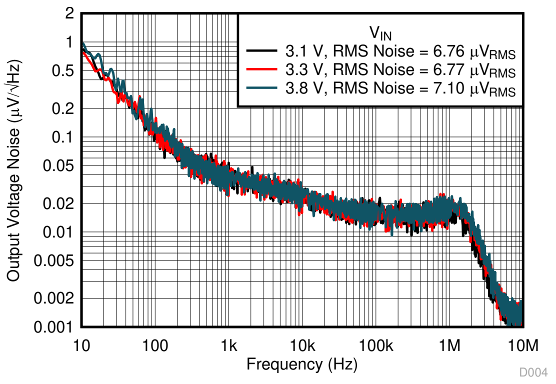


I_{OUT} = 20 mA, V_{RMS} BW = 10 Hz to 100 kHz

図 6-66. Noise vs Frequency and V_{IN}

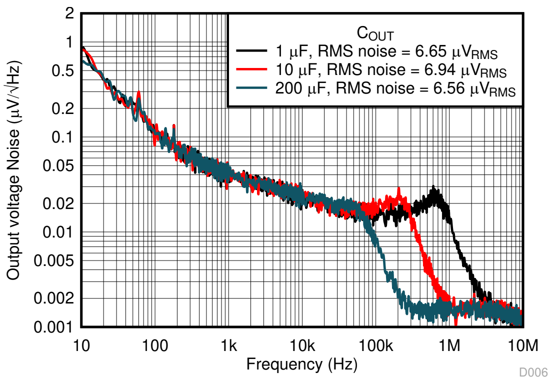
6.7 Typical Characteristics (continued)

$V_{IN} = V_{OUT(NOM)} + 0.3$ V or 1.6 V (whichever is greater), $V_{OUT} = 2.8$ V, $I_{OUT} = 1$ mA, $C_{IN} = 1$ µF, $C_{OUT} = 1$ µF, and $T_A = 25°C$ (unless otherwise noted)



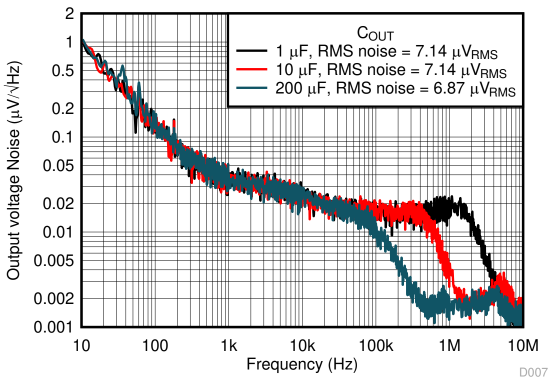
$I_{OUT} = 300$ mA, V_{RMS} BW = 10 Hz to 100 kHz

図 6-67. Noise vs Frequency and V_{IN}



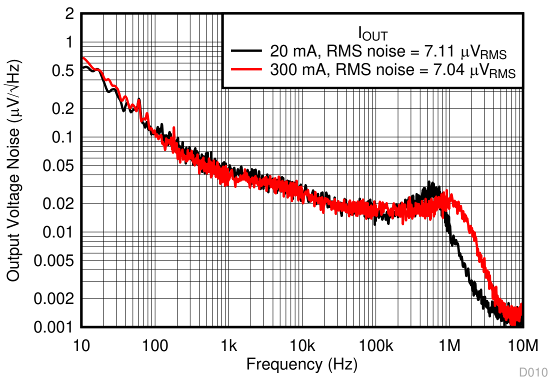
$V_{IN} = 3.8$ V, $I_{OUT} = 20$ mA, V_{RMS} BW = 10 Hz to 100 kHz

図 6-68. Noise vs Frequency and C_{OUT}



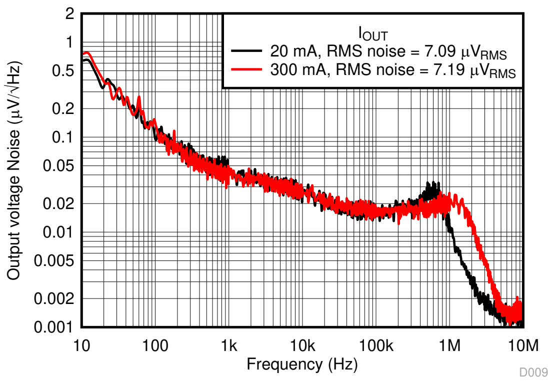
$V_{IN} = 3.8$ V, $I_{OUT} = 300$ mA, V_{RMS} BW = 10 Hz to 100 kHz

図 6-69. Noise vs Frequency and C_{OUT}



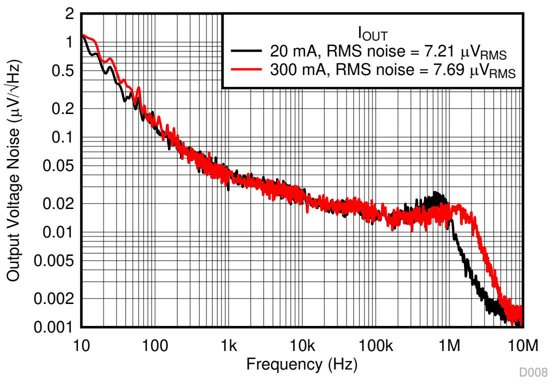
$V_{OUT} = 0.8$ V, V_{RMS} BW = 10 Hz to 100 kHz

図 6-70. Noise vs Frequency and I_{OUT}



$V_{OUT} = 0.8$ V, $V_{IN} = 1.8$ V, V_{RMS} BW = 10 Hz to 100 kHz

図 6-71. Noise vs Frequency and I_{OUT}

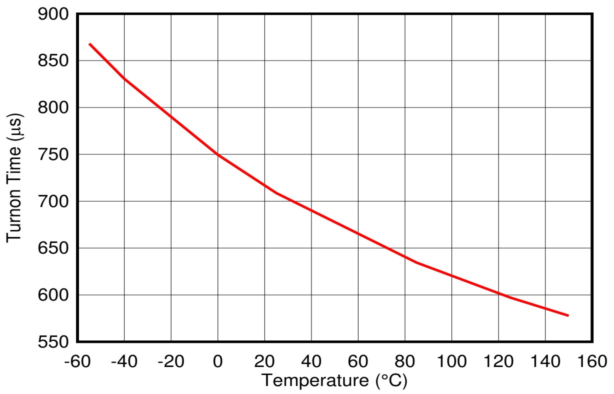


$V_{OUT} = 5.5$ V, $V_{IN} = 6$ V, V_{RMS} BW = 10 Hz to 100 kHz

図 6-72. Noise vs Frequency and I_{OUT}

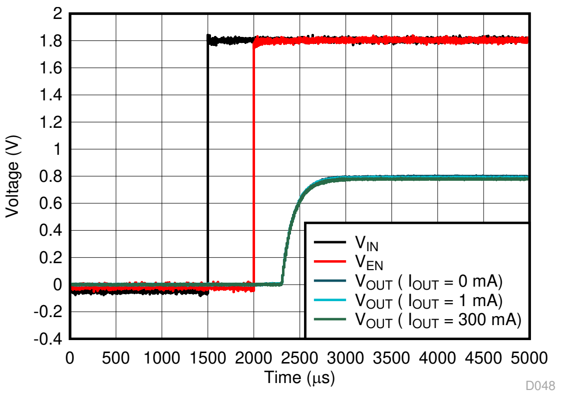
6.7 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.3 V or 1.6 V (whichever is greater), V_{OUT} = 2.8 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, and T_A = 25°C (unless otherwise noted)



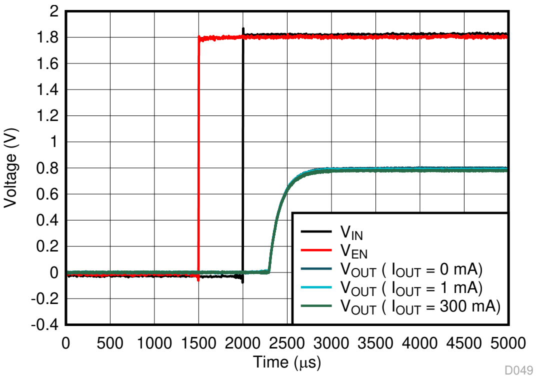
From V_{EN} = $V_{EN(HI)}$ to V_{OUT} = 95% of $V_{OUT(NOM)}$, I_{OUT} = 0 mA

図 6-73. Start-Up Turn-On Time



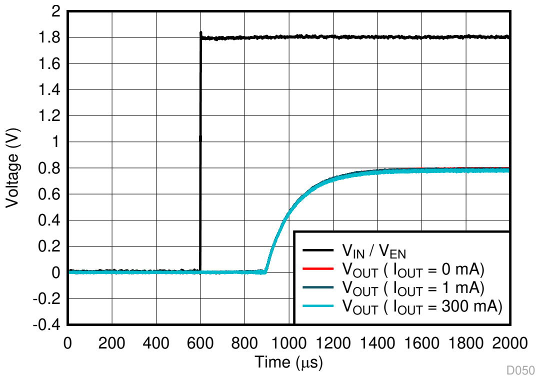
V_{OUT} = 0.8 V, V_{IN} = 0 V to 1.8 V, V_{EN} = 0 V to 1.8 V, V_{EN} rises 500 µs behind V_{IN}, V_{IN} and V_{EN} slew rate = 1 V/µs

図 6-74. Start-Up



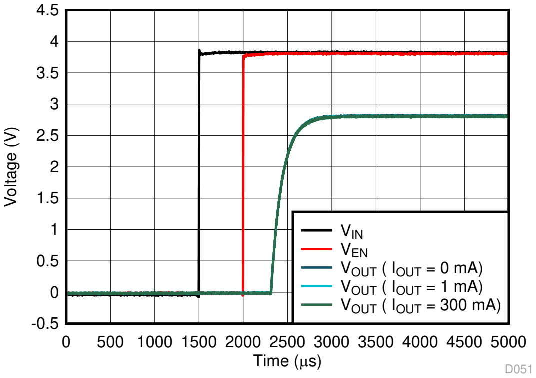
V_{OUT} = 0.8 V, V_{IN} = 0 V to 1.8 V, V_{EN} = 0 V to 1.8 V, V_{EN} rises 500 µs ahead of V_{IN}, V_{IN} and V_{EN} slew rate = 1 V/µs

図 6-75. Start-Up



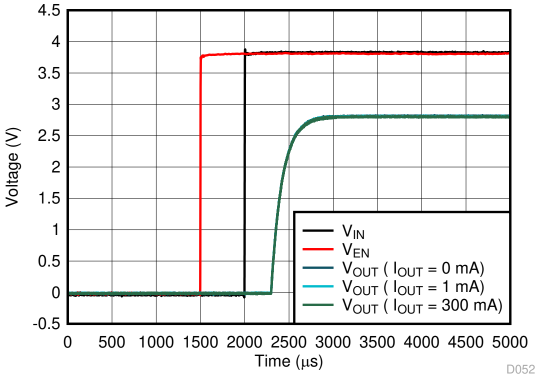
V_{OUT} = 0.8 V, V_{IN} = 0 V to 1.8 V, V_{EN} = V_{IN}, V_{IN} slew rate = 1 V/µs

図 6-76. Start-Up



V_{IN} = 0 V to 3.8 V, V_{EN} = 0 V to 3.8 V, V_{EN} rises 500 µs behind V_{IN}, V_{IN} and V_{EN} slew rate = 1 V/µs

図 6-77. Start-Up

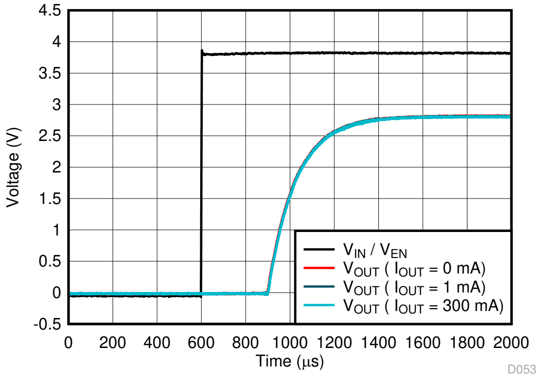


V_{IN} = 0 V to 3.8 V, V_{EN} = 0 V to 3.8 V, V_{EN} rises 500 µs ahead of V_{IN}, V_{IN} and V_{EN} slew rate = 1 V/µs

図 6-78. Start-Up

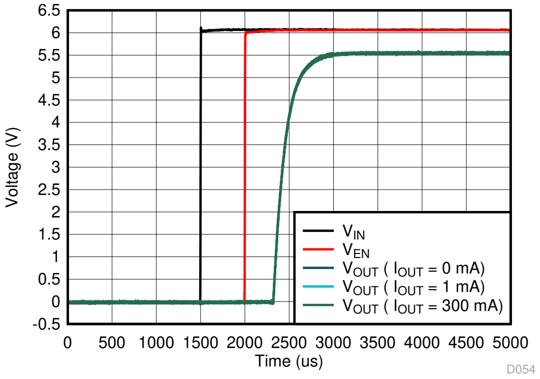
6.7 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.3 V or 1.6 V (whichever is greater), V_{OUT} = 2.8 V, I_{OUT} = 1 mA, C_{IN} = 1 μF, C_{OUT} = 1 μF, and T_A = 25°C (unless otherwise noted)



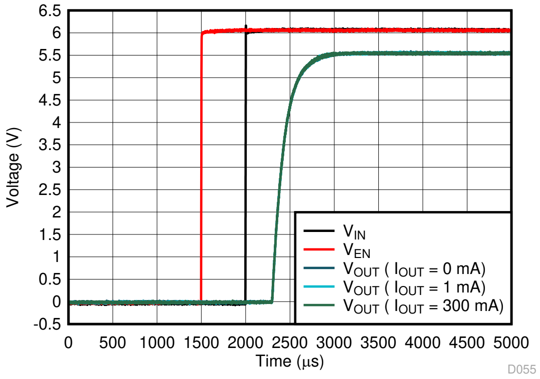
V_{IN} = 0 V to 3.8 V, V_{EN} = 0 V to 3.8 V, V_{EN} = V_{IN}, V_{IN} and slew rate = 1 V/μs

図 6-79. Start-Up



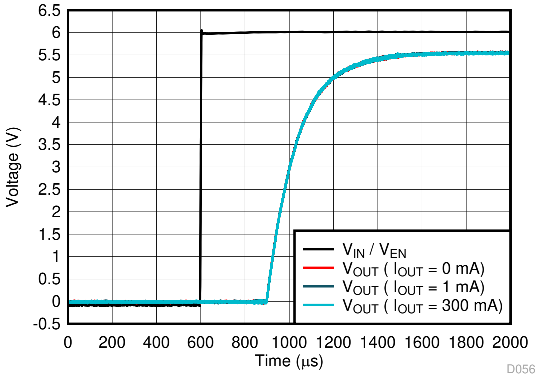
V_{OUT} = 5.5 V, V_{IN} = 0 V to 6.0 V, V_{EN} = 0 V to 6.0 V, V_{EN} rises 500 μs behind V_{IN}, V_{IN} and V_{EN} slew rate = 1 V/μs

図 6-80. Start-Up



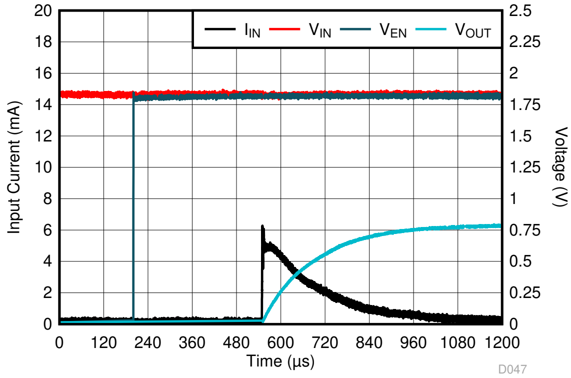
V_{OUT} = 5.5 V, V_{IN} = 0 V to 6.0 V, V_{EN} = 0 V to 6.0 V, V_{EN} rises 500 μs ahead of V_{IN}, V_{IN} and V_{EN} slew rate = 1 V/μs

図 6-81. Start-Up



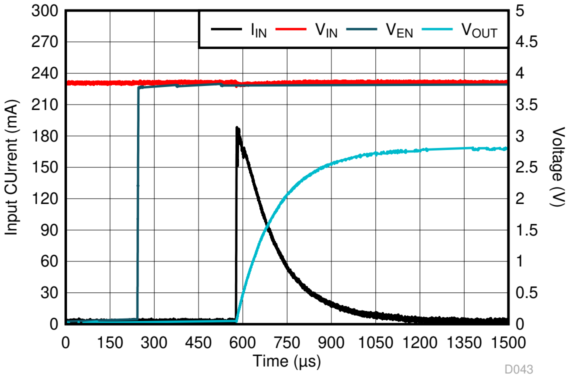
V_{OUT} = 5.5 V, V_{IN} = 0 V to 6 V, V_{EN} = V_{IN}, V_{IN} slew rate = 1 V/μs

図 6-82. Start-Up



V_{OUT} = 0.8 V, V_{IN} = 1.8 V, V_{EN} = 0 V to 1.8 V, V_{EN} slew rate = 1 V/μs, C_{OUT} = 10 μF

図 6-83. Inrush Current

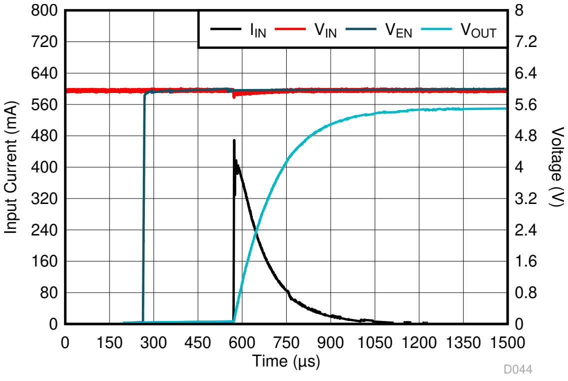


V_{IN} = 3.8 V, V_{EN} = 0 V to 3.8 V, V_{EN} slew rate = 1 V/μs, C_{OUT} = 10 μF

図 6-84. Inrush Current

6.7 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.3 V or 1.6 V (whichever is greater), V_{OUT} = 2.8 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, and T_A = 25°C (unless otherwise noted)



V_{OUT} = 5.5 V, V_{IN} = 6.0 V, V_{EN} = 0 V to 6.0 V, V_{EN} slew rate = 1 V/µs, C_{OUT} = 10 µF

図 6-85. Inrush Current

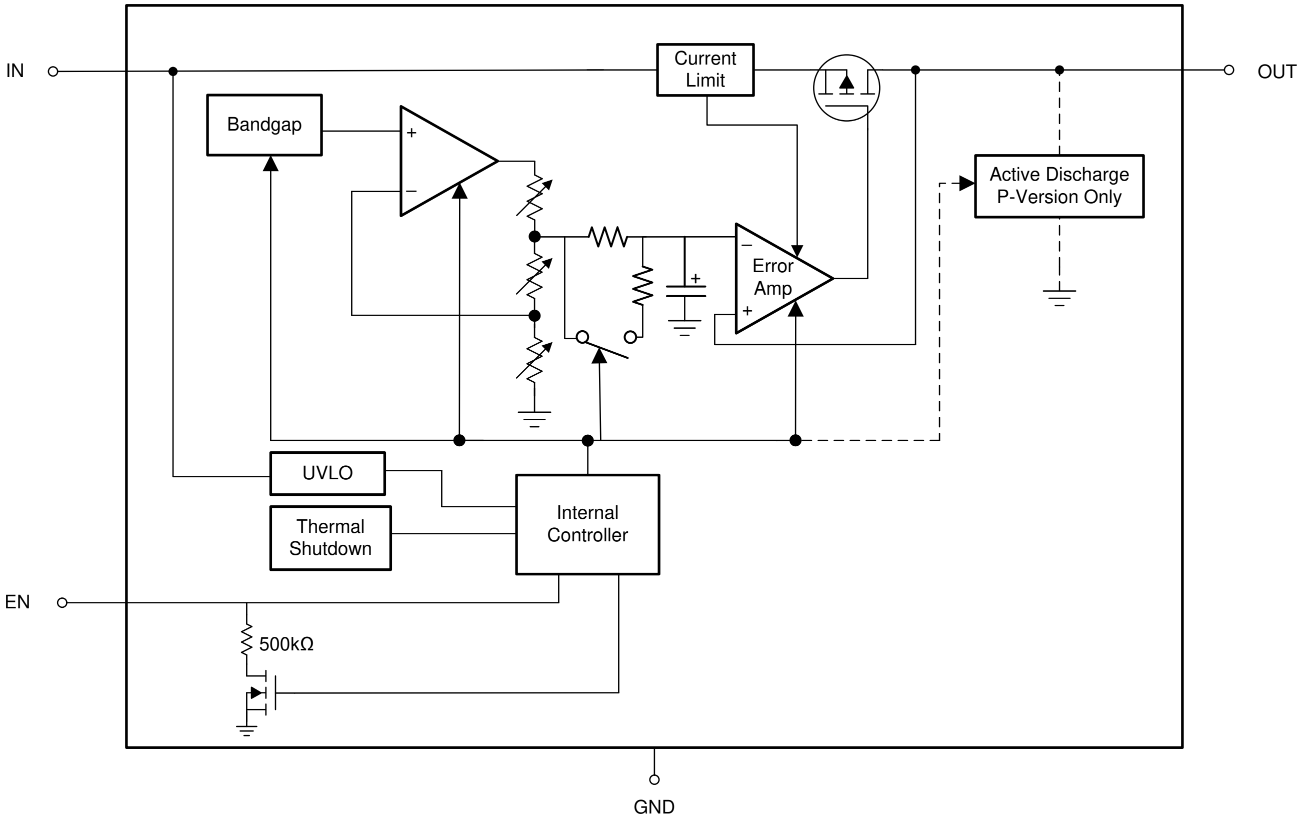
7 Detailed Description

7.1 Overview

Designed to meet the needs of sensitive RF and analog circuits, the TPS7A20 provides low noise, high PSRR, low quiescent current, as well as low line and load transient response figures. Using innovative design techniques, the TPS7A20 offers class-leading noise performance without the need for a separate noise filter capacitor.

The TPS7A20 is designed to operate with a single 1-μF input capacitor and a single 1-μF ceramic output capacitor.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Low Output Noise

Any internal noise at the TPS7A20 reference voltage is reduced by a first-order, low-pass RC filter before being passed to the output buffer stage. The low-pass RC filter has a –3-dB cut-off frequency of approximately 0.1 Hz.

During start-up, the filter resistor is bypassed to reduce output rise time; the filter begins normal operation after the output voltage reaches the correct value.

7.3.2 Smart Enable

The enable (EN) input polarity is active high. The output voltage is enabled when the voltage of the enable input is greater than $V_{EN(HI)}$ and disabled when the enable input voltage is less than $V_{EN(LOW)}$. If independent control of the output voltage is not needed, connect EN to IN.

This device has a smart enable circuit to reduce quiescent current. When the voltage on the enable pin is driven above $V_{EN(HI)}$, as listed in the *Electrical Characteristics* table, the device is enabled and the smart enable internal pulldown resistor ($R_{EN(PULLDOWN)}$) is disconnected. When the enable pin is floating, the $R_{EN(PULLDOWN)}$ is connected and pulls the enable pin low to disable the device. The $R_{EN(PULLDOWN)}$ value is listed in the *Electrical Characteristics* table.

7.3.3 Dropout Voltage

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage ($V_{IN} – V_{OUT}$) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the value required to maintain output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \tag{1}$$

7.3.4 Foldback Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brickwall-foldback scheme. The current limit transitions from a brickwall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brickwall scheme limits the output current to the current limit (I_{CL}). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current as the output voltage approaches GND. When the output is shorted, the device supplies a typical current called the short-circuit current limit (I_{SC}). I_{CL} and I_{SC} are listed in the *Electrical Characteristics* table.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brickwall current limit, the pass transistor dissipates power [($V_{IN} – V_{OUT}$) × I_{CL}]. When the device output is shorted and the output is below $V_{FOLDBACK}$, the pass transistor dissipates power [($V_{IN} – V_{OUT}$) × I_{SC}]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application report.

図 7-1 shows a diagram of the foldback current limit.

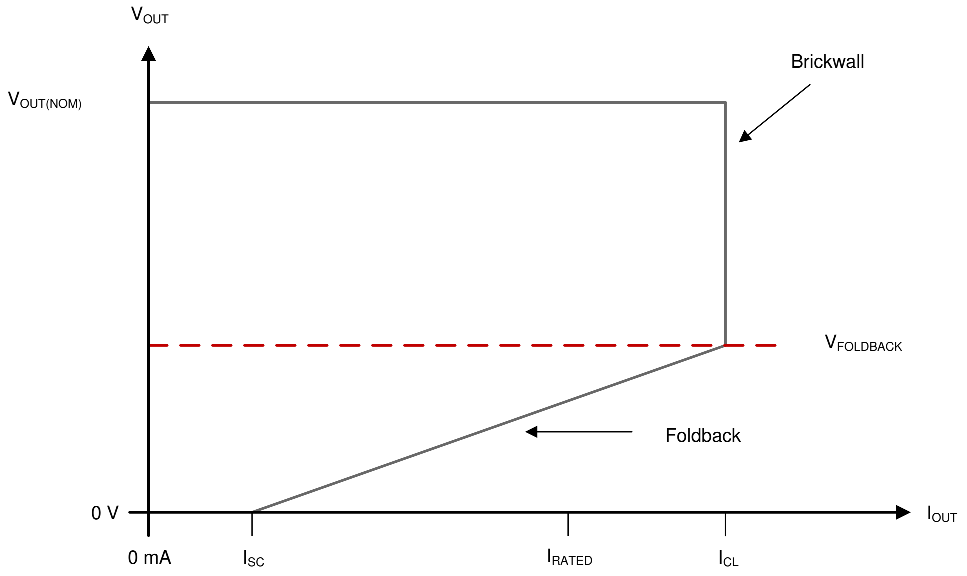


図 7-1. Foldback Current Limit

7.3.5 Undervoltage Lockout (UVLO)

The device has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage, allowing a controlled and consistent turn on and off of the output voltage. To prevent the device from turning off if the input drops during turn on, the UVLO has hysteresis as specified in the *Electrical Characteristics* table.

7.3.6 Thermal Shutdown

A thermal shutdown protection circuit disables the LDO when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis assures that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short, thus the device may cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during startup can be high from large $V_{IN} – V_{OUT}$ voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before startup completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed its operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overload conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

7.3.7 Active Discharge

An internal pulldown MOSFET connects a resistor from OUT to ground when the device is disabled to actively discharge the output capacitance. The active discharge circuit is activated by driving EN low or by the voltage on IN falling below the undervoltage lockout (UVLO) threshold.

Do not rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can possibly flow from the output to the input. This reverse current flow can cause damage to the device. Limit reverse current to no more than 5% of the device rated current for a short period of time.

7.4 Device Functional Modes

7.4.1 Device Functional Mode Comparison

表 7-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

表 7-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{EN(LOW)}$	Not applicable	$T_J > T_{SD(shutdown)}$

7.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

7.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during startup), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

7.4.4 Disabled

The output of the LDO can be shut down by driving EN to less than $V_{EN(LOW)}$ (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, internal circuits are shut down, and the output voltage is actively discharged to ground by an internal discharge circuit between OUT and ground.

8 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

8.1.1 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. As a rule of thumb, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors recommended in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

8.1.2 Input and Output Capacitor Requirements

Although the LDO itself is stable without an input capacitor, good analog design practice is to connect a capacitor from IN to GND, with a value at least equal to the nominal value specified in the *Recommended Operating Conditions* table. The input capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR, and is recommended if the source impedance is greater than 0.5 Ω. When the source resistance and inductance are sufficiently high, especially in the presence of load transients, the overall system may be susceptible to instability (including ringing and sustained oscillation) and other performance degradation if there is insufficient capacitance between IN and GND. A capacitor with a value greater than the minimum may be necessary if large, fast-rise-time load or line transients are anticipated or if the device is located more than a few centimeters from the input power source.

An output capacitor of an appropriate value helps ensure stability and improve dynamic performance. Use an output capacitor within the range specified in the *Recommended Operating Conditions* table.

8.1.3 Load Transient Response

The load-step transient response is the output voltage response by the LDO to a step in load current, whereby output voltage regulation is maintained. There are two key transitions during a load transient response: the transition from a light to a heavy load and the transition from a heavy to a light load. The regions shown in 図 8-1 are broken down as follows. Regions A, E, and H are where the output voltage is in steady-state.

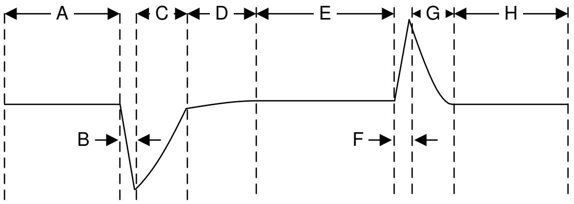


図 8-1. Load Transient Waveform

During transitions from a light load to a heavy load, the:

- Initial voltage dip is a result of the depletion of the output capacitor charge and parasitic impedance to the output capacitor (region B)
- Recovery from the dip results from the LDO increasing its sourcing current, and leads to output voltage regulation (region C)

During transitions from a heavy load to a light load, the:

- Initial voltage rise results from the LDO sourcing a large current, and leads to the output capacitor charge to increase (region F)
- Recovery from the rise results from the LDO decreasing its sourcing current in combination with the load discharging the output capacitor (region G)

A larger output capacitance reduces the peaks during a load transient but slows down the response time of the device. A larger DC load also reduces the peaks because the amplitude of the transition is lowered and a higher current discharge path is provided for the output capacitor.

8.1.4 Undervoltage Lockout (UVLO) Operation

The UVLO circuit ensures that the device stays disabled before its input supply reaches the minimum operational voltage range, and ensures that the device shuts down when the input supply collapses. 図 8-2 shows the UVLO circuit response to various input voltage events. The diagram can be separated into the following parts:

- Region A: The device does not start until the input reaches the UVLO rising threshold.
- Region B: Normal operation, regulating device.
- Region C: Brownout event above the UVLO falling threshold (UVLO rising threshold – UVLO hysteresis). The output may fall out of regulation but the device remains enabled.
- Region D: Normal operation, regulating device.
- Region E: Brownout event below the UVLO falling threshold. The device is disabled in most cases and the output falls because of the load and active discharge circuit. The device is re-enabled when the UVLO rising threshold is reached by the input voltage and a normal start-up follows.
- Region F: Normal operation followed by the input falling to the UVLO falling threshold.
- Region G: The device is disabled when the input voltage falls below the UVLO falling threshold to 0 V. The output falls because of the load and active discharge circuit.

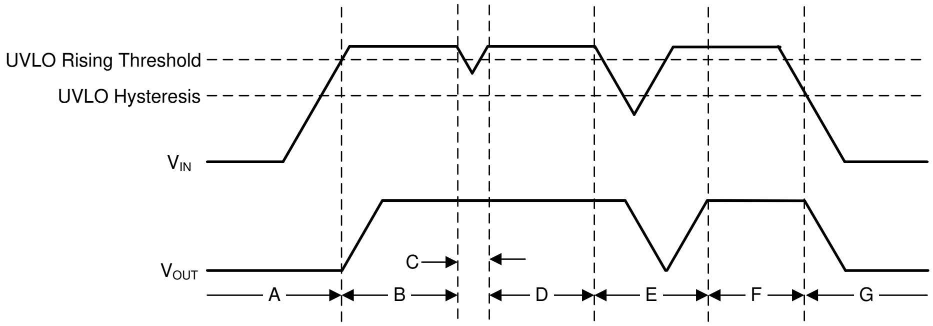


図 8-2. Typical UVLO Operation

8.1.5 Power Dissipation (P_D)

Circuit reliability demands that proper consideration be given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free as possible of other heat-generating devices that cause added thermal stresses.

As a first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. Use 式 2 to approximate P_D:

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \tag{2}$$

Power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the TPS7A20 allows for maximum efficiency across a wide range of output voltages.

The main heat conduction path for the device is through the thermal pad on the package. As such, the thermal pad must be soldered to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to any inner plane areas or to a bottom-side copper plane.

The maximum power dissipation determines the maximum allowable junction temperature (T_J) for the device. According to 式 3, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A). 式 4 rearranges 式 3 for output current.

$$T_J = T_A + (R_{\theta JA} \times P_D) \tag{3}$$

$$I_{OUT} = (T_J - T_A) / [R_{\theta JA} \times (V_{IN} - V_{OUT})] \tag{4}$$

Unfortunately, this thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the *Thermal Information* table is determined by the JEDEC standard, PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the X2SON package junction-to-case (bottom) thermal resistance ($R_{\theta JC(bot)}$) plus the thermal resistance contribution by the PCB copper.

8.1.5.1 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are used in accordance with 式 5 and are given in the *Thermal Information* table.

$$\Psi_{JT} : T_J = T_T + \Psi_{JT} \times P_D \text{ and } \Psi_{JB} : T_J = T_B + \Psi_{JB} \times P_D \tag{5}$$

where:

- P_D is the power dissipated as explained in 式 2
- T_T is the temperature at the center-top of the device package
- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

8.1.5.2 Recommended Area for Continuous Operation

The operational area of an LDO is limited by the dropout voltage, output current, junction temperature, and input voltage. The recommended area for continuous operation for a linear regulator is given in 図 8-3 and can be separated into the following parts:

- Dropout voltage limits the minimum differential voltage between the input and the output ($V_{IN} – V_{OUT}$) at a given output current level. See the *Dropout Operation* section for more details.
- The rated output currents limits the maximum recommended output current level. Exceeding this rating causes the device to fall out of specification.
- The rated junction temperature limits the maximum junction temperature of the device. Exceeding this rating causes the device to fall out of specification and reduces long-term reliability.
  - The shape of the slope is given by 式 4. The slope is nonlinear because the maximum-rated junction temperature of the LDO is controlled by the power dissipation across the LDO; thus when $V_{IN} – V_{OUT}$ increases the output current must decrease.
- The rated input voltage range governs both the minimum and maximum of $V_{IN} – V_{OUT}$.

図 8-3 shows the recommended area of operation for this device on a JEDEC-standard high-K board with a $R_{θJA}$ as given in the *Thermal Information* table.

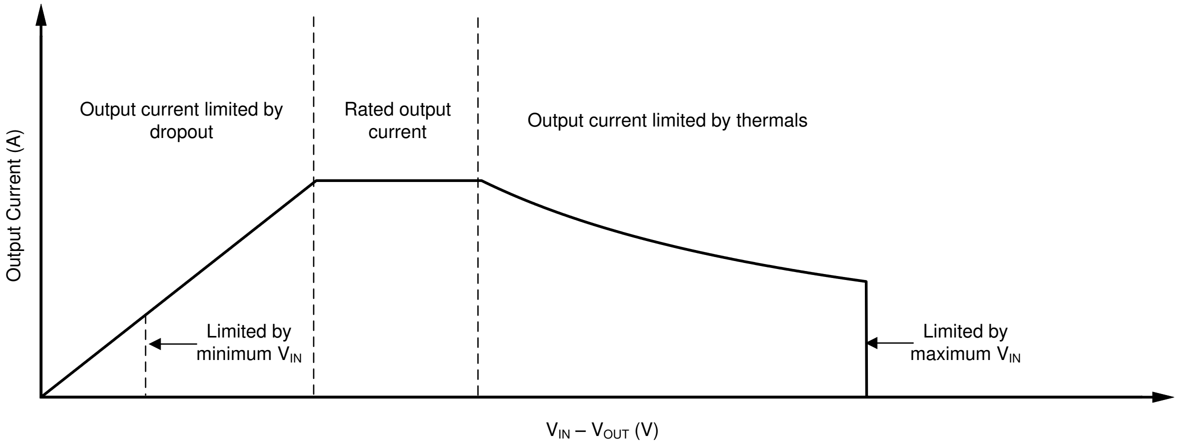


図 8-3. Region Description of Continuous Operation Regime

8.2 Typical Application

図 8-4 shows the typical application circuit for the TPS7A20. Input and output capacitances may need to be increased above the 1 µF minimum for some applications.

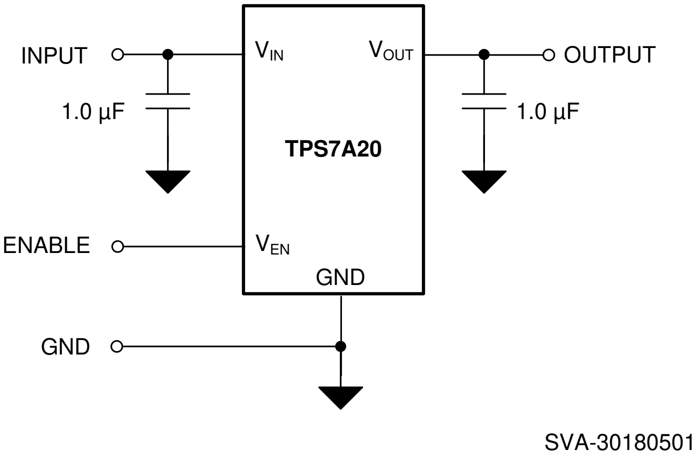


図 8-4. TPS7A20 Typical Application

8.2.1 Design Requirements

表 8-1 summarizes the design requirements for 図 8-4.

表 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	3.1 V to 3.6 V
Output voltage	2.8 V
Output current	200 mA
Maximum ambient temperature	85°C

8.2.2 Detailed Design Procedure

For this design example, the 2.8-V output version (TPS7A2028) is selected. A nominal 3.3-V input supply is assumed. A minimum 1.0-µF input capacitor is recommended to minimize the effect of resistance and inductance between the 3.3-V source and the LDO input. A minimum 1.0-µF output capacitor is also recommended for stability and good load transient response. The dropout voltage (V_{DO}) is less than 140 mV maximum at a 2.8-V output voltage and 300-mA output current, so there are no dropout issues with a minimum input voltage of 3.0 V and a maximum output current of 200 mA.

8.2.3 Application Curves

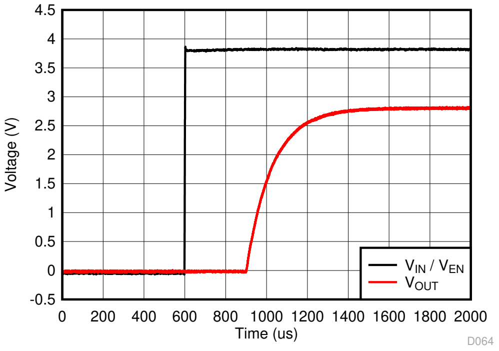


図 8-5. Start-Up

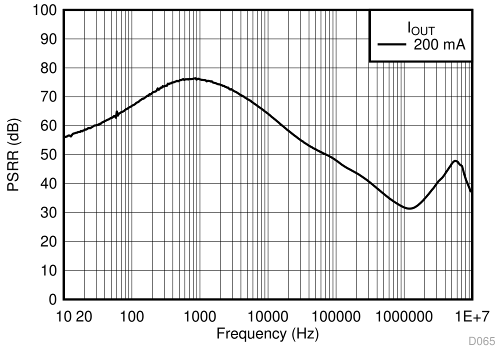


図 8-6. PSRR

9 Power Supply Recommendations

This device is designed to operate from an input supply voltage range of 1.6 V to 6.0 V. The input supply must be well regulated and free of spurious noise. To ensure that the output voltage is well regulated and dynamic performance is optimum, the input supply must be at least $V_{OUT(nom)}$ + 0.3 V or 1.6 V, whichever is greater. TI highly recommends using a 1-µF or greater input capacitor to reduce the impedance of the input supply, especially during transients.

10 Layout

10.1 Layout Guidelines

- Place input and output capacitors as close to the device as possible.
- Use copper planes for device connections to optimize thermal performance.
- Place thermal vias around the device to distribute the heat.
- Do not place a thermal via directly beneath the thermal pad of the DQN package. A via can wick solder or solder paste away from the thermal pad joint during the soldering process, leading to a compromised solder joint on the thermal pad.

10.2 Layout Examples

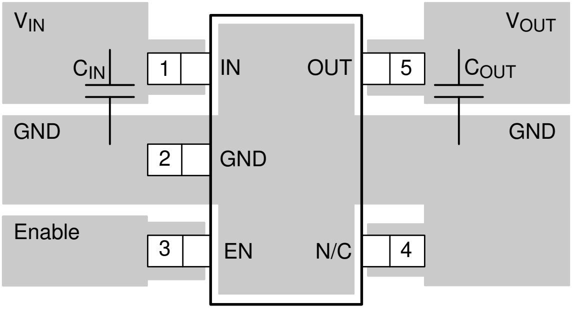


図 10-1. DBV Package (SOT-23) Typical Layout

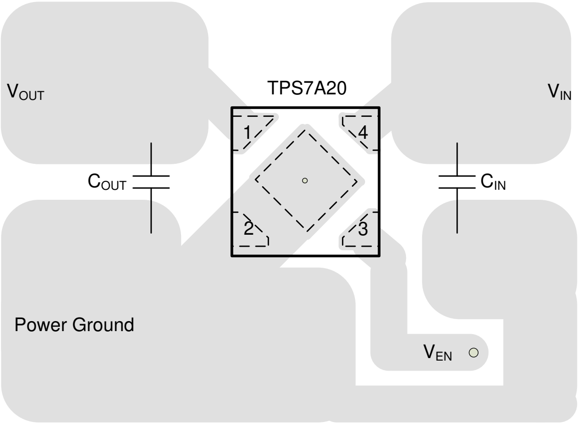


図 10-2. DQN Package (X2SON) Typical Layout

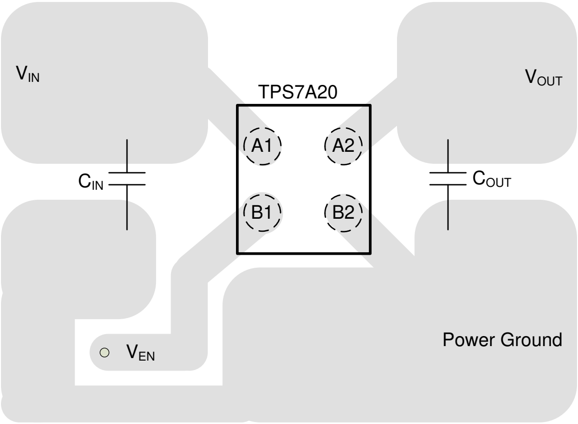


図 10-3. YCJ and YCK Package (DSBGA) Typical Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

表 11-1. Device Nomenclature

PRODUCT [1] [2]	V_{OUT}
TPS7A20**xx(x)Pyyyz**	**xx(x)** is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 28 = 2.8 V; 125 = 1.25 V). **P** indicates an active output discharge feature. All members of the TPS7A20 family actively discharge the output when the device is disabled. **yyy** is the package designator. **z** is the package quantity. R is for reel (3000 pieces for DQN and DBV; 12000 pieces for YCJ and YCK).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.
(2) Output voltages from 0.8 V to 5.5 V in 25-mV increments are available. Contact the factory for details and availability.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

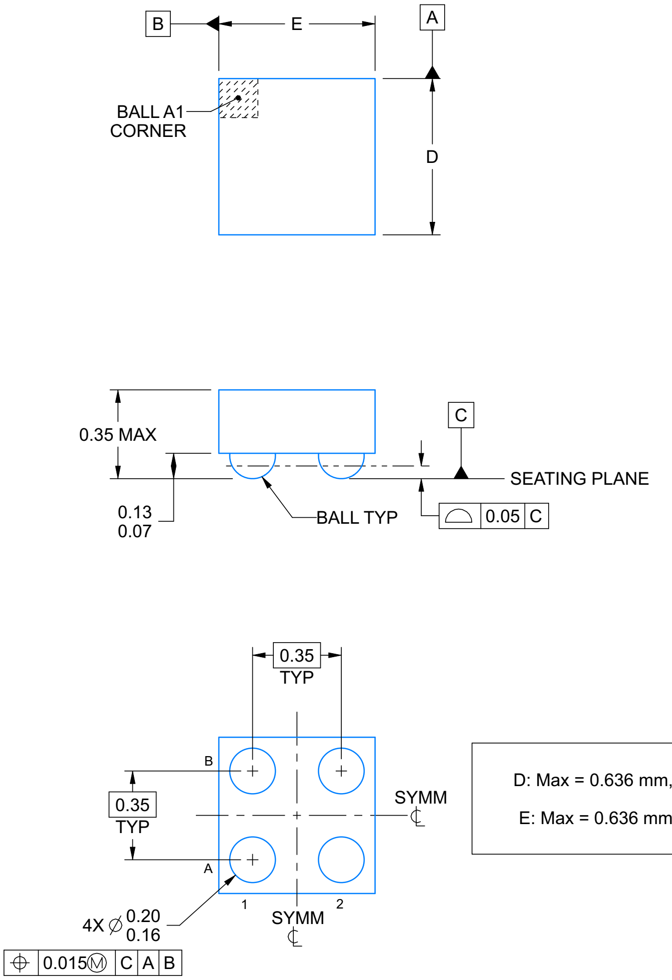
12.1 Mechanical Data

PACKAGE OUTLINE

YCJ0004-C02

DSBGA - 0.35 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 0.636 mm, Min = 0.596 mm

E: Max = 0.636 mm, Min = 0.596 mm

4226216/A 09/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

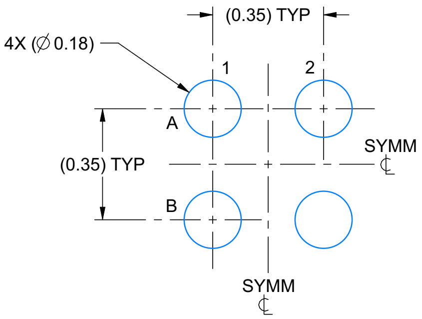
TEXAS INSTRUMENTS
www.ti.com

EXAMPLE BOARD LAYOUT

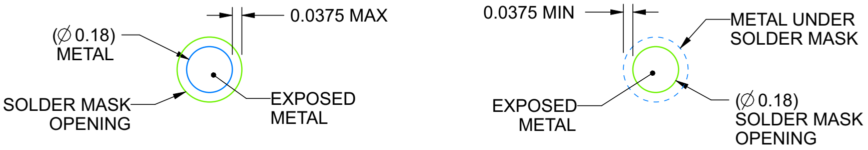
YCJ0004-C02

DSBGA - 0.35 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X



NON-SOLDER MASK
DEFINED

SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK DETAILS
NOT TO SCALE

4226216/A 09/2020

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

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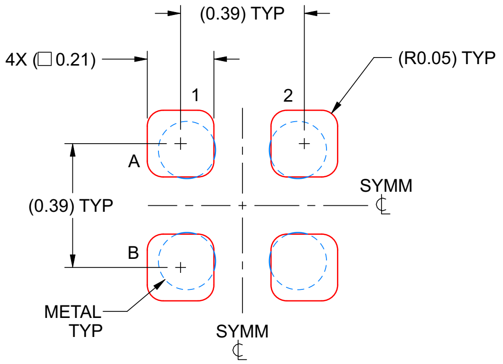
EXAMPLE STENCIL DESIGN

YCJ0004-C02

DSBGA - 0.35 mm max height

DIE SIZE BALL GRID ARRAY

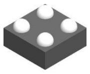


SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 50X

4226216/A 09/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

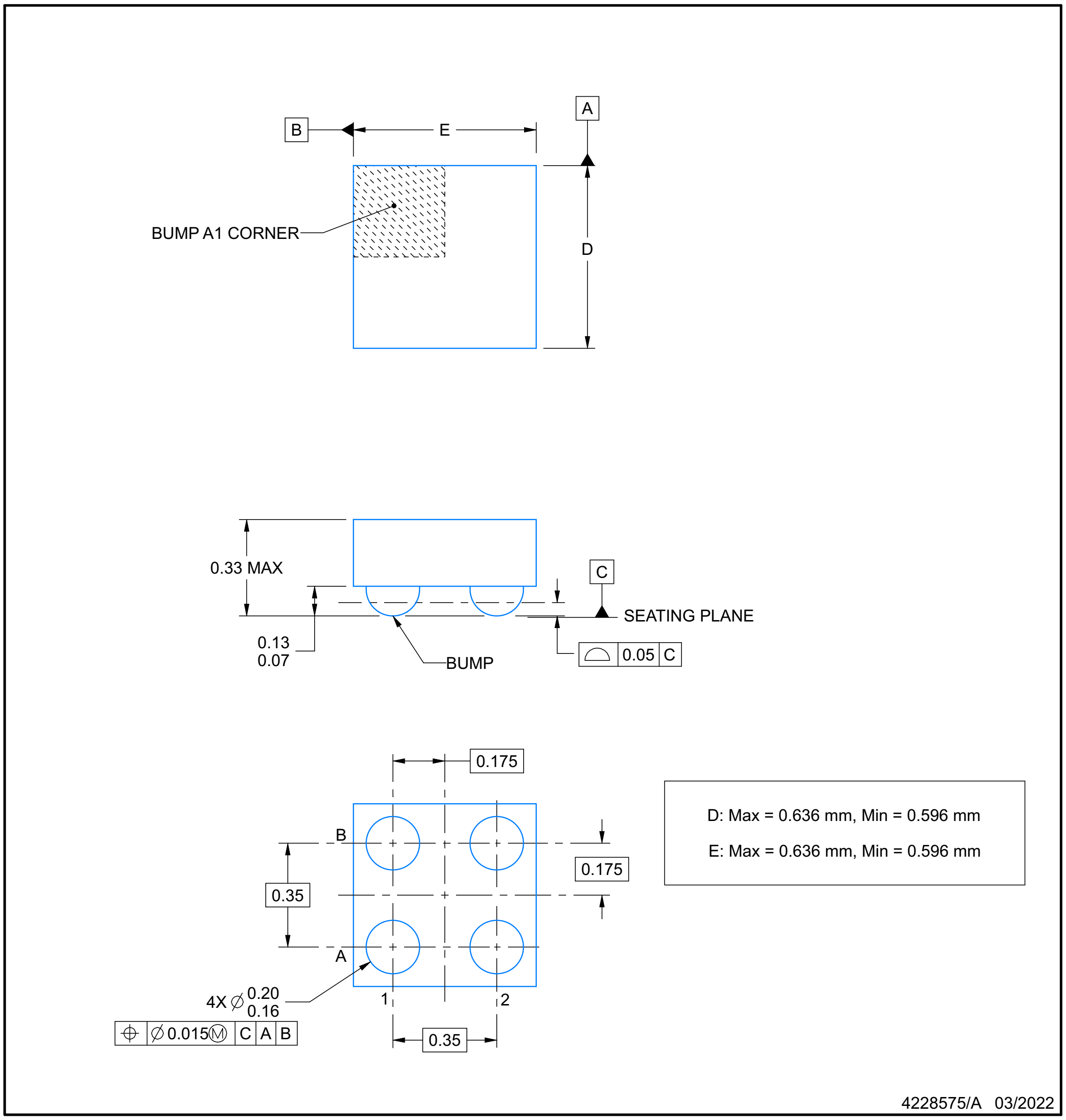


PACKAGE OUTLINE

YCK0004-C01

DSBGA - 0.33mm MAX HEIGHT

DIE SIZE BALL GRID ARRAY



D: Max = 0.636 mm, Min = 0.596 mm

E: Max = 0.636 mm, Min = 0.596 mm

4228575/A 03/2022

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

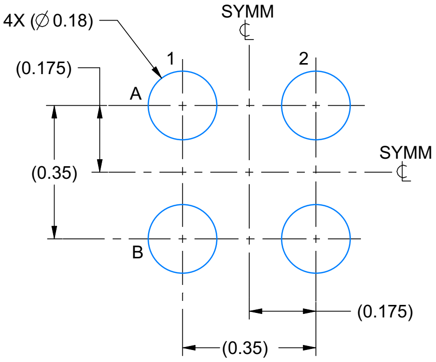
www.ti.com

EXAMPLE BOARD LAYOUT

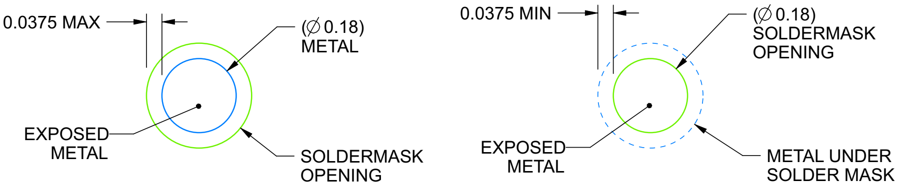
YCK0004-C01

DSBGA - 0.33mm MAX HEIGHT

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X



NON SOLDERMASK
DEFINED

SOLDERMASK
DEFINED
(PREFERRED)

SOLDERMASK DETAILS
NOT TO SCALE

4228575/A 03/2022

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

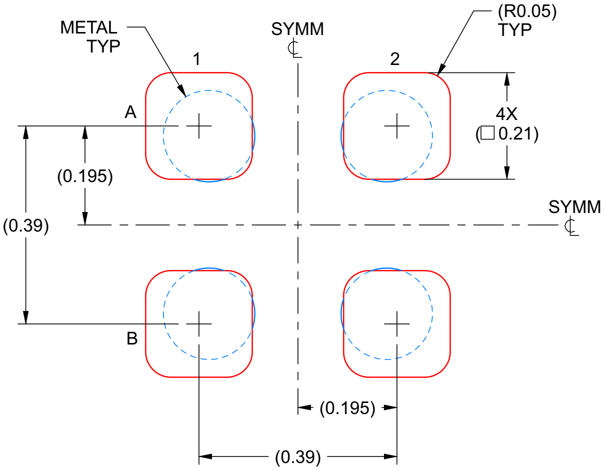
TEXAS INSTRUMENTS
www.ti.com

EXAMPLE STENCIL DESIGN

YCK0004-C01

DSBGA - 0.33mm MAX HEIGHT

DIE SIZE BALL GRID ARRAY



SOLDERPASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE:80X

4228575/A 03/2022

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTPS7A2016YCKR	ACTIVE	DSBGA	YCK	4	12000	TBD	Call TI	Call TI	-40 to 125		Samples
PTPS7A2025PDQNR	ACTIVE	X2SON	DQN	4	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTPS7A2045PDQNR	ACTIVE	X2SON	DQN	4	3000	TBD	Call TI	Call TI	-40 to 125		Samples
TPS7A2009PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	2GBF	Samples
TPS7A2009PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	KT	Samples
TPS7A20105PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	KS	Samples
TPS7A2011PYCKR	ACTIVE	DSBGA	YCK	4	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	Q	Samples
TPS7A2012PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	2ATF	Samples
TPS7A2012PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	JC	Samples
TPS7A2012PYCJR	ACTIVE	DSBGA	YCJ	4	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	M	Samples
TPS7A2015PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	2DTF	Samples
TPS7A2015PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	JD	Samples
TPS7A201825PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	IQ	Samples
TPS7A20185PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	2CBF	Samples
TPS7A20185PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	JE	Samples
TPS7A20185PYCKR	ACTIVE	DSBGA	YCK	4	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	T	Samples
TPS7A2018PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	2AUF	Samples
TPS7A2018PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	JF	Samples
TPS7A2018PDQNRM3	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	JF	Samples
TPS7A2018PYCKR	ACTIVE	DSBGA	YCK	4	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	D	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A2020PYCKR	ACTIVE	DSBGA	YCK	4	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	S	Samples
TPS7A20225PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PX	Samples
TPS7A2022PYCKR	ACTIVE	DSBGA	YCK	4	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	K	Samples
TPS7A2024PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	2CCF	Samples
TPS7A2025PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	2AVF	Samples
TPS7A2025PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	JG	Samples
TPS7A2025PYCJR	ACTIVE	DSBGA	YCJ	4	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	L	Samples
TPS7A2027PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	KO	Samples
TPS7A2027PYCJR	ACTIVE	DSBGA	YCJ	4	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	N	Samples
TPS7A20285PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	2GCF	Samples
TPS7A20285PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	KN	Samples
TPS7A20285PYCKR	ACTIVE	DSBGA	YCK	4	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	P	Samples
TPS7A2028PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	2AWF	Samples
TPS7A2028PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	JH	Samples
TPS7A2028PDQNRM3	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	JH	Samples
TPS7A2028PYCJR	ACTIVE	DSBGA	YCJ	4	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	E	Samples
TPS7A2028PYCKR	ACTIVE	DSBGA	YCK	4	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	E	Samples
TPS7A2029PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	JI	Samples
TPS7A2030PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	2AXF	Samples
TPS7A2030PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	JJ	Samples
TPS7A2031PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	2GDF	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A2032PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	2GEF	Samples
TPS7A2033PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	2AZF	Samples
TPS7A2033PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	JA	Samples
TPS7A2033PDQNRM3	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	JA	Samples
TPS7A2033PYCJR	ACTIVE	DSBGA	YCJ	4	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	O	Samples
TPS7A2036PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	2GIF	Samples
TPS7A2036PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	KP	Samples
TPS7A2040PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	KQ	Samples
TPS7A2042PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	2GFF	Samples
TPS7A2042PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	KV	Samples
TPS7A2045PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	2GGF	Samples
TPS7A2045PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	JB	Samples
TPS7A2050PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	2B1F	Samples
TPS7A2050PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	KR	Samples
TPS7A2050PDQNRM3	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	KR	Samples
TPS7A2050PYCKR	ACTIVE	DSBGA	YCK	4	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	H	Samples
TPS7A2055PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	2GHF	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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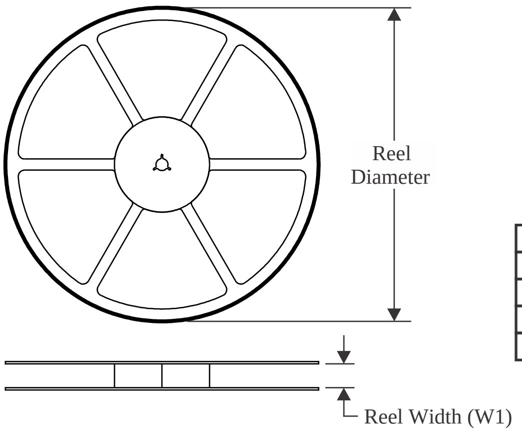
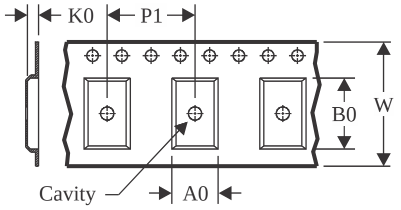
TAPE AND REEL INFORMATION

REEL DIMENSIONS

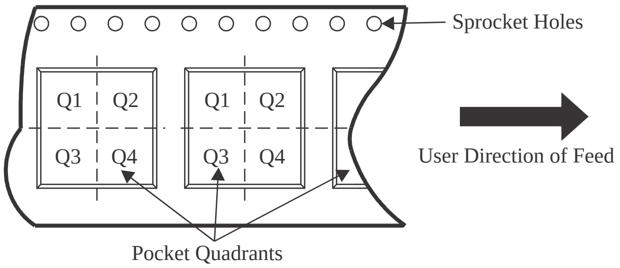


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



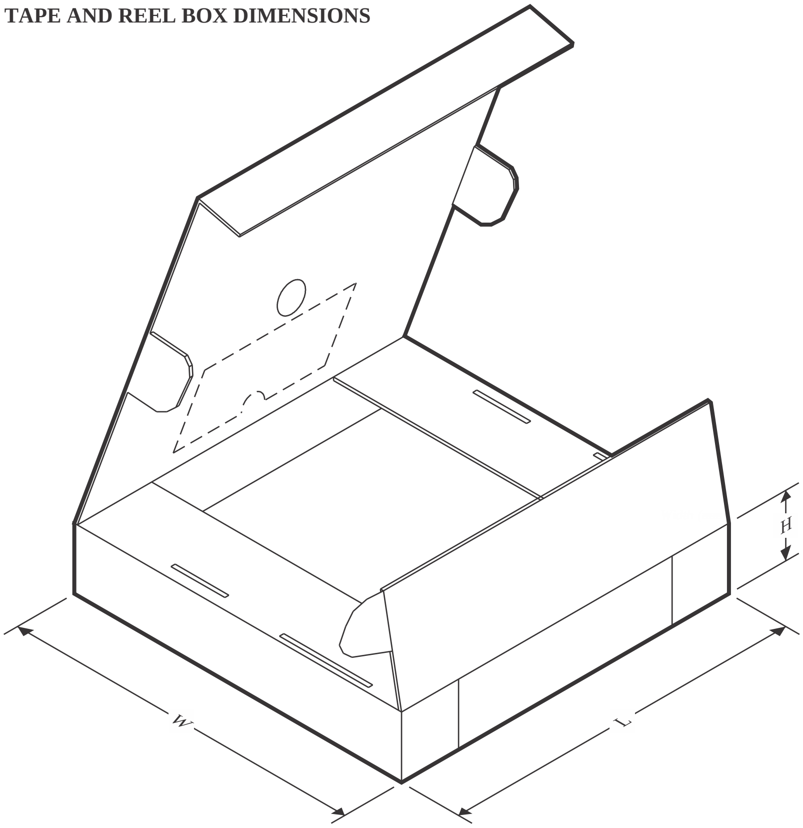
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A2009PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2009PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2009PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A20105PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A2011PYCKR	DSBGA	YCK	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A2011PYCKR	DSBGA	YCK	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A2012PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2012PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2012PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2012PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A2012PYCJR	DSBGA	YCJ	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A2012PYCJR	DSBGA	YCJ	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A2015PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2015PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2015PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A201825PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A201825PDQNR	X2SON	DQN	4	3000	178.0	8.4	1.13	1.13	0.53	4.0	8.0	Q2
TPS7A20185PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A20185PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A20185PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A20185PDQNR	X2SON	DQN	4	3000	178.0	8.4	1.13	1.13	0.53	4.0	8.0	Q2
TPS7A20185PYCKR	DSBGA	YCK	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A2018PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2018PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2018PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2018PDQNR	X2SON	DQN	4	3000	178.0	8.4	1.13	1.13	0.53	4.0	8.0	Q2
TPS7A2018PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A2018PDQNRM3	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A2018PYCKR	DSBGA	YCK	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A2018PYCKR	DSBGA	YCK	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A2020PYCKR	DSBGA	YCK	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A2020PYCKR	DSBGA	YCK	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A2022PYCKR	DSBGA	YCK	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A2022PYCKR	DSBGA	YCK	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A2024PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2024PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2024PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2025PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2025PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2025PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2025PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A2025PYCJR	DSBGA	YCJ	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A2025PYCJR	DSBGA	YCJ	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A2027PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A2027PYCJR	DSBGA	YCJ	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A2027PYCJR	DSBGA	YCJ	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A20285PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A20285PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A20285PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A20285PYCKR	DSBGA	YCK	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A2028PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2028PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A2028PDQNRM3	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A2028PYCJR	DSBGA	YCJ	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A2028PYCJR	DSBGA	YCJ	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A2028PYCKR	DSBGA	YCK	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A2028PYCKR	DSBGA	YCK	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A2029PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A2030PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2030PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2030PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2030PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A2031PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS7A2032PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2032PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS7A2033PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2033PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A2033PDQNR	X2SON	DQN	4	3000	178.0	8.4	1.13	1.13	0.53	4.0	8.0	Q2
TPS7A2033PDQNRM3	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A2033PYCJR	DSBGA	YCJ	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A2033PYCJR	DSBGA	YCJ	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A2036PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS7A2036PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2036PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A2040PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A2042PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2042PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A2045PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2045PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A2050PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2050PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2050PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A2050PDQNRM3	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A2050PYCKR	DSBGA	YCK	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A2050PYCKR	DSBGA	YCK	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A2055PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS7A2055PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A2009PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2009PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2009PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TPS7A20105PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TPS7A2011PYCKR	DSBGA	YCK	4	12000	182.0	182.0	20.0
TPS7A2011PYCKR	DSBGA	YCK	4	12000	182.0	182.0	20.0
TPS7A2012PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2012PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2012PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2012PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TPS7A2012PYCJR	DSBGA	YCJ	4	12000	182.0	182.0	20.0
TPS7A2012PYCJR	DSBGA	YCJ	4	12000	210.0	185.0	35.0
TPS7A2015PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2015PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2015PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TPS7A201825PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A201825PDQNR	X2SON	DQN	4	3000	205.0	200.0	33.0
TPS7A20185PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A20185PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A20185PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A20185PDQNR	X2SON	DQN	4	3000	205.0	200.0	33.0
TPS7A20185PYCKR	DSBGA	YCK	4	12000	182.0	182.0	20.0
TPS7A2018PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2018PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2018PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2018PDQNR	X2SON	DQN	4	3000	205.0	200.0	33.0
TPS7A2018PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A2018PDQNRM3	X2SON	DQN	4	3000	210.0	185.0	35.0
TPS7A2018PYCKR	DSBGA	YCK	4	12000	182.0	182.0	20.0
TPS7A2018PYCKR	DSBGA	YCK	4	12000	182.0	182.0	20.0
TPS7A2020PYCKR	DSBGA	YCK	4	12000	182.0	182.0	20.0
TPS7A2020PYCKR	DSBGA	YCK	4	12000	182.0	182.0	20.0
TPS7A2022PYCKR	DSBGA	YCK	4	12000	182.0	182.0	20.0
TPS7A2022PYCKR	DSBGA	YCK	4	12000	182.0	182.0	20.0
TPS7A2024PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2024PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2024PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2025PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2025PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2025PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2025PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TPS7A2025PYCJR	DSBGA	YCJ	4	12000	210.0	185.0	35.0
TPS7A2025PYCJR	DSBGA	YCJ	4	12000	182.0	182.0	20.0
TPS7A2027PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TPS7A2027PYCJR	DSBGA	YCJ	4	12000	182.0	182.0	20.0
TPS7A2027PYCJR	DSBGA	YCJ	4	12000	210.0	185.0	35.0
TPS7A20285PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A20285PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A20285PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TPS7A20285PYCKR	DSBGA	YCK	4	12000	182.0	182.0	20.0
TPS7A2028PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2028PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TPS7A2028PDQNRM3	X2SON	DQN	4	3000	210.0	185.0	35.0
TPS7A2028PYCJR	DSBGA	YCJ	4	12000	210.0	185.0	35.0
TPS7A2028PYCJR	DSBGA	YCJ	4	12000	182.0	182.0	20.0
TPS7A2028PYCKR	DSBGA	YCK	4	12000	182.0	182.0	20.0
TPS7A2028PYCKR	DSBGA	YCK	4	12000	182.0	182.0	20.0
TPS7A2029PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TPS7A2030PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2030PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2030PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0

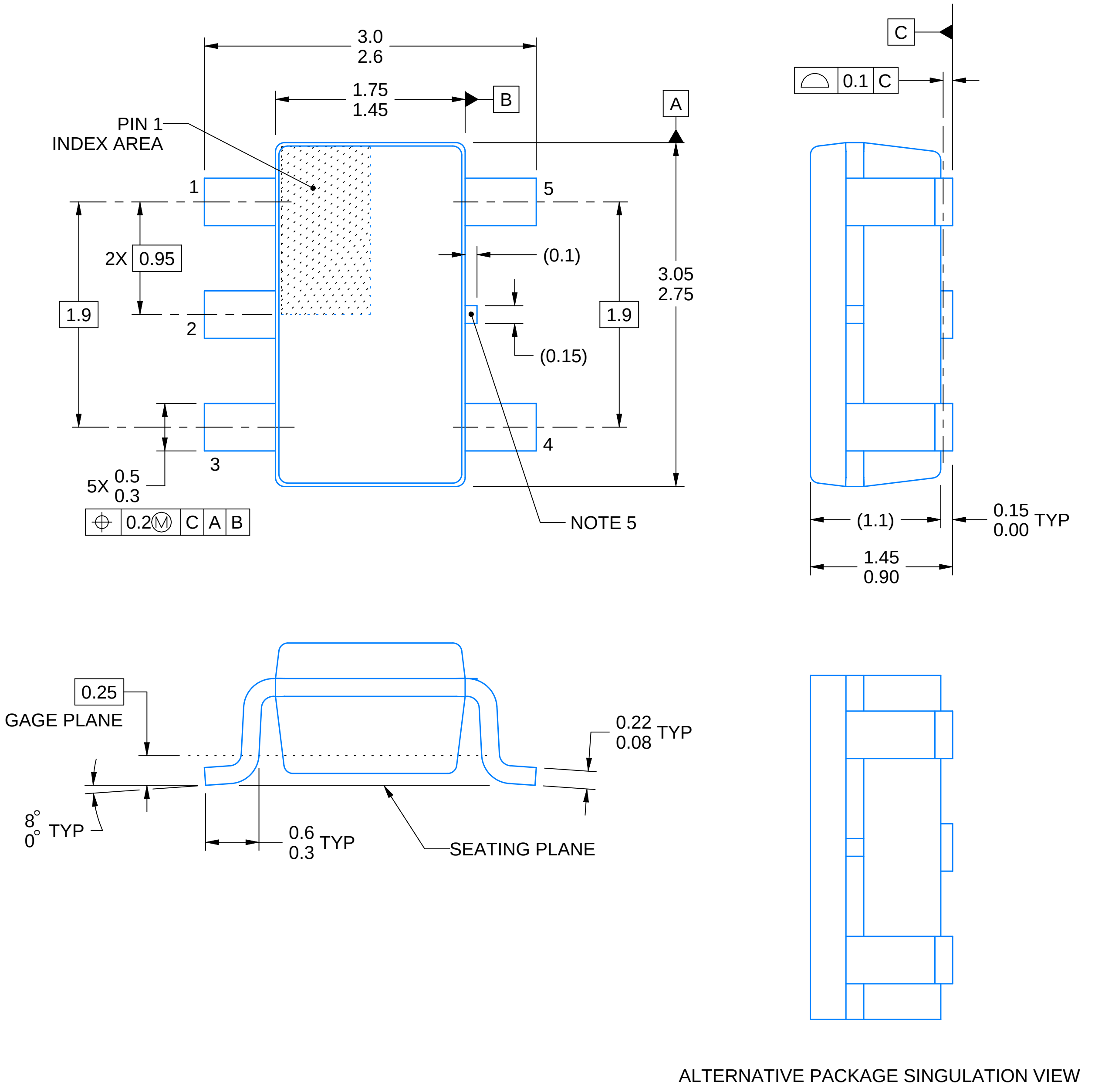
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A2030PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TPS7A2031PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS7A2032PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2032PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS7A2033PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2033PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A2033PDQNR	X2SON	DQN	4	3000	205.0	200.0	33.0
TPS7A2033PDQNRM3	X2SON	DQN	4	3000	210.0	185.0	35.0
TPS7A2033PYCJR	DSBGA	YCJ	4	12000	210.0	185.0	35.0
TPS7A2033PYCJR	DSBGA	YCJ	4	12000	182.0	182.0	20.0
TPS7A2036PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS7A2036PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2036PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TPS7A2040PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A2042PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2042PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TPS7A2045PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2045PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TPS7A2050PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2050PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2050PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TPS7A2050PDQNRM3	X2SON	DQN	4	3000	210.0	185.0	35.0
TPS7A2050PYCKR	DSBGA	YCK	4	12000	182.0	182.0	20.0
TPS7A2050PYCKR	DSBGA	YCK	4	12000	182.0	182.0	20.0
TPS7A2055PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS7A2055PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0

DBV0005A

PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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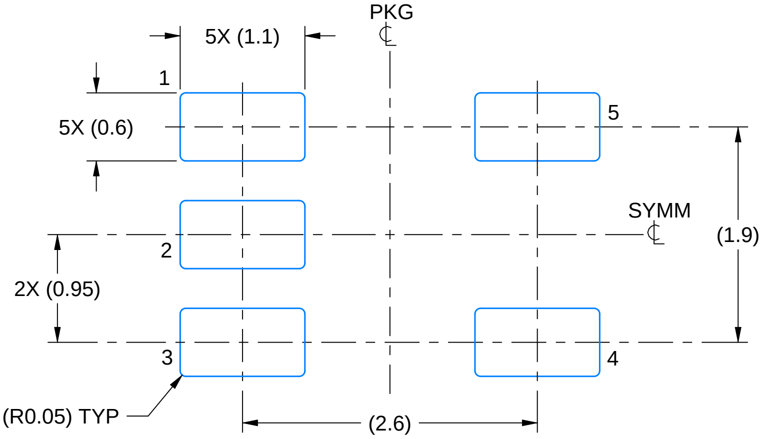
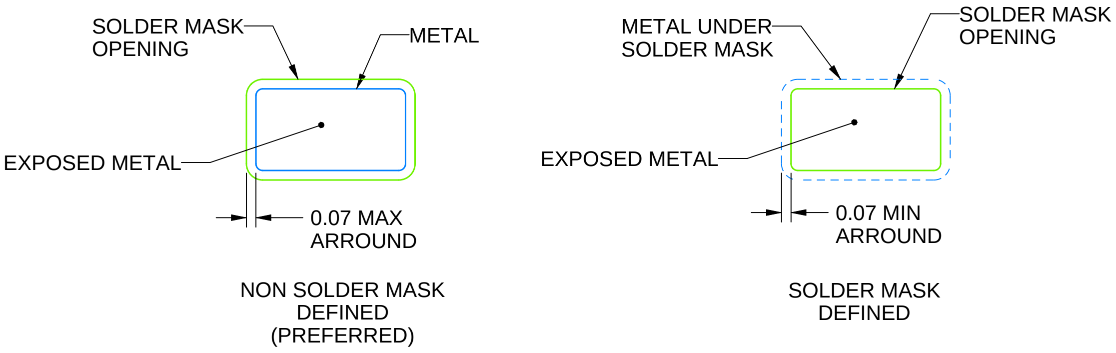
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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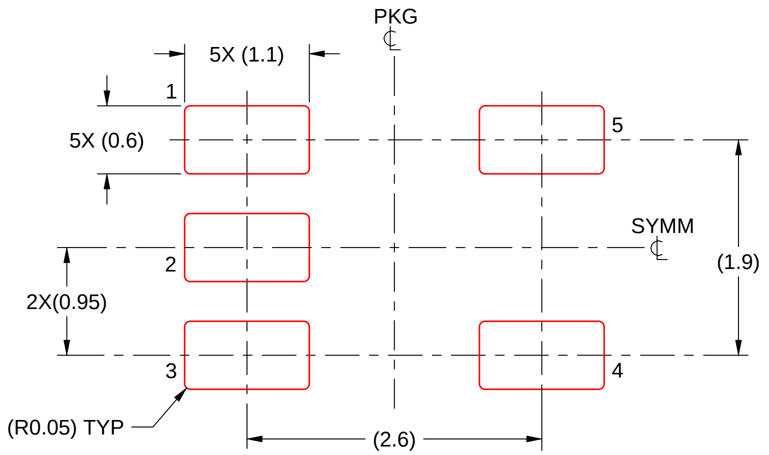
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

NOTES: (continued)

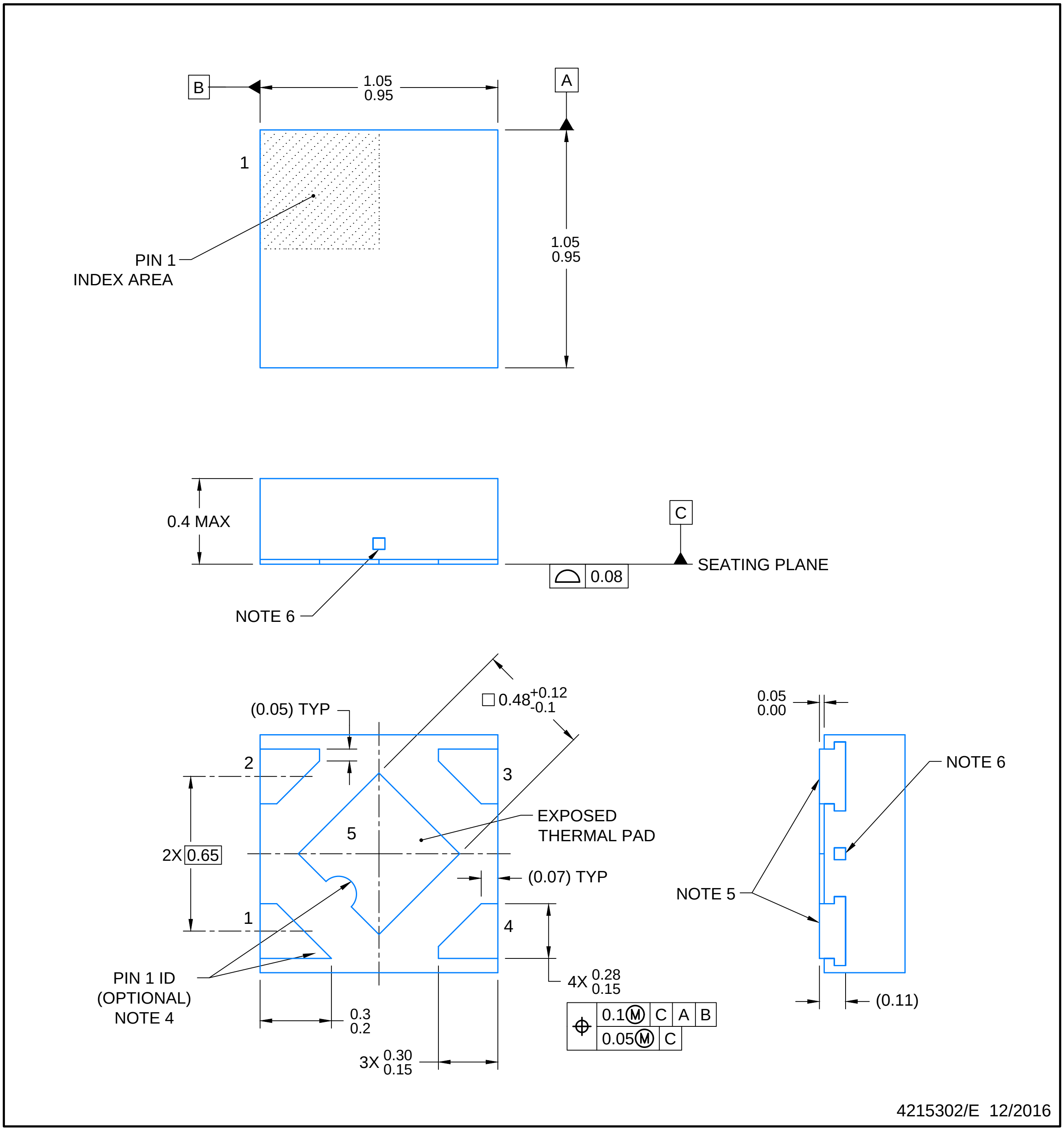
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DQN 4

X2SON - 0.4 mm max height

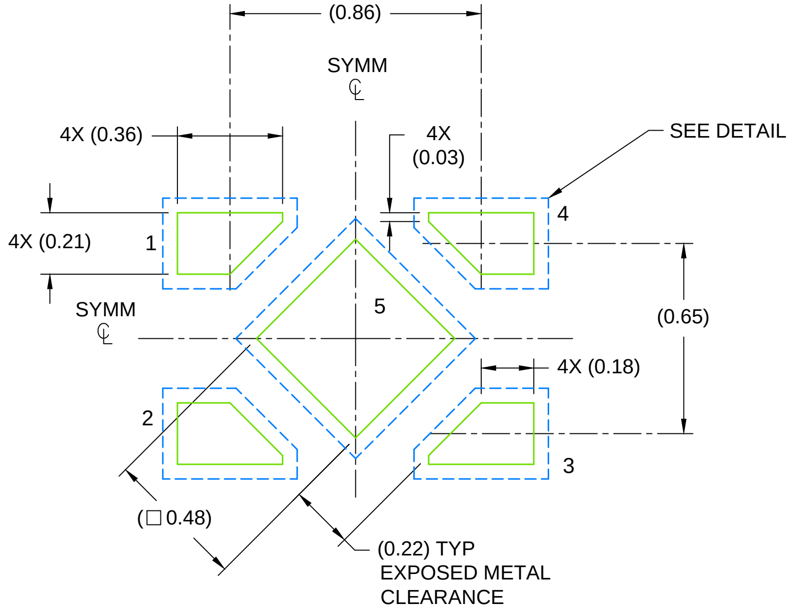
PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

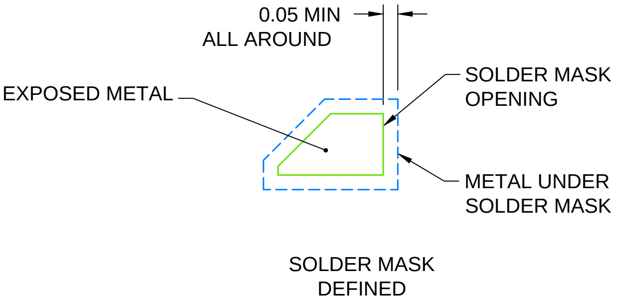


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.
5. Shape of exposed side leads may differ.
6. Number and location of exposed tie bars may vary.



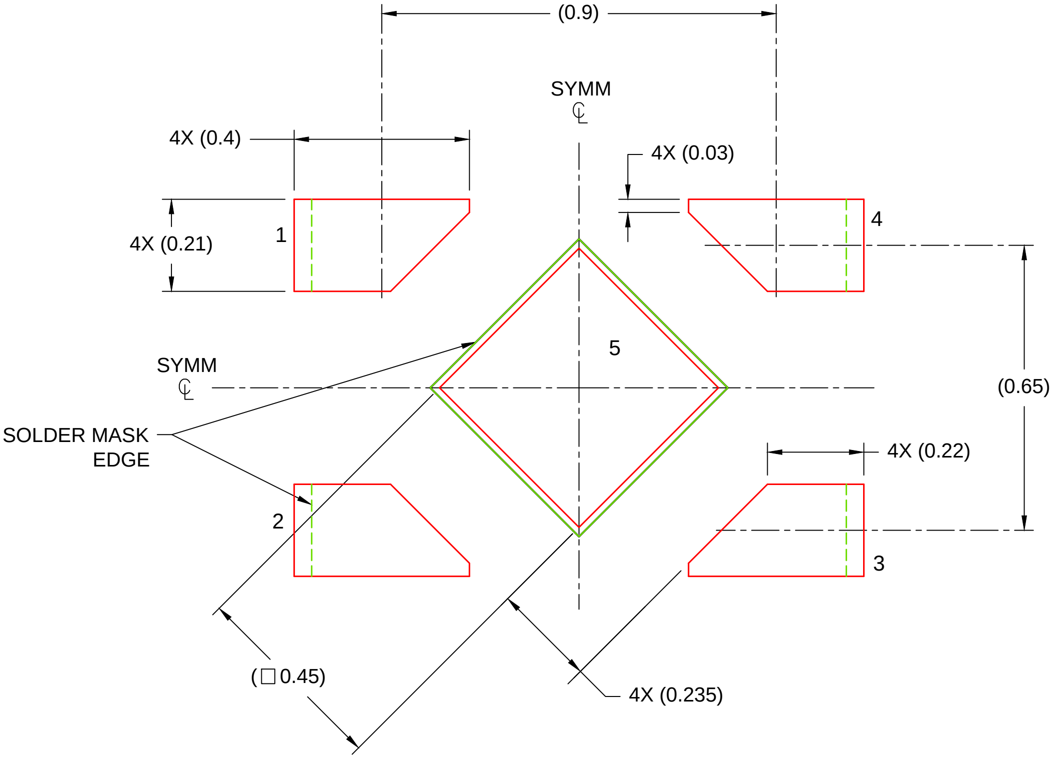
LAND PATTERN EXAMPLE
SCALE: 40X



SOLDER MASK DETAIL

NOTES: (continued)

7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
8. If any vias are implemented, it is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1mm THICK STENCIL

EXPOSED PAD
88% PRINTED SOLDER COVERAGE BY AREA
SCALE: 60X

4215302/E 12/2016

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

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