

# TPS7B81 150mA、40V、超低 $I_Q$ 、低ドロップアウト・レギュレータ

## 1 特長

- 広い入力電圧範囲：3V～40V
- 出力電流：150mA
- 非常に低い静止電流 ( $I_Q$ )
  - 軽負荷時: 2.7 $\mu$ A (標準値)
  - 軽負荷時: 4.5 $\mu$ A (最大値)
- 精度：ライン、負荷、温度の範囲全体にわたって 1.5% の誤差
- ドロップアウト電圧：100mA で 180mV (標準値)
- 広いイネーブル電圧範囲：2V～ $V_{IN}$  (最高 40V)
- 入力電圧過渡の許容値：45V
- 5V および 3.3V 固定出力電圧オプション
- 電流制限およびサーマル・シャットダウン保護
- 広い範囲のコンデンサで安定 (1 $\mu$ F～200 $\mu$ F) <sup>(1)</sup>
- 接合部温度範囲：-40°C～+150°C
- 熱性能の高いパッケージ
  - DGN (8 ピン HVSSOP)、 $R_{\theta JA} = 63.9^\circ\text{C/W}$
  - DRV (6 ピン WSON)、 $R_{\theta JA} = 72.8^\circ\text{C/W}$

(1) 出力コンデンサの要件については、「推奨動作条件」表を参照してください。

## 2 アプリケーション

- 煙 / 熱検知器
- サーモスタット
- モーション検出器 (PIR、uWave など)
- コードレス電動工具
- 家電機器用バッテリー・パック
- モータ・ドライブ

## 3 説明

TPS7B81 は、最高 40V の入力電圧で動作し、最大 150mA の電流を供給できる低ドロップアウト (LDO) リニア・レギュレータです。軽負荷時の静止電流がわずかに 2.7 $\mu$ A であるため、入力電源電圧範囲の広い設計や、スタンバイ時消費電力が非常に小さいことが要求される多セル・バッテリー駆動アプリケーションに最適です。45V の過渡電圧に耐えられるので、誘導性キックバックが発生する可能性があるアプリケーションでヘッドルームが増え、電圧抑制のための外付け回路を減らすことができます。

TPS7B81 には短絡および過電流制限機能が内蔵されているため、フォルト状態でもシステムを保護できます。スタンバイ時の消費電力が小さいことに加えて、軽負荷時のドロップアウト電圧が非常に小さいため、消耗したバッテリーで動作する場合でもレギュレーションを維持できます。

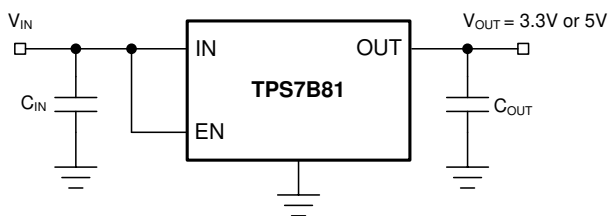
TPS7B81 は、熱的に強化された 8 ピンの HVSSOP および 6 ピンの WSON パッケージで供給されます。どちらのパッケージも熱伝導性が高くサイズが小さいため、小型の設計が可能であり、電動工具、モーター・ドライブ・モジュール、バッテリー・パックなど、スペースの制約が厳しいアプリケーションに適しています。

### 製品情報<sup>(1)</sup>

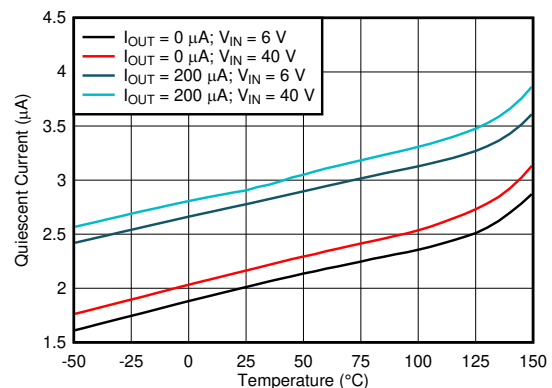
型番	パッケージ	本体サイズ (公称)
TPS7B81	HVSSOP (8)	3.00mm×3.00mm
	WSON (6)	2.00mm × 2.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

### 代表的なアプリケーションの回路図



### 静止電流と周囲温度の関係 ( $V_{OUT} = 3.3V$ )



## 目次

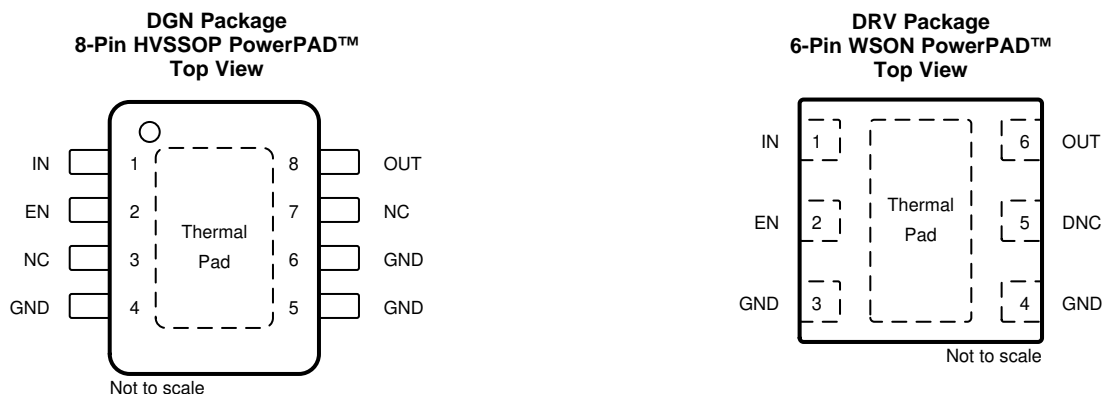
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## 4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

日付	リビジョン	注
2020 年 4 月	*	初版

## 5 Pin Configuration and Functions



### Pin Functions

NAME	PIN NO.		I/O	DESCRIPTION
	NO.			
	DGN	DRV		
DNC	—	5	—	Do not connect to a biased voltage. Tie this pin to ground or leave floating.
EN	2	2	I	Enable input pin. Drive EN greater than $V_{IH}$ to turn on the regulator. Drive EN less than $V_{IL}$ to put the low-dropout (LDO) into shutdown mode.
GND	4, 5, 6	3,4	—	Ground reference
IN	1	1	I	Input power-supply pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to ground as listed in the <a href="#">Recommended Operating Conditions</a> table and the <a href="#">Input Capacitor</a> section. Place the input capacitor as close to the output of the device as possible.
NC	3, 7	—	—	Not internally connected
OUT	8	6	O	Regulated output voltage pin. A capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger ceramic capacitor from OUT to ground; see the <a href="#">Recommended Operating Conditions</a> table and the <a href="#">Output Capacitor</a> section. Place the output capacitor as close to output of the device as possible.
Thermal pad			—	Connect the thermal pad to a large-area GND plane for improved thermal performance.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)<sup>(1)(2)</sup>

		MIN	MAX	UNIT
V <sub>IN</sub>	Unregulated input voltage <sup>(3)</sup>	-0.3	45	V
V <sub>EN</sub>	Enable input voltage <sup>(3)</sup>	-0.3	V <sub>IN</sub>	V
V <sub>OUT</sub>	Regulated output	-0.3	7	V
T <sub>J</sub>	Junction temperature	-40	150	°C
T <sub>stg</sub>	Storage temperature	-40	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND.
- (3) Absolute maximum voltage, can withstand 45 V for 200 ms.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±500	

- (1) JEDEC document JEP155 states that 2-kV HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 500-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>IN</sub>	Unregulated input voltage	3	40	V
V <sub>EN</sub>	Enable input voltage	0	V <sub>IN</sub>	V
C <sub>OUT</sub>	Output capacitor requirements <sup>(1)</sup>	1	200	μF
ESR	Output capacitor ESR requirements <sup>(2)</sup>	0.001	5	Ω
T <sub>A</sub>	Ambient temperature	-40	125	°C
T <sub>J</sub>	Junction temperature	-40	150	°C

- (1) The output capacitance range specified in the table is the effective capacitance value.
- (2) Relevant ESR value at f = 10 kHz

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS7B81		UNIT
		DGN (HVSSOP)	DRV (WSON)	
		8 PINS	6 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	63.9	72.8	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	50.2	85.8	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	22.6	37.4	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	1.8	2.7	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	22.3	37.3	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	12.1	13.8	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

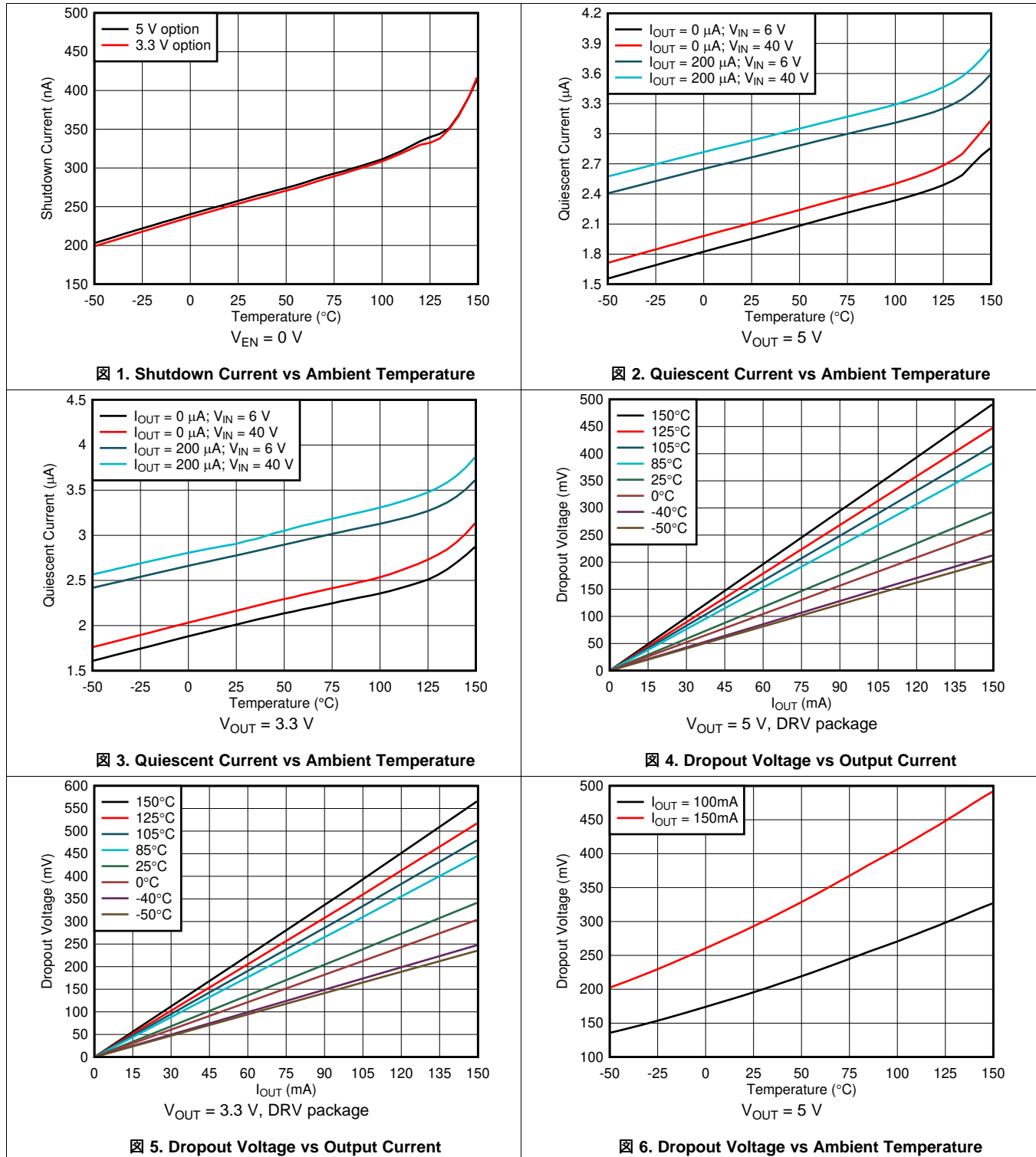
## 6.5 Electrical Characteristics

over operating ambient temperature range,  $T_J = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ,  $V_{IN} = 14\text{ V}$ , and  $10\text{-}\mu\text{F}$  ceramic output capacitor (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>SUPPLY VOLTAGE AND CURRENT (IN)</b>							
$V_{IN}$	Input voltage			$V_{OUT(Nom)} + V_{(Dropout)}$		40	V
$I_{(SD)}$	Shutdown current	$EN = 0\text{ V}$		0.3	1		$\mu\text{A}$
$I_{(Q)}$	Quiescent current	$V_{IN} = 6\text{ V to }40\text{ V}, EN \geq 2\text{ V}, I_{OUT} = 0\text{ mA}$		1.9	3.5		$\mu\text{A}$
		$V_{IN} = 6\text{ V to }40\text{ V}, EN \geq 2\text{ V}, I_{OUT} = 0.2\text{ mA}$	DGN package	2.7	6.5		
			DRV package	2.7	4.5		
$V_{(IN, UVLO)}$	$V_{IN}$ undervoltage detection	Ramp $V_{IN}$ down until the output turns off				2.7	V
		Hysteresis				200	mV
<b>ENABLE INPUT (EN)</b>							
$V_{IL}$	Logic-input low level					0.7	V
$V_{IH}$	Logic-input high level			2			V
$I_{EN}$	Enable current			10			nA
<b>REGULATED OUTPUT (OUT)</b>							
$V_{OUT}$	Regulated output	$V_{IN} = V_{OUT} + V_{(Dropout)}$ to $40\text{ V}$ , $I_{OUT} = 1\text{ mA to }150\text{ mA}$		-1.5%		1.5%	
$V_{(Line-Reg)}$	Line regulation	$V_{IN} = 6\text{ V to }40\text{ V}, I_{OUT} = 10\text{ mA}$				10	mV
$V_{(Load-Reg)}$	Load regulation	$V_{IN} = 14\text{ V}, I_{OUT} = 1\text{ mA to }150\text{ mA}$		DGN package		20	mV
				DRV package		10	
$V_{(Dropout)}$	Dropout voltage	$V_{OUT} = 5\text{ V}$	$I_{OUT} = 150\text{ mA}$	DGN package		270	mV
				DRV package		325	
			$I_{OUT} = 100\text{ mA}$	DGN package		180	
		DRV package		200			
		$V_{OUT} = 3.3\text{ V}$	$I_{OUT} = 150\text{ mA}$	DGN package		650	
				DRV package		345	
$I_{OUT} = 100\text{ mA}$					255		
$I_{OUT}$	Output current	$V_{OUT}$ in regulation, $V_{IN} = 7\text{ V}$ for the fixed 5-V option, $V_{IN} = 5.8\text{ V}$ for the fixed 3.3-V option		0		150	mA
$I_{(CL)}$	Output current limit	$V_{OUT}$ short to $90\% \times V_{OUT}$		180	510	690	mA
PSRR	Power-supply ripple rejection	$V_{(Ripple)} = 0.5\text{ V}_{PP}$ , $I_{OUT} = 10\text{ mA}$ , frequency = $100\text{ Hz}$ , $C_{OUT} = 2.2\text{ }\mu\text{F}$				60	dB
<b>OPERATING TEMPERATURE RANGE</b>							
$T_{(SD)}$	Junction shutdown temperature					175	$^{\circ}\text{C}$
$T_{(HYST)}$	Hysteresis of thermal shutdown					20	$^{\circ}\text{C}$

## 6.6 Typical Characteristics

at  $T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ,  $V_{IN} = 14\text{ V}$ , and  $V_{EN} \geq 2\text{ V}$  (unless otherwise noted)



Typical Characteristics (continued)

at  $T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ,  $V_{IN} = 14\text{ V}$ , and  $V_{EN} \geq 2\text{ V}$  (unless otherwise noted)

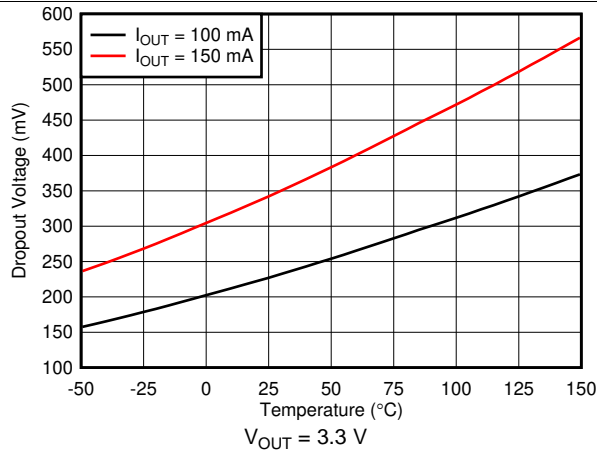


Figure 7. Dropout Voltage vs Ambient Temperature

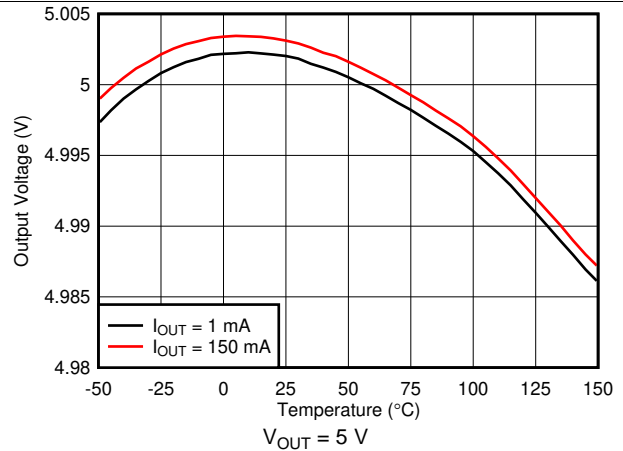


Figure 8. Output Voltage vs Ambient Temperature

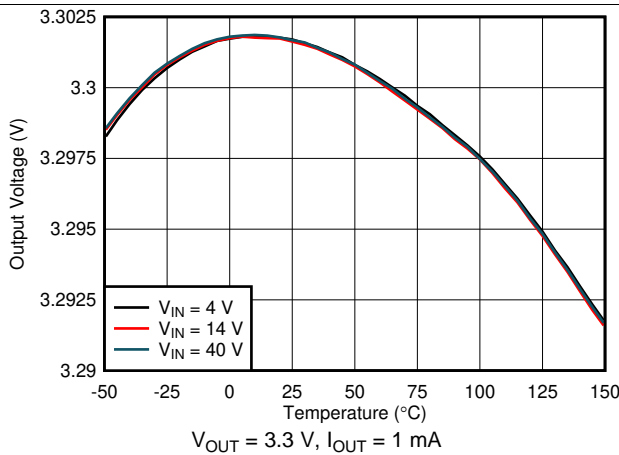


Figure 9. Output Voltage vs Ambient Temperature

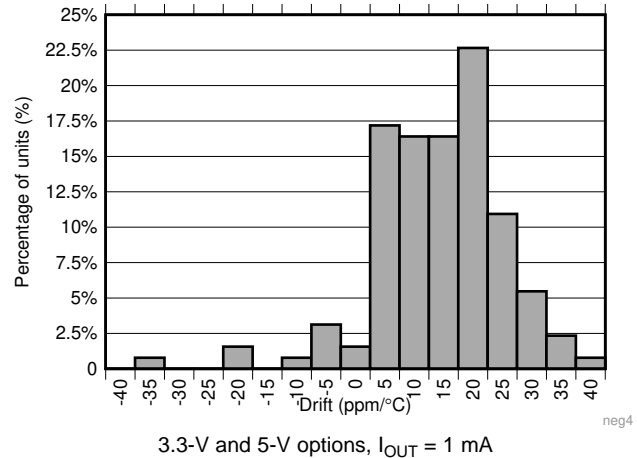


Figure 10. Temperature Drift Histogram (-40°C to +25°C)

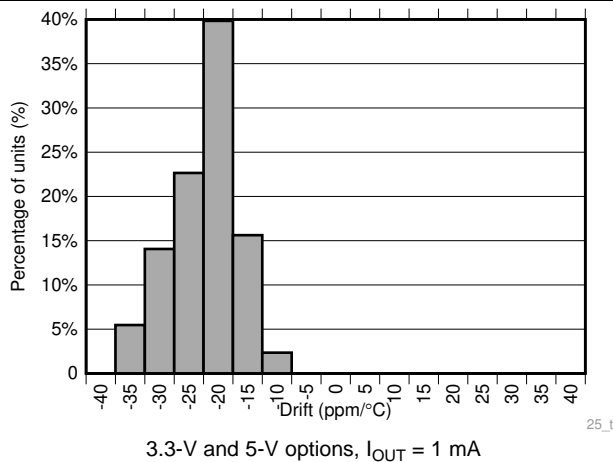


Figure 11. Temperature Drift Histogram (25°C to 150°C)

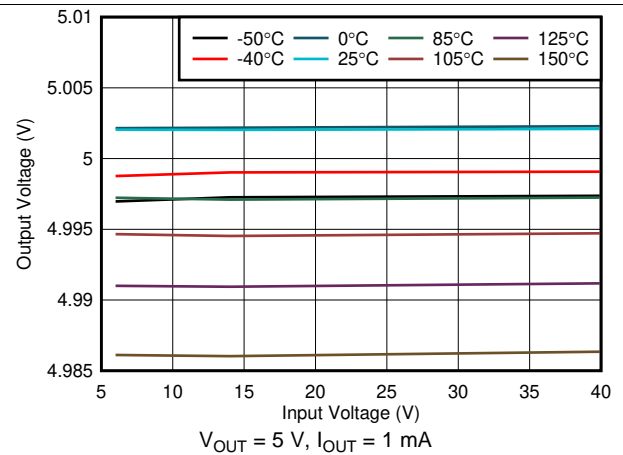
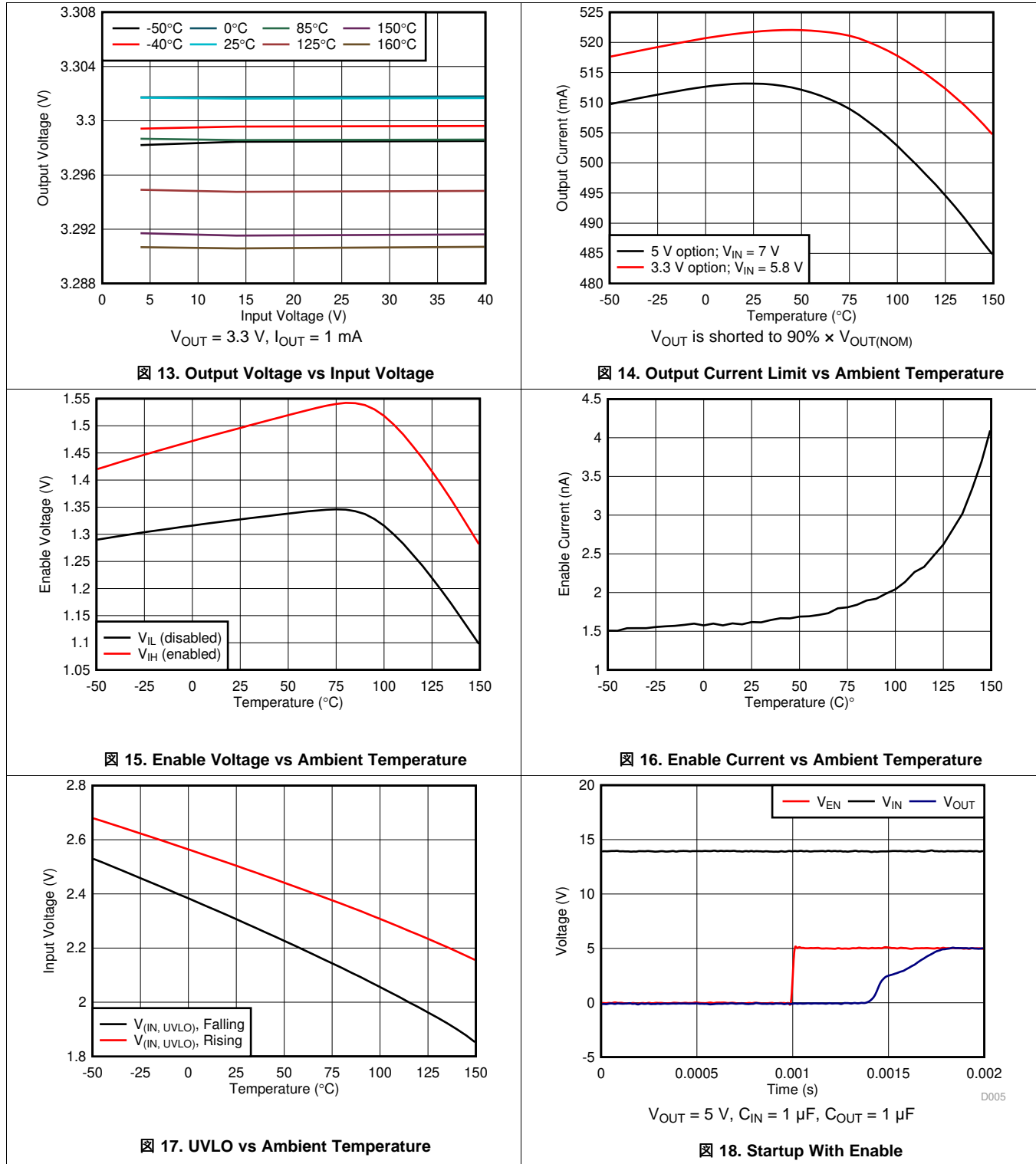


Figure 12. Output Voltage vs Input Voltage

### Typical Characteristics (continued)

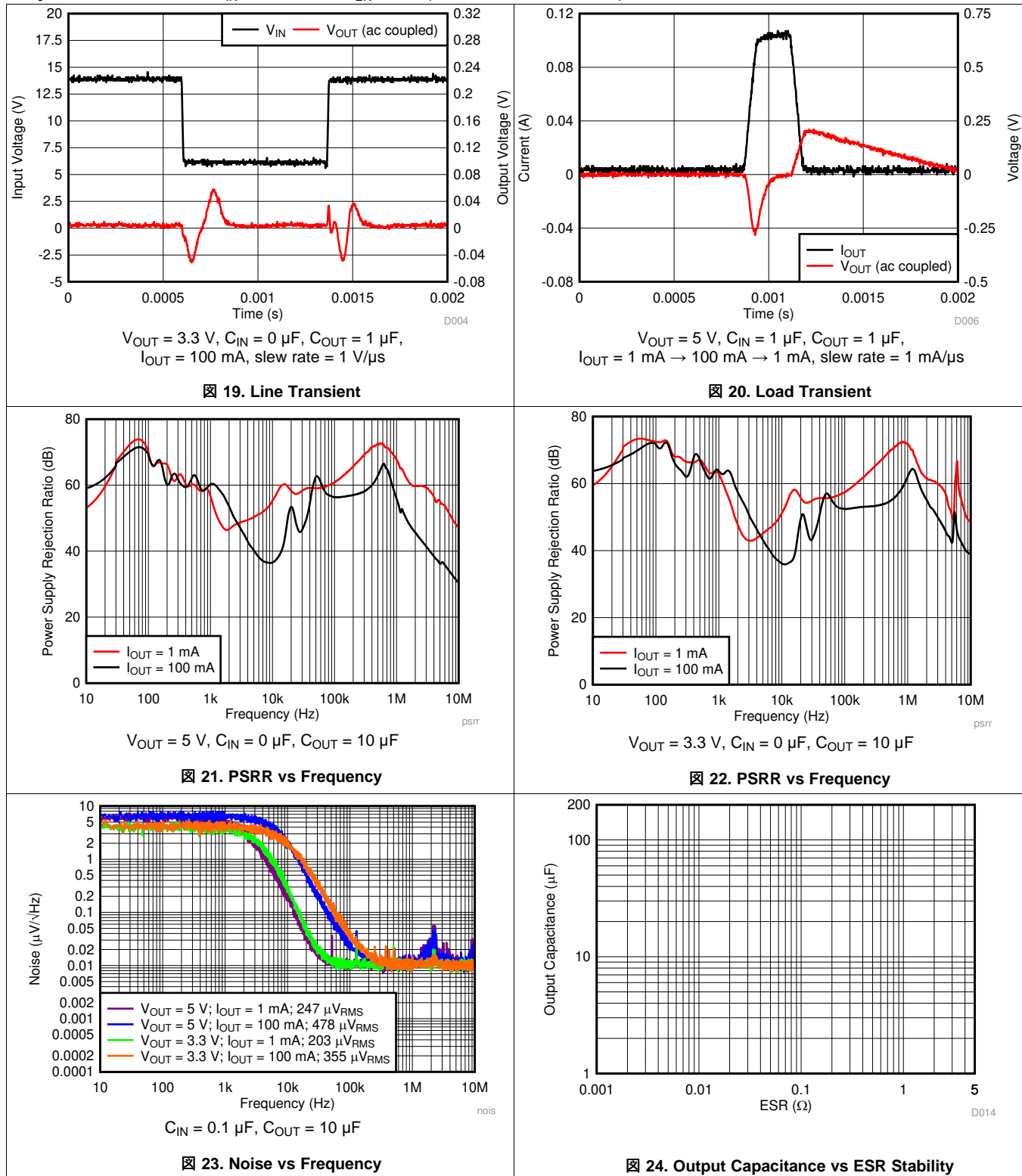
at  $T_J = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ,  $V_{IN} = 14\text{ V}$ , and  $V_{EN} \geq 2\text{ V}$  (unless otherwise noted)





Typical Characteristics (continued)

at  $T_J = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ,  $V_{IN} = 14\text{ V}$ , and  $V_{EN} \geq 2\text{ V}$  (unless otherwise noted)

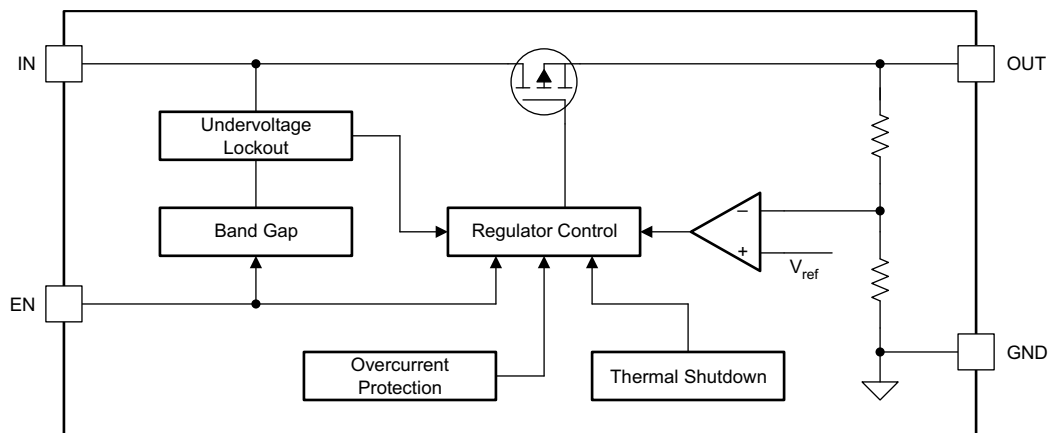


## 7 Detailed Description

### 7.1 Overview

The TPS7B81 is a 40-V, 150-mA, low-dropout (LDO) linear regulator with ultra-low quiescent current. This voltage regulator consumes only 3  $\mu$ A of quiescent current at light load, and is quite suitable for always-on applications.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

#### 7.3.1 Device Enable (EN)

The EN pin is a high-voltage-tolerant pin. A high input activates the device and turns the regulation on. Connect this pin to an external microcontroller or a digital circuit to enable and disable the device, or connect to the IN pin for self-bias applications.

#### 7.3.2 Undervoltage Shutdown

This device has an integrated undervoltage lockout (UVLO) circuit to shut down the output if the input voltage ( $V_{IN}$ ) falls below an internal UVLO threshold ( $V_{(UVLO)}$ ). This feature ensures that the regulator does not latch into an unknown state during low-input-voltage conditions. If the input voltage has a negative transient that drops below the UVLO threshold and recovers, the regulator shuts down and powers up with a normal power-up sequence when the input voltage is above the required level.

#### 7.3.3 Current Limit

This device features current-limit protection to keep the device in a safe operating area when an overload or output short-to-ground condition occurs. This feature protects the device from excessive power dissipation. For example, during a short-circuit condition on the output, the fault protection limits the current through the pass element to  $I_{(LIM)}$  to protect the device from excessive power dissipation.

#### 7.3.4 Thermal Shutdown

This device incorporates a thermal shutdown (TSD) circuit as protection from overheating. For continuous normal operation, the junction temperature must not exceed the TSD trip point. If the junction temperature exceeds the TSD trip point, the output turns off. When the junction temperature falls below the TSD trip point minus the thermal shutdown hysteresis, the output turns on again.

## 7.4 Device Functional Modes

### 7.4.1 Operation With $V_{IN}$ Lower Than 3 V

The device normally operates with input voltages above 3 V. The device can also operate at lower input voltages; the maximum UVLO voltage is 2.7 V. The device does not operate at input voltages below the actual UVLO voltage.

### 7.4.2 Operation With $V_{IN}$ Larger Than 3 V

When  $V_{IN}$  is greater than 3 V, if  $V_{IN}$  is also higher than the output set value plus the device dropout voltage,  $V_{OUT}$  is equal to the set value. Otherwise,  $V_{OUT}$  is equal to  $V_{IN}$  minus the dropout voltage.

**表 1. Device Functional Mode Comparison**

OPERATING MODE	PARAMETER			
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{(Dropout)}$ and $V_{IN} \geq 3\text{ V}$	$V_{EN} > V_{IH}$	$I_{OUT} < I_{CL}$	$T_J < 160^\circ\text{C}$
Dropout mode	$3\text{ V} \leq V_{IN} < V_{OUT(nom)} + V_{(Dropout)}$	$V_{EN} > V_{IH}$	$I_{OUT} < I_{CL}$	$T_J < 160^\circ\text{C}$
Disabled mode (any true condition disables the device)	$V_{IN} < V_{(IN, UVLO)}$	$V_{EN} < V_{IL}$	—	$T_J > 160^\circ\text{C}$

## 8 Application and Implementation

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The TPS7B81 is a 150-mA, 40-V, low-dropout (LDO) linear regulator with ultralow quiescent current. The PSpice transient model is available for download on the [product folder](#) and can be used to evaluate the basic functionality of the device.

#### 8.1.1 Power Dissipation

Circuit reliability demands that proper consideration is given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free as possible of other heat-generating devices that cause added thermal stresses.

As a first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. [式 1](#) approximates  $P_D$ :

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (1)$$

An important note is that power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the device allows for maximum efficiency across a wide range of output voltages.

The main heat conduction path for the device is through the thermal pad on the package. As such, the thermal pad must be soldered to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to any inner plane areas or to a bottom-side copper plane.

The maximum power dissipation determines the maximum allowable junction temperature ( $T_J$ ) for the device. According to [式 2](#), power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ( $R_{\theta JA}$ ) of the combined PCB, device package, and the temperature of the ambient air ( $T_A$ ). This equation is rearranged for output current in [式 3](#).

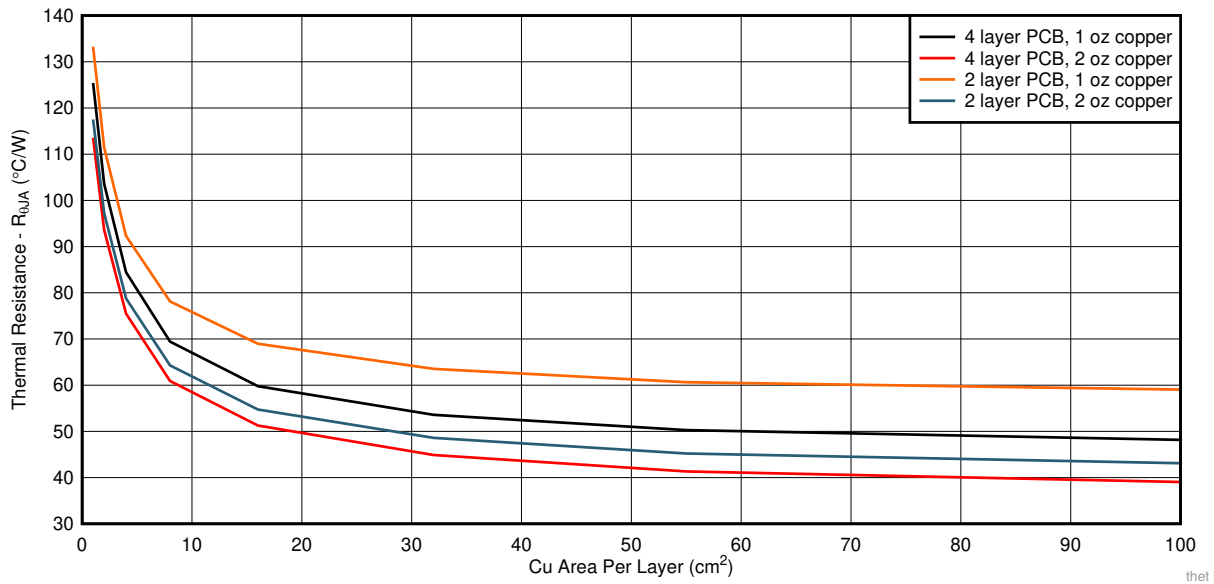
$$T_J = T_A + R_{\theta JA} \times P_D \quad (2)$$

$$I_{OUT} = (T_J - T_A) / [R_{\theta JA} \times (V_{IN} - V_{OUT})] \quad (3)$$

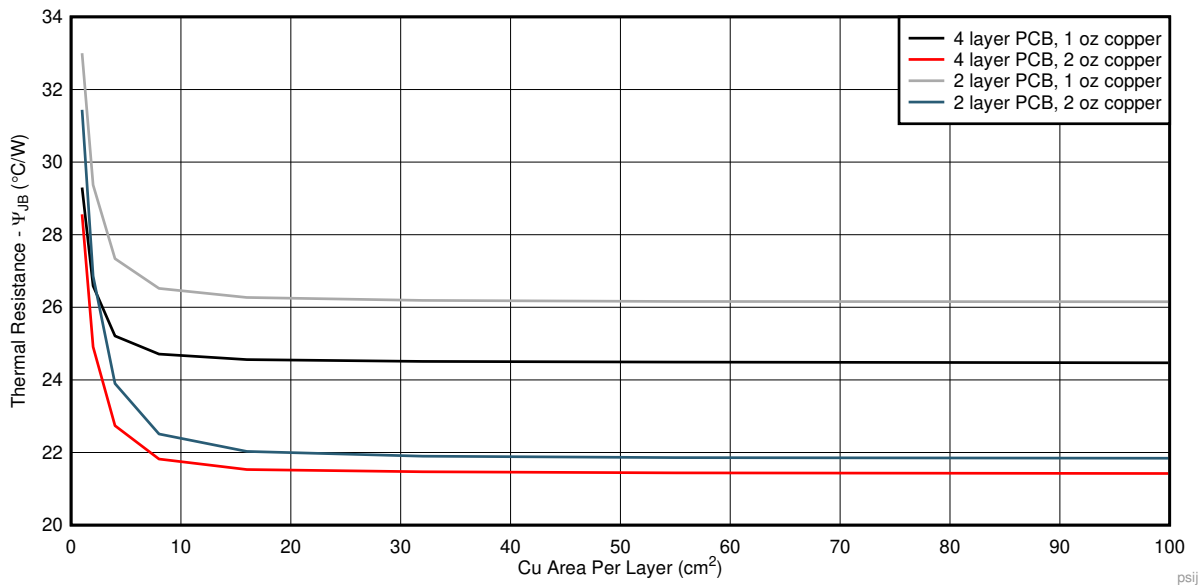
Unfortunately, this thermal resistance ( $R_{\theta JA}$ ) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The  $R_{\theta JA}$  recorded in the [Thermal Information](#) table is determined by the JEDEC standard, PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance. For a well-designed thermal layout,  $R_{\theta JA}$  is actually the sum of the package junction-to-case (bottom) thermal resistance ( $R_{\theta JCbot}$ ) plus the thermal resistance contribution by the PCB copper.

[图 25](#) through [图 28](#) illustrate the functions of  $R_{\theta JA}$  and  $\psi_{JB}$  versus copper area and thickness. These plots are generated with a 101.6-mm x 101.6-mm x 1.6-mm PCB of two and four layers. For the four-layer board, inner planes use a 1-oz copper thickness. Outer layers are simulated with both 1-oz and 2-oz copper thicknesses. A 2 x 1 array of thermal vias with a 300- $\mu$ m drill diameter and a 25- $\mu$ m copper (Cu) plating is located beneath the thermal pad of the device. The thermal vias connect the top layer, the bottom layer and, in the case of the 4-layer board, the first inner GND plane. The copper plane of each layer is of an equal area.

Application Information (continued)

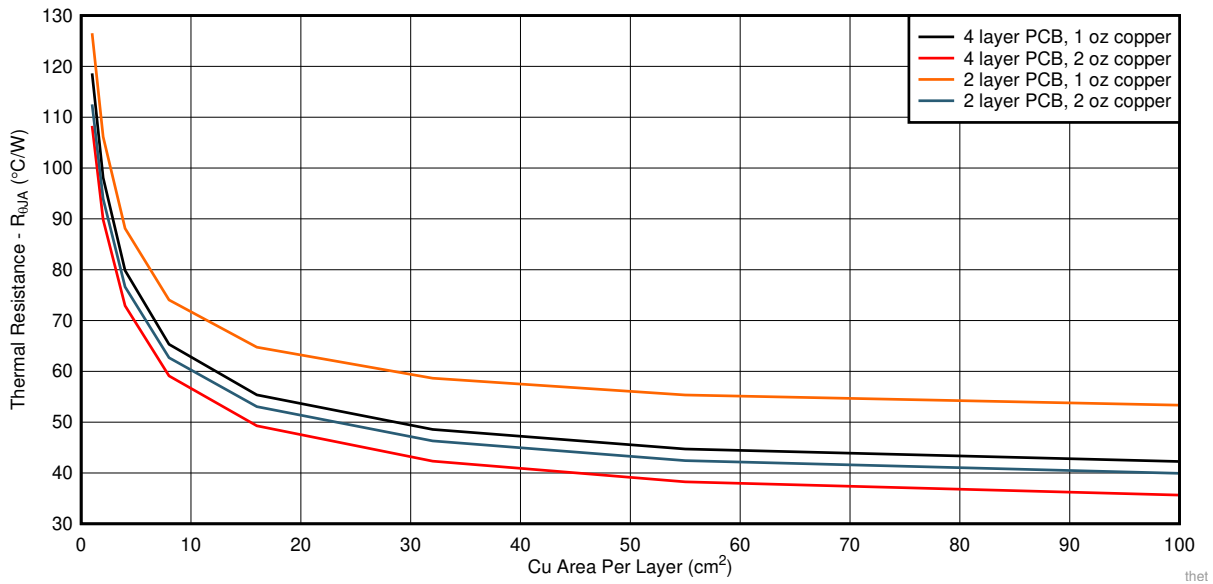


25.  $R_{\theta JA}$  versus Cu Area for the WSON (DRV) Package

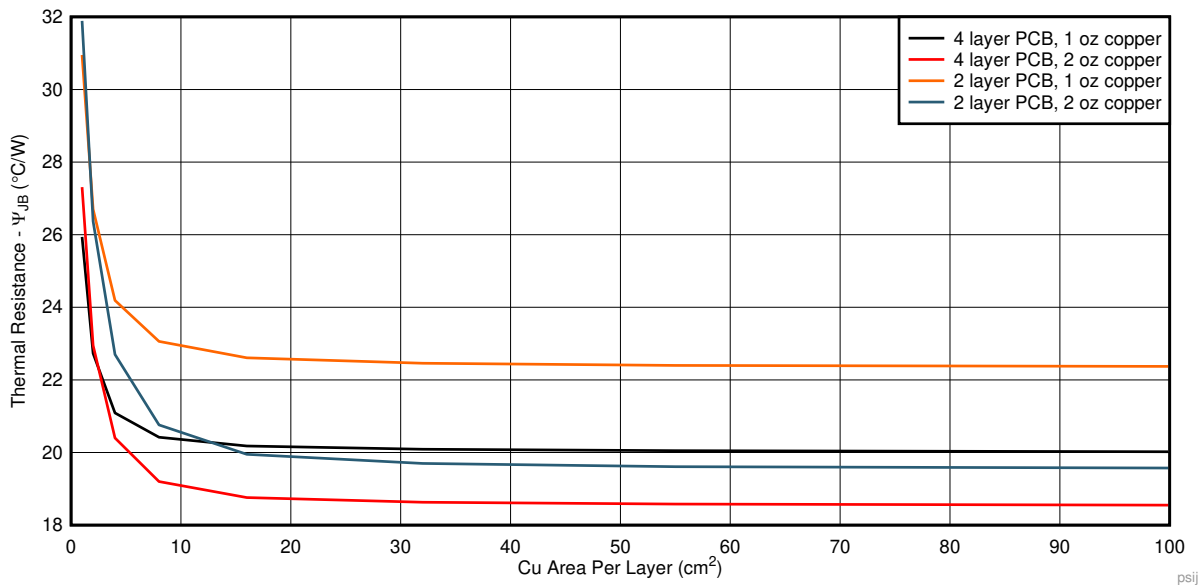


26.  $\psi_{JB}$  versus Cu Area for the WSON (DRV) Package

Application Information (continued)



27.  $R_{\theta JA}$  versus Cu Area for the HVSSOP (DGN) Package



28.  $\psi_{JB}$  versus Cu Area for the HVSSOP (DGN) Package

## Application Information (continued)

### 8.1.1.1 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi ( $\Psi$ ) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistance, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics ( $\Psi_{JT}$  and  $\Psi_{JB}$ ) are used in accordance with 式 4 and given in the *Thermal Information* table.

$$\Psi_{JT}: T_J = T_T + \Psi_{JT} \times P_D$$

$$\Psi_{JB}: T_J = T_B + \Psi_{JB} \times P_D$$

where:

- $P_D$  is the power dissipated as explained in 式 1
- $T_T$  is the temperature at the center-top of the device package
- $T_B$  is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

(4)

## 8.2 Typical Application

图 29 shows a typical application circuit for the TPS7B81. Different external component values can be used, depending on the end application. An application may require a larger output capacitor during fast load steps to prevent a large drop on the output voltage. TI recommends using a low-equivalent series resistance (ESR) ceramic capacitor with an X5R- or X7R-type dielectric.

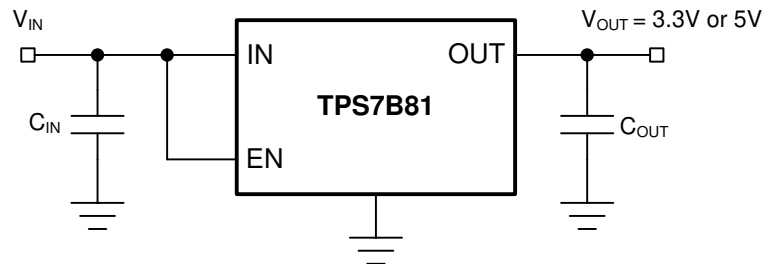


图 29. Typical Application Schematic

### 8.2.1 Design Requirements

Use the parameters listed in 表 2 for this design example.

表 2. Design Requirements Parameters

PARAMETER	VALUE
Input voltage range	3 V to 40 V
Output voltage	5 V or 3.3 V
Output current	150 mA maximum

### 8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
- Output voltage
- Output current

#### 8.2.2.1 Input Capacitor

Although an input capacitor is not required for stability, good analog design practice is to connect a 10- $\mu$ F to 22- $\mu$ F capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple rejection, and PSRR. The voltage rating must be greater than the maximum input voltage.

### 8.2.2.2 Output Capacitor

To ensure the stability of the TPS7B81, the device requires an output capacitor with a value in the range from 1  $\mu\text{F}$  to 200  $\mu\text{F}$  and with an ESR range between 0.001  $\Omega$  and 5  $\Omega$ . TI recommends selecting a ceramic capacitor with low ESR to improve the load transient response.

### 8.2.3 Application Curve

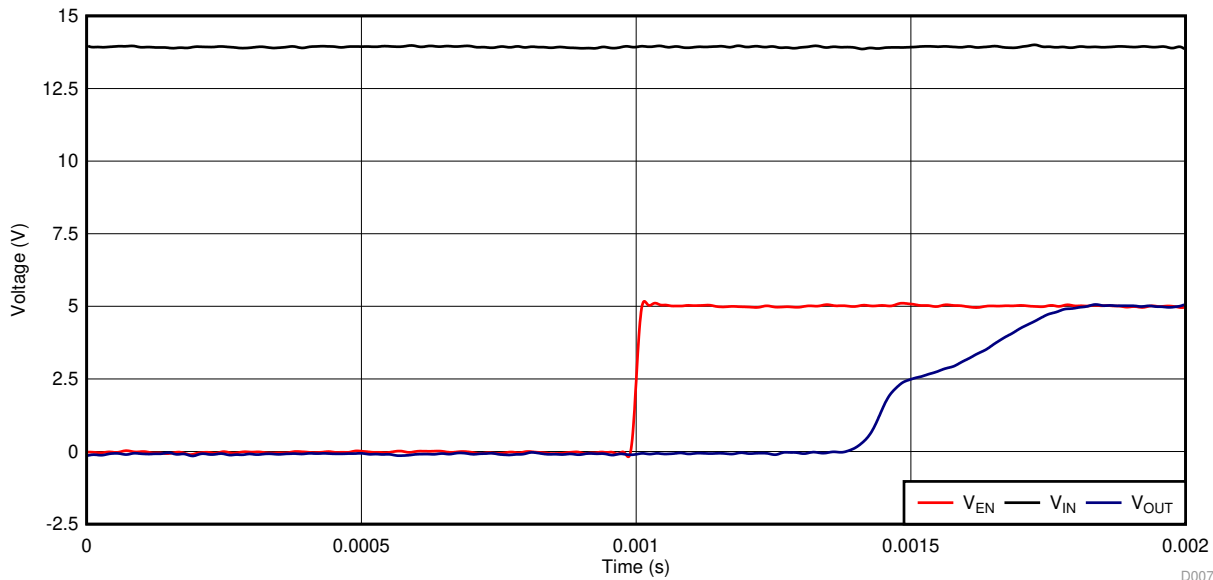


图 30. Power-Up Waveform (5 V)

## 9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 3 V to 40 V. The input supply must be well regulated. If the input supply is located more than a few inches from the TPS7B81, TI recommends adding a capacitor with a value greater than or equal to 10  $\mu\text{F}$  with a 0.1- $\mu\text{F}$  bypass capacitor in parallel at the input.

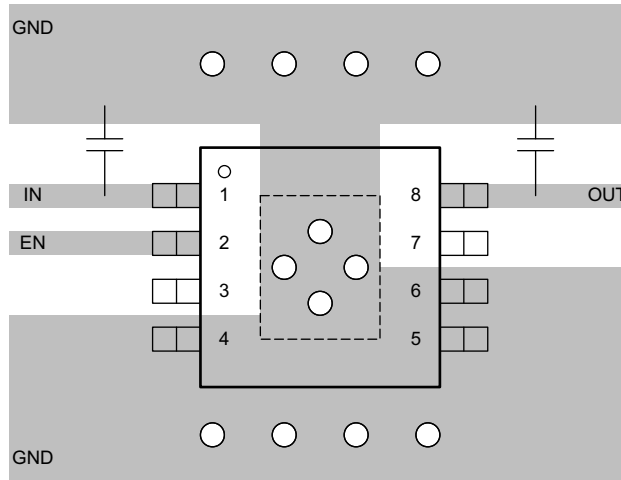


## 10 Layout

### 10.1 Layout Guidelines

Layout is an important step for LDO power supplies, especially for high-voltage and large output current supplies. If the layout is not carefully designed, the regulator can fail to deliver enough output current because of thermal limitations. To improve the thermal performance of the device, and to maximize the current output at high ambient temperature, spread the copper under the thermal pad as far as possible and put enough thermal vias on the copper under the thermal pad. [Figure 31](#) shows an example layout.

### 10.2 Layout Example



**Figure 31. Example Layout Diagram**

## 11 デバイスおよびドキュメントのサポート

### 11.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](http://ti.com)のデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

### 11.2 サポート・リソース

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 11.3 商標

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### 11.4 静電気放電に関する注意事項



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### 11.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7B8133DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	26BX	<a href="#">Samples</a>
TPS7B8133DRVR	ACTIVE	WSO	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	26DH	<a href="#">Samples</a>
TPS7B8150DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	26CX	<a href="#">Samples</a>
TPS7B8150DRVR	ACTIVE	WSO	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	26EH	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF TPS7B81 :**

- Automotive : [TPS7B81-Q1](#)

**NOTE: Qualified Version Definitions:**

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## GENERIC PACKAGE VIEW

DRV 6

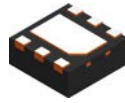
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4206925/F



4222173/B 04/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



# EXAMPLE STENCIL DESIGN

DRV0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7  
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:30X

4222173/B 04/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



## GENERIC PACKAGE VIEW

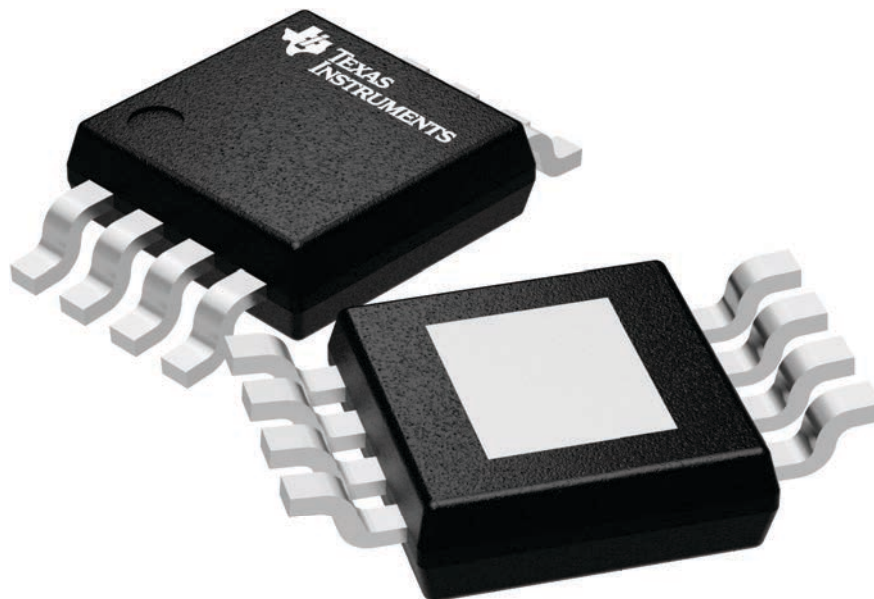
**DGN 8**

**PowerPAD VSSOP - 1.1 mm max height**

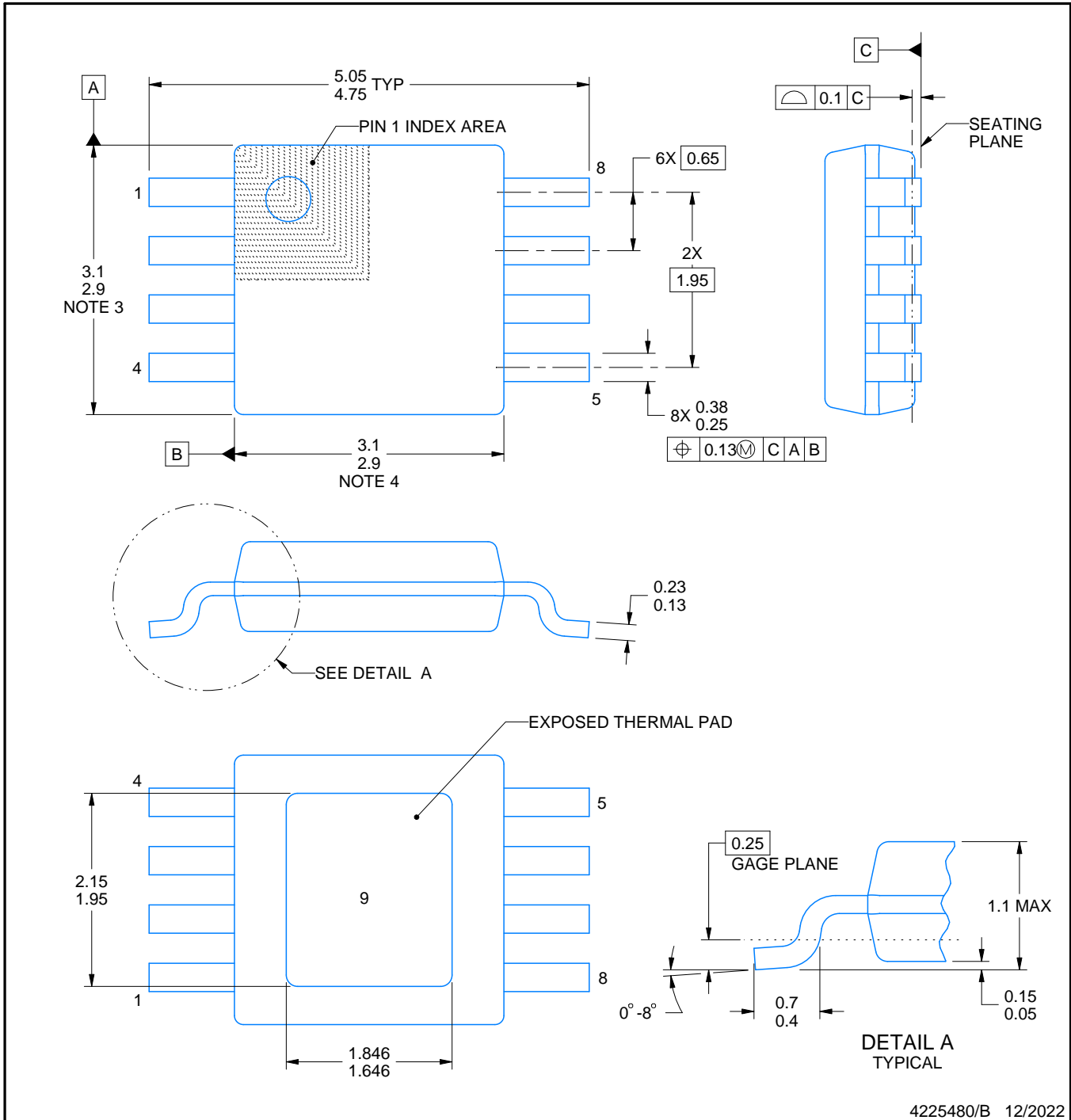
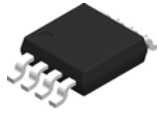
3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4225482/A



4225480/B 12/2022

NOTES:

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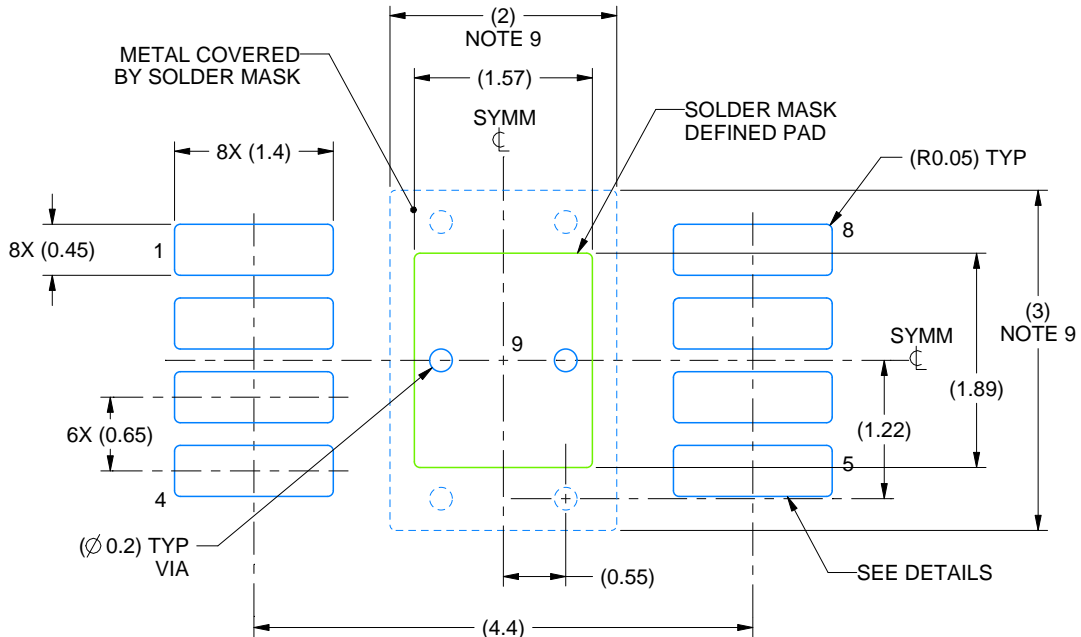
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

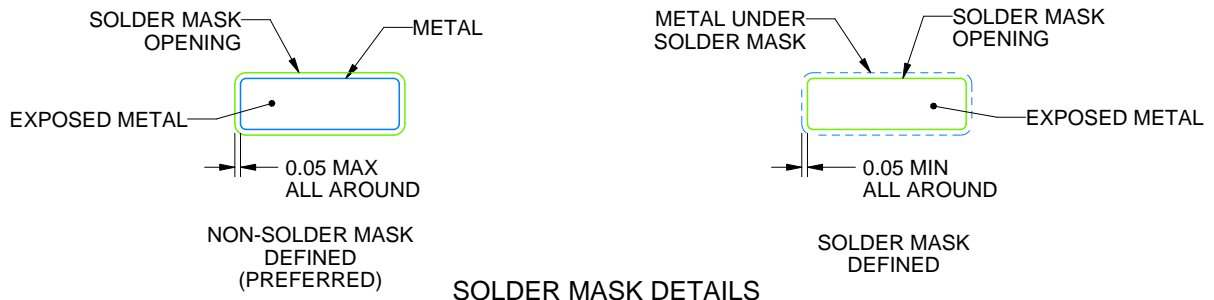
DGN0008G

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



SOLDER MASK DETAILS

4225480/B 12/2022

NOTES: (continued)

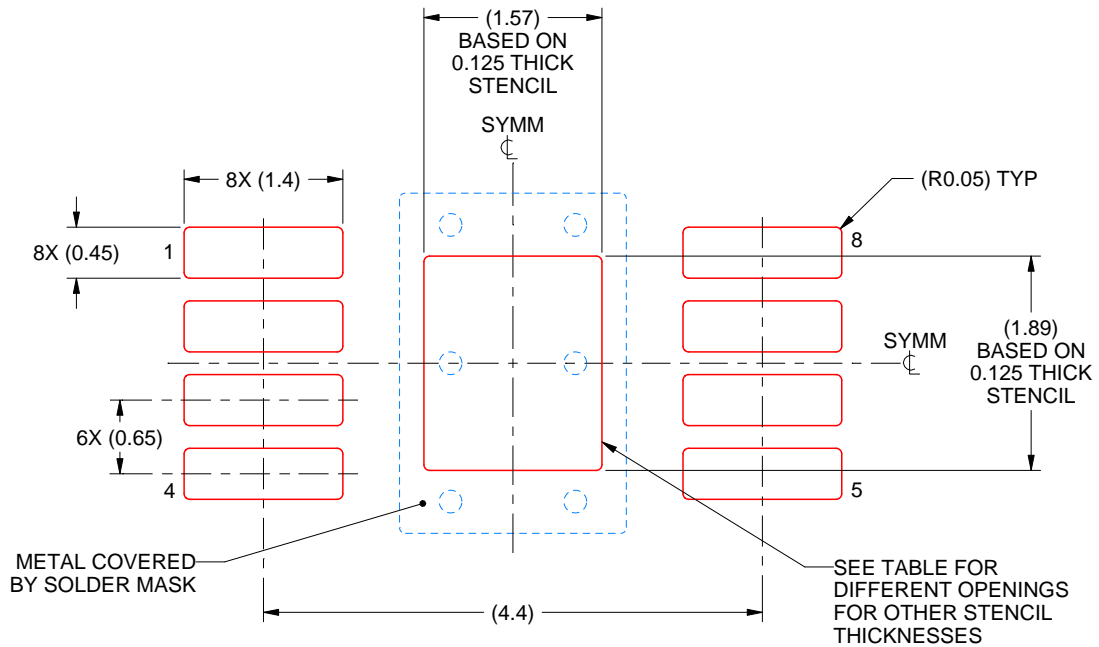
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
- 8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
- 9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DGN0008G

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



**SOLDER PASTE EXAMPLE**  
EXPOSED PAD 9:  
100% PRINTED SOLDER COVERAGE BY AREA  
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225480/B 12/2022

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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