UCCx808A 低消費電力、電流モードのプッシュプルPWM

1 特長

- プッシュプル構成のデュアル出力駆動段
- 電流センス放電トランジスタによって動的応答を改善
- 開始時電流130µA (標準値)
- 実行時電流1mA (標準値)
- 1MHzでの動作
- 内部的なソフトスタート
- ゲイン帯域幅積が2MHzのオンチップ・エラー・アンプ
- オンチップVDDクランピング
- 出力駆動ステージのピーク・ソース電流500mA、ピーク・シンク電流1A

2 アプリケーション

- 高効率のスイッチ・モード電源
- テレコムのDC/DCコンバータ
- ポイント・オブ・ロード(POL)電源モジュール
- 低コストのプッシュプルおよびハーフ・ブリッジ・アプリケーション

3 概要

UCCx808Aデバイスは BiCMOSプッシュプル、高速、低消費電力、パルス幅モジュレータのファミリです。

UCCx808Aには、オフラインまたはDC/DCの固定周波数電流モード・スイッチング電源を最小限の外付け部品で構築するため必要な、すべての制御および駆動回路が内蔵されています。

UCCx808Aデュアル出力駆動段は、プッシュプル構成に編成されています。両方の出力は、トグル・フリップ・フロップを使用して、発振器の半分の周波数でスイッチングされます。2つの出力間のデッド・タイムは、タイミング用のコンデンサおよび抵抗によって異なりますが、一般に60ns～200nsで、それぞれの出力ステージのデューティ・サイクルは50%未満に制限されます。

UCCx808Aファミリには各種のパッケージ・オプション、温度範囲オプション、低電圧誤動作防止レベルが用意されています。このファミリには、オフラインおよびバッテリ駆動システム用のUVLOスレッショルドとヒステリシス・オプションがあります。

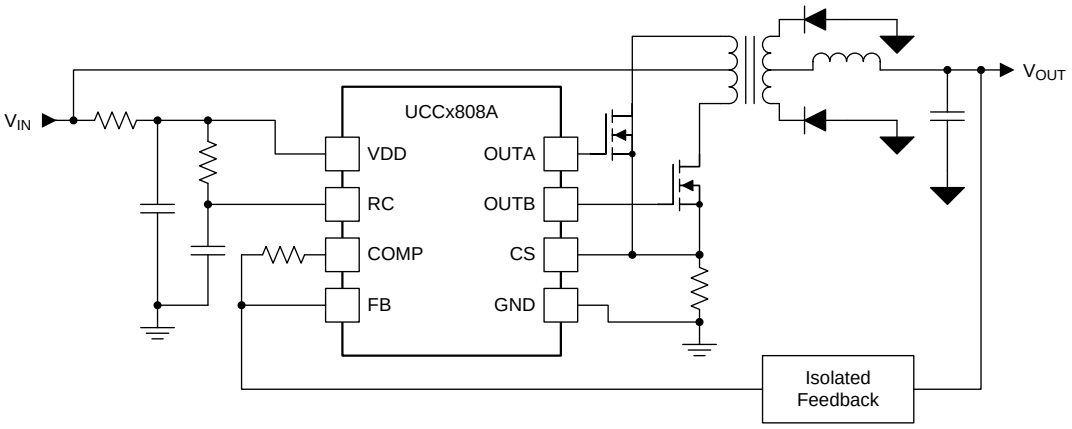
UCCx808Aは、UCC3808ファミリの拡張版です。主な相違点は、Aバージョンには CSピンからグランドへの内部放電トランジスタが搭載されており、発振器のデッド・タイム中に各クロック・サイクルでアクティブになることです。この機能により、各サイクル中にCSピン上のフィルタ容量が放電されるため、フィルタ・コンデンサの値と電流センス遅延を最小限に抑えることができます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
UCC2808A-1、UCC2808A-2、UCC3808A-2	SOIC (8)	4.90mm×3.91mm
	PDIP (8)	9.81mm×6.35mm
	TSSOP (8)	3.00mm×4.40mm
UCC3808A-1	SOIC (8)	4.90mm×3.91mm
	PDIP (8)	9.81mm×6.35mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

アプリケーション概略図



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision E (December 2016) から **Revision F** に変更 **Page**

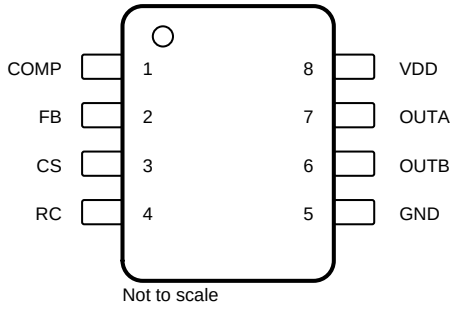
- 「*アプリケーション概略図*」変更 ... 1
- Changed references of N package to P package (PDIP) ... 5
- 変更 *静電気放電に関する注意事項*の記載 ... 15

Revision D (August 2002) から **Revision E** に変更 **Page**

- 「*ESD定格*」の表、「*機能説明*」、「*デバイスの機能モード*」、「*アプリケーションと実装*」、「*電源に関する推奨事項*」、「*レイアウト*」、「*デバイスとドキュメントのサポート*」、「*メカニカル、パッケージ、および注文情報*」追加 ... 1
- Deleted Lead temperature, soldering (10 s): 300°C maximum ... 5

5 Pin Configuration and Functions

UCCx808A D or P Package
8-Pin SOIC or PDIP
Top View



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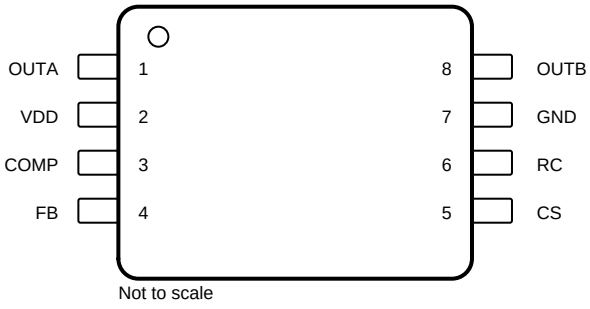
UCC2808A-x, UCC3808A-2 PW Package
8-Pin TSSOP
Top View



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Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	SOIC, PDIP	TSSOP		
COMP	1	3	O	COMP is the output of the error amplifier and the input of the PWM comparator. The error amplifier in the UCCx808A is a true low-output impedance, 2-MHz operational amplifier. As such, the COMP pin can both source and sink current. However, the error amplifier is internally current limited, so that zero duty cycle can be externally forced by pulling COMP to GND. The UCCx808A family features built-in full-cycle soft start. Soft start is implemented as a clamp on the maximum COMP voltage.
CS	3	5	I	The input to the PWM, peak current, and overcurrent comparators. The overcurrent comparator is only intended for fault sensing. Exceeding the overcurrent threshold causes a soft-start cycle. An internal MOSFET discharges the current sense filter capacitor to improve dynamic performance of the power converter.
FB	2	4	I	The inverting input to the error amplifier. For best stability, keep FB lead length as short as possible and FB stray capacitance as small as possible.
GND	5	7	G	Reference ground and power ground for all functions. Because of high currents, and high-frequency operation of the UCC3808A, a low impedance circuit board ground plane is highly recommended.
OUTA	7	1	O	Alternating high current output stages. Both stages are capable of driving the gate of a power MOSFET. Each stage is capable of 500-mA peak-source current, and 1-A peak-sink current. The output stages switch at half the oscillator frequency, in a push-pull configuration. When the voltage on the RC pin is rising, one of the two outputs is high, but during fall time, both outputs are off. This *dead time* between the two outputs, along with a slower output rise time than fall time, insures that the two outputs can not be on at the same time. This dead time is typically 60 ns to 200 ns and depends upon the values of the timing capacitor and resistor. The high-current-output drivers consist of MOSFET output devices, which switch from VDD to GND. Each output stage also provides a very low impedance to overshoot and undershoot. This means that in many cases, external-schottky-clamp diodes are not required.
OUTB	6	8	O	Alternating high current output stages. Both stages are capable of driving the gate of a power MOSFET. Each stage is capable of 500-mA peak-source current, and 1-A peak-sink current. The output stages switch at half the oscillator frequency, in a push-pull configuration. When the voltage on the RC pin is rising, one of the two outputs is high, but during fall time, both outputs are off. This *dead time* between the two outputs, along with a slower output rise time than fall time, insures that the two outputs can not be on at the same time. This dead time is typically 60 ns to 200 ns and depends upon the values of the timing capacitor and resistor. The high-current-output drivers consist of MOSFET output devices, which switch from VDD to GND. Each output stage also provides a very low impedance to overshoot and undershoot. This means that in many cases, external-schottky-clamp diodes are not required.

(1) P = Power, G = Ground, I = Input, O = Output

Pin Functions (continued)

PIN			TYPE[1]	DESCRIPTION
NAME	SOIC, PDIP	TSSOP		
RC	4	6	O	The oscillator programming pin. The UCC3808A's oscillator tracks VDD and GND internally, so that variations in power supply rails minimally affect frequency stability. *Functional Block Diagrams* shows the oscillator block diagram. Only two components are required to program the oscillator: a resistor (tied to the VDD and RC), and a capacitor (tied to the RC and GND). The approximate oscillator frequency is determined by the simple formula in Equation 1. The recommended range of timing resistors is between 10 kΩ and 200 kΩ and range of timing capacitors is between 100 pF and 1000 pF. Timing resistors less than 10 kΩ must be avoided. For best performance, keep the timing capacitor lead to GND as short as possible, the timing resistor lead from VDD as short as possible, and the leads between timing components and RC as short as possible. Separate ground and VDD traces to the external timing network are encouraged.
VDD	8	2	P	The power input connection for this device. Although quiescent VDD current is very low, total supply current is higher, depending on OUTA and OUTB current, and the programmed oscillator frequency. Total VDD current is the sum of quiescent VDD current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Qg), average OUT current can be calculated from Equation 2. To prevent noise problems, bypass VDD to GND with a ceramic capacitor as close to the chip as possible along with an electrolytic capacitor. A 1-µF decoupling capacitor is recommended.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
Supply voltage (IDD ≤ 10 mA)			15	V
Supply current			20	mA
OUTA/OUTB source current (peak)			–0.5	A
OUTA/OUTB sink current (peak)			1	A
Analog inputs (FB, CS)		–0.3	VDD + 0.3 (not to exceed 6)	V
Power dissipation at T_A = 25°C	P package		1	W
	D package		650	mW
	PW package		400	
Junction temperature, T_J		–55	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Currents are positive into, negative out of the specified terminal. Consult the packaging section of the *Power Supply Control Products Data Book* for thermal limitations and considerations of packages.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{DD}	Supply voltage	UCCx808-1	13	14	V
		UCCx808-2	5	14	
T_J	Junction temperature	UCC2808-x	–40	85	°C
		UCC3808-x	0	70	

6.4 Thermal Information

THERMAL METRIC(1)		UCCx808A		UCC2808A-x UCC3808A-2	UNIT
		D (SOIC)	P (PDIP)	PW (TSSOP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	105.4	57	151.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.9	49.6	36.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.5	34.3	81.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.7	19.5	1.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	45.9	34.2	79.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

T_A = 0°C to 70°C for the UCC3808A-x and –40°C to +85°C for the UCC2808A-x, VDD = 10 V[1], 1-µF capacitor from VDD to GND, R = 22 kΩ, C = 330 pF, and $T_A = T_J$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OSCILLATOR					
Oscillator frequency		175	194	213	kHz
Oscillator amplitude/VDD[2]		0.44	0.5	0.56	V/V
ERROR AMPLIFIER					
Input voltage	COMP = 2 V	1.95	2	2.05	V
Input bias current		–1		1	µA
Open loop voltage gain		60	80		dB
COMP sink current	FB = 2.2 V, COMP = 1 V	0.3	2.5		mA
COMP source current	FB = 1.3 V, COMP = 3.5 V	–0.2	–0.5		mA
PWM					
Maximum duty cycle	Measured at OUTA or OUTB	48%	49%	50%	
Minimum duty cycle	COMP = 0 V			0%	
CURRENT SENSE					
Gain[3]		1.9	2.2	2.5	V/V
Maximum input signal	COMP = 5 V[4]	0.45	0.5	0.55	V
CS to output delay	COMP = 3.5 V, CS from 0 mV to 600 mV		100	200	ns
CS source current		–200			nA
CS sink current	CS = 0.5 V, RC = 5.5 V[5]	5	10		mA
Over current threshold		0.7	0.75	0.8	V
COMP to CS offset	CS = 0 V	0.35	0.8	1.2	V
OUTPUT					
OUT low level	I = 100 mA		0.5	1	V
OUT high level	I = –50 mA, VDD – OUT		0.5	1	V
Rise time	C_L = 1 nF		25	60	ns
Fall time	C_L = 1 nF		25	60	ns
UNDERVOLTAGE LOCKOUT					
Start threshold	UCCx808A-1[1]	11.5	12.5	13.5	V
	UCCx808A-2	4.1	4.3	4.5	
Minimum operating voltage after start	UCCx808A-1	7.6	8.3	9	V
	UCCx808A-2	3.9	4.1	4.3	
Hysteresis	UCCx808A-1	3.5	4.2	5.1	V
	UCCx808A-2	0.1	0.2	0.3	
SOFT START					
COMP rise time	FB = 1.8 V, rise from 0.5 V to 4 V		3.5	20	ms
OVERALL					
Start-up current	VDD < start threshold		130	260	µA
Operating supply current	FB = 0 V, CS = 0 V[1][6]		1	2	mA
VDD zener shunt voltage	IDD = 10 mA[7]	13	14	15	V

(1) For UCCx808A-1, set VDD above the start threshold before setting at 10 V.
(2) Measured at RC. Signal amplitude tracks VDD.
(3) Gain is defined by: $A = \Delta V_{COMP} / \Delta V_{CS}$, $0 V \le V_{CS} \le 0.4 V$.
(4) Parameter measured at trip point of latch with FB at 0 V.
(5) The internal current sink on the CS pin is designed to discharge an external filter capacitor. It is not intended to be a DC sink path.
(6) Does not include current in the external oscillator network.
(7) Start threshold and Zener shunt threshold track one another.

6.6 Typical Characteristics

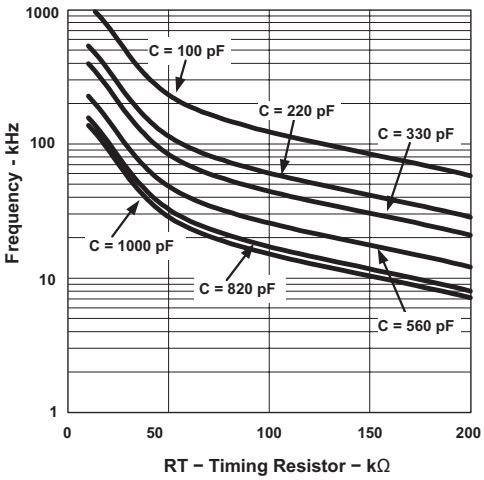


Figure 1. Oscillator Frequency vs External RC Values

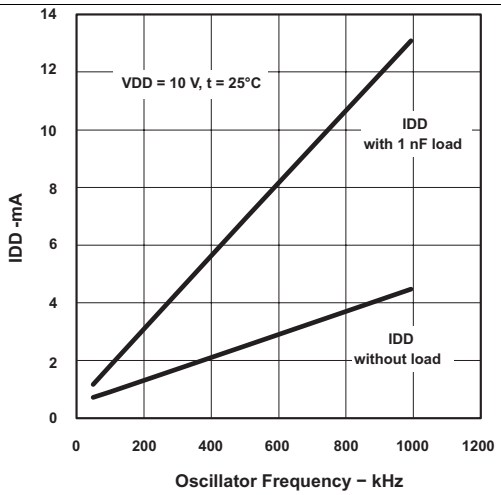


Figure 2. IDD vs Oscillator Frequency

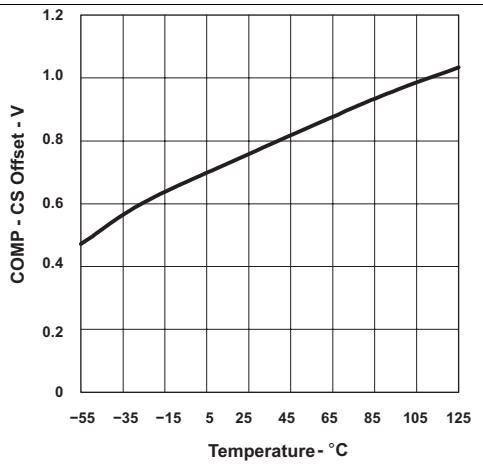


Figure 3. COMP to CS Offset vs Temperature

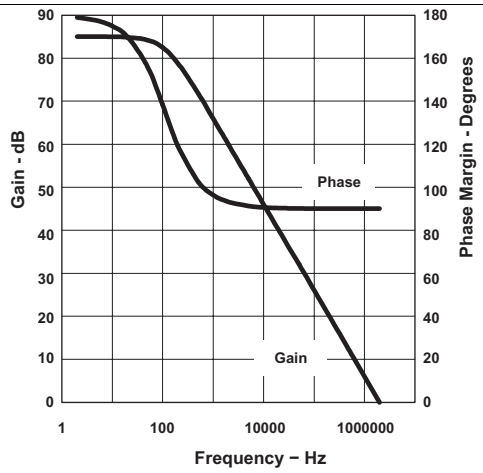


Figure 4. Error Amplifier Gain and Phase Response vs Frequency

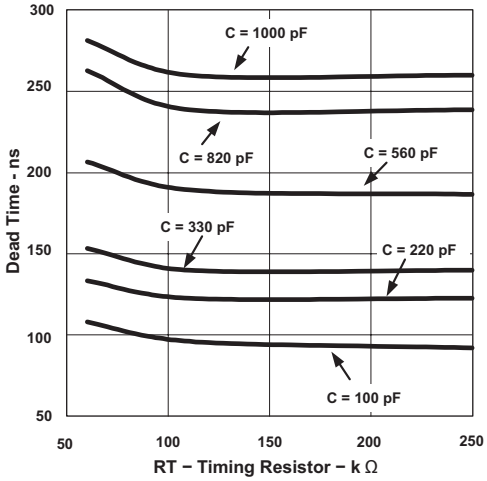


Figure 5. Output Dead Time vs External RC Values

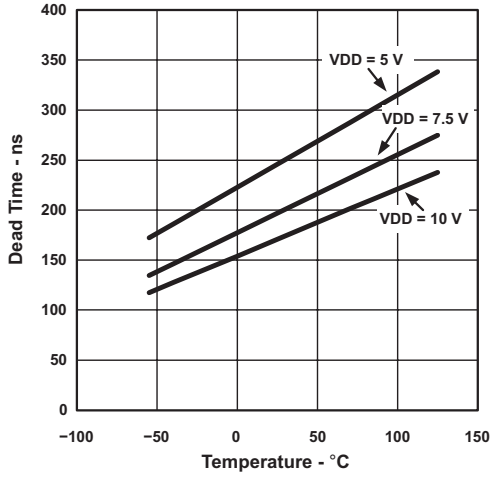


Figure 6. Dead Time vs Temperature

Typical Characteristics (continued)

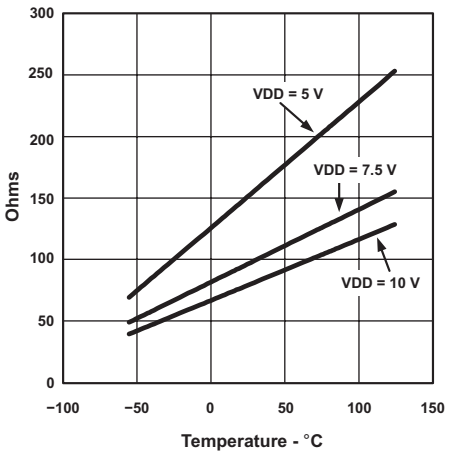


Figure 7. RC $R_{DS(on)}$ vs Temperature

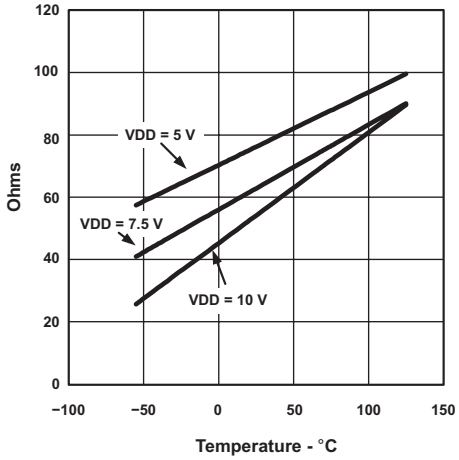


Figure 8. CS $R_{DS(on)}$ vs Temperature

7 Detailed Description

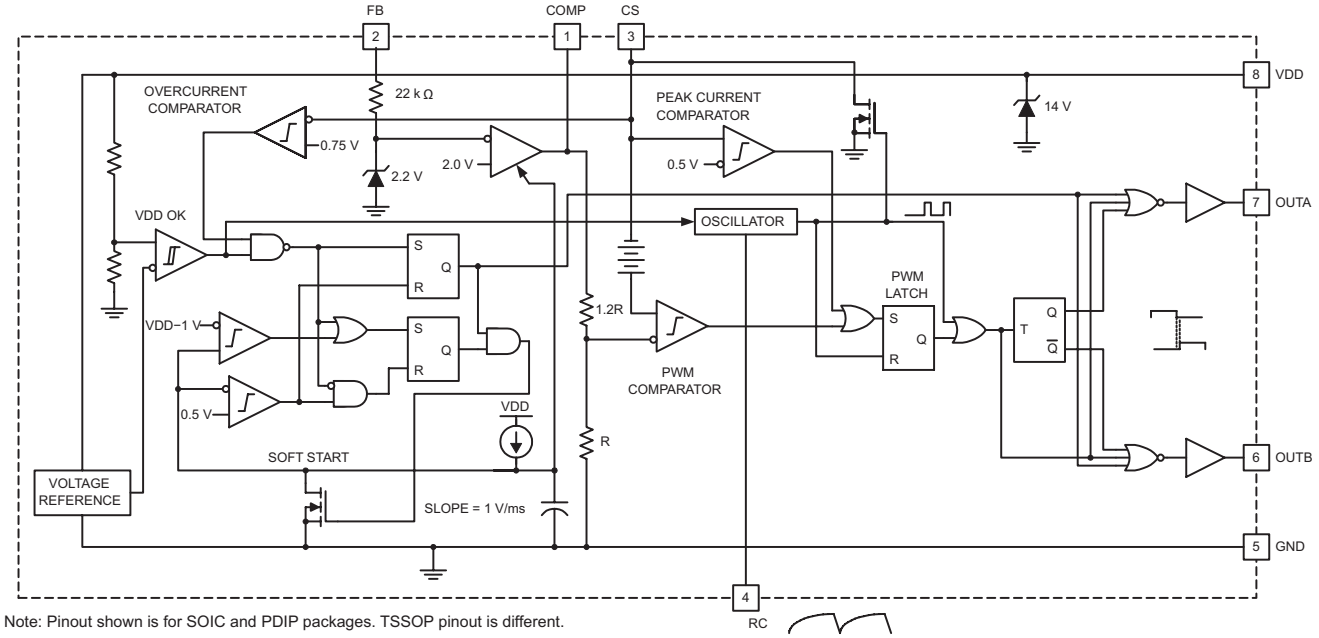
7.1 Overview

The UCCx808A-x device is a highly integrated, low-power current mode push-pull PWM controller. The controller employs low starting current and an internal control algorithm that offers accurate output voltage regulation in the presence of line and load variations. The UCCx808A-x family of parts has UVLO thresholds and hysteresis options for off-line and battery-powered systems.

Table 1. Undervoltage Lockout Levels

PART NUMBER	TURNON THRESHOLD	TURNOFF THRESHOLD
UCCx808A-1	12.5	8.3
UCCx808A-1	4.3	4.1

7.2 Functional Block Diagrams



The oscillator generates a sawtooth waveform on RC. During the RC rise time, the output stages alternate on time, but both stages are off during the RC fall time. The output stages switch a 1/2 the oscillator frequency, with ensured duty cycle of < 50% for both outputs.

Figure 9. Block Diagram

Functional Block Diagrams (continued)

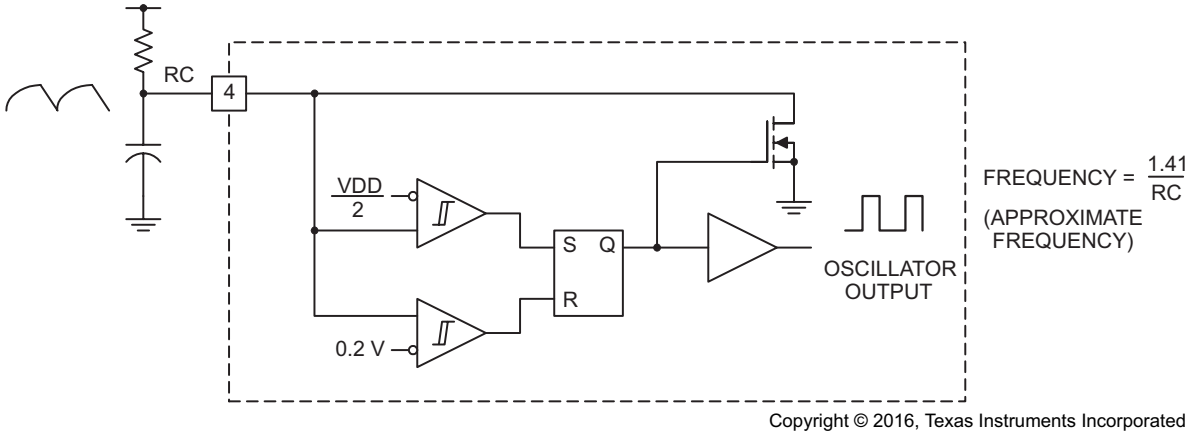


Figure 10. Block Diagram of Oscillator

7.3 Feature Description

7.3.1 Pin Descriptions

7.3.1.1 COMP

The COMP pin is the output of the error amplifier and the input of the PWM comparator. The error amplifier in the UCC3808 is a true low-output impedance, 2-MHz operational amplifier. As such, the COMP pin can both source and sink current. However, the error amplifier is internally current limited, so that zero duty cycle can be externally forced by pulling COMP to GND.

The UCC3808 family features built-in full cycle soft start. Soft start is implemented as a clamp on the maximum COMP voltage.

7.3.1.2 CS

The input to the PWM, peak current, and overcurrent comparators. The overcurrent comparator is only intended for fault sensing. Exceeding the overcurrent threshold causes a soft-start cycle.

7.3.1.3 FB

The inverting input to the error amplifier. For best stability, keep FB lead length as short as possible and FB stray capacitance as small as possible.

7.3.1.4 GND

Reference ground and power ground for all functions. Because of high currents, and high-frequency operation of the UCC3808, a low-impedance printed-circuit board ground plane is highly recommended.

7.3.1.5 OUTA and OUTB

Alternating high current output stages. Both stages are capable of driving the gate of a power MOSFET. Each stage is capable of 500-mA peak source current, and 1-A peak sink current.

The output stages switch at half the oscillator frequency, in a push-pull configuration. When the voltage on the RC pin is rising, one of the two outputs is high, but during fall time, both outputs are off. This dead time between the two outputs, along with a slower output rise time than fall time, insures that the two outputs can not be on at the same time. This dead time is typically 60 ns to 200 ns and depends upon the values of the timing capacitor and resistor.

The high-current output drivers consist of MOSFET output devices, which switch from VDD to GND. Each output stage also provides a very low impedance to overshoot and undershoot. This means that in many cases, external Schottky clamp diodes are not required.

Feature Description (continued)

7.3.1.6 RC

The oscillator programming pin. The oscillator of the UCC3808-x tracks VDD and GND internally, so that variations in power supply rails minimally affect frequency stability. Figure 10 shows the oscillator block diagram.

Only two components are required to program the oscillator: a resistor (tied to the VDD and RC), and a capacitor (tied to the RC and GND). The approximate oscillator frequency is determined by Equation 1.

$$f_{OSCILLATOR} = \frac{1.41}{RC} \quad (1)$$

where

- frequency is in Hz
- resistance in Ω
- capacitance in Farads

The recommended range of timing resistors is between 10 kΩ and 200 kΩ and range of timing capacitors is between 100 pF and 1000 pF. Timing resistors less than 10 kΩ must be avoided.

For best performance, keep the timing capacitor lead to GND as short as possible, the timing resistor lead from VDD as short as possible, and the leads between timing components and RC as short as possible. Separate ground and VDD traces to the external timing network are encouraged.

7.3.1.7 VDD

The power input connection for this device. Although quiescent VDD current is very low, total supply current is higher, depending on OUTA and OUTB current, and the programmed oscillator frequency. Total VDD current is the sum of quiescent VDD current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Qg), average OUT current can be calculated with Equation 2.

$$I_{OUT} = Q_g \times F \quad (2)$$

where

- F is frequency

To prevent noise problems, bypass VDD to GND with a ceramic capacitor as close to the chip as possible along with an electrolytic capacitor. TI recommends a 1-µF decoupling capacitor.

7.4 Device Functional Modes

7.4.1 VCC

When VCC rises above 12.5 V (for the UCCx808A-1) or above 4.3 V (for the UCCx808-2) the device is enabled. When any fault conditions are cleared, a soft-start condition is initiated and the gate driver outputs begin switching.

When VCC drops below 8.3 V (for the UCCx808-1) or 4.1 V (for the UCCx808-2) the device enters the UVLO protection mode and both gate drivers are actively pulled low.

7.4.2 Push-Pull or Half-Bridge Function

Because the device provides alternate 180° out-of-phase gate drive signals (OUTA and OUTB), it may be used as a controller for the push-pull or half-bridge topologies. For the half-bridge topology the UCCx808A-x requires a an external high side gate driver or pulse transformer on one or both of the OUTA and OUTB signals.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

A 200-kHz push-pull application circuit with a full-wave rectifier is shown in Figure 11. The output, V_O, provides 5 V at 50 W maximum and is electrically isolated from the input. Because the UCC3808A is a peak-current-mode controller the 2N2907 emitter following amplifier (buffers the CT waveform) provides slope compensation which is necessary for duty ratios greater than 50%. Capacitor decoupling is very important with a single ground IC controller, and a 1 µF is suggested as close to the IC as possible. The controller supply is a series RC for start-up, paralleled with a bias winding on the output inductor used in steady-state operation.

Isolation is provided by an optocoupler with regulation done on the secondary side using the TL431 adjustable precision shunt regulator. Small signal compensation with tight voltage regulation is achieved using this part on the secondary side. Many choices exist for the output inductor depending on cost, volume, and mechanical strength. Several design options are iron powder, molypermalloy (MPP), or a ferrite core with an air gap as shown here. The main power transformer has a Magnetics Inc. ER28 size core made of P material for efficient operation at this frequency and temperature. The input voltage may range from 36 Vdc to 72 Vdc.

8.2 Typical Application

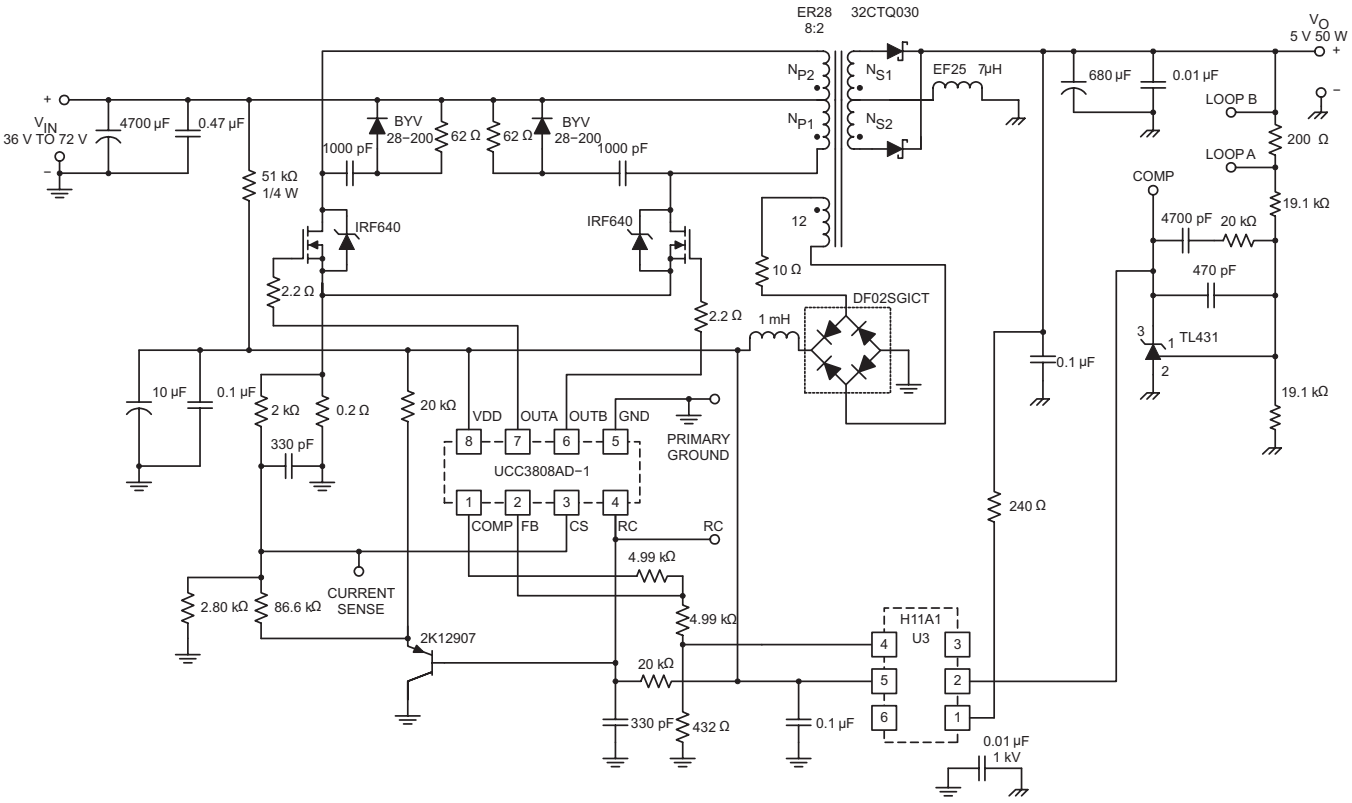


Figure 11. Typical Application Diagram: 48-Vin, 5-V, 50-W Output

Typical Application (continued)

8.2.1 Design Requirements

Table 2 lists the design parameters for the UCC3808A-x.

Table 2. Design Parameters

PARAMETER	VALUE
Output voltage	5 V
Rated output power	50 W
Input DC voltage range	36 V to 72 V
Switching frequency	210 kHz

8.2.2 Detailed Design Procedure

The output, VO, provides 5 V at 50 W maximum and is electrically isolated from the input. Because the UCC3808A is a peak current mode controller, the 2N2907 emitter follower amplifier buffers the oscillator waveform (RC pin) and provides slope compensation to the current sense (CS) input. This is necessary for duty cycle ratios of greater than 50%.

Capacitor decoupling is provided on the VDD pin. TI recommends using a minimum decoupling capacitance of 10-µF electrolytic and 0.1-µF ceramic. The ceramic capacitor must be as close to the VDD pin as possible. The UCC3808A is initially powered up from the 36-V to 72-V input supply . Once the power supply has started, the bias supply is provided by an auxiliary winding on the main power transformer.

Isolation is provided by an optocoupler with regulation done on the secondary side using the TL431 precision programmable reference. The internal error amplifier of the UCC3808A is set up as a unity gain amplifier and the compensation network is provided on the secondary side.

Many choices exist for the output inductor depending on cost and size constraints. Design options are powdered iron, molypermalloy or the ferrite core option used in this design. The power transformer is a low profile design, EFD25 size, using the Magnetics Inc. P material. This material is a good choice for low power loss at high switching frequency.

The switching frequency is set at 210 kHz with the RC network on the RC pin.

8.2.3 Application Curves

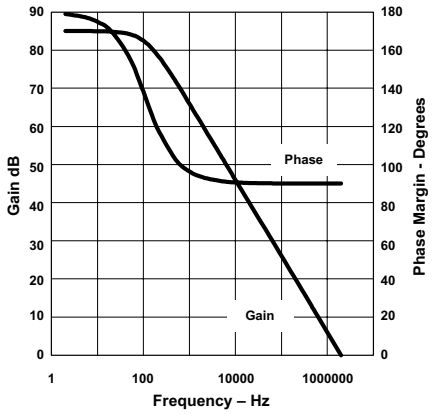


Figure 12. Error Amplifier Gain and Phase Response vs Frequency

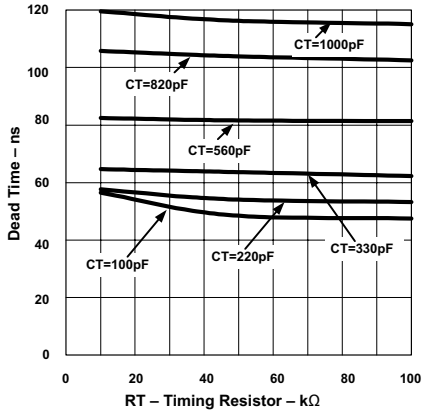


Figure 13. Dead Time vs Timing Resistor

9 Power Supply Recommendations

The VDD power terminal for the device requires the placement of electrolytic capacitor as energy storage capacitor because of the 1-A drive capability of the UCCx808A-x controller. Also a low-ESR noise decoupling capacitor is required and it must be placed as close as possible to the VDD and GND pins. Ceramic capacitors with stable dielectric characteristics over temperature are recommended. X7R is a suitable dielectric material for use here.

TI recommends a 10-µF, 25-V electrolytic capacitor part.

10 Layout

10.1 Layout Guidelines

1. Place the VDD capacitor as close as possible between the VDD pin and GND of the UCCx808A-x, tracked directly to both pins.
2. A small, external filter capacitor is recommended on the CS pin. Track the filter capacitor as directly as possible from the CS to GND pins.
3. The tracking and layout of the FB pin and connecting components is critical to minimizing noise pickup and interference. Reduce the total surface area of traces on the FB net to a minimum.
4. The OUTA and OUTB pins have a high-current source and sink capability. An external gate resistor is recommended to damp oscillations. A value of around a few Ohms is recommended. A pulldown resistor on the gate to source is recommended to prevent the MOSFET gate from floating on if there is an open-circuit fault in the gate drive path.

10.2 Layout Example

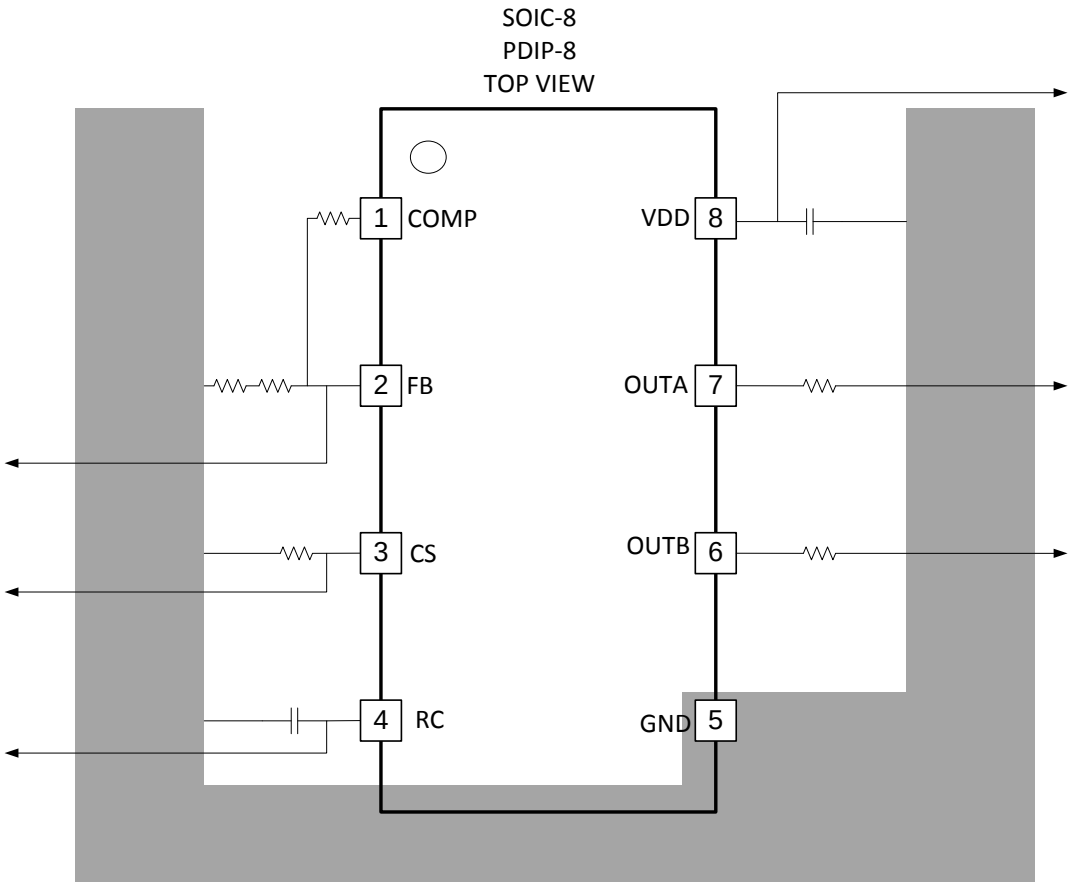


Figure 14. Recommended Layout

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントのサポート

11.1.1 関連資料

関連資料については、以下を参照してください。

『電源制御製品データ・ブック』

11.2 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 3. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
UCC2808A-1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
UCC2808A-2	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
UCC3808A-1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
UCC3808A-2	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

11.3 ドキュメントの更新通知を受け取る方法

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11.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC2808ADTR-1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2808A-1	Samples
UCC2808ADTR-1G4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2808A-1	Samples
UCC2808ADTR-2	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2808A-2	Samples
UCC2808ADTR-2G4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2808A-2	Samples
UCC2808APWTR-2	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2808A2	Samples
UCC3808ADTR-1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	3808A-1	Samples
UCC3808ADTR-1G4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	3808A-1	Samples
UCC3808ADTR-2	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	3808A-2	Samples
UCC3808APWTR-2	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	3808A2	Samples
UCC3808APWTR-2G4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	3808A2	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

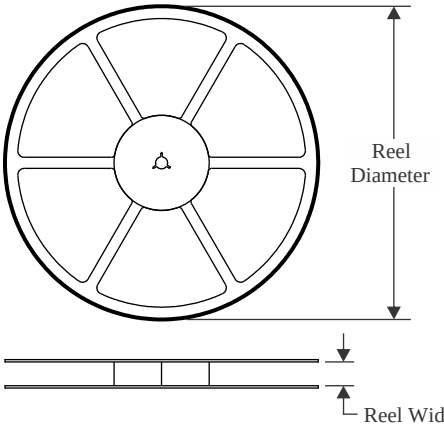
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

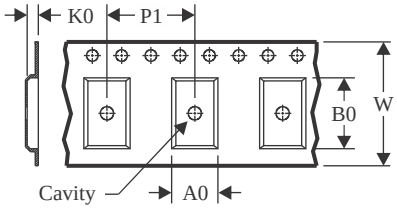
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

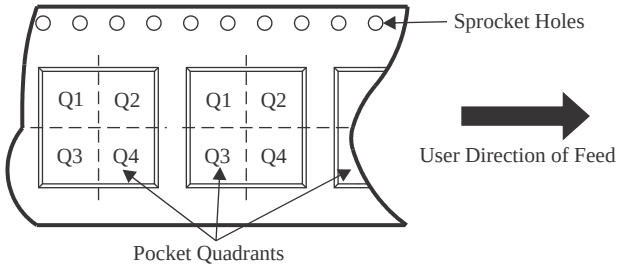


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

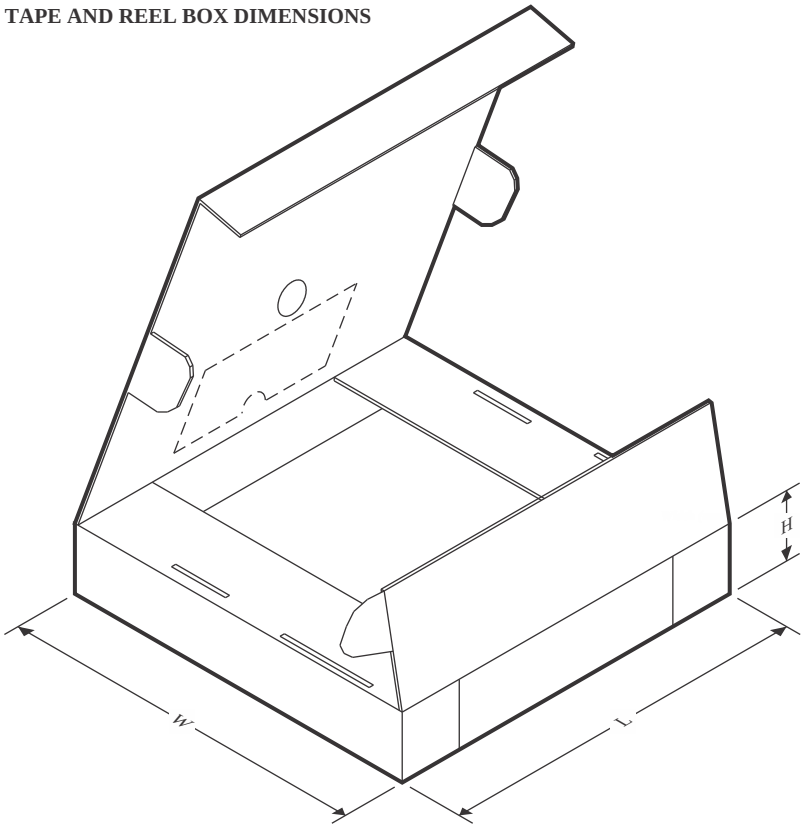
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC2808ADTR-1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2808ADTR-2	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2808APWTR-2	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
UCC3808ADTR-1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC3808ADTR-2	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC3808APWTR-2	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC2808ADTR-1	SOIC	D	8	2500	340.5	338.1	20.6
UCC2808ADTR-2	SOIC	D	8	2500	340.5	338.1	20.6
UCC2808APWTR-2	TSSOP	PW	8	2000	356.0	356.0	35.0
UCC3808ADTR-1	SOIC	D	8	2500	340.5	338.1	20.6
UCC3808ADTR-2	SOIC	D	8	2500	340.5	338.1	20.6
UCC3808APWTR-2	TSSOP	PW	8	2000	356.0	356.0	35.0

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