TEXAS INSTRUMENTS
ADS1146, ADS1147, ADS1148
JAJS456G – JULY 2009 – REVISED AUGUST 2016

ADS114x 16ビット、2kSPS、センサ測定用 プログラマブル・ゲイン・アンプ(PGA)搭載のA/Dコンバータ

1 特長

- 最大2kSPSのデータ速度をプログラム可能
- あらゆるデータ速度において1サイクルで安定
- 20SPSで50Hzと60Hzを同時に除去
- 8 (ADS1148)および4 (ADS1147)本の入力を独立に選択可能なアナログ・マルチプレクサ
- ゲインをプログラム可能: 1V/V～128V/V
- 2つのマッチングされたプログラム可能な励起電流源
- 低ドリフト係数の内蔵2.048V基準電圧
- センサのバーンアウト検出
- 4または8の汎用I/O (ADS1147およびADS1148)
- 内部温度センサ
- 電源およびV_{REF}の監視(ADS1147およびADS1148)
- 自己およびシステム較正
- SPI™互換のシリアル・インターフェイス
- アナログ電源: ユニポーラ(2.7V～5.25V)またはバイポーラ(±2.5V)
- デジタル電源: 2.7V～5.25V

2 アプリケーション

- 温度測定
  - RTD、熱電対、サーミスタ
- 圧力測定
- 流量計
- ファクトリ・オートメーションとプロセス制御

3 概要

ADS1146、ADS1147、ADS1148デバイスは高精度の16ビット・アナログA/Dコンバータ(ADC)で、多くの機能が統合されているため、センサ測定アプリケーションのシステム・コストと部品数を減らすことができます。このデバイスは、低ノイズPGA (プログラマブル・ゲイン・アンプ)、1サイクルで安定するデジタル・フィルタを備えた高精度デルタ・シグマ(ΔΣ) ADC、および内部発振回路を搭載しています。ADS1147およびADS1148デバイスには、低ドリフト係数の基準電圧と、2つのマッチングされたプログラム可能な励起電流源(IDAC)も搭載されています。

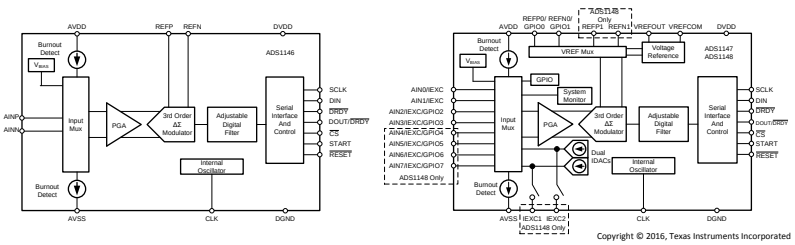
入力マルチプレクサは、ADS1148では4つ、ADS1147では2つ、ADS1146では1つの差動入力をサポートします。さらに、このマルチプレクサにはセンサのバーンアウト検出、熱電対の電圧バイアス、システム監視、汎用デジタルI/O (ADS1147およびADS1148)が組み込まれています。PGAにより、最大128V/Vのゲインを選択できます。これらの機能により、熱電対、サーミスタ、抵抗温度計(RTD)などの温度センサ測定アプリケーションや、その他抵抗性ブリッジ・センサなど小信号の測定用の完全なフロントエンド・ソリューションとなります。デジタル・フィルタは1サイクルで安定するため、入力マルチプレクサを使用するときに高速なチャネルのサイクリングが可能で、最大2kSPSのデータ速度を実現できます。20SPS以下のデータ速度では、50Hzと60Hzの両方の干渉がフィルタにより除去されます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
ADS1146	TSSOP (16)	5.00mm×4.40mm
ADS1147	TSSOP (20)	6.50mm×4.40mm
ADS1148	TSSOP (28)	9.70mm×4.40mm
	VQFN (32)	5.00mm×5.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

機能ブロック図



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision F (April 2012) から **Revision G** に変更 **Page**

- 「*ESD定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加 ... 1
- 「*特長*」および「*概要*」セクションを更新し、温度測定以外の用途での使用を追加 ... 1
- Merged all *Pin Functions* into one table ... 6
- Changed values in the *Thermal Information* table to align with JEDEC standards ... 8
- 追加 *Absolute input current* specification to *Electrical Characteristics* ... 9
- Changed compliance voltage for excitation current sources in *Electrical Characteristics*, now refers to 図 9 and 図 10; changed initial error and initial mismatch to absolute error and absolute mismatch ... 9
- 変更 IDAC mismatch specification in *Electrical Characteristics* table to reflect proper distribution ... 9
- Re-ordered elements in *Timing Requirements* tables, changed timing references to t_{CLK} ... 11
- 変更 *Low-Noise PGA* section ... 18
- Modified 図 20 to show variable resistor position ... 18
- Added f_{CLK}/f_{MOD} column to 表 5 ... 22
- 変更 *Chip Select (CS)* section ... 33
- 変更 *Data Output and Data Ready (DOUT/DRDY)* section ... 34
- 変更 Figure 42, 43, and 44 ... 35
- Added more infomation to *Data Format* section; added 図 45 ... 36
- Modified 図 46 to include $\overline{CS}$ status through SLEEP and WAKEUP command ... 38
- Updated 図 47 and 図 48 to show start of command execution ... 38
- Removed figure for *SDATAC (0001 011x)* (Stop Read Data Continuous) command ... 40
- Updated 図 53 to show MUX1 as the start of the data byte for the given command and register location ... 40

改訂履歴 (continued)

- Updated 図 54 to show start of calibration timing 41
- Updated 図 79 and 図 80 to better show timing information 66

Revision E (April 2012) から Revision F に変更 **Page**

- Added ADS1148, QFN-32 row to Package/Ordering Information table 4

Revision D (October 2011) から Revision E に変更 **Page**

- Added RHB pin configuration 5

Revision C (April 2010) から Revision D に変更 **Page**

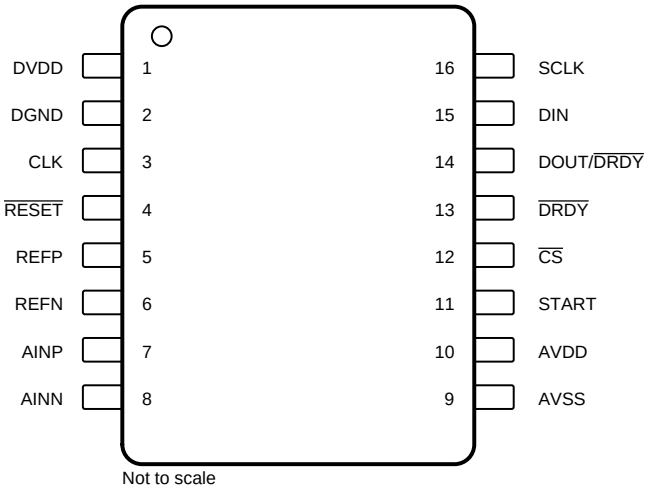
- 追加 footnote to Analog Inputs, *Full-scale input voltage* parameter typical specification in Electrical Characteristics table . 9
- 削除 Analog Inputs, *Mux leakage current* parameter from Electrical Characteristics table 9
- 追加 t_{CSPW} to minimum specification in Timing Characteristics for Figure 1 11
- 変更 t_{DTS} minimum specification in *Timing Requirements* 11
- Updated 図 1 to show t_{CSPW} timing 12
- 追加 図 6, 図 5, 図 9, and 図 10 13
- 追加 図 15, 図 16, 図 11, and 図 12 14
- Corrected 図 19 to remove constant short 17
- 追加 表 4 to *Analog Input Impedance* section 21
- Corrected 図 29 and 図 30 23
- 追加 details to *Bias Voltage Generation* section 26
- 追加 *Channel Cycling and Overload Recovery* section 30
- Corrected 表 10 31
- 追加 式 18 to *Calibration* section 31
- 追加 details to *Calibration Commands* section 32
- 追加 details to *Digital Interface* section 33
- 追加 Restricted command to 表 15 37

5 Device Comparison Table

PRODUCT	RESOLUTION (BITS)	NUMBER OF INPUTS	VOLTAGE REFERENCE	EXCITATION CURRENT SOURCES	PACKAGE (PINS)
ADS1246	24	1 Differential	External	No	TSSOP (16)
ADS1247	24	4-Input Multiplexer	Internal or External	Yes	TSSOP (20)
ADS1248	24	8-Input Multiplexer	Internal or External	Yes	TSSOP (28)
ADS1146	16	1 Differential	External	No	TSSOP (16)
ADS1147	16	4-Input Multiplexer	Internal or External	Yes	TSSOP (20)
ADS1148	16	8-Input Multiplexer	Internal or External	Yes	TSSOP (28)
	16	8-Input Multiplexer	Internal or External	Yes	VQFN (32)

6 Pin Configuration and Functions

PW Package
16-Pin TSSOP
Top View



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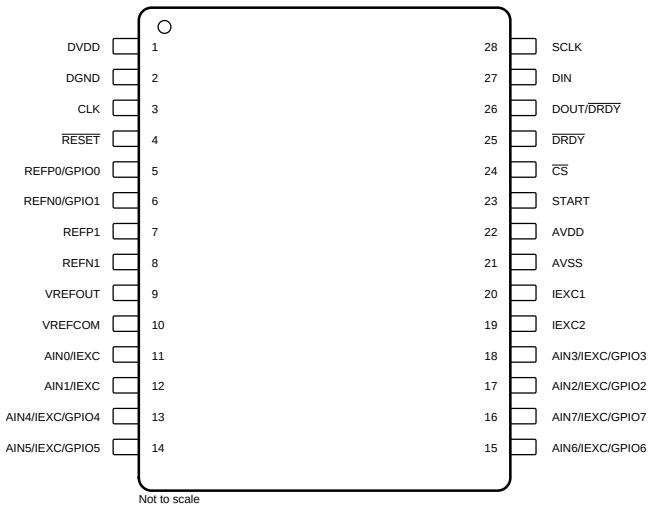
PW Package
28-Pin TSSOP
Top View



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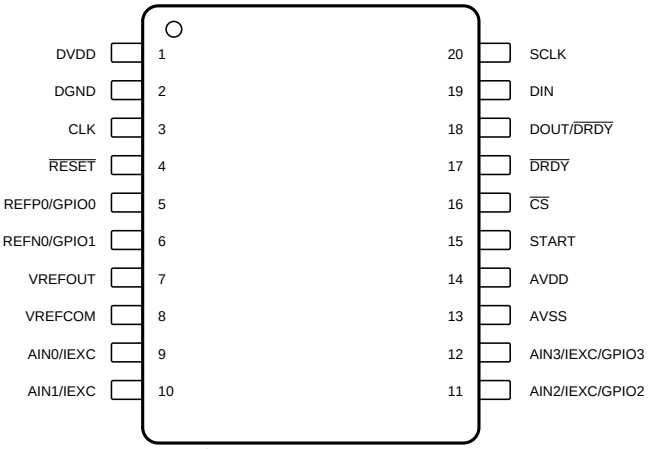
PW Package
20-Pin TSSOP
Top View



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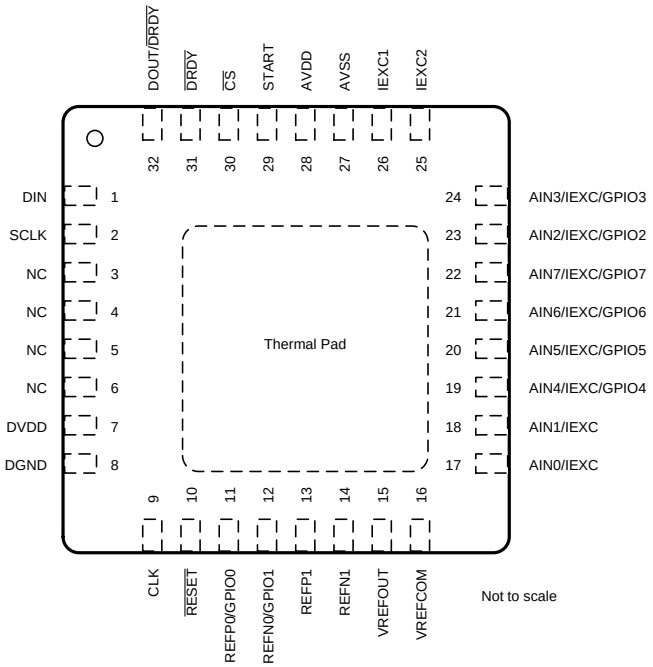
RHB Package
32-Pin VQFN
Top View



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Pin Functions

PIN					TYPE[1]	DESCRIPTION[2]
NAME	ADS1146	ADS1147	ADS1148			
	TSSOP (16)	TSSOP (20)	TSSOP (28)	VQFN (32)		
AIN0/IEXC	—	9	11	17	I	Analog input 0, optional excitation current output
AIN1/IEXC	—	10	12	18	I	Analog input 1, optional excitation current output
AIN2/IEXC/GPIO2	—	11	17	23	I/O	Analog input 2, optional excitation current output, or general-purpose digital input/output pin 2
AIN3/IEXC/GPIO3	—	12	18	24	I/O	Analog input 3, optional excitation current output, or general-purpose digital input/output pin 3
AIN4/IEXC/GPIO4	—	—	13	19	I/O	Analog input 4, optional excitation current output, or general-purpose digital input/output pin 4
AIN5/IEXC/GPIO5	—	—	14	20	I/O	Analog input 5, optional excitation current output, or general-purpose digital input/output pin 5
AIN6/IEXC/GPIO6	—	—	15	21	I/O	Analog input 6, optional excitation current output, or general-purpose digital input/output pin 6
AIN7/IEXC/GPIO7	—	—	16	22	I/O	Analog input 7, optional excitation current output, or general-purpose digital input/output pin 7
AINN	8	—	—	—	I	Negative analog input
AINP	7	—	—	—	I	Positive analog input
AVDD	10	14	22	28	P	Positive analog power supply, connect a 0.1-µF capacitor to AVSS
AVSS	9	13	21	27	P	Negative analog power supply
CLK	3	3	3	9	I	External clock input, tie to DGND to activate the internal oscillator.
$\overline{CS}$	12	16	24	30	I	Chip select (active low)
DGND	2	2	2	8	G	Digital ground
DIN	15	19	27	1	I	Serial data input
DOUT/$\overline{DRDY}$	14	18	26	32	O	Serial data output, or data out combined with data ready
$\overline{DRDY}$	13	17	25	31	O	Data ready (active low)
DVDD	1	1	1	7	P	Digital power supply, connect a 0.1-µF capacitor to DGND
IEXC1	—	—	20	26	O	Excitation current output 1
IEXC2	—	—	19	25	O	Excitation current output 2
NC	—	—	—	3, 4, 5, 6	—	Connect pin to AVSS or leave floating
REFN	6	—	—	—	I	Negative external reference input
REFN0/GPIO1	—	6	6	12	I/O	Negative external reference input 0, or general-purpose digital input/output pin 1
REFN1	—	—	8	14	I	Negative external reference input 1
REFP	5	—	—	—	I	Positive external reference input
REFP0/GPIO0	—	5	5	11	I/O	Positive external reference input 0, or general-purpose digital input/output pin 1
REFP1	—	—	7	13	I	Positive external reference input 1
$\overline{RESET}$	4	4	4	10	I	Reset (active low)
SCLK	16	20	28	2	I	Serial clock input
START	11	15	23	29	I	Conversion start
Thermal Pad	—	—	—	33	—	Connect pin to AVSS or leave floating
VREFCOM	—	8	10	16	O	Negative internal reference voltage output, connect to AVSS when using a unipolar supply or to the mid-voltage ground when using a bipolar supply
VREFOUT	—	7	9	15	O	Positive internal reference voltage output, connect a capacitor in the range of 1 µF to 47 µF to VREFCOM

(1) G = Ground, I = Input, O = Output, P = Power
(2) See *Unused Inputs and Outputs* for unused pin connections.

7 Specifications

7.1 Absolute Maximum Ratings

See (1)

		MIN	MAX	UNIT
Power-supply voltage	AVDD to AVSS	–0.3	5.5	V
	AVSS to DGND	–2.8	0.3	
	DVDD to DGND	–0.3	5.5	
Analog input voltage	AINx, REFPx, REFNx, VREFOUT, VREFCOM, IEXC1, IEXC2	AVSS – 0.3	AVDD + 0.3	V
Digital input voltage	SCLK, DIN, DOUT/$\overline{\text{DRDY}}$, $\overline{\text{DRDY}}$, $\overline{\text{CS}}$, START, $\overline{\text{RESET}}$, CLK	DGND – 0.3	DVDD + 0.3	V
Input current	Continuous, any pin except power supply pins	–10	10	mA
	Momentary, any pin except power supply pins	–100	100	
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–60	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
	Analog power supply	AVDD to AVSS	2.7		5.25	V
		AVSS to DGND	–2.65		0.1	
		AVDD to DGND	2.25		5.25	
	Digital power supply	DVDD to DGND	2.7		5.25	V
ANALOG INPUTS(1)						
V_{IN}	Differential input voltage	$V_{(AINP)} – V_{(AINN)}$(2)	$–V_{REF}$ / Gain		V_{REF} / Gain	V
V_{CM}	Common-mode input voltage	$(V_{(AINP)} + V_{(AINN)}) / 2$	See 式 3			
VOLTAGE REFERENCE INPUTS(3)						
V_{REF}	Differential reference input voltage	$V_{(REFPx)} – V_{(REFNx)}$	0.5		(AVDD – AVSS) – 1	V
$V_{(REFNx)}$	Absolute negative reference voltage		AVSS – 0.1		$V_{(REFPx)}$ – 0.5	V
$V_{(REFPx)}$	Absolute positive reference voltage		$V_{(REFNx)}$ + 0.5		AVDD + 0.1	V
EXTERNAL CLOCK INPUT(4)						
f_{CLK}	External clock frequency		1		4.5	MHz
	External clock duty cycle		25%		75%	
GENERAL-PURPOSE INPUTS AND OUTPUTS (GPIO)						
	GPIO input voltage		AVSS		AVDD	V
DIGITAL INPUTS						
	Digital input voltage		DGND		DVDD	V
TEMPERATURE RANGE						
T_A	Operating ambient temperature		–40		125	°C
	Specified ambient temperature		–40		105	°C

(1) AIN_P and AIN_N denote the positive and negative inputs of the PGA.
(2) For V_{REF} > 2.7 V, the differential input voltage must not exceed 2.7 V / Gain.
(3) REFPx and REFNx denote the differential reference input pair (ADS1146, ADS1147), or one of the two available differential reference input pairs (ADS1148).
(4) External clock only required if the internal oscillator is not used.

7.4 Thermal Information

THERMAL METRIC(1)		ADS1146	ADS1147	ADS1148		UNIT
		PW (TSSOP)	PW (TSSOP)	PW (TSSOP)	RHB (VQFN)	
		16 PINS	20 PINS	28 PINS	32 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	95.2	87.4	74.2	32.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28.9	21.7	20.2	23.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	41	39.6	31.8	6.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.5	0.8	0.8	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	40.4	38.9	31.3	6.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	1.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

Minimum and maximum specifications apply from T_A = –40°C to +105°C. Typical specifications are at T_A = 25°C. All specifications are at AVDD = 5 V, DVDD = 3.3 V, AVSS = 0 V, V_{REF} = 2.048 V, and f_{CLK} = 4.096 MHz (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
	Differential input current			100		pA
	Absolute input current			See 表 4		
PGA						
	PGA gain settings			1, 2, 4, 8, 16, 32, 64, 128		V/V
SYSTEM PERFORMANCE						
	Resolution	No missing codes		16		Bits
DR	Data rate			5, 10, 20, 40, 80, 160, 320, 640, 1000, 2000		SPS
	ADC conversion time	Single-cycle settling		See 表 10		
INL	Integral nonlinearity	Differential input, end point fit, Gain = 1, V_{CM} = 2.5 V	–1	0.5	1	LSB
	Offset error	After calibration	–1		1	LSB
	Offset drift	Gain = 1		100		nV/°C
		Gain = 128		15		nV/°C
	Gain error	Excluding V_{REF} errors	–0.5%		0.5%	
	Gain drift	Gain = 1, excludes V_{REF} drift		1		ppm°C
		Gain = 128, excludes V_{REF} drift		–3.5		ppm/°C
	Noise			See 表 1 and 表 2		
NMRR	Normal mode rejection			See 表 6		
CMRR	Common-mode rejection	At DC, Gain = 1		90		dB
		At DC, Gain = 32		100		
PSRR	Power supply rejection	AVDD, DVDD at DC		100		dB
VOLTAGE REFERENCE INPUTS						
	Reference input current			30		nA
INTERNAL VOLTAGE REFERENCE						
V_{REF}	Internal reference voltage		2.038	2.048	2.058	V
	Reference drift(1)	T_A = –40°C to +105°C		20	50	ppm/°C
	Output current(2)		–10		10	mA
	Load regulation			50		µV/mA
	Start-up time			See 表 7		
INTERNAL OSCILLATOR						
	Internal oscillator frequency		3.89	4.096	4.3	MHz
EXCITATION CURRENT SOURCES (IDACs)						
	Output current settings			50, 100, 250, 500, 750, 1000, 1500		µA
	Compliance voltage	All currents		See 図 9 and 図 10		
	Absolute error	All currents, each IDAC	–6%	±1%	6%	
	Absolute mismatch	All currents, between IDACs		±0.2%		
	Temperature drift	Each IDAC		200		ppm/°C
	Temperature drift matching	Between IDACs		10		ppm/°C
BURN-OUT CURRENT SOURCES						
	Burn-out current source settings			0.5, 2, 10		µA

(1) Specified by the combination of design and final production test.
(2) Do not exceed this loading on the internal voltage reference.

Electrical Characteristics (continued)

Minimum and maximum specifications apply from T_A = –40°C to +105°C. Typical specifications are at T_A = 25°C. All specifications are at AVDD = 5 V, DVDD = 3.3 V, AVSS = 0 V, V_{REF} = 2.048 V, and f_{CLK} = 4.096 MHz (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIAS VOLTAGE						
	Bias voltage			(AVDD + AVSS) / 2		V
	Bias voltage output impedance			400		Ω
TEMPERATURE SENSOR						
	Output voltage	T_A = 25°C		118		mV
	Temperature coefficient			405		µV/°C
GENERAL-PURPOSE INPUTS AND OUTPUTS (GPIO)						
V_{IL}	Low-level input voltage		AVSS		0.3 × AVDD	V
V_{IH}	High-level input voltage		0.7 × AVDD		AVDD	V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA	AVSS		0.2 × AVDD	V
V_{OH}	High-level output voltage	I_{OH} = 1 mA	0.8 × AVDD			V
DIGITAL INPUTS AND OUTPUTS (OTHER THAN GPIO)						
V_{IL}	Low-level input voltage		DGND		0.3 × DVDD	V
V_{IH}	High-level input voltage		0.7 × DVDD		DVDD	V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA	DGND		0.2 × DVDD	V
V_{OH}	High-level output voltage	I_{OH} = 1 mA	0.8 × DVDD			V
	Input leakage	DGND < V_{IN} < DVDD	–10		10	µA
POWER SUPPLY						
I_{AVDD}	Analog supply current	Power-down mode		0.1		µA
		Converting, AVDD = 3.3 V, DR = 20 SPS, external reference		212		
		Converting, AVDD = 5 V, DR = 20 SPS, external reference		225		
		Additional current with internal reference enabled		180		
I_{DVDD}	Digital supply current	Power-down mode		0.2		µA
		Normal operation, DVDD = 3.3 V, DR = 20 SPS, internal oscillator		210		
		Normal operation, DVDD = 5 V, DR = 20 SPS, internal oscillator		230		
P_D	Power dissipation	AVDD = DVDD = 3.3 V, DR = 20 SPS, internal oscillator, external reference		1.4		mW
		AVDD = DVDD = 5 V, DR = 20 SPS, internal oscillator, external reference		2.3		

7.6 Timing Requirements

At T_A = –40°C to +105°C and DVDD = 2.7 V to 5.5 V (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
SERIAL INTERFACE (SEE 図 1 AND 図 2)					
t_{CSSC}	Delay time, first SCLK rising edge after $\overline{CS}$ falling edge	10			ns
t_{SCCS}	Delay time, $\overline{CS}$ rising edge after final SCLK falling edge	7			t_{CLK} (1)
t_{CSPW}	Pulse duration, $\overline{CS}$ high	5			t_{CLK}
t_{SCLK}	SCLK period	488			ns
				64	Conversions
t_{SPWH}	Pulse duration, SCLK high	0.25		0.75	t_{SCLK}
t_{SPWL}	Pulse duration, SCLK low	0.25		0.75	t_{SCLK}
t_{DIST}	Setup time, DIN valid before SCLK falling edge	5			ns
t_{DIHD}	Hold time, DIN valid after SCLK falling edge	5			ns
t_{STD}	Setup time, SCLK low before $\overline{DRDY}$ rising edge	5			t_{CLK}
t_{DTS}	Delay time, SCLK rising edge after $\overline{DRDY}$ falling edge	1			t_{CLK}
MINIMUM START TIME PULSE DURATION (SEE 図 3)					
t_{START}	Pulse duration, START high	3			t_{CLK}
RESET PULSE DURATION, SERIAL INTERFACE COMMUNICATION AFTER RESET (SEE 図 4)					
$t_{\overline{RESET}}$	Pulse duration, $\overline{RESET}$ low	4			t_{CLK}
t_{RHSC}	Delay time, SCLK rising edge (start of serial interface communication) after $\overline{RESET}$ rising edge	0.6 (2)			ms

(1) t_{CLK} = 1 / f_{CLK}. The default clock frequency f_{CLK} = 4.096 MHz.
(2) Applicable only when f_{CLK} = 4.096 MHz, scales proportionally with f_{CLK} frequency.

7.7 Switching Characteristics

At T_A = –40°C to +105°C and DVDD = 2.7 V to 5.5 V (unless otherwise noted; see 図 1 and 図 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DOPD}	Propagation delay time, SCLK rising edge to valid new DOUT	DVDD ≤ 3.6 V			50	ns
		DVDD > 3.6 V			180	
t_{DOHD}	DOUT hold time		0			ns
t_{CSDO}	Propagation delay time, $\overline{CS}$ rising edge to DOUT high impedance				10	ns
t_{PWH}	Pulse duration, $\overline{DRDY}$ high		3			t_{CLK}

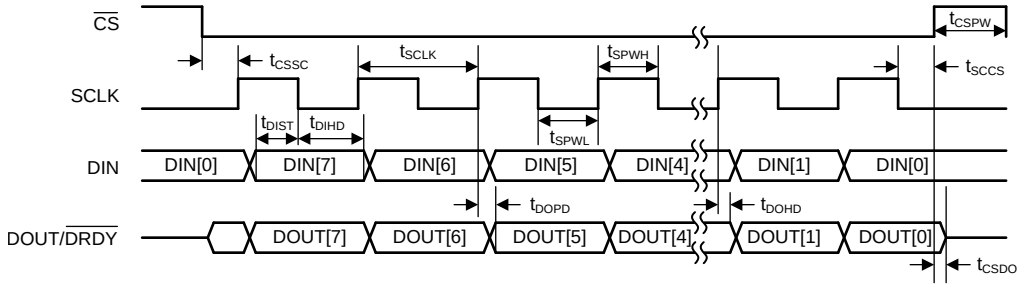
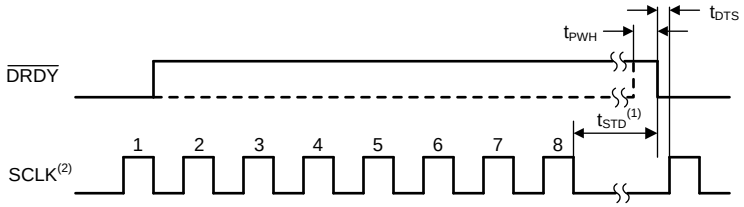


図 1. Serial Interface Timing, DRDY MODE Bit = 0



(1) This timing diagram is applicable only when the $\overline{CS}$ pin is low. SCLK does not need to be low during t_{STD} when $\overline{CS}$ is high.

(2) SCLK must only be sent in multiples of eight during partial retrieval of output data.

図 2. Serial Interface Timing to Allow Conversion Result Loading

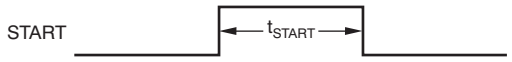


図 3. Minimum Start Pulse Duration

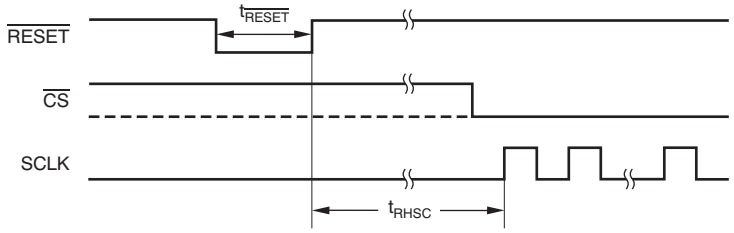


図 4. Reset Pulse Duration and Serial Interface Communication After Reset

7.8 Typical Characteristics

T_A = 25°C, AVDD = 5 V, AVSS = 0 V, and V_{REF} = 2.5 V (unless otherwise noted)

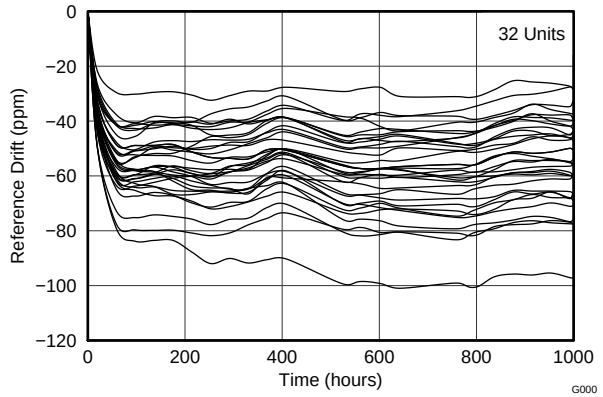


図 5. Internal Reference Long-Term Drift

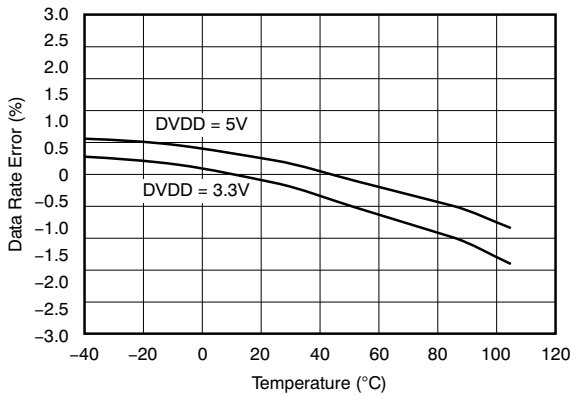


図 6. Data Rate Error vs Temperature

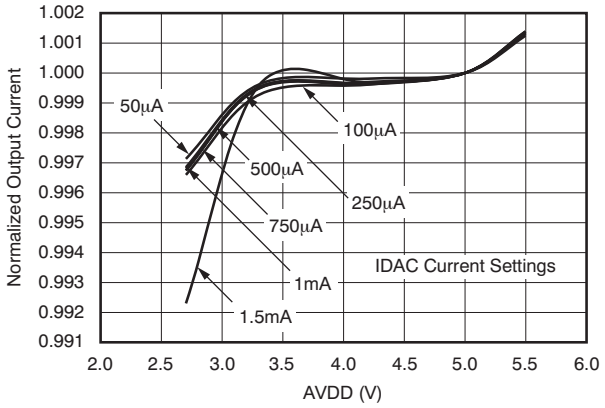


図 7. IDAC Line Regulation

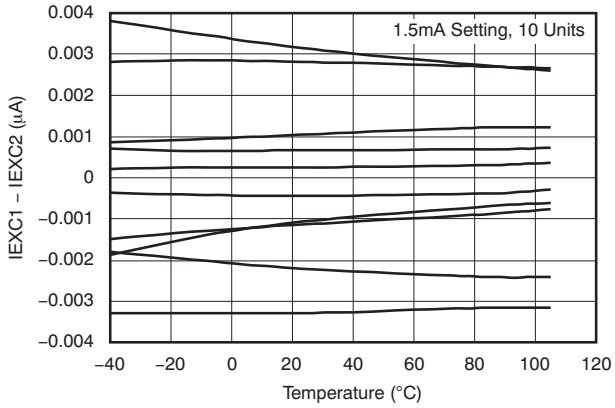


図 8. IDAC Drift

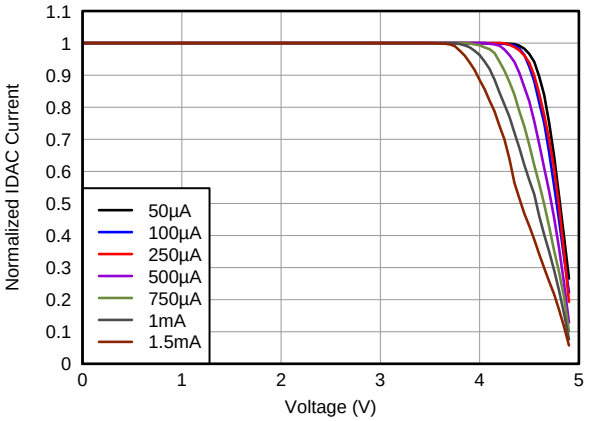


図 9. IDAC Voltage Compliance

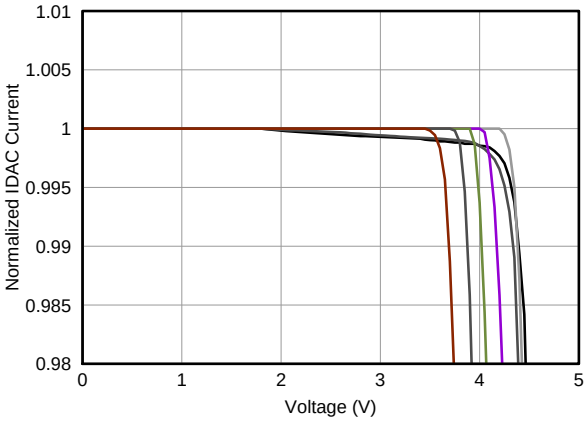


図 10. IDAC Voltage Compliance

Typical Characteristics (continued)

T_A = 25°C, AVDD = 5 V, AVSS = 0 V, and V_{REF} = 2.5 V (unless otherwise noted)

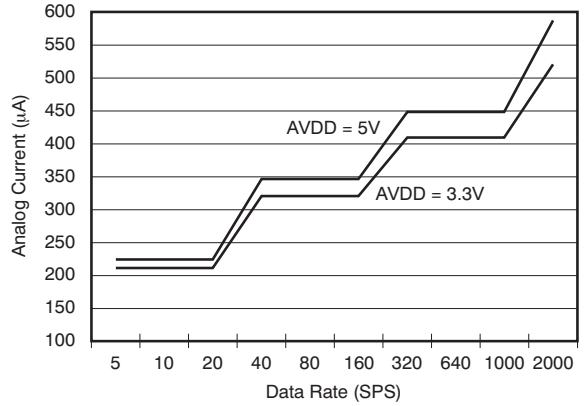


図 11. Analog Supply Current vs Data Rate

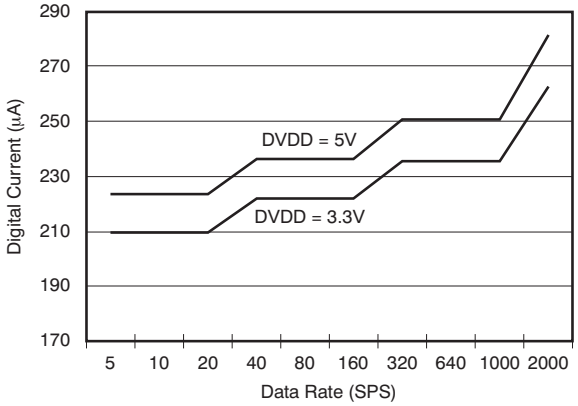


図 12. Digital Supply Current vs Data Rate

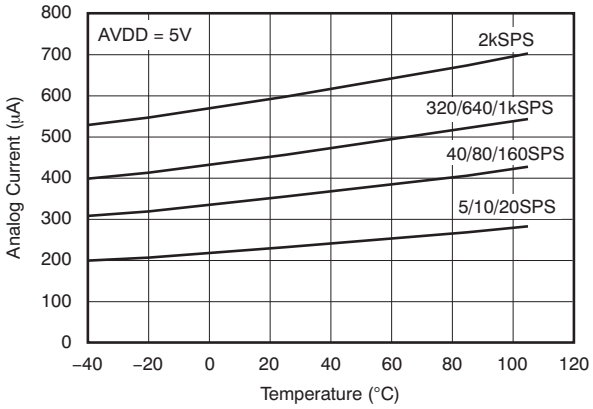


図 13. Analog Supply Current vs Temperature

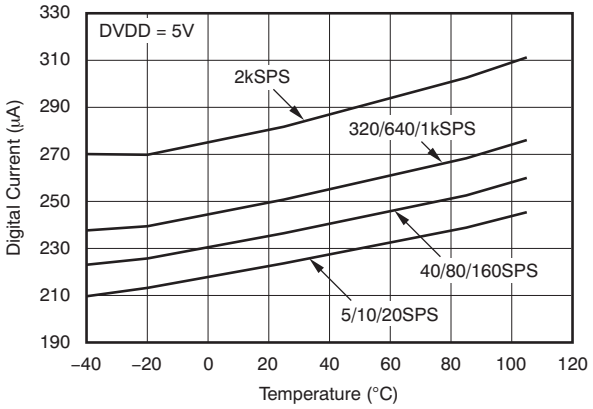


図 14. Digital Supply Current vs Temperature

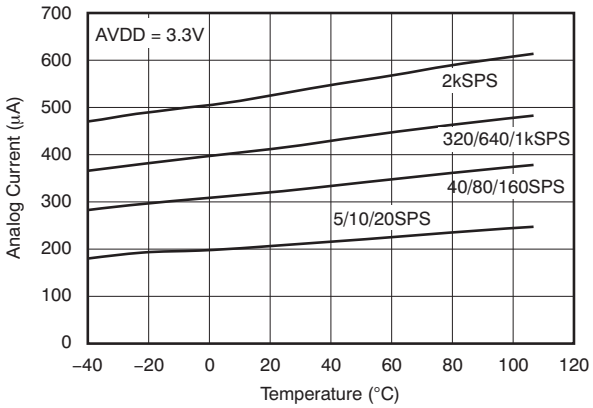


図 15. Analog Supply Current vs Temperature

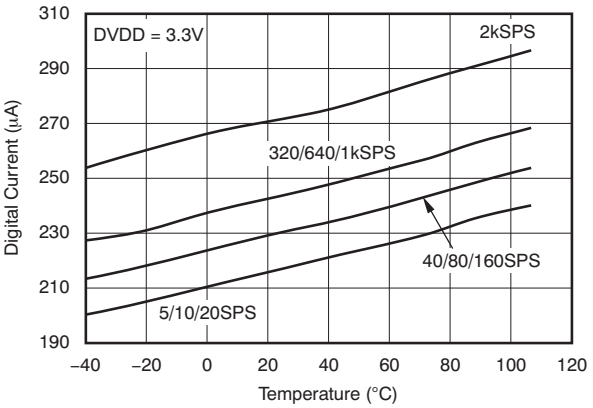


図 16. Digital Supply Current vs Temperature

8 Parameter Measurement Information

8.1 Noise Performance

The ADC noise performance is optimized by adjusting the data rate and PGA setting. Generally, the lowest input-referred noise is achieved using the highest gain possible, consistent with the input signal range. Do not set the gain too high or the result is ADC overrange. Noise also depends on the output data rate. As the data rate reduces, the ADC bandwidth correspondingly reduces. This reduction in total bandwidth results in lower overall noise. 表 1 and 表 2 summarize the noise performance of the device. The data are representative of typical noise performance at T_A = 25°C. The data shown are the result of averaging the readings from multiple devices and were measured with the inputs shorted together.

表 1 lists the input-referred noise in units of μV_{PP} for the conditions shown. 表 2 lists the corresponding data in units of ENOB (effective number of bits) where ENOB for the peak-to-peak noise is defined in 式 1.

$$ENOB = \ln((2 \times V_{REF}/Gain) / V_{NPP}) / \ln(2) \quad (1)$$

where

- V_{NPP} is the input referred peak-to-peak noise voltage

表 1. Noise in μV_{PP}
At V_{REF} = 2.048 V, AVDD = 5 V, AVSS = 0 V

DATA RATE (SPS)	PGA SETTING							
	1	2	4	8	16	32	64	128
5	62.5(1)	31.25(1)	15.63(1)	7.81(1)	3.91(1)	1.95(1)	0.98(1)	0.49(1)
10	62.5(1)	31.25(1)	15.63(1)	7.81(1)	3.91(1)	1.95(1)	0.98(1)	0.49(1)
20	62.5(1)	31.25(1)	15.63(1)	7.81(1)	3.91(1)	1.95(1)	0.98(1)	0.55
40	62.5(1)	31.25(1)	15.63(1)	7.81(1)	3.91(1)	1.95(1)	0.98(1)	0.75
80	62.5(1)	31.25(1)	15.63(1)	7.81(1)	3.91(1)	1.95(1)	1.09	0.98
160	62.5(1)	31.25(1)	15.63(1)	7.81(1)	3.91(1)	1.95(1)	1.88	1.57
320	62.5(1)	35.3	17.52	8.86	4.35	3.03	2.44	2.34
640	93.06	45.2	18.73	12.97	6.51	4.2	3.69	3.5
1000	284.59	129.77	61.3	33.04	16.82	9.08	5.42	4.65
2000	273.39	130.68	67.13	36.16	19.22	9.87	6.93	6.48

(1) Peak-to-peak noise rounded up to 1 LSB.

表 2. Effective Number of Bits From Peak-to-Peak Noise
At V_{REF} = 2.048 V, AVDD = 5 V, AVSS = 0 V

DATA RATE (SPS)	PGA SETTING							
	1	2	4	8	16	32	64	128
5	16	16	16	16	16	16	16	16
10	16	16	16	16	16	16	16	16
20	16	16	16	16	16	16	16	15.8
40	16	16	16	16	16	16	16	15.4
80	16	16	16	16	16	16	15.8	15
160	16	16	16	16	16	16	15.1	14.3
320	16	15.8	15.8	15.8	15.8	15.4	14.7	13.7
640	15.4	15.5	15.7	15.3	15.3	14.9	14.1	13.2
1000	13.8	13.9	14	13.9	13.9	13.8	13.5	12.7
2000	13.9	13.9	13.9	13.8	13.7	13.7	13.2	12.3

9 Detailed Description

9.1 Overview

The ADS1146, ADS1147 and ADS1148 devices are highly integrated 16-bit data converters. The devices include a low-noise, high-input impedance programmable gain amplifier (PGA), a delta-sigma (ΔΣ) ADC with an adjustable single-cycle settling digital filter, internal oscillator, and an SPI-compatible serial interface.

The ADS1147 and ADS1148 also include a flexible input multiplexer with system monitoring capability and general-purpose I/O settings, a low-drift voltage reference, and two matched current sources for sensor excitation. 図 17 and 図 18 show the various functions incorporated into each device.

9.2 Functional Block Diagrams

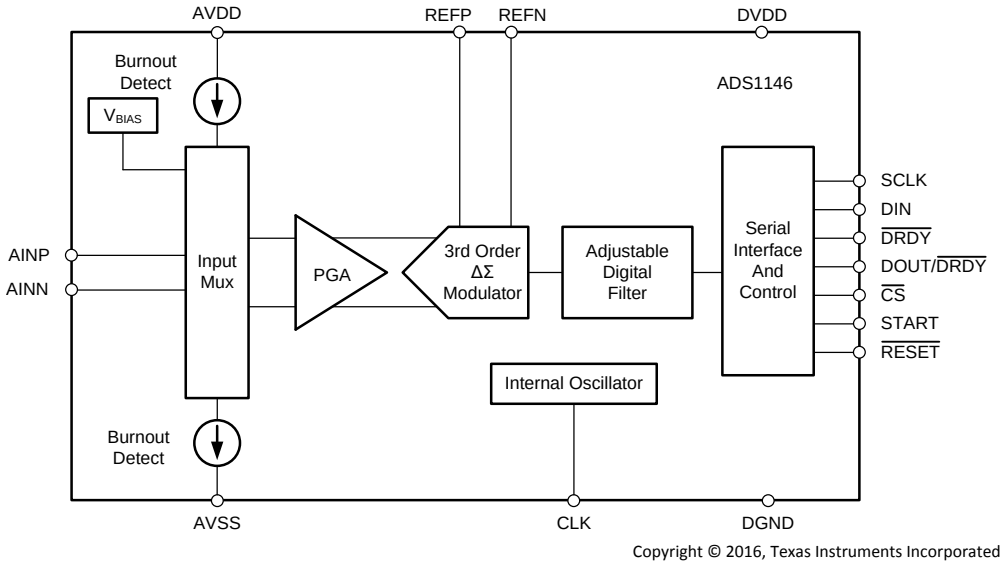


図 17. ADS1146 Diagram

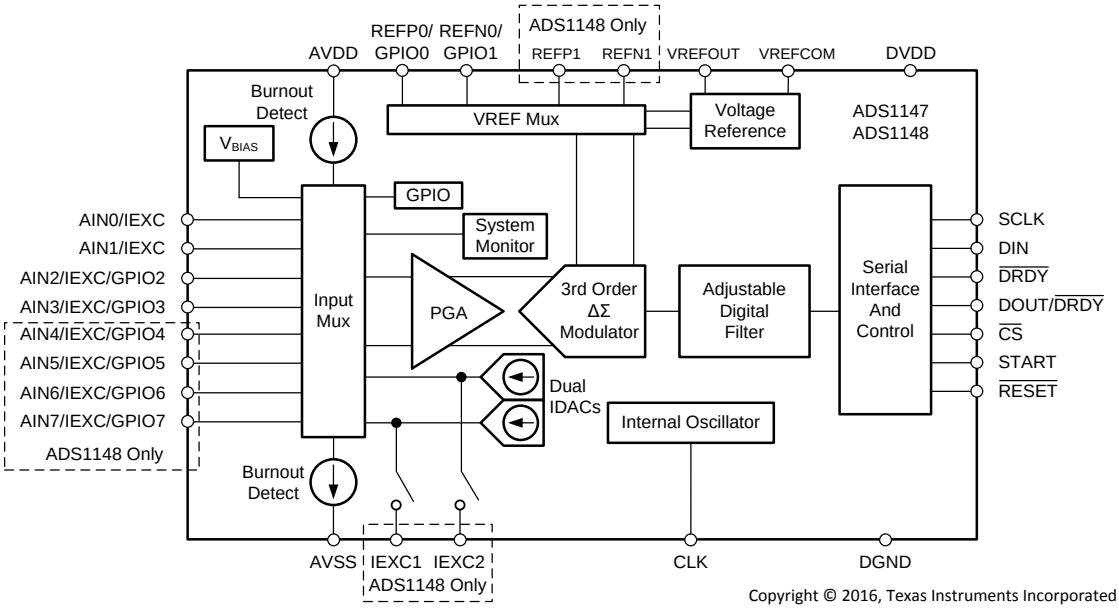


図 18. ADS1147 and ADS1148 Diagram

9.3 Feature Description

9.3.1 ADC Input and Multiplexer

The ADC measures the input signal through the onboard PGA. All analog inputs are connected to the internal AIN_P or AIN_N analog inputs through the analog multiplexer. 図 19 shows a block diagram of the analog input multiplexer.

The input multiplexer connects to eight (ADS1148) or four (ADS1147) analog inputs. Any analog input pin can be selected as the positive input or negative input through the MUX0 register, while the ADS1146 has AINP and AINN connections for a single differential channel. The multiplexer also allows the on-chip excitation current and bias voltage to be selected to a specific channel.

Through the input multiplexer, the ambient temperature (internal temperature sensor), AVDD, DVDD, and external reference can all be selected for measurement. See the *System Monitor* section for more details.

On the ADS1147 and ADS1148, the analog inputs can also be configured as general-purpose inputs and outputs (GPIOs). See the *General-Purpose Digital I/O* section for more details.

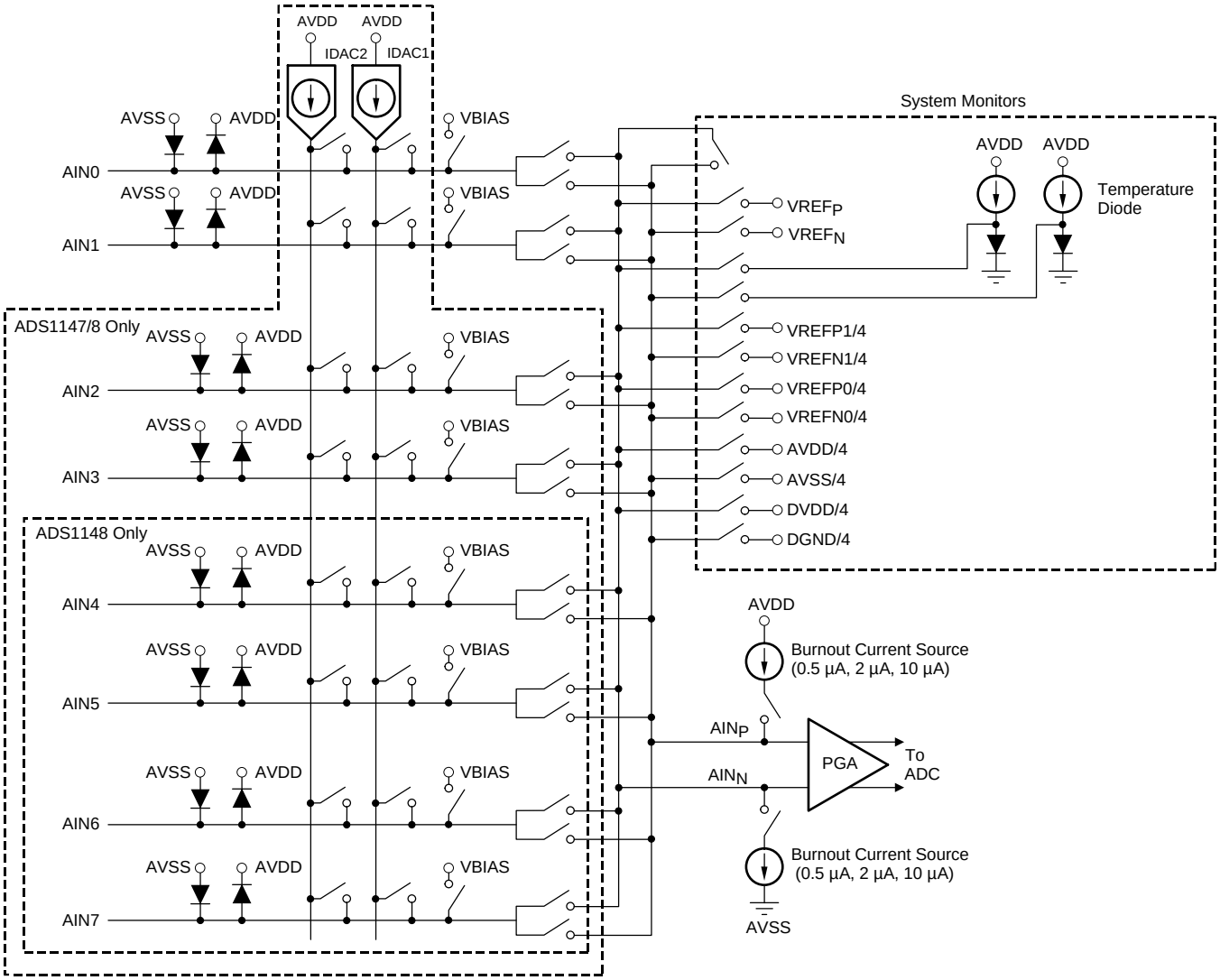


図 19. Analog Input Multiplexer Circuit

Feature Description (continued)

ESD diodes protect the ADC inputs. To prevent these diodes from turning on, make sure the voltages on the input pins do not go below AVSS by more than 100 mV, and do not exceed AVDD by more than 100 mV, as shown in 式 2. Note that the same caution is true if the inputs are configured to be GPIOs.

$$AVSS - 100\ mV < V_{(AINX)} < AVDD + 100\ mV \quad (2)$$

9.3.2 Low-Noise PGA

The ADS1146, ADS1147, and ADS1148 feature a low-drift, low-noise, high input impedance programmable gain amplifier (PGA). The PGA can be set to gains of 1, 2, 4, 8, 16, 32, 64, or 128 by register SYS0. 図 20 shows a simplified diagram of the PGA.

The PGA consists of two chopper-stabilized amplifiers (A1 and A2) and a resistor feedback network that sets the gain of the PGA. The PGA input is equipped with an electromagnetic interference (EMI) filter, as shown in 図 20. As with any PGA, ensure that the input voltage stays within the specified common-mode input range. The common-mode input (V_{CM}) must be within the range shown in 式 3.

$$\left(AVSS + 0.1\,V + \frac{V_{IN\,(MAX)} \cdot Gain}{2}\right) \le V_{CM} \le \left(AVDD - 0.1\,V - \frac{V_{IN\,(MAX)} \cdot Gain}{2}\right) \quad (3)$$

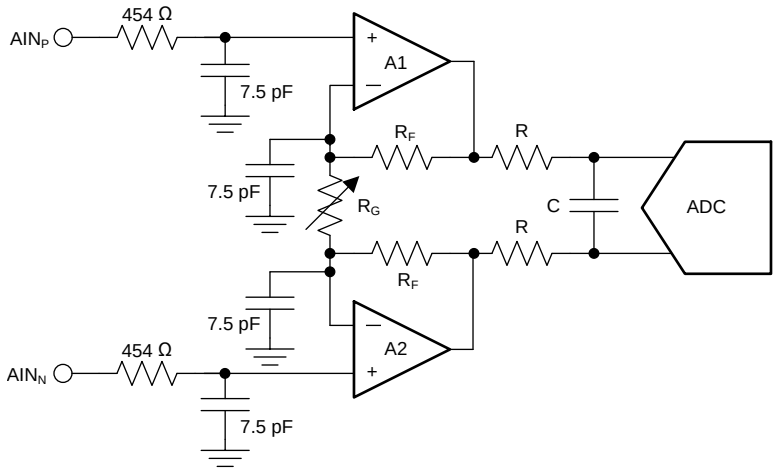


図 20. Simplified Diagram of the PGA

Gain is changed inside the device using a variable resistor, R_G. The differential full-scale input voltage range (FSR) of the PGA is defined by the gain setting and the reference voltage used, as shown in 式 4.

$$FSR = \pm V_{REF} / Gain \quad (4)$$

表 3 shows the corresponding full-scale input ranges when using the internal 2.048-V reference.

表 3. PGA Full-Scale Range

PGA GAIN SETTING	FSR
1	±2.048 V
2	±1.024 V
4	±0.512 V
8	±0.256 V
16	±0.128 V
32	±0.064 V
64	±0.032 V
128	±0.016 V

9.3.2.1 PGA Common-Mode Voltage Requirements

To stay within the linear operating range of the PGA, the input signals must meet certain requirements that are discussed in this section.

The outputs of both amplifiers (A1 and A2) in 図 20 can not swing closer to the supplies (AVSS and AVDD) than 100 mV. If the outputs OUT_P and OUT_N are driven to within 100 mV of the supply rails, the amplifiers saturate and consequently become nonlinear. To prevent this nonlinear operating condition, the output voltages must meet 式 5.

$$AVSS + 0.1\ V \le V_{(OUTN)},\ V_{(OUTP)} \le AVDD - 0.1\ V \quad (5)$$

Translating the requirements of 式 5 into requirements referred to the PGA inputs (AIN_P and AIN_N) is beneficial because there is no direct access to the outputs of the PGA. The PGA employs a symmetrical design; therefore, the common-mode voltage at the output of the PGA can be assumed to be the same as the common-mode voltage of the input signal, as shown in 図 21.

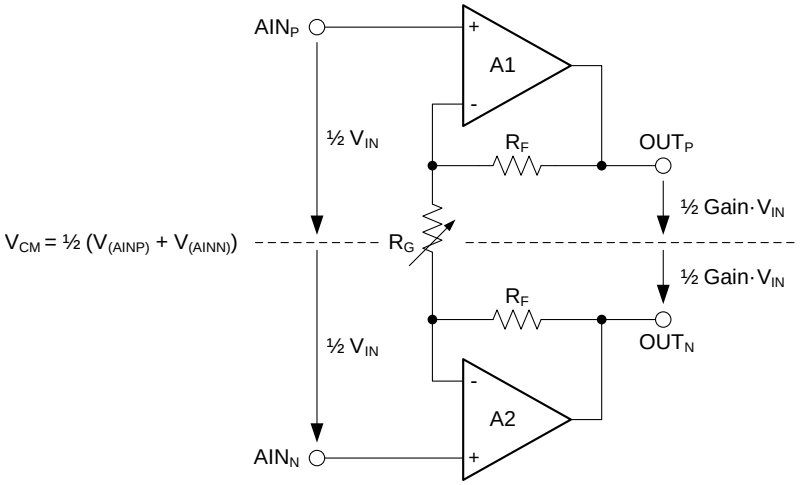


図 21. PGA Common-Mode Voltage

The common-mode voltage is calculated using 式 6.

$$V_{CM} = ½\ (V_{(AINP)} + V_{(AINN)}) = ½\ (V_{(OUTP)} + V_{(OUTN)}) \quad (6)$$

The voltages at the PGA inputs (AIN_P and AIN_N) can be expressed as 式 7 and 式 8.

$$V_{(AINP)} = V_{CM} + ½\ V_{IN} \quad (7)$$

$$V_{(AINN)} = V_{CM} - ½\ V_{IN} \quad (8)$$

The output voltages ($V_{(OUTP)}$ and $V_{(OUTN)}$) can then be calculated as 式 9 and 式 10.

$$V_{(OUTP)} = V_{CM} + ½\ Gain \times V_{IN} \quad (9)$$

$$V_{(OUTN)} = V_{CM} - ½\ Gain \times V_{IN} \quad (10)$$

The requirements for the output voltages of amplifiers A1 and A2 (式 5) can now be translated into requirements for the input common-mode voltage range using 式 9 and 式 10, which are given in 式 11 and 式 12.

$$V_{CM\ (MIN)} \ge AVSS + 0.1\ V + ½\ Gain \times V_{IN\ (MAX)} \quad (11)$$

$$V_{CM\ (MAX)} \le AVDD - 0.1\ V - ½\ Gain \times V_{IN\ (MAX)} \quad (12)$$

To calculate the minimum and maximum common-mode voltage limits, the maximum differential input voltage ($V_{IN\ (MAX)}$) that occurs in the application must be used. $V_{IN\ (MAX)}$ can be less than the maximum possible full-scale value.

9.3.2.2 PGA Common-Mode Voltage Calculation Example

The following paragraphs explain how to apply 式 11 and 式 12 to a hypothetical application. The setup for this example is AVDD = 3.3 V, AVSS = 0 V, and gain = 16, using an external reference, V_{REF} = 2.5 V. The maximum possible differential input voltage $V_{IN} = (V_{(AINP)} - V_{(AINN)})$ that can be applied is then limited to the full-scale range of FSR = ±2.5 V / 16 = ±0.156 V. Consequently, 式 11 and 式 12 yield an allowed V_{CM} range of 1.35 V ≤ V_{CM} ≤ 1.95 V.

If the sensor signal connected to the inputs in this hypothetical application does not make use of the entire full-scale range but is limited to $V_{IN\ (MAX)}$ = ±0.1 V, for example, then this reduced input signal amplitude relaxes the V_{CM} restriction to 0.9 V ≤ V_{CM} ≤ 2.4 V.

In the case of a fully-differential sensor signal, each input (AIN_P, AIN_N) can swing up to ±50 mV around the common-mode voltage ($V_{(AINP)}$ + $V_{(AINN)}$) / 2, which must remain between the limits of 0.9 V and 2.4 V. The output of a symmetrical wheatstone bridge is an example of a fully-differential signal. 図 22 shows a situation where the common-mode voltage of the input signal is at the lowest limit. $V_{(OUTN)}$ is exactly at 0.1 V in this case. Any further decrease in common-mode voltage (V_{CM}) or increase in differential input voltage (V_{IN}) drives $V_{(OUTN)}$ below 0.1 V and saturates amplifier A2.

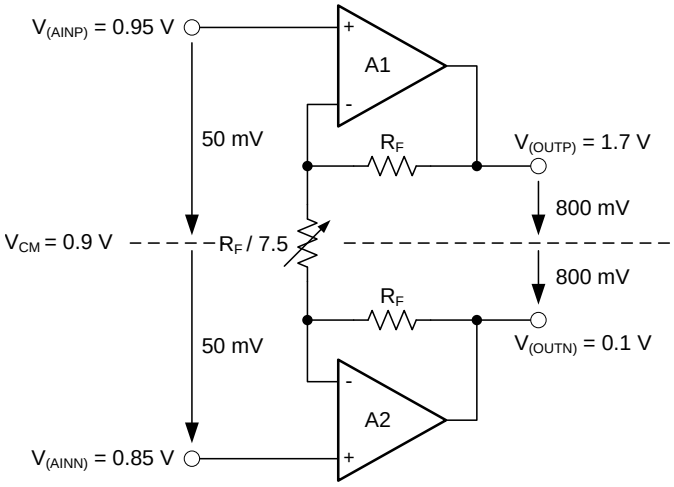


図 22. Example Where V_{CM} is at the Lowest Limit

In contrast, the signal of an RTD is of a pseudo-differential nature (if implemented as shown in the *3-Wire RTD Measurement System* section), where the negative input is held at a constant voltage other than 0 V and only the voltage on the positive input changes. When a pseudo-differential signal must be measured, the negative input in this example must be biased at a voltage from 0.85 V to 2.35 V. The positive input can then swing up to $V_{IN\ (MAX)}$ = 100 mV above the negative input. In this case, the common-mode voltage changes at the same time the voltage on the positive input changes. That is, while the input signal swings between 0 V ≤ V_{IN} ≤ $V_{IN\ (MAX)}$, the common-mode voltage swings between $V_{(AINN)}$ ≤ V_{CM} ≤ $V_{(AINN)}$ + ½ $V_{IN\ (MAX)}$. Satisfying the common-mode voltage requirements for the maximum input voltage $V_{IN\ (MAX)}$ ensures the requirements are met throughout the entire signal range.

図 23 and 図 24 show examples of both fully-differential and pseudo-differential signals, respectively.

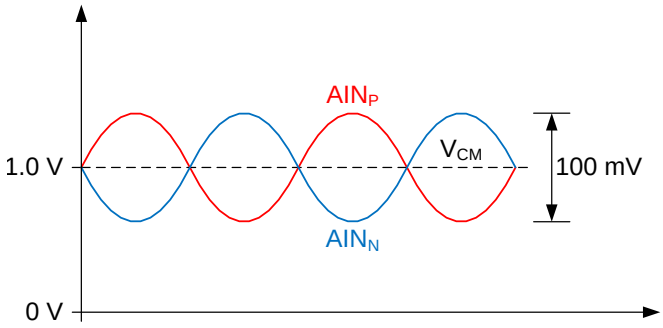


図 23. Fully-Differential Input Signal

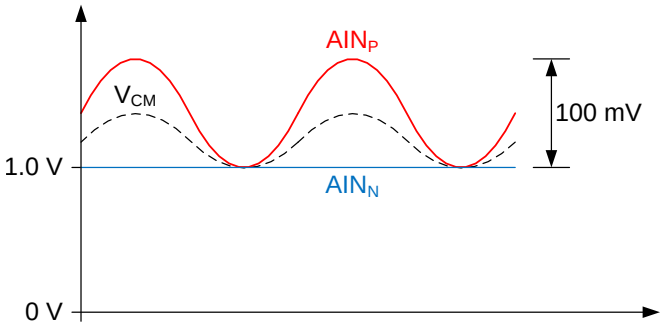


図 24. Pseudo-Differential Input Signal

注

With a unipolar power supply, the input range does not extend to the ground. 式 11 and 式 12 show the common-mode voltage requirements.

- $V_{CM\ (MIN)} \geq AVSS + 0.1\ V + ½\ Gain \times V_{IN\ (MAX)}$
- $V_{CM\ (MAX)} \leq AVDD - 0.1\ V - ½\ Gain \times V_{IN\ (MAX)}$

9.3.2.3 *Analog Input Impedance*

The device inputs are buffered through a high-input impedance PGA before they reach the ΔΣ modulator. For the majority of applications, the input current is minimal and can be neglected. However, because the PGA is chopper-stabilized for noise and offset performance, the input impedance is best described as a small absolute input current. The absolute input current for selected channels is approximately proportional to the selected modulator clock. 表 4 shows the typical values for these currents with a differential voltage coefficient and the corresponding input impedances over data rate.

表 4. Typical Values for Analog Input Current Over Data Rate(1)

CONDITION	ABSOLUTE INPUT CURRENT	EFFECTIVE INPUT IMPEDANCE
DR = 5 SPS, 10 SPS, 20 SPS	± (0.5 nA + 0.1 nA/V)	5000 MΩ
DR = 40 SPS, 80 SPS, 160 SPS	± (2 nA + 0.5 nA/V)	1200 MΩ
DR = 320 SPS, 640 SPS, 1 kSPS	± (4 nA + 1 nA/V)	600 MΩ
DR = 2 kSPS	± (8 nA + 2 nA/V)	300 MΩ

(1) Input current with V_{CM} = 2.5 V, T_A = 25°C, AVDD = 5 V, and AVSS = 0 V.

9.3.3 Clock Source

The device can use either the internal oscillator or an external clock. Connect the CLK pin to DGND before power-on or reset to activate the internal oscillator. Connecting an external clock to the CLK pin at any time deactivates the internal oscillator, with the device then operating on the external clock. After the device switches to the external clock, it cannot be switched back to the internal oscillator without cycling the power supplies or resetting the device.

9.3.4 Modulator

A third-order delta-sigma modulator is used in the ADS1146, ADS1147, and ADS1148 devices. The modulator converts the analog input voltage into a pulse code modulated (PCM) data stream. To save power, the modulator clock runs from 32 kHz up to 512 kHz for different data rates, as shown in 表 5.

表 5. Modulator Clock Frequency for Different Data Rates

DATA RATE (SPS)	MODULATOR RATE (f_{MOD})(1) (kHz)	f_{CLK}/f_{MOD}
5, 10, 20	32	128
40, 80, 160	128	32
320, 640, 1000	256	16
2000	512	8

(1) Using the internal oscillator or an external 4.096-MHz clock.

9.3.5 Digital Filter

The ADC uses linear-phase finite impulse response (FIR) digital filters that can be adjusted for different output data rates. The digital filter always settles in a single cycle.

表 6 shows the exact data rates when an external clock equal to 4.096 MHz is used. Also shown is the signal –3-dB bandwidth, and the 50-Hz and 60-Hz attenuation. For good 50-Hz or 60-Hz rejection, use a data rate of 20 SPS or slower.

The frequency responses of the digital filter are shown in 図 25 to 図 35. 図 28 shows a detailed view of the filter frequency response from 48 Hz to 62 Hz for a 20-SPS data rate. All filter plots are generated with a 4.096-MHz external clock.

Data rates and digital filter frequency responses scale proportionally with changes in the system clock frequency. The internal oscillator frequency has a variation, as specified in the *Electrical Characteristics* section, that also affects data rates and the digital filter frequency response.

表 6. Digital Filter Specifications(1)

NOMINAL DATA RATE	ACTUAL DATA RATE	–3-dB BANDWIDTH	ATTENUATION			
			f_{IN} = 50 Hz ±0.3 Hz	f_{IN} = 60 Hz ±0.3 Hz	f_{IN} = 50 Hz ±1 Hz	f_{IN} = 60 Hz ±1 Hz
5 SPS	5.018 SPS	2.26 Hz	–106 dB	–74 dB	–81 dB	–69 dB
10 SPS	10.037 SPS	4.76 Hz	–106 dB	–74 dB	–80 dB	–69 dB
20 SPS	20.075 SPS	14.8 Hz	–71 dB	–74 dB	–66 dB	–68 dB
40 SPS	40.15 SPS	9.03 Hz	—	—	—	—
80 SPS	80.301 SPS	19.8 Hz	—	—	—	—
160 SPS	160.6 SPS	118 Hz	—	—	—	—
320 SPS	321.608 SPS	154 Hz	—	—	—	—
640 SPS	643.21 SPS	495 Hz	—	—	—	—
1000 SPS	1000 SPS	732 Hz	—	—	—	—
2000 SPS	2000 SPS	1465 Hz	—	—	—	—

(1) Values shown for f_{CLK} = 4.096 MHz.

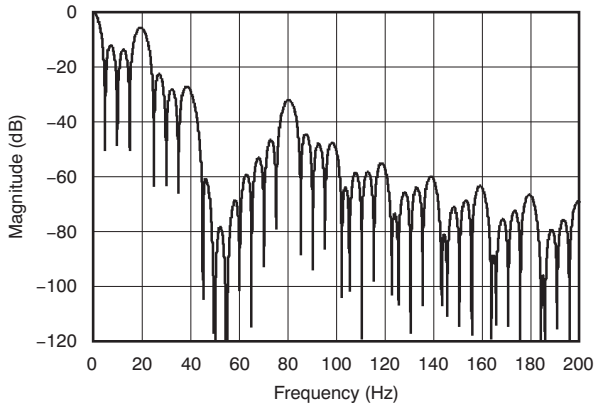


図 25. Filter Profile With Data Rate = 5 SPS

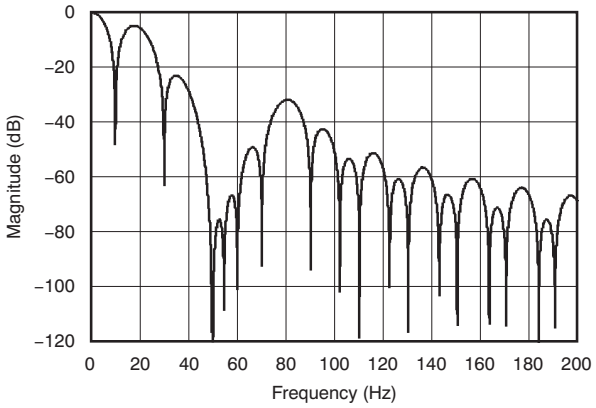


図 26. Filter Profile With Data Rate = 10 SPS

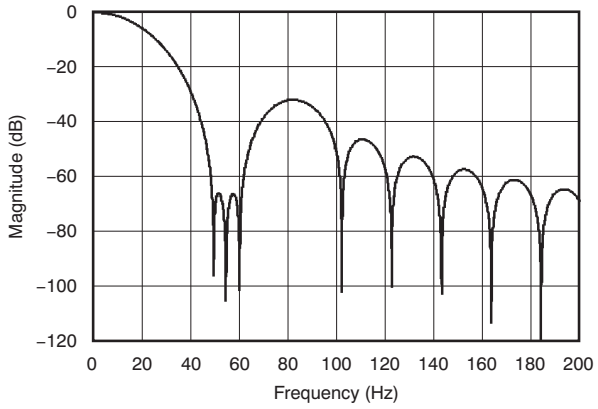


図 27. Filter Profile With Data Rate = 20 SPS

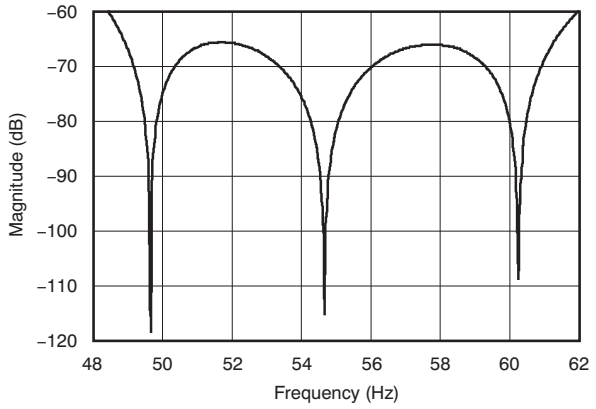


図 28. Detailed View of Filter Profile With Data Rate = 20 SPS Between 48 Hz and 62 Hz

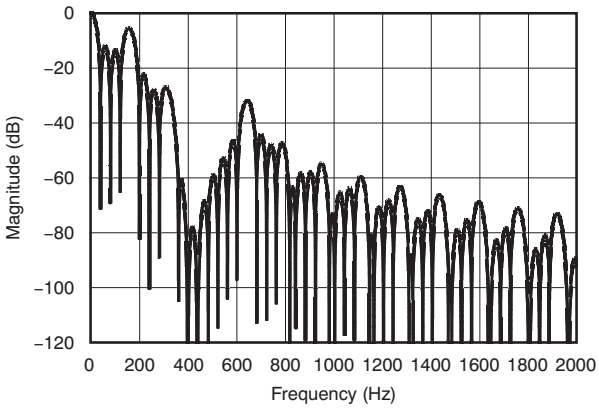


図 29. Filter Profile With Data Rate = 40 SPS

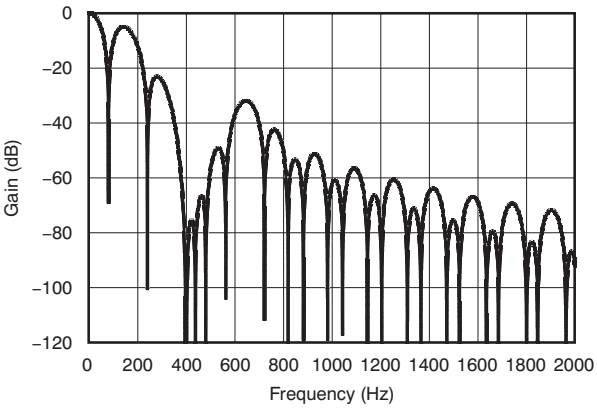


図 30. Filter Profile With Data Rate = 80 SPS

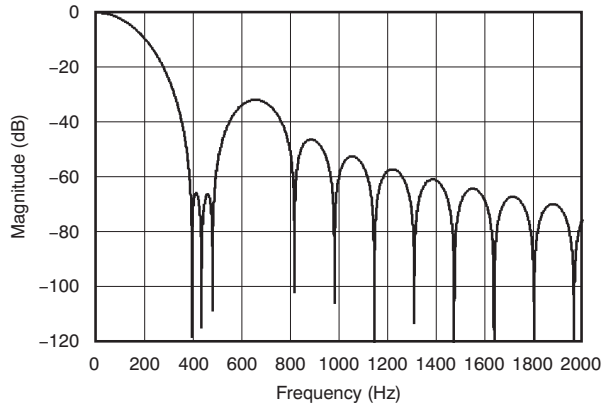


図 31. Filter Profile With Data Rate = 160 SPS

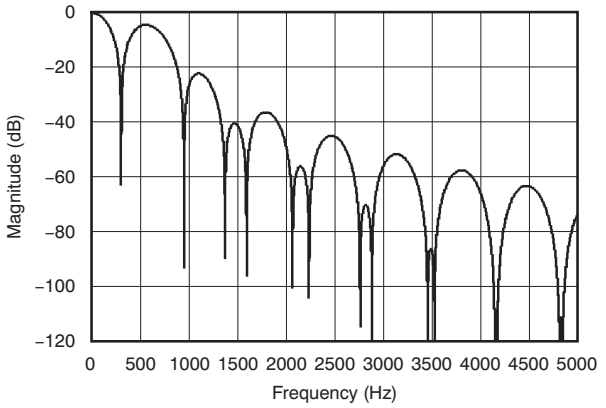


図 32. Filter Profile With Data Rate = 320 SPS

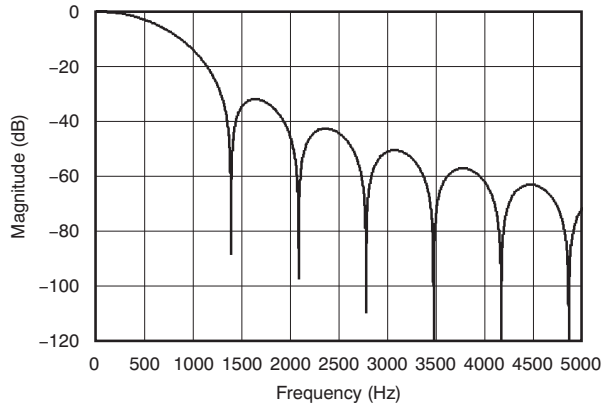


図 33. Filter Profile With Data Rate = 640 SPS

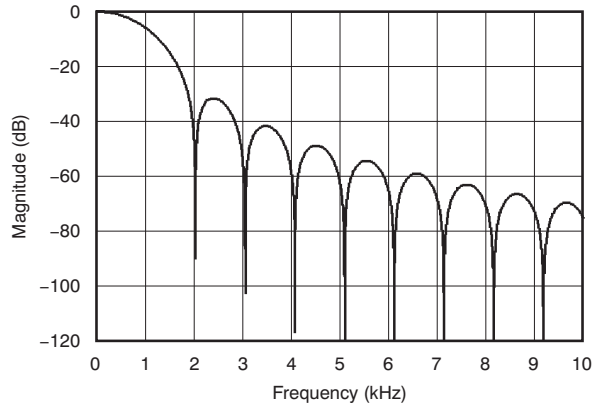


図 34. Filter Profile With Data Rate = 1 kSPS

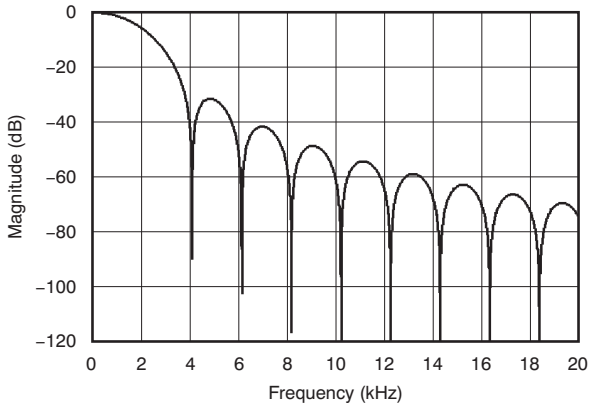


図 35. Filter Profile With Data Rate = 2 kSPS

9.3.6 Voltage Reference Input

The voltage reference for the device is the differential voltage between REFP and REFN, given by 式 13.

$$V_{REF} = V_{(REFP)} - V_{(REFN)} \quad (13)$$

In the case of the ADS1146, these pins are dedicated inputs. For the ADS1147 and ADS1148, there is a multiplexer that selects the reference inputs, as shown in 図 36. The reference inputs use buffers to increase the input impedance.

As with the analog inputs, REFP0 and REFN0 can be configured as digital I/Os on the ADS1147 and ADS1148.

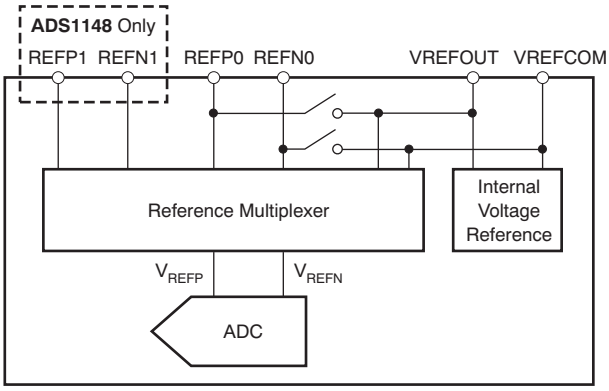


図 36. Reference Input Multiplexer

The reference input circuit has ESD diodes to protect the inputs. To prevent the diodes from turning on, make sure the voltage on the reference input pin is not less than AVSS – 100 mV, and does not exceed AVDD + 100 mV, as shown in 式 14.

$$AVSS - 100\ mV < (V_{(REFP)} \text{ or } V_{(REFN)}) < AVDD + 100\ mV \quad (14)$$

9.3.7 Internal Voltage Reference

The ADS1147 and ADS1148 have an internal voltage reference with a low temperature coefficient. The output of the voltage reference is 2.048 V (nominal) with the capability of both sourcing and sinking up to 10 mA of current.

The voltage reference must have a capacitor connected between VREFOUT and VREFCOM. The value of the capacitance must be in the range of 1 µF to 47 µF. Large values provide more filtering of the reference; however, the turnon time increases with capacitance, as shown in 表 7. For stability reasons, VREFCOM must have a low-impedance path to AC ground nodes, such as GND. VREFCOM may be connected to AVSS (for a ±2.5-V analog power supply) as long as AVSS has a low-impedance path less than 10 Ω to AC ground. In case this impedance is higher than 10 Ω, connect a capacitor of at least 0.1 µF between VREFCOM and an AC ground node (for example, GND).

注

Because time is required for the voltage reference to settle to the final voltage, take care when the device is turned off between conversions. Allow adequate time for the internal reference to fully settle before starting a new conversion.

表 7. Internal Reference Settling Time

VREFOUT CAPACITOR	SETTLING ERROR	TIME TO REACH THE SETTLING ERROR
1 µF	±0.5%	70 µs
	±0.1%	110 µs
4.7 µF	±0.5%	290 µs
	±0.1%	375 µs
47 µF	±0.5%	2.2 ms
	±0.1%	2.4 ms

The internal reference is controlled by the MUX1 register; by default, the internal reference is off after power up (see the *ADS1147 and ADS1148 Detailed Register Definitions* section for more details). Therefore, the internal reference must first be turned on and then connected through the internal reference multiplexer. Because the internal reference is used to generate the current reference for the excitation current sources, it must be turned on before the excitation currents become available.

9.3.8 Excitation Current Sources

The ADS1147 and ADS1148 provide two matched excitation current sources (IDACs) for RTD applications. For three-wire RTD applications, the matched current sources can be used to cancel the errors caused by sensor lead resistance. The output current of the IDACs can be programmed to 50 µA, 100 µA, 250 µA, 500 µA, 750 µA, 1000 µA, or 1500 µA.

The two matched current sources can be connected to dedicated current output pins IEXC1 and IEXC2 (ADS1148 only), or to any analog input pin (ADS1147 and ADS1148); see the *ADS1147 and ADS1148 Detailed Register Definitions* section for more information. Both current sources can be connected to the same pin. The internal reference must be turned on and the proper amount of capacitance applied to VREFOUT when using the excitation current sources.

9.3.9 Sensor Detection

To help detect a possible sensor malfunction, the device provides selectable current sources (0.5 µA, 2 µA, or 10 µA) to act as burn-out current sources. When enabled, one current source sources current to the selected positive analog input (AIN_P) while the other current source sinks current from the selected negative analog input (AIN_N).

In case of an open circuit in the sensor, these burn-out current sources pull the positive input towards AVDD and the negative input towards AVSS, resulting in a full-scale reading. A full-scale reading may also indicate that the sensor is overloaded or that the reference voltage is absent. A near-zero reading may indicate a shorted sensor. The absolute value of the burn-out current sources typically varies by ±10% and the internal multiplexer adds a small series resistance. Therefore, distinguishing a shorted sensor condition from a normal reading can be difficult, especially if an RC filter is used at the inputs. In other words, even if the sensor is shorted, the voltage drop across the external filter resistance and the residual resistance of the multiplexer causes the output to read a value higher than zero.

The ADC readings of a functional sensor may be corrupted when the burn-out current sources are enabled. TI recommends disabling the burn-out current sources when performing the precision measurement, and only enabling them to test for sensor fault conditions.

9.3.10 Bias Voltage Generation

A selectable bias voltage is provided for use with unbiased thermocouples. The bias voltage is (AVDD + AVSS) / 2 and can be applied to any analog input channel through the internal input multiplexer. 表 8 lists the bias voltage turnon times for different sensor capacitances.

The internal bias voltage generator, when selected on multiple channels, causes them to be internally shorted. Because of this, take care to limit the amount of current that may flow through the device. TI recommends that under no circumstances must more than 5 mA be allowed to flow through this path. This applies when the device is in operation and when it is powered down.

表 8. Bias Voltage Settling Time

SENSOR CAPACITANCE	SETTLING TIME
0.1 µF	220 µs
1 µF	2.2 ms
10 µF	22 ms
200 µF	450 ms

9.3.11 General-Purpose Digital I/O

The ADS1148 has eight pins and the ADS1147 has four pins that serve a dual purpose as either analog inputs or GPIOs.

Three registers control the function of the GPIO pins. Use the GPIO configuration register (IOCFG) to enable a pin as a GPIO pin. The GPIO direction register (IODIR) configures the GPIO pin as either an input or an output. Finally, the GPIO data register (IODAT) contains the GPIO data. If a GPIO pin is configured as an input, the respective IODAT[x] bit reads the status of the pin; if a GPIO pin is configured as an output, write the output status to the respective IODAT[x] bit. For more information about the use of GPIO pins, see the *ADS1147 and ADS1148 Detailed Register Definitions* section.

図 37 shows a diagram of how these functions are combined onto a single pin. Note that when the pin is configured as a GPIO, the corresponding logic is powered from AVDD and AVSS. When the ADS1147 and ADS1148 are operated with bipolar analog supplies, the GPIO outputs bipolar voltages. Care must be taken loading the GPIO pins when used as outputs because large currents can cause droop or noise on the analog supplies.

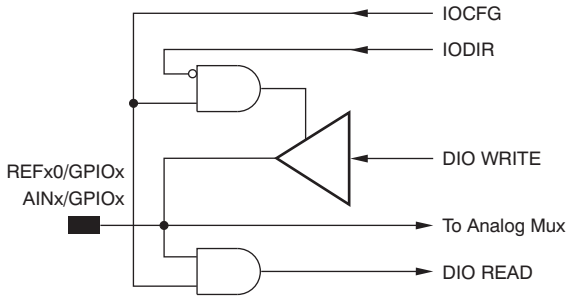


図 37. Analog and Data Interface Pin

9.3.12 System Monitor

The ADS1147 and ADS1148 provide a system monitor function. This function can measure the analog power supply, digital power supply, external voltage reference, or ambient temperature. Note that the system monitor function provides a coarse result. When the system monitor is enabled, the analog inputs are disconnected.

9.3.12.1 Power-Supply Monitor

The system monitor can measure the analog or digital power supply. When measuring the power supply (V_{SP}), the resulting conversion is approximately 1/4 of the actual power supply voltage, as shown in 式 15.

$$\text{Conversion Result} = (V_{SP} / 4) / V_{REF} \quad (15)$$

9.3.12.2 External Voltage Reference Monitor

The ADC can measure the external voltage reference. In this configuration, the monitored external voltage reference (V_{REX}) is connected to the analog input. The result (conversion code) is approximately 1/4 of the actual reference voltage, as shown in 式 16.

$$\text{Conversion Result} = (V_{REX} / 4) / V_{REF} \quad (16)$$

注

The internal reference voltage must be enabled when measuring an external voltage reference using the system monitor.

9.3.12.3 Ambient Temperature Monitor

On-chip diodes provide temperature-sensing capability. When selecting the temperature monitor function, the anodes of two diodes are connected to the ADC. Typically, the difference in diode voltage is 118 mV at T_A = 25°C with a temperature coefficient of 405 µV/°C.

9.4 Device Functional Modes

9.4.1 Power Up

When DVDD is powered up, the internal power-on reset module generates a pulse that resets all digital circuitry. All the digital circuits are held in a reset state for 2^{16} system clocks to allow the analog circuits and the internal digital power supply to settle. SPI communication cannot occur until the internal reset is released.

9.4.2 Reset

When the $\overline{\text{RESET}}$ pin goes low, the device is immediately reset. All registers are restored to default values. The device stays in reset mode as long as the $\overline{\text{RESET}}$ pin stays low. When the $\overline{\text{RESET}}$ pin goes high, the ADC comes out of reset mode and is able to convert data. After the $\overline{\text{RESET}}$ pin goes high, the digital filter and the registers are held in a reset state for 0.6 ms when f_{CLK} = 4.096 MHz. Therefore, valid SPI communication can only be resumed 0.6 ms after the $\overline{\text{RESET}}$ pin goes high; see 図 4. When the $\overline{\text{RESET}}$ pin goes low, the clock selection is reset to the internal oscillator.

A reset can also be performed by the RESET command through the serial interface and is functionally the same as using the $\overline{\text{RESET}}$ pin. For information about using the RESET command, see the *RESET* section.

9.4.3 Power-Down Mode

Power consumption is reduced to a minimum by placing the device into power-down mode. There are two ways to put the device into power-down mode: using the SLEEP command and taking the START pin low.

During power-down mode, the internal reference status depends on the setting of the VREFCON bits in the MUX1 register; see the *Register Maps* section for details.

9.4.4 Conversion Control

The START pin provides precise control of conversions. Pulse the START pin high to begin a conversion, as shown in 図 38 and 表 9. The conversion completion is indicated by the $\overline{\text{DRDY}}$ pin going low and with the DOUT/$\overline{\text{DRDY}}$ pin when the DRDY MODE bit is 1 in the IDAC0 register. When the conversion completes, the device automatically powers down. During power down, the conversion result can be retrieved; however, START must be taken high before communicating with the configuration registers. The device stays powered down until the START pin is returned high to begin a new conversion. When the START pin returned high, the decimation filter is held in a reset state for 32 modulator clock cycles internally to allow the analog circuits to settle.

Holding the START pin high configures the device to continuously convert as shown in 図 39.

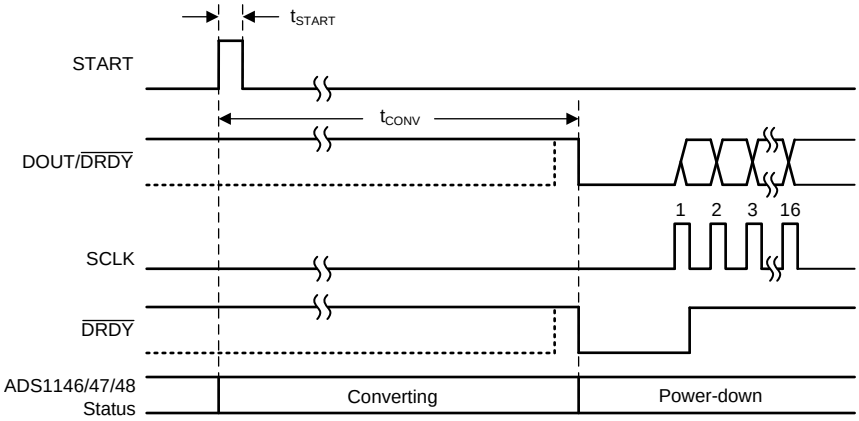
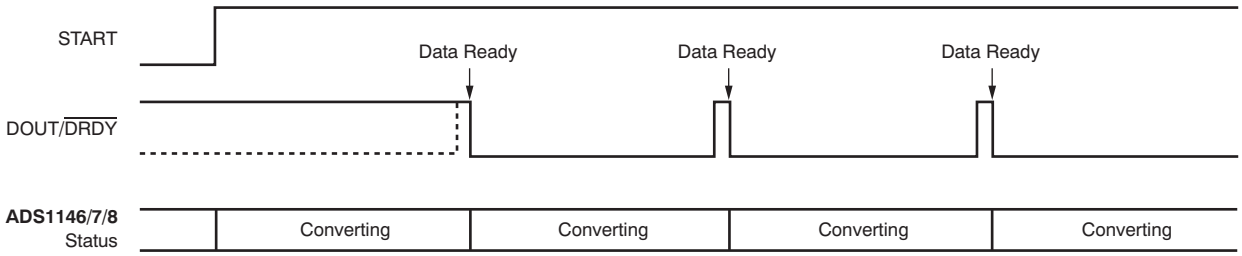


図 38. Timing for Single Conversion Using START Pin

表 9. START Pin Conversion Times for 図 38 (1)

SYMBOL	DESCRIPTION	DATA RATE (SPS)	VALUE	UNIT
t_{CONV}	Time from START pulse to $\overline{DRDY}$ and DOUT/$\overline{DRDY}$ going low	5	200.295	ms
		10	100.644	ms
		20	50.825	ms
		40	25.169	ms
		80	12.716	ms
		160	6.489	ms
		320	3.247	ms
		640	1.692	ms
		1000	1.138	ms
		2000	0.575	ms

(1) For f_{CLK} = 4.096MHz



NOTE: SCLK held low in this example.

図 39. Timing for Conversion with START Pin High

With the START pin held high, the ADC converts the selected input channels continuously. This configuration continues until the START pin is taken low. The START pin can also be used to perform synchronized measurements for multi-channel applications by pulsing the START pin. With multiple devices, if each device receives the START pin pulse at the same time, all devices start a conversion on the rise of the start pin. If all devices are operating with the same data rate, all of the devices complete the conversion at the same time.

Conversions can also be initiated through SPI commands. Similar to using the START pin, the device can be put into a power-down mode using the SLEEP command. Functionally, this is similar to taking the START pin low. To initiate a conversion, the WAKEUP command powers up the ADC and starts a conversion, similar to returning the START pin high. Note that the START pin must be held high to use commands to control conversions. Do not combine using the START pin and using commands to control conversions.

Also, sending a SYNC command immediately starts a new ADC conversion. For the SYNC command, the digital filter is reset, starting a new conversion without completing the previous conversion. This is useful in synchronizing conversions from multiple devices or maintaining periodic timing from multiple channels.

Similarly, writing to any of the first four registers (MUX0, VBIAS, MUX1, or SYS0; addresses 00h to 04h) automatically resets the digital filter. A change in any of these registers makes the appropriate setup change in the device, but also restarts the conversion similar to a SYNC command.

9.4.4.1 Settling Time for Channel Multiplexing

The device is a true single-cycle settling $\Delta\Sigma$ converter. The first data available after the start of a conversion are fully settled and valid for use, provided that the input signal has settled to its final result. The time required to settle is roughly equal to the inverse of the data rate. The exact time depends on the specific data rate and the operation that resulted in the start of a conversion; see 表 10 for specific values.

9.4.4.2 Channel Cycling and Overload Recovery

When cycling through channels, take care when configuring the device to ensure that settling occurs within one cycle. For setups that cycle through MUX channels, but do not change PGA and data rate settings, changing the MUX0 register is sufficient. However, when changing PGA and data rate settings, ensure that an overload condition cannot occur during the data transmission. When configuration register data are transferred to the device, new settings become active at the end of each byte sent. Therefore, a brief overload condition can occur during the transmission of configuration data after the completion of the MUX0 byte and before the completion of the SYS0 byte. This temporary overload can result in intermittent incorrect readings. To ensure that an overload does not occur, it may be necessary to split the communication into two separate communications allowing the change of the SYS0 register before the change of the MUX0 register.

In the event of an overloaded state, take care to ensure single-cycle settling into the next cycle. Because the device implements a chopper-stabilized PGA, changing data rates during an overload state can cause the chopper to become unstable. This instability results in slow settling time. To prevent this slow settling, always change the PGA setting or MUX setting to a non-overloaded state before changing the data rate.

9.4.4.3 Single-Cycle Settling

The ADS1146, ADS1147, and ADS1148 are capable of single-cycle settling across all gains and data rates. However, to achieve single-cycle settling at 2 kSPS, special care must be taken with respect to the interface using WREG to change a configuration register. When operating at 2 kSPS, the SCLK period must not exceed 520 ns, and the time between the beginning of writing a register byte data and the beginning of a subsequent register byte data must not exceed 4.2 µs. Additionally, when performing multiple individual write commands to the first four registers, wait at least 64 oscillator clocks before initiating another write command.

9.4.4.4 Digital Filter Reset Operation

Apart from the RESET command and the $\overline{\text{RESET}}$ pin, the digital filter is reset automatically when either a write operation to the MUX0, VBIAS, MUX1, or SYS0 registers is performed, when a SYNC command is issued, or the START pin is taken high.

The filter is reset four system clocks (t_{CLK}) after the falling edge of the seventh SCLK of the SYNC command. Similarly, if any write operation takes place in the MUX0 register, regardless of whether the register value changed or not, the filter is reset after the completion of the MUX0 write.

If any write activity takes place in the VBIAS, MUX1, or SYS0 registers, regardless of whether the register value changed or not, the filter is reset. The reset pulse lasts for 32 modulator clocks after the completion of the write operation. If there are multiple write operations, the resulting reset pulse may be viewed as the ANDed result of the different active low pulses created individually by each action.

表 10 shows the conversion time after a filter reset. Note that this time depends on the operation initiating the reset. Also, the first conversion after a filter reset has a slightly different time than the second and subsequent conversions.

表 10. Data Conversion Time

NOMINAL DATA RATE (SPS)	EXACT DATA RATE (SPS)	FIRST DATA CONVERSION TIME AFTER FILTER RESET				SECOND AND SUBSEQUENT CONVERSION TIME AFTER FILTER RESET	
		SYNC COMMAND, MUX0 REGISTER WRITE		HARDWARE RESET, RESET COMMAND, START PIN HIGH, WAKEUP COMMAND, VBIAS, MUX1, or SYS0 REGISTER WRITE			
		(ms)(1)	NO. OF SYSTEM CLOCK CYCLES	(ms)(1)	NO. OF SYSTEM CLOCK CYCLES	(ms)(1)	NO. OF SYSTEM CLOCK CYCLES
5	5.019	199.258	816160	200.26	820265	199.250	816128
10	10.038	99.633	408096	100.635	412201	99.625	408064
20	20.075	49.820	204064	50.822	208169	49.812	204032
40	40.151	24.920	102072	25.172	103106	24.906	102016
80	80.301	12.467	51064	12.719	52098	12.453	51008
160	160.602	6.241	25560	6.492	26594	6.226	25504
320	321.608	3.124	12796	3.250	13314	3.109	12736
640	643.216	1.569	6428	1.695	6946	1.554	6368
1000	1000.000	1.014	4156	1.141	4674	1.000	4096
2000	2000.000	0.514	2108	0.578	2370	0.500	2048

(1) For f_{CLK} = 4.096 MHz.

9.4.5 Calibration

The conversion data are scaled by offset and gain registers before yielding the final output code. As shown in 図 40, the output of the digital filter is first subtracted by the offset register (OFC) and then multiplied by the full-scale register (FSC) to digitally scale the gain. A digital clipping circuit ensures that the output code does not exceed 16 bits. 式 17 shows the scaling.

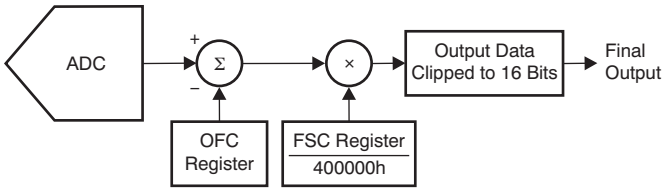


図 40. Calibration Block Diagram

$$\text{Final Output Data} = (\text{Input} - \text{OFC}[2:1]) \times \frac{\text{FSC}[2:0]}{400000\text{h}} \quad (17)$$

The values of the offset and full-scale registers are set by writing to them directly, or they are set automatically by calibration commands.

The offset and gain calibration features are intended for correction of minor system level offset and gain errors. When entering manual values into the calibration registers, take care to avoid scaling down the gain register to values far below a scaling factor of 1.0. Under extreme situations it is possible to over-range the ADC. Avoid encountering situations where analog inputs are connected to voltages greater than V_{REF} / Gain.

Take care when increasing digital gain with the FSC register. When implementing custom digital gains less than 20% higher than nominal and offsets less than 40% of full scale, no special care is required. When operating at digital gains greater than 20% higher than nominal and offsets greater than 40% of full scale, make sure that the offset and gain registers follow the conditions of 式 18.

$$\frac{2\text{ V}}{\text{Gain Scaling}} - 1.251\text{ V} > \left|\text{Offset Scaling}\right| \quad (18)$$

9.4.5.1 Offset Calibration Register: OFC[2:0]

The offset calibration is a 24-bit word, composed of three 8-bit registers. The offset is in twos complement format with a maximum positive value of 7FFFFFh and a maximum negative value of 800000h. The upper 16 bits, OFC[2:1], are the most important bits of the offset calibration register for calibration and can correct offsets ranging from –FS to +FS, as shown in 表 11. The lower eight bits, OFC[0], provide sub-LSB correction and are used by the calibration commands. If a calibration command is issued and the offset register is then read for storage and re-use later, it is recommended that all 24 bits of the OFC be used. When the calibration commands are not used and the offset is corrected by writing a user-calculated value to the OFC register, it is recommended that only OFC[2:1] be used and that OFC[0] be left as all zeros. A register value of 000000h provides no offset correction.

Note that while the offset calibration register value can correct offsets ranging from –FS to +FS (as shown in 表 11), avoid overloading the analog inputs.

表 11. Final Output Code vs Offset Calibration Register Setting

OFFSET REGISTER	FINAL OUTPUT CODE WITH V_{IN} = 0 (1)
7FFFFFh	8000h
000100h	FFFFh
000000h	0000h
FFFF00h	0001h
800000h	7FFFh

(1) Excludes effects of noise and inherent offset errors.

9.4.5.2 Full-Scale Calibration Register: FSC[2:0]

The full-scale or gain calibration is a 24-bit word composed of three 8-bit registers. The full-scale calibration value is 24-bit, straight binary, normalized to 1.0 at code 400000h. 表 12 summarizes the scaling of the full-scale register. Note that while the full-scale calibration register can correct gain errors > 1 (with gain scaling < 1), make sure to avoid overloading the analog inputs.

表 12. Gain Correction Factor vs Full-Scale Calibration Register Setting

FULL-SCALE REGISTER	GAIN SCALING
800000h	2
400000h	1
200000h	0.5
000000h	0

9.4.5.3 Calibration Commands

The device provide commands for three types of calibration: system gain calibration, system offset calibration and self offset calibration. Where absolute accuracy is required, TI recommends performing a calibration after power up, a change in temperature, a change of gain and in some cases a change in channel. At the completion of calibration, the DRDY signal goes low indicating the calibration has completed. The first data after calibration are always valid. If the START pin is taken low or a SLEEP command is issued after any calibration command, the devices powers down after completing calibration.

After a calibration has started, allow the calibration to complete before issuing any other commands (other than the SLEEP command). Issuing commands during a calibration can result in corrupted data. If this occurs, either resend the calibration command that was aborted or issue a device reset.

9.4.5.3.1 System Offset and Self Offset Calibration

System offset calibration corrects both internal and external offset errors. The system offset calibration is initiated by sending the SYSOCAL command while applying a zero differential input voltage (V_{IN} = 0 V) to the selected analog inputs with the inputs set within the specified input common-mode range, ideally at mid-supply.

The self offset calibration is initiated by sending the SELFOCAL command. During self offset calibration, the selected inputs are disconnected from the internal circuitry and a zero differential signal is applied internally, connecting the inputs to mid-supply. With both offset calibrations the offset calibration register (OFC) is updated afterwards. When either offset calibration command is issued, the device stops the current conversion and starts the calibration procedure immediately. An offset calibration must be performed before a gain calibration.

9.4.5.3.2 System Gain Calibration

System gain calibration corrects for gain error in the signal path. The system gain calibration is initiated by sending the SYSGCAL command while applying a full-scale input to the selected analog inputs. Afterwards the full-scale calibration register (FSC) is updated. When a system gain calibration command is issued, the device stops the current conversion and starts the calibration procedure immediately.

9.4.5.4 Calibration Timing

When calibration is initiated, the device performs 16 consecutive data conversions and averages the results to calculate the calibration value. This provides a more accurate calibration value. The time required for calibration is shown in 表 13 and can be calculated using 式 19.

$$\text{Calibration Time} = t_{CAL} = \frac{50}{f_{CLK}} + \frac{32}{f_{MOD}} + \frac{16}{f_{DATA}} \quad (19)$$

表 13. Calibration Time vs Data Rate

DATA RATE (SPS)	CALIBRATION TIME (t_{CAL}) (ms)(1)
5	3201.01
10	1601.01
20	801.012
40	400.26
80	200.26
160	100.14
320	50.14
640	25.14
1000	16.14
2000	8.07

(1) For f_{CLK} = 4.096 MHz.

9.5 Programming

9.5.1 Digital Interface

The device provides an SPI-compatible serial communication interface plus a data ready signal ($\overline{DRDY}$). Communication is full-duplex with the exception of a few limitations in regards to the RREG command and the RDATA command. These limitations are explained in detail in the *Commands* section. For the basic serial interface timing characteristics, see 図 1 and 図 2 of this document.

9.5.1.1 Chip Select ($\overline{CS}$)

The $\overline{CS}$ pin activates SPI communication. $\overline{CS}$ must be low before data transactions and must stay low for the entire SPI communication period. When $\overline{CS}$ is high, the DOUT/$\overline{DRDY}$ pin enters a high-impedance state. Therefore, reading and writing to the serial interface are ignored and the serial interface is reset. $\overline{DRDY}$ pin operation is independent of $\overline{CS}$. $\overline{DRDY}$ still indicates that a new conversion has completed and is forced high as a response to SCLK, even if $\overline{CS}$ is high.

Taking $\overline{CS}$ high deactivates only the SPI communication with the device. Data conversion continues and the $\overline{DRDY}$ signal can be monitored to check if a new conversion result is ready. A master device monitoring the $\overline{DRDY}$ signal can select the appropriate slave device by pulling the $\overline{CS}$ pin low.

Programming (continued)

9.5.1.2 Serial Clock (SCLK)

SCLK provides the clock for serial communication. SCLK is a Schmitt-trigger input, but TI recommends keeping SCLK as free from noise as possible to prevent glitches from inadvertently shifting the data. Data are shifted into DIN on the falling edge of SCLK and shifted out of DOUT on the rising edge of SCLK.

9.5.1.3 Data Input (DIN)

DIN is used along with SCLK to send data to the device. Data on DIN are shifted into the device on the falling edge of SCLK.

The communication of this device is full-duplex in nature. The device monitors commands shifted in even when data are being shifted out. Data that are present in the output shift register are shifted out when sending in a command. Therefore, make sure that whatever is being sent on the DIN pin is valid when shifting out data. When no command is to be sent to the device when reading out data, send the NOP command on DIN.

9.5.1.4 Data Ready ($\overline{DRDY}$)

The $\overline{DRDY}$ pin goes low to indicate a new conversion is complete, and the conversion result is stored in the conversion result buffer. SCLK must be held low for t_{DTS} after the $\overline{DRDY}$ low transition (see 図 2) so that the conversion result is loaded into both the result buffer and the output shift register. Therefore, issue no commands during this time frame if the conversion result is to be read out later. This constraint applies only when $\overline{CS}$ is asserted and the device is in RDATAC mode. When $\overline{CS}$ is not asserted, SPI communication with other devices on the SPI bus does not affect loading of the conversion result. After the $\overline{DRDY}$ pin goes low, it is forced high on the first falling edge of SCLK (so that the $\overline{DRDY}$ pin can be polled for 0 instead of waiting for a falling edge). If the $\overline{DRDY}$ pin is not taken high by clocking in SCLKs after it falls low, a short high pulse for a duration of t_{PWH} indicates new data are ready.

9.5.1.5 Data Output and Data Ready (DOUT/$\overline{DRDY}$)

The DOUT/$\overline{DRDY}$ pin has two modes: data out (DOUT) only, or DOUT combined with data ready ($\overline{DRDY}$). The DRDY MODE bit determines the function of this pin and can be found in the *ID register* in the ADS1146 and the *IDAC0 register* in the ADS1147 and ADS1148. In either mode, the DOUT/$\overline{DRDY}$ pin goes to a high-impedance state when $\overline{CS}$ is taken high.

When the DRDY MODE bit is set to 0, this pin functions as DOUT only. Data are clocked out on the rising edge of SCLK, MSB first (as shown in 図 41).

When the DRDY MODE bit is set to 1, this pin functions as both DOUT and $\overline{DRDY}$. Data are shifted out as with DOUT, but the pin adds the $\overline{DRDY}$ function. Note that this mode is not operational when the device is in stop read data continuous mode when the SDATAC command is given.

The DRDY MODE bit modifies only the DOUT/$\overline{DRDY}$ pin functionality. The $\overline{DRDY}$ pin functionality remains unaffected.

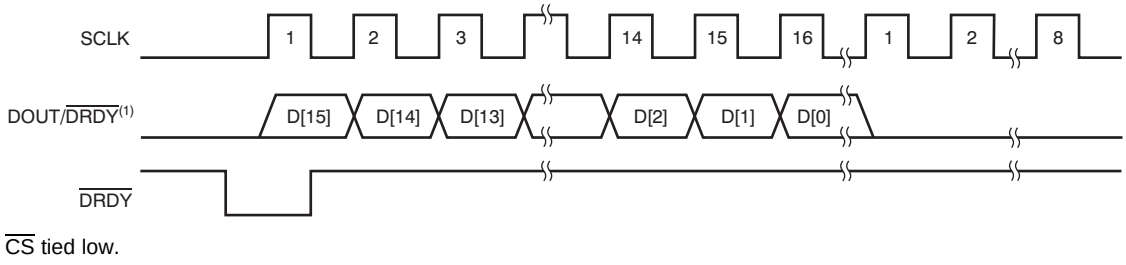
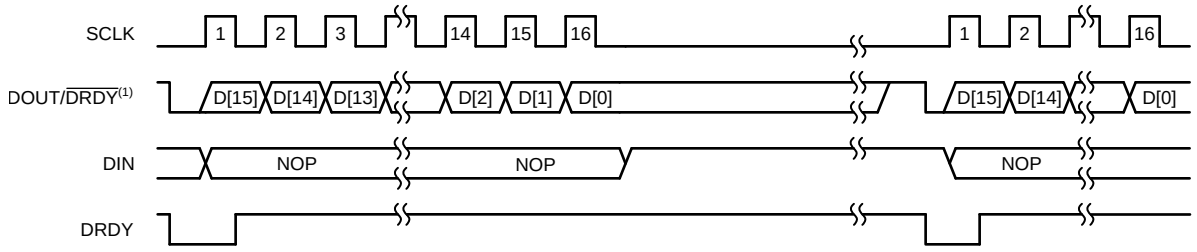


図 41. Data Retrieval With the DRDY MODE Bit = 0 (Disabled)

When the DRDY MODE bit is enabled and a new conversion is complete, DOUT/$\overline{DRDY}$ goes low if it is high. If it is already low, then DOUT/$\overline{DRDY}$ goes high and then goes low (as shown in 図 42). Similar to the $\overline{DRDY}$ pin, a falling edge on the DOUT/$\overline{DRDY}$ pin signals that a new conversion result is ready. After DOUT/$\overline{DRDY}$ goes low, the data can be clocked out by providing 16 SCLKs if the device is in read data continuous mode. To force DOUT/$\overline{DRDY}$ high (so that DOUT/$\overline{DRDY}$ can be polled for a 0 instead of waiting for a falling edge), a no

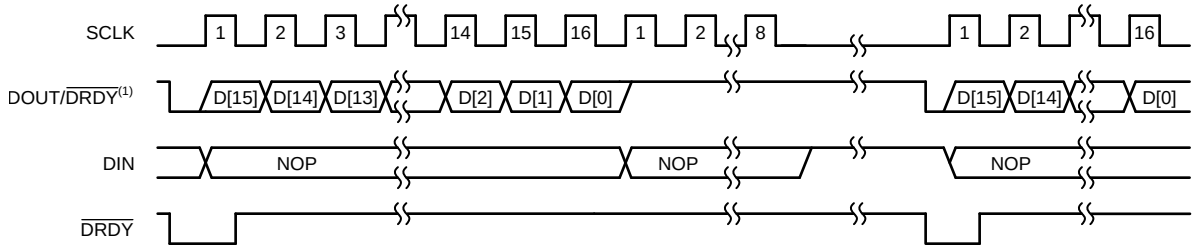
Programming (continued)

operation command (NOP) or any other command that does not load the data output register can be sent after reading out the data. Because SCLKs can only be sent in multiples of eight, a NOP can be sent to force DOUT/DRDY high if no other command is pending. The DOUT/DRDY pin goes high after the first rising edge of SCLK after reading the conversion result completely (as shown in 図 43). The same condition also applies after an RREG command. After all the register bits have been read out, the first rising edge of SCLK forces DOUT/DRDY high. 図 44 shows an example where sending an extra NOP command after reading out a register with an RREG command forces the DOUT/DRDY pin high.



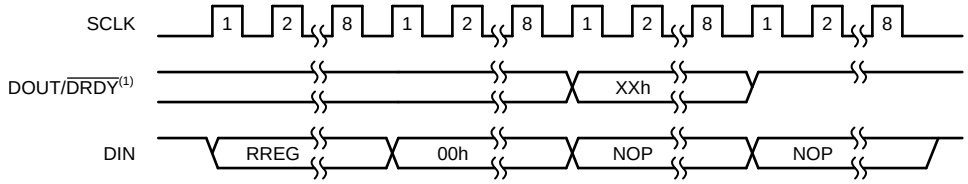
CS tied low.

図 42. Data Retrieval With the DRDY MODE Bit = 1 (Enabled)



DRDY MODE bit enabled, CS tied low.

図 43. DOUT/DRDY Forced High After Retrieving the Conversion Result



DRDY MODE bit enabled, CS tied low.

図 44. DOUT/DRDY Forced High After Reading Register Data

9.5.1.6 SPI Reset

SPI communication is reset in several ways. To reset the serial interface (without resetting the registers or the digital filter), the CS pin can be pulled high. Taking the RESET pin low resets the serial interface along with all the other digital functions. This also returns all registers to their default values and start a new conversion.

In systems where CS is tied low permanently, register writes must always be fully completed in 8-bit increments. If a glitch on SCLK disrupts SPI communications, commands are not recognized by the device. The device implements a timeout function for all listed commands in the event that data are corrupted and the CS pin is permanently tied low. The SPI timeout resets the interface if idle for 64 conversion cycles.

Programming (continued)

9.5.1.7 SPI Communication During Power-Down Mode

When the START pin is low or the device is in power-down mode, only the RDATA, RDATAC, SDATAC, WAKEUP, and NOP commands can be issued. The RDATA command can be used to repeatedly read the last conversion result during power-down mode. Other commands do not function because the internal clock is shut down to save power during power-down mode.

9.5.2 Data Format

The device provides 16 bits of data in binary twos complement format. The size of one code (LSB) is calculated using 式 20.

$$1\ \text{LSB} = (2 \times V_{REF} / \text{Gain}) / 2^{16} = +\text{FS} / 2^{15} \quad (20)$$

A positive full-scale (FS) input [$V_{IN} \geq (+\text{FS} - 1\ \text{LSB}) = (V_{REF} / \text{Gain} - 1\ \text{LSB})$] produces an output code of 7FFFh and a negative full-scale input ($V_{IN} \leq -\text{FS} = -V_{REF} / \text{Gain}$) produces an output code of 8000h. The output clips at these codes for signals that exceed full-scale. 表 14 summarizes the ideal output codes for different input signals.

表 14. Ideal Output Code vs Input Signal

INPUT SIGNAL, V_{IN} ($AIN_P - AIN_N$)	IDEAL OUTPUT CODE(1)
≥ FS ($2^{15} - 1$) / 2^{15}	7FFFh
FS / 2^{15}	0001h
0	0000h
–FS / 2^{15}	FFFFh
≤ –FS	8000h

(1) Excludes effects of noise, linearity, offset, and gain errors.

図 45 shows the mapping of the analog input signal to the output codes.

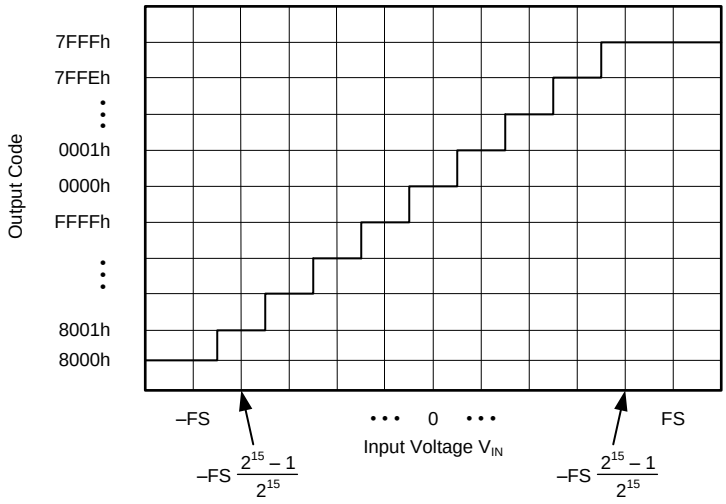


図 45. Code Transition Diagram

9.5.3 Commands

The device offers 13 commands to control device operation as shown in 表 15. Some of the commands are stand-alone commands (WAKEUP, SLEEP, SYNC, RESET, SYSOCAL, SYSGCAL, and SELFOCAL). There are three additional commands used to control the read of data from the device (RDATA, RDATAC, and SDATAC). The commands to read (RREG) and write (WREG) configuration register data from and to the device require additional information as part of the instruction. A no-operation command (NOP) can be used to clock out data from the device without clocking in a command.

Operands:

- n = number of registers to be read or written (number of bytes – 1)
- r = register (0 to 15)
- x = don't care

表 15. SPI Commands

COMMAND(1)	DESCRIPTION	1st COMMAND BYTE	2nd COMMAND BYTE
WAKEUP	Exit power down mode	0000 000x (00h, 01h)	
SLEEP	Enter power down mode	0000 001x (02h, 03h)	
SYNC	Synchronize ADC conversions	0000 010x (04h, 05h)	0000 010x (04,05h)
RESET	Reset to default values	0000 011x (06h, 07h)	
NOP	No operation	1111 1111 (FFh)	
RDATA	Read data once	0001 001x (12h, 13h)	
RDATAC	Read data continuous mode	0001 010x (14h, 15h)	
SDATAC	Stop read data continuous mode	0001 011x (16h, 17h)	
RREG	Read from register *rrrr*	0010 rrrr (2xh)	0000 nnnn
WREG	Write to register *rrrr*	0100 rrrr (4xh)	0000 nnnn
SYSOCAL	System offset calibration	0110 0000 (60h)	
SYSGCAL	System gain calibration	0110 0001 (61h)	
SELFOCAL	Self offset calibration	0110 0010 (62h)	
Restricted	Restricted command. Never send to the device.	1111 0001 (F1h)	

(1) When the START pin is low or the device is in power-down mode, only the RDATA, RDATAC, SDATAC, WAKEUP, and NOP commands can be issued.

9.5.3.1 WAKEUP (0000 000x)

Use the WAKEUP command to power up the device after a SLEEP command. After execution of the WAKEUP command, the device powers up on the falling edge of the eighth SCLK.

9.5.3.2 SLEEP (0000 001x)

The SLEEP command places the device into power-down mode. When the SLEEP command is issued, the device completes the current conversion and then goes into power-down mode. Note that this command does not automatically power down the internal voltage reference; see the VREFCON bits in the *MUX1* section for each device for further details.

To exit power-down mode, issue the WAKEUP command. Single conversions can be performed by issuing a WAKEUP command followed by a SLEEP command.

Both WAKEUP and SLEEP are the software command equivalents of using the START pin to control the device, as shown in 図 46.

注

If the START pin is held low, a WAKEUP command does not power up the device. When using the SLEEP command, $\overline{CS}$ must be held low for the duration of the power-down mode.

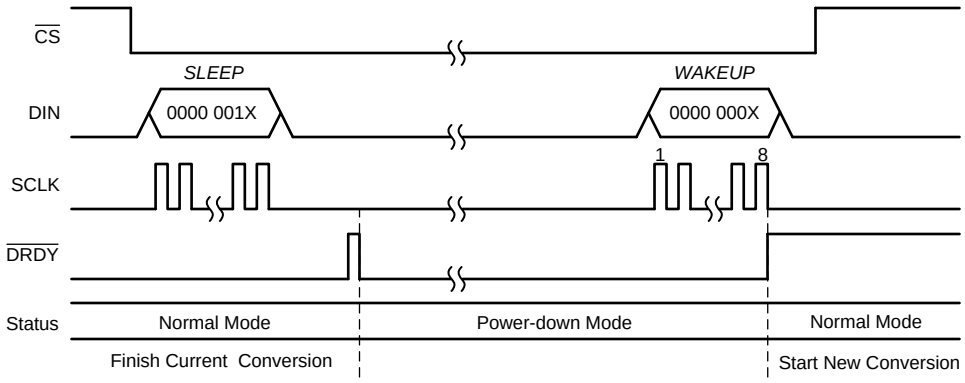


図 46. SLEEP and WAKEUP Commands Operation

9.5.3.3 SYNC (0000 010x)

The SYNC command resets the ADC digital filter and starts a new conversion. The $\overline{\text{DRDY}}$ pin from multiple devices connected to the same SPI bus can be synchronized by issuing a SYNC command to all of devices simultaneously.

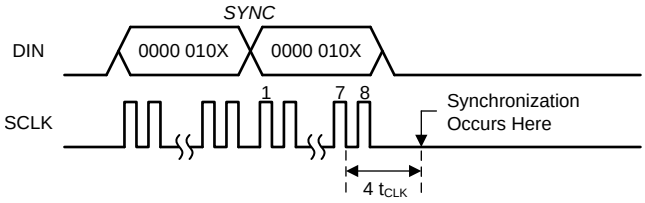


図 47. SYNC Command Operation

9.5.3.4 RESET (0000 011x)

The RESET command restores the registers to the respective default values. This command also resets the digital filter. RESET is the command equivalent of using the $\overline{\text{RESET}}$ pin to reset the device. However, the RESET command does not reset the serial interface. If the RESET command is issued when the serial interface is out of synchonization due to a glitch on SCLK, the device does not reset. The $\overline{\text{CS}}$ pin can be used to reset the serial interface first, and then a RESET command can be issued to reset the device. The RESET command holds the registers and the decimation filter in a reset state for 0.6 ms when the system clock frequency is 4.096 MHz, similar to the hardware reset. Therefore, SPI communication can only be started 0.6 ms after the RESET command is issued, as shown in 図 48.

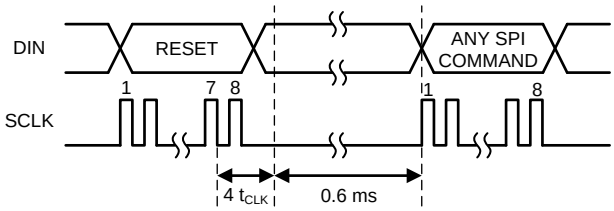


図 48. SPI Communication after an SPI Reset

9.5.3.5 RDATA (0001 001x)

The RDATA command loads the most recent conversion result into the output register. After issuing this command, the conversion result is read out by sending 16 SCLKs, as shown in 図 49. This command also works in RDATAC mode.

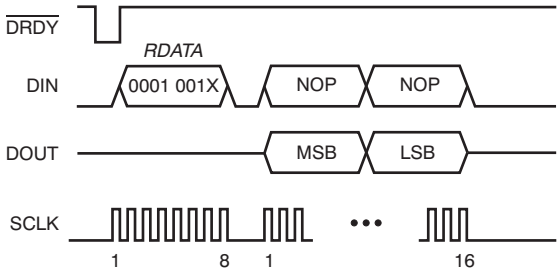


図 49. Figure Read Data Once

When performing multiple reads of the conversion result, the RDATA command can be sent when the last eight bits of the conversion result are being shifted out during the course of the first read operation by taking advantage of the duplex communication nature of the serial interface, as shown in 図 50.

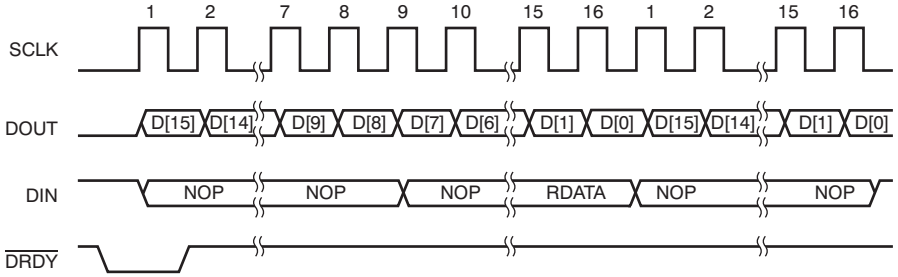


図 50. Using RDATA in Full-Duplex Mode

9.5.3.6 RDATAC (0001 010x)

The RDATAC command enables read data continuous mode. This is the default mode after a power up or reset. In read data continuous mode, new conversion results are automatically loaded onto DOUT. The conversion result can be received from the device after the DRDY signal goes low by sending 16 SCLKs. It is not necessary to read back all the bits, as long as the number of bits read out is a multiple of eight. The RDATAC command must be issued after DRDY goes low, and the command takes effect on the next DRDY as shown in 図 51.

Be sure to complete data retrieval (conversion result or register read-back) before DRDY returns low, or the resulting data is corrupted. Successful register read operations in RDATAC mode require the knowledge of when the next DRDY falling edge occurs.

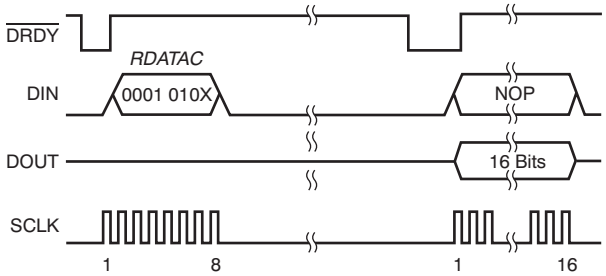


図 51. Read Data Continuously

9.5.3.7 SDATAC (0001 011x)

The SDATAC command terminates read data continuous mode. In stop read data continuous mode, the conversion result is not automatically loaded onto DOUT when $\overline{\text{DRDY}}$ goes low, and register read operations can be performed without interruption from new conversion results being loaded into the output shift register. Use the RDATA command to retrieve conversion data. The SDATAC command takes effect after the next $\overline{\text{DRDY}}$.

If $\overline{\text{DRDY}}$ is not actively monitored for data conversions, the stop read data continuous mode is the preferred method of reading data. In this mode, a read of ADC data is not interrupted by the completion of a new ADC conversion.

9.5.3.8 RREG (0010 rrrr, 0000 nnnn)

The RREG command outputs the data from up to 15 registers, starting with the register address specified as part of the instruction. The number of registers read is one plus the value of the second byte. If the count exceeds the remaining registers, the addresses wrap back to the beginning. The two byte command structure for RREG is listed below.

- First Command Byte: 0010 rrrr, where rrrr is the address of the first register to read.
- Second Command Byte: 0000 nnnn, where nnnn is the number of bytes to read –1.
- Byte(s): data read from the registers are clocked out with NOPs.

It is not possible to use the full-duplex nature of the serial interface when reading out the register data. For example, a SYNC command cannot be issued when reading out the VBIAS and MUX1 data, as shown in 図 52. Any command sent during the readout of the register data is ignored. Thus, TI recommends sending NOPs through DIN when reading out the register data.

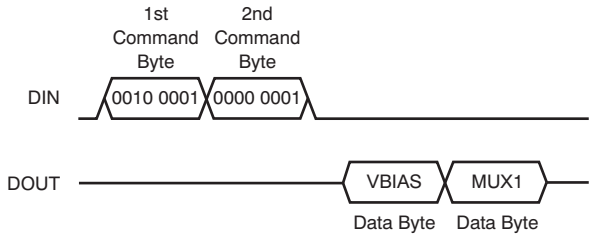


図 52. Read from Register

9.5.3.9 WREG (0100 rrrr, 0000 nnnn)

The WREG command writes to the registers, starting with the register specified as part of the instruction. The number of registers that are written is one plus the value of the second byte. The command structure for WREG is listed below.

- First Command Byte: 0100 rrrr, where rrrr is the address of the first register to be written.
- Second Command Byte: 0000 nnnn, where nnnn is the number of bytes to be written – 1.
- Byte(s): data to be written to the registers.

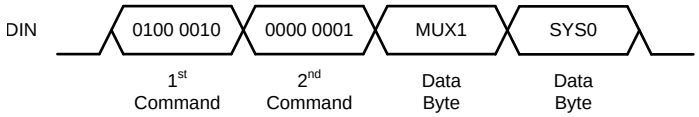


図 53. Write to Register

9.5.3.10 SYSOCAL (0110 0000)

The SYSOCAL command initiates a system offset calibration. For a system offset calibration, the inputs must be externally shorted to a voltage within the input common-mode range. The inputs must be near the mid-supply voltage of (AVDD + AVSS) / 2. The OFC register is updated when the command completes. Timing for the calibration commands can be found in 図 54.

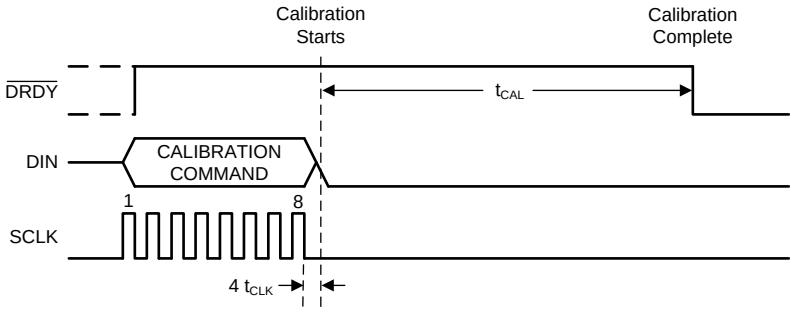


図 54. Calibration Command

9.5.3.11 SYSGCAL (0110 0001)

The SYSGCAL command initiates the system gain calibration. For a system gain calibration, the input must be set to full-scale. The FSC register is updated after this operation. Timing for the calibration commands can be found in 図 54.

9.5.3.12 SELFOCAL (0110 0010)

The SELFOCAL command initiates a self offset calibration. The device internally shorts the inputs to mid-supply and performs the calibration. The OFC register is updated after this operation. Timing for the calibration commands can be found in 図 54.

9.5.3.13 NOP (1111 1111)

This is a no-operation command. This is used to clock out data without clocking in a command.

9.5.3.14 Restricted Command (1111 0001)

This is a restricted command. This command must never be issued to the device.

9.6 Register Maps

9.6.1 ADS1146 Register Map

表 16. ADS1146 Register Map

ADDRESS	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00h	BCS	BCS[1:0]		0	0	0	0	0	1
01h	VBIAS	0	0	0	0	0	0	VBIAS[1:0]	
02h	MUX1	CLKSTAT	0	0	0	0	MUXCAL[2:0]		
03h	SYS0	0	PGA[2:0]			DR[3:0]			
04h	OFC0	OFC[7:0]							
05h	OFC1	OFC[15:8]							
06h	OFC2	OFC[23:16]							
07h	FSC0	FSC[7:0]							
08h	FSC1	FSC[15:8]							
09h	FSC2	FSC[23:16]							
0Ah	ID	ID[3:0]				DRDY MODE	0	0	0

9.6.2 ADS1146 Detailed Register Definitions

9.6.2.1 BCS—Burn-out Current Source Register (offset = 00h) [reset = 01h]

These bits control the sensor burn-out detect current source.

図 55. Burn-out Current Source Register

7	6	5	4	3	2	1	0
BCS[1:0]		0	0	0	0	0	1
R/W-0h		R-0h	R-0h	R-0h	R-0h	R-0h	R-1h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 17. Burn-out Current Source Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:6	BCS[1:0]	R/W	0h	**Burn-out Detect Current Source** These bits control the setting of the sensor burn-out detect current source 00: Burn-out current source off (default) 01: Burn-out current source on, 0.5 µA 10: Burn-out current source on, 2 µA 11: Burn-out current source on, 10 µA
5:0	RESERVED	R	01h	**Reserved** Always write 000001

9.6.2.2 VBIAS—Bias Voltage Register (offset = 01h) [reset = 00h]

This register enables a bias voltage on the analog inputs.

図 56. Bias Voltage Register

7	6	5	4	3	2	1	0
0	0	0	0	0	0	VBIAS[1:0]	
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 18. Bias Voltage Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:2	RESERVED	R	00h	**Reserved** Always write 000000
1	VBIAS[1]	R/W	0h	**VBIAS[1] Voltage Enable** A bias voltage of mid-supply (AVDD + AVSS) / 2 is applied to AINN 0: Bias voltage is not enabled (default) 1: Bias voltage is applied to AINN
0	VBIAS[0]	R/W	0h	**VBIAS[0] Voltage Enable** A bias voltage of mid-supply (AVDD + AVSS) / 2 is applied to AINP 0: Bias voltage is not enabled (default) 1: Bias voltage is applied to AINP

9.6.2.3 MUX—Multiplexer Control Register (offset = 02h) [reset = x0h]

図 57. Multiplexer Control Register

7	6	5	4	3	2	1	0
CLKSTAT	0	0	0	0	MUXCAL[2:0]		
R-xh	R-0h	R-0h	R-0h	R-0h	R/W-0h		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 19. Multiplexer Control Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	CLKSTAT	R	xh	**Clock status** This bit is read-only and indicates whether the internal oscillator or external clock is being used. 0: Internal oscillator in use 1: External clock in use
6:3	RESERVED	R	0h	**Reserved** Always write 0000
2:0	MUXCAL[2:0]	R/W	0h	**System Monitor Control** These bits are used to select a system monitor. The MUXCAL selection supercedes the selections from the VBIAS register. 000: Normal operation (default) 001: Offset calibration. The analog inputs are disconnected and AIN_P and AIN_N are internally connected to mid-supply (AVDD + AVSS) / 2. 010: Gain calibration. The analog inputs are connected to the voltage reference. 011: Temperature measurement. The inputs are connected to a diode circuit that produces a voltage proportional to the ambient temperature of the device.

表 20 lists the ADC input connection and PGA settings for each MUXCAL setting. The PGA setting reverts to the original SYS0 register setting when MUXCAL is taken back to normal operation or offset measurement.

表 20. MUXCAL Settings

MUXCAL[2:0]	PGA GAIN SETTING	ADC INPUT
000	Set by SYS0 register	Normal operation
001	Set by SYS0 register	Offset calibration: inputs shorted to mid-supply (AVDD + AVSS) / 2
010	Forced to 1	Gain calibration: $V_{(REFP)} - V_{(REFN)}$ (full-scale)
011	Forced to 1	Temperature measurement diode

9.6.2.4 SYS0—System Control Register 0 (offset = 03h) [reset = 00h]

図 58. System Control Register 0

7	6	5	4	3	2	1	0
0	PGA[2:0]			DR[3:0]			
R-0h	R/W-0h			R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 21. System Control Register 0 Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	RESERVED	R	0h	**Reserved** Always write 0
6:4	PGA[2:0]	R/W	0h	**Gain Setting for PGA** These bits determine the gain of the PGA 000: PGA = 1 (default) 001: PGA = 2 010: PGA = 4 011: PGA = 8 100: PGA = 16 101: PGA = 32 110: PGA = 64 111: PGA = 128
3:0	DR[3:0]	R/W	0h	**Data Output Rate Setting** These bits determine the data output rate of the ADC 0000: DR = 5 SPS (default) 0001: DR = 10 SPS 0010: DR = 20 SPS 0011: DR = 40 SPS 0100: DR = 80 SPS 0101: DR = 160 SPS 0110: DR = 320 SPS 0111: DR = 640 SPS 1000: DR = 1000 SPS 1001 to 1111: DR = 2000 SPS

9.6.2.5 OFC—Offset Calibration Coefficient Registers (offset = 04h, 05h, 06h) [reset = 00h, 00h, 00h]

These bits make up the offset calibration coefficient register of the ADS1146.

図 59. Offset Calibration Coefficient Registers

7	6	5	4	3	2	1	0
OFC[7:0]							
R/W-00h							
15	14	13	12	11	10	9	8
OFC[15:8]							
R/W-00h							
23	22	21	20	19	18	17	16
OFC[23:16]							
R/W-00h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 22. Offset Calibration Coefficient Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
23:0	OFC[23:0]	R/W	000000h	**Offset Calibration Register** Three registers compose the ADC 24-bit offset calibration word and is in twos complement format. The upper 16 bits (OFC[23:8]) can correct offsets ranging from -FS to +FS, while the lower eight bits (OFC[7:0]) provide sub-LSB correction. The ADC subtracts the register value from the conversion result before full scale operation.

9.6.2.6 FSC—Full-Scale Calibration Coefficient Registers (offset = 07h, 08h, 09h) [reset = 00h, 00h, 40h]

These bits make up the full-scale calibration coefficient register.

図 60. Full-Scale Calibration Coefficient Registers

7	6	5	4	3	2	4	0
FSC[7:0]							
R/W-00h							
15	14	13	12	11	10	9	8
FSC[15:8]							
R/W-00h							
23	22	21	20	19	18	17	16
FSC[23:16]							
R/W-40h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 23. Full-Scale Calibration Coefficient Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
23:0	FSC[23:0]	R/W	400000h	**Full-Scale Calibration Register** Three registers compose the ADC 24-bit full-scale calibration word. The 24-bit word is straight binary. The ADC divides the register value of the FSC register by 400000h to derive the scale factor for calibration. After the offset calibration, the ADC multiplies the scale factor by the conversion result.

9.6.2.7 ID—ID Register (offset = 0Ah) [reset = x0h]

図 61. ID Register

7	6	5	4	3	2	1	0
ID[3:0]				DRDY MODE	0	0	0
R-xh				R/W-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 24. ID Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:4	ID[3:0]	R	xh	**Revision Identification** Read-only, factory-programmed bits used for revision identification. *Note: The revision ID may change without notification*
3	DRDY MODE	R/W	0h	**Data Ready Mode Setting** This bit sets the DOUT/$\overline{\text{DRDY}}$ pin functionality. In either setting of the DRDY MODE bit, the dedicated $\overline{\text{DRDY}}$ pin continues to indicate data ready, active low. 0: DOUT/$\overline{\text{DRDY}}$ pin functions only as Data Out (default) 1: DOUT/$\overline{\text{DRDY}}$ pin functions both as Data Out and Data Ready, active low(1)
2:0	RESERVED	R	0h	**RESERVED** These bits must always be set to 000

(1) Cannot be used in SDATAC mode

9.6.3 ADS1147 and ADS1148 Register Map

表 25. ADS1147 and ADS1148 Register Map

ADDRESS	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00h	MUX0	BCS[1:0]		MUX_SP[2:0]			MUX_SN[2:0]		
01h	VBIAS	VBIAS[7:0]							
02h	MUX1	CLKSTAT	VREFCON[1:0]		REFSELT[1:0]		MUXCAL[2:0]		
03h	SYS0	0	PGA[2:0]			DR[3:0]			
04h	OFC0	OFC[7:0]							
05h	OFC1	OFC[15:8]							
06h	OFC2	OFC[23:16]							
07h	FSC0	FSC[7:0]							
08h	FSC1	FSC[15:8]							
09h	FSC2	FSC[23:16]							
0Ah	IDAC0	ID[3:0]				DRDY MODE	IMAG[2:0]		
0Bh	IDAC1	I1DIR[3:0]				I2DIR[3:0]			
0Ch	GPIOCFG	IOCFG[7:0]							
0Dh	GPIODIR	IODIR[7:0]							
0Eh	GPIODAT	IODAT[7:0]							

9.6.4 ADS1147 and ADS1148 Detailed Register Definitions

9.6.4.1 MUX0—Multiplexer Control Register 0 (offset = 00h) [reset = 01h]

This register allows any combination of differential inputs to be selected on any of the input channels. Note that this setting can be superceded by the MUXCAL and VBIAS bits.

図 62. Multiplexer Control Register 0

7	6	5	4	3	2	1	0
BCS[1:0]		MUX_SP[2:0]			MUX_SN[2:0]		
R/W-0h		R/W-0h			R/W-1h		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 26. Multiplexer Control Register 0 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:6	BCS[1:0]	R/W	0h	**Burn-out Detect Current Source Register** These bits control the setting of the sensor burnout detect current source 00: Burn-out current source off (default) 01: Burn-out current source on, 0.5 µA 10: Burn-out current source on, 2 µA 11: Burn-out current source on, 10 µA
5:3	MUX_SP[2:0]	R/W	0h	**Multiplexer Selection - ADC Positive Input** Positive input channel selection bits 000: AIN0 (default) 001: AIN1 010: AIN2 011: AIN3 100: AIN4 (ADS1148 only) 101: AIN5 (ADS1148 only) 110: AIN6 (ADS1148 only) 111: AIN7 (ADS1148 only)
2:0	MUX_SN[2:0]	R/W	1h	**Multiplexer Selection - ADC Negative Input** Negative input channel selection bits 000: AIN0 001: AIN1 (default) 010: AIN2 011: AIN3 100: AIN4 (ADS1148 only) 101: AIN5 (ADS1148 only) 110: AIN6 (ADS1148 only) 111: AIN7 (ADS1148 only)

9.6.4.2 VBIAS—Bias Voltage Register (offset = 01h) [reset = 00h]

図 63. Bias Voltage Register (ADS1147)

7	6	5	4	3	2	1	0
0	0	0	0	VBIAS[3:0]			
R-0h	R-0h	R-0h	R-0h	R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 27. Bias Voltage Register Field Descriptions (ADS1147)

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:4	RESERVED	R	0h	**Reserved** Always write 0000
3	VBIAS[3]	R/W	0h	**VBIAS[3] Voltage Enable** A bias voltage of mid-supply (AVDD + AVSS) / 2 is applied to AIN3 0: Bias voltage is not enabled (default) 1: Bias voltage is applied to AIN3
2	VBIAS[2]	R/W	0h	**VBIAS[2] Voltage Enable** A bias voltage of mid-supply (AVDD + AVSS) / 2 is applied to AIN2 0: Bias voltage is not enabled (default) 1: Bias voltage is applied to AIN2
1	VBIAS[1]	R/W	0h	**VBIAS[1] Voltage Enable** A bias voltage of mid-supply (AVDD + AVSS) / 2 is applied to AIN1 0: Bias voltage is not enabled (default) 1: Bias voltage is applied to AIN1
0	VBIAS[0]	R/W	0h	**VBIAS[0] Voltage Enable** A bias voltage of mid-supply (AVDD + AVSS) / 2 is applied to AIN0 0: Bias voltage is not enabled (default) 1: Bias voltage is applied to AIN0

図 64. Bias Voltage Register (ADS1148)

7	6	5	4	3	2	1	0
VBIAS[7:0]							
R/W-00h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 28. Bias Voltage Register Field Descriptions (ADS1148)

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	VBIAS[7]	R/W	0h	**VBIAS[7] Voltage Enable** A bias voltage of mid-supply (AVDD + AVSS) / 2 is applied to AIN7 0: Bias voltage is not enabled (default) 1: Bias voltage is applied to AIN7
6	VBIAS[6]	R/W	0h	**VBIAS[6] Voltage Enable** A bias voltage of mid-supply (AVDD + AVSS) / 2 is applied to AIN6 0: Bias voltage is not enabled (default) 1: Bias voltage is applied to AIN6
5	VBIAS[5]	R/W	0h	**VBIAS[5] Voltage Enable** A bias voltage of mid-supply (AVDD + AVSS) / 2 is applied to AIN5 0: Bias voltage is not enabled (default) 1: Bias voltage is applied to AIN5
4	VBIAS[4]	R/W	0h	**VBIAS[4] Voltage Enable** A bias voltage of mid-supply (AVDD + AVSS) / 2 is applied to AIN4 0: Bias voltage is not enabled (default) 1: Bias voltage is applied to AIN4
3	VBIAS[3]	R/W	0h	**VBIAS[3] Voltage Enable** A bias voltage of mid-supply (AVDD + AVSS) / 2 is applied to AIN3 0: Bias voltage is not enabled (default) 1: Bias voltage is applied to AIN3
2	VBIAS[2]	R/W	0h	**VBIAS[2] Voltage Enable** A bias voltage of mid-supply (AVDD + AVSS) / 2 is applied to AIN2 0: Bias voltage is not enabled (default) 1: Bias voltage is applied to AIN2
1	VBIAS[1]	R/W	0h	**VBIAS[1] Voltage Enable** A bias voltage of mid-supply (AVDD + AVSS) / 2 is applied to AIN1 0: Bias voltage is not enabled (default) 1: Bias voltage is applied to AIN1
0	VBIAS[0]	R/W	0h	**VBIAS[0] Voltage Enable** A bias voltage of mid-supply (AVDD + AVSS) / 2 is applied to AIN0 0: Bias voltage is not enabled (default) 1: Bias voltage is applied to AIN0

9.6.4.3 MUX1—Multiplexer Control Register 1 (offset = 02h) [reset = x0h]

図 65. Multiplexer Control Register 1

7	6	5	4	3	2	1	0
CLKSTAT	VREFCON[1:0]		REFSELT[1:0]		MUXCAL[2:0]		
R-xh	R/W-0h		R/W-0h		R/W-0h		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 29. Multiplexer Control Register 0 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	CLKSTAT	R	xh	**Clock Status** This bit is read-only and indicates whether the internal oscillator or external clock is being used 0: Internal oscillator in use 1: External clock in use
6:5	VREFCON[1:0]	R/W	0h	**Internal Reference Control** These bits control the internal voltage reference. These bits allow the reference to be turned on or off completely, or allow the reference state to follow the state of the device. Note that the internal reference is required for operation of the IDAC functions. 00: Internal reference is always off (default) 01: Internal reference is always on 10 or 11: Internal reference is on when a conversion is in progress and powers down when the device receives a SLEEP command or the START pin is taken low
4:3	REFSELT[1:0]	R/W	0h	**Reference Select Control** These bits select the reference input for the ADC. 00: REFP0 and REFN0 reference inputs selected (default) 01: REFP1 and REFN1 reference inputs selected (ADS1148 only) 10: Internal reference selected 11: Internal reference selected and internally connected to REFP0 and REFN0 input pins
2:0	MUXCAL[2:0](1)	R/W	0h	**System Monitor Control** These bits are used to select a system monitor. The MUXCAL selection supercedes selections from the MUX0, MUX1, and VBIAS registers (includes MUX_SP, MUX_SN, VBIAS, and reference input selections). 000: Normal operation (default) 001: Offset calibration. The analog inputs are disconnected and AIN_P and AIN_N are internally connected to mid-supply (AVDD + AVSS) / 2. 010: Gain calibration. The analog inputs are connected to the voltage reference. 011: Temperature measurement. The inputs are connected to a diode circuit that produces a voltage proportional to the ambient temperature of the device. 100: REF1 monitor. The analog inputs are disconnected and AIN_P and AIN_N are internally connected to $(V_{(REFP1)} – V_{(REFN1)}) / 4$ (ADS1148 only) 101: REF0 monitor. The analog inputs are disconnected and AIN_P and AIN_N are internally connected to $(V_{(REFP0)} – V_{(REFN0)}) / 4$ 110: Analog supply monitor. The analog inputs are disconnected and AIN_P and AIN_N are internally connected to (AVDD – AVSS) / 4 111: Digital supply monitor. The analog inputs are disconnected and AIN_P and AIN_N are internally connected to (DVDD – DGND) / 4

(1) When using either reference monitor, the internal reference must be enabled.

表 30 provides the ADC input connection and PGA settings for each MUXCAL setting. The PGA setting reverts to the original SYS0 register setting when MUXCAL is taken back to normal operation or offset measurement.

表 30. MUXCAL Settings

MUXCAL[2:0]	PGA GAIN SETTING	ADC INPUT
000	Set by SYS0 register	Normal operation
001	Set by SYS0 register	Inputs shorted to mid-supply (AVDD + AVSS) / 2
010	Forced to 1	$V_{(REFP)} – V_{(REFN)}$ (full-scale)
011	Forced to 1	Temperature measurement diode
100	Forced to 1	$(V_{(REFP1)} – V_{(REFN1)}) / 4$
101	Forced to 1	$(V_{(REFP0)} – V_{(REFN0)}) / 4$
110	Forced to 1	(AVDD – AVSS) / 4
111	Forced to 1	(DVDD – DGND) / 4

9.6.4.4 SYS0—System Control Register 0 (offset = 03h) [reset = 00h]

図 66. System Control Register 0

7	6	5	4	3	2	1	0
0	PGA[2:0]			DR[3:0]			
R-0h	R/W-0h			R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 31. System Control Register 0 Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	RESERVED	R	0h	**Reserved** Always write 0
6:4	PGA[2:0]	R/W	0h	**Gain Setting for PGA** These bits determine the gain of the PGA 000: PGA = 1 (default) 001: PGA = 2 010: PGA = 4 011: PGA = 8 100: PGA = 16 101: PGA = 32 110: PGA = 64 111: PGA = 128
3:0	DR[3:0]	R/W	0h	**Data Output Rate Setting** These bits determine the data output rate of the ADC 0000: DR = 5 SPS (default) 0001: DR = 10 SPS 0010: DR = 20 SPS 0011: DR = 40 SPS 0100: DR = 80 SPS 0101: DR = 160 SPS 0110: DR = 320 SPS 0111: DR = 640 SPS 1000: DR = 1000 SPS 1001 to 1111: DR = 2000 SPS

9.6.4.5 OFC—Offset Calibration Coefficient Register (offset = 04h, 05h, 06h) [reset = 00h, 00h, 00h]

These bits make up the offset calibration coefficient register of the ADS1147 and ADS1148.

図 67. Offset Calibration Coefficient Register

7	6	5	4	3	2	1	0
OFC[7:0]							
R/W-00h							
15	14	13	12	11	10	9	8
OFC[15:8]							
R/W-00h							
23	22	21	20	19	18	17	16
OFC[23:16]							
R/W-00h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 32. Offset Calibration Coefficient Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
23:0	OFC[23:0]	R/W	000000h	**Offset Calibration Register** Three registers compose the ADC 24-bit offset calibration word and is in twos complement format. The upper 16 bits (OFC[23:8]) can correct offsets ranging from -FS to +FS, while the lower eight bits (OFC[7:0]) provide sub-LSB correction. The ADC subtracts the register value from the conversion result before full scale operation.

9.6.4.6 FSC—Full-Scale Calibration Coefficient Register (offset = 07h, 08h, 09h) [reset = 00h, 00h, 40h]

These bits make up the full-scale calibration coefficient register.

図 68. Full-Scale Calibration Coefficient Register

7	6	5	4	3	2	4	0
FSC[7:0]							
R/W-00h							
15	14	13	12	11	10	9	8
FSC[15:8]							
R/W-00h							
23	22	21	20	19	18	17	16
FSC[23:16]							
R/W-40h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 33. Full-Scale Calibration Coefficient Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
23:0	FSC[23:0]	R/W	400000h	**Full-Scale Calibration Register** Three registers compose the ADC 24-bit full-scale calibration word. The 24-bit word is straight binary. The ADC divides the register value of the FSC register by 400000h to derive the scale factor for calibration. After the offset calibration, the ADC multiplies the scale factor by the conversion result.

9.6.4.7 IDAC0—IDAC Control Register 0 (offset = 0Ah) [reset = x0h]

図 69. IDAC Control Register 0

7	6	5	4	3	2	1	0
ID[3:0]				DRDY MODE	IMAG[2:0]		
R-xh				R/W-0h	R/W-0h		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 34. IDAC Control Register 0 Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:4	ID[3:0]	R	xh	**Revision Identification** Read-only, factory-programmed bits used for revision identification. *Note: The revision ID may change without notification*
3	DRDY MODE	R/W	0h	**Data Ready Mode Setting** This bit sets the DOUT/$\overline{\text{DRDY}}$ pin functionality. In either setting of the DRDY MODE bit, the dedicated $\overline{\text{DRDY}}$ pin continues to indicate data ready, active low. 0: DOUT/$\overline{\text{DRDY}}$ pin functions only as Data Out (default) 1: DOUT/$\overline{\text{DRDY}}$ pin functions both as Data Out and Data Ready, active low(1)
2:0	IMAG[2:0]	R/W	0h	**IDAC Excitation Current Magnitude** The ADS1147 and ADS1148 have two excitation current sources (IDACs) that can be used for sensor excitation. The IMAG bits control the magnitude of the excitation current. The IDACs require the internal reference to be on. 000: off (default) 001: 50 µA 010: 100 µA 011: 250 µA 100: 500 µA 101: 750 µA 110: 1000 µA 111: 1500 µA

(1) Cannot be used in SDATAC mode

9.6.4.8 IDAC1—IDAC Control Register 1 (offset = 0Bh) [reset = FFh]

図 70. IDAC Control Register 1

7	6	5	4	3	2	1	0
I1DIR[3:0]				I2DIR[3:0]			
R/W-Fh				R/W-Fh			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

The two IDACs on the ADS1148 can be routed to either the IEXC1 and IEXC2 output pins or directly to the analog inputs.

表 35. IDAC Control Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:4	I1DIR[3:0]	R/W	Fh	**IDAC Excitation Current Output 1** These bits select the output pin for the first excitation current source 0000: AIN0 0001: AIN1 0010: AIN2 0011: AIN3 0100: AIN4 (ADS1148 only) 0101: AIN5 (ADS1148 only) 0110: AIN6 (ADS1148 only) 0111: AIN7 (ADS1148 only) 10x0: IEXC1 (ADS1148 only) 10x1: IEXC2 (ADS1148 only) 11xx: Disconnected (default)
3:0	I2DIR[3:0]	R/W	Fh	**IDAC Excitation Current Output 2** These bits select the output pin for the second excitation current source 0000: AIN0 0001: AIN1 0010: AIN2 0011: AIN3 0100: AIN4 (ADS1148 only) 0101: AIN5 (ADS1148 only) 0110: AIN6 (ADS1148 only) 0111: AIN7 (ADS1148 only) 10x0: IEXC1 (ADS1148 only) 10x1: IEXC2 (ADS1148 only) 11xx: Disconnected (default)

9.6.4.9 GPIOCFG—GPIO Configuration Register (offset = 0Ch) [reset = 00h]

図 71. GPIO Configuration Register (ADS1147)

7	6	5	4	3	2	1	0
0	0	0	0	IOCFG[3:0]			
R-0h	R-0h	R-0h	R-0h	R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 36. GPIO Configuration Register Field Descriptions (ADS1147)

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:4	RESERVED	R	0h	**Reserved** Always write 0000
3	IOCFG[3]	R/W	0h	**GPIO[3] (AIN3) Pin Configuration** 0: GPIO[3] is not enabled (default) 1: GPIO[3] is applied to AIN3
2	IOCFG[2]	R/W	0h	**GPIO[2] (AIN2) Pin Configuration** 0: GPIO[2] is not enabled (default) 1: GPIO[2] is applied to AIN2
1	IOCFG[1]	R/W	0h	**GPIO[1] (REFN0) Pin Configuration** 0: GPIO[1] is not enabled (default) 1: GPIO[1] is applied to REFN0
0	IOCFG[0]	R/W	0h	**GPIO[0] (REFP0) Pin Configuration** 0: GPIO[0] is not enabled (default) 1: GPIO[0] is applied to REFP0

図 72. GPIO Configuration Register (ADS1148)

7	6	5	4	3	2	1	0
IOCFG[7:0]							
R/W-00h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 37. GPIO Configuration Register Field Descriptions (ADS1148)

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	IOCFG[7]	R/W	0h	**GPIO[7] (AIN7) Pin Configuration** 0: GPIO[7] is not enabled (default) 1: GPIO[7] is applied to AIN7
6	IOCFG[6]	R/W	0h	**GPIO[6] (AIN6) Pin Configuration** 0: GPIO[6] is not enabled (default) 1: GPIO[6] is applied to AIN6
5	IOCFG[5]	R/W	0h	**GPIO[5] (AIN5) Pin Configuration** 0: GPIO[5] is not enabled (default) 1: GPIO[5] is applied to AIN5
4	IOCFG[4]	R/W	0h	**GPIO[4] (AIN4) Pin Configuration** 0: GPIO[4] is not enabled (default) 1: GPIO[4] is applied to AIN4
3	IOCFG[3]	R/W	0h	**GPIO[3] (AIN3) Pin Configuration** 0: GPIO[3] is not enabled (default) 1: GPIO[3] is applied to AIN3
2	IOCFG[2]	R/W	0h	**GPIO[2] (AIN2) Pin Configuration** 0: GPIO[2] is not enabled (default) 1: GPIO[2] is applied to AIN2
1	IOCFG[1]	R/W	0h	**GPIO[1] (REFN0) Pin Configuration** 0: GPIO[1] is not enabled (default) 1: GPIO[1] is applied to REFN0
0	IOCFG[0]	R/W	0h	**GPIO[0] (REFP0) Pin Configuration** 0: GPIO[0] is not enabled (default) 1: GPIO[0] is applied to REFP0

9.6.4.10 GPIODIR—GPIO Direction Register (offset = 0Dh) [reset = 00h]

図 73. GPIO Direction Register (ADS1147)

7	6	5	4	3	2	1	0
0	0	0	0	IODIR[3:0]			
R-0h	R-0h	R-0h	R-0h	R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 38. GPIO Direction Register Field Descriptions (ADS1147)

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:4	RESERVED	R	0h	**Reserved** Always write 0000
3	IODIR[3]	R/W	0h	**GPIO[3] (AIN3) Pin Direction** Configures GPIO[3] as a GPIO input or GPIO output 0: GPIO[3] is an output (default) 1: GPIO[3] is an input
2	IODIR[2]	R/W	0h	**GPIO[2] (AIN2) Pin Direction** Configures GPIO[2] as a GPIO input or GPIO output 0: GPIO[2] is an output (default) 1: GPIO[2] is an input
1	IODIR[1]	R/W	0h	**GPIO[1] (REFN0) Pin Direction** Configures GPIO[1] as a GPIO input or GPIO output 0: GPIO[1] is an output (default) 1: GPIO[1] is an input
0	IODIR[0]	R/W	0h	**GPIO[0] (REFP0) Pin Direction** Configures GPIO[0] as a GPIO input or GPIO output 0: GPIO[0] is an output (default) 1: GPIO[0] is an input

図 74. GPIO Direction Register (ADS1148)

7	6	5	4	3	2	1	0
IODIR[7:0]							
R/W-00h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 39. GPIO Direction Register Field Descriptions (ADS1148)

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	IODIR[7]	R/W	0h	**GPIO[7] (AIN7) Pin Direction** Configures GPIO[7] as a GPIO input or GPIO output 0: GPIO[7] is an output (default) 1: GPIO[7] is an input
6	IODIR[6]	R/W	0h	**GPIO[6] (AIN6) Pin Direction** Configures GPIO[6] as a GPIO input or GPIO output 0: GPIO[6] is an output (default) 1: GPIO[6] is an input
5	IODIR[5]	R/W	0h	**GPIO[5] (AIN5) Pin Direction** Configures GPIO[5] as a GPIO input or GPIO output 0: GPIO[5] is an output (default) 1: GPIO[5] is an input
4	IODIR[4]	R/W	0h	**GPIO[4] (AIN4) Pin Direction** Configures GPIO[4] as a GPIO input or GPIO output 0: GPIO[4] is an output (default) 1: GPIO[4] is an input
3	IODIR[3]	R/W	0h	**GPIO[3] (AIN3) Pin Direction** Configures GPIO[3] as a GPIO input or GPIO output 0: GPIO[3] is an output (default) 1: GPIO[3] is an input
2	IODIR[2]	R/W	0h	**GPIO[2] (AIN2) Pin Direction** Configures GPIO[2] as a GPIO input or GPIO output 0: GPIO[2] is an output (default) 1: GPIO[2] is an input
1	IODIR[1]	R/W	0h	**GPIO[1] (REFN0) Pin Direction** Configures GPIO[1] as a GPIO input or GPIO output 0: GPIO[1] is an output (default) 1: GPIO[1] is an input
0	IODIR[0]	R/W	0h	**GPIO[0] (REFP0) Pin Direction** Configures GPIO[0] as a GPIO input or GPIO output 0: GPIO[0] is an output (default) 1: GPIO[0] is an input

9.6.4.11 GPIODAT—GPIO Data Register (offset = 0Eh) [reset = 00h]

図 75. GPIO Data Register (ADS1147)

7	6	5	4	3	2	1	0
0	0	0	0	IODAT[3:0]			
R-0h	R-0h	R-0h	R-0h	R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 40. GPIO Data Register Field Descriptions (ADS1147)

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:4	RESERVED	R	0h	**Reserved** Always write 0000
3	IODAT[3]	R/W	0h	**GPIO[3] (AIN3) Pin Data** Configured as an output, read returns the register value Configured as an input, write sets the register value only 0: GPIO[3] is low (default) 1: GPIO[3] is high
2	IODAT[2]	R/W	0h	**GPIO[2] (AIN2) Pin Data** Configured as an output, read returns the register value Configured as an input, write sets the register value only 0: GPIO[2] is low (default) 1: GPIO[2] is high
1	IODAT[1]	R/W	0h	**GPIO[1] (REFN0) Pin Data** Configured as an output, read returns the register value Configured as an input, write sets the register value only 0: GPIO[1] is low (default) 1: GPIO[1] is high
0	IODAT[0]	R/W	0h	**GPIO[0] (REFP0) Pin Data** Configured as an output, read returns the register value Configured as an input, write sets the register value only 0: GPIO[0] is low (default) 1: GPIO[0] is high

図 76. GPIO Data Register (ADS1148)

7	6	5	4	3	2	1	0
IODAT[7:0]							
R/W-00h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 41. GPIO Data Register Field Descriptions (ADS1148)

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	IODAT[7]	R/W	0h	**GPIO[7] (AIN7) Pin Data** Configured as an output, read returns the register value Configured as an input, write sets the register value only 0: GPIO[7] is low (default) 1: GPIO[7] is high
6	IODAT[6]	R/W	0h	**GPIO[6] (AIN6) Pin Data** Configured as an output, read returns the register value Configured as an input, write sets the register value only 0: GPIO[6] is low (default) 1: GPIO[6] is high
5	IODAT[5]	R/W	0h	**GPIO[5] (AIN5) Pin Data** Configured as an output, read returns the register value Configured as an input, write sets the register value only 0: GPIO[5] is low (default) 1: GPIO[5] is high
4	IODAT[4]	R/W	0h	**GPIO[4] (AIN4) Pin Data** Configured as an output, read returns the register value Configured as an input, write sets the register value only 0: GPIO[4] is low (default) 1: GPIO[4] is high
3	IODAT[3]	R/W	0h	**GPIO[3] (AIN3) Pin Data** Configured as an output, read returns the register value Configured as an input, write sets the register value only 0: GPIO[3] is low (default) 1: GPIO[3] is high
2	IODAT[2]	R/W	0h	**GPIO[2] (AIN2) Pin Data** Configured as an output, read returns the register value Configured as an input, write sets the register value only 0: GPIO[2] is low (default) 1: GPIO[2] is high
1	IODAT[1]	R/W	0h	**GPIO[1] (REFN0) Pin Data** Configured as an output, read returns the register value Configured as an input, write sets the register value only 0: GPIO[1] is low (default) 1: GPIO[1] is high
0	IODAT[0]	R/W	0h	**GPIO[0] (REFP0) Pin Data** Configured as an output, read returns the register value Configured as an input, write sets the register value only 0: GPIO[0] is low (default) 1: GPIO[0] is high

10 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The ADS1146, ADS1147, and ADS1148 make up a family of precision, 16-bit, ΔΣ ADCs that offers many integrated features to ease the measurement of the most common sensor types including various types of temperature and bridge sensors. Primary considerations when designing an application with these devices include connecting and configuring the serial interface, designing the analog input filtering, establishing an appropriate external reference for ratiometric measurements, and setting the common-mode input voltage for the internal PGA. These considerations are discussed in the following sections.

10.1.1 Serial Interface Connections

図 77 shows the principle serial interface connections for the ADS1148.

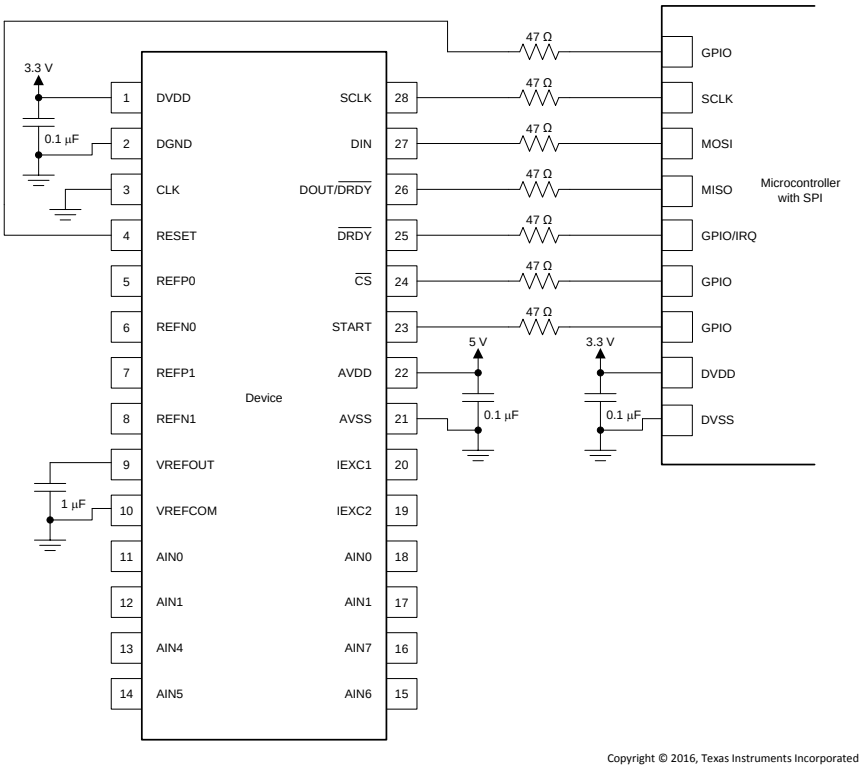


図 77. Serial Interface Connections

Most microcontroller SPI peripherals can operate with the ADS1148. The interface operates in SPI mode 1 where CPOL = 0 and CPHA = 1. In SPI mode 1, SCLK idles low and data are launched or changed only on SCLK rising edges; data are latched or read by the master and slave on SCLK falling edges. Details of the SPI communication protocol employed by the device can be found in the *Serial Interface Timing Requirements* section.

TI recommends placing 47-Ω resistors in series with all digital input and output pins ($\overline{CS}$, SCLK, DIN, DOUT/$\overline{DRDY}$, $\overline{DRDY}$, $\overline{RESET}$ and START). This resistance smooths sharp transitions, suppresses overshoot, and offers some overvoltage protection. Care must be taken to meet all SPI timing requirements because the additional resistors interact with the bus capacitances present on the digital signal lines.

Application Information (continued)

10.1.2 Analog Input Filtering

Analog input filtering serves two purposes: first, to limit the effect of aliasing during the sampling process and second, to reduce external noise from being a part of the measurement.

As with any sampled system, aliasing can occur if proper anti-alias filtering is not in place. Aliasing occurs when frequency components are present in the input signal that are higher than half the sampling frequency of the ADC (also known as the Nyquist frequency). These frequency components are folded back and show up in the actual frequency band of interest below half the sampling frequency. Note that inside a ΔΣ ADC, the input signal is sampled at the modulator frequency, f_{MOD} and not at the output data rate. The filter response of the digital filter repeats at multiples of the f_{MOD}, as shown in 図 78. Signals or noise up to a frequency where the filter response repeats are attenuated to a certain amount by the digital filter depending on the filter architecture. Any frequency components present in the input signal around the modulator frequency or multiples thereof are not attenuated and alias back into the band of interest, unless attenuated by an external analog filter.

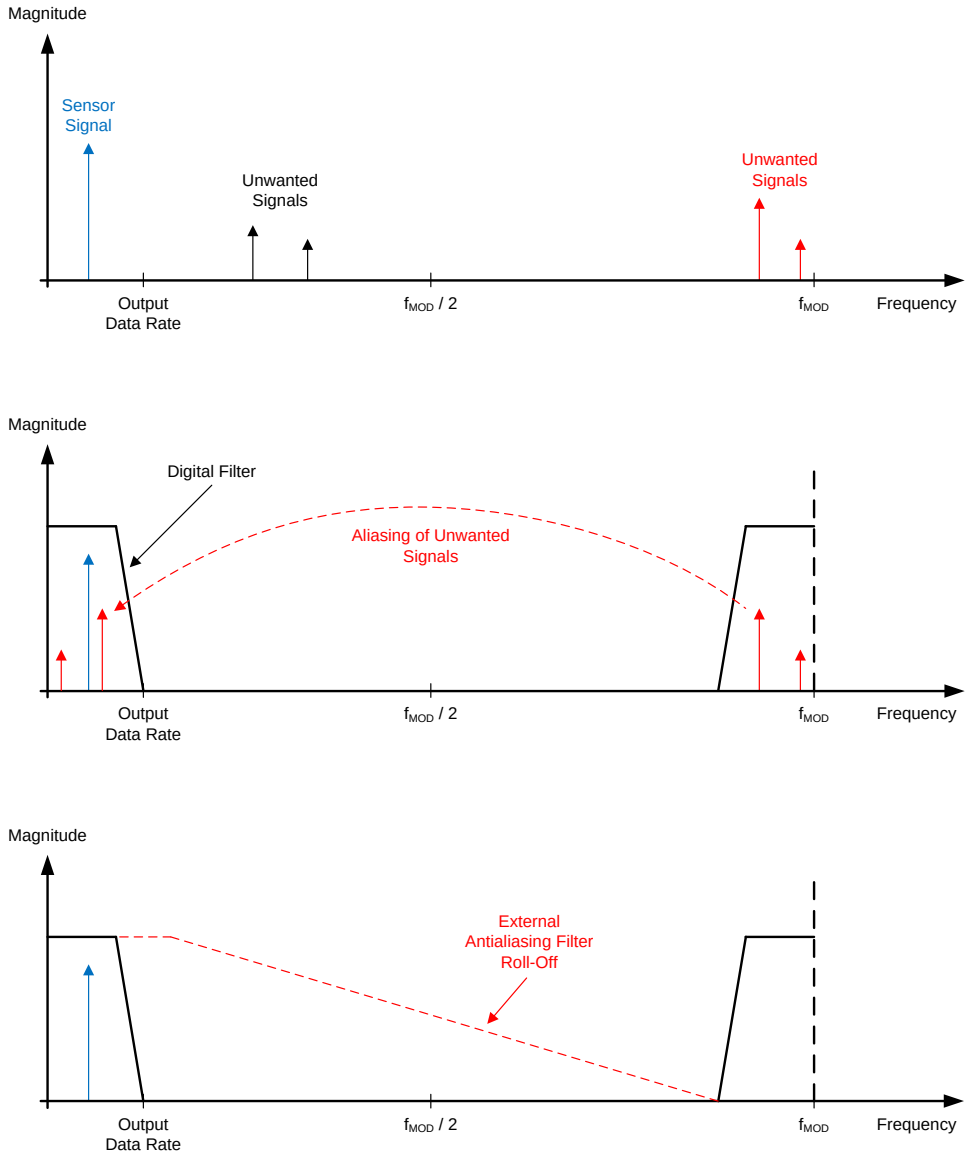


図 78. Effect of Aliasing

Application Information (continued)

Many sensor signals are inherently bandlimited; for example, the output of a thermocouple has a limited rate of change. In this case, the sensor signal does not alias back into the pass-band when using a ΔΣ ADC. However, any noise pickup along the sensor wiring or the application circuitry can potentially alias into the pass-band. Power line-cycle frequency and harmonics are one common noise source. External noise can also be generated from electromagnetic interference (EMI) or radio frequency interference (RFI) sources, such as nearby motors and cellular phones. Another noise source typically exists on the printed-circuit board (PCB) itself in the form of clocks and other digital signals. Analog input filtering helps remove unwanted signals from affecting the measurement result.

A first-order resistor-capacitor (RC) filter is (in most cases) sufficient to either totally eliminate aliasing, or to reduce the effect of aliasing to a level within the noise floor of the sensor. Ideally, any signal beyond $f_{MOD}/2$ is attenuated to a level below the noise floor of the ADC. The digital filter of the ADS1148 attenuates signals to a certain degree, as illustrated in the filter response plots in the *Digital Filter* section. In addition, noise components are usually smaller in magnitude than the actual sensor signal. Therefore, using a first-order RC filter with a cutoff frequency set at the output data rate or 10× higher is generally a good starting point for a system design.

Internal to the device, prior to the PGA inputs, is an EMI filter; see 図 20. The cutoff frequency of this filter is approximately 47 MHz, which helps reject high-frequency interferences.

10.1.3 External Reference and Ratiometric Measurements

The full-scale range of the ADS1148 is defined by the reference voltage and the PGA gain (FSR = $\pm V_{REF}$ / Gain). An external reference can be used instead of the integrated 2.048-V reference to adapt the FSR to the specific system requirements. An external reference must be used if V_{IN} > 2.048 V. For example, an external 2.5-V reference is required to measure signals as large as 2.5 V. Note that the input signal must be within the common-mode input range to be valid, and that the reference input voltage must be between 0.5 V and (AVDD – AVSS – 1 V).

The buffered reference inputs of the device also allow the implementation of ratiometric measurements. In a ratiometric measurement, the same excitation source that is used to excite the sensor is also used to establish the reference for the ADC. As an example, a simple form of a ratiometric measurement uses the same current source to excite both the resistive sensor element (such as an RTD) and another resistive reference element that is in series with the element being measured. The voltage that develops across the reference element is used as the reference source for the ADC. In this configuration, current noise and drift are common to both the sensor measurement and the reference; therefore, these components cancel out in the ADC transfer function. The output code is only a ratio of the sensor element value and the reference resistor value, and is not affected by the absolute value of the excitation current.

10.1.4 Establishing a Proper Common-Mode Input Voltage

The ADS1148 is used to measure various types of signal configurations. However, configuring the input of the device properly for the respective signal type is important.

The ADS1148 features an 8-input multiplexer (while the ADS1147 has a 4-input multiplexer). Each input can be independently selected as the positive input or the negative input to be measured by the ADC. With an 8-input multiplexer, the user can measure four independent differential-input channels. The user can also choose to measure 7 channels, using one input as a fixed common input. Regardless of the analog input configuration, make sure that all inputs, including the common input are within the common-mode input voltage range.

If the supply is unipolar (for example, AVSS = 0 V and AVDD = 5 V), then $V_{(AINN)}$ = 0 V is not within the common-mode input range as shown by 式 3. Therefore, a single-ended measurement with the common input connected to ground is not possible. TI recommends connecting the common-input to mid-supply or alternatively to VREFOUT. Note that the common-mode range becomes further restricted with increasing PGA gain.

If the supply is bipolar (AVSS = –2.5 V and AVDD = 2.5 V), then ground is within the common-mode input range. Single-ended measurements with the common input connected to 0 V are possible in this case.

For a detailed explanation of the common-mode input range as it relates to the PGA see the *PGA Common-Mode Voltage Requirements* section.

Application Information (continued)

10.1.5 Isolated (or Floating) Sensor Inputs

Isolated sensors (sensors that are not referenced to the ADC ground) must have a common-mode voltage established within the specified ADC input range. Level shift the common-mode voltage by external resistor biasing, by connecting the negative lead to ground (bipolar analog supply), or by connecting to a DC voltage (unipolar analog supply). The 2.048-V reference output voltage may also be used to provide level shifting to floating sensor inputs.

10.1.6 Unused Inputs and Outputs

To minimize leakage currents on the analog inputs, leave unused analog inputs floating, connect them to mid-supply, or connect them to AVDD. Connecting unused analog inputs to AVSS is possible as well, but can yield higher leakage currents than the options mentioned before.

Do not float unused digital inputs or excessive power-supply leakage current may result. Tie all unused digital inputs to the appropriate levels, DVDD or DGND, including when in power-down mode. If the $\overline{\text{DRDY}}$ output is not used, leave the pin unconnected or tie it to DVDD using a weak pullup resistor.

10.1.7 Pseudo Code Example

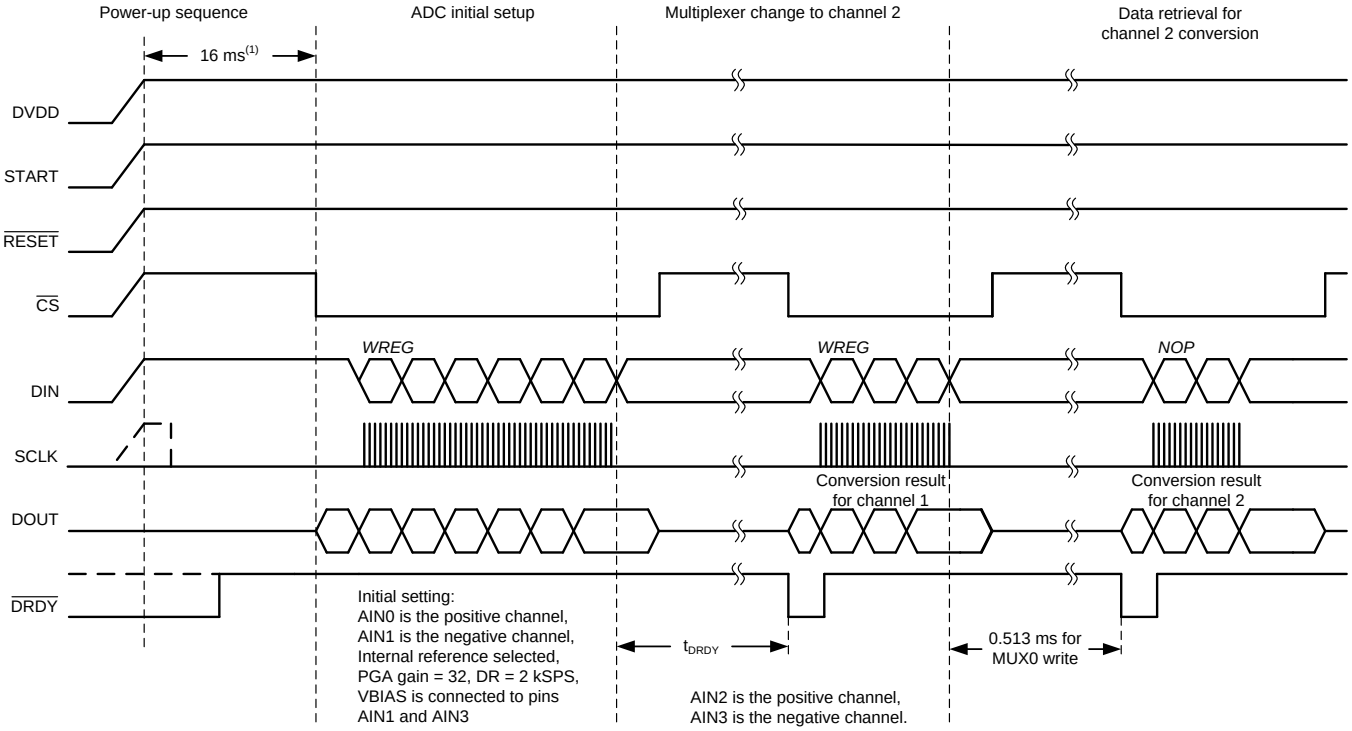
The following list shows a pseudo code sequence with the required steps to set up the device and the microcontroller that interfaces to the ADC to take subsequent readings from the ADS1148 in stop read data continuous (SDATAC) mode. In SDATAC mode, it is sufficient to wait for a time period longer than the data rate to retrieve the conversion result. New conversion data does not interrupt the reading of registers or data on DOUT. However in this example, the dedicated $\overline{\text{DRDY}}$ pin is used to indicate availability of new conversion data instead of waiting a set time period for a readout. The default configuration register settings are changed to PGA gain = 16, using the internal reference, and a data rate of 20 SPS.

```
Power up;
Delay for a minimum of 16 ms to allow power supplies to settle and power-on reset to complete;
Enable the device by setting the START pin high;
Configure the serial interface of the microcontroller to SPI mode 1 (CPOL = 0, CPHA =1);
If the CS pin is not tied low permanently, configure the microcontroller GPIO connected to CS as an
output;
Configure the microcontroller GPIO connected to the DRDY pin as a falling edge triggered interrupt
input;
Set CS to the device low;
Delay for a minimum of tCSSC;
Send the RESET command (06h) to make sure the device is properly reset after power up;
Delay for a minimum of 0.6 ms;
Send SDATAC command (16h) to prevent the new data from interrupting data or register transactions;
Write the respective register configuration with the WREG command (40h, 03h, 01h, 00h, 03h and 42h);
As an optional sanity check, read back all configuration registers with the RREG command (four bytes
from 20h, 03h);
Send the SYNC command (04h) to start the ADC conversion;
Delay for a minimum of tSCCS;
Clear CS to high (resets the serial interface);
Loop
{
    Wait for DRDY to transition low;
    Take CS low;
    Delay for a minimum of tCSSC;
    Send the RDATA command (12h);
    Send 16 SCLKs to read out conversion data on DOUT/DRDY;
    Delay for a minimum of tSCCS;
    Clear CS to high;
}
Take CS low;
Delay for a minimum of tCSSC;
Send the SLEEP command (02h) to stop conversions and put the device in power-down mode;
```

Application Information (continued)

10.1.8 Channel Multiplexing Example

This example applies only to the ADS1147 and ADS1148. It explains a method to use the device with two sensors connected to two different analog channels. 図 79 shows the sequence of SPI operations performed on the device. After power up, 2^{16} t_{CLK} cycles are required before communication can be started. During the first 2^{16} t_{CLK} cycles, the device is internally held in a reset state. In this example, one of the sensors is connected to channels AIN0 and AIN1 and the other sensor is connected to channels AIN2 and AIN3. The ADC is operated at a data rate of 2 kSPS. The PGA gain is set to 32 for both sensors. VBIAS is connected to the negative terminal of both sensors (that is, channels AIN1 and AIN3). All these settings can be changed by performing a block write operation on the first four registers of the device. After the DRDY pin goes low, the conversion result can be immediately retrieved by sending in 16 SCLK pulses because the device defaults to RDATAC mode. As the conversion result is being retrieved, the active input channels can be switched to AIN2 and AIN3 by writing into the MUX0 register in a full-duplex manner, as shown in 図 79. The write operation is completed with an additional eight SCLK pulses. The time from the write operation into the MUX0 register to the next DRDY low transition is shown in 図 79 and is 0.513 ms in this case. After DRDY goes low, the conversion result can be retrieved and the active channel can be switched as before.



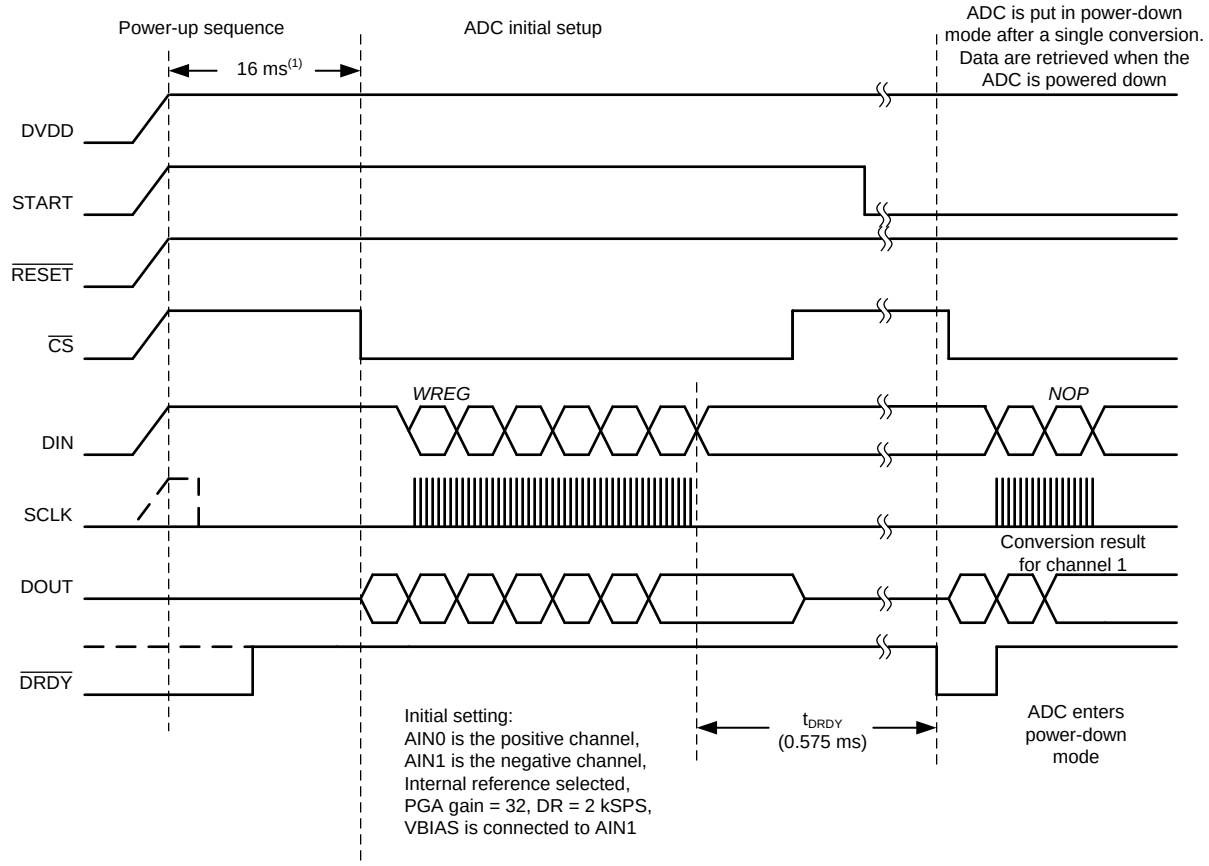
(1) For f_{CLK} = 4.096 MHz.

図 79. SPI Communication Sequence for Channel Multiplexing

Application Information (continued)

10.1.9 Power-Down Mode Example

This second example deals with performing one conversion after power up and then entering power-down mode. In this example, a sensor is connected to input channels AIN0 and AIN1. Commands to set up the device must occur at least 2^{16} system clock cycles after powering up the device. The ADC operates at a data rate of 2 kSPS. The PGA gain is set to 32. VBIAS is connected to the negative terminal of the sensor (that is, channel AIN1). All these settings can be changed by performing a block write operation on the first four registers of the device. After performing the block write operation, the START pin can be taken low. The device enters the power-down mode as soon as $\overline{\text{DRDY}}$ goes low 0.575 ms after writing into the SYS0 register. The conversion result can be retrieved even after the device enters power-down mode by sending 16 SCLK pulses.



(1) For f_{CLK} = 4.096 MHz.

図 80. SPI Communication Sequence for Entering Power-Down Mode After a Conversion

10.2 Typical Applications

10.2.1 Ratiometric 3-Wire RTD Measurement System

図 81 shows a 3-wire RTD application circuit with lead-wire compensation using the ADS1147. The two IDAC current sources integrated in the ADS1147 are used to implement the lead-wire compensation. One IDAC current source (IDAC1) provides excitation to the RTD element. The other current source (IDAC2) has the same current setting, providing cancellation of lead-wire resistance by generating a voltage drop across lead-wire resistance R_{LEAD2} equal to the voltage drop across R_{LEAD1}. Because the voltage across the RTD is measured differentially at ADC pins AIN1 and AIN2, the voltages across the lead-wire resistances cancel. The ADC reference voltage (pins REFP0 and REFN0) is derived from the voltage across R_{REF} with the currents from IDAC1 and IDAC2, providing ratiometric cancellation of current-source drift. R_{REF} also level shifts the RTD signal to within the ADC specified common-mode input range.

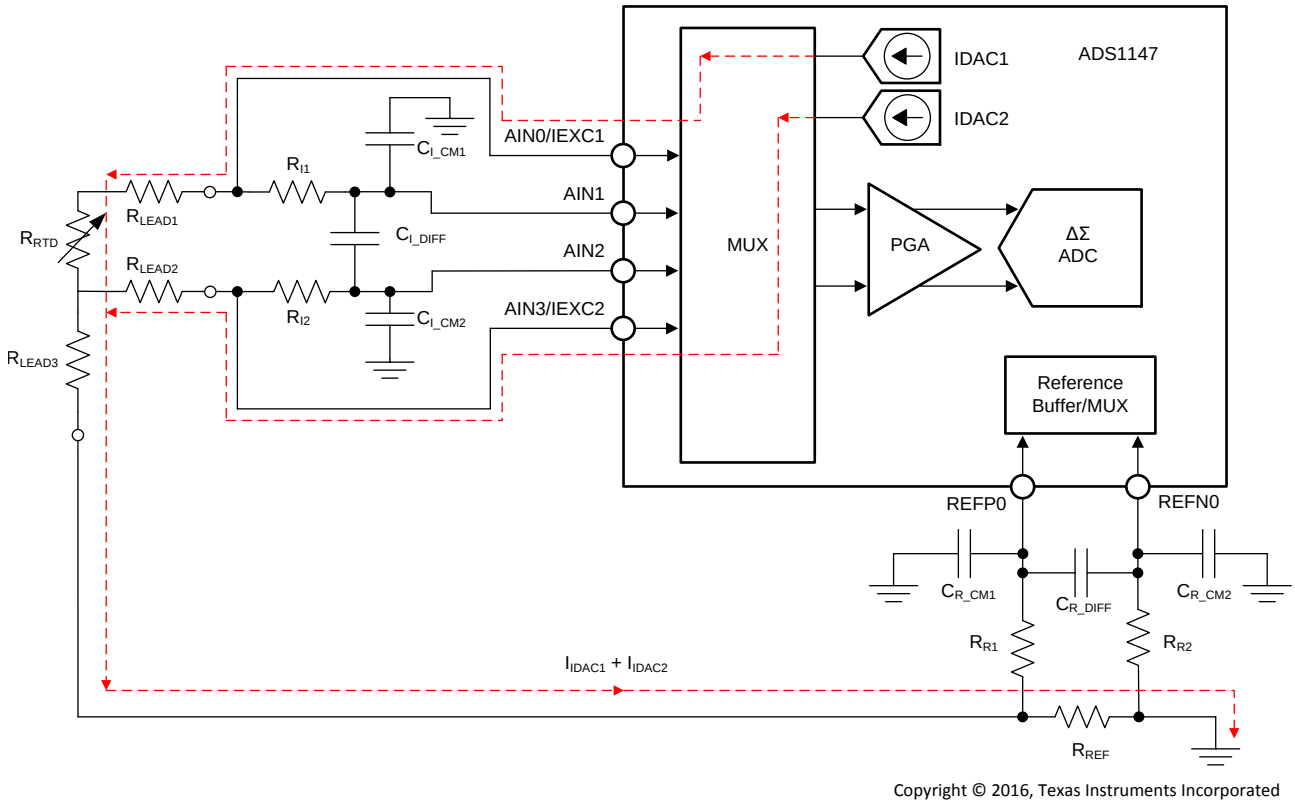


図 81. Ratiometric 3-Wire RTD Measurement System Featuring the ADS1147

10.2.1.1 Design Requirements

表 42 shows the design requirements of the 3-wire RTD application.

表 42. 3-Wire RTD Application Requirements

PARAMETER	VALUE
Supply voltage	3.3 V
Data rate	20 SPS
RTD type	3-wire PT100
RTD excitation current	1 mA
Temperature	–200°C to 850°C
Calibrated temperature measurement accuracy at T_A = 25ºC (1)	±0.2°C

(1) Not accounting for error of RTD; a two-point gain and offset calibration are performed, as well as chopping of the excitation currents to remove IDAC mismatch errors.

10.2.1.2 Detailed Design Procedure

10.2.1.2.1 Topology

図 82 shows the basic topology of a ratiometric measurement using an RTD. Shown are the ADC with the RTD and a reference resistor R_{REF}. There is a single current source, labeled IDAC1 which is used to excite the RTD as well as to establish a reference voltage for the ADC across R_{REF}.

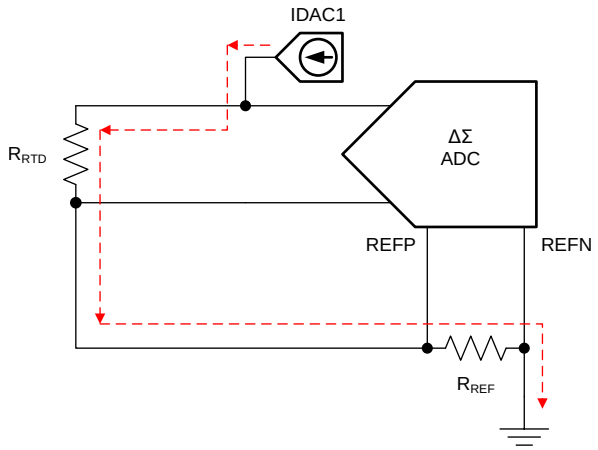


図 82. Example of a Ratiometric RTD Measurement

With IDAC1, the ADC measures the RTD voltage using the voltage across R_{REF} as the reference. This gives a measurement such that the output code is proportional to the ratio of the RTD voltage and the reference voltage as shown in 式 21 and 式 22.

$$\text{Code} \propto V_{RTD} / V_{REF} \quad (21)$$

$$\text{Code} \propto (R_{RTD} \times I_{IDAC1}) / (R_{REF} \times I_{IDAC1}) \quad (22)$$

The currents cancel so that the equation reduces to 式 23:

$$\text{Code} \propto R_{RTD} / R_{REF} \quad (23)$$

As shown in 式 23, the measurement depends on the resistive value of the RTD and the reference resistor R_{REF}, but not on the IDAC1 current value. Therefore, the absolute accuracy and temperature drift of the excitation current does not matter. This is a ratiometric measurement. As long as there is no current leakage from IDAC1 outside of this circuit, the measurement depends only on R_{RTD} and R_{REF}.

In 図 83, the lead resistances of a 3-wire RTD are shown and another excitation current source is added, labeled IDAC2.

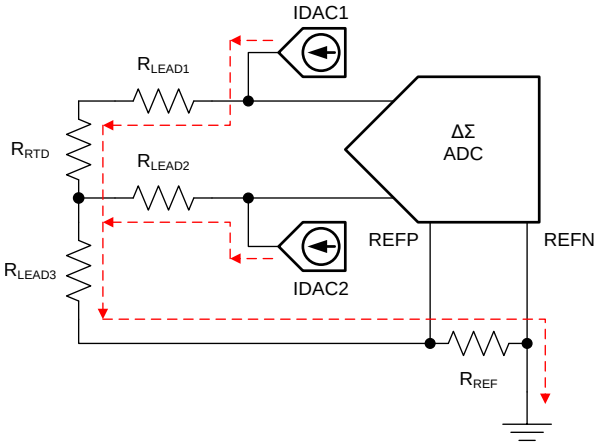


図 83. Example of Lead Wire Compensation

With a single excitation current source, R_{LEAD1} adds an error to the measurement. By adding IDAC2, the second excitation current source is used to cancel out the error in the lead wire resistance. When adding the lead resistances and the second current source, the equation becomes:

$$\text{Code} \propto (V_{RTD} + (R_{LEAD1} \times I_{IDAC1}) - (R_{LEAD2} \times I_{IDAC2})) / (V_{REF} \times (I_{IDAC1} + I_{IDAC2})) \quad (24)$$

If the lead resistances match and the excitation currents match, then $R_{LEAD1} = R_{LEAD2}$ and $I_{IDAC1} = I_{IDAC2}$. The lead wire resistances cancel out so that 式 24 reduces to the result in 式 25 maintaining a ratiometric measurement.

$$\text{Code} \propto R_{RTD} / (2 \times R_{REF}) \quad (25)$$

R_{LEAD3} is not part of the measurement, because it is not in the input measurement path or in the reference input path.

As 式 24 shows, the two current sources must be matched to cancel the lead resistances of the RTD wires. Any mismatch in the two current sources is minimized by using the multiplexer to swap or *chop* the two current sources between the two inputs. Taking measurements in both configurations and averaging the readings reduces the effects of mismatched current sources. The design uses the multiplexer in the ADS1147 to implement this chopping technique to remove the mismatch error between IDAC1 and IDAC2.

10.2.1.2.2 RTD Selection

The RTD is first chosen to be a PT100 element. The RTD resistance is defined by the Callendar-Van Dusen (CVD) equations and the resistance of the RTD is known depending on the temperature. The PT100 RTD has an impedance of 100 Ω at 0˚C and roughly 0.385 Ω of resistance change per 1˚C in temperature change. With a desired temperature measurement accuracy of 0.2˚C, this translates to a resistive measurement accuracy of approximately 0.077 Ω. The RTD resistance at the low end of the temperature range of –200˚C is 18.59 Ω and the resistance at the high end of the temperature range of 850˚C is 390.48 Ω.

10.2.1.2.3 Excitation Current

For the best possible resolution, the voltage across the RTD must be made as large as possible compared to the noise floor in the measurement. In general, measurement resolution improves with increasing excitation current. However, a larger excitation current creates self-heating in the RTD, which causes drift and error in the measurement. The selection of excitation currents trades off resolution against sensor self-heating.

The excitation current sources in this design are selected to be 1 mA. This maximizes the value of the RTD voltage while keeping the self-heating low. The typical range of RTD self-heating coefficients is 2.5 mW/°C for small, thin-film elements and 65 mW/°C for larger, wire-wound elements. With 1-mA excitation at the maximum RTD resistance value, the power dissipation in the RTD is less than 0.4 mW and keeps the measurement errors due to self-heating to less than 0.01˚C.

As mentioned in the *Topology* section, chopping of the excitation current sources cancels mismatches between the IDACs. This technique is necessary for getting the best possible accuracy from the system. Mismatch between the excitation current sources is a large source of error if chopping is not implemented.

The internal reference voltage must be enabled while using the IDACs, even if an external ratiometric measurement is used for ADC conversions.

表 43 shows the ADS1147 register settings for setting up the internal reference and the excitation current sources.

表 43. Register Bit Settings for Excitation Current Sources

REGISTER (ADDRESS)	BIT NAME	BIT VALUES	COMMENT
MUX1 (02h)(1)	VREFCON[1:0]	01	Internal reference enabled
MUX1 (02h)	REFSELT[1:0]	00	REFP0 and REFN0 reference inputs selected
IDAC0 (0Ah)	IMAG[2:0]	110	IDAC magnitude = 1 mA
IDAC1 (0Bh)	I1DIR[3:0](2)	0000	IDAC1 = AIN0
IDAC1 (0Bh)	I2DIR[3:0](2)	0011	IDAC2 = AIN3

(1) The internal reference is required to be enabled to use the IDAC current sources.
(2) To implement chopping, swap IDAC1 direction for IDAC2 direction. Set I1DIR[3:0] = 0011 and I2DIR[3:0] = 0000

10.2.1.2.4 Reference Resistor, R_{REF}

TI recommends setting the common-mode voltage of the measurement near mid-supply, this helps keep the input within the common-mode input range of the PGA.

The reference resistor is selected to be 820 Ω. The voltage across R_{REF} is calculated from 式 26.

$$V_{REF} = R_{REF} \times (I_{IDAC1} + I_{IDAC2}) = 820\ \Omega \times 2\ mA = 1.64\ V \quad (26)$$

With AVDD = 3.3 V, 式 26 shows that the input voltage is just below mid-supply.

The excitation current sources operate properly to a maximum IDAC compliance voltage. Above this compliance voltage, the current sources lose current regulation. In this example, the output voltage of the excitation current source is calculated from the sum of the voltages across the RTD and R_{REF} as shown in 式 27.

$$V_{IDAC1\ MAX} = R_{RTD\ MAX} \times I_{IDAC1} + (R_{REF} \times (I_{IDAC1} + I_{IDAC2})) = 0.4\ V + 1.64\ V = 2.04\ V \quad (27)$$

A compliance voltage of 3.3 V – 2.04 V = 1.26 V is sufficient for proper IDAC operation. See 図 9 and 図 10 in the *Typical Characteristics* section for details.

Because the voltage across R_{REF} sets the reference voltage for the ADC, the tolerance and temperature drift of R_{REF} directly affect the measurement gain. A resistor with 0.01% maximum tolerance is selected for this measurement.

10.2.1.2.5 PGA Setting

Because the excitation current is small to reduce self-heating, the PGA in the ADS1147 is used to amplify the signal across the RTD to use the full-scale range of the ADC. Starting with the reference voltage, the ADC is able to measure a differential input signal range of ±1.64 V. The maximum allowable PGA gain setting is based on the reference voltage, the maximum RTD resistance, and the excitation current.

As mentioned previously, the maximum resistance of the RTD is seen at the top range of the temperature measurement at 850°C. This gives the largest voltage measurement of the ADC. $R_{RTD@850°C}$ is 390.48 Ω.

$$V_{RTD\ MAX} = R_{RTD@850°C} \times I_{IDAC1} = 390.48\ \Omega \times 1\ mA = 390.48\ mV \quad (28)$$

With a reference voltage of 1.64 V, the maximum gain for the PGA, without over-ranging the ADC, is shown in 式 29.

$$Gain_{MAX} = V_{REF} / V_{RTD\ MAX} = 1.64\ V / 390.48\ mV = 4.2\ V/V \quad (29)$$

Selecting a PGA gain of 4 gives a maximum measurement of 95% of the positive full-scale range. 表 44 shows the register settings to set the PGA gain as well as the inputs for the ADC.

表 44. Register Bit Settings for the Input Multiplexer and PGA

REGISTER (ADDRESS)	BIT NAME	BIT VALUES	COMMENT
MUX0 (01h)	MUX_SP[2:0]	001	AIN_P = AIN1
MUX0 (01h)	MUX_SN[2:0]	010	AIN_N = AIN2
SYS0 (03h)	PGA[2:0]	010	PGA Gain = 4

10.2.1.2.6 Common-Mode Input Range

Now that the component values are selected, the common-mode input range must be verified to ensure that the ADC and PGA are not limited in operation. Start with the maximum input voltage, which gives the most restriction in the common-mode input range. At the maximum input voltage, the common-mode input voltage seen by the ADC is shown in 式 30.

$$V_{CM} = V_{REF} + (V_{RTD\_MAX} / 2) = 1.64\ V + (390.48\ mV / 2) = 1.835\ V \quad (30)$$

As mentioned in the *Low-Noise PGA* section, the common-mode input range is shown in 式 3 and is applied to 式 31.

$$AVSS + 0.1\ V + (V_{RTD\_MAX} \times Gain) / 2 \le V_{CM} \le AVDD - 0.1\ V - (V_{RTD\_MAX} \times Gain) / 2 \quad (31)$$

After substituting in the appropriate values, the common-mode input range can be found in 式 32 and 式 33.

$$0\ V + 0.1\ V + (390.48\ mV \times 4) / 2 \le V_{CM} \le 3.3\ V - 0.1\ V - (390.48\ mV \times 4) / 2 \quad (32)$$

$$881\ mV \le V_{CM} \le 2.42\ V \quad (33)$$

Because V_{CM} = 1.835 V is within the limits of 式 33, the RTD measurement is within the input common-mode range of the ADC and PGA. At the RTD voltage minimum ($V_{RTD\ MIN}$ = 18.59 mV), a similar calculation can be made to show that the input common-mode voltage is within the range as well.

10.2.1.2.7 Input and Reference Low-Pass Filters

The differential filters chosen for this application are designed to have a –3-dB corner frequency at least 10 times larger than the bandwidth of the ADC. The selected ADS1147 sampling rate of 20 SPS results in a –3-dB bandwidth of 14.8 Hz. The –3-dB filter corner frequency is set to be roughly 250 Hz at mid-scale measurement resistance. For proper operation, the differential cutoff frequencies of the reference and input low-pass filters must be well matched. This can be difficult because as the resistance of the RTD changes over the span of the measurement, the filter cutoff frequency changes as well. To mitigate this effect, the two resistors used in the input filter (R_{I1} and R_{I2}) are chosen to be two orders of magnitude larger than the RTD. Input bias currents of the ADC causes a voltage drop across the filter resistors that shows up as a differential offset error if the bias currents and/or filter resistors are not equal. TI recommends limiting the resistors to at most 10 kΩ to reduce DC offset errors due to input bias current. R_{I1} and R_{I2} are chosen to be 4.7 kΩ.

The input filter differential capacitor (C_{I_DIFF}) is calculated starting from the cutoff frequency as shown in 式 34.

$$f_{-3dB\_DIFF} = 1 / (2 \pi \times C_{I\_DIFF} \times (R_{I1} + R_{RTD} + R_{I2})) \quad (34)$$

$$f_{-3dB\_DIFF} = 1 / (2 \pi \times C_{I\_DIFF} \times (4.7\ k\Omega + 150\ \Omega + 4.7\ k\Omega)) \quad (35)$$

After solving for C_{I_DIFF}, the capacitor is chosen to be a standard value of 68 nF.

To ensure that mismatch of the common-mode filter capacitors does not translate to a differential voltage, the common-mode capacitors (C_{I_CM1} and C_{I_CM2}) are chosen to be 10 times smaller than the differential capacitor, making them 6.8 nF each. This results in a common-mode cutoff frequency that is roughly 20 times larger than the differential filter, making the matching of the common-mode cutoff frequencies less critical.

$$f_{-3dB\_CM+} = 1 / (2 \pi \times C_{I\_CM1} \times (R_{I1} + R_{RTD} + R_{REF})) \quad (36)$$

$$f_{-3dB\_CM-} = 1 / (2 \pi \times C_{I\_CM1} \times (R_{I2} + R_{REF})) \quad (37)$$

After substituting values into 式 36 and 式 37, the common-mode cutoff frequencies are found to be f_{-3dB_CM+} = 4.13 kHz and f_{-3dB_CM-} = 4.24 kHz.

Often, filtering the reference input is not necessary and adding bulk capacitance at the reference input is sufficient. However, equations showing a design procedure calculating filter values for the reference inputs are shown below.

The differential reference filter is designed to have a –3-dB corner frequency of 250 Hz to match the differential input filter. The two reference filter resistors are selected to be 9.09 kΩ, several times larger than the value of R_{REF}. The reference filter resistors must not be sized larger than 10 kΩ or DC bias errors become significant. The differential capacitor for the reference filter is calculated as shown in 式 38.

$$f_{-3dB\_DIFF} = 1 / (2 \pi \times C_{R\_DIFF} \times (R_{R1} + R_{RTD} + R_{R2})) \quad (38)$$

$$C_{R\_DIFF} \approx 33\ nF \quad (39)$$

After solving for C_{R_DIFF}, the capacitor is chosen to be a standard value of 33 nF.

To ensure that mismatch of the common-mode filter capacitors does not translate to a differential voltage, the reference common-mode capacitors (C_{R_CM1} and C_{R_CM2}) are chosen to be 10 times smaller than the reference differential capacitor, making them 3.3 nF each. Again, the resulting cutoff frequency for the common-mode filters is roughly 20 times larger than the differential filter, making the matching of the cutoff frequencies less critical.

$$f_{-3dB\_CM+} = 1 / (2 \pi \times C_{R\_CM1} \times (R_{R1} + R_{REF})) \quad (40)$$

$$f_{-3dB\_CM-} = 1 / (2 \pi \times C_{R\_CM2} \times R_{R2}) \quad (41)$$

After substituting values into 式 40 and 式 41, common-mode cutoff frequencies for the reference filter are found to be f_{-3dB_CM+} = 4.87 kHz and f_{-3dB_CM+} = 5.31 kHz.

10.2.1.2.8 Register Settings

The register settings for this design are shown in 表 45.

表 45. Register Settings

REGISTER	NAME	SETTING	DESCRIPTION
00h	MUX0	0Ah	Select AIN_P = AIN1 and AIN_N = AIN2
01h	VBIAS	00h	
02h	MUX1	20h	Internal reference enabled, REFP0 and REFN0 reference inputs selected
03h	SYS0	22h	PGA Gain = 4, DR = 20 SPS
04h	OFC0 (1)	xxh	
05h	OFC1	xxh	
06h	OFC2	xxh	
07h	FSC0 (1)	xxh	
08h	FSC1	xxh	
09h	FSC2	xxh	
0Ah	IDAC0	x6h	ID bits may be version dependent, IDAC magnitude set to 1 mA
0Bh	IDAC1	03h (2)	IDAC1 set to AIN0; IDAC2 set to AIN3
0Ch	GPIOCFG	00h	
0Dh	GPIOCDIR	00h	
0Eh	GPIODAT	00h	

(1) A two-point gain calibration and offset calibration remove errors from the R_{REF} tolerance, offset voltage and gain error. The results are used for the OFC and FSC registers
(2) To chop the excitation current sources, swap output pins with IDAC1 register and set to 30h

10.2.1.3 Application Curves

To test the accuracy of the acquisition circuit, a series of calibrated, high-precision discrete resistors are used as the input to the system. Measurements are taken at T_A = 25°C. 図 84 displays the uncalibrated resistance measurement accuracy of the system over an input span from 20 Ω to 400 Ω. For each resistor value, 512 measurements are taken. With each measurement, IDAC1 and IDAC2 are chopped to remove the excitation current mismatch.

The uncalibrated measurement error is displayed in 図 85. The offset and gain error can be primarily attributed to the offset and gain error of the ADC. However, the accuracy of R_{REF} contributes directly to the accuracy of the measurement. To keep the gain error low, R_{REF} must be a low-drift precision resistor.

Precision temperature measurement applications are typically calibrated to remove the effects of gain and offset errors, which generally dominate the total system error. The simplest calibration method is a linear, or two-point, calibration which applies an equal and opposite gain and offset term to cancel the measured system gain and offset errors. Using the results of 図 85, the uncalibrated gain and offset error are then used to modify the Offset Calibration and the Full-Scale Calibration registers in the device. The results of this calibrated system measurement are shown in 図 86.

The results in 図 86 are converted to temperature accuracy by dividing the results by the RTD sensitivity (α) at the measured resistance. Over the full resistance input range, the maximum total measured error is ±0.011 Ω. 式 42 uses the measured resistance error and the nominal RTD sensitivity to calculate the measured temperature accuracy.

$$Error\ (^{\circ}C) = \frac{Error\ (\Omega)}{\alpha_{@0^{\circ}C}} = \frac{0.011\,\Omega}{0.385\,\frac{\Omega}{^{\circ}C}} = \pm 0.0286^{\circ}C \quad (42)$$

図 87 displays the calculated temperature measurement accuracy of the circuit assuming a linear RTD resistance to temperature response. It does not include any linearity compensation of the RTD.

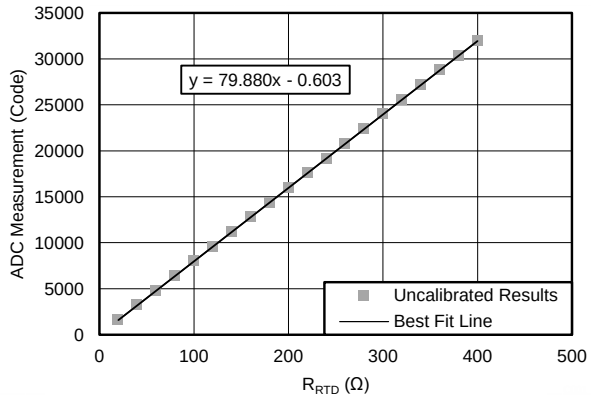


図 84. Resistance Measurement Results With Precision Resistors Before Calibration

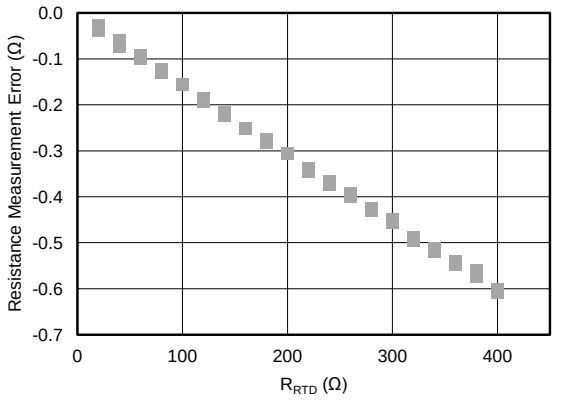


図 85. Resistance Measurement Error With Precision Resistors Before Calibration

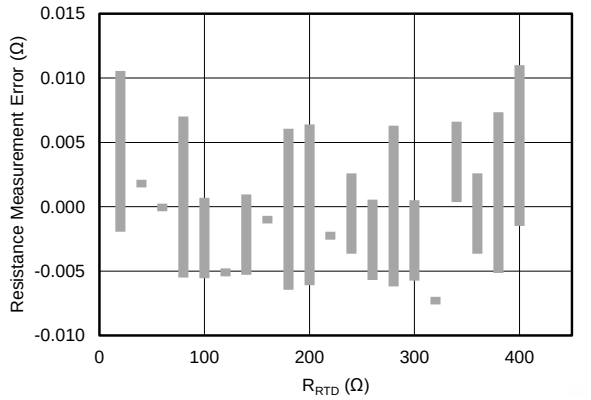


図 86. Resistance Measurement Error With Precision Resistors After Calibration

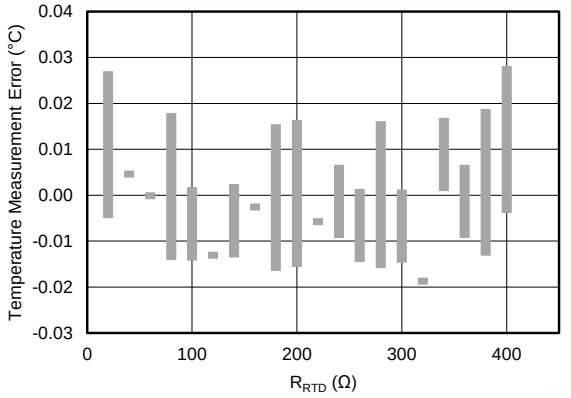


図 87. Calculated Temperature Measurement Error from Resistance Measurement Error

表 46 compares the measurement accuracy with the design goal from 表 42.

表 46. Comparison of Design Goals and Measured Performance

	GOAL	MEASURED
Calibrated resistance measurement accuracy at T_A = 25ºC	±0.077 Ω	±0.011 Ω
Calibrated temperature measurement accuracy at T_A = 25ºC	±0.2°C	±0.029°C

10.2.2 K-Type Thermocouple Measurement (–200°C to 1250°C) With Cold-Junction Compensation

図 88 shows the basic connections of a thermocouple measurement system based on the ADS1148. This circuit uses a cold-junction compensation measurement based on the *Ratiometric 3-Wire RTD Measurement System* topology shown in the previous application example. Using the IEXC1 and IEXC2 pins allow for routing of the IDAC currents without using any other analog pins. Along with the thermocouple and cold-junction measurements, four other analog inputs (AIN4 to AIN7 not shown in the schematic) are available for alternate measurements or use as GPIO pins.

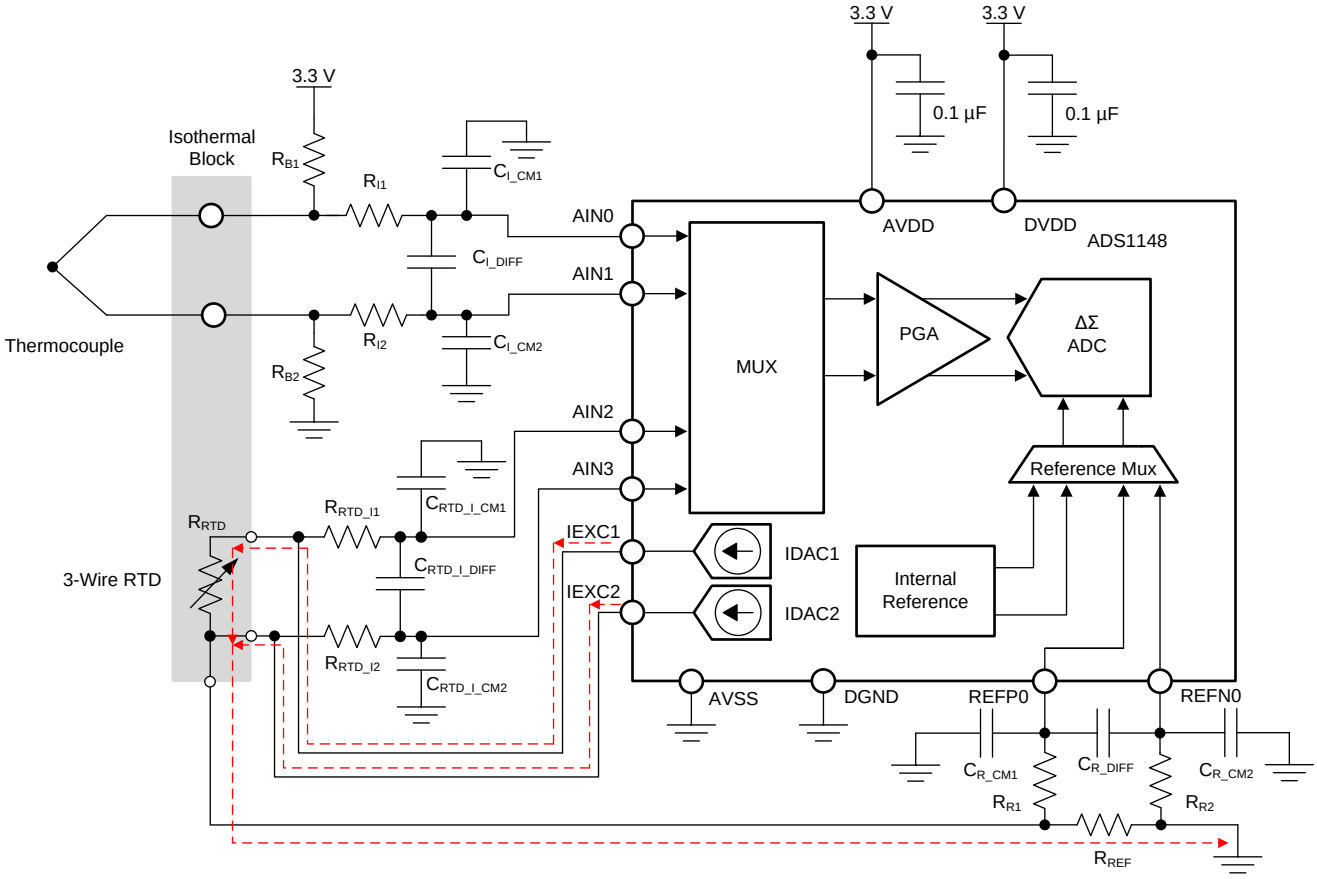


図 88. Thermocouple Measurement System Using the ADS1148

10.2.2.1 Design Requirements

表 47 shows the design requirements of the thermocouple application for the ADS1148.

表 47. Example Thermocouple Application Requirements

PARAMETER	VALUE
Supply voltage	3.3 V
Reference voltage	Internal 2.048-V reference
Update rate	≥ 10 readings per second
Thermocouple type	K
Temperature measurement	–200ºC to 1250ºC
Measurement accuracy at T_A = 25ºC (1)	±0.5ºC

(1) Not accounting for error of thermocouple and the cold-junction measurement; offset calibration is performed at $T_{(TC)} = T_{(CJ)} = 25°C$; no gain calibration.

10.2.2.2 Detailed Design Procedure

10.2.2.2.1 Biasing Resistors

The biasing resistors R_{B1} and R_{B2} are used to set the common-mode voltage of the thermocouple to within the specified common-mode voltage range of the PGA (in this example, to mid-supply AVDD / 2). If the application requires the thermocouple to be biased to GND, a bipolar supply (for example, AVDD = 2.5 V and AVSS = –2.5 V) must be used for the device to meet the common-mode voltage requirement of the PGA. When choosing the values of the biasing resistors, care must be taken so that the biasing current does not degrade measurement accuracy. The biasing current flows through the thermocouple and can cause self-heating and additional voltage drops across the thermocouple leads. Typical values for the biasing resistors range from 1 MΩ to 50 MΩ.

In addition to biasing the thermocouple, R_{B1} and R_{B2} are also useful for detecting an open thermocouple lead. When one of the thermocouple leads fails open, the biasing resistors pull the analog inputs (AIN0 and AIN1) to AVDD and AVSS, respectively. The ADC consequently reads a full-scale value, which is outside the normal measurement range of the thermocouple voltage, to indicate this failure condition.

10.2.2.2.2 Input Filtering

Although the digital filter attenuates high-frequency components of noise, TI recommends providing a first-order, passive RC filter at the inputs to further improve performance. The differential RC filter formed by R_{I1}, R_{I2}, and the differential capacitor C_{I_DIFF} offers a cutoff frequency that is calculated using 式 43.

$$f_C = 1 / (2 \pi \times (R_{I1} + R_{I2}) \times C_{I\_DIFF}) \quad (43)$$

Two common-mode filter capacitors (C_{I_CM1} and C_{I_CM2}) are also added to offer attenuation of high-frequency, common-mode noise components. TI recommends that the differential capacitor C_{I_DIFF} be at least an order of magnitude (10×) larger than the common-mode capacitors (C_{I_CM1} and C_{I_CM2}) because mismatches in the common-mode capacitors can convert common-mode noise into differential noise.

The filter resistors R_{F1} and R_{F2} also serve as current-limiting resistors. These resistors limit the current into the analog inputs (AIN0 and AIN1) of the device to safe levels if an overvoltage on the inputs occurs. Care must be taken when choosing the filter resistor values because the input currents flowing into and out of the device cause a voltage drop across the resistors. This voltage drop shows up as an additional offset error at the ADC inputs. For thermocouple measurements, TI recommends limiting the filter resistor values to below 10 kΩ.

The filter component values used in this design are: $R_{I1} = R_{I2} = 1$ kΩ, $C_{I\_DIFF} = 100$ nF, and $C_{I\_CM1} = C_{I\_CM2} = 10$ nF.

10.2.2.2.3 PGA Setting

The highest measurement resolution is achieved when matching the largest potential input signal to the FSR of the ADC by choosing the highest possible gain. From the design requirement, the maximum thermocouple voltage occurs at $T_{TC} = 1250$°C and is $V_{TC} = 50.644$ mV as defined in the tables published by the National Institute of Standards and Technology (NIST) using a cold-junction temperature of $T_{CJ} = 0$°C. A thermocouple produces an output voltage that is proportional to the temperature difference between the thermocouple tip and the cold junction. If the cold junction is at a temperature below 0°C, the thermocouple produces a voltage larger than 50.644 mV. The isothermal block area is constrained by the operating temperature range of the device. Therefore, the isothermal block temperature is limited to –40°C. A K-type thermocouple at $T_{TC} = 1250$°C produces an output voltage of $V_{TC} = 50.644$ mV – (–1.527 mV) = 52.171 mV when referenced to a cold-junction temperature of $T_{CJ} = –40$°C. The maximum gain that can be applied when using the internal 2.048-V reference is then calculated as 39.3 from 式 44. The next smaller PGA gain setting the device offers is 32.

$$Gain_{MAX} = V_{REF} / V_{TC\ MAX} = 2.048\ V / 52.171\ mV = 39.3 \quad (44)$$

10.2.2.2.4 Cold-Junction Measurement

AIN2 and AIN3 are attached to a 3-wire RTD that is used to measure the cold-junction temperature. Similar to the example in the *Ratiometric 3-Wire RTD Measurement System* section, the 3-wire RTD design is the same except the inputs and excitation current sources have been changed. Note that R_{REF} and PGA Gain can be optimized for a reduced temperature range.

The device does not perform an automatic cold-junction compensation of the thermocouple. This compensation must be done in the microcontroller that interfaces to the device. The microcontroller requests one or multiple readings of the thermocouple voltage from the device and then sets the device to measure the cold junction with the RTD to compensate for the cold-junction temperature.

An algorithm similar to the following must be implemented on the microcontroller to compensate for the cold-junction temperature:

1. Measure the thermocouple voltage, $V_{(TC)}$, between AIN0 and AIN1.
2. Measure the temperature of the cold junction, $T_{(CJ)}$, using a ratiometric measurement with the 3-wire RTD across AIN2 and AIN3.
3. Convert the cold-junction temperature into an equivalent thermoelectric voltage, $V_{(CJ)}$, using the tables or equations provided by NIST.
4. Add $V_{(TC)}$ and $V_{(CJ)}$ and translate the summation back into a thermocouple temperature using the NIST tables or equations again.

There are alternate methods of measuring the cold-junction temperature. The additional analog input channels of the device can be used in this case to measure the cold-junction temperature with a thermistor or an alternate analog temperature sensor.

10.2.2.2.5 Calculated Resolution

To get an approximation of the achievable temperature resolution, the peak-to-peak noise of the ADS1148 at Gain = 32 and DR = 20 SPS (1.95 μV_{PP}) is taken from 表 1. The noise is divided by the average sensitivity of a K-type thermocouple (41 µV/°C), as shown in 式 45.

$$\text{Temperature Resolution} = 1.95\ \mu V / 41\ \mu V/°C = 0.048°C \quad (45)$$

10.2.2.2.6 Register Settings

The register settings for this design are shown in 表 48. The inputs are selected to measure the thermocouple and the internal reference is enabled and selected. The excitation current sources are also enabled and selected. While this does consume some power, it allows for a quick transition for the cold-junction measurement.

表 48. Register Settings for the Thermocouple Measurement

REGISTER	NAME	SETTING	DESCRIPTION
00h	MUX0	01h	Select AIN_P = AIN0, AIN_N = AIN1
01h	VBIAS	00h	
02h	MUX1	30h	Internal reference enabled, internal reference selected
03h	SYS0	52h	PGA Gain = 32, DR = 20 SPS
04h	OFC0	xxh	
05h	OFC1	xxh	
06h	OFC2	xxh	
07h	FSC0	xxh	
08h	FSC1	xxh	
09h	FSC2	xxh	
0Ah	IDAC0	x6h	IDAC magnitude set to 1 mA
0Bh	IDAC1	89h	IDAC1 set to IEXC1, IDAC2 set to IEXC2
0Ch	GPIOCFG	00h	
0Dh	GPIOCDIR	00h	
0Eh	GPIODAT	00h	

Changing to the cold-junction measurement, the registers are set to measure the RTD. This requires changing the input, the reference input, the gain, and any calibration settings required for the measurement accuracy. 表 49 shows the register settings for the RTD measurement used for cold-junction compensation.

表 49. Register Settings for the Cold-Junction Measurement

REGISTER	NAME	SETTING	DESCRIPTION
00h	MUX0	13h	Select AIN_P = AIN2, AIN_N = AIN3
01h	VBIAS	00h	
02h	MUX1	20h	Internal reference enabled, REFP0 and REFN0 selected
03h	SYS0	22h	PGA Gain = 4, DR = 20 SPS
04h	OFC0	xxh	Calibration values are different between measurement settings
05h	OFC1	xxh	
06h	OFC2	xxh	
07h	FSC0	xxh	
08h	FSC1	xxh	
09h	FSC2	xxh	
0Ah	IDAC0	x6h	IDAC magnitude set to 1 mA
0Bh	IDAC1	89h	IDAC1 set to IEXC1, IDAC2 set to IEXC2
0Ch	GPIOCFG	00h	
0Dh	GPIOCDIR	00h	
0Eh	GPIODAT	00h	

10.3 Do's and Don'ts

- Do partition the analog, digital, and power supply circuitry into separate sections on the PCB.
- Do use a single ground plane for analog and digital grounds.
- Do place the analog components close to the ADC pins using short, direct connections.
- Do keep the SCLK pin free of glitches and noise.
- Do verify that the analog input voltages are within the specified PGA input voltage range under all input conditions.
- Do float unused analog input pins to minimize input leakage current. Connecting unused pins to AVDD is the next best option.
- Do provide current limiting to the analog inputs in case overvoltage faults occur.
- Do use a low-dropout linear regulator (LDO) to reduce ripple voltage generated by switch-mode power supplies. This is especially true for AVDD where the supply noise may affect the performance.
- Don't cross analog and digital signals.
- Don't allow the analog and digital power supply voltages to exceed 5.5 V under all conditions, including during power up and power down.

図 89 shows Do's and Don'ts of ADC circuit connections.

Do's and Don'ts (continued)

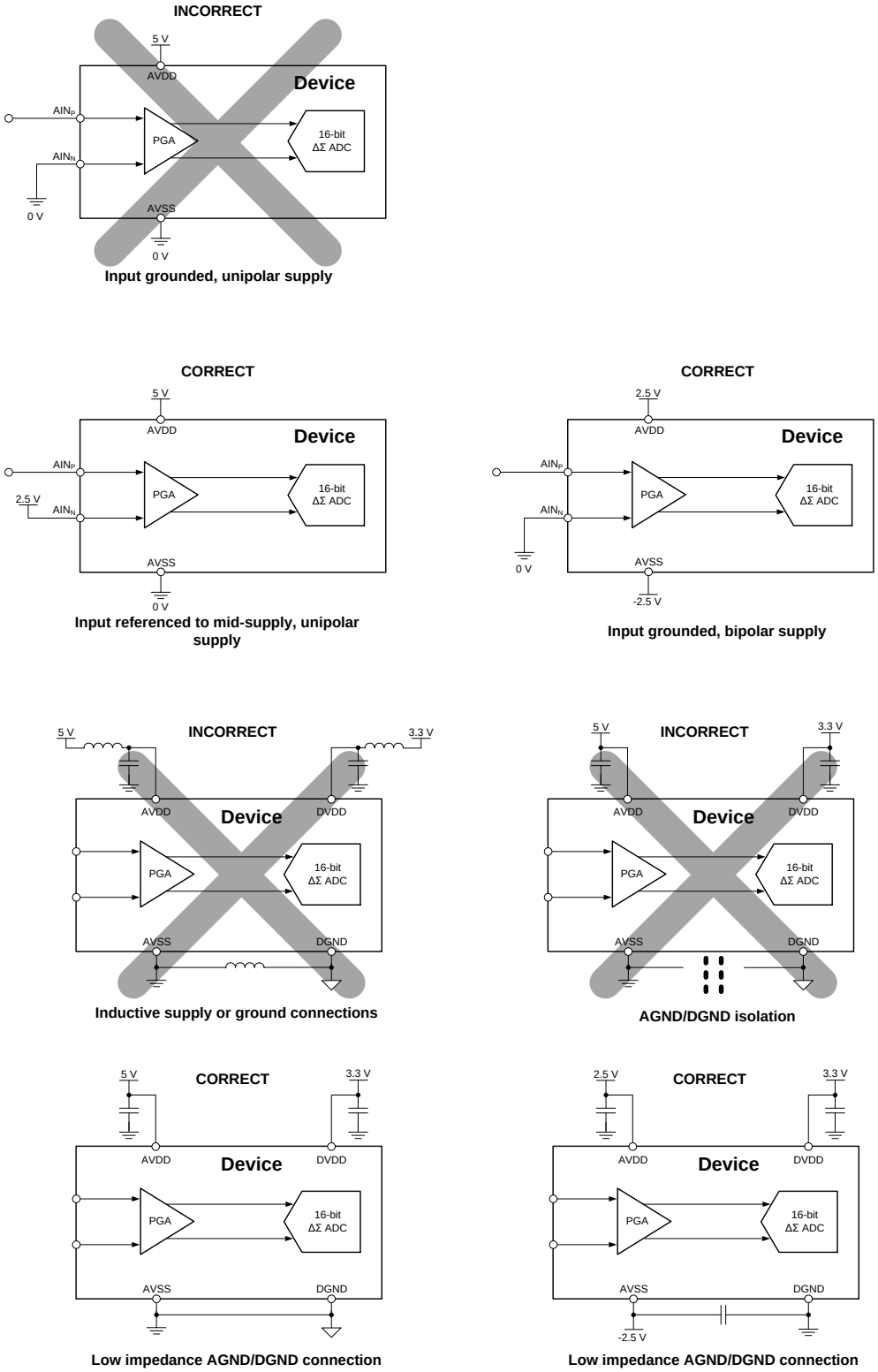


図 89. Do's and Don'ts Circuit Connections

11 Power Supply Recommendations

The device requires two power supplies: analog (AVDD, AVSS) and digital (DVDD, DGND). The analog power supply can be bipolar (for example, AVDD = 2.5 V, AVSS = –2.5 V) or unipolar (for example, AVDD = 3.3 V, AVSS = 0 V) and is independent of the digital power supply. The digital supply sets the digital I/O levels (with the exception of the GPIO levels which are set by the analog supply of AVDD to AVSS).

11.1 Power Supply Sequencing

The power supplies can be sequenced in any order but in no case must any analog or digital inputs exceed the respective analog or digital power-supply voltage limits. Wait at least 2^{16} t_{CLK} cycles after all power supplies are stabilized before communicating with the device to allow the power-on reset process to complete.

11.2 Power Supply Decoupling

Good power-supply decoupling is important to achieve optimum performance. AVDD, AVSS (when using a bipolar supply) and DVDD must be decoupled with at least a 0.1-µF capacitor, as shown in 図 90. Place the bypass capacitors as close to the power-supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes. TI recommends connecting analog and digital ground together as close to the device as possible.

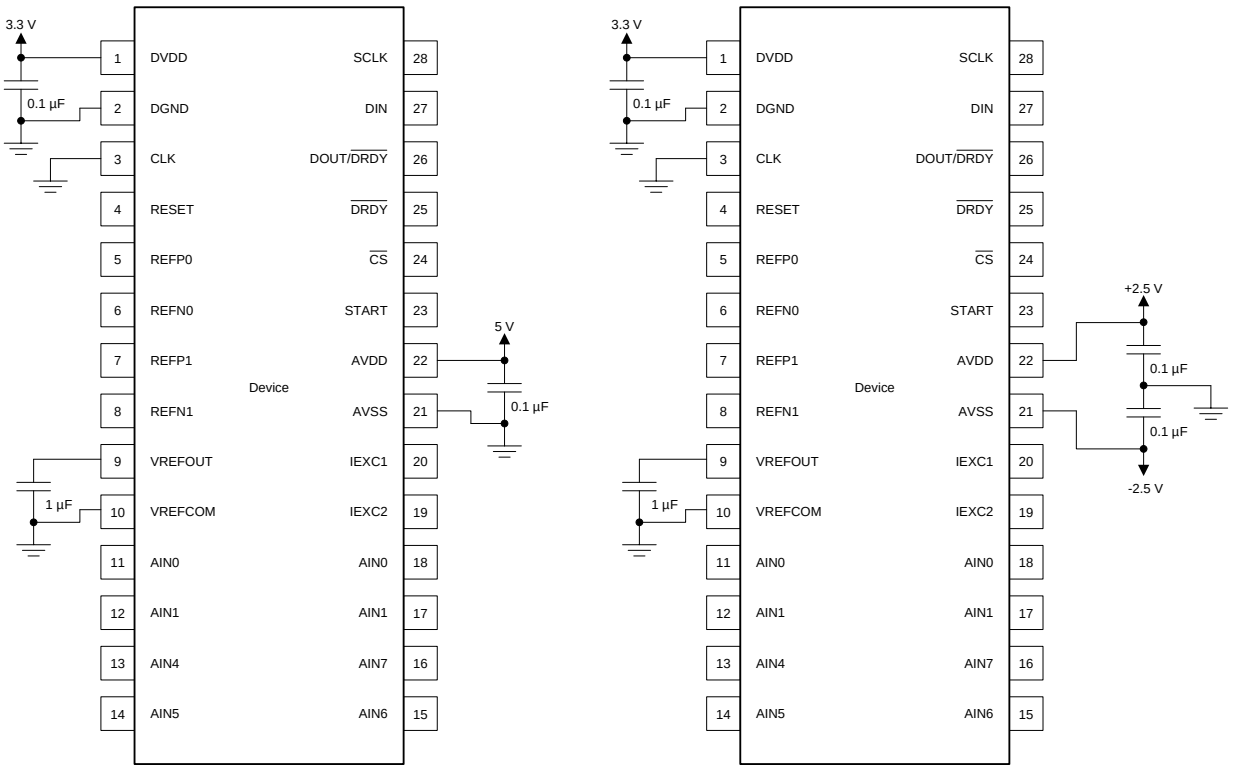


図 90. Power Supply Decoupling for Unipolar and Bipolar Supply Operation

12 Layout

12.1 Layout Guidelines

TI recommends employing best design practices when laying out a printed-circuit board (PCB) for both analog and digital components. This recommendation generally means that the layout separates analog components [such as ADCs, amplifiers, references, digital-to-analog converters (DACs), and analog MUXs] from digital components [such as microcontrollers, complex programmable logic devices (CPLDs), field-programmable gate arrays (FPGAs), radio frequency (RF) transceivers, universal serial bus (USB) transceivers, and switching regulators]. An example of good component placement is shown in 図 91. Although 図 91 provides a good example of component placement, the best placement for each application is unique to the geometries, components, and PCB fabrication capabilities employed. That is, there is no single layout that is perfect for every design and careful consideration must always be used when designing with any analog component.

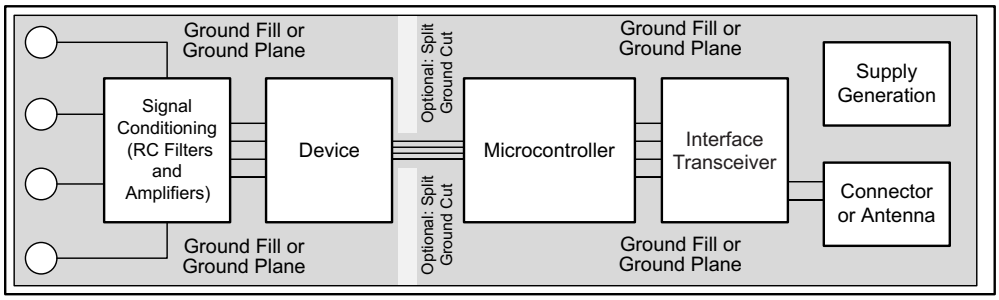


図 91. System Component Placement

The following outlines some basic recommendations for the layout of the ADS1148 to get the best possible performance of the ADC. A good design can be ruined with a bad circuit layout.

- Separate analog and digital signals. To start, partition the board into analog and digital sections where the layout permits. Route digital lines away from analog lines. This prevents digital noise from coupling back into analog signals.
- The ground plane can be split into an analog plane (AGND) and digital plane (DGND), but this is not necessary. Place digital signals over the digital plane, and analog signals over the analog plane. As a final step in the layout, the split between the analog and digital grounds must be connected to together at the ADC.
- Fill void areas on signal layers with ground fill.
- Provide good ground return paths. Signal return currents flow on the path of least impedance. If the ground plane is cut or has other traces that block the current from flowing right next to the signal trace, it has to find another path to return to the source and complete the circuit. If it is forced into a larger path, it increases the chance that the signal radiates. Sensitive signals are more susceptible to EMI interference.
- Use bypass capacitors on supplies to reduce high frequency noise. Do not place vias between bypass capacitors and the active device. Placing the bypass capacitors on the same layer as close to the active device yields the best results.
- Consider the resistance and inductance of the routing. Often, traces for the inputs have resistances that react with the input bias current and cause an added error voltage. Reducing the loop area enclosed by the source signal and the return current reduces the inductance in the path. Reducing the inductance reduces the EMI pickup and reduce the high frequency impedance seen by the device.
- Watch for parasitic thermocouples in the layout. Dissimilar metals going from each analog input to the sensor may create a parasitic themocouple which can add an offset to the measurement. Differential inputs must be matched for both the inputs going to the measurement source.
- Analog inputs with differential connections must have a capacitor placed differentially across the inputs. Best input combinations for differential measurements use adjacent analog input lines such as AIN0, AIN1 and AIN2, AIN3. The differential capacitors must be of high quality. The best ceramic chip capacitors are C0G (NPO), which have stable properties and low noise characteristics.

12.2 Layout Example

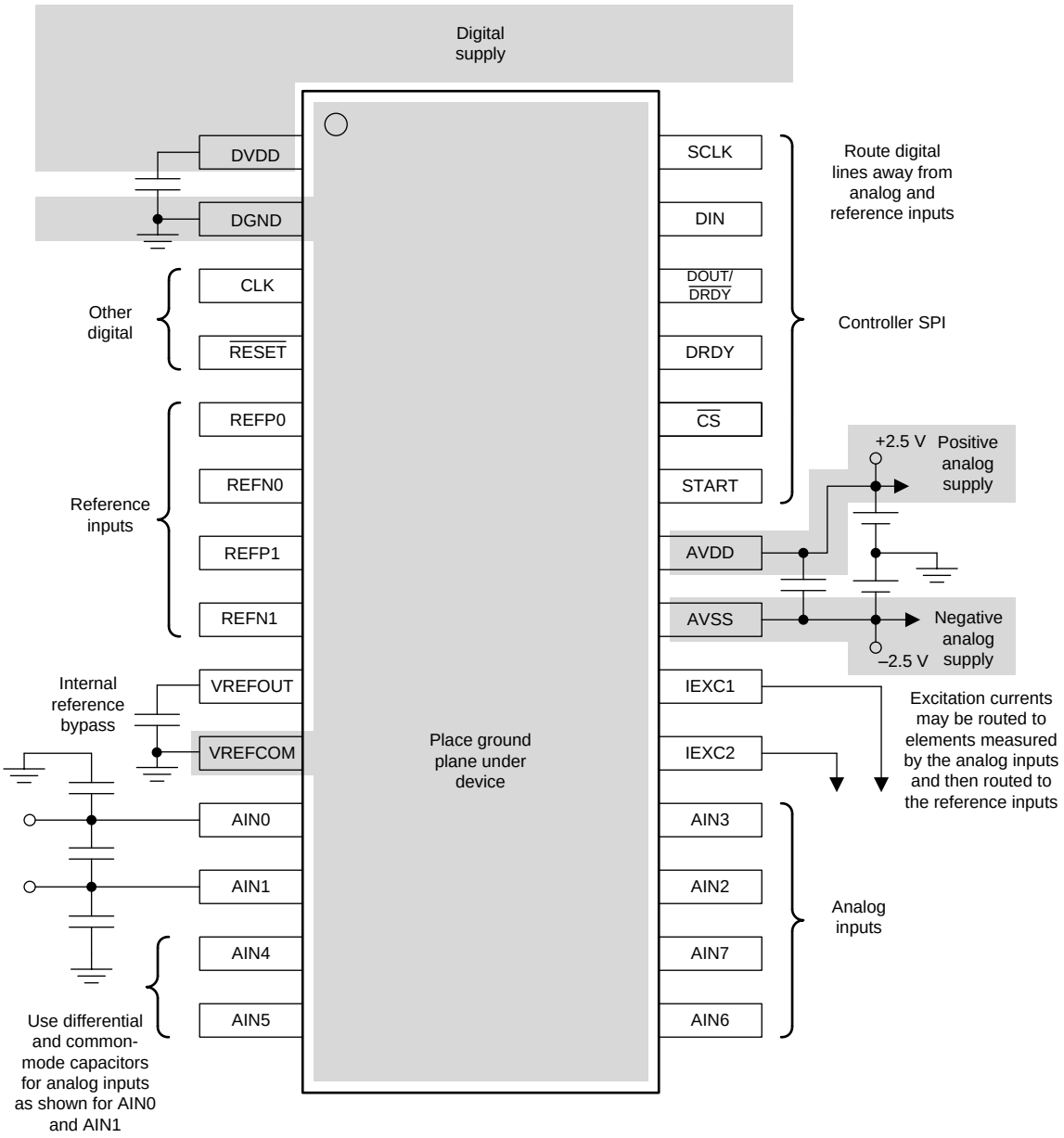


図 92. ADS114x Layout Example

13 デバイスおよびドキュメントのサポート

13.1 ドキュメントのサポート

13.1.1 関連資料

関連資料については、以下を参照してください。

- *『ADS1247およびADS1248を使用する温度測定アプリケーションの例』*(SBAA180)
- *『ADS1148およびADS1248ファミリのデバイスを使用するRTDレシオメトリック測定およびフィルタリング』*(SBAA201)
- *『3線式RTD測定システムのリファレンス・デザイン、-200℃～850℃』*(SLAU520)
- *『A/D仕様およびパフォーマンス特性の用語集』*(SBAA147)

13.2 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 50. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
ADS1146	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
ADS1147	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
ADS1148	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

13.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

13.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.5 商標

E2E is a trademark of Texas Instruments.
SPI is a trademark of Motorola, Inc.
All other trademarks are the property of their respective owners.

13.6 静電気放電に関する注意事項

これらのデバイスは、限定的なESD(静電破壊)保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS1146IPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ADS1146	Samples
ADS1146IPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ADS1146	Samples
ADS1147IPW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ADS1147	Samples
ADS1147IPWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ADS1147	Samples
ADS1148IPW	ACTIVE	TSSOP	PW	28	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ADS1148	Samples
ADS1148IPWR	ACTIVE	TSSOP	PW	28	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ADS1148	Samples
ADS1148IRHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ADS 1148	Samples
ADS1148IRHBT	ACTIVE	VQFN	RHB	32	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ADS 1148	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF ADS1148 :

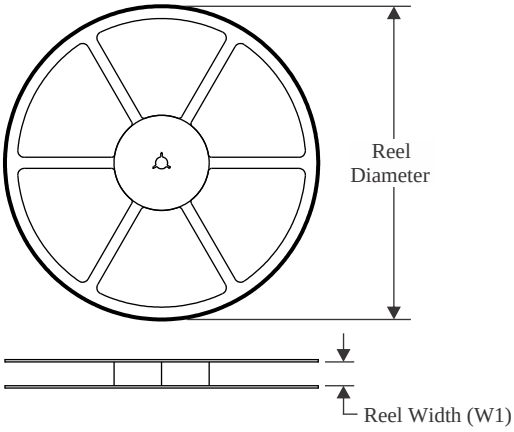
- Automotive : ADS1148-Q1

NOTE: Qualified Version Definitions:

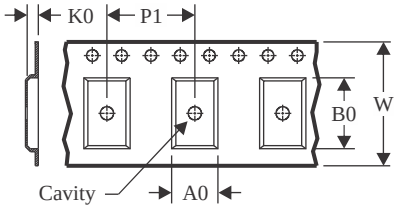
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

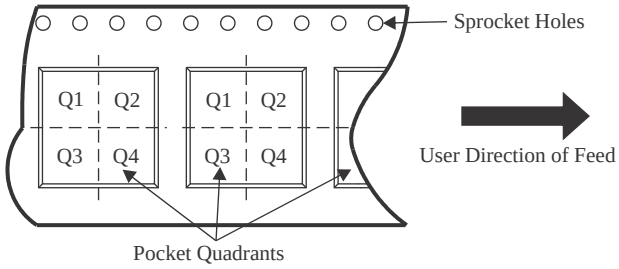


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

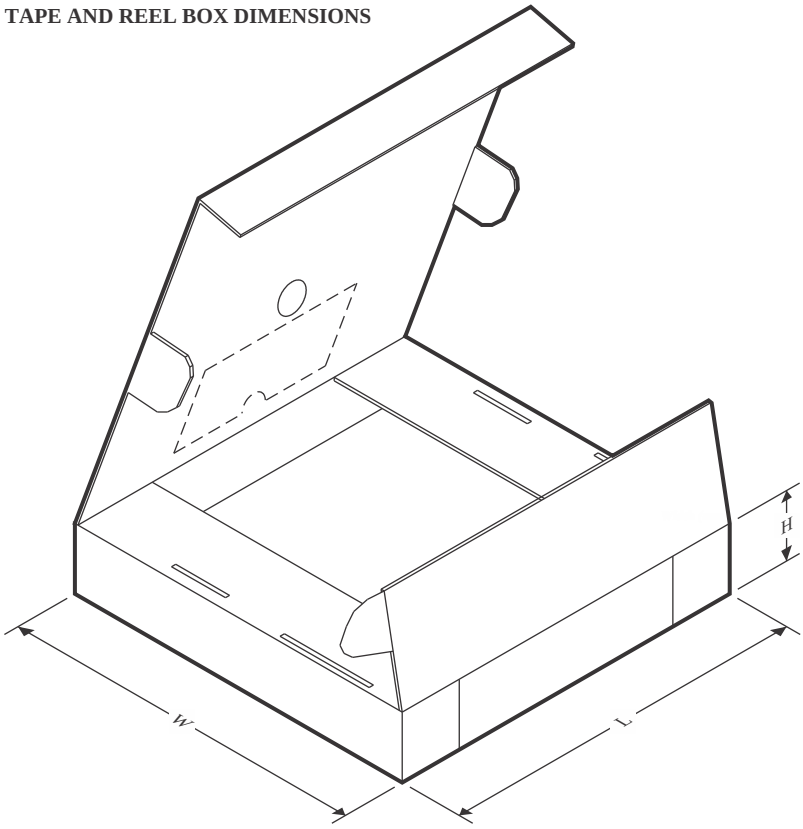
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1146IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
ADS1147IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
ADS1148IPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
ADS1148IRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
ADS1148IRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

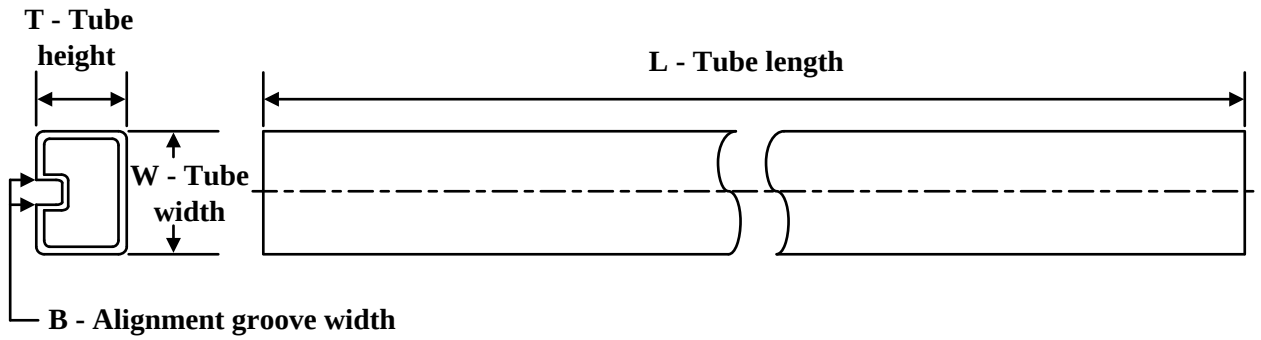
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1146IPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
ADS1147IPWR	TSSOP	PW	20	2000	356.0	356.0	35.0
ADS1148IPWR	TSSOP	PW	28	2000	356.0	356.0	35.0
ADS1148IRHBR	VQFN	RHB	32	3000	346.0	346.0	33.0
ADS1148IRHBT	VQFN	RHB	32	250	182.0	182.0	20.0

TUBE



*All dimensions are nominal

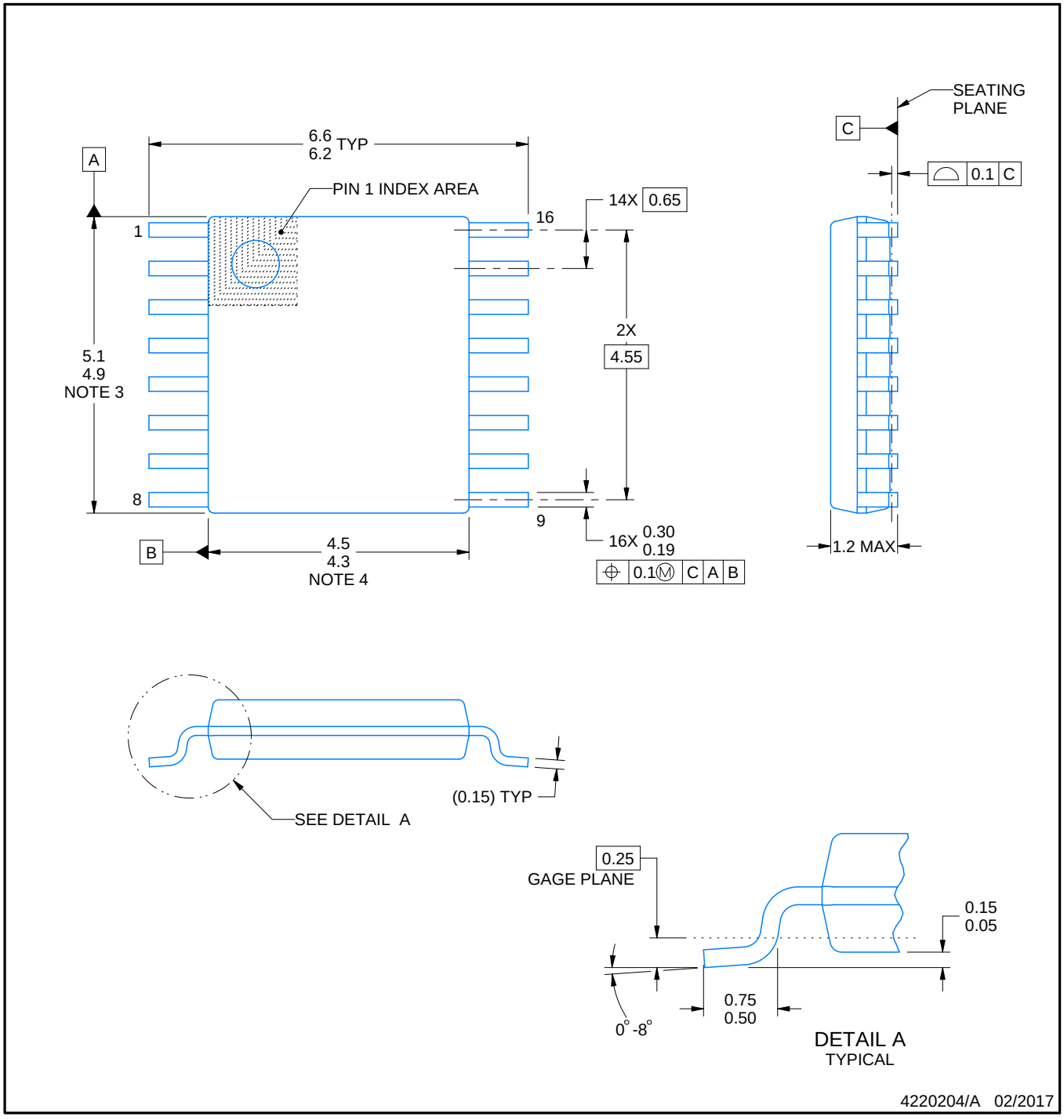
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ADS1146IPW	PW	TSSOP	16	90	530	10.2	3600	3.5
ADS1147IPW	PW	TSSOP	20	70	530	10.2	3600	3.5
ADS1148IPW	PW	TSSOP	28	50	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0016A

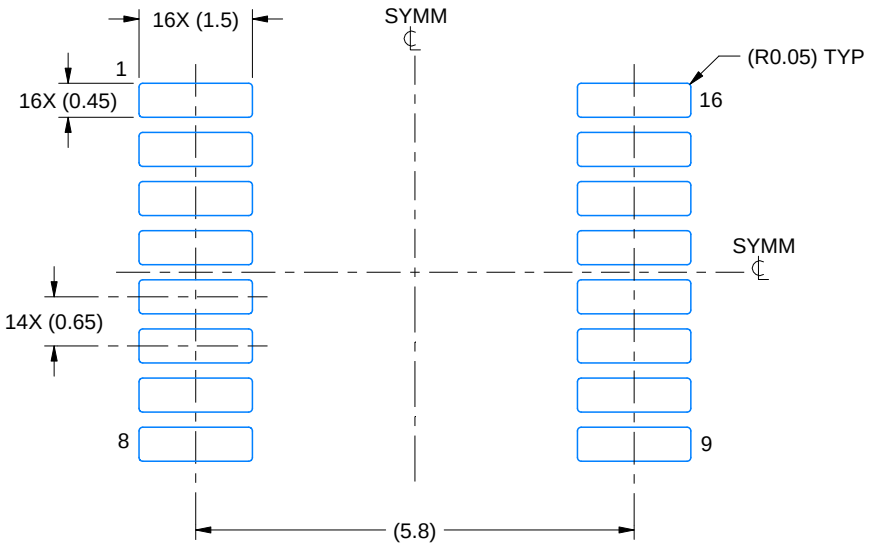
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

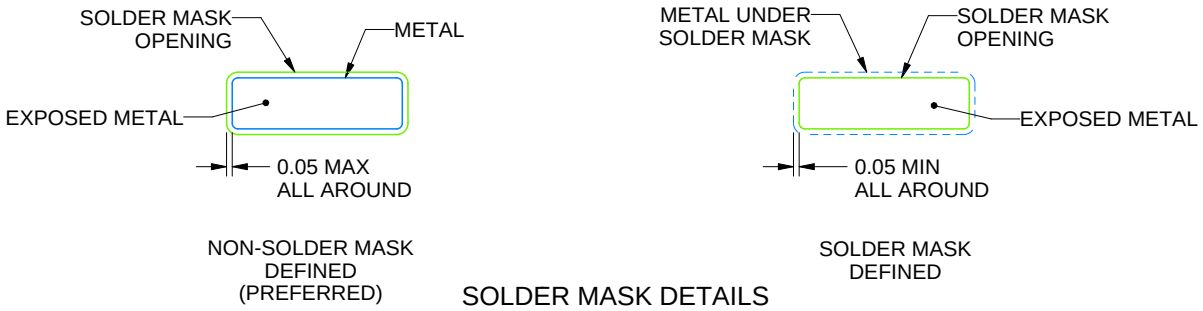


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

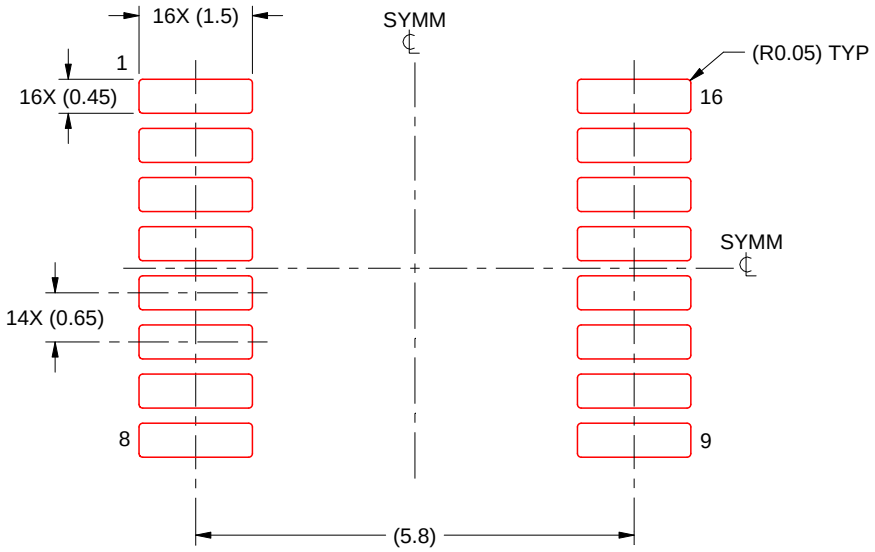


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



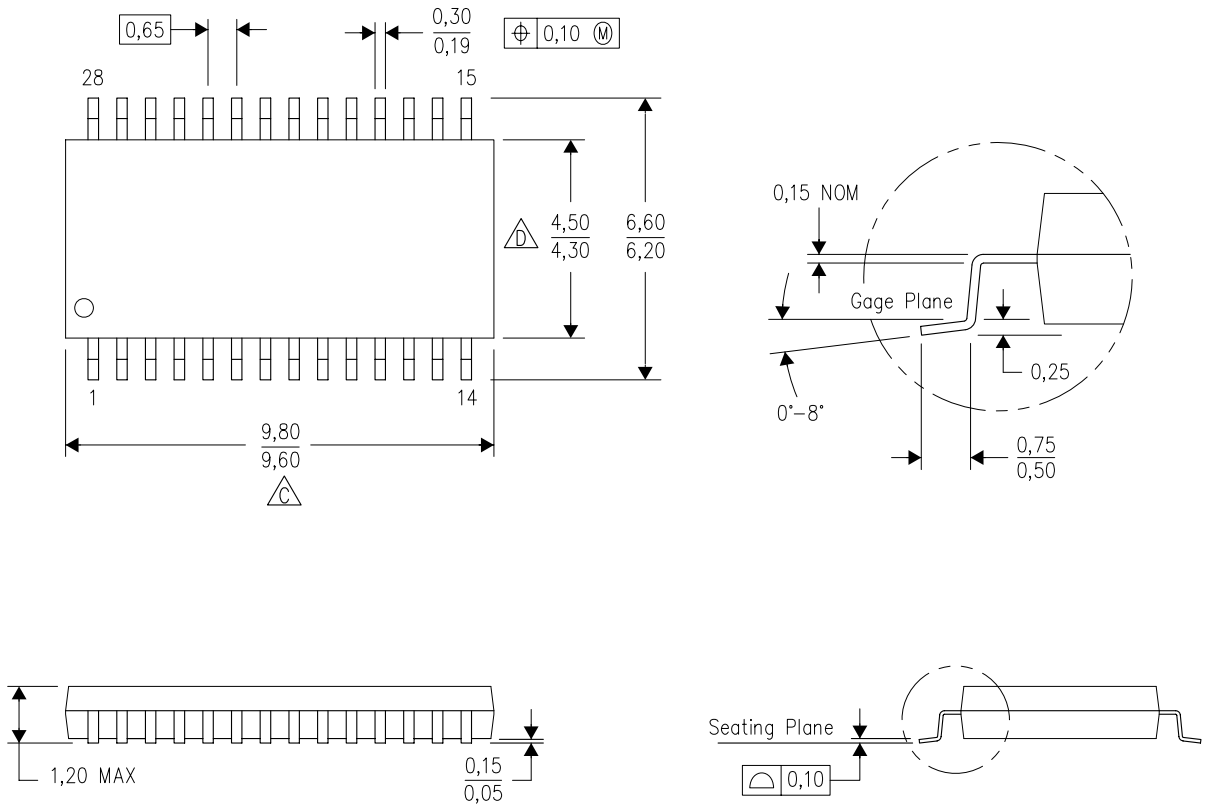
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

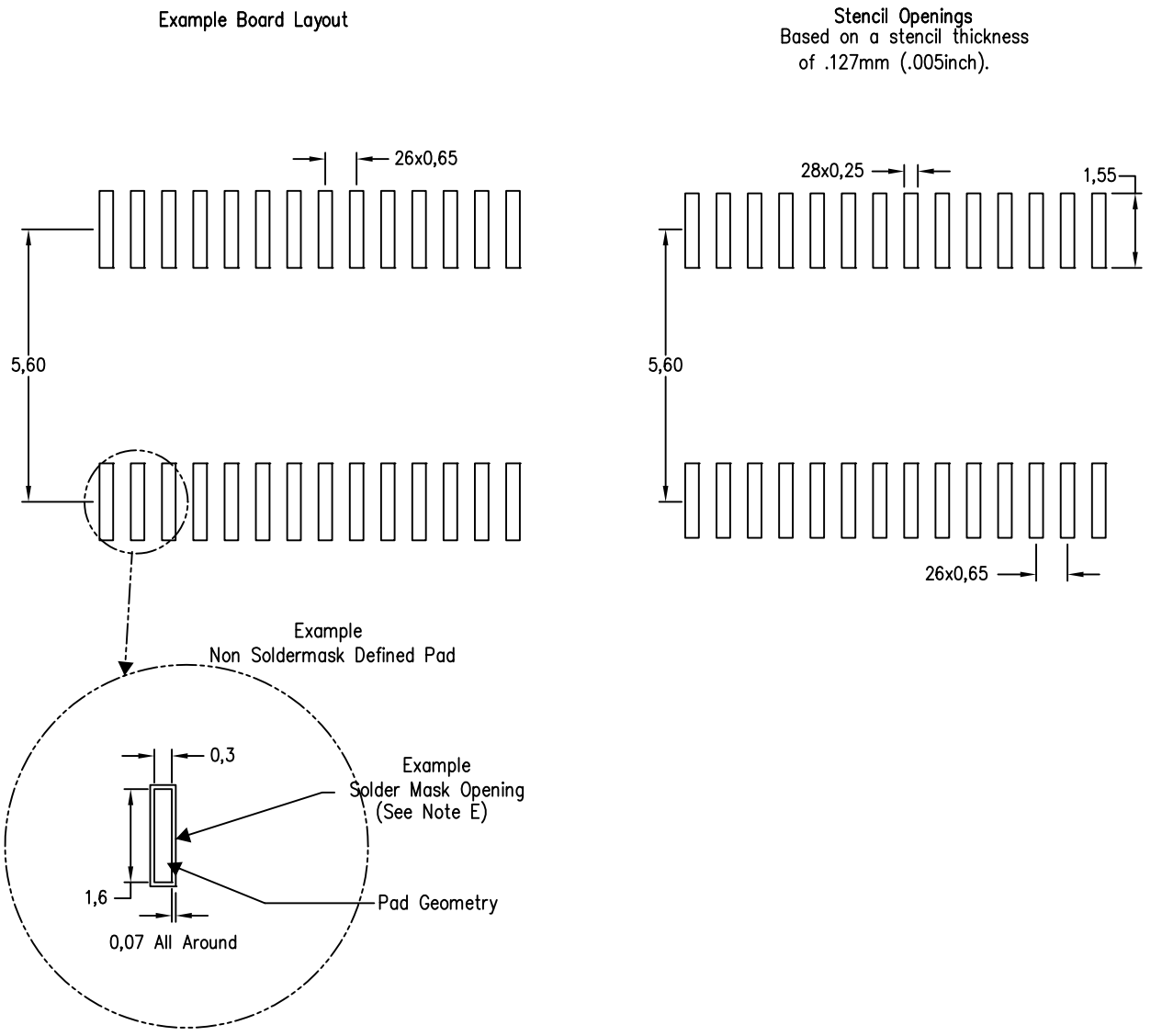
PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



4040064–7/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



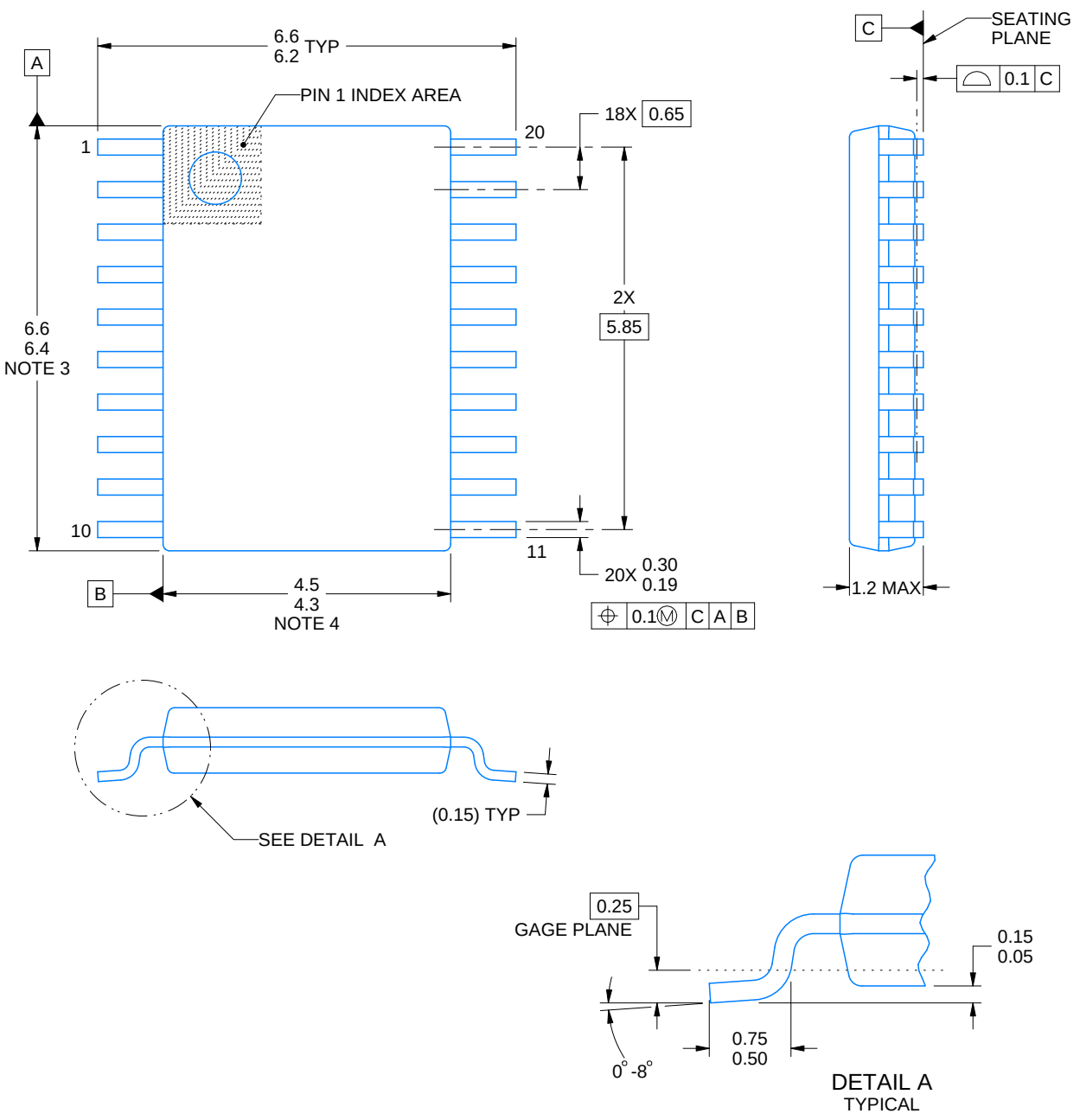
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PW0020A

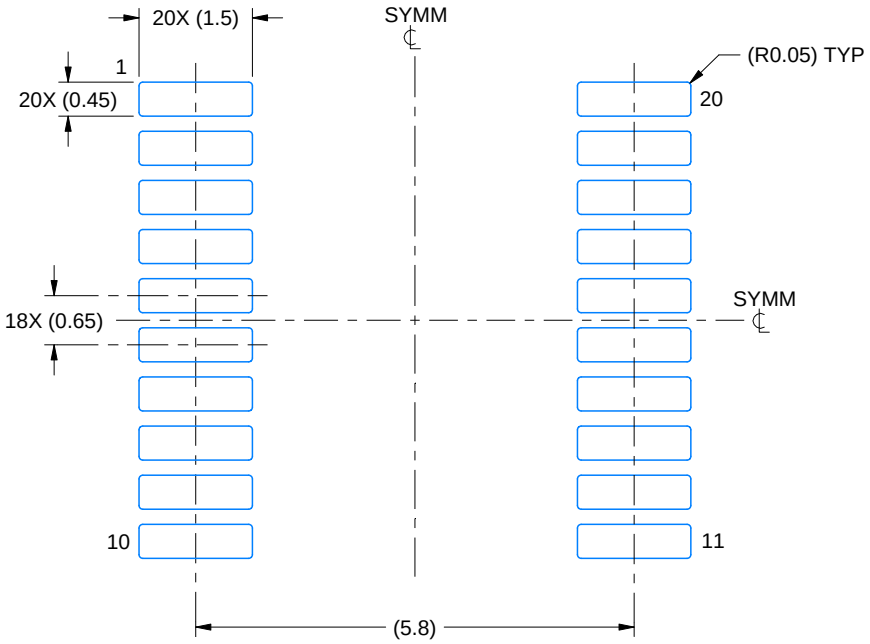
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



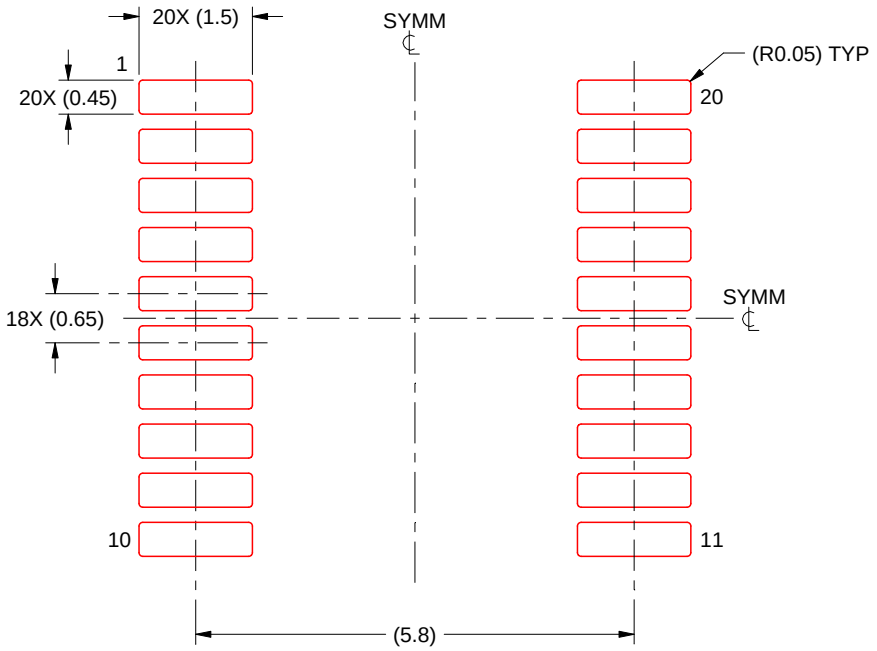
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



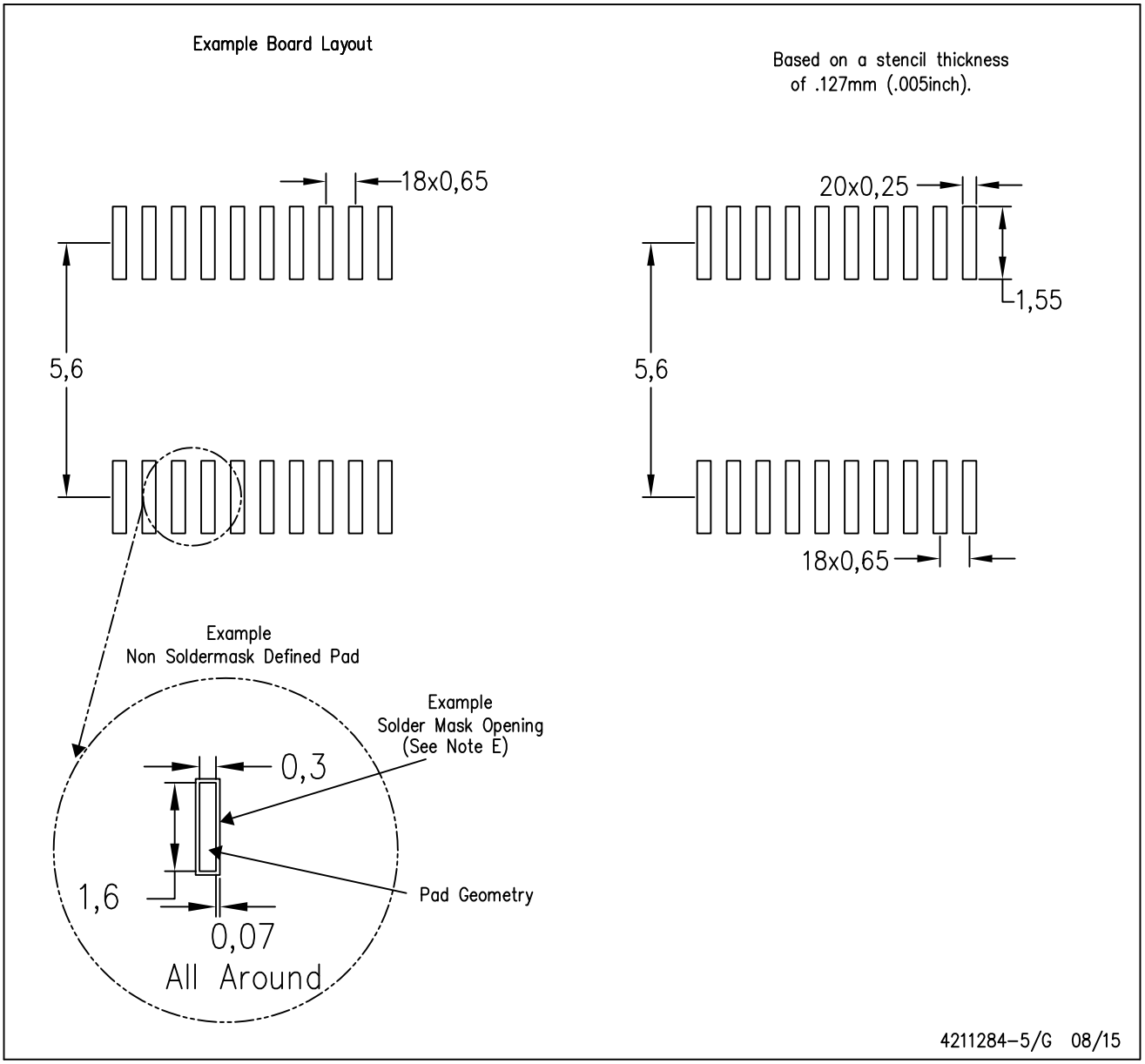
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

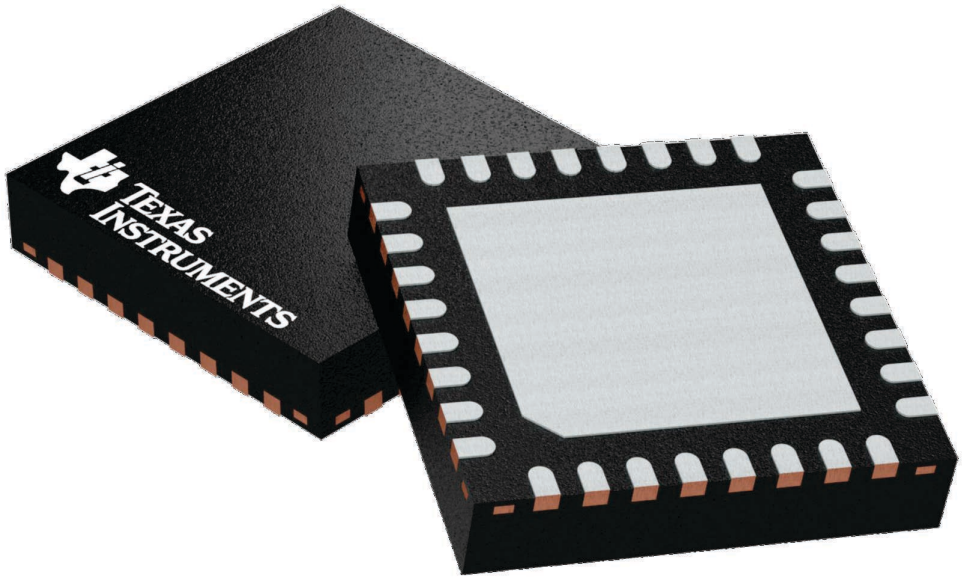
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

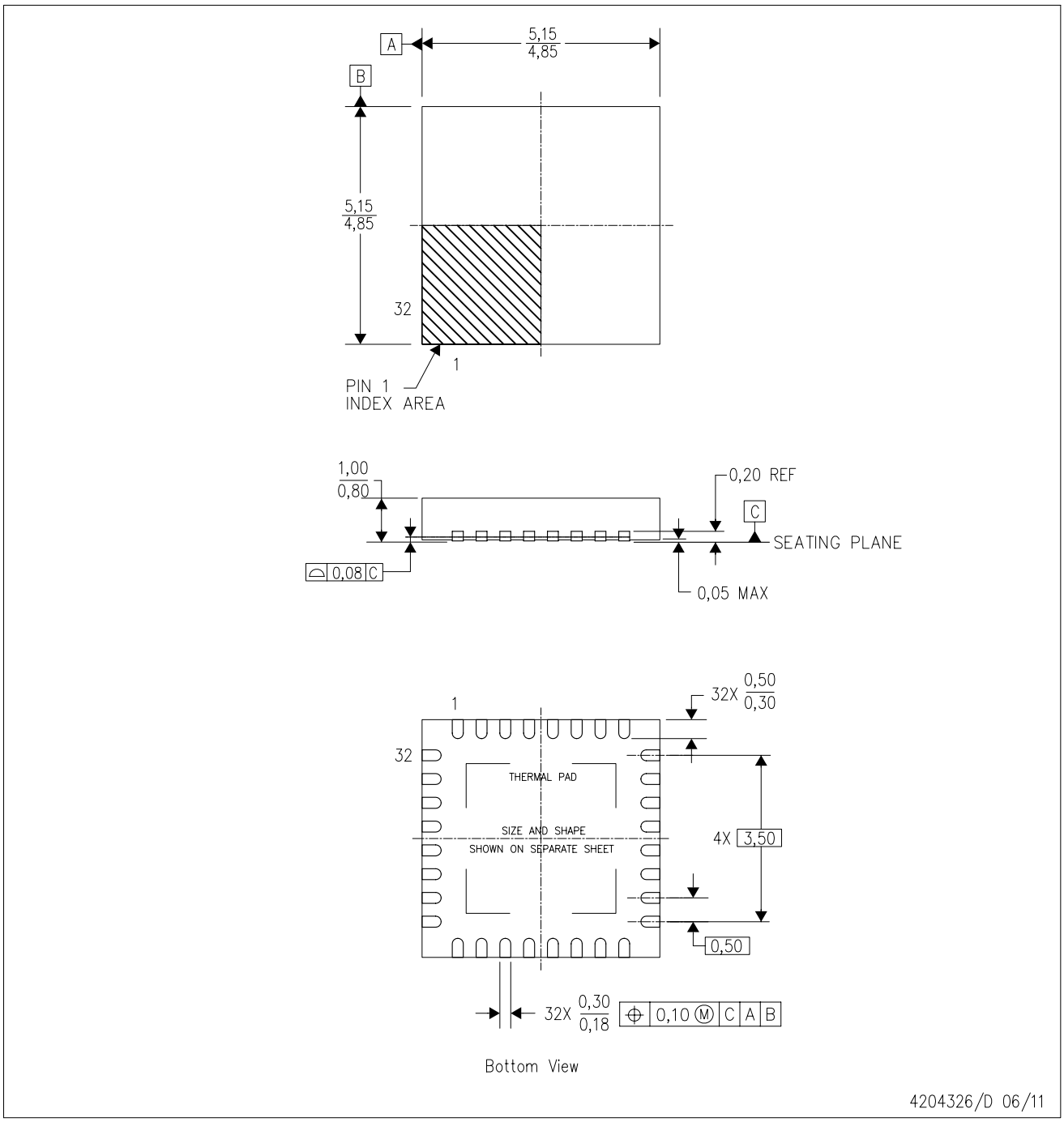
PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224745/A

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

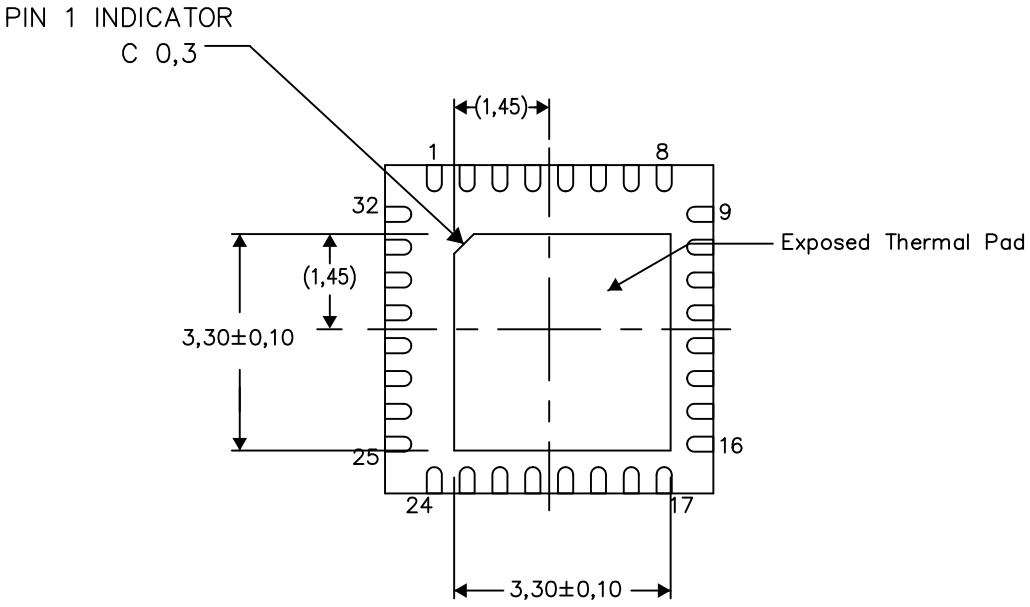
RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206356–8/AC 05/15

NOTE: A. All linear dimensions are in millimeters

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