TEXAS INSTRUMENTS
ADS1288
JAJSQP4 – FEBRUARY 2024

ADS1288 地震検出アプリケーション向け、32 ビット、デルタ シグマ ADC

1 特長

- 消費電力:
  - PGA 動作:5mW (標準値)
  - バッファ動作:3mW (標準値)
- ダイナミック レンジ:
  - PGA ゲイン:1、500SPS (122dB、標準値)
  - バッファ動作:500SPS (122dB、標準値)
- THD:< –120dB (標準値)
- CMRR:120dB (標準値)
- フレキシブルなデジタル フィルタ:
  - Sinc + FIR + IIR (選択可能)
  - 線形または最小位相
  - ハイパス フィルタ
- データ レート:125SPS～2000SPS
- PGA ゲイン:1～64
- SYNC 入力
- クロック誤差補償
- 2 チャネル マルチプレクサ
- オフセットおよびゲインの較正
- 汎用デジタル I/O
- アナログ電源の動作:5V、3.3V または ±2.5V

2 アプリケーション

- エネルギー探査
- 受動的地震波観測
- 地球科学および地質学
- 高精度計測機器

3 概要

ADS1288 は、プログラマブル ゲイン アンプ (PGA) と有限インパルス応答 (FIR) フィルタを備えた 32 ビット、低消費電力の A/D コンバータ (ADC) です。この ADC は、低消費電力による長いバッテリ動作時間が求められる地震関連機器の厳しい要件に合わせて設計されています。

低ノイズ PGA により、ADC のゲイン 1～64 のダイナミック レンジが拡張されます。この PGA により、外付けアンプを使用せずに、ジオフォンやトランス結合のハイドロフォンを直接接続できます。オプションのユニティ ゲイン バッファによって消費電力が低減されます。

この ADC は、高分解能のデルターシグマ (ΔΣ) 変調器と、位相応答を設定できる FIR フィルタを内蔵しています。ハイパス フィルタは、DC および低周波数成分を信号から除去します。サンプル レート コンバータは、最大 7ppb の分解能の精度でクロック周波数誤差を補償します。

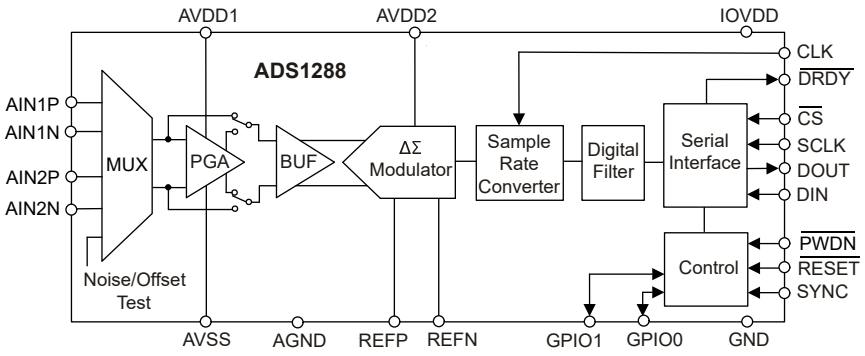
デバイスの消費電力を最小限に抑えるため、この ADC は 3.3V の動作をサポートしています。消費電力は、バッファ モード動作で 3mW (標準値)、PGA モード動作で 5mW (標準値) です。

この ADC は小型の 5mm × 5mm VQFN パッケージで供給され、–40℃～+85℃の周囲温度範囲で仕様が規定されています。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
ADS1288	RHB (VQFN、32)	5mm × 5mm

(1) 詳細については、「メカニカル、パッケージ、および注文情報」を参照してください。
(2) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



機能ブロック図

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4 Pin Configuration and Functions

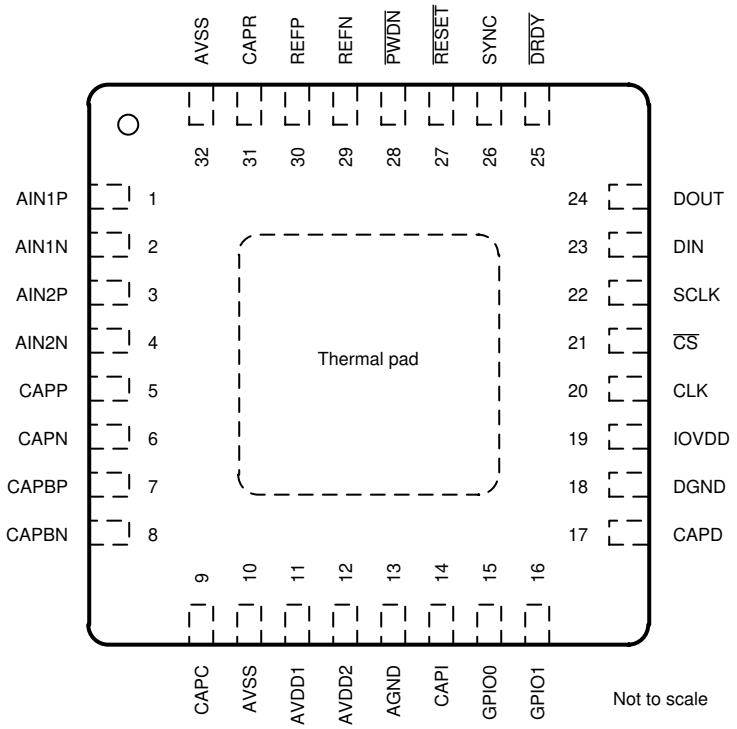


図 4-1. RHB Package, 32-Pin, 5mm × 5mm VQFN (Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	AIN1P	Analog input	Channel 1 positive input.
2	AIN1N	Analog input	Channel 1 negative input.
3	AIN2P	Analog input	Channel 2 positive input.
4	AIN2N	Analog input	Channel 2 negative input.
5	CAPP	Analog internal	PGA positive capacitor. Connect a 10nF C0G capacitor across CAPP and CAPN.
6	CAPN	Analog internal	PGA negative capacitor. Connect a 10nF C0G capacitor across CAPP and CAPN.
7	CAPBP	Analog internal	Buffer positive capacitor. Connect a 47nF C0G capacitor to AVSS.
8	CAPBN	Analog internal	Buffer negative capacitor. Connect a 47nF C0G capacitor to AVSS.
9	CAPC	Analog internal	Charge-pump capacitor. Connect a 4.7nF, minimum 10V rated capacitor to AGND.
10	AVSS	Analog supply	PGA negative analog supply. See the *Analog Power Supplies* section for details.
11	AVDD1	Analog supply	PGA positive analog supply. See the *Analog Power Supplies* section for details.
12	AVDD2	Analog supply	Modulator analog supply. See the *Analog Power Supplies* section for details.
13	AGND	Analog ground	Analog ground.
14	CAPI	Analog internal	Input bias capacitor. Connect a 100nF ceramic capacitor to AGND.
15	GPIO0	Digital I/O	General-purpose I/O.
16	GPIO1	Digital I/O	General-purpose I/O.
17	CAPD	Analog output	Digital low-dropout regulator (LDO) output. Connect a 220nF ceramic capacitor to DGND.
18	DGND	Ground	Digital ground.
19	IOVDD	Digital supply	Digital I/O power supply. See the *IOVDD Power Supply* section for details.
20	CLK	Digital input	ADC clock input.

表 4-1. Pin Functions (続き)

PIN		TYPE	DESCRIPTION
NO.	NAME		
21	$\overline{CS}$	Digital input	Serial interface select, active low.
22	SCLK	Digital input	Serial interface clock.
23	DIN	Digital input	Serial interface data in.
24	DOUT	Digital output	Serial interface data out.
25	$\overline{DRDY}$	Digital output	Data ready, active low.
26	SYNC	Digital input	ADC synchronization, active high.
27	$\overline{RESET}$	Digital input	ADC reset, active low.
28	$\overline{PWDN}$	Digital input	ADC power down, active low.
29	REFN	Analog input	Negative reference input. See the *Voltage Reference Input* section for details.
30	REFP	Analog input	Positive reference input. See the *Voltage Reference Input* section for details.
31	CAPR	Analog internal	Reference bias capacitor. Connect a 100nF ceramic capacitor to AVSS.
32	AVSS	Analog supply	PGA negative supply.
Thermal pad			Connect the thermal pad to AVSS. Thermal vias placed in the printed circuit board (PCB) land are optional to allow placement of bottom side components.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Power-supply voltages	AVDD1 to AVSS	–0.3	5.5	V
	AVSS to AGND	–2.8	0.3	
	AVDD2 to AGND	–0.3	5.5	
	AVDD2 to AVSS	–0.3	5.5	
	IOVDD to DGND	–0.3	3.9	
	IOVDD to DGND (IOVDD connected to CAPD)	–0.3	2.2	
Grounds	AGND to DGND	– 0.3	0.3	V
Analog input voltage	AIN1P, AIN1N, AIN2P, AIN2N, REFP, REFN	AVSS – 0.3	AVDD1 + 0.3	V
Digital input voltage	CLK, DIN, SCLK, $\overline{CS}$, GPIO0, GPIO1, SYNC, $\overline{RESET}$, $\overline{PWDN}$	DGND – 0.3	IOVDD + 0.3	V
Input current	Continuous, any digital or analog pin (2)	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–60	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional – this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Analog input pins AIN1P, AIN1N, AIN2P, AIN2N, REFP and REFN are diode-clamped to AVDD1 and AVSS. Limit the input current to 10mA in the event the analog input voltage exceeds AVDD1 + 0.3V or AVSS – 0.3V. Digital input pins are clamped to IOVDD and DGND. Limit the input current if the digital input voltage exceeds IOVDD + 0.3V or DGND – 0.3V.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged-device model (CDM), per JEDEC JESD22-C101(2)	1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
	Analog power supplies	AVDD1 to AVSS	3		5.25	V
		AVDD1 to AGND	2.375			V
		AVSS to AGND	–2.625		0	
		AVDD2 to AGND	2.375		5.25	
		AVDD2 to AVSS			5.25	
	Digital power supply	IOVDD to DGND	2.7		3.6	V
		IOVDD connected to CAPD	1.65		1.95	
ANALOG INPUTS						
V_{IN}	Differential input voltage	$V_{IN} = V_{AINP} – V_{AINN}$		$\pm V_{REF}$ / Gain		V
	Absolute input voltage	Buffer operation	AVSS + 0.1		AVDD1 – 0.1	V
		PGA operation	AVSS + 1.1		AVDD1 – 0.85	
	Absolute output voltage	Buffer operation	AVSS + 0.1		AVDD1 – 0.1	V
		PGA operation	AVSS + 0.15		AVDD1 – 0.15	
	Calibration range (1)				6%	FSR

5.3 Recommended Operating Conditions (続き)

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
VOLTAGE REFERENCE INPUT						
V_{REF}	$V_{REF} = V_{REFP} – V_{REFN}$		2.4	2.5	2.6	V
V_{REFN}	Negative reference input		AVSS – 0.05			V
V_{REFP}	Positive reference input				AVDD1 + 0.1	V
DIGITAL INPUTS						
V_{INL}	Low-level input voltage				0.2 × IOVDD	V
V_{INH}	High-level input voltage		0.8 × IOVDD			V
f_{CLK}	Clock input frequency		3	4.096	4.15	MHz
TEMPERATURE						
T_A	Ambient temperature	Operational	–50		85	°C
		Specification	–40		85	

(1) Calibration range is the sum of the offset and gain error correction.

5.4 Thermal Information

THERMAL METRIC[1]		ADS1288 RHB (VQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	19.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	10.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	10.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

minimum and maximum specifications over –40°C to +85°C; typical specifications are at 25°C; all specifications are at AVDD1 = 5V, AVDD2 = 2.5V to 5V, AVSS = 0V, IOVDD = 1.8V, V_{REFP} = 2.5V, V_{REFN} = 0V, V_{CM} = 2.5V, PGA gain = 1, R_S = 0Ω, f_{CLK} = 4.096MHz and f_{DATA} = 500SPS (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG INPUTS							
	Input mux on-resistance	Input 1 to input 2 cross connection			60		Ω
PGA OPERATION							
I_B	Input current				45		nA
I_{OS}	Input offset current				±3		nA
	Gain				1, 2, 4, 8, 16, 32, 64		V/V
e_{n-PGA}	Input voltage noise density	PGA Gain = 16			20		nV/√Hz
i_{n-PGA}	Input current noise density	Differential			2.5		pA/√Hz
	Antialias filter frequency				30		kHz
BUFFER OPERATION							
I_B	Input current	V_{IN} = 2.5V			±0.3		µA
DC PERFORMANCE							
e_n	Noise			See Noise Performance section for details			
V_{OS}	Offset error	PGA operation		–350/gain - 10	±30/gain + 5	350/gain + 10	µV
		Buffer operation		–600	±50	600	
		After calibration			±1		
	Offset error drift	PGA operation			0.5/gain		µV/°C
		Buffer operation			1		
	Gain error	PGA operation, gain = 1		–0.05%	±0.02%	0.05%	
		After calibration			2		ppm
		Buffer operation		–0.07%	±0.05%	0.07%	
	Gain match	Relative to PGA gain = 1		–0.2%	±0.06%	0.2%	
	Gain drift	All PGA gains			2		ppm/°C
CMRR	Common-mode rejection ratio	f = 60Hz		104	120		dB
PSRR	Power-supply rejection ratio	AVDD2	At dc	80	95		dB
		AVSS, AVDD1	At dc	85	110		
		IOVDD	At dc	100	120		
AC PERFORMANCE							
e_{n-MOD}	Modulator voltage noise density				100		nV/√Hz
THD	Total harmonic distortion	AVDD1 = 3.3V, AVSS = 0V, f_{IN} = 31.25Hz, V_{IN} = –0.5dBFS	Buffer operation		–124	-117	dB
			PGA gain = 2		–122		
			PGA gain = 4		–124	-116	
			PGA gain = 8		–125		
			PGA gain = 16		–123	-115	
			PGA gain = 32 and 64		–124		
		AVDD1 = 5V, AVSS = 0V, f_{IN} = 31.25Hz, V_{IN} = –0.5dBFS	Buffer operation		–123	-117	
			PGA gain = 1		–121	-115	
			PGA gain = 2		–124		
			PGA gain = 4		–125	-115	
			PGA gain = 8		–122		
			PGA gain = 16		–121	-113	
			PGA gain = 32 and 64		–123		
SFDR	Spurious-free dynamic range	f_{IN} = 31.25Hz, V_{IN} = –0.5dBFS			115		dB
	Crosstalk	f_{IN} = 31.25Hz, V_{IN} = –0.5dBFS			–140		dB

5.5 Electrical Characteristics (続き)

minimum and maximum specifications over –40°C to +85°C; typical specifications are at 25°C; all specifications are at AVDD1 = 5V, AVDD2 = 2.5V to 5V, AVSS = 0V, IOVDD = 1.8V, V_{REFP} = 2.5V, V_{REFN} = 0V, V_{CM} = 2.5V, PGA gain = 1, R_S = 0Ω, f_{CLK} = 4.096MHz and f_{DATA} = 500SPS (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
VOLTAGE REFERENCE INPUT							
	Reference input current				80		µA/V
FIR DIGITAL FILTER							
f_{DATA}	Data rate			125		2000	SPS
	Pass-band ripple			–0.003		0.003	dB
	Pass-band (–0.01dB)				0.375 × f_{DATA}		Hz
	Bandwidth (–3dB)				0.413 × f_{DATA}		Hz
	Stop band				0.5 × f_{DATA}		Hz
	Stop-band attenuation (1)			135			dB
	Group delay	Minimum phase filter, at dc			5 / f_{DATA}		s
		Linear phase filter			31/ f_{DATA}		
	Settling time (latency)	Minimum phase filter			62 / f_{DATA}		s
		Linear phase filter			62 / f_{DATA}		
IIR DIGITAL FILTER							
	High-pass corner frequency			0.1		10	Hz
SAMPLE RATE CONVERTER							
	Frequency compensation range			–244		244	ppm
	Resolution				7.45		ppb
DIGITAL INPUT/OUTPUT							
V_{OH}	High-level output voltage	I_{OH} = 1mA		0.8 × IOVDD			V
V_{OL}	Low-level output voltage	I_{OL} = –1mA				0.2 × IOVDD	V
I_{lkg}	Input leakage			–1		1	µA
POWER SUPPLY							
I_{AVDD1}, I_{AVSS}	AVDD1, AVSS current	AVDD1 = 3.3V	PGA operation		0.85	1.1	mA
			Buffer operation		0.25	0.45	
		AVDD1 = 5V	PGA operation		0.85	1.1	
			Buffer operation		0.25	0.45	
		Power-down mode			1	5	µA
I_{AVDD2}	AVDD2 current	AVDD2 = 2.5V			0.7	0.85	mA
		Power-down mode			1	5	µA
I_{IOVDD}	IOVDD current				0.24	0.4	mA
		Power-down mode			1	10	µA
		Standby mode			200		
	IOVDD additional current	Sample rate converter operation			0.6		mA
P_d	Power dissipation (2)	AVDD1 = 3.3V AVDD2 = 2.5V	PGA operation		5.0	6.5	mW
			Buffer operation		3.0	4.2	
		AVDD1 = 5V AVDD2 = 2.5V	PGA operation		6.4	8.3	
			Buffer operation		3.4	5.1	

(1) Input frequencies at N × 16 kHz ± f_{DATA} / 2 (where *N* = 1, 2, 3, and so on) intermodulate with the chopper clock. At these frequencies stop band attenuation = –90dBFS (typ).
(2) Excluding current consumed by the voltage reference input or by sample rate converter operation. See voltage reference input current and IOVDD supply current for sample rate converter operation.

5.6 Timing Requirements: 1.65V ≤ IOVDD ≤ 1.95V and 2.7V ≤ IOVDD ≤ 3.6V

over operating ambient temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
CLOCK					
$t_{c(CLK)}$	CLK period	241	244.14	332	ns
$t_{w(CLKH)}$	Pulse duration, CLK high	110			ns
$t_{w(CLKL)}$	Pulse duration, CLK low	110			ns
SERIAL INTERFACE					
$t_{w(CSH)}$	Pulse duration, $\overline{CS}$ high	20			ns
$t_{d(CSSC)}$	Delay time, first SCLK rising edge after $\overline{CS}$ falling edge	20			ns
$t_{c(SCLK)}$	SCLK period	120			ns
$t_{w(SCH)}$	Pulse duration, SCLK high	50			ns
$t_{w(SCL)}$	Pulse duration, SCLK low	50			ns
$t_{su(DI)}$	Setup time, DIN valid before SCLK rising edge	10			ns
$t_{h(DI)}$	Hold time, DIN valid after SCLK rising edge	10			ns
$t_{su(SRC-W)}$	Setup time, SRC[1:0] register write before $\overline{DRDY}$ falling edge	256			$1 / f_{(CLK)}$
SYNC					
$t_{w(SYNL)}$	Pulse duration, SYNC low	2			$1 / f_{(CLK)}$
$t_{w(SYNH)}$	Pulse duration, SYNC high	2			$1 / f_{(CLK)}$
$t_{su(SYNCLK)}$	Setup time, SYNC high before CLK rising edge	10			ns
$t_{h(SYNCLK)}$	Hold time, SYNC high after CLK rising edge	10			ns
$\overline{RESET}$					
$t_{w(RSTL)}$	Pulse duration, $\overline{RESET}$ low	2			$1 / f_{(CLK)}$
$t_{su(RSTCLK)}$	Setup time, $\overline{RESET}$ high before CLK rising edge	10			ns
$t_{h(RSTCLK)}$	Hold time, $\overline{RESET}$ high after CLK rising edge	10			ns

5.7 Switching Characteristics: 1.65V ≤ IOVDD ≤ 1.95V and 2.7V ≤ IOVDD ≤ 3.6V

over operating ambient temperature range and C_{LOAD} = 20pF (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
SERIAL INTERFACE					
$t_{w(DRH)}$	Pulse duration, $\overline{DRDY}$ high			8	$1 / f_{(CLK)}$
$t_{p(CSDO)}$	Propagation delay time, $\overline{CS}$ falling edge to DOUT driven valid			50	ns
$t_{p(SCDO)}$	Propagation delay time, SCLK falling edge to new DOUT valid			50	ns
$t_{h(SCDO)}$	Propagation delay time, SCLK falling edge to DOUT invalid	5			ns
SYNC					
$t_{p(SYNDR)}$	Propagation delay time, SYNC rising edge to valid data $\overline{DRDY}$ falling edge		$62.98145 / f_{DATA} + 930 / f_{CLK}$		s
$\overline{RESET}$					
$t_{p(RSTDR)}$	Propagation delay time, $\overline{RESET}$ rising edge to $\overline{DRDY}$ falling edge		516,874		$1/ f_{CLK}$
$\overline{PWDN}$					
$t_{p(PDDR)}$	Propagation delay time, $\overline{PWDN}$ rising edge to $\overline{DRDY}$ falling edge		$62.98145 / f_{DATA} + 946 / f_{(CLK)}$		s
POWER UP					
$t_{p(SUPDR)}$	Propagation delay time, power supply and CLK applied to first $\overline{DRDY}$ pulse		650,000		$1 / f_{CLK}$

5.8 Timing Diagrams

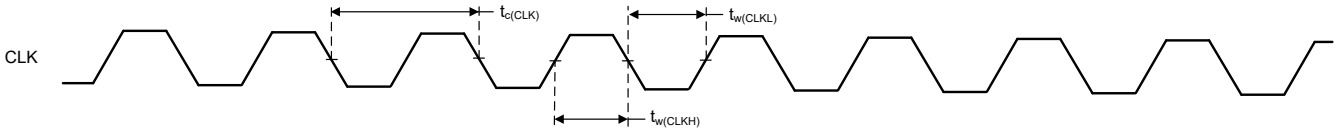


図 5-1. Clock Timing Requirements

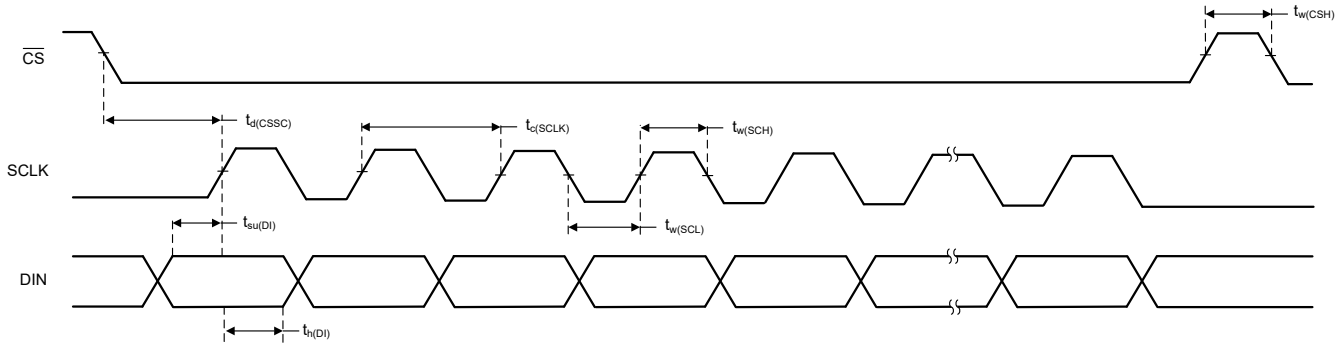


図 5-2. Serial Interface Timing Requirements

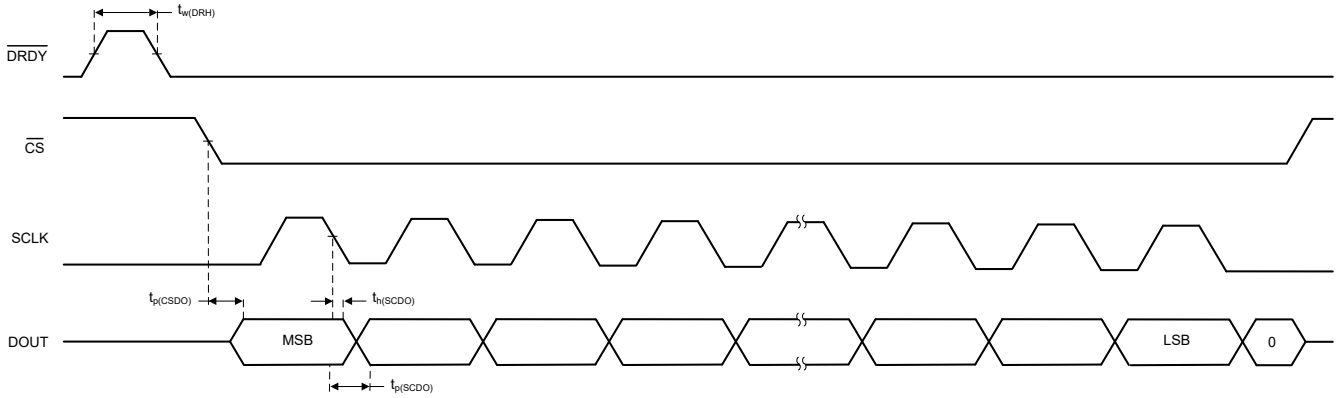


図 5-3. Serial Interface Switching Characteristics

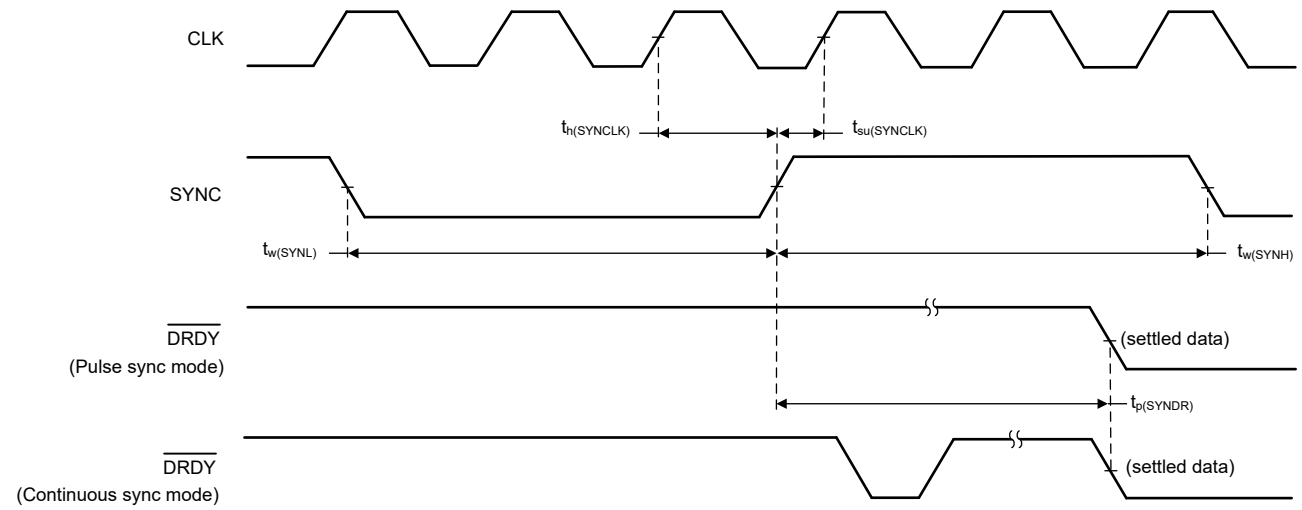


図 5-4. SYNC Timing Requirements and Switching Characteristics

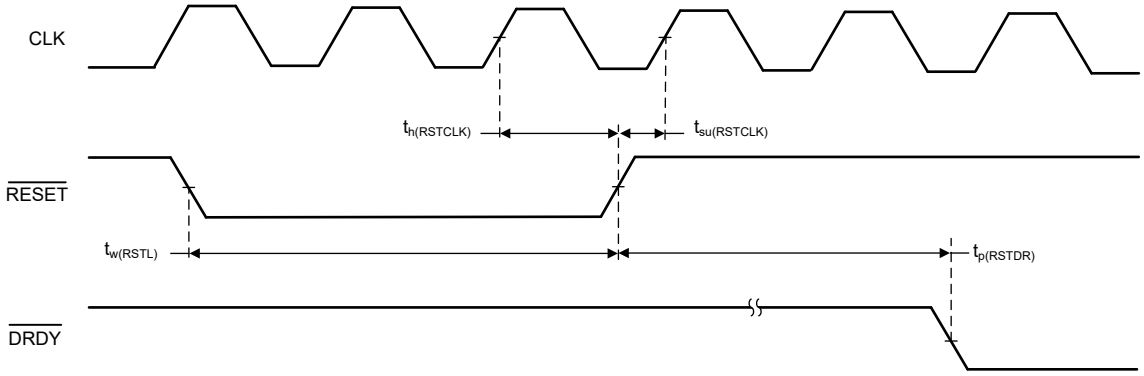


図 5-5. RESET Timing Requirements and Switching Characteristics

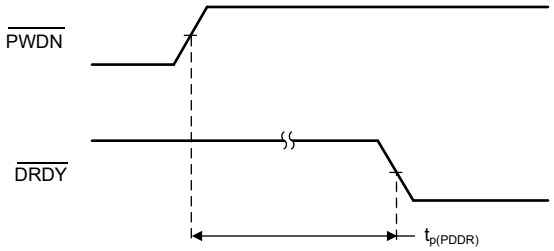


図 5-6. PWDN Switching Characteristics

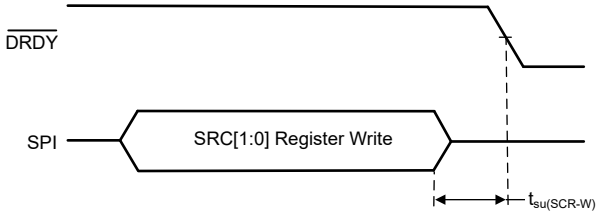


図 5-7. Sample Rate Converter Register-Write Timing Requirements

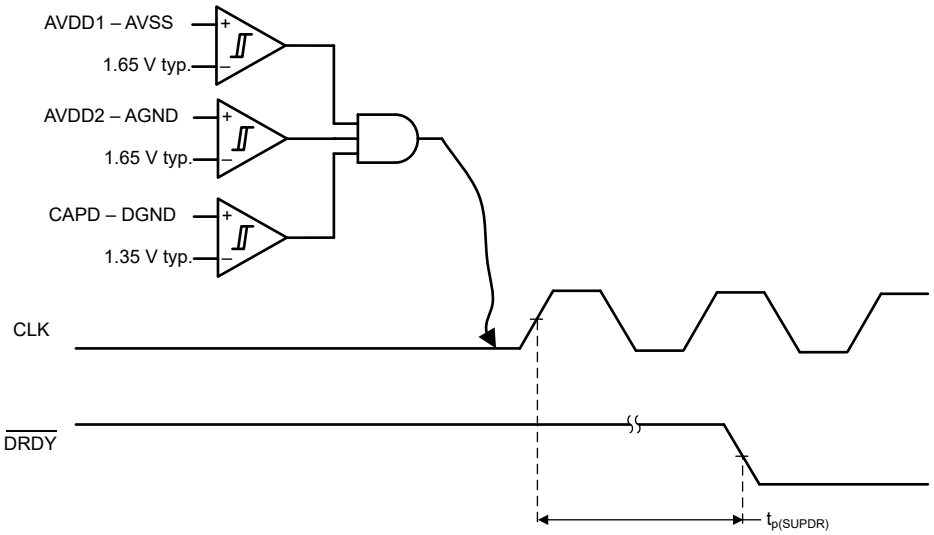
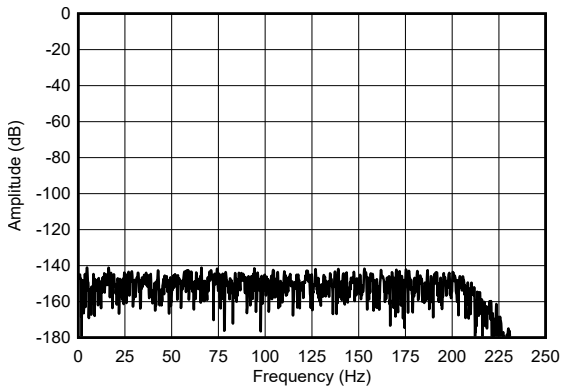


図 5-8. Power-Up Switching Characteristics

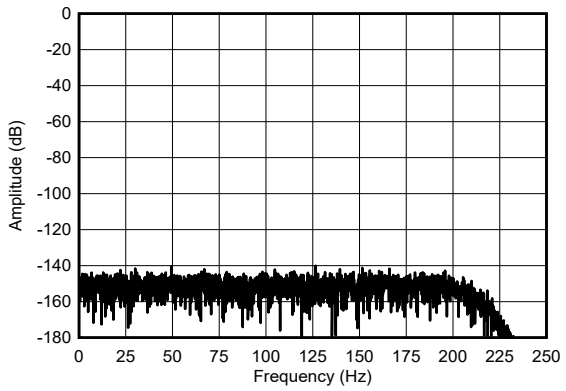
5.9 Typical Characteristics

at T_A = 25°C, AVDD1 = 5V, AVSS = 0V, AVDD2 = 2.5V, IOVDD = 1.8V, f_{CLK} = 4.096MHz, V_{REFP} = 2.5V, V_{REFN} = 0V, PGA gain = 1, R_S = 0Ω, V_{CM} = 2.5V, and f_{DATA} = 500SPS (unless otherwise noted)



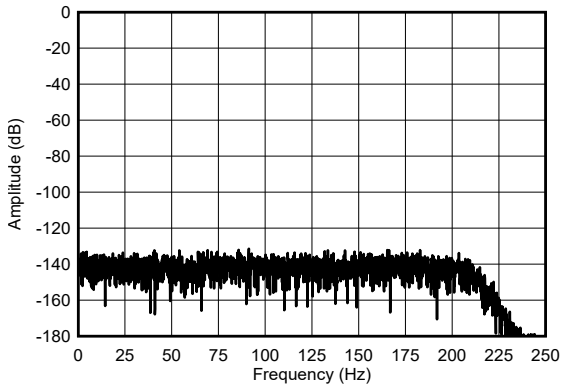
Buffer mode

図 5-9. Shorted Input FFT



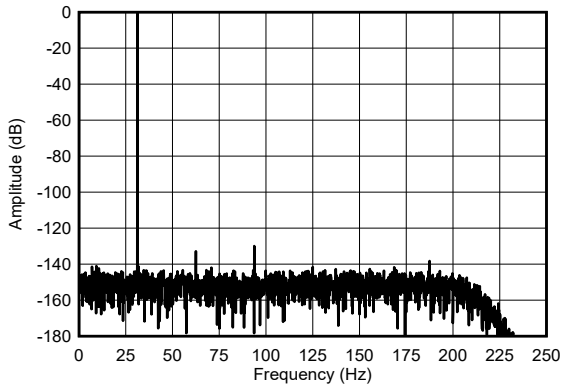
PGA gain = 2

図 5-10. Shorted Input FFT



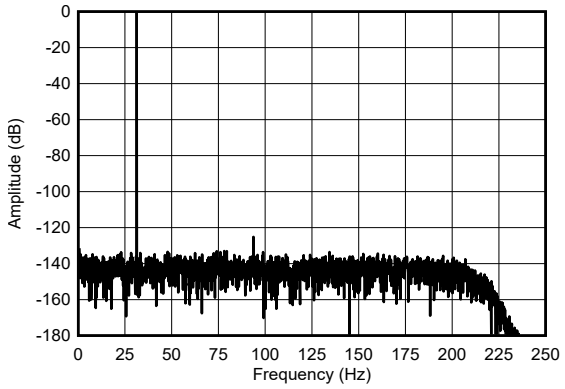
PGA gain = 16

図 5-11. Shorted Input FFT



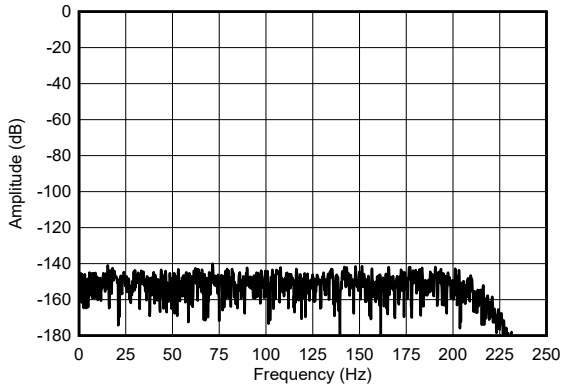
PGA gain = 2

図 5-12. Full-Scale Input FFT



PGA gain = 16

図 5-13. Full-Scale Input FFT



AIN2: 31.25Hz, –0.5dBFS signal, AIN1: input shorted measured channel

図 5-14. Channel Crosstalk

5.9 Typical Characteristics (continued)

at T_A = 25°C, AVDD1 = 5V, AVSS = 0V, AVDD2 = 2.5V, IOVDD = 1.8V, f_{CLK} = 4.096MHz, V_{REFP} = 2.5V, V_{REFN} = 0V, PGA gain = 1, R_S = 0Ω, V_{CM} = 2.5V, and f_{DATA} = 500SPS (unless otherwise noted)

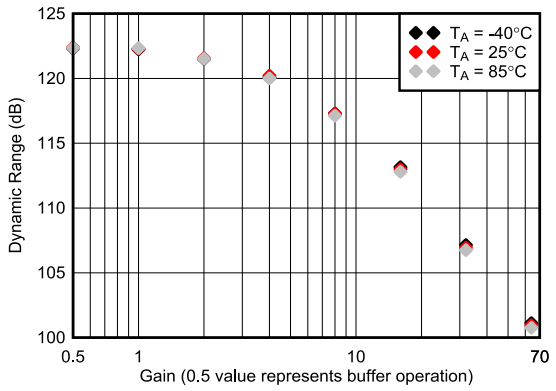


図 5-15. Dynamic Range vs PGA Gain

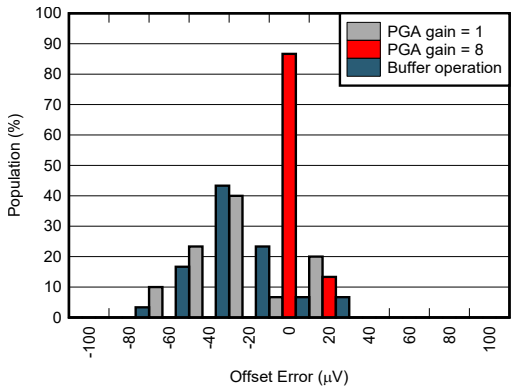


図 5-16. Offset Error Distribution

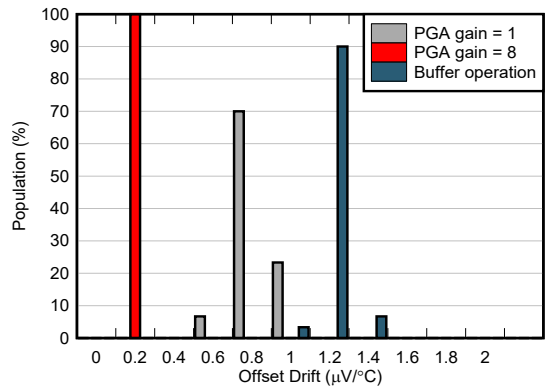


図 5-17. Offset Drift Distribution

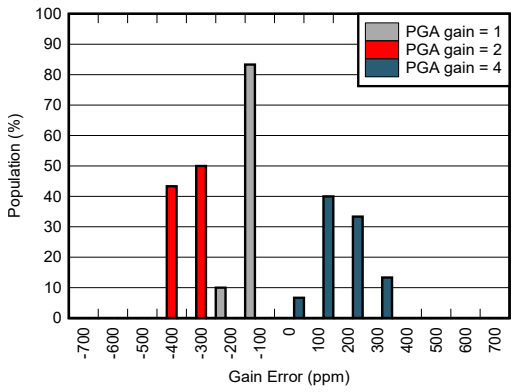


図 5-18. Gain Error Distribution

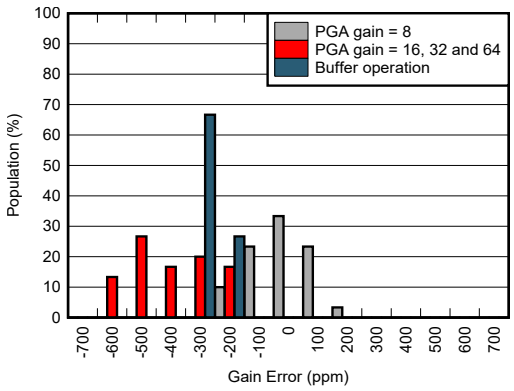


図 5-19. Gain Error Distribution

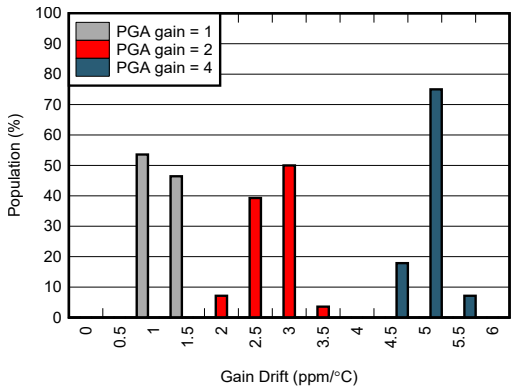
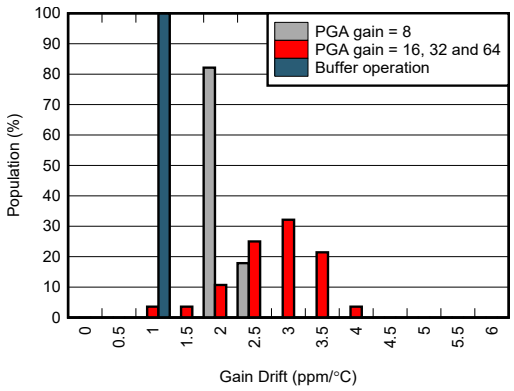


図 5-20. Gain Drift Distribution

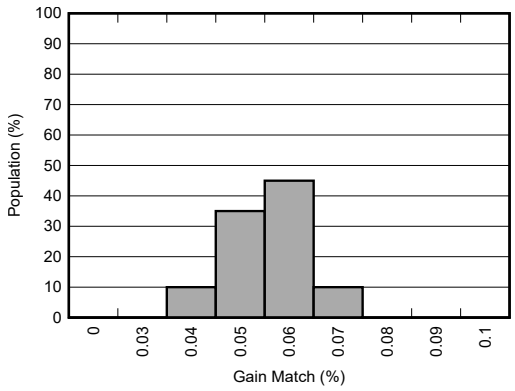
5.9 Typical Characteristics (continued)

at T_A = 25°C, AVDD1 = 5V, AVSS = 0V, AVDD2 = 2.5V, IOVDD = 1.8V, f_{CLK} = 4.096MHz, V_{REFP} = 2.5V, V_{REFN} = 0V, PGA gain = 1, R_S = 0Ω, V_{CM} = 2.5V, and f_{DATA} = 500SPS (unless otherwise noted)



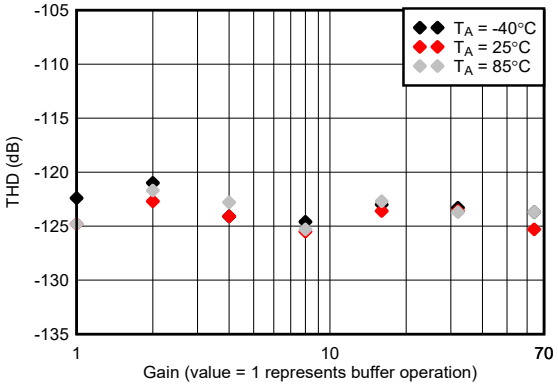
30 units

図 5-21. Gain Drift Distribution



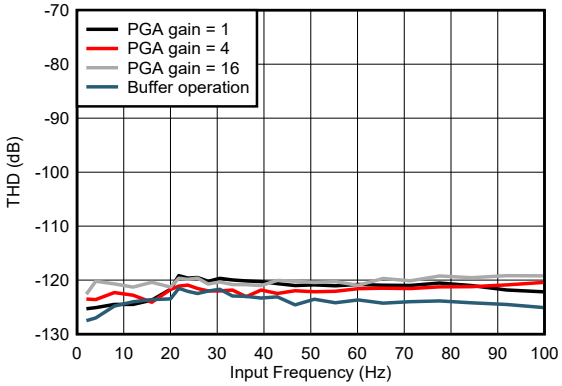
30 units

図 5-22. Gain Match Distribution



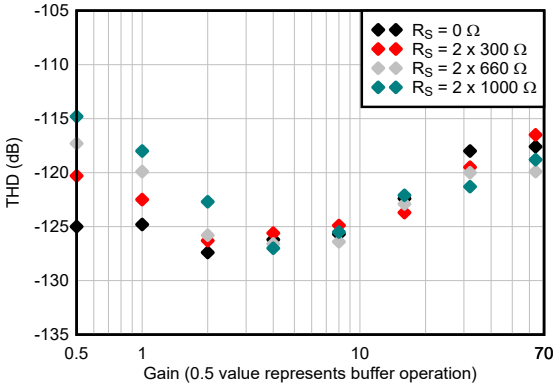
AVDD1 = 3.3V, f_{IN} = 31.25Hz, V_{IN} = –0.5dBFS

図 5-23. THD vs PGA Gain



f_{IN} = 31.25Hz, V_{IN} = –0.5dBFS

図 5-24. THD vs Input Frequency



f_{IN} = 31.25Hz, V_{IN} = –0.5dBFS

図 5-25. THD vs Source Impedance

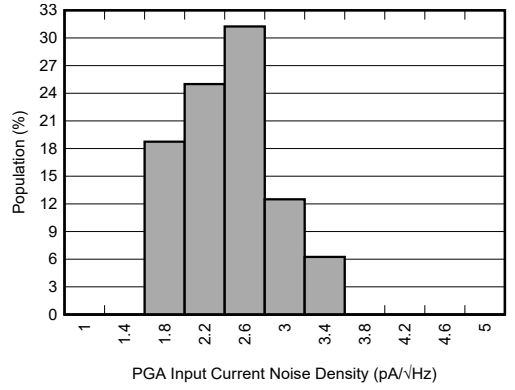


図 5-26. PGA Input Current Noise Distribution

5.9 Typical Characteristics (continued)

at T_A = 25°C, AVDD1 = 5V, AVSS = 0V, AVDD2 = 2.5V, IOVDD = 1.8V, f_{CLK} = 4.096MHz, V_{REFP} = 2.5V, V_{REFN} = 0V, PGA gain = 1, R_S = 0Ω, V_{CM} = 2.5V, and f_{DATA} = 500SPS (unless otherwise noted)

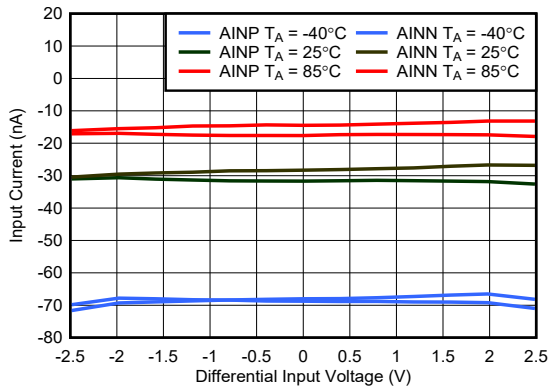


図 5-27. PGA Input Current vs Input Voltage

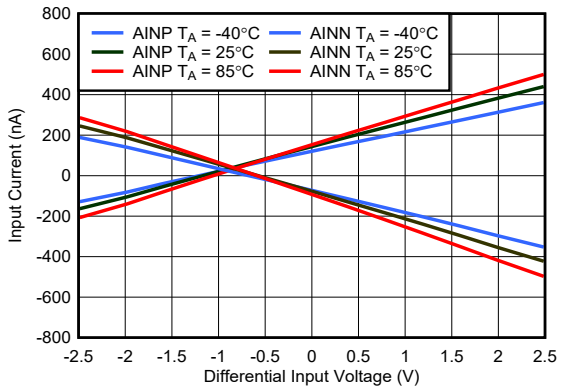


図 5-28. Buffer Input Current vs Input Voltage

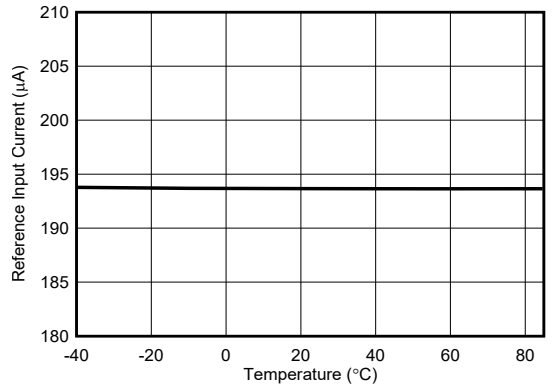


図 5-29. Reference Input Current vs Temperature

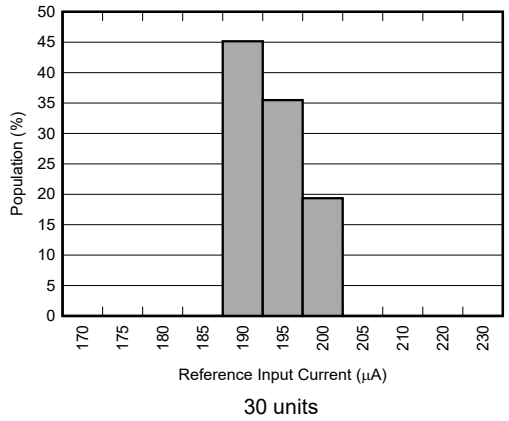


図 5-30. Reference Input Current Distribution

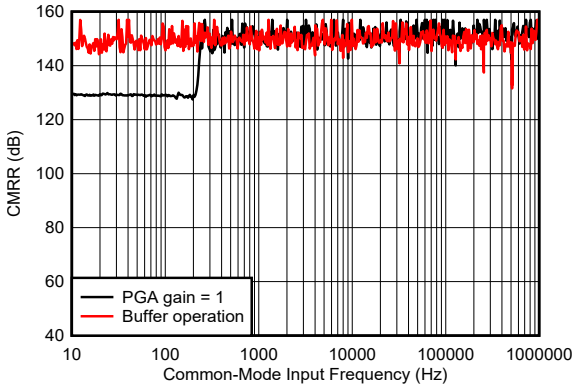


図 5-31. CMRR vs Common-Mode Input Frequency

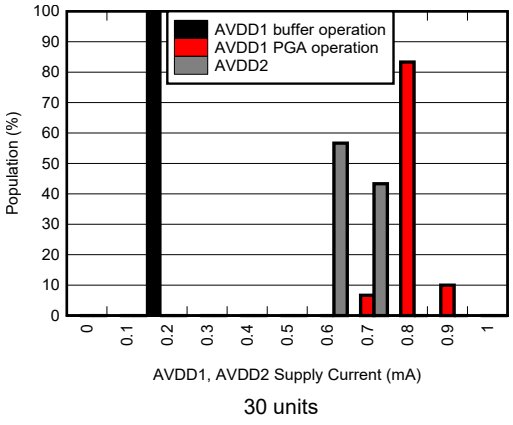


図 5-32. Power-Supply Current Distribution

5.9 Typical Characteristics (continued)

at T_A = 25°C, AVDD1 = 5V, AVSS = 0V, AVDD2 = 2.5V, IOVDD = 1.8V, f_{CLK} = 4.096MHz, V_{REFP} = 2.5V, V_{REFN} = 0V, PGA gain = 1, R_S = 0Ω, V_{CM} = 2.5V, and f_{DATA} = 500SPS (unless otherwise noted)

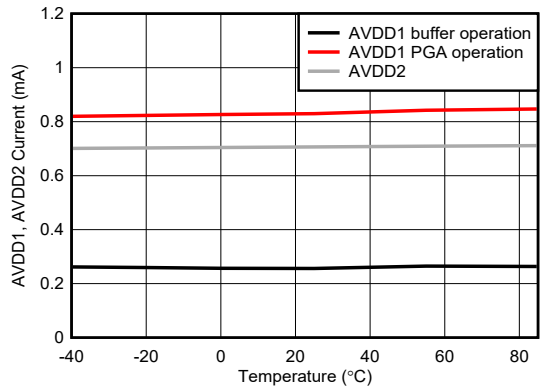


図 5-33. Power-Supply Current vs Temperature

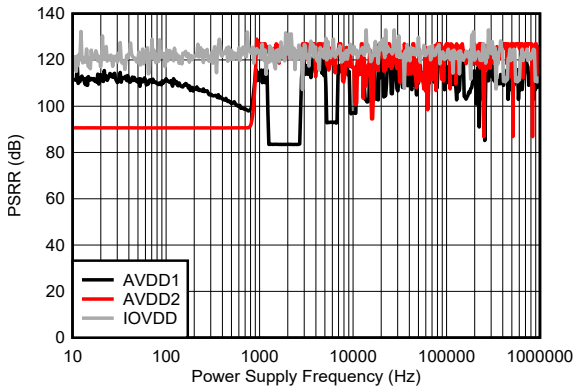


図 5-34. PSRR vs Power-Supply Frequency

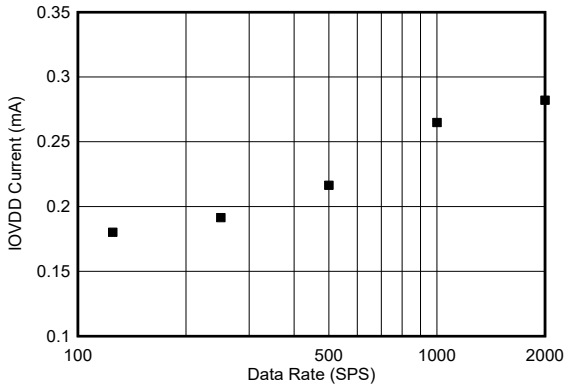


図 5-35. IOVDD Current vs Data Rate

6 Parameter Measurement Information

6.1 Noise Performance

The ADS1288 is a low-power, low-noise, delta-sigma ADC operating on the principle of oversampling. Oversampling averages the high-frequency data of the modulator to produce the final output data. Increasing the oversampling ratio lowers the data rate, the corresponding signal bandwidth, and total noise by averaging more samples from the modulator to yield one conversion result.

The gain of the PGA reduces noise when the noise value is referred to the input. With increased gain, dynamic range performance decreases because the ratio of the input voltage range to the input-referred voltage noise also decreases.

Dynamic range and input noise are equivalent parameters that describe the available resolution of the ADC. 式 1 derives dynamic range from the input-referred noise data:

$$\text{Dynamic Range (dB)} = 20 \times \log \left[\frac{1.768\ \text{V}}{\text{Gain} \times e_n} \right] \quad (1)$$

where:

- e_n = Input-referred voltage noise (RMS)

表 6-1 shows dynamic range and input-referred noise performance, tested with input source resistance (R_S) = 0Ω. Noise data are at T_A = 25°C and are representative of typical ADC performance. The data are the standard deviation of 4096 consecutive ADC conversion results with the ADC inputs shorted, measured over the 0.413 × f_{DATA} bandwidth. Because of the statistical nature of noise, repeated measurements can yield varying noise performance results.

表 6-1. Noise Performance (AVDD1 = 3.3V or 5V, R_S = 0Ω)

GAIN	MODE	DYNAMIC RANGE (dB)					e_n, INPUT-REFERRED NOISE (μV_{RMS})				
		f_{DATA} (SPS)					f_{DATA} (SPS)				
		125	250	500	1000	2000	125	250	500	1000	2000
1	Buffer	128	125	122	119	116	0.70	0.99	1.4	2.0	2.8
1(1)	PGA	128	125	122	119	116	0.70	0.99	1.4	2.0	2.8
2	PGA	127	124	121	118	115	0.39	0.56	0.79	1.1	1.6
4	PGA	126	123	120	117	114	0.23	0.32	0.45	0.63	0.89
8	PGA	123	120	117	114	111	0.16	0.22	0.31	0.44	0.62
16	PGA	118	115	112	109	106	0.14	0.20	0.28	0.39	0.55
32	PGA	112	109	106	103	100	0.14	0.20	0.28	0.39	0.55
64	PGA	106	103	100	97	94	0.14	0.20	0.28	0.39	0.55

(1) PGA gain = 1 dynamic range performance specified at AVDD1 = 5V.

7 Detailed Description

7.1 Overview

The ADS1288 is a high-resolution, low-power analog-to-digital converter (ADC) designed for applications in energy exploration, geology, and seismic monitoring where low-power consumption and high resolution are required. The output data resolution is 32 bits spanning data rates from 125SPS to 2000SPS. The programmable gain amplifier (PGA) expands the system dynamic range with seven input ranges of ±2.5V_{PP} to ±0.039V_{PP}.

As illustrated in the *Functional Block Diagram*, the ADC consists of the following sections: input multiplexer (MUX), programmable gain amplifier (PGA), unity-gain buffer, delta-sigma (ΔΣ) modulator, sample rate converter, infinite impulse response (IIR) high-pass filter (HPF), finite impulse response (FIR) low-pass filter (LPF), and an SPI-compatible serial interface used for both device configuration and conversion data readback.

The input multiplexer selects between inputs 1 and 2, and internal options designed for self-test, including an input-short connection to test device offset and noise performance.

The input multiplexer is followed by a low-noise PGA. The range of PGA gains is 1 to 16, with gains 32 and 64 implemented as digital gains. The PGA is chopper-stabilized to reduce 1/f noise and input offset voltage. The PGA output connects to a buffer which drives the modulator. An external 10nF capacitor, connected to PGA output pins CAPP and CAPN, provides an antialias filter for the input signal.

Disable the PGA to lower device power consumption by operating the ADC with the unity-gain buffer. External 47nF capacitors connected to each buffer output filter the modulator sampling pulses.

The ΔΣ modulator measures the differential input signal (V_{IN}) at the PGA output against the differential reference voltage (V_{REF} = 2.5V). Modulator data are processed by the digital filter to provide the final conversion result. The digital filter consists of a sinc filter followed by a programmable phase, FIR low-pass filter, and an IIR high-pass filter. The high-pass filter removes dc and low-frequency components from the data.

The sample rate converter (SRC) compensates clock signal error by resampling the output data to correct the output data rate. Write the desired compensation value to the SRC register for data rate correction with up to 7ppb accuracy.

User-programmable gain and offset calibration registers correct offset and gain errors.

The SYNC pin synchronizes the ADC. Synchronization has two modes of operation: pulse synchronization and continuous synchronization. The $\overline{\text{RESET}}$ pin resets the ADC, including user-configuration settings. The pins are noise-resistant, Schmitt-trigger inputs to increase reliability in high-noise environments.

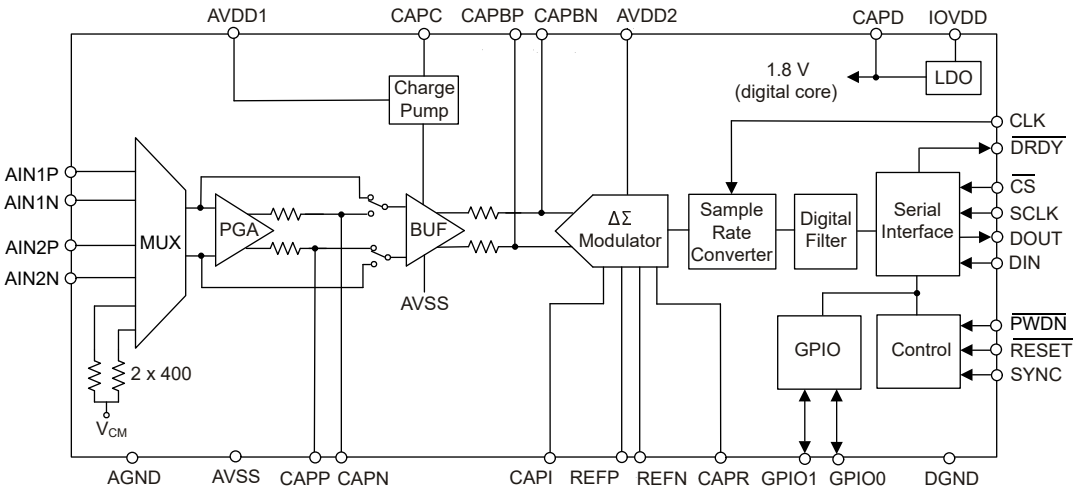
The $\overline{\text{PWDN}}$ pin powers down the ADC when not in use. The software power-down mode (STANDBY) is available through the serial interface

The 4-wire, SPI-compatible, serial interface reads conversion data and reads or writes device register data.

Two general-purpose digital I/Os are available to control external switches for diagnostic tests.

Power for the PGA and buffer is supplied by pins AVDD1 and AVSS. A charge pump voltage regulator increases the buffer supply voltage to increase input voltage range. Power for the modulator is supplied by the AVDD2 pin. The digital I/O voltage pin (IOVDD) powers the digital logic core through a 1.8V low-dropout regulator (LDO).

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Analog Input

図 7-1 shows the analog input circuit and input multiplexer.

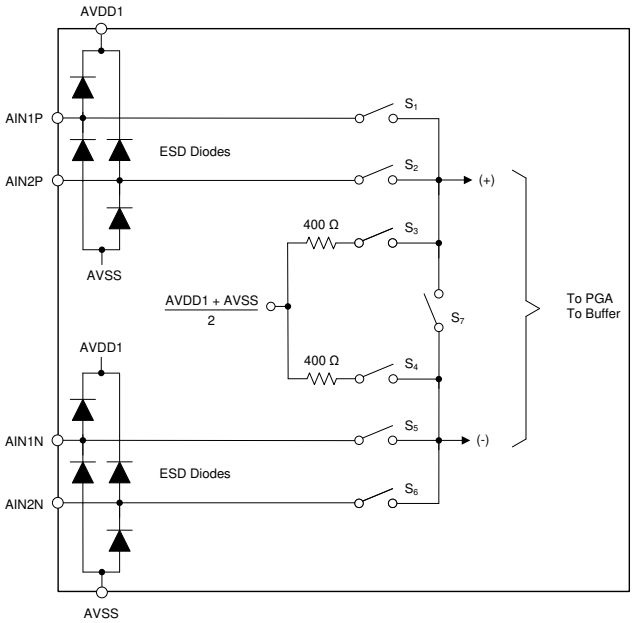


図 7-1. Analog Input and Multiplexer

Electrostatic discharge (ESD) diodes are incorporated to protect the ADC inputs from ESD events that occur during device manufacturing and printed circuit board (PCB) assembly process when assembled in an ESD-controlled environment. For system-level protection, consider using external ESD protection devices to protect the input that are exposed to ESD events.

If the inputs are driven below AVSS – 0.3V, or above AVDD1 + 0.3V, the protection diodes can conduct. If these conditions are possible, use external clamp diodes, series resistors, or both to limit input current to the specified maximum value. Overdriving an unused input channel can affect the conversion results of the active input channel. Clamp the overdriven voltage with Schottky diodes to prevent channel crosstalk.

The ADC incorporates two differential input channels. The multiplexer selects between the two differential inputs for measurement. A test mode to measure noise and offset is also provided by the multiplexer. The shorted input test configuration is available with or without the 400Ω resistors to simulate the thermal noise generated by an 800Ω geophone. 表 7-1 summarizes the multiplexer configurations.

表 7-1. Input Multiplexer Modes

MUX[2:0] BITS	SWITCHES	DESCRIPTION
000	S_1, S_5	Input AIN1P, AIN1N connection.
001	S_2, S_6	Input AIN2P, AIN2N connection.
010	S_3, S_4	400Ω input-short test mode for offset and noise test.
011	S_1, S_5,S_2, S_6	Cross-connection test mode. Inputs AIN1P, AIN2P *and* AIN2P, AIN2N are connected.
100	—	Reserved
101	S_3,S_4,S_7	0Ω input-short test mode for offset and noise test.

To test geophone THD performance, apply a test signal to the test channel through series resistors. The series resistors are typically half the value of the geophone impedance. Select the multiplexer for the cross-connection test mode (MUX[2:0] = 011b). In cross-connection mode, the test signal is cross-fed to the geophone input.

Geophone THD test performance can be affected by the nonlinear on-resistance of the multiplexer (R_{SW}). 図 7-2 shows a model of the input multiplexer resistance for the geophone THD test. 図 7-3 shows THD performance versus a test resistor (R_{LOAD}) used to simulate geophone resistance. Small amplitude test signals (such as, V_{IN} = 0.221V), shows less THD performance degradation for geophone resistance < 500Ω.

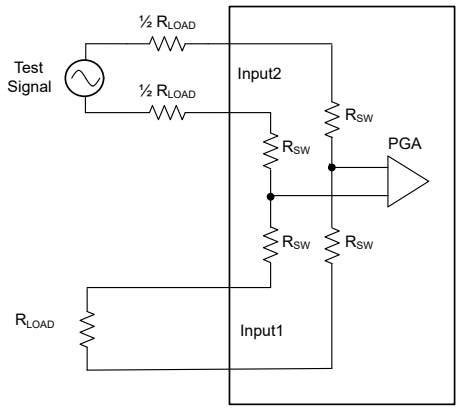


図 7-2. THD versus R_{LOAD} Test Circuit

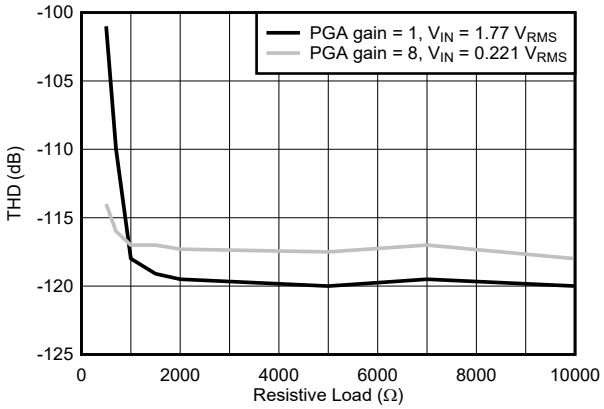


図 7-3. THD Performance vs R_{LOAD}

7.3.2 PGA and Buffer

図 7-4 shows the simplified PGA and buffer block diagram.

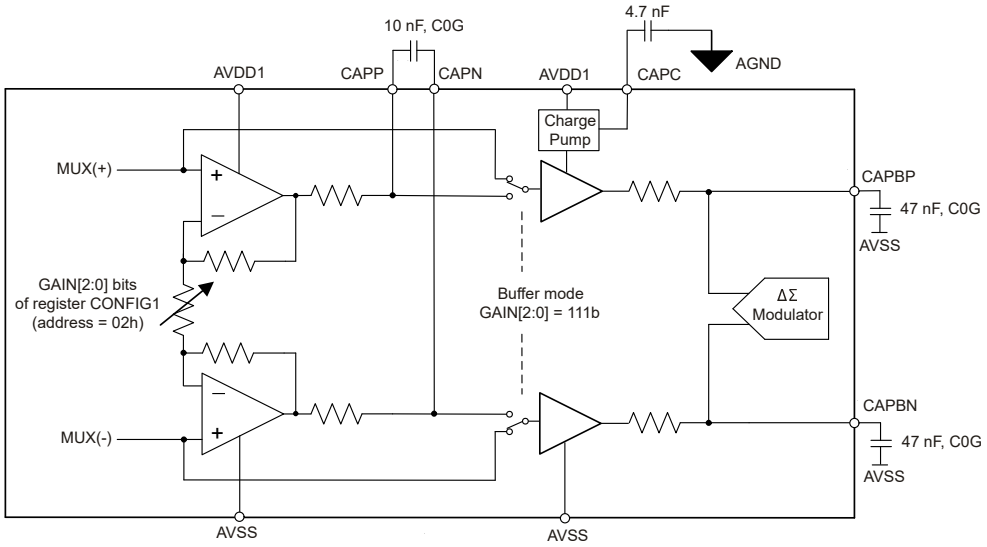


図 7-4. PGA and Buffer Block Diagram

The device can be operated with the PGA or the unity-gain buffer. Buffer operation disables the PGA, reducing device power consumption. Because of the limited input headroom for PGA gain = 1 when operating AVDD1 at 3.3V, the buffer must be used in this condition.

7.3.2.1 Programmable Gain Amplifier (PGA)

The PGA is a low-noise, chopper-stabilized differential amplifier that extends the ADC dynamic range performance. The PGA provides analog gains from 1 to 16, with gains of 32 and 64 provided by digital scaling. The PGA output signal is routed to the CAPP and CAPN pins through 270Ω resistors. Connect an external 10nF, C0G-dielectric capacitor across these pins. An antialias filter is formed by these components to attenuate the signal level at the modulator aliasing frequency (f_{MOD}).

As illustrated in 図 7-4, the buffer is used between the PGA and the modulator. Connect two 47nF, C0G-dielectric capacitors from each buffer output to AVSS (CAPBP and CAPBN). A voltage charge pump increases the buffer input voltage headroom. Connect an external 4.7nF capacitor between CAPC and AGND for charge pump operation.

The PGA gain is programmed by the GAIN[2:0] bits of the CONFIG1 register. 表 7-2 shows the PGA gain settings and buffer selection.

表 7-2. PGA Gains

GAIN[2:0] REGISTER BITS	PGA GAIN	INPUT SIGNAL RANGE (V_{PP})
000	1	±2.5
001	2	±1.25
010	4	±0.625
011	8	±0.3125
100	16	±0.15625
101	32	±0.078125
110	64	±0.0390625
111	Buffer mode, gain = 1	±2.5

Observe the PGA input and output voltage headroom specification. 図 7-5 shows the input and output voltage headroom when operating with AVDD1 = 5V, an input common-mode voltage (V_{CM}) = 2.5V, a differential input voltage = ±2.5V_{PP}, and at gain = 1. The absolute minimum and maximum PGA input voltages (1.25V and 3.75V) are ±1/2 of the differential signal voltage plus the common-mode voltage. The PGA provides 0.15V input voltage margin at the negative peak and 0.4V input voltage margin at the positive peak. The PGA provides 1.1V output voltage margin at the positive and negative peaks.

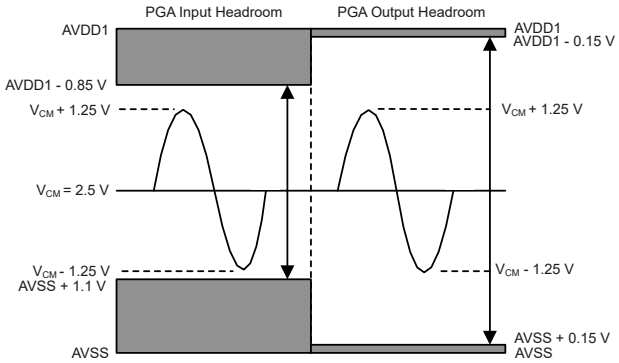


図 7-5. PGA Headroom (AVDD1 = 5V, Gain = 1)

When operating with AVDD1 = 3.3V, the PGA cannot support ±2.5V_{PP} input signals. Use the buffer for ±2.5V_{PP} input signals. For ±1.25V_{PP} input signals (PGA gain = 2), the input headroom is increased by increasing the common-mode voltage by 0.1V to AVSS + 1.75V. 図 7-6 shows the input and output operating headroom for AVDD1 = 3.3V, V_{CM} = 1.75V, input signal = ±1.25V_{PP}, and gain = 2.

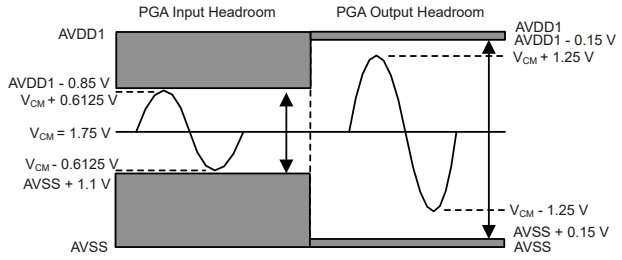


図 7-6. PGA Headroom (AVDD1 = 3.3V, Gain = 2)

7.3.2.2 Buffer Operation (PGA Bypass)

The ADC provides a buffer option, bypassing the PGA. The PGA is powered-down in buffer mode. Use the buffer for ±2.5V_{PP} input signals when operating AVDD1 at 3.3V. Buffer operation is enabled by setting the GAIN[2:0] bits = 111b of the CONFIG1 register.

図 7-7 shows the buffer voltage headroom with AVDD1 = 3.3V, V_{CM} = 1.65V, and the input signal = ±2.5V_{PP}. The buffer has sufficient voltage headroom for ±2.5V_{PP} input signals when operating with AVDD1 = 3.3V.

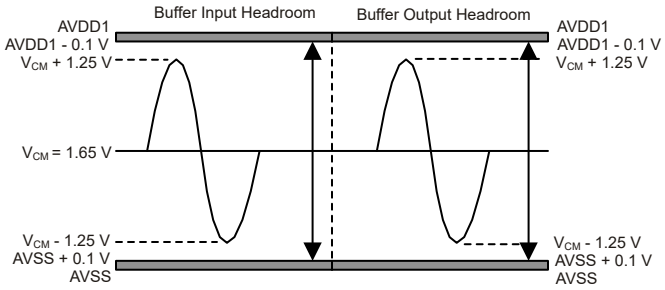


図 7-7. Buffer Headroom (3.3V Operation Shown)

Regardless of PGA or buffer operation, connect two 47nF, C0G-dielectric capacitors from each buffer output to AVSS (CAPBP and CAPBN). The voltage charge pump increases the buffer input operating headroom. Connect an external 4.7nF capacitor between CAPC and AGND for the charge pump operation.

7.3.3 Voltage Reference Input

The ADC requires a reference voltage for operation. The reference voltage input is differential, defined as the voltage between the REFP and REFN pins: $V_{REF} = V_{REFP} – V_{REFN}$. Because of the differential input, route the VREFN trace to the voltage reference ground terminal to avoid ground noise pickup. Use a precision 2.5V voltage reference with low noise, optimally less than 2μV_{RMS} over the measurement bandwidth.

図 7-8 shows the simplified reference input circuit. Similar to the analog inputs, the reference inputs are protected by ESD diodes. If the reference inputs are driven below AVSS – 0.3V or above AVDD1 + 0.3V, the protection diodes can conduct. If these conditions are possible, use external clamp diodes, series resistors, or both to limit the reference input current to the specified value.

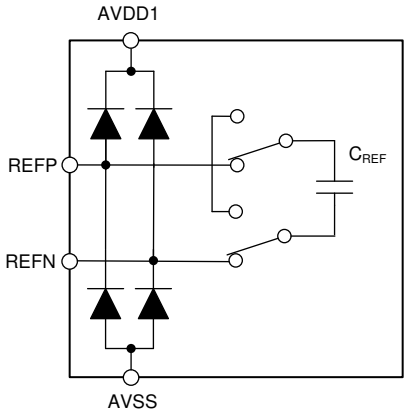


図 7-8. Simplified Voltage Reference Input Circuit

The ADC samples the reference voltage by an internal capacitor (C_{REF}) and then discharges the capacitor at the modulator sampling frequency (f_{MOD}). The sampling operation results in transient current flow into the reference inputs. The transient current is filtered by a 0.1µF ceramic capacitor placed directly at the reference pins with a larger 10µF to 47µF capacitor at the voltage reference output. In applications where the voltage reference drives multiple ADCs, use 0.1µF capacitors at each ADC.

The external capacitors filter the current transients, resulting in 80µA/V average reference current. With V_{REF} = 2.5V, the reference input current is 80µA / V × 2.5V = 200µA.

7.3.4 IOVDD Power Supply

The IOVDD digital supply operates in two voltage ranges: 1.65V to 1.95V and 2.7V to 3.6V. If operating IOVDD in the 1.65V to 1.95V range, connect IOVDD directly to the CAPD pin. 図 7-9 shows the required connection if IOVDD is operating in the 1.65V to 1.95V range. Otherwise, if operating IOVDD in the 2.7V to 3.6V range, do not connect these pins together.

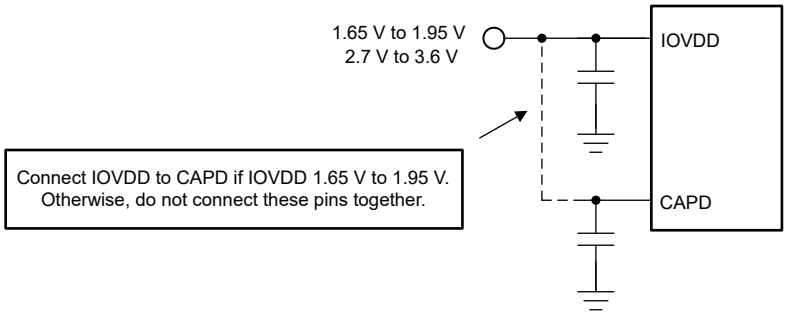


図 7-9. IOVDD Power-Supply Connection

7.3.5 Modulator

The modulator is a multibit delta-sigma architecture featuring low power consumption with very low levels of spurious tones in the output. The modulator shapes the quantization noise of the internal quantizer to an out-of-band frequency range where the noise is removed by the digital filter. Noise remaining within the pass-band region is thermal, with the characteristic of constant noise density (white noise). The total noise in the ADC output is determined by the digital filter OSR.

7.3.5.1 Modulator Overdrive

The modulator is an inherently stable design and, therefore exhibits predictable recovery from input overdrive. If the modulator is overdriven at the peaks of the input signal, the filter output data can clip, but not necessarily so depending on the duration of the signal overdrive resulting from data averaging of the digital filter. If the

modulator is heavily overdriven, then the likelihood of clipped conversion data in the output increases. Be aware the group delay of the digital filter delays the time of an input overdrive event to the output data.

7.3.6 Digital Filter

The digital filter decimates and filters the modulator data to provide high-resolution output data. By adjusting the amount of filtering though the OSR, trade-offs can be made between output data noise and bandwidth. Increasing the OSR reduces output data noise while decreasing the signal bandwidth.

As shown in 図 7-10, the sample rate converter (SRC) receives data from the modulator prior to the digital filter block. See the *Sample Rate Converter* section for details.

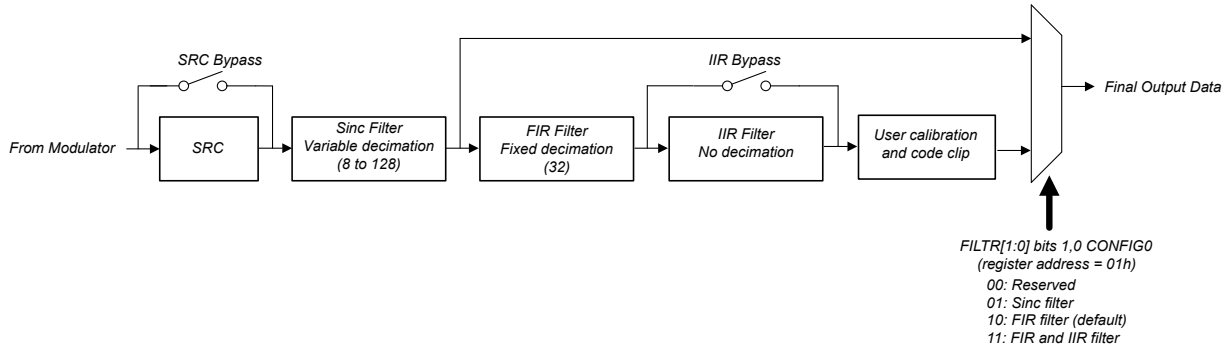


図 7-10. Digital Filter Block Diagram

The digital filter consists of three sections: a variable-decimation sinc filter; a variable-coefficient, fixed-decimation FIR filter; and a programmable high-pass filter (IIR). The desired filter sections are selected by the FILTER[1:0] bits of the CONFIG0 register. The sinc filter provides partially filtered data, bypassing the FIR and HPF filters and the user calibration stage. For fully filtered data, select the FIR filter option. The IIR filter stage removes dc and low-frequency data. The FIR and the combined FIR + IIR filter are routed to the user calibration block and output code clipping block. See the *Offset and Gain Calibration* section for details of user calibration.

7.3.6.1 Sinc Filter Section

The first section of the digital filter is a variable-decimation, fifth-order sinc filter (sinx/x). Modulator data are passed through the sample rate converter to the sinc filter at the nominal rate of $f_{MOD} = f_{CLK} / 4 = 1.024MHz$. The sinc filter partially filters the data for the FIR filter that produces the final frequency response. The sinc filter output data are intended to be used with post-processing filters to shape the final frequency response.

表 7-3 shows the decimation ratio and the resulting output data rate of the sinc filter. The sinc filter data rate is programmed by the DR[2:0] bits of the CONFIG0 register.

表 7-3. Sinc Filter Data Rates

DR[2:0] BITS	SINC DECIMATION RATIO (N)	DATA RATE (SPS)
000	256	4,000
001	128	8,000
010	64	16,000
011	32	32,000
100	16	64,000

式 2 shows the Z-domain transfer function of the sinc filter.

$$H(Z) = \left[\frac{1 - Z^{-N}}{N(1 - Z^{-1})} \right]^{5} \quad (2)$$

where:

- N = Decimation ratio of 表 7-3

式 3 shows the frequency domain transfer function of the sinc filter.

$$|H(f)| = \left| \frac{\sin\left(\frac{\pi N \times f}{f_{MOD}}\right)}{N \sin\left(\frac{\pi \times f}{f_{MOD}}\right)} \right|^5 \quad (3)$$

where:

- N = Decimation ratio shown in 表 7-3
- f = Input signal frequency
- f_{MOD} = Modulator sampling frequency = f_{CLK} / 4 (sample rate converter disabled)

The sinc filter frequency response has notches (or zeros) occurring at the output data rate and multiples thereof. At these frequencies, the filter has zero gain. 図 7-11 shows the wide-band frequency response of the sinc filter and 図 7-12 shows the –3dB response.

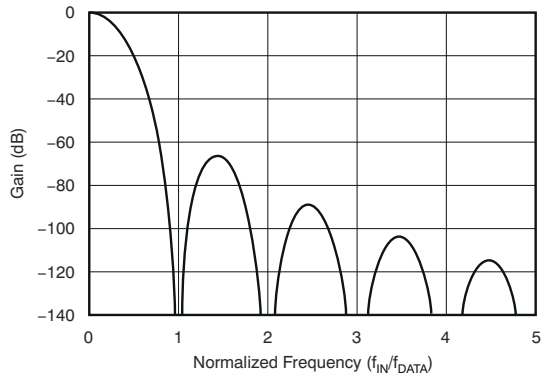


図 7-11. Sinc Filter Frequency Response

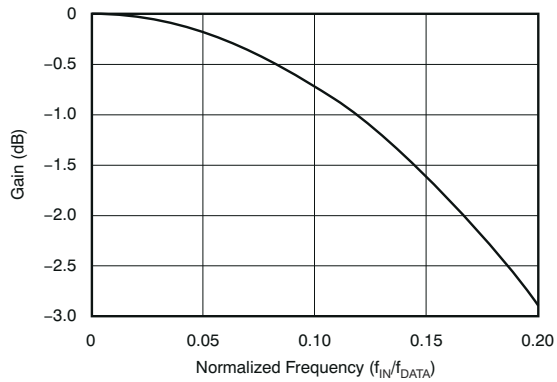


図 7-12. Sinc Filter –3dB Response

図 7-13 shows the sinc filter frequency response at f_{DATA} = 32kSPS. The tones at 1kHz and harmonics are the result of dither added to the modulator input to suppress idle tones. The frequency of the dither signal is f_{MOD} divided by the combined decimation ratio from 表 7-4. The rise of the noise floor at 2kHz is resultant of modulator noise shaping. For sinc filter decimation N = 32 (data rate = 32kSPS), the usable bandwidth through the use of external post filtering is 500Hz.

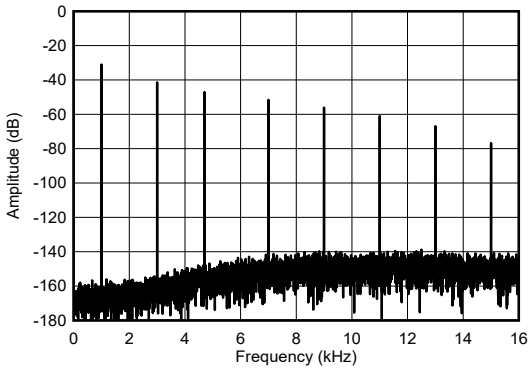


図 7-13. FFT Output of the Sinc Filter (f_{DATA} = 32kSPS)

The sinc filter data bypasses the data scaling, clip stage, and user calibration stages, and as a result, the sinc filter data are scaled differently compared to the FIR filter data. See the *Conversion Data Format* section for details of sinc filter data scaling.

7.3.6.2 FIR Filter Section

The second section of the digital filter is a multistage, FIR low-pass filter. Partially filtered data from the sinc filter are input to the FIR filter. The FIR filter determines the final frequency and phase response of the output data. 図 7-14 shows that the FIR filter consists of four stages.

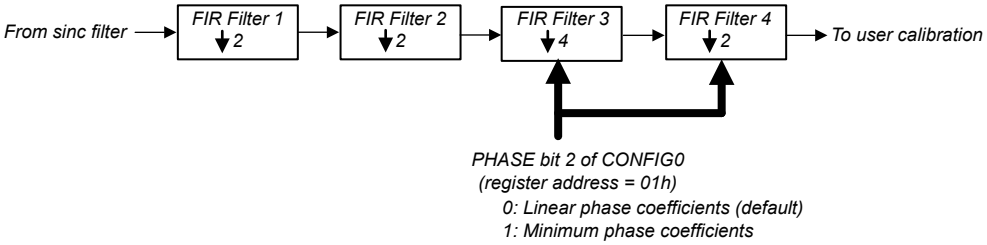


図 7-14. FIR Filter

The first two FIR stages are half-band filters with decimation = 2 in each stage. The third and fourth FIR stages determine the final frequency and phase response. Decimation is 4 and 2, in stages three and four. The total decimation ratio of the FIR filter is 32. Different filter coefficient sets in stage 3 and 4 determine linear or minimum phase filter response. The phase response is selected by the PHASE bit of the CONFIG0 register. 表 7-4 lists the combined decimation ratio of the sinc and FIR filter stages and the corresponding FIR filter data rate.

表 7-4. FIR Filter Data Rate

DR[2:0] BITS	COMBINED DECIMATION RATIO	DATA RATE (SPS)
000	8192	125
001	4096	250
010	2048	500
011	1024	1000
100	512	2000

表 7-5 lists the FIR filter coefficients and the data scaling for the linear and minimum phase coefficients.

表 7-5. FIR Filter Coefficients

COEFFICIENT	STAGE 1	STAGE 2	STAGE 3		STAGE 4	
	SCALE = 1/512	SCALE = 1/8388608	SCALE = 1/134217728		SCALE = 1/134217728	
	LINEAR PHASE	LINEAR PHASE	LINEAR PHASE	MINIMUM PHASE	LINEAR PHASE	MINIMUM PHASE
b_0	3	–10944	0	819	–132	11767
b_1	0	0	0	8211	–432	133882
b_2	–25	103807	–73	44880	–75	769961
b_3	0	0	–874	174712	2481	2940447
b_4	150	–507903	–4648	536821	6692	8262605
b_5	256	0	–16147	1372637	7419	17902757
b_6	150	2512192	–41280	3012996	–266	30428735
b_7	0	4194304	–80934	5788605	–10663	40215494
b_8	–25	2512192	–120064	9852286	–8280	39260213
b_9	0	0	–118690	14957445	10620	23325925
b_{10}	3	–507903	–18203	20301435	22008	–1757787
b_{11}		0	224751	24569234	348	–21028126
b_{12}		103807	580196	26260385	–34123	–21293602
b_{13}		0	893263	24247577	–25549	–3886901
b_{14}		–10944	891396	18356231	33460	14396783
b_{15}			293598	9668991	61387	16314388
b_{16}			–987253	327749	–7546	1518875
b_{17}			–2635779	–7171917	–94192	–12979500

表 7-5. FIR Filter Coefficients (続き)

COEFFICIENT	STAGE 1	STAGE 2	STAGE 3		STAGE 4	
	SCALE = 1/512	SCALE = 1/8388608	SCALE = 1/134217728		SCALE = 1/134217728	
	LINEAR PHASE	LINEAR PHASE	LINEAR PHASE	MINIMUM PHASE	LINEAR PHASE	MINIMUM PHASE
b_{18}			–3860322	–10926627	–50629	–11506007
b_{19}			–3572512	–10379094	101135	2769794
b_{20}			–822573	–6505618	134826	12195551
b_{21}			4669054	–1333678	–56626	6103823
b_{22}			12153698	2972773	–220104	–6709466
b_{23}			19911100	5006366	–56082	–9882714
b_{24}			25779390	4566808	263758	–353347
b_{25}			27966862	2505652	231231	8629331
b_{26}			25779390	126331	–215231	5597927
b_{27}			19911100	–1496514	–430178	–4389168
b_{28}			12153698	–1933830	34715	–7594158
b_{29}			4669054	–1410695	580424	–428064
b_{30}			–822573	–502731	283878	6566217
b_{31}			–3572512	245330	–588382	4024593
b_{32}			–3860322	565174	–693209	–3679749
b_{33}			–2635779	492084	366118	–5572954
b_{34}			–987253	231656	1084786	332589
b_{35}			293598	–9196	132893	5136333
b_{36}			891396	–125456	–1300087	2351253
b_{37}			893263	–122207	–878642	–3357202
b_{38}			580196	–61813	1162189	–3767666
b_{39}			224751	–4445	1741565	1087392
b_{40}			–18203	22484	–522533	3847821
b_{41}			–118690	22245	–2490395	919792
b_{42}			–120064	10775	–688945	–2918303
b_{43}			–80934	940	2811738	–2193542
b_{44}			–41280	–2953	2425494	1493873
b_{45}			–16147	–2599	–2338095	2595051
b_{46}			–4648	–1052	–4511116	–79991
b_{47}			–874	–43	641555	–2260106
b_{48}			–73	214	6661730	–963855
b_{49}			0	132	2950811	1482337
b_{50}			0	33	–8538057	1480417
b_{51}			0	0	–10537298	–586408
b_{52}					9818477	–1497356
b_{53}					41426374	–168417
b_{54}					56835776	1166800
b_{55}					41426374	644405
b_{56}					9818477	–675082
b_{57}					–10537298	–806095
b_{58}					–8538057	211391
b_{59}					2950811	740896
b_{60}					6661730	141976
b_{61}					641555	–527673
b_{62}					–4511116	–327618
b_{63}					–2338095	278227
b_{64}					2425494	363809
b_{65}					2811738	–70646
b_{66}					–688945	–304819
b_{67}					–2490395	–63159
b_{68}					–522533	205798
b_{69}					1741565	124363

表 7-5. FIR Filter Coefficients (続き)

COEFFICIENT	STAGE 1	STAGE 2	STAGE 3		STAGE 4	
	SCALE = 1/512	SCALE = 1/8388608	SCALE = 1/134217728		SCALE = 1/134217728	
	LINEAR PHASE	LINEAR PHASE	LINEAR PHASE	MINIMUM PHASE	LINEAR PHASE	MINIMUM PHASE
b_{70}					1162189	–107173
b_{71}					–878642	–131357
b_{72}					–1300087	31104
b_{73}					132893	107182
b_{74}					1084786	15644
b_{75}					366118	–71728
b_{76}					–693209	–36319
b_{77}					–588382	38331
b_{78}					283878	38783
b_{79}					580424	–13557
b_{80}					34715	–31453
b_{81}					–430178	–1230
b_{82}					–215231	20983
b_{83}					231231	7729
b_{84}					263758	–11463
b_{85}					–56082	–8791
b_{86}					–220104	4659
b_{87}					–56626	7126
b_{88}					134826	–732
b_{89}					101135	–4687
b_{90}					–50629	–976
b_{91}					–94192	2551
b_{92}					–7546	1339
b_{93}					61387	–1103
b_{94}					33460	–1085
b_{95}					–25549	314
b_{96}					–34123	681
b_{97}					348	16
b_{98}					22008	–349
b_{99}					10620	–96
b_{100}					–8280	144
b_{101}					–10663	78
b_{102}					–266	–46
b_{103}					7419	–42
b_{104}					6692	9
b_{105}					2481	16
b_{106}					–75	0
b_{107}					–432	–4
b_{108}					–132	0
b_{109}					0	0

図 7-15 shows the FIR pass-band frequency response to 0.375 × f_{DATA} with ±0.003dB pass-band ripple. 図 7-16 shows the pass-band, transition-band, and stop-band performance from 0Hz to f_{DATA}. The filter is designed for –135dB stop-band attenuation at the Nyquist frequency.

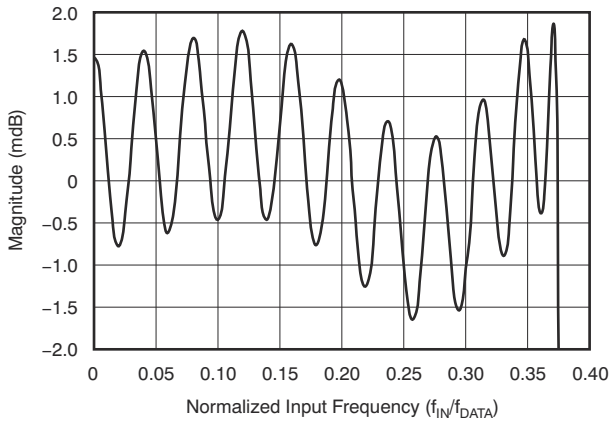


図 7-15. FIR Filter Pass-Band Response

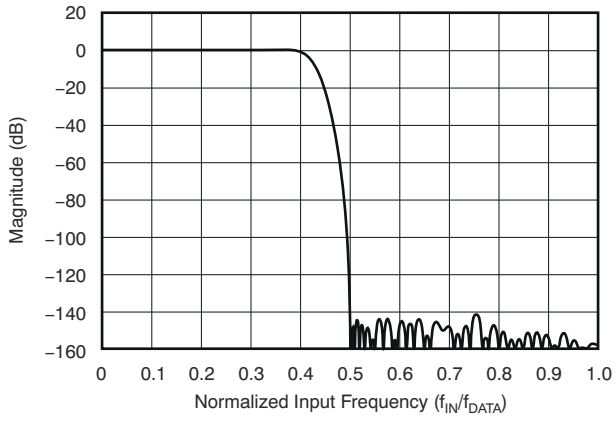


図 7-16. FIR Filter Transition Band Response

As with many sampled systems, the filter response repeats at multiples of the modulator sample rate (f_{MOD}). The filter response repeats at frequencies = N × f_{MOD} ± f_0, where N = 1, 2, and so on, and f_0 = filter pass-band). If present in the signal, these frequencies fold back (or alias) into the pass-band, causing errors. A low-pass input filter at the input removes the out-of-band signal to reduce the aliasing error. For the low-frequency output signal typical of many geophones, a single-pole filter at the PGA output is sufficient to reduce aliasing of the geophone thermal noise.

7.3.6.3 Group Delay and Step Response

The FIR filter offers linear and minimum phase filter options. The pass-band, transition band, and stop-band responses of the linear and minimum phase filters are the same but differ in phase and step response behavior.

7.3.6.3.1 Linear Phase Response

A linear phase filter has the unique property that the delay from input to output is constant across all input frequencies (that is, constant group delay). The constant delay property is independent of the nature of the input signal (impulse or swept-tone), and therefore the phase is linear across frequency, which can be important when analyzing multitone signals. However, as shown in 図 7-17, the group delay is longer for the linear phase filter compared to minimum phase. For both the linear and minimum filters, fully settled data are available 62 conversions after a step input change occurs.

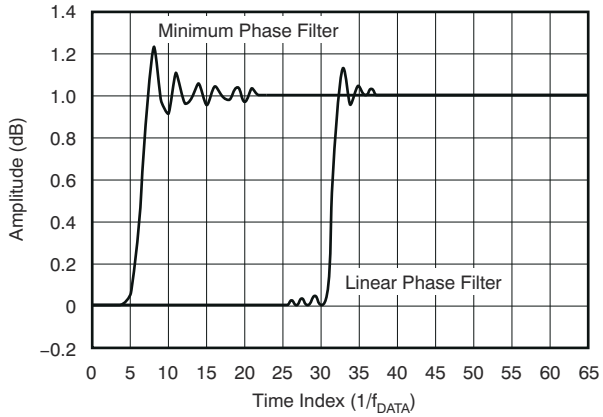


図 7-17. FIR Step Response

7.3.6.3.2 Minimum Phase Response

The minimum phase filter provides a short group delay for data from filter input to filter output. 図 7-18 shows the group delay for minimum and linear phase filters. The group delay of the minimum phase filter is a function of signal frequency. The PHASE bit of the CONFIG0 register programs the filter phase.

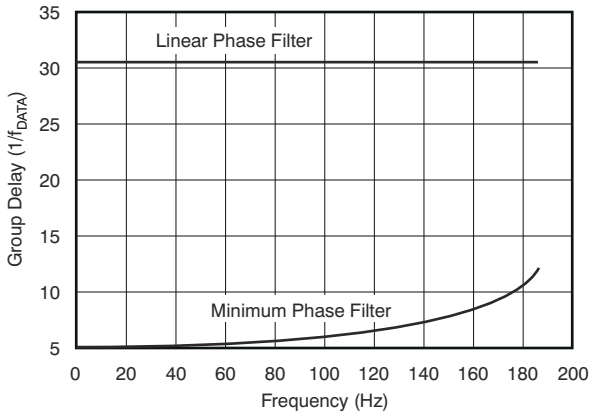


図 7-18. FIR Group Delay (f_{DATA} = 500SPS)

7.3.6.4 HPF Stage

The last stage of the digital filter is the high-pass filter (HPF). The high-pass filter is implemented as a first-order IIR filter. The high-pass filter removes dc and low frequencies from the data. The HPF is enabled by programming the FILTR[1:0] bits = 11b of the CONFIG0 register.

式 4 shows the z-domain transfer function of the filter:

$$H(z) = \frac{2 - a}{2} \frac{1 - z^{-1}}{1 - (1 - a)z^{-1}} \quad (4)$$

where:

$$a = \frac{2\sin(\omega_N)}{\cos(\omega_N) + \sin(\omega_N)}$$

- $\omega_N = \pi \times f_C / f_{DATA}$ (normalized corner frequency, radians)
- f_C = Corner frequency (Hz)
- f_{DATA} = Output data rate (Hz)

Be aware the corner frequency programming is a function of f_{DATA}. As shown by 式 5, the value written to the HPF1, HPF0 registers is value *a*, computed by 式 4, × 2^{16}.

$$HPF[15:0] = a \times 2^{16} \quad (5)$$

表 7-6 shows examples of the high-pass filter programming.

表 7-6. High-Pass Filter Value Examples

HPF[15:0]	f_C (Hz)	f_{DATA} (SPS)
0332h	0.5	250
0332h	1.0	500
019Ah	1.0	1000

The HPF accumulates data to perform the high-pass function. Similar to the operation of an analog HPF after a dc step change is applied to the input, the filter takes time to accumulate data to remove dc from the signal. The lower the corner frequency, the longer the filter takes to settle.

To shorten the HPF settling time, the offset register is used as a *seed* value for the HPF accumulator. The accumulator is loaded with the offset register each time the HPF state is changed from *disabled* to *enabled*. The offset register can be preset with an estimated value, or a calibrated value if the dc level is known. To improve accuracy, scale the offset value by the inverse value of GAIN[3:0] / 400000h. The normal offset operation is disabled when the HPF is enabled.

To initialize the HPF accumulator with the OFFSET[2:0] registers:

1. Disable the HPF.
2. Write the desired value to the OFFSET[2:0] registers.
3. Enable the HPF. OFFSET[2:0] is loaded to the HPF data accumulator.
4. The HPF tracks the remaining dc value from the signal.

Subsequent writes to the OFFSET[2:0] registers are ignored. To reload the contents of the OFFSET[2:0] registers to the HPF, disable and re-enable the HPF.

7.3.7 Clock Input

A clock signal is required for operation. The clock signal is applied to the CLK pin at 4.096MHz. As with many precision data converters, a low-jitter clock is required to achieve data sheet performance. Avoid the use of R-C clock oscillators. A crystal-based clock source is recommended. Avoid ringing on the clock signal by placing a series resistor in the clock PCB trace to source-terminate. Keep the clock signal routed away from other clock signals, input pins, and analog components.

7.3.8 GPIO

The ADC provides two general-purpose I/O (GPIO) pins that can be used as digital inputs or outputs. The GPIO voltage levels are IOVDD and DGND. 図 7-19 illustrates the GPIO block diagram.

The GPIOs are programmed by the GPIO register. The GPIOs are programmed as an input or output by the GPIOx_DIR bits. The GPIO state is read or written by the GPIOx_DAT bits. When programmed as an output, reading the GPIOx_DAT bits returns the register bit value previously written. If the GPIOs are unused, terminate the GPIOs with pulldown resistors to prevent the pins from floating.

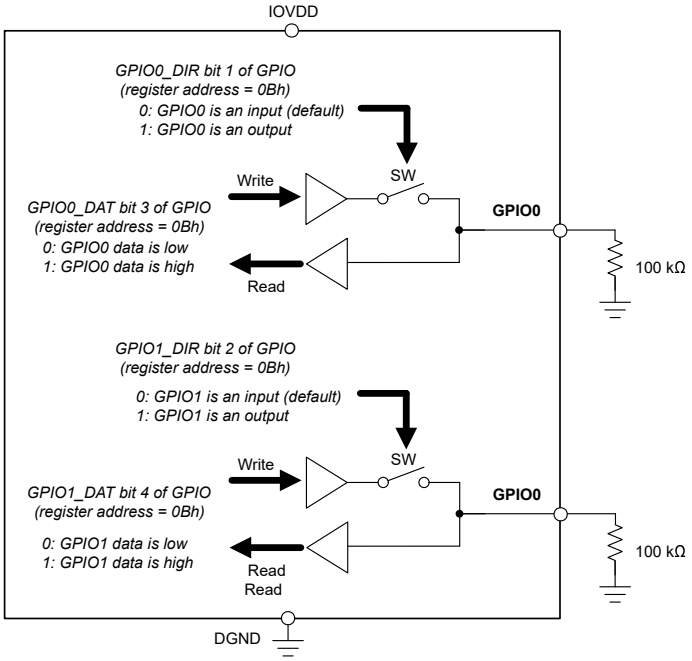


図 7-19. GPIO Operation

7.4 Device Functional Modes

7.4.1 Power-Down Mode

Power-down is engaged by taking the $\overline{\text{PWDN}}$ pin low, or by software control, by sending the STANDBY command. To exit power-down, take $\overline{\text{PWDN}}$ high or send the WAKEUP command to exit software power-down (with the clock running). Power-down disables the analog circuit; however, the digital LDO (CAPD pin) remains biased, drawing a small bias current from IOVDD. In comparison, software power-down draws larger IOVDD bias current. In both power-down modes, the ac signals of the digital outputs are stopped but remain driven high or low. The digital inputs must not be allowed to float; otherwise, leakage current can flow from the IOVDD supply. Reset the ADC if the clock is interrupted in power-down. Synchronization is lost in power-down; therefore, resynchronize the ADC.

7.4.2 Reset

The ADC is reset by three methods: power-on reset (POR), the $\overline{\text{RESET}}$ pin, or the RESET command. Power-on reset occurs when the power-supply voltages cross the respective thresholds. See the *Power-Up Switching Characteristics* for details. To reset the ADC by pin, drive $\overline{\text{RESET}}$ low for at least two f_{CLK} cycles and return high for reset. By command, reset takes effect on the next rising f_{CLK} edge after the eighth rising edge of SCLK of the reset command. At reset, the filter is restarted and the user registers are reset to default. Reset timing is illustrated in 図 5-5.

7.4.3 Synchronization

The ADC is synchronized by the SYNC pin or by the SYNC command, resulting in restart of the digital filter cycle. Synchronization by the pin occurs on the next rising edge of CLK after SYNC is taken high on the falling edge of CLK. Synchronization by the SYNC command occurs on the rising edge of CLK following the eighth bit of the command.

The following results in loss of synchronization:

- When a power-up cycle or ADC reset occurs
- When the hardware or software power-down modes are entered
- The following register mode changes occur:
  - DR[2:0] (data rate)

- PHASE (filter phase)
- SYNC (synchronization mode)
- SRC[1:0] (sample rate converter enabled or disabled)

There are two synchronization control modes: pulse sync and continuous sync. The synchronization mode is programmed by the SYNC bit of the ID/SYNC register.

7.4.3.1 Pulse-Sync Mode

Pulse-sync mode unconditionally synchronizes the ADC on the rising edge of SYNC. When synchronized, the internal filter memory is reset, $\overline{\text{DRDY}}$ goes high, and the filter cycle restarts. The following 63 $\overline{\text{DRDY}}$ periods are disabled to allow for digital filter settling. $\overline{\text{DRDY}}$ asserts low when the conversion data are ready. See 図 5-4 for synchronization timing details.

7.4.3.2 Continuous-Sync Mode

Continuous-sync mode offers the option of accepting a continuous clock signal on the SYNC pin. The ADC compares the period of the SYNC clock signal to *N* periods of the $\overline{\text{DRDY}}$ signal to qualify resynchronization. Initially, the first SYNC positive edge synchronizes the ADC. Resynchronization occurs only when the time period between rising edges of SYNC over *N* multiple $\overline{\text{DRDY}}$ periods differ by at least ± one f_{CLK} cycle, where *N* = 1, 2, 3, and so on. Otherwise, the SYNC clock period is in synchronization with the existing $\overline{\text{DRDY}}$ pulses, so no resynchronization occurs. Be aware the continuous sync mode cannot be used when the sample rate converter is enabled.

After synchronization, $\overline{\text{DRDY}}$ continues to pulse; however, data are held low for 63 data periods to allow for the digital filter to settle. See 図 5-4 for the $\overline{\text{DRDY}}$ behavior. Because of the initial delay of the digital filter, the SYNC input signal and the $\overline{\text{DRDY}}$ pulses exhibit an offset time. The offset time is a function of the data rate.

7.4.4 Sample Rate Converter

The sample rate converter (SRC) compensates clock frequency error by resampling the modulator data at a new rate set by a compensation factor written to the SRC registers. The compensation range is ±244ppm with 7.45ppb ($1 / 2^{27}$) resolution.

Clock frequency error is compensated by writing a value to the SCR0 and SRC1 registers. The register value is in two's-complement format for positive and negative error compensation. Positive register data values decrease the data rate frequency (increases the period). The compensated data rate frequency is observed by the frequency of the $\overline{\text{DRDY}}$ signal.

表 7-7 shows example values of SRC compensation. 8000h disables the sample rate converter. 0000h passes the data through with no compensation but adds an $8 / f_{CLK}$ delay to the existing time delay of SYNC input to the $\overline{\text{DRDY}}$ pulses.

表 7-7. Example SRC Compensation Values

SRC[15:0] VALUE	COMPENSATION FACTOR
7FFFh	$(1 – 32{,}767 / 2^{27}) \times f_{DATA}$
0001h	$(1 – 1 / 2^{27}) \times f_{DATA}$
0000h	$1 \times f_{DATA}$
7FFFh	$(1 + 1 / 2^{27}) \times f_{DATA}$
8001h	$(1 + 32{,}767 / 2^{27}) \times f_{DATA}$
8000h	$1 \times f_{DATA}$ (SRC disabled)

Resynchronize the ADC after the sample rate converter is enabled or disabled.

Because the SRC is a digital function, operation is deterministic without error. When the target compensation value is determined, the value can be immediately written to the ADC, or incrementally written up to the determined value to reduce the effect of step changes in the output frequency. Because two bytes are used for the SRC registers, use the multibyte command operation to write to the SRC registers and complete the write

operation 256 CLK cycles before the $\overline{DRDY}$ falling edge. This procedure simultaneously loads the high and low bytes for compensation. See 図 5-7 for details.

7.4.5 Offset and Gain Calibration

The ADC integrates calibration registers to correct offset and gain errors. As shown in 式 6 and 図 7-20, the 24-bit offset value (OFFSET[23:0]) is subtracted from the filter data before multiplication by the 24-bit gain value (GAIN[23:0]), divided by 400000h. The data are clipped to 32 bits to yield the final output. The offset operation is bypassed when the high-pass filter is enabled.

$$\text{Output} = (\text{Input} - \text{OFFSET}[23:0]) \cdot \frac{\text{GAIN}[23:0]}{400000h} \quad (6)$$

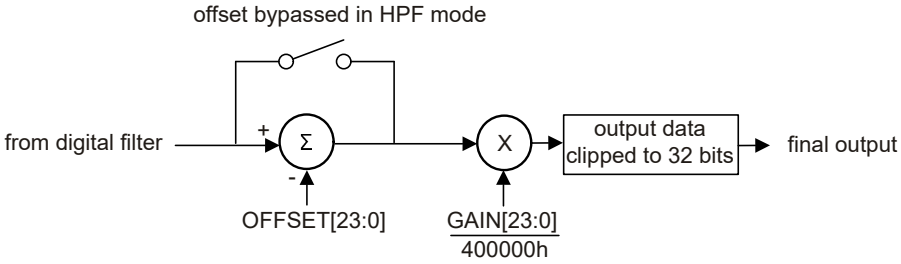


図 7-20. Calibration Block Diagram

7.4.5.1 OFFSET Register

Offset correction is by a 24-bit word consisting of three 8-bit registers (high address is the MSB). The offset value is left-justified to align to the 32-bit data. The offset value is two's-complement coding with a maximum positive value of 7FFFFFh and a maximum negative value of 800000h. As given in 表 7-8, OFFSET is subtracted from the conversion data. Offset error is corrected by the offset calibration command with the input-short multiplexer option, or by collecting shorted-input ADC data and writing the value to the registers.

Although the offset correction range is from –FS to +FS, the sum of offset and gain correction must not exceed 106% of the uncalibrated range.

When the high-pass filter is enabled, offset correction is disabled. The offset value is used instead as a starting value to shorten the high-pass filter settling time. To reload the offset value to the HPF, disable and re-enable the high-pass filter. See the *HPF Stage* section for more details.

表 7-8. Offset Calibration Values

OFFSET[31:0]	CALIBRATED OUTPUT CODE (1)
00007Fh	FFFF8100h
000000h	00000000h
FFFF7Fh	00008100h

(1) Ideal code value with no offset error.

7.4.5.2 GAIN Register

Gain correction is through a 24-bit word, consisting of three 8-bit registers (high address = MSB). The gain value is 24 bits, coded in straight binary and normalized to 1.0 for GAIN[23:0] equal to 400000h. With a calibration signal applied, gain error is calibrated by either the gain calibration command, or by collecting ADC data and writing a computed value to the gain registers. 表 7-9 lists examples of the GAIN[23:0] register values. Although the range of gain values can be much greater or less than 1, the sum of offset and gain correction must not exceed 106% of the uncalibrated range.

表 7-9. Gain Calibration Values

GAIN[31:0]	GAIN CORRECTION FACTOR
433333h	1.05
400000h	1.00
3CCCCCh	0.95

7.4.5.3 Calibration Procedure

ADC calibration is performed by ADC calibration commands or manual calibration. The calibration procedure is as follows:

1. Select the PGA or buffer operation, input channel, and PGA gain condition for calibration.
2. Preset the OFFSET register = 000000h and the GAIN register = 400000h.
3. Disable the high-pass filter for offset calibration. Short the inputs to the system, or use the input MUX to provide the input short. A system-level input short yields more accurate calibration. After the input settles, either send the OFSCAL command or perform a manual calibration.
   a. OFSCAL command. After the command is sent, $\overline{DRDY}$ is driven low 81 conversion periods later to indicate calibration is complete. The OFFSET register is updated with the new calibration value. As shown in 図 7-21, the first data output uses the new OFFSET value.
   b. Manual calibration. Wait at least 64 conversions for the digital filter to settle then average a number of data points to improve calibration accuracy. Write the value to the 24-bit OFFSET register.
4. Apply a gain calibration voltage. After the input settles, either send the GANCAL command or perform a manual calibration.
   a. GANCAL command. Apply a positive dc full-scale calibration voltage. After the command is sent, $\overline{DRDY}$ is driven low 81 conversion periods later to indicate calibration is complete. The ADC calculates GAIN such that the full-scale code is equal to the applied calibration signal. As shown in 図 7-21, the first data output uses the new GAIN value.
   b. Manual calibration. Apply an ac signal coherent to the sample rate or dc calibration signal that are slightly below full-scale (for example, 2.4V for gain = 1). Using a calibration signal less than the full-scale range prevents clipped output codes that otherwise lead to incorrect calibration. Wait 64 conversions for the digital filter to settle then average a number of data points to improve calibration accuracy. For ac-signal calibration, use a number of coherent signal periods to compute the RMS value.

   式 7 computes the value of GAIN for manual calibration.

$$\text{GAIN}[23:0] = 400000\text{h} \cdot \frac{\text{Expected Output Code}}{\text{Actual Output Code}} \tag{7}$$

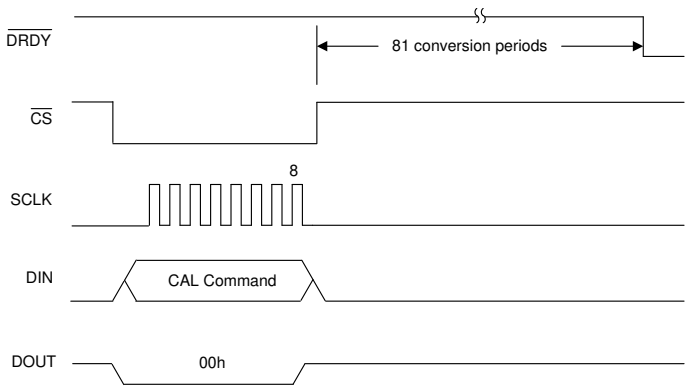


図 7-21. Calibration Command

7.5 Programming

7.5.1 Serial Interface

Conversion data are read and ADC configuration is made through the SPI-compatible serial interface. The interface consists of four signals: $\overline{CS}$, SCLK, DIN, and DOUT. $\overline{DRDY}$ asserts low when conversion data are ready. The serial interface is passive (peripheral mode), where the serial clock (SCLK) is an input. The ADC operates in SPI mode 0, where CPOL = 0 and CPHA = 0. In mode 0, SCLK idles low and data are updated on the SCLK falling edges and are read on the SCLK rising edges.

7.5.1.1 Chip Select ($\overline{CS}$)

$\overline{CS}$ is an active-low input that selects the serial interface for communication. A communication frame is started by taking $\overline{CS}$ low and is ended by taking $\overline{CS}$ high. Because only one command per frame is permitted, toggle $\overline{CS}$ between commands. Taking $\overline{CS}$ high before the command is completed resets the operation and blocks further SCLK inputs. $\overline{CS}$ high forces DOUT to a high-impedance state. $\overline{DRDY}$ remains active regardless of the state of $\overline{CS}$.

7.5.1.2 Serial Clock (SCLK)

SCLK is the serial clock input that shifts data into and out of the ADC. The ADC latches DIN data on the rising edge of SCLK. DOUT data are shifted out on the falling edge of SCLK. Keep SCLK low when not active. The SCLK pin is a Schmidt-trigger input that reduces sensitivity to SCLK noise. However, keep the SCLK signal as noise free as possible to prevent inadvertent shifting of the data.

7.5.1.3 Data Input (DIN)

DIN inputs data to the ADC. DIN data are latched on the rising edge of SCLK.

7.5.1.4 Data Output (DOUT)

DOUT is the data output pin. Data are shifted out on the falling edge of SCLK and are latched by the host on the rising edge. Because the conversion data MSB is on DOUT when $\overline{CS}$ is driven low ($\overline{DRDY}$ low), the MSB of the data is read on the first rising edge of SCLK. Minimize trace length to reduce load capacitance on the pin. Place a series termination resistor close to the pin to terminate the PCB trace impedance. Taking $\overline{CS}$ high forces DOUT to a high-impedance state.

7.5.1.5 Data Ready ($\overline{DRDY}$)

$\overline{DRDY}$ is an active-low output that indicates conversion data are ready. $\overline{DRDY}$ is active regardless of the state of $\overline{CS}$. $\overline{DRDY}$ is driven high on the first falling edge of SCLK, regardless if data are being read or if a command is input. As shown in 図 7-22, if data are not retrieved, $\overline{DRDY}$ pulses high for eight f_{CLK} periods.

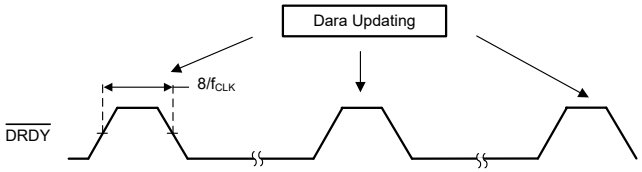


図 7-22. $\overline{DRDY}$ With No Data Retrieval

7.5.2 Conversion Data Format

As listed in 表 7-10, the conversion data are coded in 32-bit, two's-complement format to represent positive and negative numbers. If desired, the data read operation can be shortened to 24 bits by taking $\overline{CS}$ high. In sinc filter mode, data are scaled by half compared to the FIR filter mode.

表 7-10. Output Data Format

V_{IN} (V)	CONVERSION CODES(1)	
	FIR FILTER	SINC FILTER(2)
≥ 2.5V × (2^{31} – 1) / 2^{31} / Gain	7FFFFFFFh	3FFFFFFFh

表 7-10. Output Data Format (続き)

V_{IN} (V)	CONVERSION CODES(1)	
	FIR FILTER	SINC FILTER(2)
2.5V / (Gain × (2^{31} – 1))	00000001h	<00000001h
0	00000000h	00000000h
–2.5V / (Gain × 2^{31})	FFFFFFFFh	>FFFFFFFFh
≤ –2.5V / Gain	80000000h	C0000000h

(1) Excluding the effects of reference voltage error, noise, linearity, offset, and gain errors.
(2) Because of the low values of OSR, full 32-bit resolution is not available in sinc filter mode. When the input signal is overdriven, the sinc filter continues to output code values beyond the nominal full-scale values until clipped when the modulator saturates.

7.5.3 Commands

表 7-11 lists the commands for the ADC. Most commands are one byte in length. However, the number of bytes for the register read and write commands depend on the amount of register data specified in the command.

表 7-11. Command Descriptions

MNEMONIC	TYPE	DESCRIPTION	BYTE 1(1)	BYTE 2
WAKEUP	Control	Wake from standby mode or NOP	0000 000x (00h or 01h)	—
STANDBY	Control	Enter standby (software power-down mode)	0000 001x (02h or 03h)	—
SYNC	Control	Synchronize	0000 010x (04h or 5h)	—
RESET	Control	Reset	0000 011x (06h or 07h)	—
RDATA	Data	Read conversion data	0001 0010 (12h)	—
RREG	Register	Read *nnnn* registers beginning at address *rrrr*	0010 *rrrr* (20h + *rrrr*)(2)	0000 *nnnn* (00h + *nnnn*)(3)
WREG	Register	Write *nnnn* registers beginning at address *rrrr*	0100 *rrrr* (40h + *rrrr*)(2)	0000 *nnnn* (00h + *nnnn*)(3)
OFSCAL	Calibration	Offset calibration	0110 0000 (60h)	—
GANCAL	Calibration	Gain calibration	0110 0001 (61h)	—

(1) x = Don't care.
(2) rrrr = Starting address for register read and write commands.
(3) nnnn = Number of registers to be read or written – 1. For example, to read or write three registers, *nnnn* = 2.

7.5.3.1 Single Byte Command

図 7-23 shows the general format of a single byte command. For the response bytes of the RDATA command, see the RDATA command.

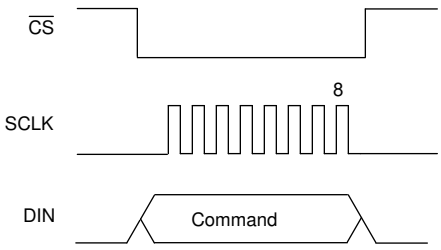


図 7-23. Single Byte Command Format

7.5.3.2 WAKEUP: Wake Command

The WAKEUP command exits standby mode to resume normal operation. If the ADC is already powered, the command is no operation (NOP). When exiting standby mode, the ADC requires resynchronization. See the *Power-Down Mode* section for details of power-down mode.

7.5.3.3 STANDBY: Software Power-Down Command

The STANDBY command enters the software power-down mode. The ADC exits software power-down mode by the WAKEUP command. See the *Power-Down Mode* section for details of power-down mode.

7.5.3.4 SYNC: Synchronize Command

The SYNC command synchronizes the ADC. Synchronization occurs at the eighth bit of the SYNC command byte. When synchronized, the current conversion is stopped and restarted. To synchronize multiple ADCs by software command, send the command simultaneously to all devices. The SYNC pin must be high when using the command. See the *Synchronization* section for details of synchronization.

7.5.3.5 RESET: Reset Command

The RESET command resets the ADC. See the *Reset* section for details of the reset operation.

7.5.3.6 Read Data Direct

There are two methods to read conversion data: read data direct and read data by command.

Read data direct does not require a command, instead after $\overline{\text{DRDY}}$ falls low, simply apply SCLK to read the data. 図 7-24 shows the read data direct operation. When $\overline{\text{DRDY}}$ falls low, take $\overline{\text{CS}}$ low to start the read operation. $\overline{\text{CS}}$ low causes DOUT to transition from tri-state mode to the output of the data MSB. Data are read on the rising edge of SCLK and updated on the falling edge of SCLK. $\overline{\text{DRDY}}$ returns high on the first falling edge of SCLK. DOUT is low after 32 data bits are read. To read the same data again before new data are available, use the RDATA command.

Keep DIN low when reading conversion data. If the RDATA (read conversion data) or RREG (read register data) command is sent, output data are interrupted in response to the command. If $\overline{\text{DRDY}}$ falls low during the read operation, the new data are lost unless a minimum of three bytes of the old data are read.

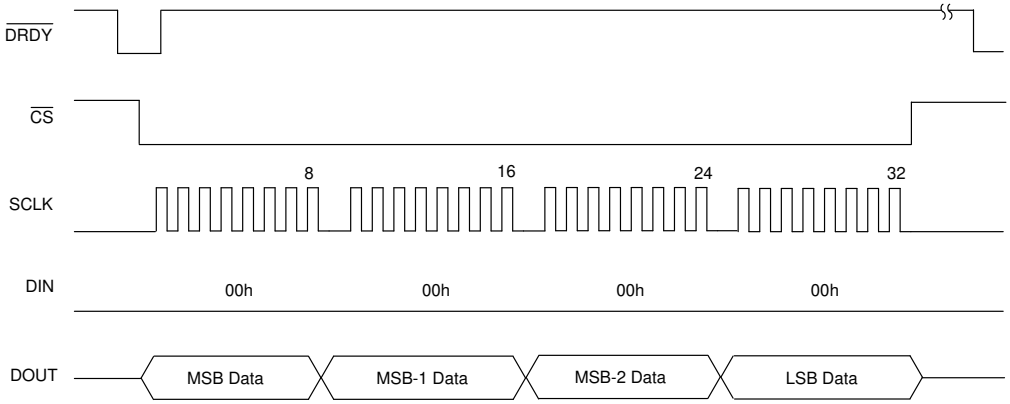


図 7-24. Read Data Direct

7.5.3.7 RDATA: Read Conversion Data Command

The RDATA command (図 7-25) is useful to re-read data within the same conversion period or to read data interrupted by a read register command. In both cases, $\overline{\text{DRDY}}$ is high because $\overline{\text{DRDY}}$ is driven high on the first SCLK of the previous operation. If $\overline{\text{DRDY}}$ is high, the first output byte is zero followed by data. If low, the first output byte is byte 1 of the conversion data, which is restarted for output byte 2.

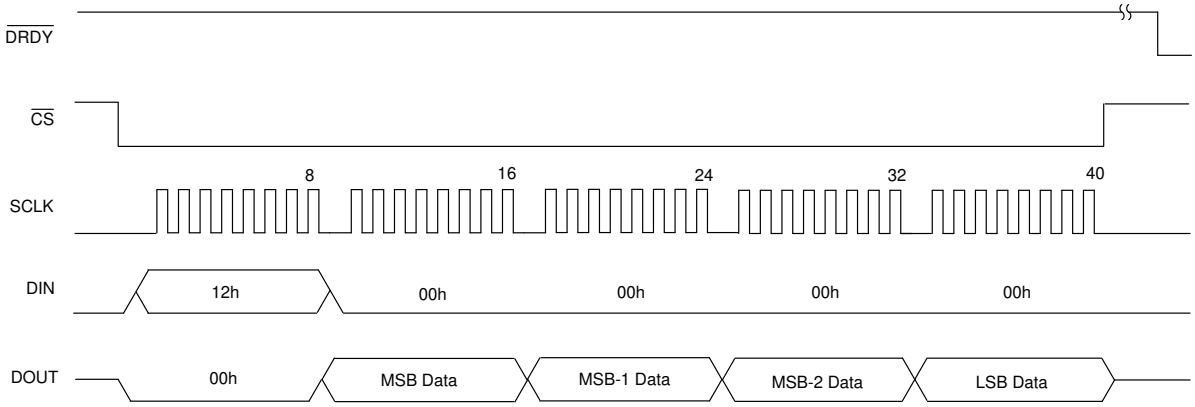


図 7-25. Read Conversion Data by Command

7.5.3.8 RREG: Read Register Command

The RREG command reads register data. The command is comprised of two bytes followed by output of the designated number of register bytes. The ADC auto-increments the address up to the number of registers specified in byte 2 of the command. The incrementing address does not wrap. The first byte of the command is the opcode added to the register starting address, and the second byte is the number of registers to read minus one.

- First command byte: 0010 rrrr, where *rrrr* is the starting register address
- Second command byte: 0000 nnnn, where *nnnn* is the number of registers to read minus one

図 7-26 shows an example of a three-register read operation starting at register address 01h. The first register data appears on DOUT at the 16th falling edge of SCLK. The data are latched on the rising edge of SCLK.

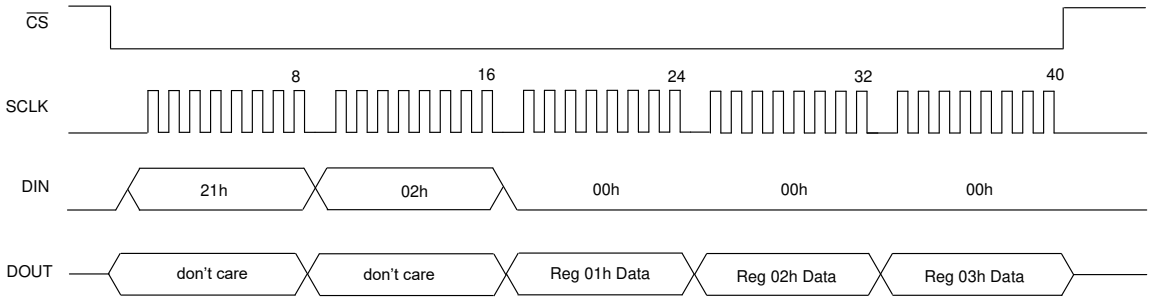


図 7-26. Read Register Data

7.5.3.9 WREG: Write Register Command

The WREG command writes register data. The command is two bytes followed by the designated number of register bytes to be written. The ADC auto-increments the address up to the number of registers specified in the command. The incrementing address does not wrap. The first byte of the command is the opcode added to the register starting address, and the second byte is the number of registers to write minus one.

- First command byte: 0100 rrrr, where *rrrr* is the starting address of the first register
- Second command byte: 0000 nnnn, where *nnnn* is the number of registers to write minus one
- Data bytes: Dependent on the number of registers specified

図 7-27 shows an example of a three-register write operation starting at register address 01h.

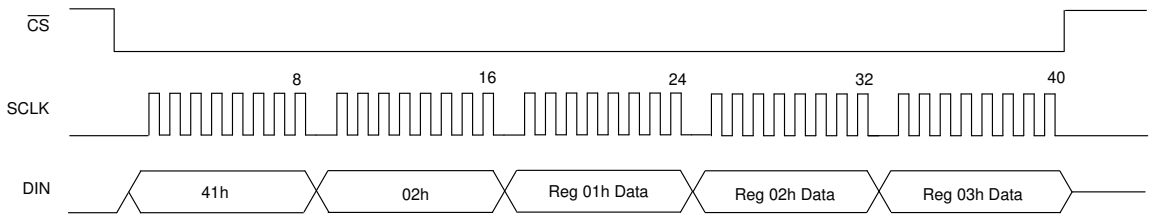


図 7-27. Write Register Data

7.5.3.10 OFSCAL: Offset Calibration Command

The OFSCAL command performs offset calibration. See the *Calibration Procedure* section for details of operation.

7.5.3.11 GANCAL: Gain Calibration Command

The GANCAL command performs a gain calibration. See the *Calibration Procedure* section for details of operation.

8 Register Map

Collectively, the registers contain all the information needed to configure the device (such as data rate, filter mode, specific reference voltage, and so on). The registers are accessed by the read and write commands (RREG and WREG). Registers can be accessed individually, or accessed in multiples given by the number of registers specified in the command field.

Changes made to certain register bits result in a filter reset, thus requiring resynchronization of the ADC. See the *Synchronization* section for details.

表 8-1. Register Map

ADDRESS	REG LINK	RESET	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00h	ID/SYNC	xxxx0010b	REVID[3:0]					DEVID[2:0]		SYNC
01h	CONFIG0	10010010b	RESERVED		DR[2:0]			PHASE	FILTR[1:0]	
02h	CONFIG1	00010000b	MUX[2:0]			RESERVED		GAIN[2:0]		
03h	HPF0	00110010h	HPF[7:0]							
04h	HPF1	00000011b	HPF[15:8]							
05h	OFFSET0	00000000b	OFFSET[7:0]							
06h	OFFSET1	00000000b	OFFSET[15:8]							
07h	OFFSET2	00000000b	OFFSET[23:16]							
08h	GAIN0	00000000b	GAIN[7:0]							
09h	GAIN1	00000000b	GAIN[15:8]							
0Ah	GAIN2	01000000b	GAIN[23:16]							
0Bh	GPIO	000xx000b	RESERVED			GPIO1_DAT	GPIO0_DAT	GPIO1_DIR	GPIO0_DIR	RESERVED
0Ch	SRC0	00000000b	SRC[7:0]							
0Dh	SRC1	10000000b	SRC[15:8]							

8.1 Register Descriptions

表 8-2 shows the register access codes for the ADS1288 registers.

表 8-2. ADS1288 Access Codes

Access Type	Code	Description
R	R	Read
R-W	R/W	Read or write
W	W	Write
-n		Value after reset or the default value

8.1.1 ID/SYNC: Device ID, SYNC Register (Address = 00h) [Reset = xxxx0010b]

図 8-1. ID/SYNC Register

7	6	5	4	3	2	1	0
REVID[3:0]				DEVID[2:0]			SYNC
R-xxxxb				R-001b			R/W-0b

表 8-3. ID/SYNC Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	REVID[3:0]	R	xxxxb	Factory-programmed die revision. These bits identify the revision of the die. The die revision is subject to change without notification.
3:1	DEVID[2:0]	R	001b	Factory-programmed device identification. These bits identify the ADC. 001b = ADS1288
0	SYNC	R/W	0b	Synchronization mode selection. See the *Synchronization* section for details. 0b = Pulse-sync mode 1b = Continuous-sync mode

8.1.2 CONFIG0: Configuration Register 0 (Address = 01h) [Reset = 92h]

図 8-2. CONFIG0 Register

7	6	5	4	3	2	1	0
RESERVED		DR[2:0]			PHASE	FILTR[1:0]	
R-10b		R/W-010b			R/W-0b	R/W-10b	

表 8-4. CONFIG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	10b	Reserved bits
5:3	DR[2:0]	R/W	010b	Data rate selection. See the *Digital Filter* section for details. 000b = 125SPS 001b = 250SPS 010b = 500SPS 011b = 1000SPS 100b = 2000SPS 101b –111b = Reserved
2	PHASE	R/W	0b	FIR filter phase selection. See the *Digital Filter* section for details. 0b = Linear phase 1b = Minimum phase
1:0	FILTR[1:0]	R/W	10b	Digital filter configuration. See the *Digital Filter* section for details. 00b = Reserved 01b = Sinc filter output 10b = FIR filter output 11b = FIR + IIR filter output

8.1.3 CONFIG1: Configuration Register 1 (Address = 02h) [Reset = 10h]

図 8-3. CONFIG1 Register

7	6	5	4	3	2	1	0
MUX[2:0]			RESERVED		GAIN[2:0]		
R/W-000b			R-10b		R/W-000b		

表 8-5. CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	MUX[2:0]	R/W	000b	Input MUX selection. See the *Analog Input* section for details. 000b = Input 1 001b = Input 2 010b = Internal short with a 400Ω resistor 011b = Input 1 and input 2 100b = Reserved 101b = Internal short with a 0Ω resistor 110b, 111b = Reserved
4:3	RESERVED	R	10b	Reserved bits
2:0	GAIN[2:0]	R/W	000b	PGA gain selection. See the *PGA and Buffer* section for details. 000b = 1 001b = 2 010b = 4 011b = 8 100b = 16 101b = 32 110b = 64 111b = Buffer operation

8.1.4 HPF0, HPF1: High-Pass Filter Registers (Address = 03h, 04h) [Reset = 32h, 03h]

図 8-4. HPF0 Register

7	6	5	4	3	2	1	0
HPF[7:0]							
R/W-32h							

図 8-5. HPF1 Register

7	6	5	4	3	2	1	0
HPF[15:8]							
R/W-03h							

表 8-6. HPF0, HPF1 Registers Field Description

Bit	Field	Type	Reset	Description
15:0	HPF[15:0]	R/W	0332h	High-pass filter programming. These registers program the corner frequency of the high-pass filter. See the *HPF Stage* section for details.

8.1.5 OFFSET0, OFFSET1, OFFSET2: Offset Calibration Registers (Address = 05h, 06h, 07h) [Reset = 00h, 00h, 00h]

図 8-6. OFFSET0 Register

7	6	5	4	3	2	1	0
OFFSET[7:0]							
R/W-00h							

図 8-7. OFFSET1 Register

7	6	5	4	3	2	1	0
OFFSET[15:8]							
R/W-00h							

図 8-8. OFFSET2 Register

7	6	5	4	3	2	1	0
OFFSET[23:16]							
R/W-00h							

表 8-7. OFFSET0, OFFSET1, OFFSET2 Registers Field Description

Bit	Field	Type	Reset	Description
23:0	OFFSET[23:0]	R/W	000000h	Offset calibration. These bits are the 24-bit offset calibration word. The format is two's-complement coding. The ADC subtracts the value of offset from the conversion result prior to the gain calibration operation. See the *Offset and Gain Calibration* section for details.

8.1.6 GAIN0, GAIN1, GAIN2: Gain Calibration Registers (Address = 08h, 09h, 0Ah) [Reset = 00h, 00h, 40h]

図 8-9. GAIN0 Register

7	6	5	4	3	2	1	0
GAIN[7:0]							
R/W-00h							

図 8-10. GAIN1 Register

7	6	5	4	3	2	1	0
GAIN[15:8]							
R/W-00h							

図 8-11. GAIN2 Register

7	6	5	4	3	2	1	0
GAIN[23:16]							
R/W-40h							

表 8-8. GAIN0, GAIN1, GAIN2 Registers Field Description

Bit	Field	Type	Reset	Description
23:0	GAIN[23:0]	R/W	400000h	Gain calibration. These bits are the 24-bit, gain calibration word. Gain calibration is straight-binary coding. The register value is divided by 400000h (2^{22}) and multiplied with the conversion data. The gain operation occurs after the offset operation. See the *Offset and Gain Calibration* section for details.

8.1.7 GPIO: Digital Input/Output Register (Address = 0Bh) [Reset = 000xx000b]

図 8-12. GPIO Register

7	6	5	4	3	2	1	0
RESERVED			GPIO1_DAT	GPIO0_DAT	GPIO1_DIR	GPIO0_DIR	RESERVED
R/W-000b			R/W-xb	R/W-xb	R/W-0b	R/W-0b	R/W-0b

表 8-9. GPIO Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	000b	Always write 000b.
4	GPIO1_DAT	R/W	xb	GPIO1 data. See the *GPIO* section for details. 0b = GPIO1 is low 1b = GPIO1 is high
3	GPIO0_DAT	R/W	xb	GPIO0 data. 0b = GPIO0 is low 1b = GPIO0 is high
2	GPIO1_DIR	R/W	0b	GPIO1 direction. 0b = GPIO1 is an input 1b = GPIO1 is an output
1	GPIO0_DIR	R/W	0b	GPIO0 direction. 0b = GPIO0 is an input 1b = GPIO0 is an output
0	RESERVED	R/W	0b	Always write 0b.

8.1.8 SRC0, SRC1: Sample Rate Converter Registers (Address = 0Ch, 0Dh) [Reset = 00h, 80h]

図 8-13. SRC0 Register

7	6	5	4	3	2	1	0
SRC[7:0]							
R/W-00h							

図 8-14. SRC1 Register

7	6	5	4	3	2	1	0
SRC[15:8]							
R/W-80h							

表 8-10. SRC0, SRC1 Registers Field Description

Bit	Field	Type	Reset	Description
15:0	SRC[15:0]	R/W	8000h	Sample rate converter. These registers program the sample rate converter. See the *Sample Rate Converter* section for details of operation. 8000h = SRC function is disabled

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The ADS1288 is a high-resolution ADC designed for low-power seismic data acquisition equipment. Optimizing performance requires special attention to the support circuitry and printed-circuit board (PCB) layout. As much as possible, locate noisy circuit components (such as microcontrollers, oscillators, switching regulators, and so forth) away from the ADC input circuit components, reference voltage, and the clock signal.

9.2 Typical Application

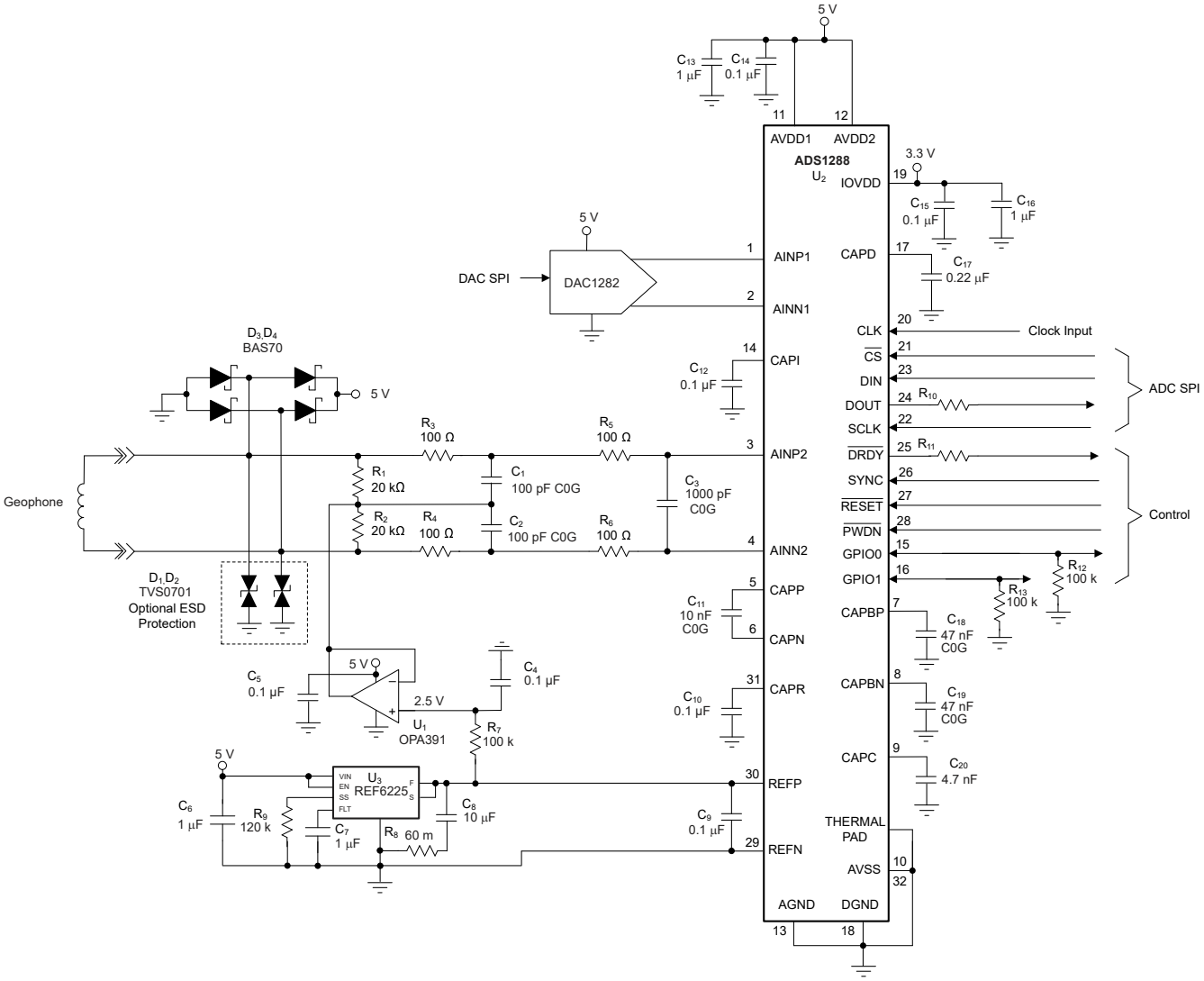


図 9-1. Geophone Input Application Example

9.2.1 Design Requirements

図 9-1 depicts a typical application of a geophone input circuit. The application shows the ADC operating with a 5V power supply and a 2.5V level-shift voltage applied to the ADC inputs. The goal of this evaluation is to analyze the effect of noise resulting from source resistance. The source resistance is the sum of the series input resistors and the geophone output resistance.

9.2.2 Detailed Design Procedure

Referring to 図 9-1, Schottky diodes (BAS70 or equivalent) protect the ADC inputs from voltage overloads. The ADC inputs are protected from ESD events by the optional ESD protection diodes (TVS0701). The geophone signal is level-shifted to mid-supply by driving the input termination resistors (R_1 and R_2) common point to 2.5V. The level-shift voltage is derived from the reference voltage and is buffered by the OPA391 op amp. The input termination resistors also provide the input bias current return path for the ADC inputs.

The input signal is filtered to reduce out-of-band noise. The filter is comprised of common-mode and differential sections. The common-mode section filters noise common to both inputs, consisting of R_3, R_4, C_1, and C_2. The differential section filters differential noise, consisting of R_3 through R_6 and C_3. The resistor values are kept low to reduce thermal noise.

The REF6225 provides the 2.5V reference voltage.

The AVDD1 power-supply voltage is shown at 5V, with AVSS connected to AGND. The AVDD2 voltage is also 5V to simplify the power-supply requirements. IOVDD is shown at 3.3V. If IOVDD = 1.8V, connect the CAPD pin (pin 19) to IOVDD.

Besides the power-supply pins, place additional capacitors at certain pins. Capacitors are required between CAPP – CAPN, REFP – REFN, and at the CAPBP, CAPBN, CAPI, CAPR, CAPC, and CAPD pins with the capacitance values given in 図 9-1. The CAPP – CAPN, CAPBP, and CAPBN capacitors are C0G type.

The DAC1282 provides a low-distortion signal to test THD performance, and through the DAC1282 dc test mode, test geophone impulse response. Increase the value of the DAC1282 capacitors CAPP and CAPN to 10nF to optimize the ADS1288 THD test performance. See the DAC1282 data sheet for additional circuit details.

9.2.3 Application Curves

表 9-1 lists the effect of geophone source resistance (R_S) and the effect of input current noise to total noise performance. Geophone R_S = 1000Ω, 5000Ω, and two values of input current noise taken from the input current noise distribution of 図 9-2. Input current noise values = 1.5pA/√Hz and 3pA/√Hz are evaluated. Geophone R_S thermal noise, current noise × R_S, and ADC input-referred noise are summed to derive total noise.

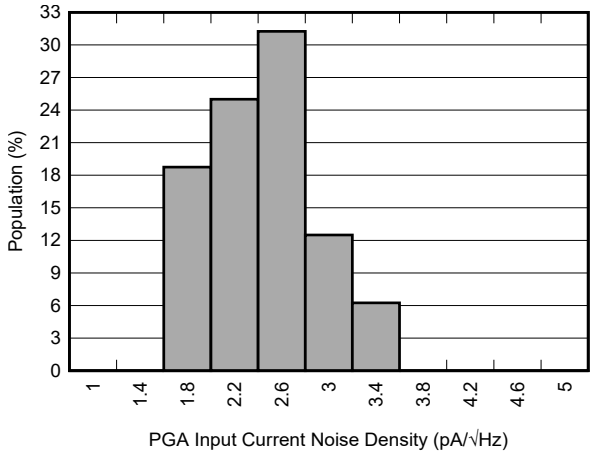


図 9-2. PGA Input Current Noise Distribution

表 9-1. Total Noise

R_S (Ω)	GAIN	R_S NOISE (μV)	i_n NOISE (pA/√Hz)	$i_n \times R_S$ NOISE (μV)	ADC NOISE (μV)	TOTAL NOISE (μV)
1000	1	0.06	1.5	0.024	1.4	1.4
		0.06	3	0.048		1.4
	16	0.06	1.5	0.024	0.28	0.29
		0.06	3	0.048		0.29
5000	1	0.13	1.5	0.11	1.4	1.41
		0.13	3	0.22		1.41
	16	0.13	1.5	0.11	0.28	0.33
		0.13	3	0.22		0.38

The analysis data is over a 206Hz noise bandwidth (f_{DATA} = 500SPS). The data shows the greatest of the total noise increase compared to ADC noise alone is with 5000Ω geophone source resistance, PGA gain = 16, and i_n = 3pA/√Hz. The 1000Ω geophone source resistance shows an insignificant noise increase under the same condition.

9.3 Power Supply Recommendations

The ADC has four power supplies: AVDD1, AVDD2, AVSS, and IOVDD. Among the power-supply options, the number of power supplies can be reduced to a single 3.3V supply used for AVDD1, AVDD2, and IOVDD, with AVSS connected to ground. Be aware that 3.3V operation requires using the buffer for gain = 1.

The power supplies can be sequenced in any order. The ADC is held in reset until the power supplies have crossed the retrospective power-on voltage thresholds and the clock signal is applied (see 図 5-8 for details of the voltage thresholds).

9.3.1 Analog Power Supplies

The ADC has three analog power supplies, AVDD1, AVDD2, and AVSS, all of which must be well regulated and free from switching power-supply noise (voltage ripple < 1mV). The AVDD1 power-supply voltage is relative to AVSS and powers the PGA and buffer. AVSS is the negative power supply. The ADC can be configured for single-supply operation with AVDD1 = 5V or 3.3V with AVSS connected to ground. Because the minimum voltage of AVDD1 to AGND = 2.375V, dual-supply operation is only possible when AVDD1 – AVSS = ±2.5V. Single-power supply operation requires a level-shift voltage at the geophone input through the input termination resistors. The level-shift voltage is typically equal to AVDD1 / 2. Bypass AVDD1 with 1μF and 0.1μF parallel capacitors to AVSS.

The AVDD2 power-supply powers the modulator. To simplify system power management, AVDD2 can be connected to AVDD1, regardless whether AVDD1 and AVSS are configured for single- or dual-supply operation (AVDD2 voltage range is 2.375V to 5.25V with respect to AGND). Bypass AVDD2 with 1μF and 0.1μF parallel capacitors to AGND.

9.3.2 Digital Power Supply

IOVDD is the digital power supply. IOVDD is the digital pin I/O voltage and also powers the digital core by a 1.8V low-dropout regulator (LDO). The LDO output is the CAPD pin and is bypassed with a 0.22μF capacitor to DGND. Do not externally load the CAPD voltage output. Bypass the IOVDD pin with 1μF and 0.1μF parallel capacitors to DGND.

If IOVDD is in the range of 1.65V to 1.95V, tie the IOVDD and CAPD pins together. This connection forces the internal LDO off, thereby the IOVDD voltage now directly powers the digital core. Pay close attention to the absolute maximum voltage rating of IOVDD driving the CAPD pin to avoid damaging the device.

9.3.3 Grounds

The ADC has two ground pins, AGND and DGND. Connect the AGND and DGND pins together at the ADC to a single ground plane using short direct connections.

9.3.4 Thermal Pad

The thermal pad does not carry device current but must be soldered and connected to the most negative power-supply voltage (AVSS). Because of the low power dissipation, PCB thermal vias can be omitted to provide space for bottom layer components under the device.

9.4 Layout

9.4.1 Layout Guidelines

図 9-3 shows the layout of the geophone input application example of 図 9-1. In most cases, a single unbroken ground plane connecting the grounds of the analog and digital components is preferred. A four-layer PCB is used, with the inner layers dedicated for ground and power-supply planes. Low resistance power-supply planes are necessary to maintain THD performance.

Connect the REFN pin of the ADC directly to the ground terminal of the voltage reference to avoid ground noise coupling. Similarly, avoid ground noise between the tie-points of termination resistors R_1 and R_2 by connecting the resistors together first, then connect to ground (dual-supply operation).

Place the smaller of the parallel power-supply bypass capacitors closest to the device supply pins. The thermal pad of the package connects to the most negative power-supply voltage (AVSS). 図 9-3 shows single-supply operation, with AVSS tied to AGND. In this case, the thermal pad connects to AGND. For dual-supply operation, connect the thermal pad to AVSS.

9.4.2 Layout Example

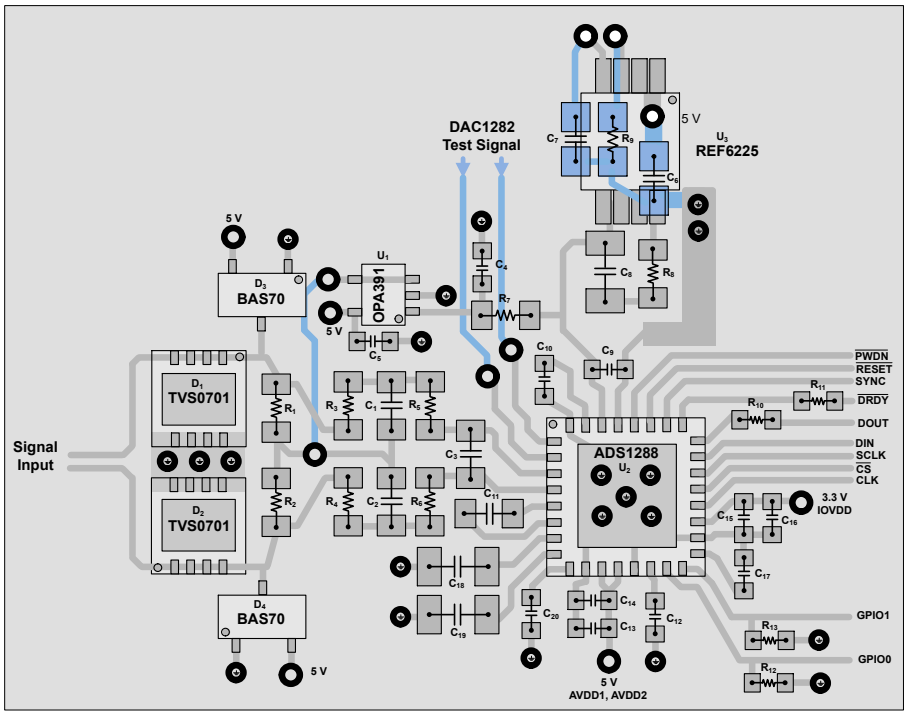


図 9-3. Example Layout

10 Device and Documentation Support

10.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

10.2 サポート・リソース

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10.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
February 2024	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS1288IRHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 1288	Samples
ADS1288IRHBT	ACTIVE	VQFN	RHB	32	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 1288	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

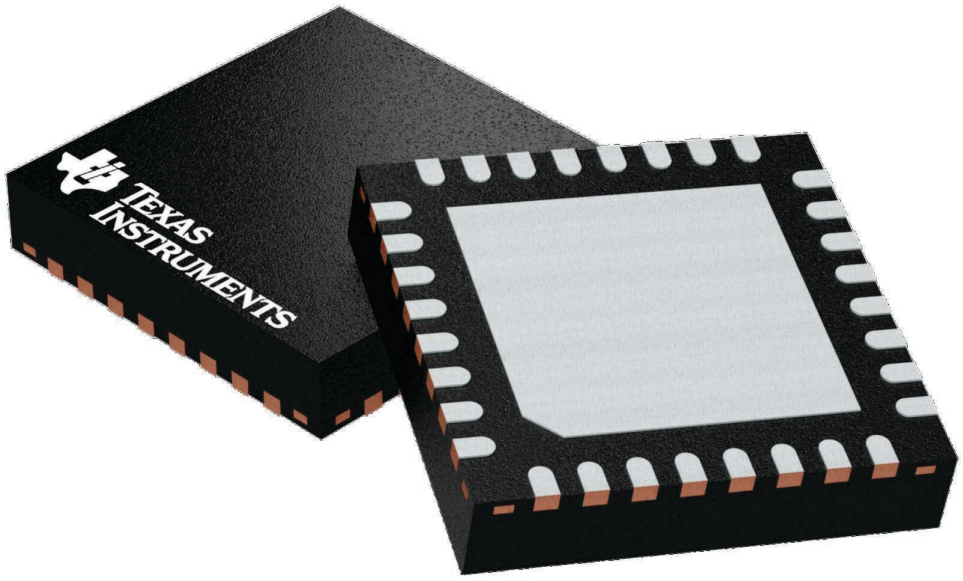
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

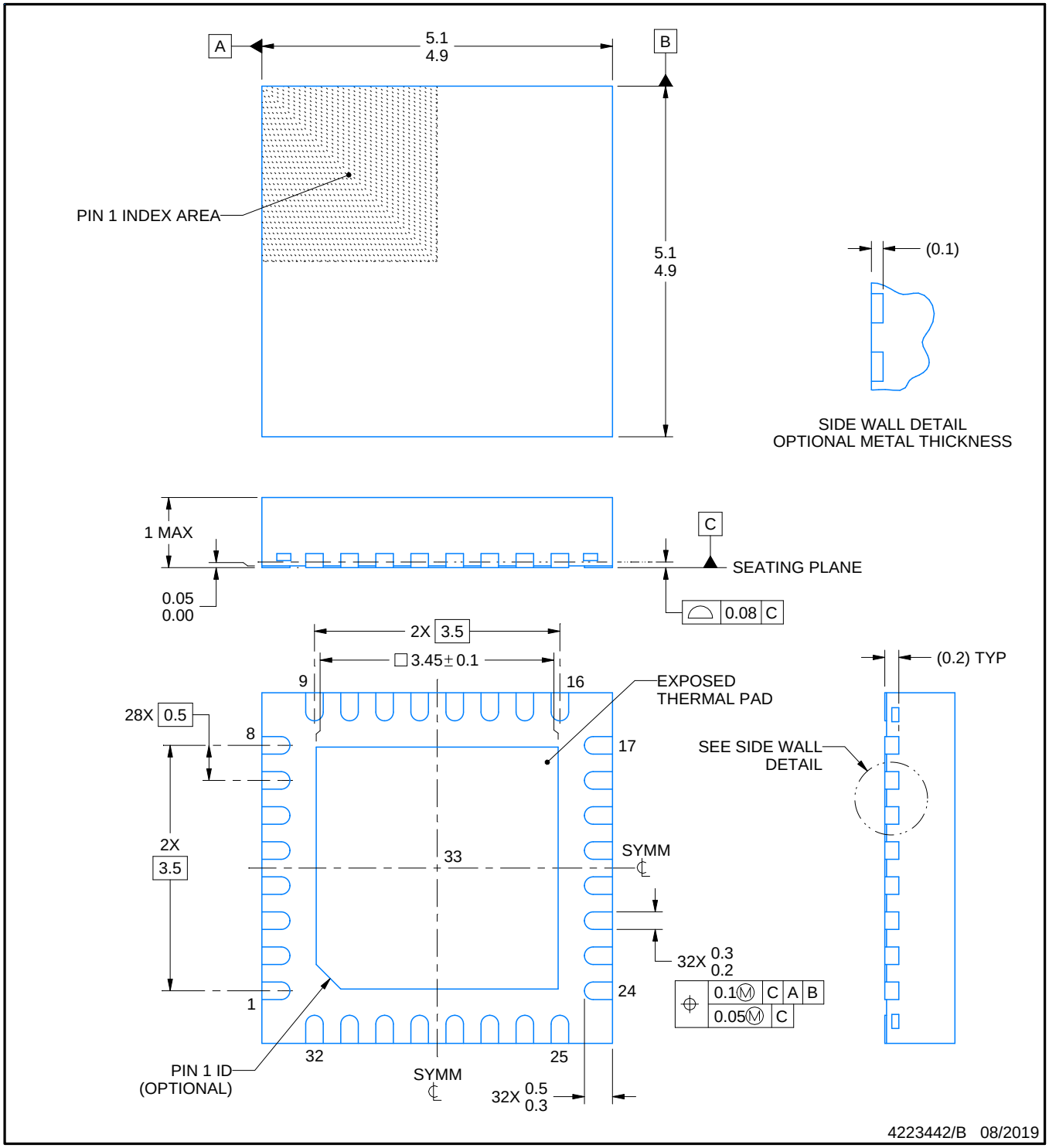
4224745/A

RHB0032E

PACKAGE OUTLINE

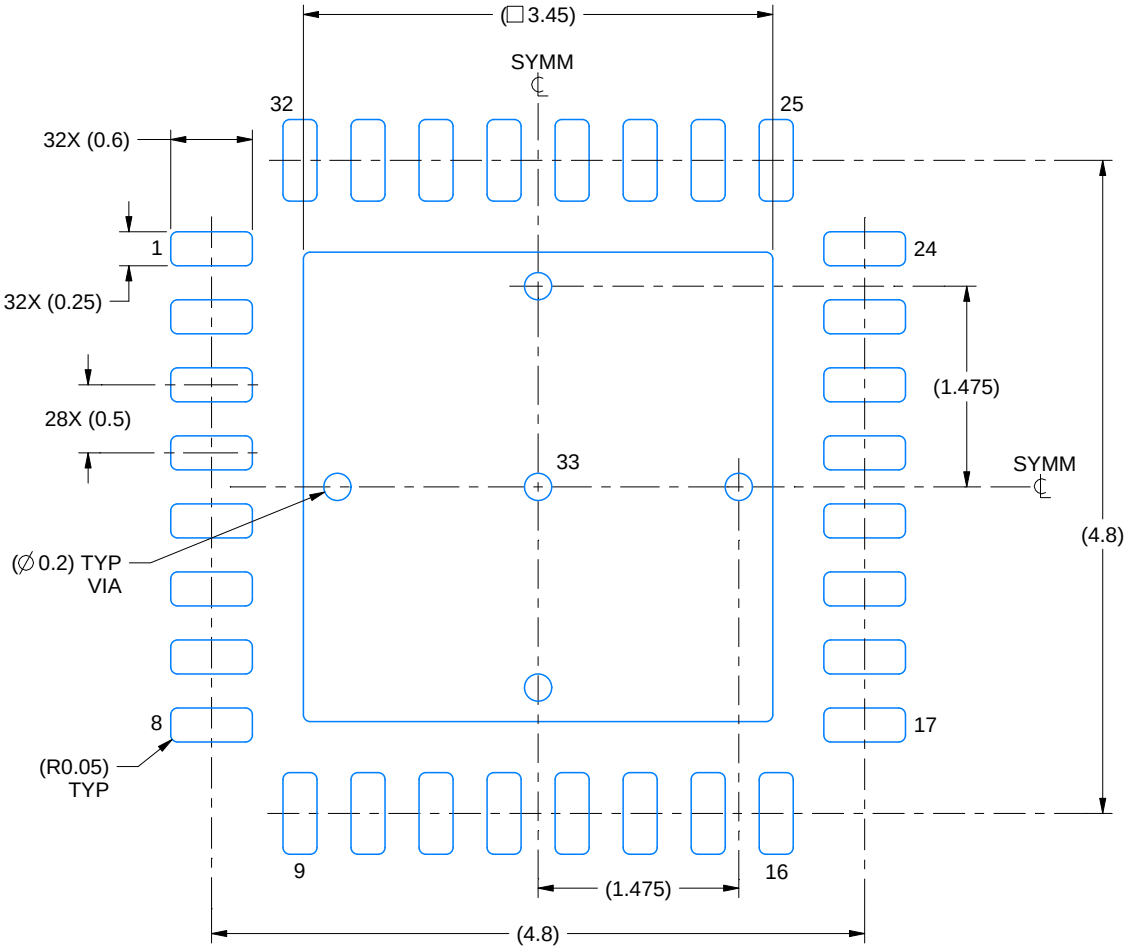
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

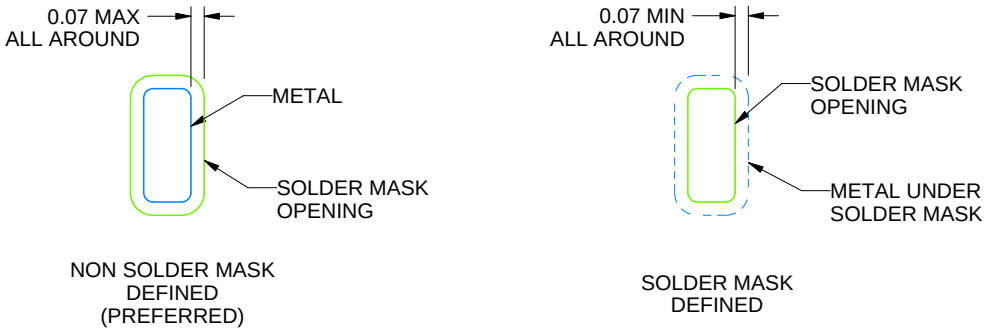


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X



SOLDER MASK DETAILS

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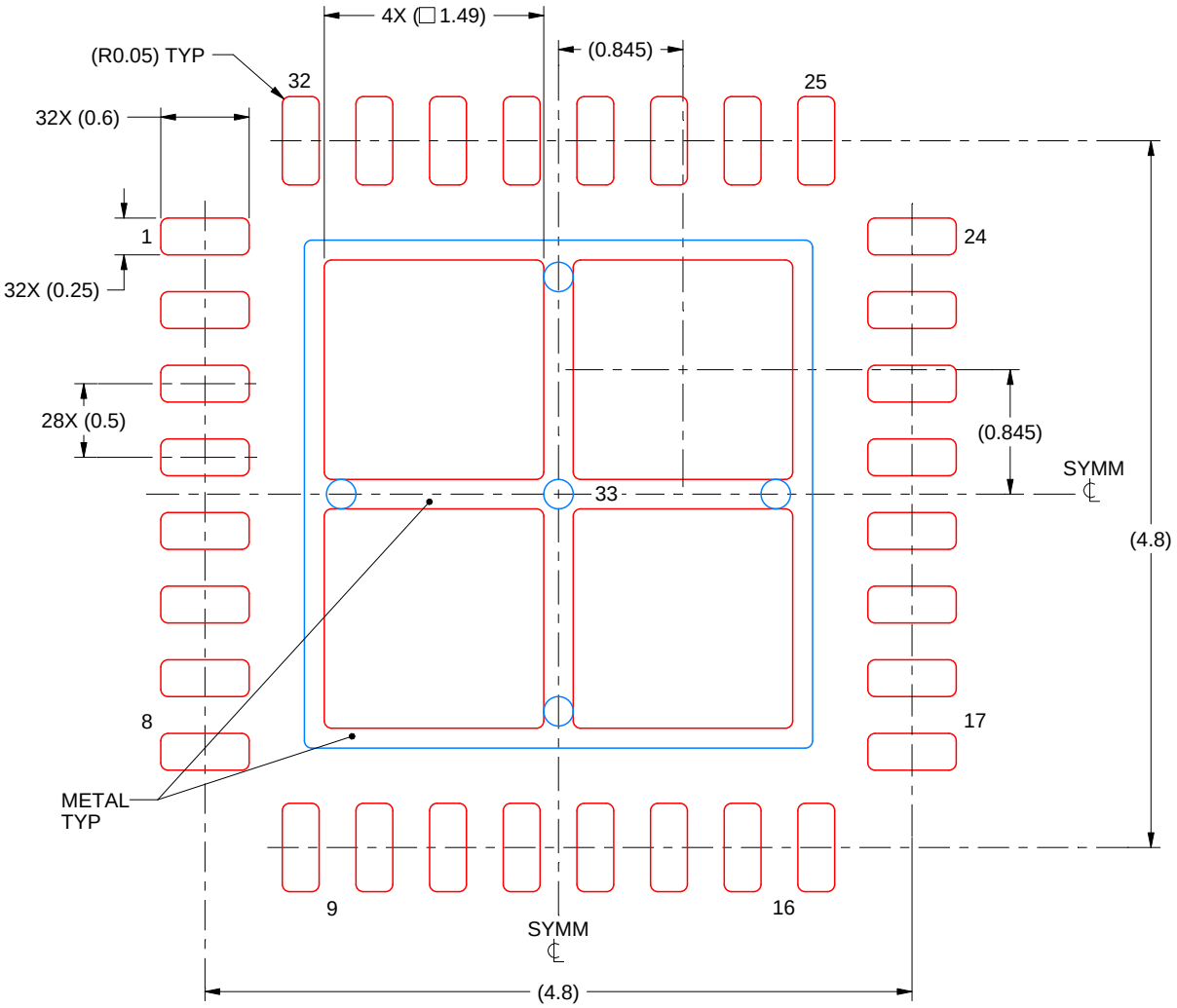
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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