参考資料

ADS130B02-Q1 車載用、2 チャネル、32kSPS、同時サンプリング、16 ビット、デルタ･シグマ ADC

1 特長

- 車載アプリケーション用に AEC-Q100 認定取得済み：
  - 温度グレード 1：-40℃～+125℃、T_A
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 2 同時サンプリング、差動入力 ADC
- データ･レートをプログラム可能：最大 32kSPS
- ゲインをプログラム可能：最大 128
- グローバル･チョップ･モードにより、温度と時間の間のオフセット･ドリフトを除去
- センサと直接接続できる高インピーダンス･アナログ入力
- 内蔵された負チャージ･ポンプにより、グランドより低い入力信号に対応が可能
- チャネル間のクロストーク：–120dB
- 低ドリフトの内部リファレンス：1.2V
- 高精度内部発振回路
- 通信とレジスタ･マップでの CRC
- アナログおよびデジタル電源：2.7V～3.6V
- 低消費電力：3.3V AVDD および DVDD で 3mW

2 アプリケーション

- EV 充電ステーション
  - DC e メーター
- バッテリ管理システム (BMS)：
  - 電流シャント測定
  - 外付けの分圧抵抗を使用した電圧測定
  - サーミスタまたはアナログ出力温度センサを使用した温度測定
- エネルギー･ストレージ･システム (ESS)

3 概要

ADS130B02-Q1 は、two チャネルの同時サンプリング、16 ビット、デルタ･シグマ (ΔΣ) アナログ / デジタル･コンバータ (ADC) です。ダイナミック･レンジが広く、低消費電力であり、バッファ付きアナログ入力を備えているため、バッテリ管理システム (BMS) に非常に適しています。ADC 入力は、双方向のバッテリ電流測定用のシャント抵抗、高電圧測定用の分圧抵抗ネットワーク、または温度センサ (サーミスタやアナログ出力温度センサなど) に直接接続できます。

ADC チャネルは、センサ入力に応じて個別に構成可能です。低ノイズのプログラマブル･ゲイン･アンプ (PGA) により、1～128 の範囲のゲインで低レベルの信号を増幅できます。このデバイスには、温度と時間の間のオフセット･ドリフトを除去するためのグローバル･チョップ･モードが搭載されています。

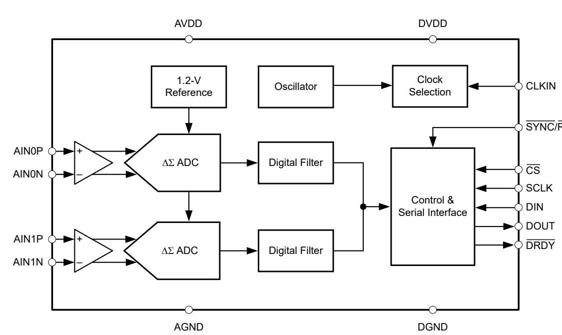
本デバイスには低ドリフトの 1.2V 基準電圧と高精度の発振器が内蔵されているため、プリント基板 (PCB) の面積を削減できます。データ入力、データ出力、レジスタ･マップでの任意の巡回冗長性検査 (CRC) は通信の整合性を維持します。

この完全なアナログ･フロントエンド (AFE) ソリューションは、20 ピン TSSOP パッケージで供給され、車載用温度範囲の –40℃～+125℃で動作が規定されています。

製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
ADS130B02-Q1	TSSOP (20)	6.50mm × 4.40mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



ブロック概略図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
November 2021	*	Initial Release

5 Pin Configuration and Functions

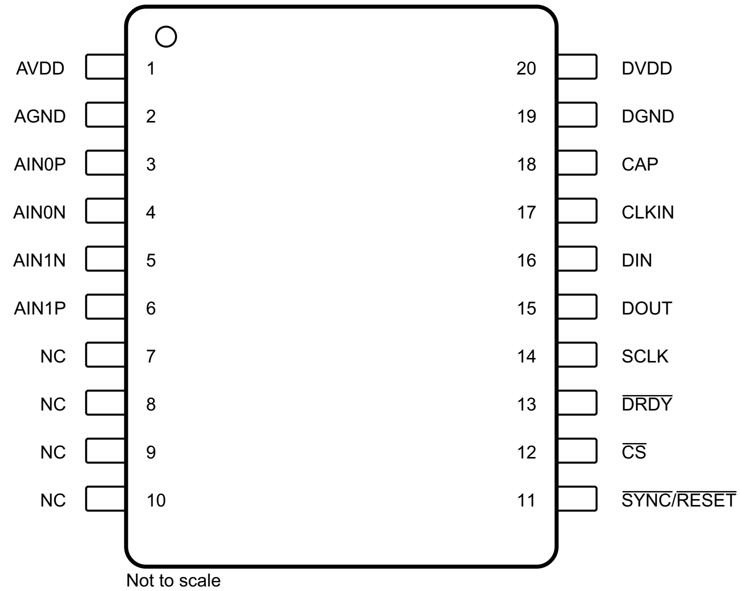


図 5-1. PW Package, 20-Pin TSSOP (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION(1)
NAME	NO.		
AGND	2	Supply	Analog ground
AIN0N	4	Analog input	Negative analog input 0
AIN0P	3	Analog input	Positive analog input 0
AIN1N	5	Analog input	Negative analog input 1
AIN1P	6	Analog input	Positive analog input 1
AVDD	1	Supply	Analog supply. Connect a 1-µF capacitor to AGND.
CAP	18	Analog output	Digital low-dropout (LDO) regulator output. Connect a 220-nF capacitor to DGND.
CLKIN	17	Digital input	External clock input
$\overline{CS}$	12	Digital input	Chip select; active low
DGND	19	Supply	Digital ground
DIN	16	Digital input	Serial data input
DOUT	15	Digital output	Serial data output
$\overline{DRDY}$	13	Digital output	Data ready; active low
DVDD	20	Supply	Digital I/O supply. Connect a 1-µF capacitor to DGND.
NC	7, 8, 9, 10	-	Leave unconnected or connect to AGND
SCLK	14	Digital input	Serial data clock
$\overline{SYNC/RESET}$	11	Digital input	Conversion synchronization or system reset; active low

(1) See the *Unused Inputs and Outputs* section for details on how to connect unused pins.

6 Specifications

6.1 Absolute Maximum Ratings

See [(1)]

		MIN	MAX	UNIT
Power-supply voltage	AVDD to AGND	–0.3	3.9	V
	AGND to DGND	–0.3	0.3	
	DVDD to DGND	–0.3	3.9	
	CAP to DGND	–0.3	2.2	
Analog input voltage	AINxP, AINxN	AGND – 1.6	AVDD + 0.3	V
Digital input voltage	$\overline{CS}$, CLKIN, DIN, SCLK, $\overline{SYNC/RESET}$	DGND – 0.3	DVDD + 0.3	V
Input current	Continuous, all pins except power-supply pins	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–60	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional – this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[(1)] HBM ESD classification level 2		±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD classification level C4B	Corner pins	±750	
			All other non-corner pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
	Analog power supply	AVDD to AGND	2.7	3.3	3.6	V
		AGND to DGND	–0.3	0	0.3	
	Digital power supply	DVDD to DGND	2.7	3.3	3.6	V
ANALOG INPUTS(1)						
V_{AINxP}, V_{AINxN}	Absolute input voltage	Gain = 1, 2	AGND – 0.1		AVDD – 1.2	V
		Gain = 4, 8, 16, 32, 64, 128	AGND – 0.3		AVDD – 2.4	
V_{IN}	Differential input voltage	$V_{IN} = V_{AINxP} - V_{AINxN}$	$-V_{REF}$ / Gain		V_{REF} / Gain	V
EXTERNAL CLOCK SOURCE(2)						
f_{CLKIN}	External clock frequency	High-resolution mode	0.3	8.192	8.2	MHz
		Low-power mode	0.3	4.096	4.15	
		Very-low-power mode	0.3	2.048	2.08	
	Duty cycle		40%	50%	60%	
DIGITAL INPUTS						
	Input voltage		DGND		DVDD	V
TEMPERATURE						
T_A	Operating ambient temperature		–40		125	°C

(1) The subscript "x" signifies the channel. For example, the positive analog input of channel 0 is named AIN0P. See the *Pin Configuration and Functions* section for the pin names.
(2) An external clock is not required when the internal oscillator is used.

6.4 Thermal Information

THERMAL METRIC(1)		ADS130B02-Q1 PW (TSSOP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	91.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	31.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	42.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at AVDD = 3.3 V, DVDD = 3.3 V, external clock, f_{CLKIN} = 8.192 MHz, high-resolution mode, all channels, all gains, data rate = 4 kSPS, all channels enabled, and global-chop mode disabled (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
Z_{in}	Differential input impedance	Global-chop disabled		25		MΩ
		Global-chop enabled		300		MΩ
		All power modes, all data rates		See 表 8-2		
	Absolute input current	Global-chop disabled, V_{AINxP} = V_{AINxN} = 0 V		±1		nA
		Global-chop enabled, V_{AINxP} = V_{AINxN} = 0 V		±1		nA
	Differential input current	Global-chop disabled, V_{AINxP} = V_{AINxN} = 0 V		±50		pA
		Global-chop enabled, V_{AINxP} = V_{AINxN} = 0 V		±30		pA
ADC CHARACTERISTICS						
	Resolution		24			Bits
	Gain settings			1, 2, 4, 8, 16, 32, 64, 128		
f_{DATA}	Data rate	High-resolution mode, f_{CLKIN} = 8.192 MHz	250		32k	SPS
		Low-power mode, f_{CLKIN} = 4.096 MHz	125		16k	SPS
		Very-low-power mode, f_{CLKIN} = 2.048 MHz	62.5		8k	SPS
ADC PERFORMANCE						
INL	Integral nonlinearity (best fit)	Differential-ended input		10		ppm of FSR
	Offset error (input referred)	Global-chop disabled	–800	±200	800	µV
		Global-chop enabled[(3)]	–4	±0.4	4	µV
	Offset drift	Global-chop disabled, gain = 1 to 4		100	500	nV/°C
		Global-chop disabled, gain = 8 to 128		50	200	nV/°C
		Global-chop enabled		10	30	nV/°C
	Offset error long-term drift	1000 hours at T_A = 85°C, global-chop disabled		0.8		µV
		1000 hours at T_A = 85°C, global-chop enabled		0.25		µV
	Gain error	Including error of internal voltage reference, T_A = 25°C	–0.7%	±0.2%	0.7%	
	Gain drift	Including drift of internal voltage reference, T_A = –40°C to +85°C, gain = 1 to 4		8	30	ppm/°C
		Including drift of internal voltage reference, T_A = –40°C to +85°C, gain = 8 to 128		7	25	ppm/°C
		Including drift of internal voltage reference, T_A = –40°C to +125°C		13	40	ppm/°C
	Gain error long-term drift	1000 hours at T_A = 85°C, gain = 1, including drift of internal voltage reference		250		ppm
CMRR	Common-mode rejection ratio	At dc, global-chop disabled, gain = 1		96		dB
		At dc, global-chop enabled, gain = 1		128		dB
		f_{CM} = 50 Hz or 60 Hz, global-chop disabled, gain = 1		89		dB
		f_{CM} = 50 Hz or 60 Hz, global-chop enabled, gain = 1		106		dB

6.5 Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at AVDD = 3.3 V, DVDD = 3.3 V, external clock, f_{CLKIN} = 8.192 MHz, high-resolution mode, all channels, all gains, data rate = 4 kSPS, all channels enabled, and global-chop mode disabled (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSRR	Power-supply rejection ratio	AVDD at dc, global-chop disabled, gain = 1		81		dB
		AVDD at dc, global-chop enabled, gain = 1		116		
		DVDD at dc, global-chop disabled, gain = 1		109		
		DVDD at dc, global-chop enabled, gain = 1		117		
	Input-referred noise			See 表 7-1		
	Crosstalk	f_{IN} = 50 Hz or 60 Hz		–120		dB
INTERNAL VOLTAGE REFERENCE						
V_{REF}	Internal reference voltage			1.2		V
INTERNAL OSCILLATOR						
f_{OSC}	Frequency			8.192		MHz
	Accuracy		–5%	±0.5%	2.5%	
	Frequency long-term drift	1000 hours at T_A = 85°C		0.2%		
DIGITAL INPUTS/OUTPUTS						
V_{IL}	Logic input level, low		DGND		0.2 DVDD	V
V_{IH}	Logic input level, high		0.8 DVDD		DVDD	V
V_{OL}	Logic output level, low	I_{OL} = –1 mA			0.2 DVDD	V
V_{OH}	Logic output level, high	I_{OH} = 1 mA	0.8 DVDD			V
I_{IN}	Input current	DGND < $V_{Digital\ Input}$ < DVDD	–1		1	µA
POWER SUPPLY						
I_{AVDD}	Analog supply current	High-resolution mode, gain = 1, 2		2.9	3.6	mA
		High-resolution mode, gain = 4 to 128		3.3	4.2	
		Low-power mode, gain = 1, 2		1.5	2	
		Low-power mode, gain = 4 to 128		1.7		
		Very-low-power mode, gain = 1, 2		0.8	1.2	
		Very-low-power mode, gain = 4 to 128		0.9		
		Standby mode		0.4		µA
		Internal oscillator		140		
I_{DVDD}	Digital supply current(1)	High-resolution mode		0.3	0.4	mA
		Low-power mode		0.15	0.2	
		Very-low-power mode		0.1	0.14	
		Standby mode(2)		1.2		µA
P_D	Power dissipation	High-resolution mode, gain = 1, 2		10.6	13.2	mW
		High-resolution mode, gain = 4 to 128		11.9	15.2	
		Low-power mode, gain = 1, 2		5.4	7.3	
		Very-low-power mode, gain = 1, 2		3	4.4	

(1) Currents measured with SPI idle.
(2) External clock stopped.
(3) Offset error may be limited by LSB size in certain OSR and gain configurations.

6.6 Timing Requirements

over operating ambient temperature range, and DOUT load = 20 pF || 100 kΩ (unless otherwise noted)

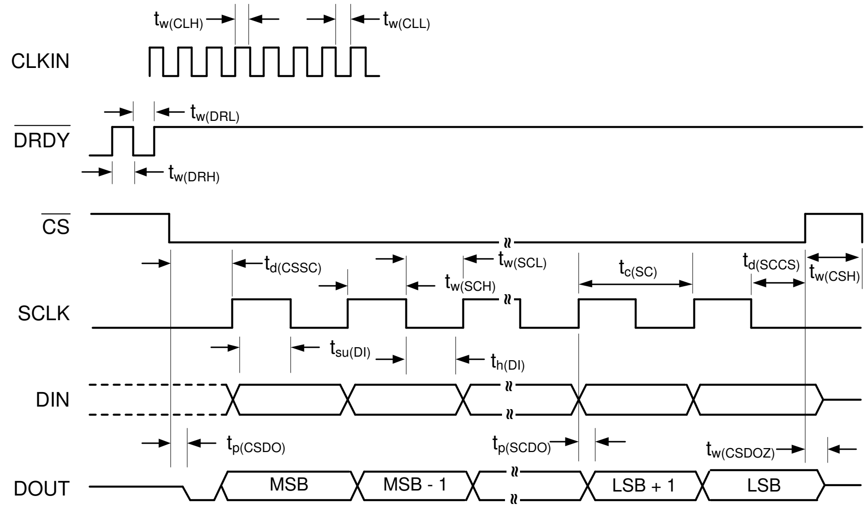
		MIN	MAX	UNIT
2.7 V ≤ DVDD ≤ 3.6 V				
$t_{w(CLL)}$	Pulse duration, CLKIN low	49		ns
$t_{w(CLH)}$	Pulse duration, CLKIN high	49		ns
$t_{c(SC)}$	SCLK period	40		ns
$t_{w(SCL)}$	Pulse duration, SCLK low	20		ns
$t_{w(SCH)}$	Pulse duration, SCLK high	20		ns
$t_{w(CSH)}$	Pulse duration, $\overline{CS}$ high	15		ns
$t_{d(CSSC)}$	Delay time, first SCLK rising edge after $\overline{CS}$ falling edge	16		ns
$t_{d(SCCS)}$	Delay time, $\overline{CS}$ rising edge after final SCLK falling edge	10		ns
$t_{su(DI)}$	Setup time, DIN valid before SCLK falling edge	5		ns
$t_{h(DI)}$	Hold time, DIN valid after SCLK falling edge	8		ns
$t_{su(SY)}$	Setup time, $\overline{SYNC}/\overline{RESET}$ valid before CLKIN rising edge	10		ns
$t_{w(SYL)}$	Pulse duration, $\overline{SYNC}/\overline{RESET}$ low for synchronization	1	2047	t_{MCLK}
$t_{w(RSL)}$	Pulse duration, $\overline{SYNC}/\overline{RESET}$ low to generate device reset	2048		t_{MCLK}

6.7 Switching Characteristics

over operating ambient temperature range, and DOUT load = 20 pF || 100 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
2.7 V ≤ DVDD ≤ 3.6 V						
$t_{p(CSDO)}$	Propagation delay time, $\overline{CS}$ falling edge to DOUT driven				50	ns
$t_{p(SCDO)}$	Progapation delay time, SCLK rising edge to valid new DOUT				20	ns
$t_{p(CSDOZ)}$	Propagation delay time, $\overline{CS}$ rising edge to DOUT high impedance				75	ns
$t_{w(DRH)}$	Pulse duration, $\overline{DRDY}$ high			4		t_{MCLK}
$t_{w(DRL)}$	Pulse duration, $\overline{DRDY}$ low			4		t_{MCLK}
	SPI timeout		32768			t_{MCLK}
t_{POR}	Power-on-reset time	Measured from supplies at 90% to first $\overline{DRDY}$ rising edge		250		µs
t_{REGACQ}	Register default acquisition time			5		µs

6.8 Timing Diagrams



SPI settings are CPOL = 0 and CPHA = 1. $\overline{CS}$ transitions must take place when SCLK is low.

図 6-1. SPI Timing Diagram

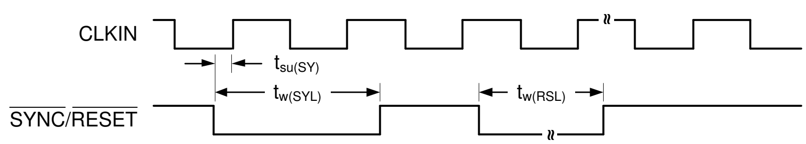


図 6-2. $\overline{SYNC}/\overline{RESET}$ Timing Requirements

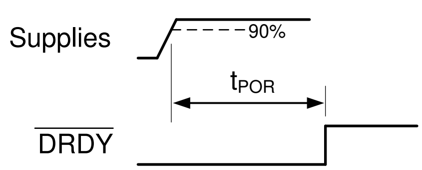
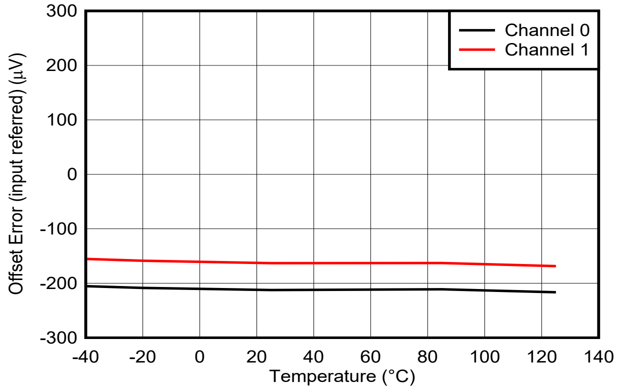


図 6-3. Power-On-Reset Timing

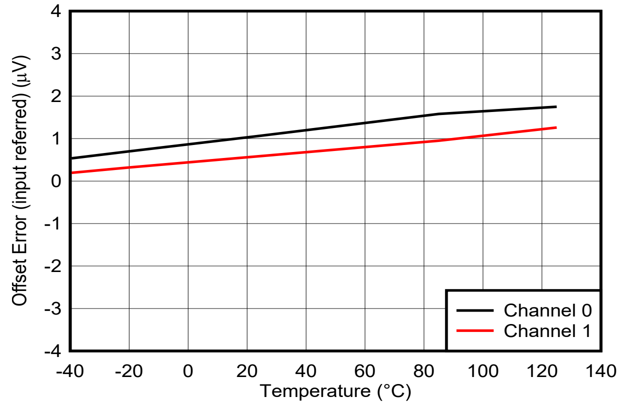
6.9 Typical Characteristics

at T_A = 25°C, AVDD = 3.3 V, DVDD = 3.3 V, f_{CLKIN} = 8.192 MHz, data rate = 4 kSPS, and gain = 1 (unless otherwise noted)



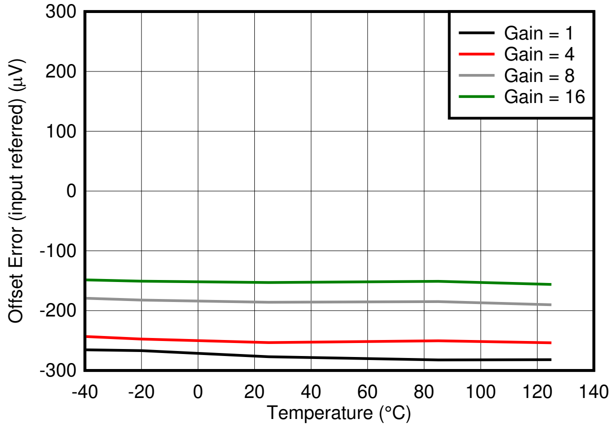
Gain = 8, global-chop mode disabled

図 6-4. Offset Error vs Temperature



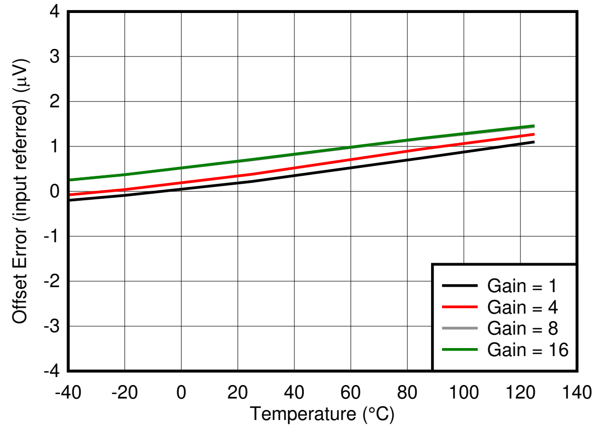
Gain = 8, global-chop mode enabled

図 6-5. Offset Error vs Temperature



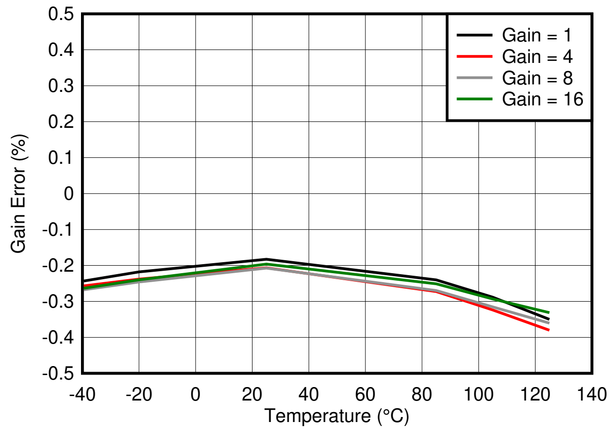
Global-chop mode disabled

図 6-6. Offset Error vs Temperature



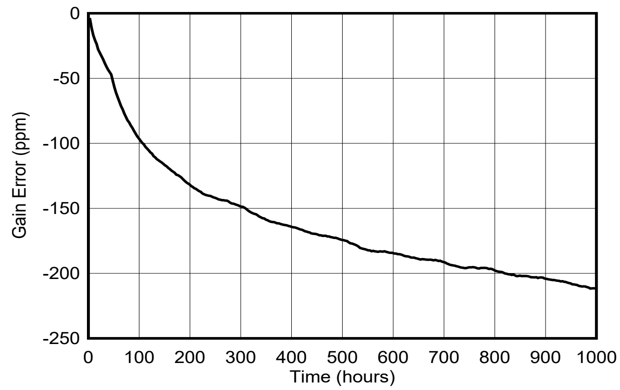
Global-chop mode enabled

図 6-7. Offset Error vs Temperature



Including error of internal voltage reference

図 6-8. Gain Error vs Temperature



Gain = 1, including error of internal voltage reference

図 6-9. Gain Error Long-Term Drift

6.9 Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3.3 V, DVDD = 3.3 V, f_{CLKIN} = 8.192 MHz, data rate = 4 kSPS, and gain = 1 (unless otherwise noted)

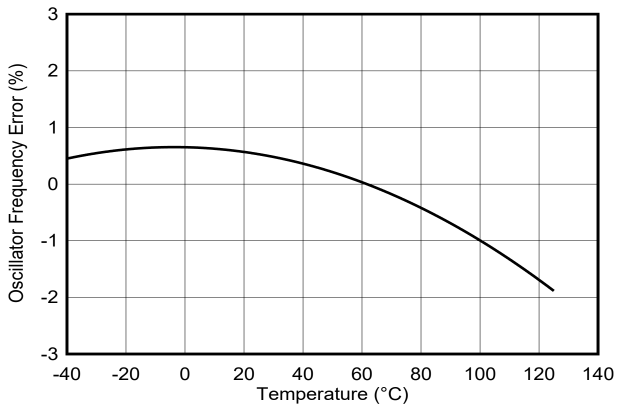
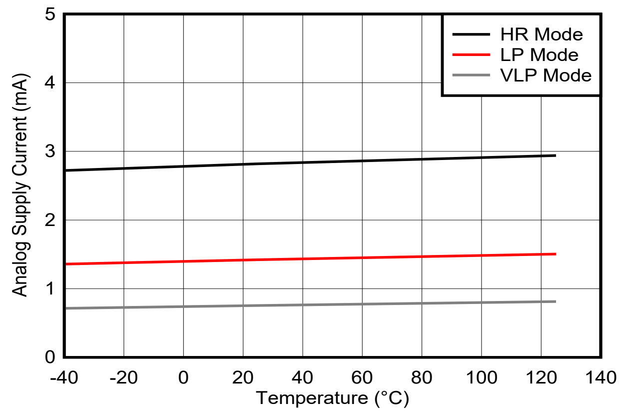
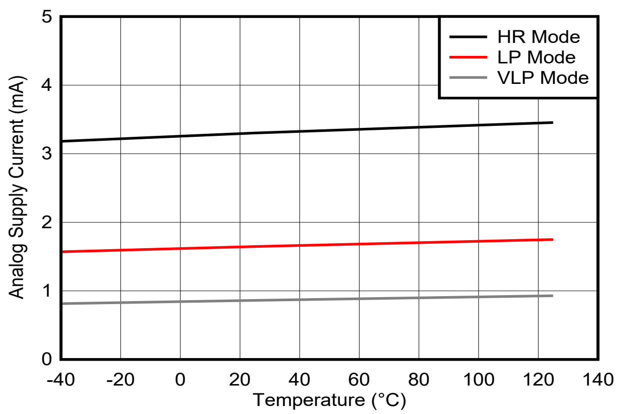


図 6-10. Oscillator Frequency Error vs Temperature



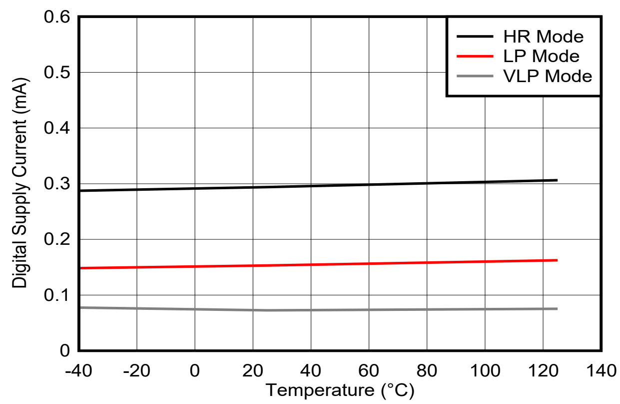
Gain = 1, OSR = 1024, all two ADC channels enabled

図 6-11. Analog Supply Current vs Temperature



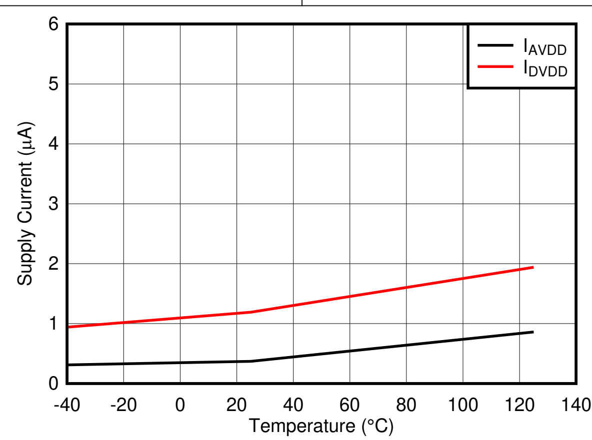
Gain = 8, OSR = 1024, all two ADC channels enabled

図 6-12. Analog Supply Current vs Temperature



OSR = 1024

図 6-13. Digital Supply Current vs Temperature



Standby mode

図 6-14. Supply Current vs Temperature

7 Parameter Measurement Information

7.1 Noise Measurements

Adjust the data rate and gain to optimize the ADS130B02-Q1 noise performance. When averaging is increased by reducing the data rate, noise drops correspondingly. 表 7-1 summarizes the ADS130B02-Q1 noise performance using the 1.2-V internal reference and a 3.3-V analog power supply. The data are representative of typical noise performance at T_A = 25°C when f_{MCLK} = 8.192 MHz. The modulator clock frequency f_{MOD} = f_{MCLK} / 2. The data shown are typical input-referred noise results with the analog inputs shorted together and taking an average of multiple readings across all channels. A minimum 1 second of consecutive readings are used to calculate the RMS noise for each reading. 表 7-2 shows the effective resolution calculated from the noise data. 式 1 calculates effective resolution. In each case, V_{REF} corresponds to the internal 1.2-V reference. In global-chop mode, noise is improved by a factor of $\sqrt{2}$.

The noise performance scales with the oversampling rate (OSR) and gain settings, but is independent from the configured power mode. Thus, the device exhibits the same noise performance in different power modes when selecting the same OSR and gain settings. However, the data rate at the OSR settings scales based on the main clock frequency for the different power modes.

$$\text{Effective Resolution} = \log_2\left(\frac{2 \times V_{REF}}{\text{Gain} \times V_{RMS}}\right) \tag{1}$$

表 7-1. Noise (μV_{RMS}) at T_A = 25°C

OSR	DATA RATE (kSPS), f_{MCLK} = 8.192 MHz	GAIN							
		1	2	4	8	16	32	64	128
16384	0.25	36.62	18.31	9.16	4.58	2.29	1.14	0.57	0.42
8192	0.5	36.62	18.31	9.16	4.58	2.29	1.14	0.57	0.58
4096	1	36.62	18.31	9.16	4.58	2.29	1.14	0.80	0.80
2048	2	36.62	18.31	9.16	4.58	2.29	1.14	1.05	1.05
1024	4	36.62	18.31	9.16	4.58	2.29	1.27	1.27	1.27
512	8	36.62	18.31	9.16	4.58	2.29	1.80	1.80	1.80
256	16	36.62	18.31	9.16	4.58	2.56	2.53	2.53	2.53
128	32	36.62	18.31	13.64	4.58	3.73	3.63	3.63	3.63

表 7-2. Effective Resolution at T_A = 25°C

OSR	DATA RATE (kSPS), f_{MCLK} = 8.192 MHz	GAIN							
		1	2	4	8	16	32	64	128
16384	0.25	16	16	16	16	16	16	16	15.4
8192	0.5	16	16	16	16	16	16	16	15.0
4096	1	16	16	16	16	16	16	15.5	14.5
2048	2	16	16	16	16	16	16	15.1	14.1
1024	4	16	16	16	16	16	15.8	14.8	13.8
512	8	16	16	16	16	16	15.3	14.3	13.3
256	16	16	16	16	16	15.8	14.9	13.9	12.9
128	32	16	16	15.4	16	15.3	14.3	13.3	12.3

8 Detailed Description

8.1 Overview

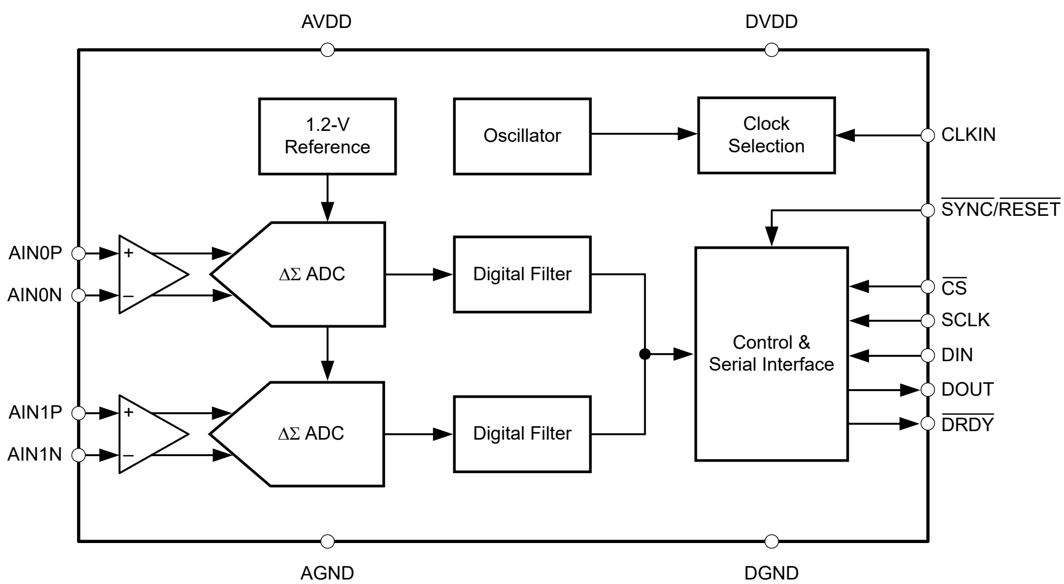
The ADS130B02-Q1 is a low-power, two-channel, simultaneous-sampling, 16-bit, delta-sigma (ΔΣ) analog-to-digital converter (ADC) with a low-drift internal reference voltage. The dynamic range, size, feature set, and power consumption are optimized for cost-sensitive applications requiring simultaneous sampling.

The ADS130B02-Q1 requires both analog and digital supplies. The analog power supply (AVDD – AGND) can operate between 2.7 V and 3.6 V. An integrated negative charge pump allows absolute input voltages as low as 0.3 V below AGND, which enables measurements of input signals varying around ground with a unipolar power supply. The digital power supply (DVDD – DGND) can operate between 2.7 V and 3.6 V. The device features a high input impedance programmable gain amplifier (PGA) with gains up to 128. The ADC receives its reference voltage from an integrated 1.2-V reference. The device allows differential input voltages as large as the reference. Three power-scaling modes allow designers to trade power consumption for noise performance.

Each channel on the ADS130B02-Q1 contains a digital decimation filter that demodulates the output of the ΔΣ modulators. The filter enables data rates as high as 32 kSPS per channel in high-resolution mode. The *Functional Block Diagram* provides a detailed diagram of the ADS130B02-Q1.

The device communicates via a serial peripheral interface (SPI)-compatible interface. Several SPI commands and internal registers control the operation of the ADS130B02-Q1. Other devices can be added to the same SPI bus by adding discrete CS control lines. The SYNC/RESET pin can be used to synchronize conversions between multiple ADS130B02-Q1 devices as well as to maintain synchronization with external events.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input ESD Protection Circuitry

Basic electrostatic discharge (ESD) circuitry protects the ADS130B02-Q1 inputs from ESD and overvoltage events in conjunction with external circuits and assemblies. 図 8-1 shows a simplified representation of the ESD circuit. The protection for input voltages exceeding AVDD can be modeled as a simple diode.

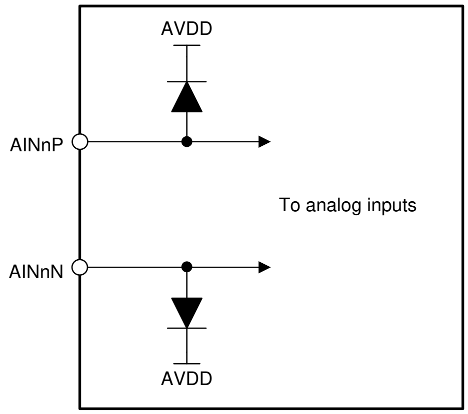


図 8-1. Input ESD Protection Circuitry

The ADS130B02-Q1 has an integrated negative charge pump that allows for input voltages below AGND with a unipolar supply. Consequently, shunt diodes between the inputs and AGND cannot be used to clamp excessive negative input voltages. Instead, the same diode that clamps overvoltage is used to clamp undervoltage at the reverse breakdown voltage. Take care to prevent input voltages or currents from exceeding the limits provided in the *Absolute Maximum Ratings* table.

8.3.2 Input Multiplexer

Each channel of the ADS130B02-Q1 has a dedicated input multiplexer. The multiplexer controls which signals are routed to the ADC channels. Configure the input multiplexer using the MUXn[1:0] bits in the CHn_CFG register. The input multiplexer allows the following inputs to be connected to the ADC channel:

- The analog input pins corresponding to the given channel
- AGND, which is helpful for offset calibration
- Positive dc test signal
- Negative dc test signal

See the *Internal Test Signals* section for more information about the test signals. 図 8-2 shows a diagram of the input multiplexer on the ADS130B02-Q1.

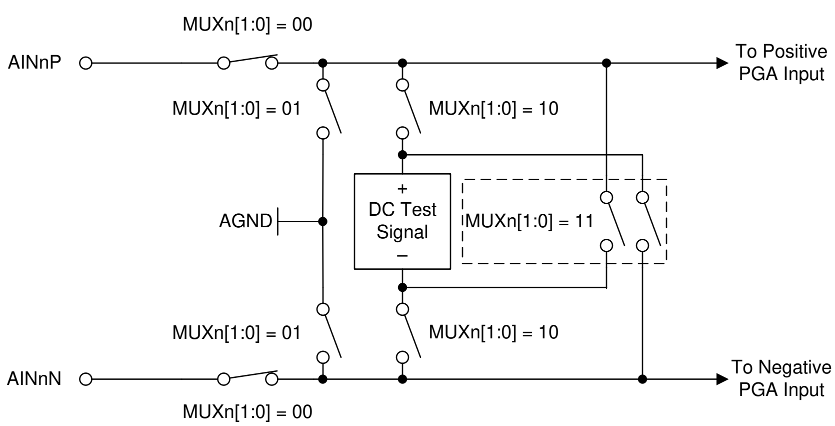


図 8-2. Input Multiplexer

8.3.3 Programmable Gain Amplifier (PGA)

Each channel of the ADS130B02-Q1 features an integrated programmable gain amplifier (PGA) that provides gains of 1, 2, 4, 8, 16, 32, 64, and 128. The gains for all channels are individually controlled by the PGAGAINn bits for each channel in the GAIN register.

Varying the PGA gain scales the differential full-scale input voltage range (FSR) of the ADC. 式 2 describes the relationship between FSR and gain. 式 2 uses the internal reference voltage, 1.2 V, as the scaling factor without accounting for gain error caused by tolerance in the reference voltage.

$$FSR = \pm 1.2\ V / Gain \quad (2)$$

表 8-1 shows the corresponding full-scale ranges for each gain setting.

表 8-1. Full-Scale Range

GAIN SETTING	FSR
1	±1.2 V
2	±600 mV
4	±300 mV
8	±150 mV
16	±75 mV
32	±37.5 mV
64	±18.75 mV
128	±9.375 mV

The input impedance of the ADS130B02-Q1 depends on three factors: the main clock frequency (f_{MCLK}), the selected OSR setting, and the global-chop mode setting. 表 8-2 shows typical input impedance values for f_{MCLK} = 8.192 MHz. The input impedance scales indirectly proportional with the MCLK frequency, which means that at f_{MCLK} = 4.096 MHz, the impedance values in 表 8-2 increase by a factor of 2. Minimize the output impedance of the circuit that drives the ADS130B02-Q1 inputs to obtain the best possible gain error, INL, and distortion performance.

表 8-2. Input Impedance

OSR SETTING	INPUT IMPEDANCE[(1)]	
	GLOBAL-CHOP DISABLED	GLOBAL-CHOP ENABLED
128	6 MΩ	40 MΩ
256	13 MΩ	75 MΩ
512	25 MΩ	150 MΩ
1024	25 MΩ	300 MΩ
2048	25 MΩ	600 MΩ
4096	25 MΩ	≥1 GΩ
8192	25 MΩ	≥1 GΩ
16384	25 MΩ	≥1 GΩ

(1) f_{MCLK} = 8.192 MHz, default global-chop delay setting.

8.3.4 Voltage Reference

The ADS130B02-Q1 uses an internally generated, low-drift, band-gap voltage to supply the reference for the ADC. The reference has a nominal voltage of 1.2 V, allowing the differential input voltage to swing from –1.2 V to 1.2 V at Gain = 1. The reference circuitry starts up very quickly to accommodate the fast start-up feature of this device. The device waits until after the reference circuitry is fully settled before generating conversion data.

8.3.5 Internal Test Signals

The ADS130B02-Q1 features an internal analog test signal that is useful for troubleshooting and diagnosis. A positive or negative dc test signal can be applied to the channel inputs through the input multiplexer. The multiplexer is controlled through the MUXn[1:0] bits in the CHn_CFG register. The test signals are created by internally dividing the reference voltage. The same signal is shared by all channels.

The test signal is nominally 2 / 15 × V_{REF}. The test signal automatically adjusts its voltage level with the gain setting such that the ADC always measures a signal that is 2 / 15 × $V_{Diff\ Max}$. For example, at a gain of 1, this voltage equates to 160 mV. At a gain of 2, this voltage is 80 mV.

8.3.6 Clocking

The ADS130B02-Q1 requires a main clock (MCLK) to operate. The main clock to the ADS130B02-Q1 is provided in one of two ways, as shown in 図 8-3: an external clock on the CLKIN pin or the internal oscillator. The CLK_SEL bit in the CLOCK register selects the according main clock source for the device.

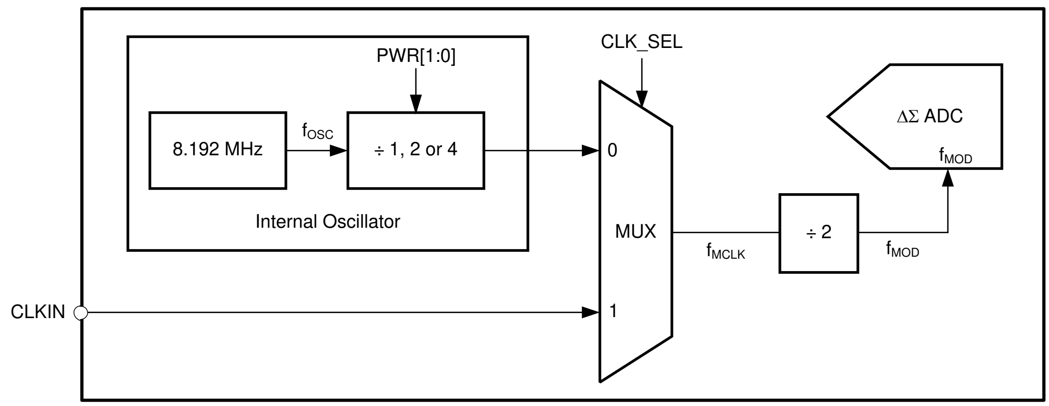


図 8-3. Main Clock Selection Diagram

8.3.6.1 External Clock Using CLKIN Pin

By default, the ADS130B02-Q1 is configured to operate with an external clock, such as at power-up. An LVCMOS clock must be provided at the CLKIN pin continuously when the ADS130B02-Q1 is running in normal operation. The frequency of the clock can be scaled in conjunction with the power mode to provide a trade-off between power consumption and noise performance.

The PWR[1:0] bits in the CLOCK register allow the device to be configured in one of three power modes: high-resolution (HR), low-power (LP), or very-low-power (VLP). Changing the PWR[1:0] bits scales the internal bias currents to achieve the expected power levels. Follow the guidance for the external clock frequency provided in the *Recommended Operating Conditions* table corresponding to the intended power mode in order for the device to perform according to the specification.

8.3.6.2 Internal Oscillator

The internal oscillator can be selected as the MCLK source by setting the CLK_SEL bit in the CLOCK register. At device power-up, the internal oscillator is disabled by default.

As shown in 図 8-3 and 表 8-3, the internal oscillator frequency (f_{OSC}) is scaled using a clock divider to provide the appropriate nominal main clock frequency (f_{MCLK}) for the different power modes. Correspondingly, the modulator clock frequency (f_{MOD}) scales as well because $f_{MOD} = f_{MCLK} / 2$.

表 8-3. Scaling of the Internal Oscillator Frequency Based on the Selected Power Mode

POWER MODE	CLOCK DIVIDER SETTING	f_{MCLK}	f_{MOD}
HR	1	8.192 MHz	4.096 MHz
LP	2	4.096 MHz	2.048 MHz
VLP	4	2.048 MHz	1.024 MHz

To switch between a running CLKIN and the internal oscillator as the MCLK source, put the device in standby mode to avoid creating glitches when switching the clock source because there are no clock sequencers in the device. Likewise, put the device in standby mode before changing power modes because a change in power mode changes the MCLK frequency based on the clock divider setting.

When always using the internal oscillator as the MCLK source, tie the CLKIN pin to DGND. Tying the CLKIN pin to DGND avoids the need to enter standby mode when switching from an external clock to the internal oscillator at power-up or after a reset.

8.3.7 ΔΣ Modulator

The ADS130B02-Q1 uses a delta-sigma (ΔΣ) modulator to convert the analog input voltage to a one's density modulated digital bit-stream. The ΔΣ modulator oversamples the input voltage at a frequency many times greater than the output data rate. The modulator frequency, f_{MOD}, of the ADS130B02-Q1 is equal to half the main clock frequency (that is, $f_{MOD} = f_{MCLK} / 2$).

The output of the modulator is fed back to the modulator input through a digital-to-analog converter (DAC) as a means of error correction. This feedback mechanism shapes the modulator quantization noise in the frequency domain to make the noise more dense at higher frequencies and less dense in the band of interest. The digital decimation filter following the ΔΣ modulator significantly attenuates the out-of-band modulator quantization noise, allowing the device to provide excellent dynamic range.

8.3.8 Digital Filter

The ΔΣ modulator bit-stream feeds into a digital filter. The digital filter is a linear phase, finite impulse response (FIR), low-pass sinc-type filter that attenuates the out-of-band quantization noise of the ΔΣ modulator. The digital filter demodulates the output of the ΔΣ modulator by averaging. The data passing through the filter is decimated and downsampled, to reduce the rate at which data come out of the modulator (f_{MOD}) to the output data rate (f_{DATA}). The decimation factor, defined as per 式 3, is called the *oversampling ratio (OSR)*.

$$OSR = f_{MOD} / f_{DATA} \tag{3}$$

The OSR is configurable and is set by the OSR[2:0] bits in the CLOCK register. There are eight OSR settings in the ADS130B02-Q1, allowing eight different data rate settings for any given main clock frequency. 表 8-4 lists the OSR settings and their corresponding output data rates for the nominal MCLK frequencies mentioned.

The OSR determines the amount of averaging of the modulator output in the digital filter and therefore also the filter bandwidth. The filter bandwidth directly affects the noise performance of the ADC because lower bandwidth results in lower noise, whereas higher bandwidth results in higher noise. See 表 7-1 for the noise specifications for various OSR settings.

表 8-4. OSR Settings and Data Rates for Nominal Main Clock Frequencies

POWER MODE	NOMINAL f_{MCLK}	f_{MOD}	OSR	OUTPUT DATA RATE
HR	8.192 MHz	4.096 MHz	128	32 kSPS
			256	16 kSPS
			512	8 kSPS
			1024	4 kSPS
			2048	2 kSPS
			4096	1 kSPS
			8192	500 SPS
			16384	250 SPS
LP	4.096 MHz	2.048 MHz	128	16 kSPS
			256	8 kSPS
			512	4 kSPS
			1024	2 kSPS
			2048	1 kSPS
			4096	500 SPS
			8192	250 SPS
			16384	125 SPS
VLP	2.048 MHz	1.024 MHz	128	8 kSPS
			256	4 kSPS
			512	2 kSPS
			1024	1 kSPS
			2048	500 SPS
			4096	250 SPS
			8192	125 SPS
			16384	62.5 SPS

8.3.8.1 Digital Filter Implementation

図 8-4 shows the digital filter implementation of the ADS130B02-Q1. The modulator bitstream feeds two parallel filter paths, a $sinc^3$ filter, and a fast-settling filter path.

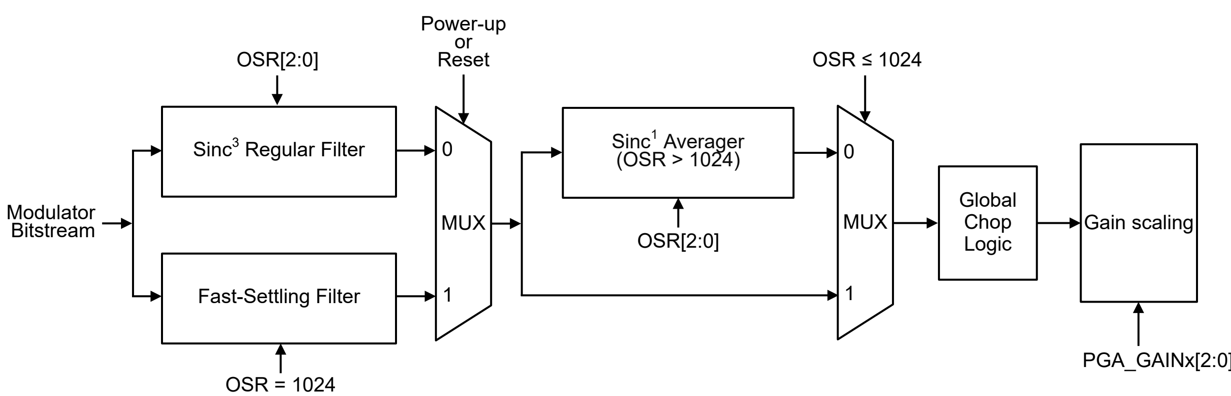


図 8-4. Digital Filter Implementation

8.3.8.1.1 Fast-Settling Filter

When the ADCs start converting for the first time after power-up or a device reset, the ADS130B02-Q1 selects the fast-settling filter to allow for settled output data generation with minimal latency. The fast-settling filter has the characteristic of a first-order sinc filter ($sinc^1$). After two conversions, the device switches to and remains in the $sinc^3$ filter path until the next time the device is powered down or reset.

The fast-settling filter exhibits wider bandwidth and less stop-band attenuation than the $sinc^3$ filter. Consequently, the noise performance when using the fast-settling filter is not as high as with the $sinc^3$ filter. The first two samples available from the ADS130B02-Q1 after a supply ramp or reset have the noise performance and frequency response corresponding to the fast-settling filter as specified in the *Electrical Characteristics* table, whereas subsequent samples have the noise performance and frequency response consistent with the $sinc^3$ filter. See the *Fast Start-Up Behavior* section for more details regarding the fast start-up capabilities of the ADS130B02-Q1.

8.3.8.1.2 $SINC^3$ and $SINC^3$ + $SINC^1$ Filter

The ADS130B02-Q1 selects the $sinc^3$ filter path two conversions after power-up or device reset. For OSR settings of 128 to 1024, the $sinc^3$ filter output directly feeds into the global-chop logic. For OSR settings of 2048 and higher, the $sinc^3$ filter is followed by a $sinc^1$ filter. As shown in 表 8-5, the $sinc^3$ filter operates at a fixed OSR of 1024 in this case while the $sinc^1$ filter implements the additional OSRs of 2 to 16. That means, when an OSR of 4096 (for example) is selected, the $sinc^3$ filter operates at an OSR of 1024 and the $sinc^1$ filter at an OSR of 4.

The filter has infinite attenuation at integer multiples of the data rate except for integer multiples of f_{MOD}. Like all digital filters, the digital filter response of the ADS130B02-Q1 repeats at integer multiples of the modulator frequency, f_{MOD}. The data rate and filter notch frequencies scale with f_{MOD}.

When possible, plan frequencies for unrelated periodic processes in the application for integer multiples of the data rate such that any parasitic effect they have on data acquisition is effectively canceled by the notches of the digital filter. Avoid frequencies near integer multiples of f_{MOD} whenever possible because tones in these bands can alias to the band of interest.

The $sinc^3$ and $sinc^3$ + $sinc^1$ filters for a given channel require time to settle after a channel is enabled, the channel multiplexer or gain setting is changed, or a resynchronization event occurs. 表 8-5 lists the settling times of the $sinc^3$ and $sinc^3$ + $sinc^1$ filters for each OSR setting. The ADS130B02-Q1 does not gate unsettled data. Therefore, the host must account for the filter settling time and disregard unsettled data if any are read. The data at the next $\overline{DRDY}$ falling edge after the filter settling time listed in 表 8-5 has expired can be considered fully settled.

表 8-5. Digital Filter Settling Times

OSR (Overall)	OSR ($SINC^3$)	OSR ($SINC^1$)	SETTLING TIME (t_{MOD})
128	128	N/A	432
256	256	N/A	816
512	512	N/A	1584
1024	1024	N/A	3120
2048	1024	2	6192
4096	1024	4	10288
8192	1024	8	18480
16384	1024	16	34864

8.3.8.2 Digital Filter Characteristic

式 4 calculates the z-domain transfer function of a $sinc^3$ filter that is used for OSRs ranging from 128 to 1024:

$$|H(z)| = \left| \frac{1 - Z^{-N}}{N\left(1 - Z^{-1}\right)} \right|^3 \quad (4)$$

where:

- N is the OSR

式 5 calculates the transfer function of a sinc^3 filter in terms of the continuous-time frequency parameter *f*:

$$\left|H(f)\right| = \left|\frac{\sin\left(\frac{N\pi f}{f_{MOD}}\right)}{N \times \sin\left(\frac{\pi f}{f_{MOD}}\right)}\right|^3 \quad (5)$$

where:

- N is the OSR

図 8-5 and 図 8-6 show the digital filter response of the fast-settling filter and the sinc^3 filter for OSRs ranging from 128 to 1024. 図 8-7 and 図 8-8 compare the digital filter responses of the sinc^3 filter at an OSR of 1024 and $\text{sinc}^3 + \text{sinc}^1$ filter for an OSR of 4096.

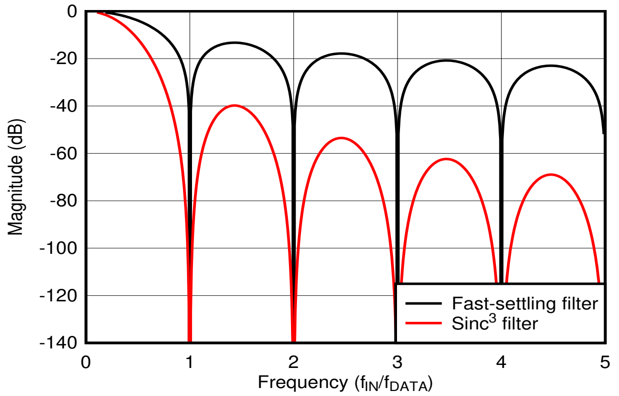


図 8-5. Fast-Settling and Sinc^3 Digital Filter Response

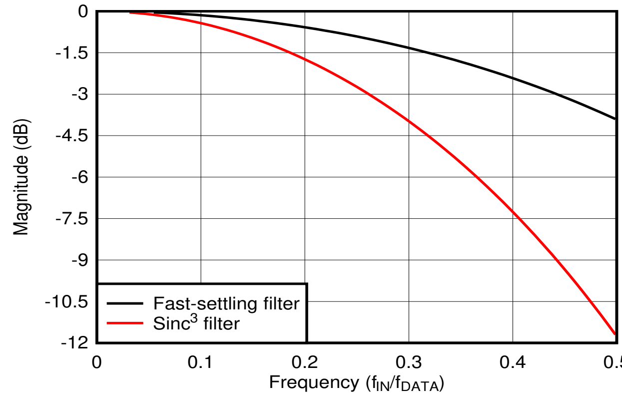


図 8-6. Fast-Settling and Sinc^3 Digital Filter Response, Pass-Band Detail

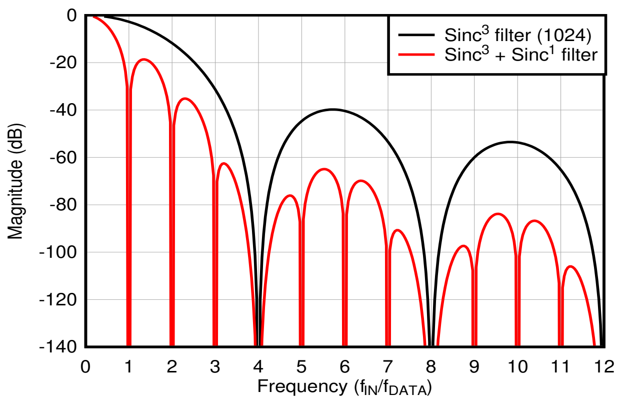


図 8-7. Digital Filter Response for OSR = 1024 and OSR = 4096

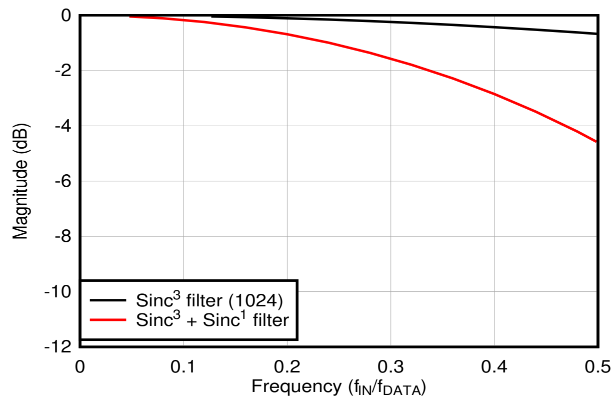


図 8-8. Digital Filter Response for OSR = 1024 and OSR = 4096, Pass-Band Detail

8.3.9 Register Map CRC

The ADS130B02-Q1 performs a CRC on its own register map as a means to check for unintended changes to the registers. Enable the register map CRC by setting the REG_CRC_EN bit in the MODE register. When enabled, the device constantly calculates the register map CRC across the registers ranging from address 02h to 12h including the reserved registers. The CRC is calculated beginning with the MSB of register 02h and ending with the LSB of register 12h using the polynomial selected in the CRC_TYPE bit in the MODE register. Two types of CRC polynomials are available: CCITT CRC and ANSI CRC (CRC-16). See 表 8-7 for details on the CRC polynomials. The CRC calculation is initialized with the seed value of FFFFh.

The calculated CRC is a 16-bit value and is stored in the REGMAP_CRC register. The calculation is done using one register map bit per MCLK period and constantly checks the result against the previous calculation. The REG_MAP bit in the STATUS register is set to flag the host if the register map CRC changes, including changes resulting from register writes. The REG_MAP bit is cleared by reading the STATUS register, or when the STATUS register is output as a response to the NULL command.

8.4 Device Functional Modes

図 8-9 shows a state diagram depicting the major functional modes of the ADS130B02-Q1 and the transitions between these modes.

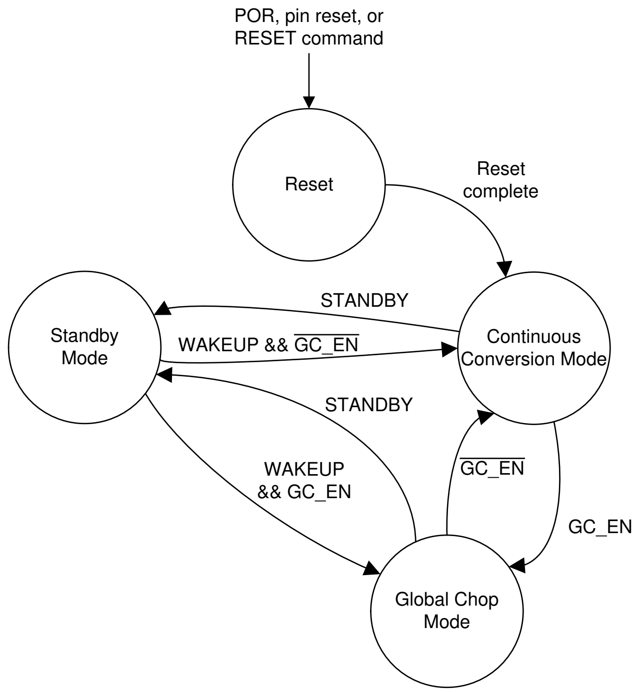


図 8-9. State Diagram Depicting Device Functional Modes

8.4.1 Power-Up and Reset

The ADS130B02-Q1 is reset in one of three ways: by a power-on reset (POR), by the SYNC/RESET pin, or by a RESET command. After a reset occurs, the configuration registers are reset to the default values and the device begins generating conversion data as soon as a valid MCLK is provided. In all three cases a low to high transition on the DRDY pin indicates that the SPI interface is ready for communication. The device ignores any SPI communication before this point.

8.4.1.1 Power-On Reset

Power-on reset (POR) is the reset that occurs when a valid supply voltage is first applied. The POR process requires t_{POR} to complete from when the supply voltages reach 90% of their nominal value to allow for the internal circuitry to power up. The DRDY pin transitions from low to high immediately after t_{POR} indicating the SPI interface is ready for communication.

8.4.1.2 SYNC/RESET Pin

The SYNC/RESET pin is an active low, dual-function pin that generates a reset if the pin is held low for longer than $t_{w(RSL)}$. The device maintains a reset state until SYNC/RESET is returned high. The host must wait for at least t_{REGACQ} after SYNC/RESET is brought high or for the DRDY rising edge before communicating with the device.

8.4.1.3 RESET Command

The ADS130B02-Q1 can be reset via the SPI RESET command. The device communicates in frames of a fixed length. Four words are required to complete a frame on the ADS130B02-Q1. The RESET command is transmitted in the first word of the data frame on DIN, but the command is not latched and executed by the device until the entire frame is complete. Terminating the frame early causes the RESET command to be ignored. A device reset occurs immediately after the RESET command is latched. The host must wait for at least t_{REGACQ} or for the DRDY rising edge before communicating with the device.

8.4.2 Fast Start-Up Behavior

The ADS130B02-Q1 begins generating conversion data shortly after start-up as soon as a valid MCLK signal is provided to the ΔΣ modulators. Fast start-up is accomplished via two mechanisms. First, the device internal power-supply circuitry is designed specifically to enable fast start-up. Second, the digital decimation filter dynamically switches from a fast-settling filter to a $sinc^3$ filter when the $sinc^3$ filter has settled.

After the supplies are ramped to 90% of their final values, the device requires t_{POR} for the internal circuitry to settle. The end of t_{POR} is indicated by a transition of $\overline{DRDY}$ from low to high. The transition of $\overline{DRDY}$ from low to high also indicates the SPI interface is ready to accept commands.

The ΔΣ modulators of the ADS130B02-Q1 require CLKIN to toggle after t_{POR} to begin working, or alternatively, activate the internal oscillator by setting the CLK_SEL bit in the CLOCK register. The modulators begin sampling the input signal after an initial wait time delay of (256 + 44) × t_{MOD} when MCLK begins toggling. Therefore, when using an external clock, provide a valid clock signal on CLKIN as soon as possible after the supply ramp to achieve the fastest possible start-up time.

The data generated by the ΔΣ modulators are fed to the digital filter blocks. The data are provided to both the fast-settling filter and the $sinc^3$ filter paths. The fast-settling filter requires only one data rate period to provide settled data. Meanwhile, the $sinc^3$ filter requires three data rate periods to settle. The fast-settling filter generates the output data for the two interim ADC output samples indicated by $\overline{DRDY}$ transitioning from high to low while the $sinc^3$ filter is settling. The device disables the fast-settling filter and provides conversion data from the $sinc^3$ filter path for the third and following samples. 図 8-10 shows the behavior of the fast-start-up feature when using an external clock that is provided to the device right after the supplies have ramped. 表 8-6 shows the values for the various start-up and settling times relevant to the device start-up.

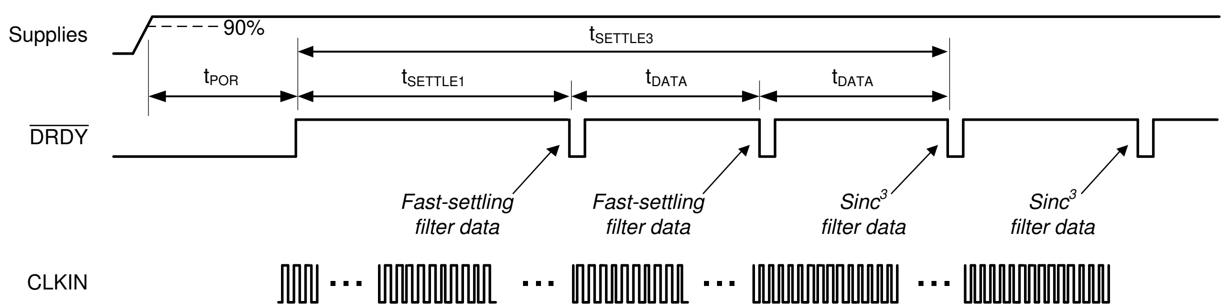


図 8-10. Fast Start-Up Behavior and Settling Times

表 8-6. Fast Start-Up Settling Times for Default OSR = 1024

PARAMETER	VALUE (DETAILS) (t_{MOD})	VALUE (t_{MOD})	VALUE AT f_{MCLK} = 8.192 MHz (ms)
$t_{DATA} = 1/f_{DATA}$	1024	1024	0.250
$t_{SETTLE1}$	256 + 44 + 1024	1324	0.323
$t_{SETTLE3}$	256 + 44 + 3 × 1024	3372	0.823

The fast-settling filter provides conversion data that are significantly noisier than the data that comes from the $sinc^3$ filter path, but allows the device to provide settled conversion data during the longer settling time of the more accurate $sinc^3$ digital filter. If the level of precision provided by the fast-settling filter is insufficient even for the first samples immediately following start-up, ignore the first two instances of $\overline{DRDY}$ toggling from high to low and begin collecting data on the third instance.

The start-up process following a RESET command or a pin reset using the $\overline{SYNC/RESET}$ pin is similar to what occurs after power up. However there is no t_{POR} in the case of a command or pin reset because the supplies are already ramped. After reset, the device waits for the initial wait time delay of (256 + 44) × t_{MOD} before providing modulator samples to the two digital filters. The fast-settling filter is enabled for the first two output samples. Remember to enable the internal oscillator every time again after a reset in case the internal oscillator is to be used, because the device defaults to using an external clock.

8.4.3 Conversion Modes

There are two ADC conversion modes on the ADS130B02-Q1: continuous-conversion and global-chop mode. Continuous-conversion mode is a mode where ADC conversions are generated constantly by the ADC at a rate defined by f_{MOD} / OSR. Global-chop mode differs from continuous-conversion mode because global-chop periodically chops (or swaps) the inputs, which reduces system offset errors at the cost of settling time between the points when the inputs are swapped. In either continuous-conversion or global-chop mode, there are three power modes that provide flexible options to scale power consumption with bandwidth and dynamic range. The *Power Modes* section discusses these power modes in further detail.

8.4.3.1 Continuous-Conversion Mode

Continuous-conversion mode is the mode in which ADC data are generated constantly at the rate of f_{DATA} = f_{MOD} / OSR. New data are indicated by a $\overline{DRDY}$ falling edge at this rate. Continuous-conversion mode is intended for measuring AC signals because this mode allows for higher output data rates than global-chop mode.

8.4.3.2 Global-Chop Mode

The ADS130B02-Q1 incorporates a global-chop mode option to reduce offset error and offset drift inherent to the device resulting from mismatch in the internal circuitry to very low levels. When global-chop mode is enabled by setting the GC_EN bit in the GLOBAL_CHOP_CFG register, the device uses the conversion results from two consecutive internal conversions taken with opposite input polarity to cancel the device offset voltage. Conversion *n* is taken with normal input polarity. The device then reverses the internal input polarity for conversion $\overline{n+1}$. The average of two consecutive conversions (n and $\overline{n+1}$, $\overline{n+1}$ and $n+2$, and so on) yields the final offset compensated result.

図 8-11 shows a block diagram of the global-chop mode implementation. The combined PGA and ADC internal offset voltage is modeled as V_{OFS}. Only this device inherent offset voltage is reduced by global-chop mode. Offset in the external circuitry connected to the analog inputs is not affected by global-chop mode.

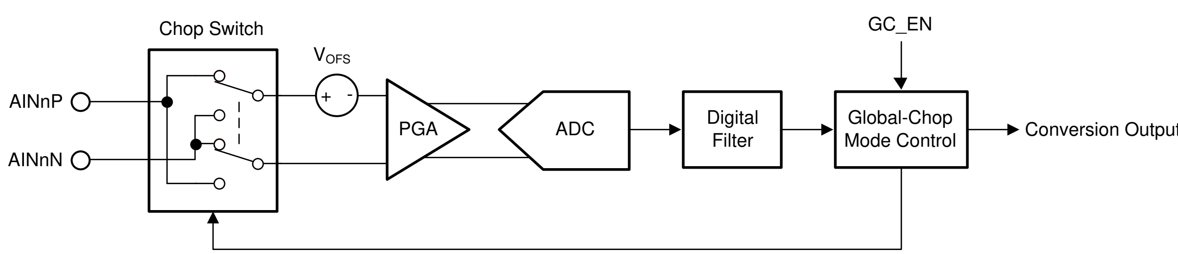


図 8-11. Global-Chop Mode Implementation

The conversion period in global-chop mode differs from the conversion time when global-chop mode is disabled (t_{DATA} = OSR × t_{MOD}). 図 8-12 shows the conversion timing for an ADC channel using global-chop mode.

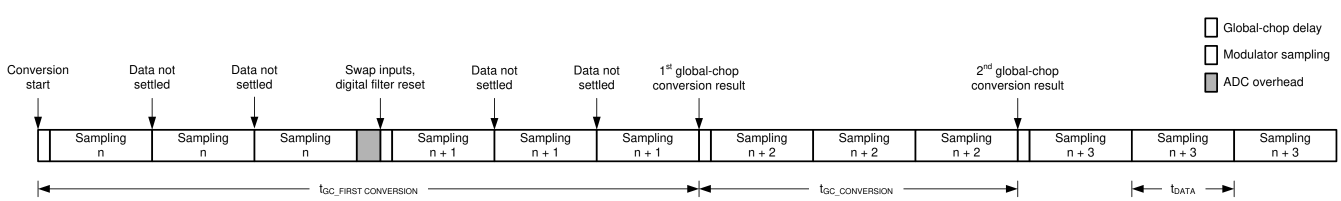


図 8-12. Conversion Timing With Global-Chop Mode Enabled

Every time the device swaps the input polarity, the digital filter is reset. The ADC then always takes three internal conversions to produce one settled global-chop conversion result.

The ADS130B02-Q1 provides a programmable delay (t_{GC_DLY}) between the end of the previous conversion period and the beginning of the subsequent conversion period after the input polarity is swapped. This delay allows for external input circuitry to settle because the chopping switches interface directly with the analog inputs. The GC_DLY[3:0] bits in the GLOBAL_CHOP_CFG register configure the delay after chopping the inputs. The global-chop delay is selected in terms of modulator clock periods from 2 to 65,536 × t_{MOD}.

The effective conversion period in global-chop mode follows 式 6. A $\overline{DRDY}$ falling edge is generated each time a new global-chop conversion becomes available to the host.

The conversion process of all ADC channels in global-chop mode is restarted in the following two conditions so that all channels start sampling at the same time:

- Falling edge of $\overline{SYNC}/\overline{RESET}$ pin
- Change of OSR setting

The conversion period of the first conversion after the ADC channels are reset is considerably longer than the conversion period of all subsequent conversions mentioned in 式 6, because the device first must perform two fully settled internal conversions with the input polarity swapped. The conversion period for the first conversion in global-chop mode follows 式 7.

$$t_{GC\_CONVERSION} = t_{GC\_DLY} + 3 \times OSR \times t_{MOD} \quad (6)$$

$$t_{GC\_FIRST\_CONVERSION} = t_{GC\_DLY} + 3 \times OSR \times t_{MOD} + t_{GC\_DLY} + 3 \times OSR \text{ x } t_{MOD} + 44 \times t_{MOD} \quad (7)$$

Using global-chop mode reduces the ADC noise shown in 表 7-1 at a given OSR by a factor of $\sqrt{2}$ because two consecutive internal conversions are averaged to yield one global-chop conversion result. The dc test signal cannot be measured in global-chop mode.

8.4.4 Power Modes

In both continuous-conversion and global-chop mode, there are three selectable power modes that allow scaling of power with bandwidth and performance: high-resolution (HR) mode, low-power (LP) mode, and very-low-power (VLP) mode. The mode is selected by the PWR[1:0] bits in the CLOCK register. See the *Clocking* section for restrictions on the CLKIN frequency for each power mode in case an external clock source is used, or how the main clock frequency is scaled with each power mode in case the internal oscillator is enabled.

8.4.5 Standby Mode

Standby mode is a low-power state in which all channels are disabled, and the reference, internal oscillator and other non-essential circuitry are powered down. This mode differs from completely powering down the device because the device retains its register settings. Enter standby mode by sending the STANDBY command. Stop toggling CLKIN when the device is in standby mode and an external clock is used to minimize device power consumption. See the *Clocking* section for recommendations on how to use standby mode when switching between internal and external clock generation. Exit standby mode by sending the WAKEUP command.

8.4.6 Synchronization

Synchronization can be performed by the host to make sure the ADC conversions are synchronized to an external event. For example, synchronization can realign the data capture to the expected timing of the host if a glitch on the clock causes the host and device to become out of synchronization.

The $\overline{SYNC}/\overline{RESET}$ pin is a multifunction digital input pin that allows the host to synchronize conversions to an external event or to reset the device. See the *$\overline{SYNC}/\overline{RESET}$ Pin* section for more details regarding how the device is reset.

Provide a negative pulse on the $\overline{SYNC}/\overline{RESET}$ pin with a duration less than $t_{w(RSL)}$ but greater than a MCLK period to trigger synchronization. The device internally compares the leading negative edge of the pulse to its internal clock that tracks the data rate. The internal data rate clock has timing equivalent to the $\overline{DRDY}$ pin. If the negative edge on $\overline{SYNC}/\overline{RESET}$ aligns with the internal data rate clock, the device is determined to be synchronized and therefore no action is taken. If there is misalignment, the digital filters on the device are reset to be synchronized with the $\overline{SYNC}/\overline{RESET}$ pulse.

In global-chop mode conversions are always immediately restarted at the falling edge of the $\overline{SYNC}/\overline{RESET}$ pin.

8.5 Programming

8.5.1 Serial Interface

The ADS130B02-Q1 uses an SPI-compatible interface to configure the device and retrieve conversion data. The device always acts as an SPI peripheral; SCLK and $\overline{CS}$ are inputs to the interface. The interface operates in SPI mode 1 where CPOL = 0 and CPHA = 1. In SPI mode 1, the SCLK idles low and data are launched or changed only on SCLK rising edges; data are latched or read by the controller and peripheral on SCLK falling edges. The interface is full-duplex, meaning data can be sent and received simultaneously by the interface. The device includes the typical SPI signals: SCLK, $\overline{CS}$, DIN (MOSI), and DOUT (MISO). In addition, there are two other digital pins that provide additional functionality. The $\overline{DRDY}$ pin serves as a flag to the host to indicate new conversion data are available. The $\overline{SYNC/RESET}$ pin is a dual-function pin that allows synchronization of conversions to an external event and allows for a hardware device reset.

8.5.1.1 Chip Select ($\overline{CS}$)

The $\overline{CS}$ pin is an active-low input signal that selects the device for communication. The device ignores any communication and DOUT is high impedance when $\overline{CS}$ is held high. Hold $\overline{CS}$ low for the duration of a communication frame to maintain proper communication. The interface is reset each time $\overline{CS}$ is taken high.

8.5.1.2 Serial Data Clock (SCLK)

The SCLK pin is an input that serves as the serial clock for the interface. Output data on the DOUT pin transition on the rising edge of SCLK and input data on DIN are latched on the falling edge of SCLK.

8.5.1.3 Serial Data Input (DIN)

The DIN pin is the serial data input pin for the device. Serial commands are shifted in through the DIN pin by the device with each SCLK falling edge when the $\overline{CS}$ pin is low.

8.5.1.4 Serial Data Output (DOUT)

The DOUT pin is the serial data output pin for the device. The device shifts out command responses and ADC conversion data serially with each rising SCLK edge when the $\overline{CS}$ pin is low. This pin assumes a high-impedance state when $\overline{CS}$ is high.

8.5.1.5 Data Ready ($\overline{DRDY}$)

The $\overline{DRDY}$ pin is an active-low digital output that indicates when new conversion data are available for readout. Connect the $\overline{DRDY}$ pin to a digital input on the host to trigger periodic data retrieval in conversion mode.

A high-to-low transition of the $\overline{DRDY}$ output indicates that new conversion data completed and are ready for readout. The period between $\overline{DRDY}$ falling edges is the data-rate period. A low level of the $\overline{DRDY}$ pin indicates that the latest conversion data have not yet been read. $\overline{DRDY}$ transitions high when the conversion data of the two ADC channels, including those of disabled channels, are shifted out of the device. $\overline{DRDY}$ stays low if the data read is incomplete, thus indicating that not all ADC data have been retrieved. In case conversion data are not read before the next conversion cycle completes, $\overline{DRDY}$ transitions high $t_{w(DRH)}$ ahead of the next $\overline{DRDY}$ falling edge. See the *Collecting Data for the First Time or After a Pause in Data Collection* section for more information about the behavior of $\overline{DRDY}$ when data are not consistently read. The $\overline{DRDY}$ high pulse is blocked when new conversions complete while conversion data are read. Therefore, avoid reading ADC data during the time where new conversions complete in order to achieve consistent $\overline{DRDY}$ behavior.

The DRDY_HIZ bit in the MODE register configures the state of the $\overline{DRDY}$ pin when deasserted. By default the bit is 0b, meaning the pin is actively driven high using a push-pull output stage. When the bit is 1b, $\overline{DRDY}$ behaves like an open-drain digital output. Use a 100-kΩ pullup resistor to pull the pin high when $\overline{DRDY}$ is not asserted.

8.5.1.6 SPI Communication Frames

SPI communication on the ADS130B02-Q1 is performed in frames. Each SPI communication frame consists of several words. The word size is configurable as either 16 bits, 24 bits, or 32 bits by programming the WLENGTH[1:0] bits in the MODE register.

The interface is full duplex, meaning that the interface is capable of transmitting data on DOUT while simultaneously receiving data on DIN. The input frame that the host sends on DIN always begins with a command. The first word on the output frame that the device transmits on DOUT always begins with the response to the command that was written on the previous input frame. The number of words in a command depends on the command provided. For most commands, there are four words in a frame. On DIN, the host provides the command, the command CRC if input CRC is enabled or a word of zeros if input CRC is disabled, and two additional words of zeros. Simultaneously on DOUT, the device outputs the response from the previous frame command, two words of ADC data representing the two ADC channels, and a CRC word. 図 8-13 shows a typical command frame structure.

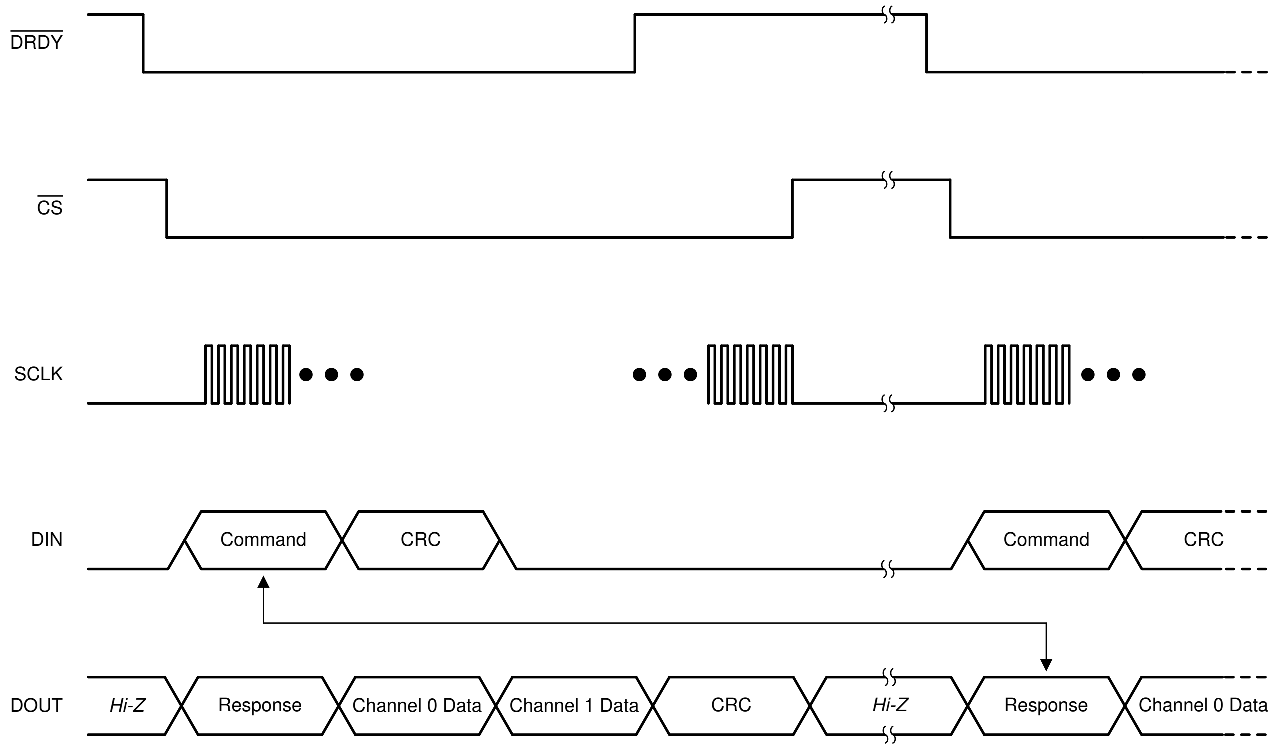


図 8-13. Typical Communication Frame

There are some commands that require more or less than four words. In the case of a read register (RREG) command where more than a single register is read, the response to the command contains the acknowledgment of the command followed by the register contents requested, which may require a longer frame depending on how many registers are read. See the *RREG command* section for more details on the RREG command.

In the case of a write register (WREG) command where more than a single register is written, the frame extends to accommodate the additional data. See the *WREG command* section for more details on the WREG command.

See the *Commands* section for a list of all valid commands and their corresponding responses on the ADS130B02-Q1.

Under special circumstances, a data frame can be shortened by the host. See the *Short SPI Frames* section for more information about artificially shortening communication frames.

8.5.1.7 SPI Communication Words

An SPI communication frame with the ADS130B02-Q1 is made of words. Words on DIN can contain commands, register settings during a register write, or a CRC of the input data. Words on DOUT can contain command responses, register settings during a register read, ADC conversion data, or CRC of the output data.

Words can be 16, 24, or 32 bits. The word size is configured by the WLENGTH[1:0] bits in the MODE register. The device defaults to a 24-bit word size. ADC conversion data, commands, responses, CRC, and registers always contain 16 bits of actual data. All words are most significant bit (MSB) aligned, and therefore the least significant bits (LSBs) are zero-padded to accommodate 24- or 32-bit word sizes.

図 8-14 through 図 8-16 show the locations of the individual bits in an SPI frame for the different word size options using a WREG command frame for writing two registers as an example.

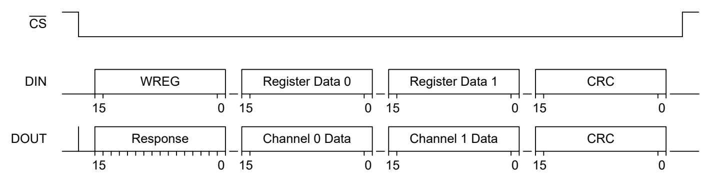


図 8-14. SPI Frame using 16-bit Word Size

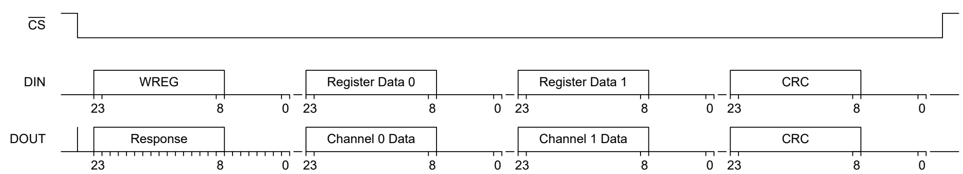


図 8-15. SPI Frame using 24-bit, zero-padded Word Size

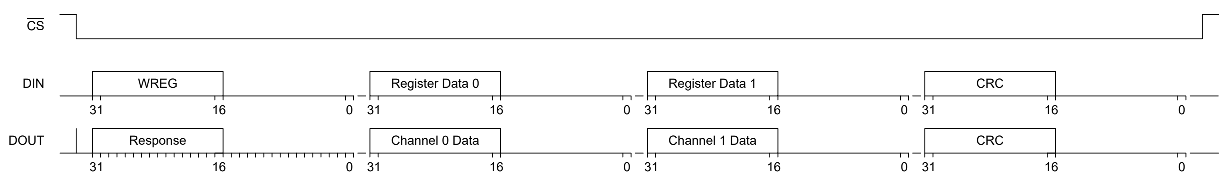


図 8-16. SPI Frame using 32-bit, zero-padded Word Size

8.5.1.8 Short SPI Frames

The SPI frame can be shortened to only send commands and receive responses if the ADCs are disabled and no ADC data are being output by the device. Read out all expected output data words from each sample period if the ADCs are enabled. Reading all of the data output with each frame provides predictable $\overline{DRDY}$ pin behavior. If reading out all the data on each output data period is not feasible, see the *Collecting Data for the First Time or After a Pause in Data Collection* section on how to begin reading data again after a pause from when the ADCs were last enabled.

A short frame is not possible when using the RESET command. A full frame must be provided for a device reset to take place when sending the RESET command.

8.5.1.9 Communication Cyclic Redundancy Check (CRC)

The ADS130B02-Q1 features a cyclic redundancy check (CRC) engine on both input and output data to mitigate SPI communication errors. The CRC word is 16 bits wide for either input or output CRC. Coverage includes all words in the SPI frame where the CRC is enabled, including zero-padded bits.

CRC on the SPI input is optional and can be enabled and disabled by writing the RX_CRC_EN bit in the MODE register. Input CRC is disabled by default. When the input CRC is enabled, the device checks the provided input CRC against the CRC generated based on the input data. A CRC error occurs if the CRC words do not match. The device does not execute any commands, except for the WREG command, if the input CRC check fails. A WREG command always executes even when the CRC check fails. The device sets the CRC_ERR bit in the STATUS register for all cases of a CRC error. The response on the output in the SPI frame following the frame where the CRC error occurred is that of a NULL command, which means the STATUS register plus the conversion data are output in the following SPI frame. The CRC_ERR bit is cleared when the STATUS register is output.

The output CRC cannot be disabled and always appears at the end of the output frame. The host can ignore the data if the output CRC is not used.

There are two types of CRC polynomials available: CCITT CRC and ANSI CRC (CRC-16). The CRC setting determines the algorithm for both the input and output CRC. The CRC type is programmed by the CRC_TYPE bit in the MODE register. 表 8-7 lists the details of the two CRC types. The CRC calculation is initialized with the seed value of FFFFh to detect errors in the event that DIN or DOUT are stuck low.

表 8-7. CRC Types

CRC TYPE	POLYNOMIAL	BINARY POLYNOMIAL
CCITT CRC	$x^{16} + x^{12} + x^5 + 1$	0001 0000 0010 0001
ANSI CRC	$x^{16} + x^{15} + x^2 + 1$	1000 0000 0000 0101

8.5.1.10 SPI Timeout

The ADS130B02-Q1 features an SPI timeout as a means to recover SPI communication, especially in situations where $\overline{CS}$ is permanently tied low. Enable the SPI timeout using the TIMEOUT bit in the MODE register. When enabled, the entire SPI frame (first SCLK to last SCLK) must complete in 2^{15} MCLK cycles, otherwise the SPI logic will reset. When a timeout happens the device starts interpreting the data starting with the next SCLK as a new SPI frame.

8.5.2 ADC Conversion Data Format

The device provides conversion data for each channel at the data rate. All data are available immediately following $\overline{DRDY}$ assertion. The conversion status of all channels is available as the DRDY[1:0] bits in the STATUS register. The STATUS register content is automatically output as the response to the NULL command.

Conversion data are 16 bits. The LSBs are zero padded when operating with a 24-bit or 32-bit word size.

Data are given in binary two's complement format. Use 式 8 to calculate the size of one code (LSB).

$$1\ LSB = (2.4\ /\ Gain)\ /\ 2^{16} = +FSR\ /\ 2^{15} \quad (8)$$

A positive full-scale input V_{IN} ≥ +FSR – 1 LSB = 1.2 / Gain – 1 LSB produces an output code of 7FFFh and a negative full-scale input (V_{IN} ≤ –FSR = –1.2 / Gain) produces an output code of 8000h. The output clips at these codes for signals that exceed full-scale.

表 8-8 summarizes the ideal output codes for different input signals.

表 8-8. Ideal Output Code versus Input Signal

INPUT SIGNAL ($V_{IN} = V_{AINP} - V_{AINN}$)	IDEAL OUTPUT CODE
≥ FSR $(2^{15} – 1) / 2^{15}$	7FFFh
FSR / 2^{15}	0001h
0	0000h
–FSR / 2^{15}	FFFFh
≤ –FSR	8000h

図 8-17 shows the mapping of the analog input signal to the output codes.

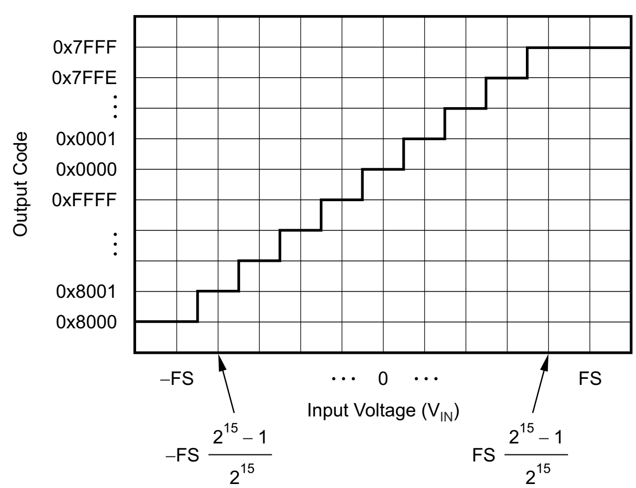


図 8-17. Code Transition Diagram

8.5.3 Commands

表 8-9 contains a list of all valid commands, a short description of their functionality, their binary command word, and the expected response that appears in the following frame.

表 8-9. Command Definitions

COMMAND	DESCRIPTION	COMMAND WORD	RESPONSE
NULL	No operation	0000 0000 0000 0000	STATUS register
RESET	Reset the device	0000 0000 0001 0001	1111 1111 0101 0010
STANDBY	Place the device into standby mode	0000 0000 0010 0010	0000 0000 0010 0010
WAKEUP	Wake the device from standby mode to conversion mode	0000 0000 0011 0011	0000 0000 0011 0011
LOCK	Lock the interface such that only the NULL, UNLOCK, and RREG commands are valid	0000 0101 0101 0101	0000 0101 0101 0101
UNLOCK	Unlock the interface after the interface is locked	0000 0110 0101 0101	0000 0110 0101 0101
RREG	Read *nnn nnnn* plus 1 registers beginning at address *a aaaa a*	101*a aaaa annn nnnn*	*dddd dddd dddd dddd* or 111*a aaaa annn nnnn* (1)
WREG	Write *nnn nnnn* plus 1 registers beginning at address *a aaaa a*	011*a aaaa annn nnnn*	010*a aaaa ammm mmmm* (2)

(1) When *nnn nnnn* is 0, the response is the requested register data *dddd dddd dddd dddd*. When *nnn nnnn* is greater than 0, the response begins with 111*a aaaa annn nnnn*, followed by the register data.
(2) In this case, *mmm mmmm* represents the number of registers that are actually written minus one. This value may be less than *nnn nnnn* in some cases.

8.5.3.1 NULL (0000 0000 0000 0000)

The NULL command is the *no-operation* command that results in no registers read or written, and the state of the device remains unchanged. The intended use case for the NULL command is to read out ADC conversion data. The command response for the NULL command is the contents of the STATUS register. Any invalid command also gives the NULL response.

8.5.3.2 RESET (0000 0000 0001 0001)

The RESET command resets the ADC to its register defaults. The command is latched by the device at the end of the frame. A reset occurs immediately after the command is latched. The host must wait for t_{REGACQ} after reset or for the $\overline{DRDY}$ rising edge before communicating with the device to make sure the registers have assumed their default settings. The device sends an acknowledgment of FF52h when the ADC is properly RESET. The device responds with 0011h if the command word is sent but the frame is not completed and therefore the device is not reset. See the *RESET Command* section for more information regarding the operation of the reset command. 図 8-18 illustrates a properly sent RESET command frame.

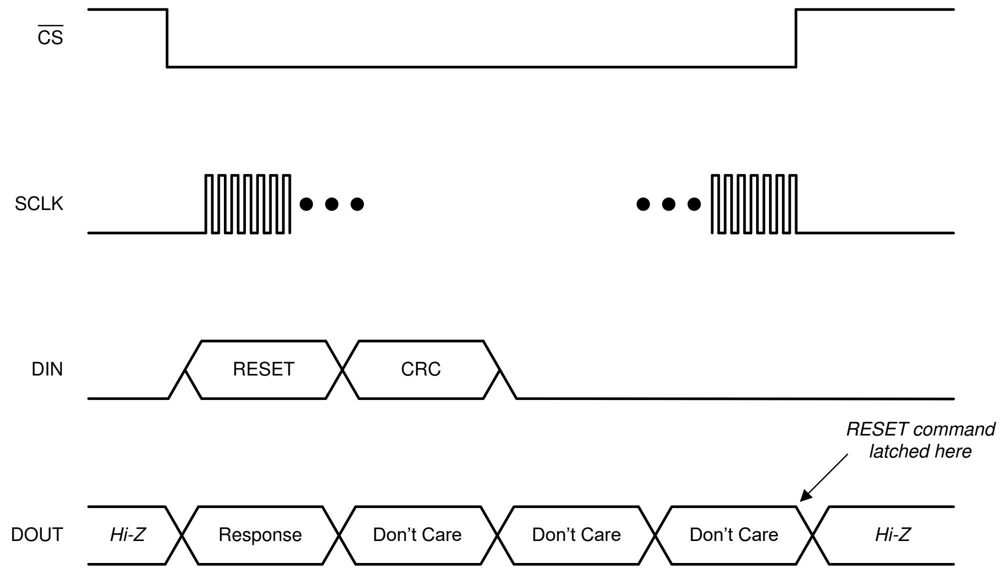


図 8-18. RESET Command Frame

8.5.3.3 STANDBY (0000 0000 0010 0010)

The STANDBY command places the device in a low-power standby mode. The command is latched by the device at the end of the frame. The device enters standby mode immediately after the command is latched. See the *Standby Mode* section for more information. This command has no effect when the device is already in standby mode.

8.5.3.4 WAKEUP (0000 0000 0011 0011)

The WAKEUP command returns the device to conversion mode from standby mode. This command has no effect if the device is already in conversion mode.

8.5.3.5 LOCK (0000 0101 0101 0101)

The LOCK command locks the interface, preventing the device from accidentally latching unwanted commands that can change the state of the device. When the interface is locked, the device only responds to the NULL, RREG, and UNLOCK commands. The device continues to output conversion data even when locked.

8.5.3.6 UNLOCK (0000 0110 0110 0110)

The UNLOCK command unlocks the interface if previously locked by the LOCK command.

8.5.3.7 RREG (101a aaaa annn nnnn)

The RREG is used to read the device registers. The binary format of the command word is 101*a aaaa annn nnnn*, where *a aaaa a* is the binary address of the register to begin reading and *nnn nnnn* is the unsigned binary number of consecutive registers to read minus one. There are two cases for reading registers on the ADS130B02-Q1. When reading a single register (*nnn nnnn* = 000 0000b), the device outputs the register contents in the command response word of the following frame. If multiple registers are read using a single command (*nnn nnnn* > 000 0000b), the device outputs the requested register data sequentially in order of addresses.

8.5.3.7.1 Reading a Single Register

Read a single register from the device by specifying *nnn nnnn* as zero in the RREG command word. As with all SPI commands on the ADS130B02-Q1, the response occurs on the output in the frame following the command. Instead of a unique acknowledgment word, the response word is the contents of the register whose address is specified in the command word. 図 8-19 shows an example of reading a single register.

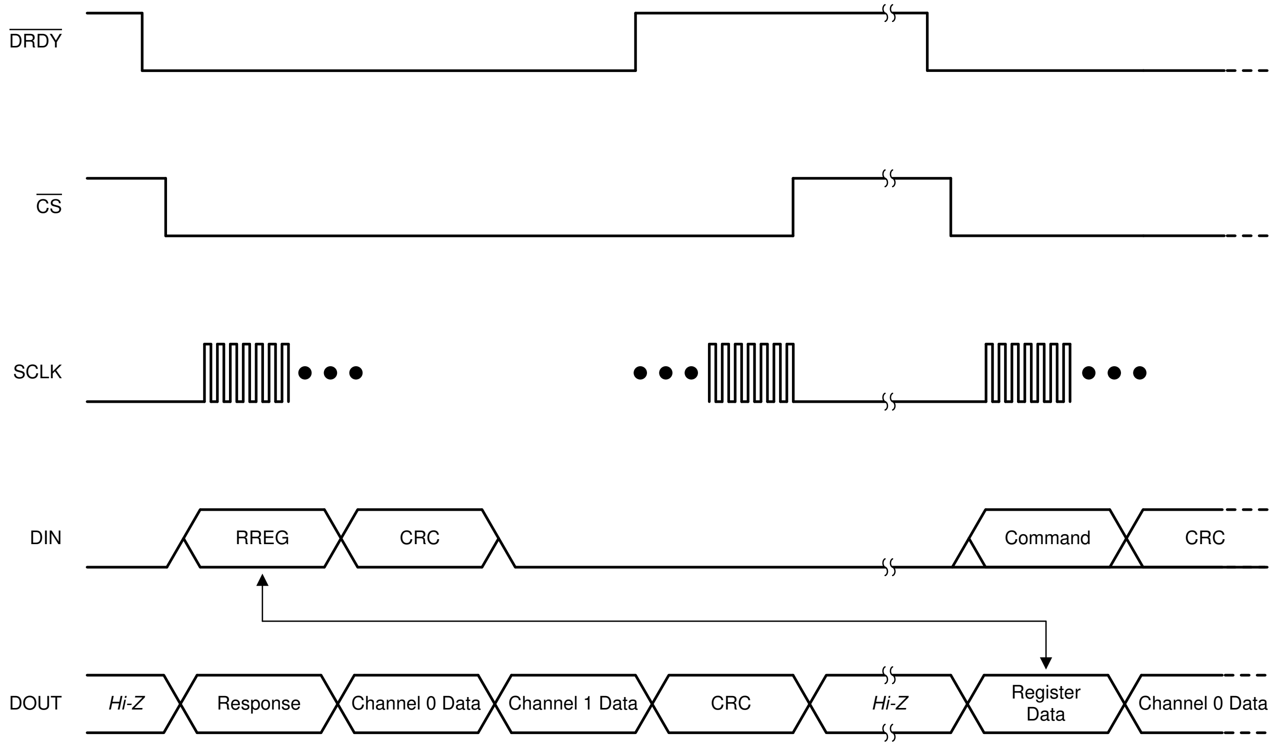


図 8-19. Reading a Single Register

8.5.3.7.2 Reading Multiple Registers

Multiple registers are read from the device when nnn nnnn is specified as a number greater than zero in the RREG command word. Like all SPI commands on the ADS130B02-Q1, the response occurs on the output in the frame following the command. Instead of a single acknowledgment word, the response spans multiple words in order to shift out all requested registers. Continue toggling SCLK to accommodate outputting the entire data stream. ADC conversion data are not output in the frame following an RREG command to read multiple registers. 図 8-20 shows an example of reading multiple registers.

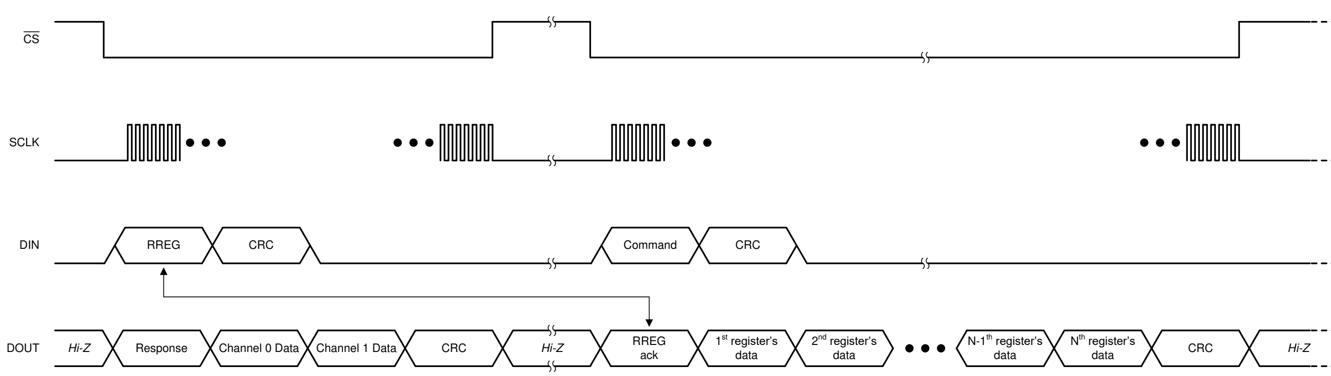


図 8-20. Reading Multiple Registers

8.5.3.8 WREG (011a aaaa annn nnnn)

The WREG command allows writing an arbitrary number of contiguous device registers. The binary format of the command word is 011*a aaaa annn nnnn*, where *a aaaa a* is the binary address of the register to begin writing and *nnn nnnn* is the unsigned binary number of consecutive registers to write minus one. Send the data to be written immediately following the command word. Write the intended contents of each register into individual words, MSB aligned.

If the input CRC is enabled, write this CRC after the register data. The registers are written to the device as they are shifted into DIN. Therefore, a CRC error does not prevent an erroneous value from being written to a register. An input CRC error during a WREG command sets the CRC_ERR bit in the STATUS register.

The device ignores writes to read-only registers or to out-of-bounds addresses. Gaps in the register map address space are still included in the parameter *nnn nnnn*, but are not writeable so no change is made to them. The response to the WREG command that occurs in the following frame appears as 010*a aaaa ammm mmmm* where *mmm mmmm* is the number of registers actually written minus one. This number can be checked by the host against *nnn nnnn* to make sure the expected number of registers are written.

図 8-21 shows a typical WREG sequence. In this example, the number of registers to write is larger than the number of ADC channels and, therefore, the frame is extended beyond the ADC channels and output CRC word. Make sure all of the ADC data and output CRC are shifted out during each transaction where new data are available. Therefore, the frame must be extended beyond the number of words required to send the register data in some cases.

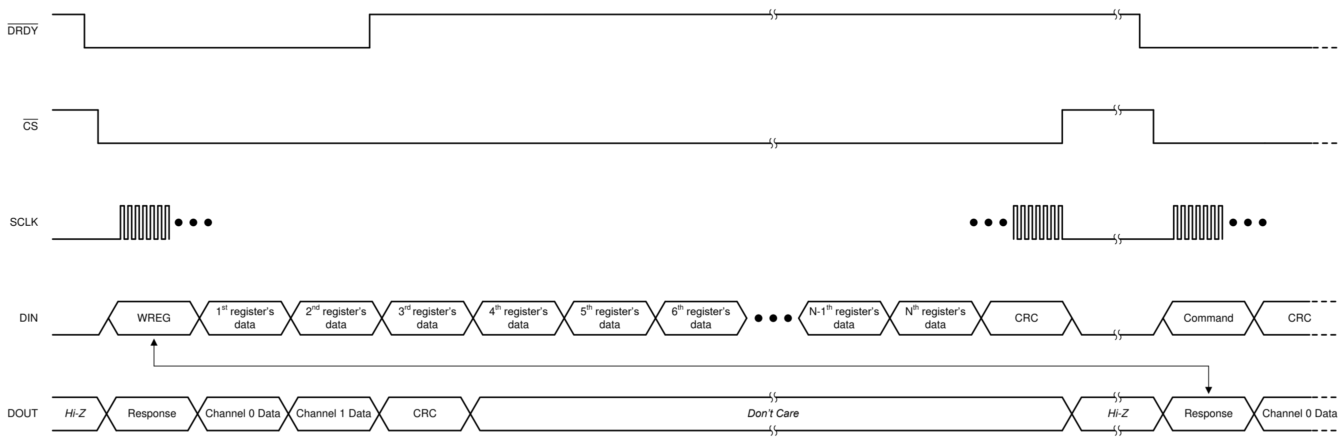


図 8-21. Writing Registers

8.5.4 Collecting Data for the First Time or After a Pause in Data Collection

Take special precaution when collecting data for the first time or when beginning to collect data again after a pause. The internal mechanism that outputs data contains a first-in-first-out (FIFO) buffer that can store two samples of data per channel at a time. The DRDY flag for each channel in the STATUS register remains set until both samples for each channel are read from the device. This condition is not obvious under normal circumstances when the host is reading each consecutive sample from the device. In that case, the samples are cleared from the device each time new data are generated so the DRDY flag for each channel in the STATUS register is cleared with each read. However, both slots of the FIFO are full if a sample is missed or if data are not read for a period of time. Either strobe the SYNC/RESET pin to resynchronize conversions and clear the FIFOs, or quickly read two data packets when data are read for the first time or after a gap in reading data. This process maintains predictable DRDY pin behavior. See the *Synchronization* section for information about the synchronization feature. These methods do not need to be employed if each channel data was read for each output data period from when the ADC was enabled.

図 8-22 shows an example of how to collect data after a period of the ADC running, but where no data are being retrieved. In this instance, the SYNC/RESET pin is used to clear the internal FIFOs and realign the ADS130B02-Q1 output data with the host.

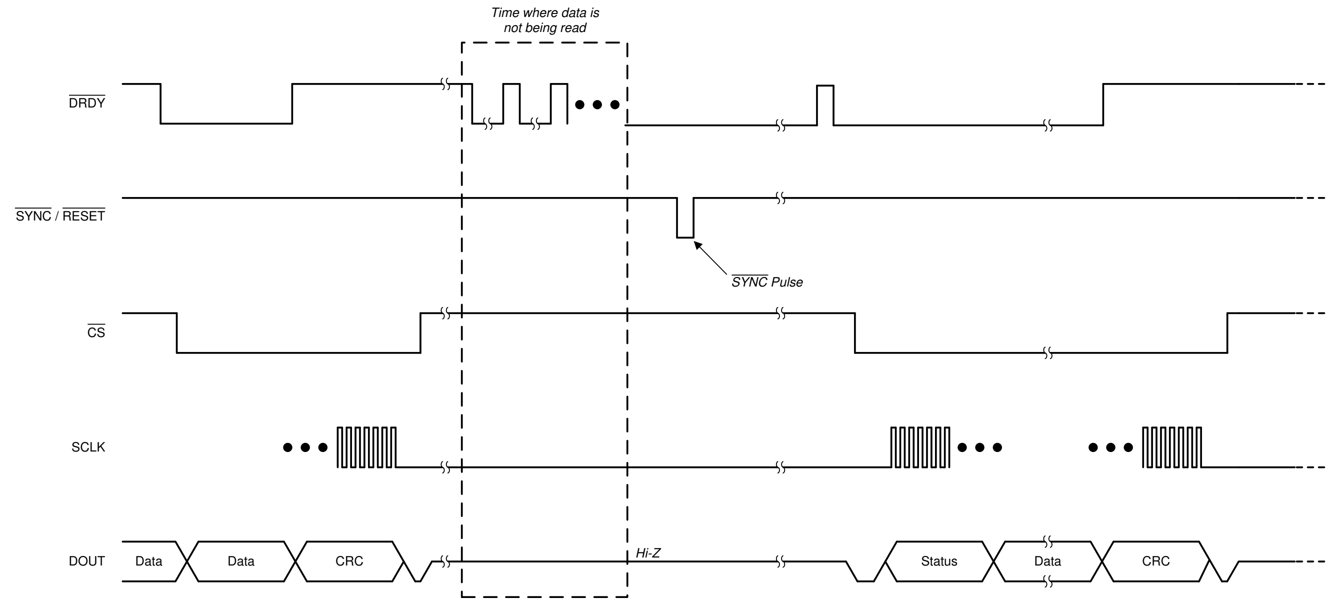


図 8-22. Collecting Data After a Pause in Data Collection Using the SYNC/RESET Pin

Another functionally equivalent method for clearing the FIFO after a pause in collecting data is to begin by reading two samples in quick succession. 図 8-23 depicts this method. There is a very narrow pulse on DRDY immediately after the first set of data are shifted out of the device. This pulse may be too narrow for some microcontrollers to detect. Therefore, do not rely upon this pulse, but instead immediately read out the second data set after the first data set. DRDY transitions high after the second data set is read, which indicates that no other new data are available for readout.

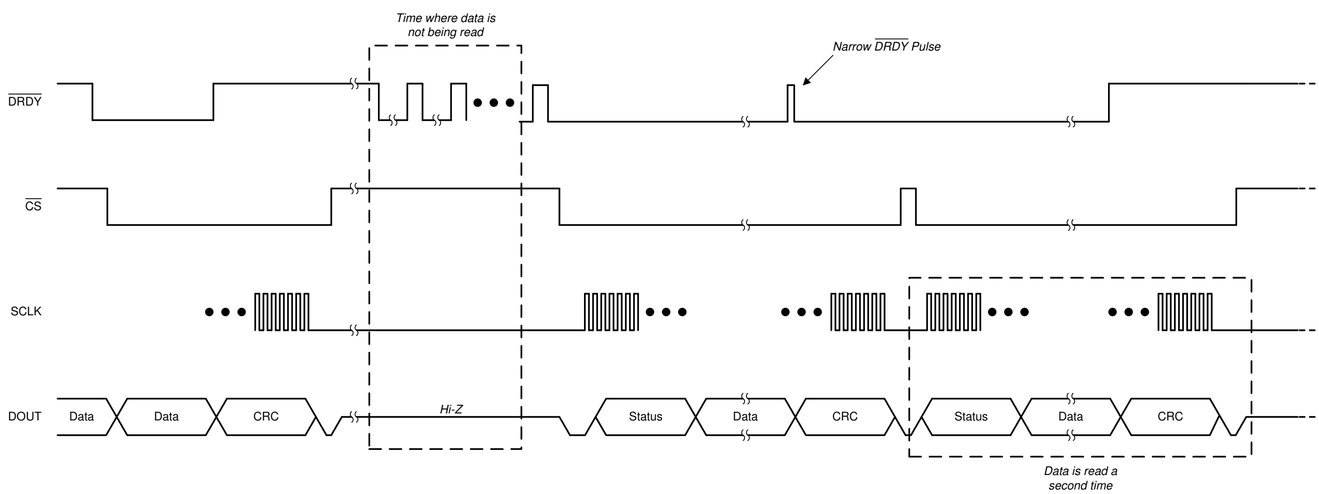


図 8-23. Collecting Data After a Pause in Data Collection by Reading Data Twice

8.6 Register Map

表 8-10 lists the ADS130B02-Q1 registers. All register addresses not listed in 表 8-10 should be considered as reserved locations with the default setting of 0000h and the register contents should not be modified from its default setting.

表 8-10. Register Map

ADDRESS	REGISTER	RESET VALUE	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
			BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DEVICE SETTINGS AND STATUS INDICATORS (Read-Only Registers)										
00h	ID	52xxh	RESERVED				CHANCNT[3:0]			
			RESERVED							
01h	STATUS	0500h	LOCK	F_RESYNC	REG_MAP	CRC_ERR	CRC_TYPE	RESET	WLENGTH[1:0]	
			RESERVED						DRDY1	DRDY0
GLOBAL SETTINGS ACROSS CHANNELS										
02h	MODE	0510h	RESERVED		REGCRC_EN	RX_CRC_EN	CRC_TYPE	RESET	WLENGTH[1:0]	
			RESERVED			TIMEOUT	RESERVED		DRDY_HiZ	RESERVED
03h	CLOCK	038Eh	RESERVED						CH1_EN	CH0_EN
			CLK_SEL	RESERVED		OSR[2:0]			PWR[1:0]	
04h	GAIN	0000h	RESERVED							
			RESERVED	PGAGAIN1[2:0]			RESERVED	PGAGAIN0[2:0]		
06h	GLOBAL_CHOP_CFG	0600h	RESERVED			GC_DLY[3:0]				GC_EN
			RESERVED							
CHANNEL-SPECIFIC SETTINGS										
09h	CH0_CFG	0000h	RESERVED							
			RESERVED						MUX0[1:0]	
0Ch	RESERVED	8000h	RESERVED							
			RESERVED							
0Eh	CH1_CFG	0000h	RESERVED							
			RESERVED						MUX1[1:0]	
11h	RESERVED	8000h	RESERVED							
			RESERVED							
REGISTER MAP CRC REGISTER (Read-Only Register)										
3Eh	REGMAP_CRC	0000h	REG_CRC[15:8]							
			REG_CRC[7:0]							

表 8-11 shows the codes that are used for access types in this section.

表 8-11. Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.6.1 ID Register (Address = 00h) [reset = 52xxh]

The ID register is shown in 図 8-24 and described in 表 8-12.

Return to the Summary Table.

図 8-24. ID Register

15	14	13	12	11	10	9	8
RESERVED				CHANCNT[3:0]			
R-0101b				R-0010b			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R-xxxxxxxxb							

表 8-12. ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R	0101b	Reserved Always reads 0101b
11:8	CHANCNT[3:0]	R	0010b	Channel count Always reads 0010b
7:0	RESERVED	R	xxxxxxxxb	Reserved Values are subject to change without notice

8.6.2 STATUS Register (Address = 01h) [reset = 0500h]

The STATUS register is shown in 図 8-25 and described in 表 8-13.

Return to the Summary Table.

図 8-25. STATUS Register

15	14	13	12	11	10	9	8
LOCK	F_RESYNC	REG_MAP	CRC_ERR	CRC_TYPE	RESET	WLENGTH[1:0]	
R-0b	R-0b	R-0b	R-0b	R-0b	R-1b	R-01b	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						DRDY1	DRDY0
R-000000b						R-0b	R-0b

表 8-13. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	LOCK	R	0b	SPI interface lock indicator 0b = Unlocked 1b = Locked
14	F_RESYNC	R	0b	ADC resynchronization indicator Bit is set each time the ADC resynchronizes. 0b = No resynchronization 1b = Resynchronization occurred
13	REG_MAP	R	0b	Register map CRC fault indicator 0b = No change in the register map CRC 1b = register map CRC changed
12	CRC_ERR	R	0b	SPI input CRC error indicator 0b = No CRC error 1b = Input CRC error occurred
11	CRC_TYPE	R	0b	CRC type indicator 0b = 16 bit CCITT 1b = 16 bit ANSI
10	RESET	R	1b	Reset status indicator 0b = No reset occurred 1b = Reset occurred
9:8	WLENGTH[1:0]	R	01b	Data word length indicator 00b = 16 bit 01b = 24 bits 10b = 32 bits: LSB zero padding 11b = Reserved
7:2	RESERVED	R	000000b	Reserved Always reads 000000b
1	DRDY1	R	0b	Channel 1 ADC data available indicator 0b = No new data available 1b = New data available
0	DRDY0	R	0b	Channel 0 ADC data available indicator 0b = No new data available 1b = New data available

8.6.3 MODE Register (Address = 02h) [reset = 0510h]

The MODE register is shown in 図 8-26 and described in 表 8-14.

Return to the Summary Table.

図 8-26. MODE Register

15	14	13	12	11	10	9	8
RESERVED		REG_CRC_EN	RX_CRC_EN	CRC_TYPE	RESET	WLENGTH[1:0]	
R/W-00b		R/W-0b	R/W-0b	R/W-0b	R/W-1b	R/W-01b	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			TIMEOUT	RESERVED		DRDY_HiZ	RESERVED
R/W-000b			R/W-1b	R/W-00b		R/W-0b	R/W-0b

表 8-14. MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R/W	00b	Reserved Always write 00b
13	REG_CRC_EN	R/W	0b	Register map CRC enable 0b = Disabled 1b = Enabled
12	RX_CRC_EN	R/W	0b	SPI input CRC enable 0b = Disabled 1b = Enabled
11	CRC_TYPE	R/W	0b	SPI and register map CRC type selection 0b = 16 bit CCITT 1b = 16 bit ANSI
10	RESET	R/W	1b	Reset Write 0b to clear this bit in the STATUS register 0b = No reset occurred 1b = Reset occurred
9:8	WLENGTH[1:0]	R/W	01b	Data word length selection 00b = 16 bits 01b = 24 bits 10b = 32 bits: LSB zero padding 11b = Reserved. Do not use.
7:5	RESERVED	R/W	000b	Reserved Always write 000b
4	TIMEOUT	R/W	1b	SPI Timeout enable 0b = Disabled 1b = Enabled
3:2	RESERVED	R/W	00b	Reserved Always write 00b
1	DRDY_HiZ	R/W	0b	$\overline{\text{DRDY}}$ pin state selection when conversion data is not available 0b = Logic high 1b = High impedance
0	RESERVED	R/W	0b	Reserved Always write 0b

8.6.4 CLOCK Register (Address = 03h) [reset = 038Eh]

The CLOCK register is shown in 図 8-27 and described in 表 8-15.

Return to the Summary Table.

図 8-27. CLOCK Register

15	14	13	12	11	10	9	8
RESERVED						CH1_EN	CH0_EN
R-000000b						R/W-1b	R/W-1b
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLK_SEL	RESERVED		OSR[2:0]			PWR[1:0]	
R/W-1b	R/W-00b		R/W-011b			R/W-10b	

表 8-15. CLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED	R	000000b	Reserved Always reads 000000b
9	CH1_EN	R/W	1b	Channel 1 ADC enable 0b = Disabled 1b = Enabled
8	CH0_EN	R/W	1b	Channel 0 ADC enable 0b = Disabled 1b = Enabled
7	CLK_SEL	R/W	1b	Clock source selection 0b = Internal oscillator 1b = External clock
6:5	RESERVED	R/W	00b	Reserved Always write 00b
4:2	OSR[2:0]	R/W	011b	Modulator oversampling ratio selection 000b = 128 001b = 256 010b = 512 011b = 1024 100b = 2048 101b = 4096 110b = 8192 111b = 16384
1:0	PWR[1:0]	R/W	10b	Power mode selection 00b = Very-low power 01b = Low power 10b = High resolution 11b = High resolution

8.6.5 GAIN Register (Address = 04h) [reset = 0000h]

The GAIN register is shown in 図 8-28 and described in 表 8-16.

Return to the Summary Table.

図 8-28. GAIN Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-00000000b							

7	6	5	4	3	2	1	0
RESERVED	PGAGAIN1[2:0]			RESERVED	PGAGAIN0[2:0]		
R/W-0b	R/W-000b			R/W-0b	R/W-000b		

表 8-16. GAIN Register Field Descriptions

Bit	Field	Type	Reset	Description
15:7	RESERVED	R/W	00000000 0b	Reserved Always write 000000000b
6:4	PGAGAIN1[2:0]	R/W	000b	PGA gain selection for channel 1 000b = 1 001b = 2 010b = 4 011b = 8 100b = 16 101b = 32 110b = 64 111b = 128
3	RESERVED	R/W	0b	Reserved Always write 0b
2:0	PGAGAIN0[2:0]	R/W	000b	PGA gain selection for channel 0 000b = 1 001b = 2 010b = 4 011b = 8 100b = 16 101b = 32 110b = 64 111b = 128

8.6.6 GLOBAL_CHOP_CFG Register (Address = 06h) [reset = 0600h]

The GLOBAL_CHOP_CFG register is shown in 図 8-29 and described in 表 8-17.

Return to the Summary Table.

図 8-29. GLOBAL_CHOP_CFG Register

15	14	13	12	11	10	9	8
RESERVED			GC_DLY[3:0]				GC_EN
R/W-000b			R/W-0011b				R/W-0b

7	6	5	4	3	2	1	0
RESERVED							
R/W-00000000b							

表 8-17. GLOBAL_CHOP_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED	R/W	000b	Reserved Always write 000b
12:9	GC_DLY[3:0]	R/W	0011b	Global chop delay selection Delay in modulator clock periods (t_{MOD}) before measurement begins. 0000b = 2 0001b = 4 0010b = 8 0011b = 16 0100b = 32 0101b = 64 0110b = 128 0111b = 256 1000b = 512 1001b = 1024 1010b = 2048 1011b = 4096 1100b = 8192 1101b = 16484 1110b = 32768 1111b = 65536
8	GC_EN	R/W	0b	Global chop enable 0b = Disabled 1b = Enabled
7:0	RESERVED	R/W	00000000b	Reserved Always write 00000000b

8.6.7 CH0_CFG Register (Address = 09h) [reset = 0000h]

The CH0_CFG register is shown in 図 8-30 and described in 表 8-18.

Return to the Summary Table.

図 8-30. CH0_CFG Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-00000000b							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		RESERVED			RESERVED	MUX0[1:0]	
R/W-00b		R-000b			R/W-0b	R/W-00b	

表 8-18. CH0_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:6	RESERVED	R/W	00000000 00b	Reserved Always write 0000000000b
5:3	RESERVED	R	000b	Reserved Always reads 000b
2	RESERVED	R/W	0b	Reserved Always write 0b
1:0	MUX0[1:0]	R/W	00b	Channel 0 input selection 00b = AIN0P and AIN0N 01b = AIN0 disconnected, ADC inputs shorted 10b = Positive dc test signal 11b = Negative dc test signal

8.6.8 CH1_CFG Register (Address = 0Eh) [reset = 0000h]

The CH1_CFG register is shown in 図 8-31 and described in 表 8-19.

Return to the Summary Table.

図 8-31. CH1_CFG Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-00000000b							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		RESERVED			RESERVED	MUX1[1:0]	
R/W-00b		R-000b			R/W-0b	R/W-00b	

表 8-19. CH1_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:6	RESERVED	R/W	00000000 00b	Reserved Always write 0000000000b
5:3	RESERVED	R	000b	Reserved Always reads 000b
2	RESERVED	R/W	0b	Reserved Always write 0b
1:0	MUX1[1:0]	R/W	00b	Channel 1 input selection 00b = AIN1P and AIN1N 01b = AIN1 disconnected, ADC inputs shorted 10b = Positive dc test signal 11b = Negative dc test signal

8.6.9 REGMAP_CRC Register (Address = 3Eh) [reset = 0000h]

The REGMAP_CRC register is shown in 図 8-32 and described in 表 8-20.

Return to the Summary Table.

図 8-32. REGMAP_CRC Register

15	14	13	12	11	10	9	8
REG_CRC[15:8]							
R-00000000b							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REG_CRC[7:0]							
R-00000000b							

表 8-20. REGMAP_CRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	REG_CRC[15:0]	R	00000000 00000000b	Register map CRC value

9 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

9.1.1 Troubleshooting

表 9-1 lists common issues faced when designing with the ADS130B02-Q1 and the corresponding solutions. This list is not comprehensive.

表 9-1. Troubleshooting Common Issues Using the ADS130B02-Q1

ISSUE	POSSIBLE ROOT CAUSE	POSSIBLE SOLUTION
The F_RESYNC bit is set in the STATUS word even though this bit was already cleared.	The $\overline{\text{SYNC/RESET}}$ pin is being toggled asynchronously to CLKIN.	The $\overline{\text{SYNC/RESET}}$ pin functions as a constant synchronization check, rather than a *convert start* pin. See the *Synchronization* section for more details on the intended usage of the $\overline{\text{SYNC/RESET}}$ pin.
The same ADC conversion data are output twice before changing.	The entire frame is not being sent to the device. The device does not recognize data as being read.	Read all data words in the output data frame, including those for channels that are disabled.

9.1.2 Unused Inputs and Outputs

Leave any unused analog inputs floating or connect them to AGND.

Do not float unused digital inputs because excessive power-supply leakage current can result. Tie all unused digital inputs to the appropriate levels, DVDD or DGND.

Tie the CLKIN pin to DGND if the internal oscillator is used.

Leave the $\overline{\text{DRDY}}$ pin unconnected if unused or connect it to DVDD using a weak pullup resistor.

9.1.3 Antialias Filter

An analog low-pass filter is required in front of each of the ADC channel inputs to prevent out-of-band noise and interferers from coupling into the band of interest. Because the ADS130B02-Q1 is a delta-sigma ADC, the integrated digital filter provides substantial attenuation for frequencies outside of the band of interest up to the frequencies adjacent to f_{MOD}. Therefore, a single-order RC filter with a cutoff frequency set at least two decades below the modulator frequency provides sufficient antialiasing protection in the vast majority of applications. 図 9-1 shows a typical RC filter that yields a cutoff frequency of f_C = 39.8 kHz, which is generally a good starting point for a design that uses f_{MOD} = 4.096 MHz.

Applications that only need to measure dc signals can use much lower filter-cutoff frequencies by increasing the resistor or capacitor values. Larger resistor values have the added benefit of limiting the current into the ADC inputs in case of an overvoltage event.

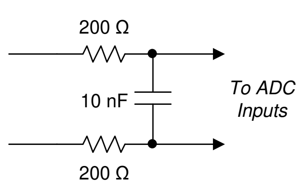


図 9-1. Antialias Filter Example

9.1.4 Minimum Interface Connections

図 9-2 depicts how the ADS130B02-Q1 can be configured for the minimum number of interface pins. This configuration is useful when using data isolation to minimize the number of isolation channels required or when the microcontroller (MCU) pins are limited.

The CLKIN pin requires an LVCMOS clock that can be either generated by the MCU or created using a local LVCMOS output oscillator when the device is configured for use with an external clock. Otherwise tie the CLKIN pin to DGND if the internal oscillator is used. Tie the SYNC/RESET pin to DVDD in hardware if unused. The DRDY pin can be left floating if unused. Connect either SYNC/RESET or DRDY to the MCU to make sure the MCU stays synchronized to ADC conversions. If the MCU provides CLKIN, the CLKIN periods can be counted to determine the sample period rather than forcing synchronization using the SYNC/RESET pin or monitoring the DRDY pin. Synchronization cannot be regained if a bit error occurs on the clock and samples can be missed if the SYNC/RESET or DRDY pins are not used. CS can be tied low in hardware if the ADS130B02-Q1 is the only device on the SPI bus. Make sure the data input and output CRC are enabled and are used to guard against faulty register reads and writes if CS is tied low permanently.

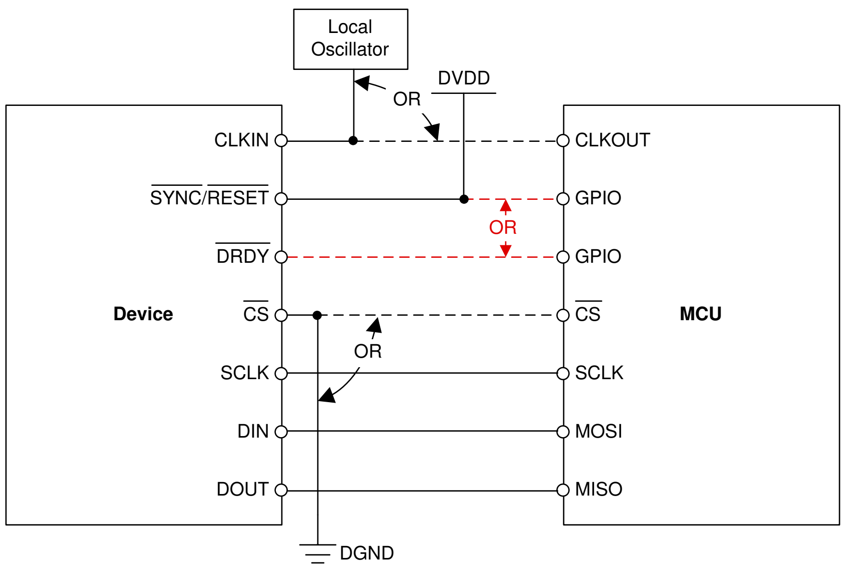


図 9-2. Minimum Connections Required to Operate the ADS130B02-Q1

9.1.5 Multiple Device Configuration

Multiple ADS130B02-Q1 devices can be arranged to capture all signals simultaneously. The same clock must be provided to all devices and the SYNC/RESET pins must be strobed simultaneously at least one time to align the sample periods internally between devices.

The devices can share the same SPI bus where only the CS pins for each device are unique. Each device can be addressed sequentially by asserting CS for the device that the host wishes to communicate with. The DOUT pin remains high impedance when the CS pin is high, allowing the DOUT lines to be shared between devices as long as no two devices sharing the bus simultaneously have their CS pins low. 図 9-3 shows multiple devices configured for simultaneous data acquisition while sharing the same SPI bus.

Monitoring the DRDY output of only one of the devices is sufficient because all devices convert simultaneously.

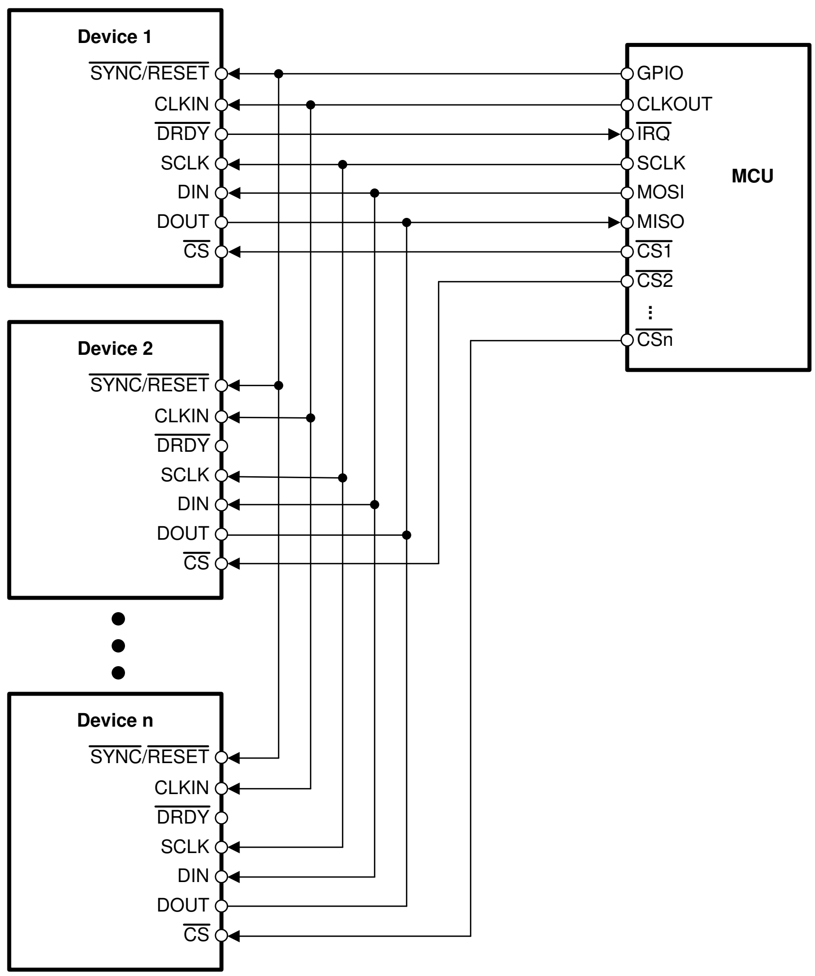


図 9-3. Multiple Device Configuration

9.2 Typical Application

This section describes a typical battery management system (BMS) application circuit using the ADS130B02-Q1. The device serves the following primary functions in this BMS:

- Measure battery current with high resolution and accuracy using a low-side current shunt sensor
- Measure peak currents and detect overcurrent or short-circuit conditions
- Measure battery-pack voltage using a high-voltage resistor divider

図 9-4 shows the front-end for the battery management system circuit design.

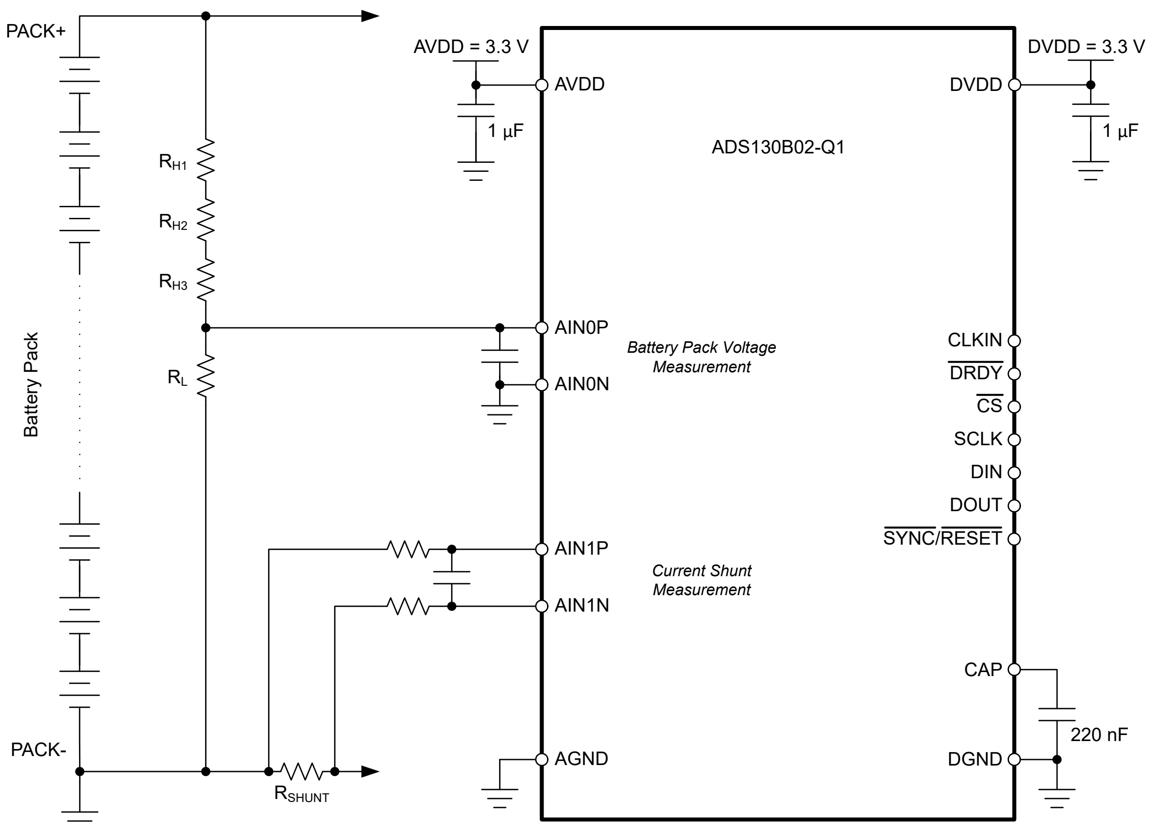


図 9-4. ADS130B02-Q1 in a Typical Battery Management System Application

9.2.1 Design Requirements

表 9-2. Design Requirements

DESIGN PARAMETER	VALUE
Current Measurement	
Current measurement range	±5 kA
Current shunt value	35 µΩ
Update rate	1 ms
Battery-Pack Voltage Measurement	
Voltage measurement range	0 V to 800 V

9.2.2 Detailed Design Procedure

The following sections provide guidelines for selecting the external components and the configuration of the ADS130B02-Q1 for the various measurements in this application example.

9.2.2.1 Current Shunt Measurement

In a typical BMS, the current through the shunt resistor must be measured in both directions for charging and discharging the battery pack. In an overcurrent or short-circuit condition, the current can be as high as I_{BAT_MAX} = ±5 kA in this example application. Therefore, the maximum voltage drop across the shunt is up to V_{SHUNT} = R_{SHUNT} × I_{BAT_MAX} = 35 µΩ × ±4 kA = ±140 mV.

In order to measure this shunt voltage, channel 1 of the ADS130B02-Q1 is configured for gain = 8, which allows differential voltage measurements of V_{IN1} = V_{AIN1P} – V_{AIN1N} = ±V_{REF} / 8 = ±1.2 V / 8 = ±150 mV. The integrated charge pump in the device allows voltage measurements 300 mV below AGND for gains of 4 and higher while using a unipolar analog power supply. This bipolar voltage measurement capability is important because one side of the shunt is connected to the same GND potential as the AGND pin of the ADS130B02-Q1, which means that the absolute voltage that the device must measure is up to 140 mV below AGND.

To enable fast overcurrent detection within 1 ms while providing high accuracy and resolution, the ADS130B02-Q1 is operated at 4 kSPS (OSR = 1024, high-resolution mode) using global-chop mode. Global-chop mode enables measurements with minimal offset error over temperature and time. The conversion time using these settings is 0.754 ms according to 式 6.

9.2.2.2 Battery Pack Voltage Measurement

The 800-V battery-pack voltage is divided down to the voltage range of the ADS130B02-Q1 using a high-voltage resistor divider (R_{H1}, R_{H2}, R_{H3}, and R_L). Gain = 1 is used for channel 0 in this case to allow differential voltage measurements of V_{IN0} = V_{AIN0P} – V_{AIN0N} = ±1.2 V. The battery-pack voltage measurement is a unipolar, single-ended measurement. Thus, only the voltage range from 0 V to 1.2 V of the ADS130B02-Q1 is used. 式 9 calculates the resistor divider ratio.

$$V_{IN} / V_{BAT\_MAX} = 1.2\text{ V} / 800\text{ V} = R_L / (R_L + R_{H1} + R_{H2} + R_{H3}) \quad (9)$$

The leakage current drawn by the resistor divider should be less than 100 µA in this example to avoid unnecessarily draining the battery. The resistance of the divider must therefore be larger than R_{TOTAL} ≥ V_{BAT_MAX} / $I_{LEAKAGE}$ = 800 V / 100 µA = 8 MΩ. The resistor values are chosen as R_{H1} = R_{H2} = R_{H3} = 2.8 MΩ and R_L = 12.4 kΩ. Thus, the maximum voltage across R_L is 1.18 V at V_{BAT_MAX} = 800 V, leaving some headroom to the maximum input voltage of 1.2 V of the ADS130B02-Q1.

The maximum resistance of a single resistor that can be used in an automotive circuit design is often limited to a certain value. Also, the maximum voltage a single resistor can withstand is limited. These reasons are why the high-side resistor of the divider is split into multiple resistors (R_{H1}, R_{H2}, and R_{H3}). Another reason is that in case a single resistor has a short-circuit fault, the remaining resistors still limit the current into the ADS130B02-Q1 analog input pin (AIN0P) to safe levels.

9.2.3 Application Curves

図 9-5 shows the measurement accuracy of the current measurement (ADC channel 1) over temperature for a 0-A current through the shunt. 図 9-6 shows the gain error of the current measurement (ADC channel 1) over temperature excluding the error of the shunt. The offset and gain error are calibrated at 25°C.

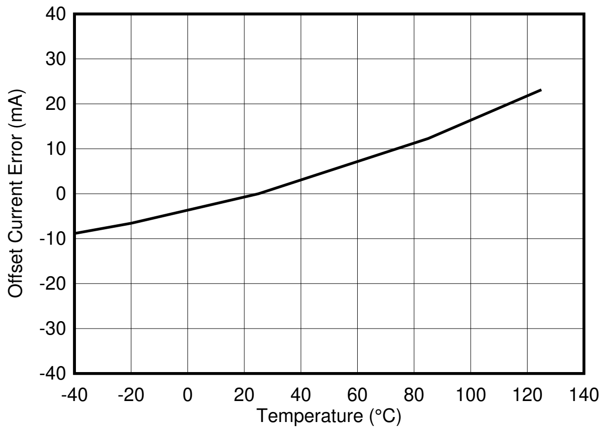


図 9-5. Offset Current Error vs Temperature

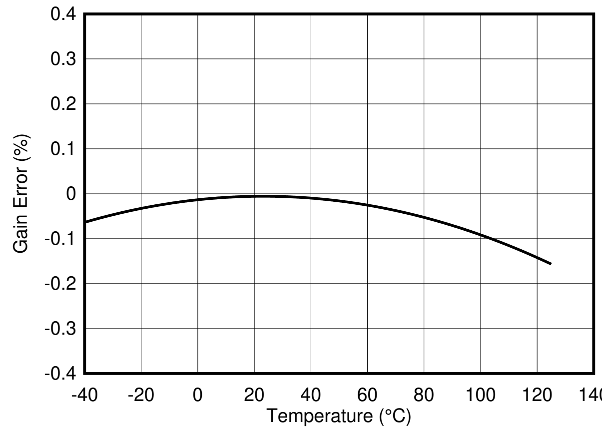


図 9-6. Gain Error vs Temperature

10 Power Supply Recommendations

10.1 CAP Pin Capacitor Requirement

The ADS130B02-Q1 core digital supply voltage of 1.8 V is created by an internal LDO from DVDD. The CAP pin outputs the LDO voltage created from the DVDD supply and requires an external bypass capacitor. Place a 220-nF capacitor on the CAP pin to DGND.

10.2 Power-Supply Sequencing

The power supplies can be sequenced in any order but the analog and digital inputs must never exceed the respective analog or digital power-supply voltage limits.

10.3 Power-Supply Decoupling

Good power-supply decoupling is important to achieve optimum performance. AVDD and DVDD must each be decoupled with a 1-µF capacitor. Place the bypass capacitors as close to the power-supply pins of the device as possible with low-impedance connections. Using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics are recommended for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins can offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes.

11 Layout

11.1 Layout Guidelines

For best performance, dedicate an entire PCB layer to a ground plane and do not route any other signal traces on this layer. However, depending on restrictions imposed by specific end equipment, a dedicated ground plane may not be practical. If ground plane separation is necessary, make a direct connection of the planes at the ADC. Do not connect individual ground planes at multiple locations because this configuration creates ground loops.

Route digital traces away from all analog inputs and associated components in order to minimize interference.

Use C0G capacitors on the analog inputs. Use ceramic capacitors (for example, X7R grade) for the power-supply decoupling capacitors. High-K capacitors (Y5V) are not recommended. Place the required capacitors as close as possible to the device pins using short, direct traces. For optimum performance, use low-impedance connections on the ground-side connections of the bypass capacitors.

When applying an external clock, be sure the clock is free of overshoot and glitches. A source-termination resistor placed at the clock buffer often helps reduce overshoot. Glitches present on the clock input can lead to noise within the conversion data.

11.2 Layout Example

図 11-1 shows an example layout of the ADS130B02-Q1 requiring a minimum of two PCB layers. In general, analog signals and planes are partitioned to the left and digital signals and planes to the right.

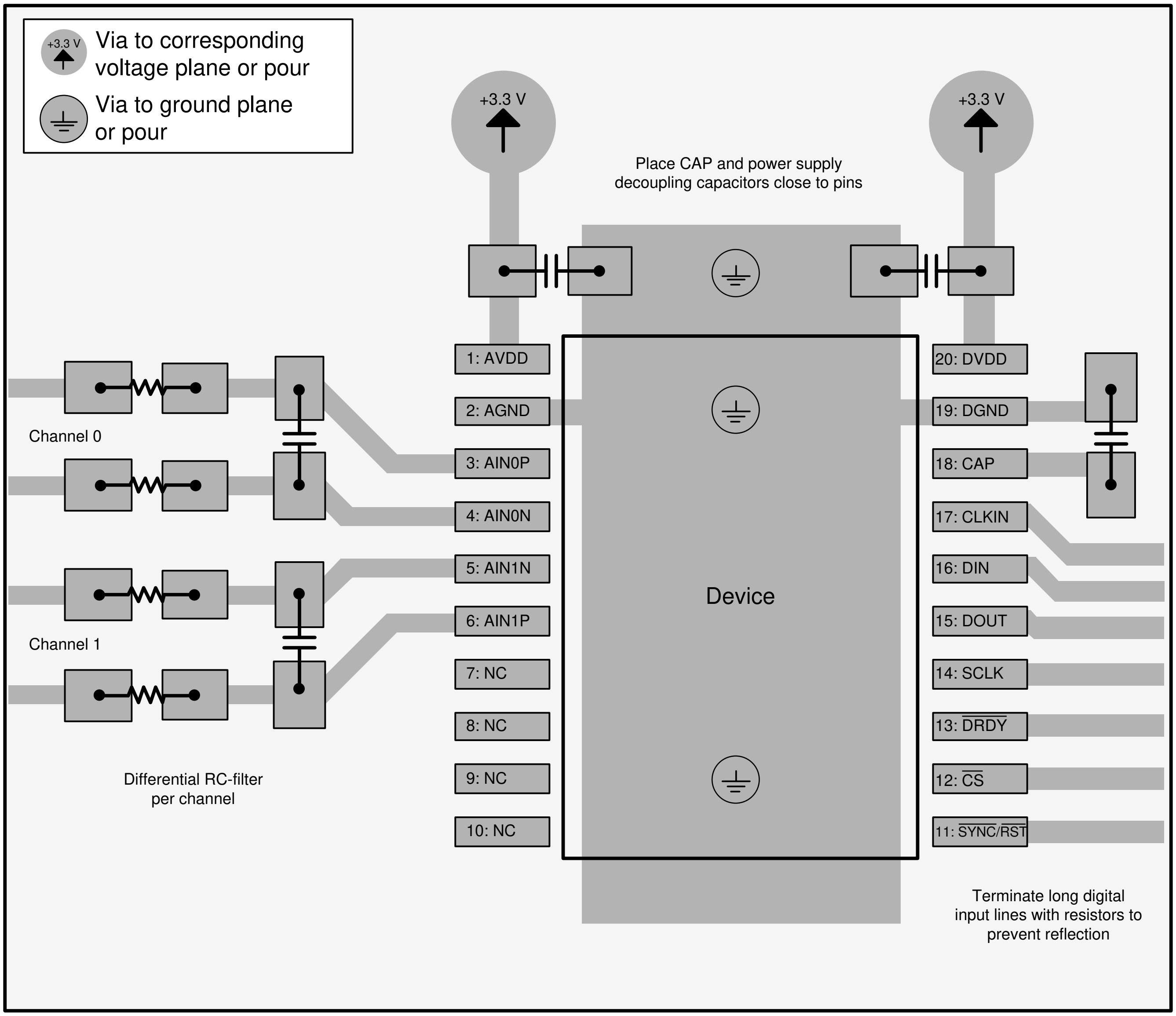


図 11-1. Layout Example

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 サポート・リソース

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12.3 Trademarks

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12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS130B02QPWRQ1	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	A130B02Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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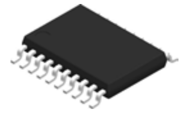
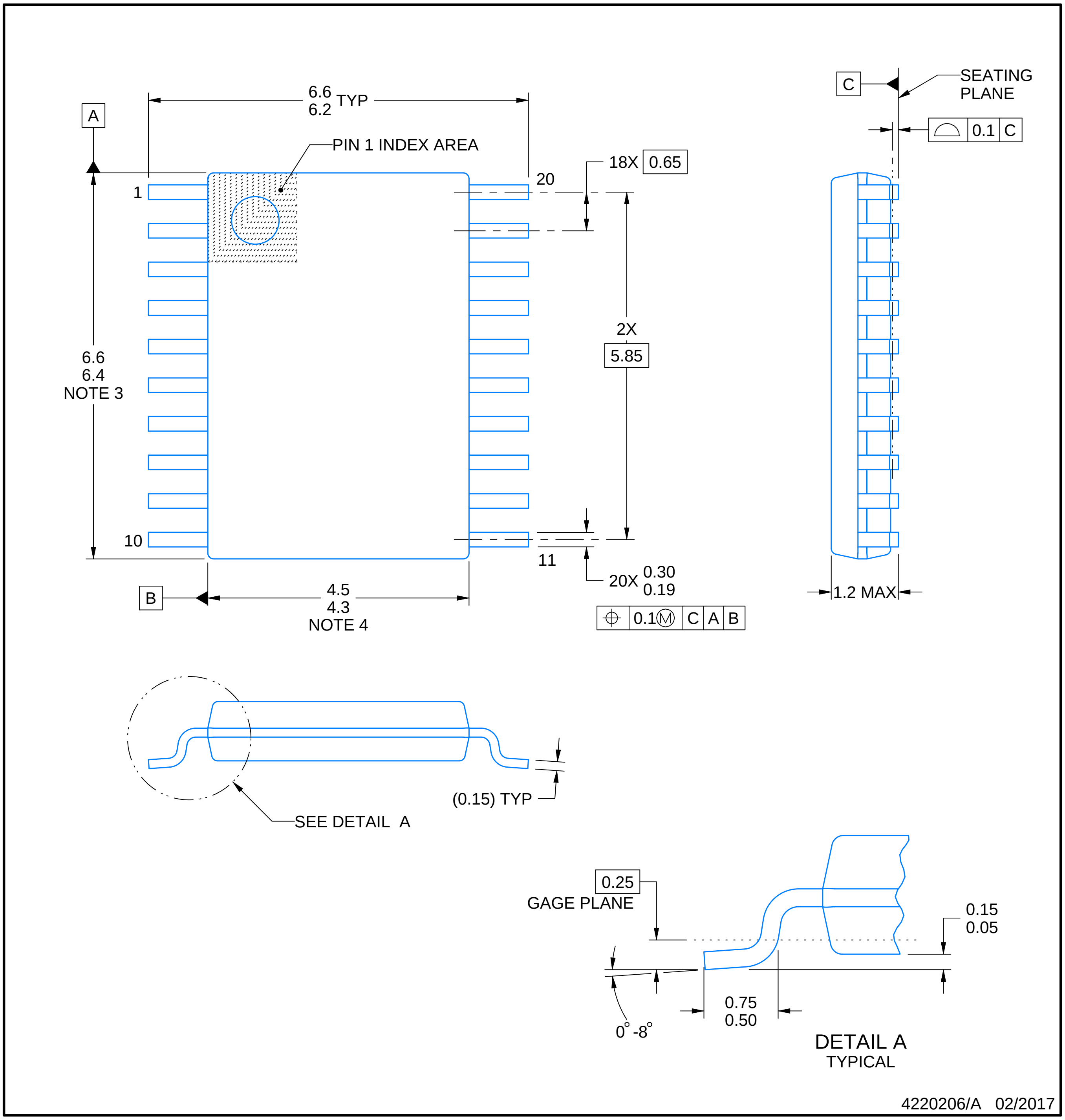
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



PACKAGE OUTLINE

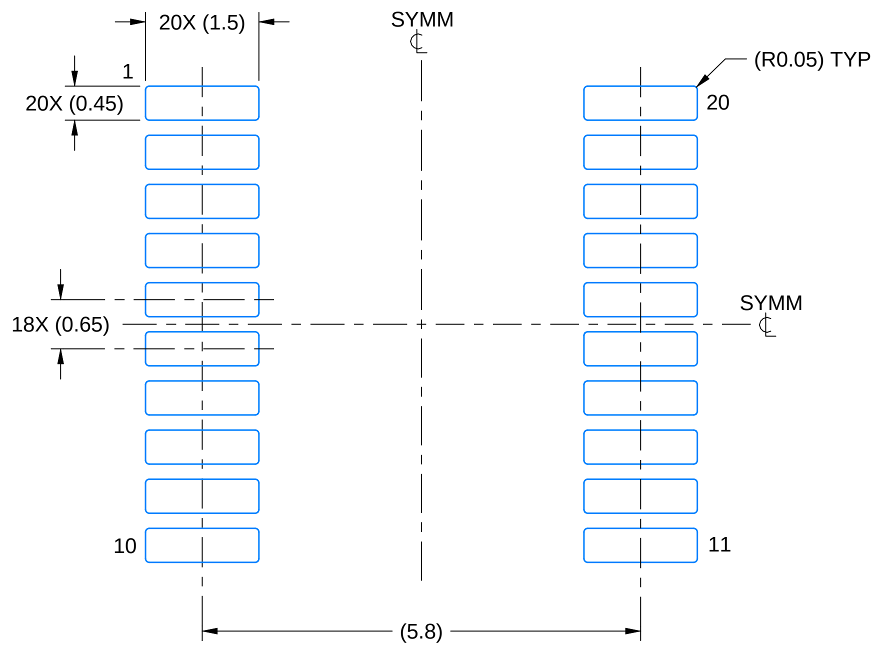
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



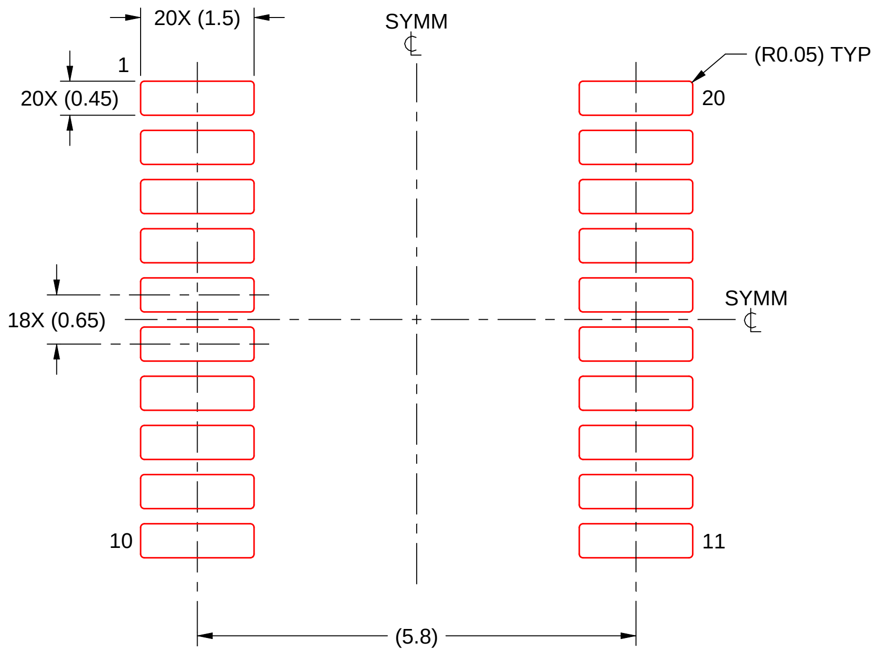
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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