ADS7038-Q1 小型の 8 チャネル、12 ビット ADC、SPI インターフェイス、GPIO、CRC 搭載

1 特長

- 車載アプリケーション用に AEC-Q100 認定取得済み
  - 温度グレード 1：-40℃ ~ 125℃、T_A
- 小型のパッケージ
  - WQFN 3mm × 3mm
  - ウェッタブル・フランクによりハンダ接合部を目視検査可能
- 8 つのチャネルを次の任意の組み合わせに構成可能
  - 最大 8 つのアナログ入力、デジタル入力、またはデジタル出力
- GPIO による I/O の拡張
  - オープン・ドレイン、プッシュプル・デジタル出力
- アナログ・ウォッチドッグ
  - チャネルごとにスレッショルドをプログラム可能
  - 過渡除去用のイベント・カウンタ
- 広い動作範囲
  - AVDD：2.35V ~ 5.5V
  - DVDD：1.65V ~ 5.5V
- 拡張 SPI デジタル・インターフェイス：
  - 高速 (60MHz) インターフェイス
- CRC を使用した読み取り / 書き込み動作：
  - データ読み取り / 書き込み時の CRC
  - 起動構成時の CRC
- 平均化フィルタをプログラム可能：
  - 平均化のサンプル・サイズをプログラム可能
  - 内部変換による平均化
  - 16 ビット分解能
- 最大 3.2MSPS の速度のターボ・コンパレータ・モード

2 アプリケーション

- バッテリ管理システム (BMS)
- 車載クラスタ・ディスプレイ
- インバータおよびモータ制御
- オンボード・チャージャ (OBC) とワイヤレス・チャージャ

3 概要

ADS7038-Q1 は、使いやすい 8 チャネル、多重化、12 ビット、1MSPS、逐次比較型アナログ / デジタル・コンバータ (SAR ADC) です。8 つのチャネルは、アナログ入力、デジタル入力、デジタル出力のいずれかとして独立して構成可能です。このデバイスは、ADC 変換プロセス用の発振器を内蔵しています。

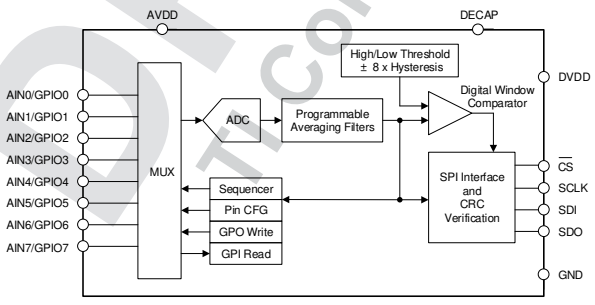
ADS7038-Q1 は SPI 互換のインターフェイスを使用して通信を行い、自律モードまたはシングル・ショット変換モードで動作します。ADS7038-Q1 は、プログラム可能な高および低スレッショルド、ヒステリシス、イベント・カウンタを備えたデジタル・ウィンドウ・コンパレータを使用して、チャネルごとのイベント・トリガ割り込みによるアナログ・ウォッチドッグ機能を実装しています。ADS7038-Q1 は、データの読み取り / 書き込み動作と起動構成のための巡回冗長性検査 (CRC) を内蔵しています。

製品情報 (1) (1 ページ)

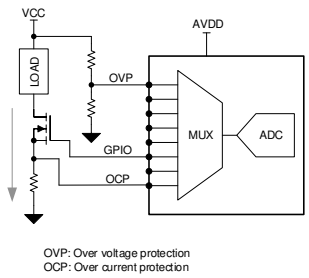
型番	パッケージ	本体サイズ (公称)
ADS7038-Q1	WQFN (16)	3.00mm × 3.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

Device Block Diagram



Example System Architecture



ADS7038-Q1 のブロック図とアプリケーション

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (May 2020) to Revision A (November 2020)	Page
• ドキュメントのステータスを事前情報から量産データに変更	1

5 Device Comparison Table

PART NUMBER	DESCRIPTION	CRC MODULE	ZERO-CROSSING-DETECT (ZCD) MODULE	ROOT-MEAN-SQUARE (RMS) MODULE
ADS7028	8-channel, 12-bit ADC with SPI interface and GPIOs	Yes	Yes	Yes
ADS7038		Yes	No	No
ADS7038-Q1		Yes	No	No

6 Pin Configuration and Functions

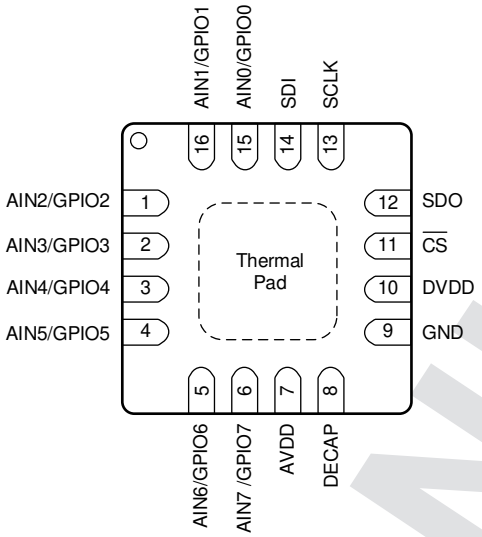


図 6-1. RTE Package, 16-Pin WQFN, Top View

Pin Functions

PIN		FUNCTION[1]	DESCRIPTION
NAME	NO.		
AIN0/GPIO0	15	AI, DI, DO	Channel 0; can be configured as either an analog input (default), digital input, or digital output.
AIN1/GPIO1	16	AI, DI, DO	Channel 1; can be configured as either an analog input (default), digital input, or digital output.
AIN2/GPIO2	1	AI, DI, DO	Channel 2; can be configured as either an analog input (default), digital input, or digital output.
AIN3/GPIO3	2	AI, DI, DO	Channel 3; can be configured as either an analog input (default), digital input, or digital output.
AIN4/GPIO4	3	AI, DI, DO	Channel 4; can be configured as either an analog input (default), digital input, or digital output.
AIN5/GPIO5	4	AI, DI, DO	Channel 5; can be configured as either an analog input (default), digital input, or digital output.
AIN6/GPIO6	5	AI, DI, DO	Channel 6; can be configured as either an analog input (default), digital input, or digital output.
AIN7/GPIO7	6	AI, DI, DO	Channel 7; can be configured as either an analog input (default), digital input, or digital output.
AVDD	7	Supply	Analog supply input, also used as the reference voltage to the ADC; connect a 1-µF decoupling capacitor to GND.
$\overline{CS}$	11	DI	Chip-select input pin; active low. The device takes control of the data bus when $\overline{CS}$ is low. The device starts converting the active input channel on the rising edge of $\overline{CS}$. SDO goes hi-Z when $\overline{CS}$ is high.
DECAP	8	Supply	Connect a 1-µF decoupling capacitor to GND for the internal power supply.
DVDD	10	Supply	Digital I/O supply voltage; connect a 1-µF decoupling capacitor to GND.
GND	9	Supply	Ground for the power supply; all analog and digital signals are referred to this pin voltage.
SCLK	13	DI	Serial clock for the SPI interface.
SDI	14	DI	Serial data in for the device.
SDO	12	DO	Serial data out for the device.
Thermal pad	—	Supply	Exposed thermal pad; connect to GND.

(1) AI = analog input, DI = digital input, and DO = digital output.

7 Specifications

7.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
DVDD to GND	–0.3	5.5	V
AVDD to GND	–0.3	5.5	V
AINx/GPOx(3) to GND	GND – 0.3	AVDD + 0.3	V
Digital input to GND	GND – 0.3	5.5	V
Current through any pin except supply pins(2)	–10	10	mA
Junction temperature, T_J	–40	125	°C
Storage temperature, T_{stg}	–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Pin current must be limited to 10 mA or less.
(3) AINx/GPIOx refers to pins 1, 2, 3, 4, 5, 6, 15, and 16.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011; corner pins (1, 4, 5, 8, 9, 12, 13, 16)	±750	
		Charged-device model (CDM), per AEC Q100-011; all other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
AVDD	Analog supply voltage		2.35	3.3	5.5	V
DVDD	Digital supply voltage		1.65	3.3	5.5	V
ANALOG INPUTS						
FSR	Full-scale input range	AIN_X - GND	0		AVDD	V
V_{IN}	Absolute input voltage	AIN_X - GND	–0.1		AVDD + 0.1	V
TEMPERATURE RANGE						
T_A	Ambient temperature		–40	25	125	℃

(1) AINx refers to AIN0, AIN1, AIN2, AIN3, AIN4, AIN5, AIN6, and AIN7.

7.4 Thermal Information

THERMAL METRIC[1]		ADS7038-Q1 RTE (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	24.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	9.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

at AVDD = 2.35 V to 5 V, DVDD = 1.65 V to 5.5 V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
C_{SH}	Sampling capacitance			12		pF
DC PERFORMANCE						
	Resolution	No missing codes		12		bits
DNL	Differential nonlinearity		–0.75	±0.25	0.75	LSB
INL	Integral nonlinearity		–1.4	±0.4	1.4	LSB
$V_{(OS)}$	Input offset error	Post offset calibration	–2	±0.08	2	LSB
	Input offset thermal drift	Post offset calibration		±1		ppm/°C
G_E	Gain error		–0.075	±0.05	0.075	%FSR
	Gain error thermal drift			±1		ppm/°C
AC PERFORMANCE						
SINAD	Signal-to-noise + distortion ratio	AVDD = 5 V, f_{IN} = 2 kHz	70.2	72.9		dB
		AVDD = 3 V, f_{IN} = 2 kHz	70.2	72.7		
SNR	Signal-to-noise ratio	AVDD = 5 V, f_{IN} = 2 kHz	71.2	73.1		dB
		AVDD = 3 V, f_{IN} = 2 kHz	70.5	72.9		
THD	Total harmonic distortion	f_{IN} = 2 kHz		–87.5		dB
SFDR	Spurious-free dynamic range	f_{IN} = 2 kHz		91		dB
	Isolation crosstalk	f_{IN} = 100 kHz		–100		dB
DECAP Pin						
	Decoupling capacitor on DECAP pin		0.22	1	4.7	µF
SPI INTERFACE ($\overline{CS}$, SCLK, SDI, SDO)						
V_{IH}	Input high logic level		0.7 x DVDD		5.5	V
V_{IL}	Input low logic level		–0.3		0.3 x DVDD	V
V_{OH}	Output high logic level	Source current = 2 mA, DVDD > 2 V	0.8 x DVDD		DVDD	V
		Source current = 2 mA, DVDD ≤ 2 V	0.7 x DVDD		DVDD	
V_{OL}	Output low logic level	Sink current = 2 mA, DVDD > 2 V	0		0.4	V
		Sink current = 2 mA, DVDD ≤ 2 V	0		0.2 x DVDD	
GPIOs						
V_{IH}	Input high logic level		0.7 x AVDD		AVDD + 0.3	V
V_{IL}	Input low logic level		–0.3		0.3 x AVDD	V
	Input leakge current	GPIO configured as input		10	100	nA
V_{OH}	Output high logic level	GPO_DRIVE_CFG = push-pull, I_{SOURCE} = 2 mA	0.8 x AVDD		AVDD	V
V_{OL}	Output low logic level	I_{SINK} = 2 mA	0		0.2 x AVDD	V
I_{OH}	Output high source current	V_{OH} > 0.7 x AVDD			5	mA
I_{OL}	Output low sink current	V_{OL} < 0.3 x AVDD			5	mA
POWER-SUPPLY CURRENTS						
I_{AVDD}	Analog supply current	Full throughput, AVDD = 5 V		490	600	µA
		Full throughput, AVDD = 3 V		455	550	
		No conversion, AVDD = 5 V		7	25	

7.6 Timing Requirements

at AVDD = 5 V, DVDD = 1.65 V to 5.5 V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C ; typical values at T_A = 25°C

		MIN	MAX	UNIT
CONVERSION CYCLE				
f_{CYCLE}	Sampling frequency		1000	kSPS
t_{CYCLE}	ADC cycle-time period	1 / f_{CYCLE}		s
t_{ACQ}	Acquisition time (CONV_MODE = 00b or 01b)	400		ns
	Acquisition time in turbo comparator mode (CONV_MODE = 10b)	90		
t_{QUIET}	Quiet acquisition time	10		ns
t_{WH_CSZ}	Pulse duration: $\overline{CS}$ high	230		ns
t_{WL_CSZ}	Pulse duration: $\overline{CS}$ low	200		ns
SPI INTERFACE TIMINGS				
f_{CLK}	Maximum SCLK frequency		60	MHz
t_{CLK}	Minimum SCLK time period	16.67		ns
t_{PH_CK}	SCLK high time	0.45	0.55	t_{CLK}
t_{PL_CK}	SCLK low time	0.45	0.55	t_{CLK}
t_{SU_CSCK}	Setup time: $\overline{CS}$ falling to the first SCLK capture edge	5.5		ns
t_{SU_CKDI}	Setup time: SDI data valid to the SCLK capture edge	5		ns
t_{HT_CKDI}	Hold time: SCLK capture edge to data valid on SDI	3.5		ns
t_{D_CKCS}	Delay time: last SCLK falling to $\overline{CS}$ rising	9		ns

7.7 Switching Characteristics

at AVDD = 5 V, DVDD = 1.65 V to 5.5 V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C ; typical values at T_A = 25°C

PARAMETER		Test Conditions	MIN	MAX	UNIT
CONVERSION CYCLE					
t_{CONV}	ADC comparison time in turbo comparator mode	CONV_MODE = 10b		192	ns
	ADC conversion time	CONV_MODE - 00b or 01b		600	
RESET and ALERT					
t_{PU}	Power-up time for device	AVDD ≥ 2.35 V, C_{DECAP} = 1 µF		5	ms
t_{RST}	Delay time; RST bit = 1b to device reset complete(1)			5	ms
t_{ALERT_HI}	ALERT high period	ALERT_LOGIC[1:0] = 1x	50	150	ns
t_{ALERT_LO}	ALERT low period	ALERT_LOGIC[1:0] = 1x	50	150	ns
SPI INTERFACE TIMINGS					
t_{DEN_CSDO}	Delay time: $\overline{CS}$ falling to data enable			15	ns
t_{DZ_CSDO}	Delay time: $\overline{CS}$ rising to SDO going Hi-Z			21	ns
t_{D_CKDO}	Delay time: SCLK launch edge to (next) data valid on SDO			16	ns

(1) RST bit is automatically reset to 0b after t_{RST}.

7.8 Timing Diagrams

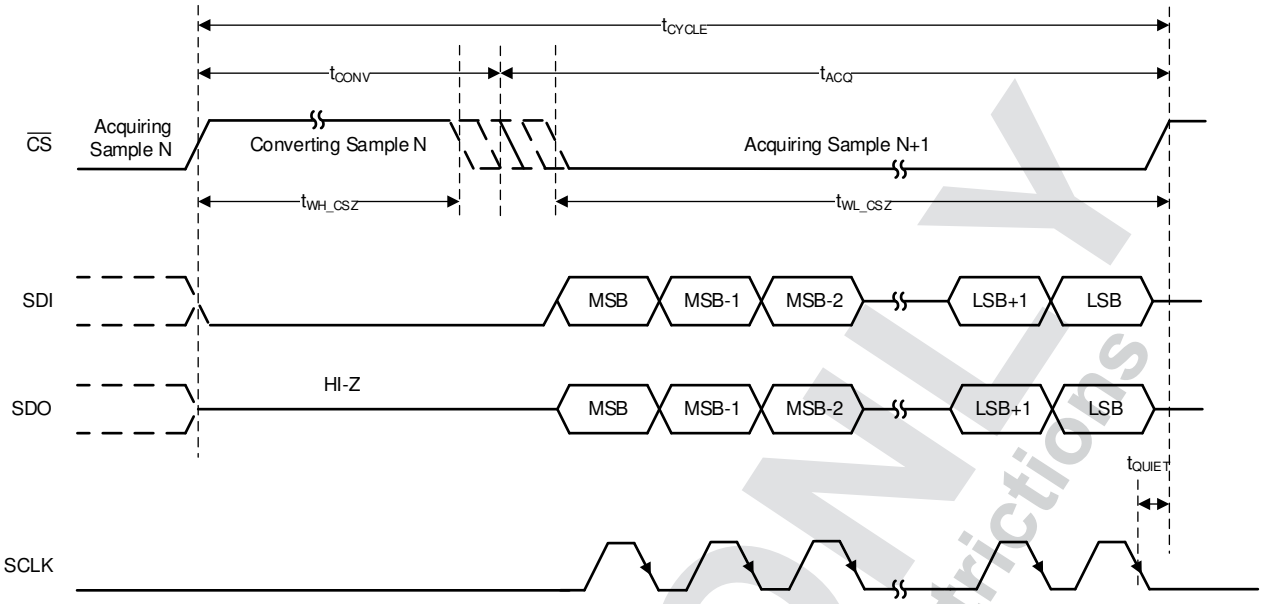
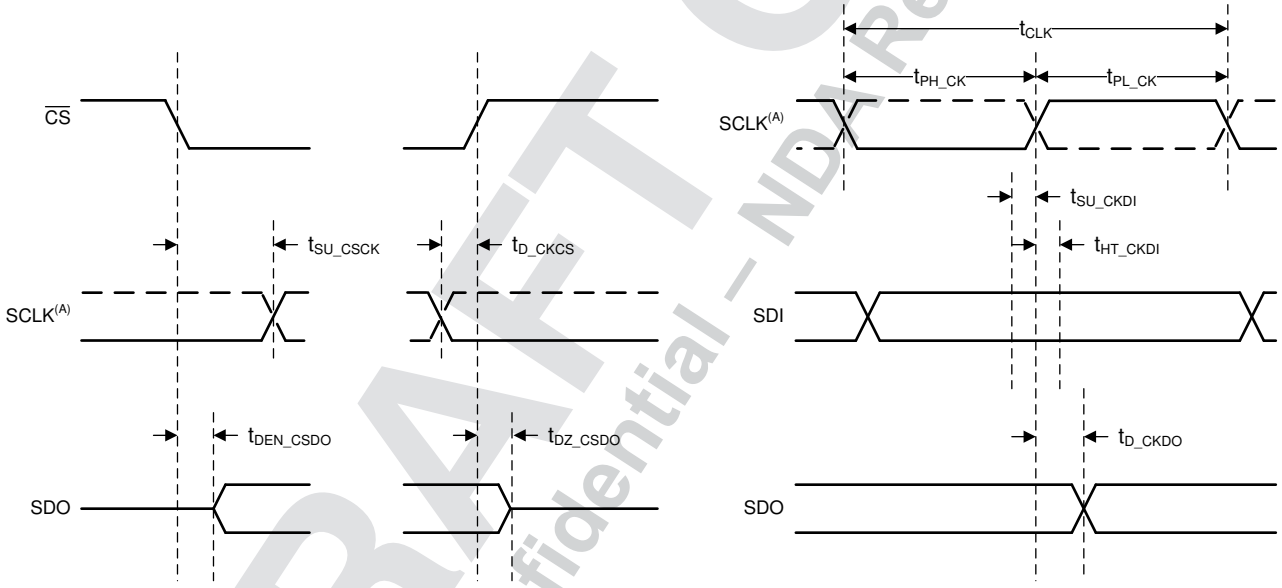


図 7-1. Conversion Cycle Timing

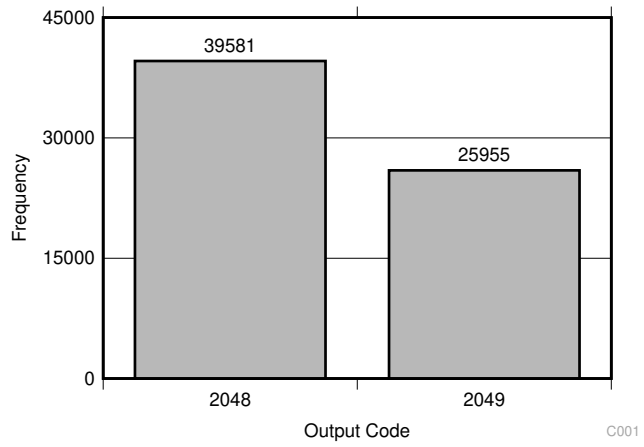


A. The SCLK polarity, launch edge, and capture edge depend on the SPI protocol selected.

図 7-2. SPI-Compatible Serial Interface Timing

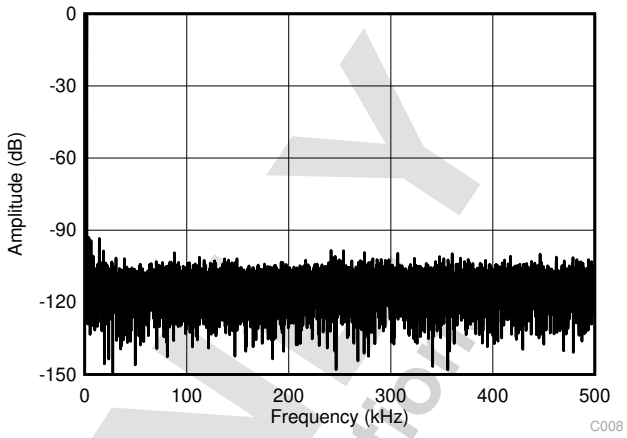
7.9 Typical Characteristics

at T_A = 25°C, AVDD = 5 V, DVDD = 1.8 V, and f_{SAMPLE} = 1 MSPS (unless otherwise noted)



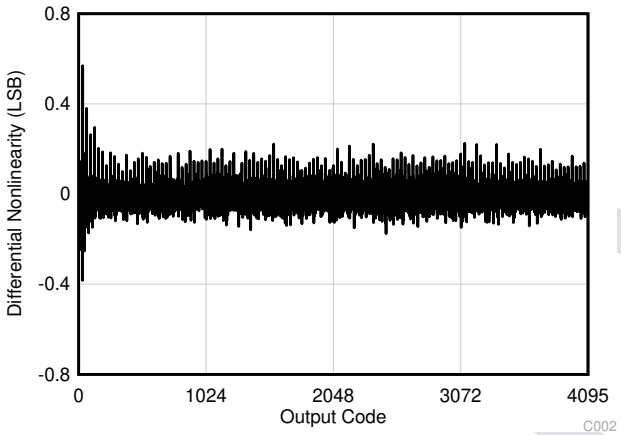
Standard deviation = 0.49 LSB

図 7-3. DC Input Histogram



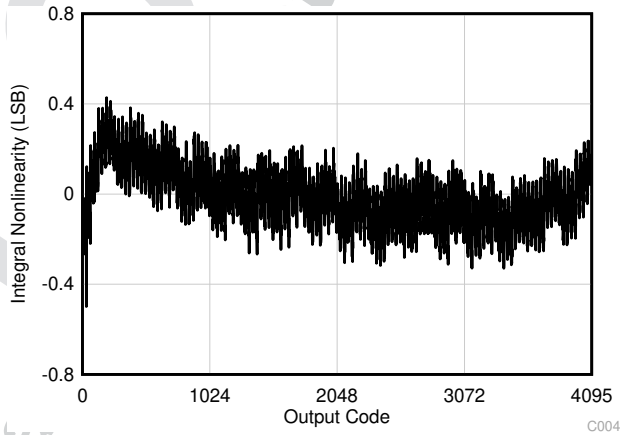
f_{IN} = 2 kHz, SNR = 73.2 dB, THD = –92.1 dB

図 7-4. Typical FFT



Typical DNL = ±0.5 LSB

図 7-5. Typical DNL



Typical INL = ±0.5 LSB

図 7-6. Typical INL

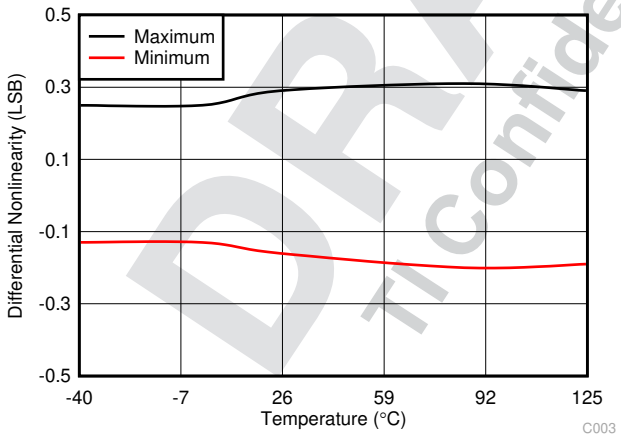


図 7-7. DNL vs Temperature

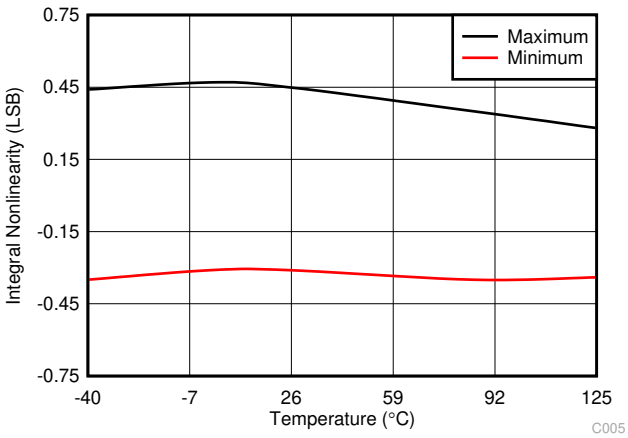


図 7-8. INL vs Temperature

7.9 Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 1.8 V, and f_{SAMPLE} = 1 MSPS (unless otherwise noted)

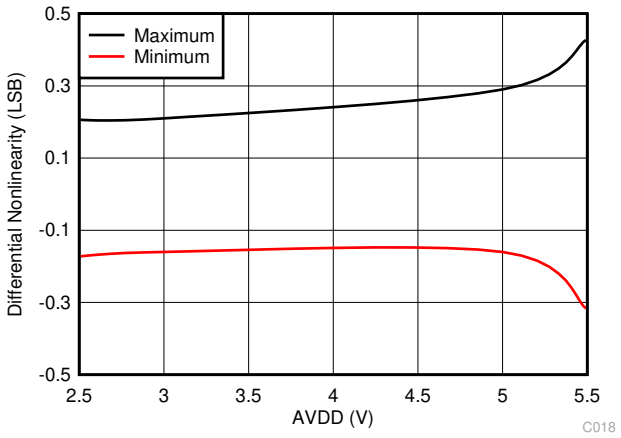


図 7-9. DNL vs AVDD

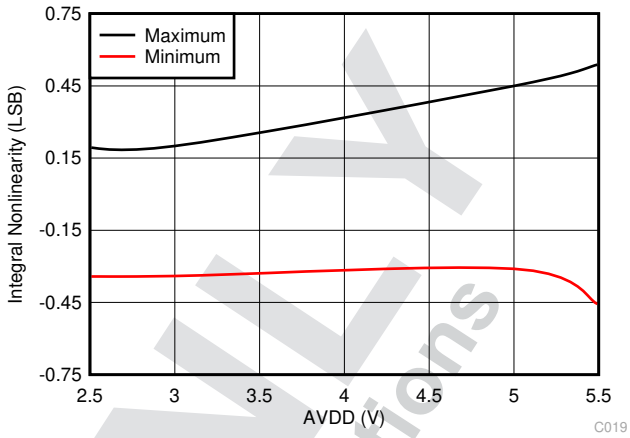


図 7-10. INL vs AVDD

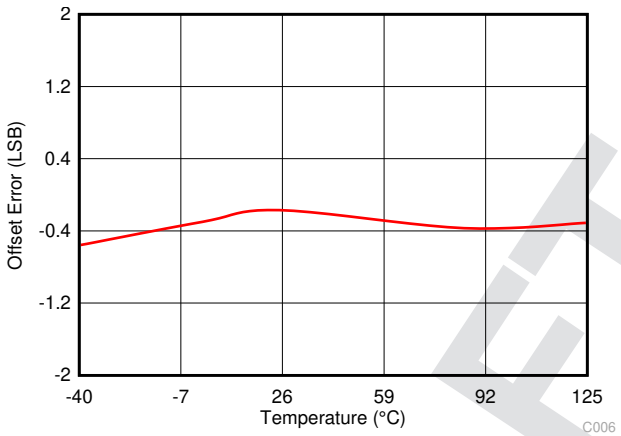


図 7-11. Offset Error vs Temperature

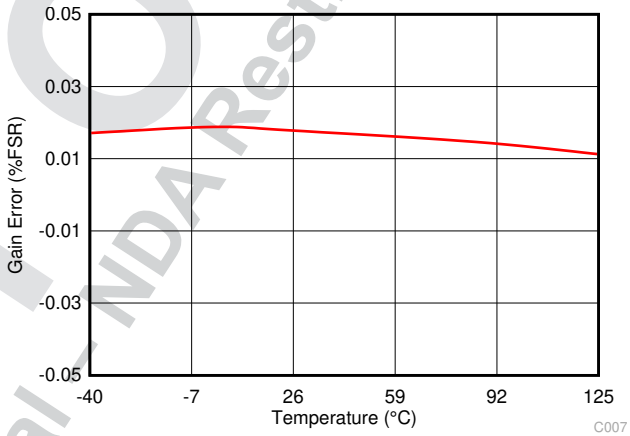


図 7-12. Gain Error vs Temperature

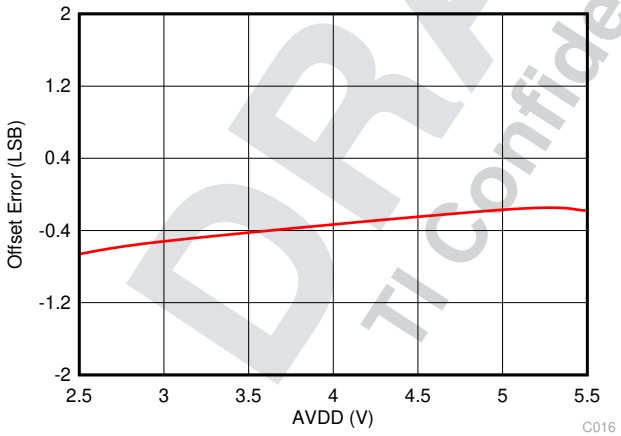


図 7-13. Offset Error vs AVDD

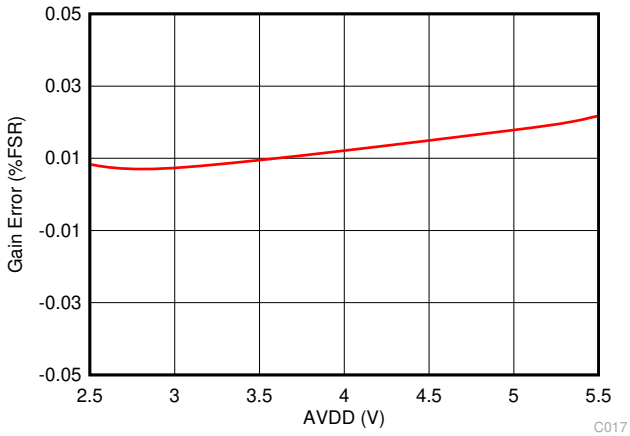


図 7-14. Gain Error vs AVDD

7.9 Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 1.8 V, and f_{SAMPLE} = 1 MSPS (unless otherwise noted)

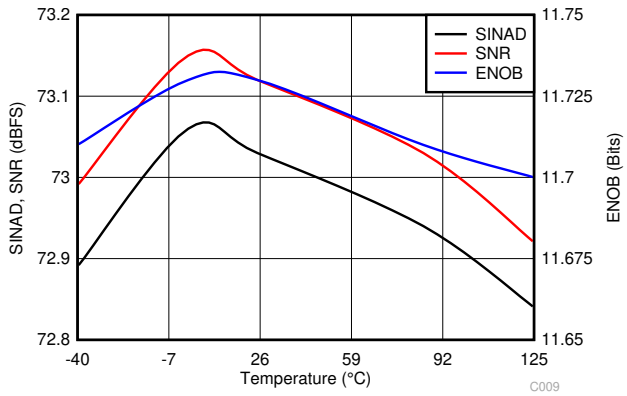


図 7-15. Noise Performance vs Temperature

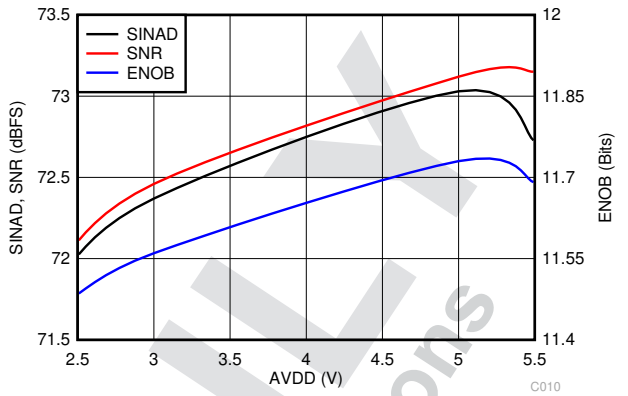


図 7-16. Noise Performance vs AVDD

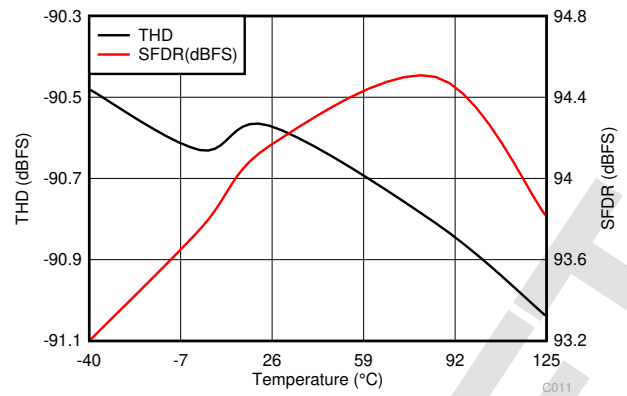


図 7-17. Distortion Performance vs Temperature

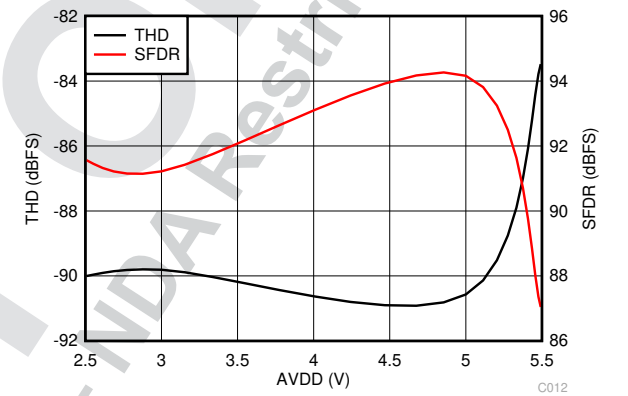


図 7-18. Distortion Performance vs AVDD

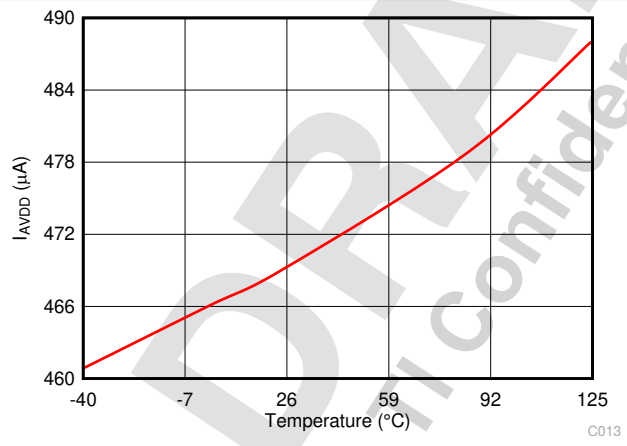


図 7-19. Analog Supply Current vs Temperature

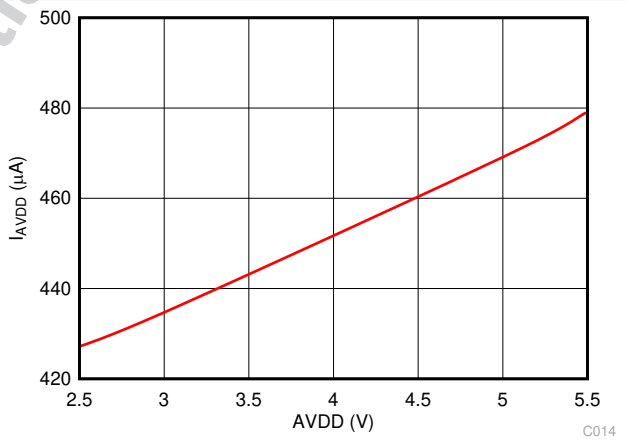


図 7-20. Analog Supply Current vs AVDD

7.9 Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 1.8 V, and f_{SAMPLE} = 1 MSPS (unless otherwise noted)

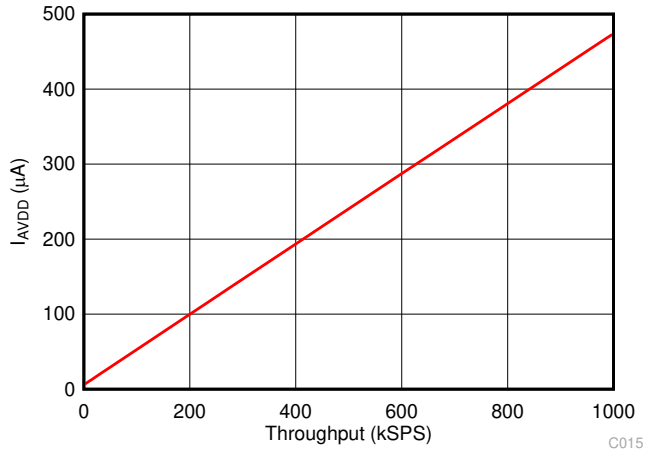


図 7-21. Analog Supply Current vs Throughput

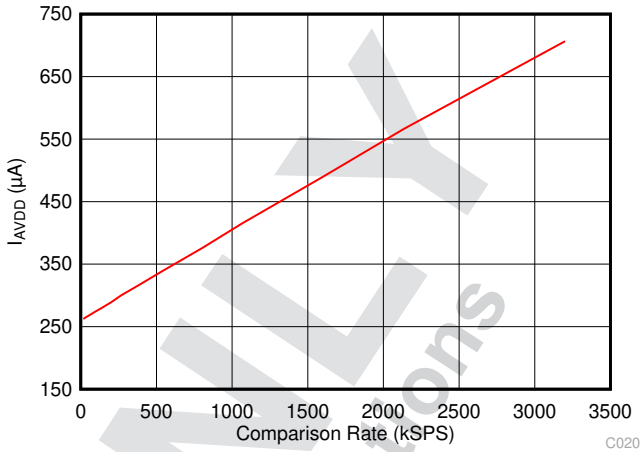


図 7-22. Analog Supply Current vs Comparison Rate (OSC_SEL = 0) in Turbo Comparator Mode

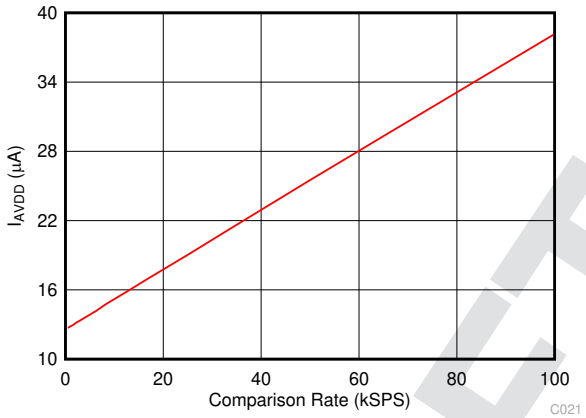


図 7-23. Analog Supply Current vs Comparison Rate (OSC_SEL = 1) in Turbo Comparator Mode

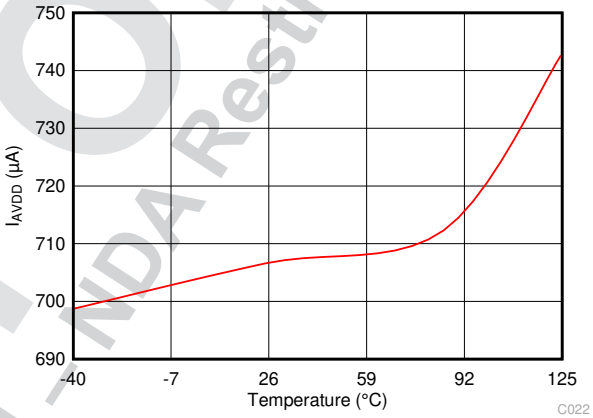


図 7-24. Analog Supply Current vs Temperature (OSC_SEL = 0, CLK_DIV = 0) in Turbo Comparator Mode

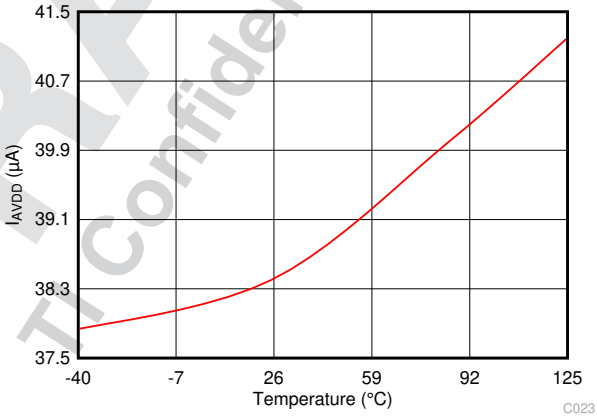


図 7-25. Analog Supply Current vs Temperature (OSC_SEL = 1, CLK_DIV = 0) in Turbo Comparator Mode

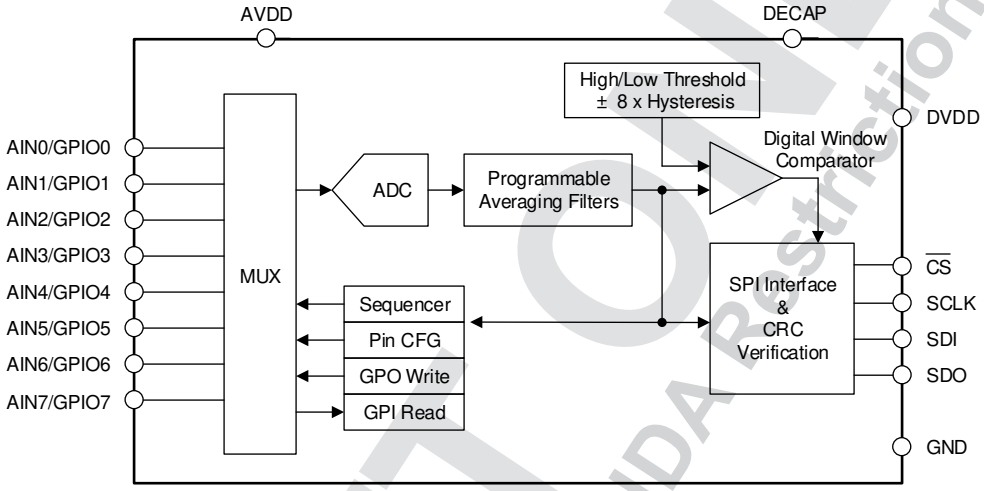
8 Detailed Description

8.1 Overview

The ADS7038-Q1 is a small, eight-channel, multiplexed, 12-bit, 1-MSPS, analog-to-digital converter (ADC) with an enhanced-SPI serial interface. The eight channels of the ADS7038-Q1 can be individually configured as either analog inputs, digital inputs, or digital outputs. The device includes a digital window comparator that can be used to alert the host when a programmed high or low threshold is crossed on any input channel. The device uses an internal oscillator for conversion. The ADC can be used in manual mode for reading ADC data over the SPI interface or in autonomous and turbo comparator modes for monitoring the analog inputs without an active SPI interface.

The device features a programmable averaging filter that outputs a 16-bit result for enhanced resolution.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Multiplexer and ADC

The eight channels of the multiplexer can be independently configured as ADC inputs or general-purpose inputs/outputs (GPIOs). As shown in 図 8-1, every AINx/GPIOx channel has ESD protection diodes to AVDD and GND. On power-up or after device reset, all eight multiplexer channels are configured as analog inputs.

図 8-1 shows the equivalent circuit for pins configured as analog inputs. The ADC sampling switch is represented by an ideal switch (SW) in series with the resistor (R_{SW}, typically 150 Ω) and the sampling capacitor (C_{SH}).

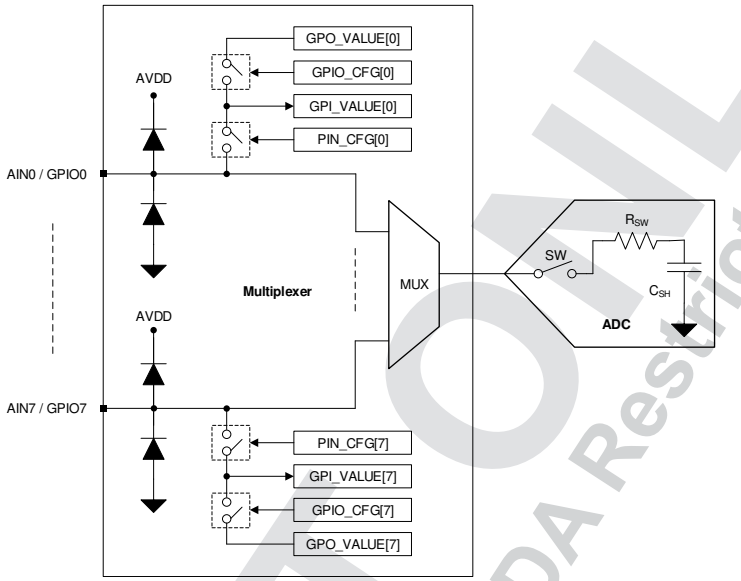


図 8-1. Analog Inputs, GPIOs, and ADC Connections

The switch SW is closed to allow the signal on the selected analog input channel to charge the internal sampling capacitor during acquisition time. The switch SW is opened to disconnect the sampling capacitor on the $\overline{CS}$ rising edge and the analog-to-digital conversion process begins.

The multiplexer channels can be configured as GPIOs using the PIN_CFG register. The direction of a GPIO (either as an input or an output) can be set in the GPIO_CFG register. The logic level on all device channels can be read from the GPI_VALUE register. The digital outputs can be configured by writing to the GPO_VALUE register. The digital outputs can be configured as either open-drain or push-pull in the GPO_DRIVE_CFG register.

8.3.2 Reference

The device uses the analog supply voltage (AVDD) as the reference for the analog-to-digital conversion process. TI recommends connecting a 1-µF, low-equivalent series resistance (ESR) ceramic decoupling capacitor between the AVDD and GND pins.

8.3.3 ADC Transfer Function

The ADC output is in straight binary format. 式 1 computes the ADC resolution:

$$1\ LSB = V_{REF} / 2^N \quad (1)$$

where:

- V_{REF} = AVDD
- N = 12

図 8-2 and 表 8-1 detail the transfer characteristics for the device.

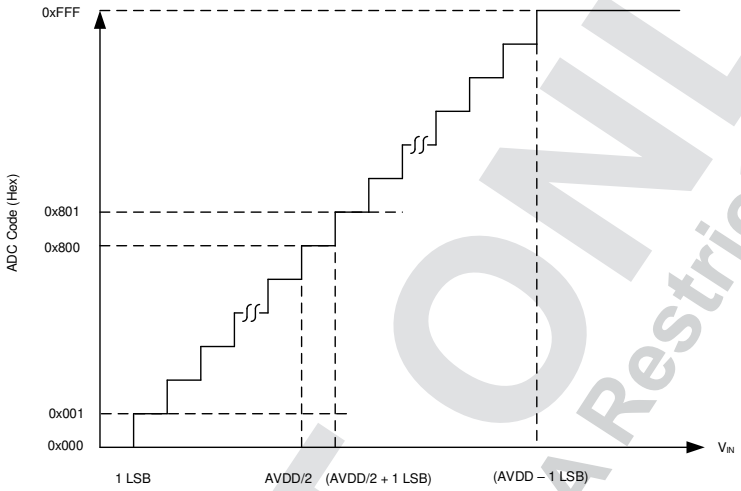


図 8-2. Ideal Transfer Characteristics

表 8-1. Transfer Characteristics

INPUT VOLTAGE	CODE	IDEAL OUTPUT CODE
≤1 LSB	Zero	000
1 LSB to 2 LSBs	Zero + 1	001
(AVDD / 2) to (AVDD / 2) + 1 LSB	Mid-scale code	800
(AVDD / 2) + 1 LSB to (AVDD / 2) + 2 LSB	Mid-scale code + 1	801
≥ AVDD – 1 LSB	Full-scale code	FFF

8.3.4 ADC Offset Calibration

The variation in ADC offset error resulting from changes in temperature or AVDD can be calibrated by setting the CAL bit in the GENERAL_CFG register. The CAL bit is reset to 0 after calibration. The host can poll the CAL bit to check the ADC offset calibration completion status.

Multiplexer sequencing must be stopped (SEQ_START = 0b) before initiating offset calibration.

8.3.5 Oscillator and Timing Control

The device uses an internal oscillator for conversions. The host initiates the first conversion and subsequent conversions are generated internally by the device when using the averaging module. However, in the autonomous mode of operation, the start of the conversion signal is generated by the device. As described in 表 8-2, the sampling rate can be controlled by the OSC_SEL and CLK_DIV register fields when the device initiates conversion internally.

The conversion time of the device, given by t_{CONV} in the *Switching Characteristics* table, is independent of the OSC_SEL and CLK_DIV configuration.

表 8-2. Configuring Sampling Rate for Internal Conversion Start Control

CLK_DIV[3:0]	OSC_SEL = 0		OSC_SEL = 1	
	SAMPLING FREQUENCY, f_{CYCLE_OSR} (kSPS)	CYCLE TIME, t_{CYCLE_OSR} (µs)	SAMPLING FREQUENCY, f_{CYCLE_OSR} (kSPS)	CYCLE TIME, t_{CYCLE_OSR} (µs)
0000b	1000	1	31.25	32
0001b	666.7	1.5	20.83	48
0010b	500	2	15.63	64
0011b	333.3	3	10.42	96
0100b	250	4	7.81	128
0101b	166.7	6	5.21	192
0110b	125	8	3.91	256
0111b	83	12	2.60	384
1000b	62.5	16	1.95	512
1001b	41.7	24	1.3	768
1010b	31.3	32	0.98	1024
1011b	20.8	48	0.65	1536
1100b	15.6	64	0.49	2048
1101b	10.4	96	0.33	3072
1110b	7.8	128	0.24	4096
1111b	5.2	192	0.16	6144

As shown in 表 8-3, the comparison time in *Turbo Comparator Mode* can be controlled by the OSC_SEL and CLK_DIV register fields.

表 8-3. Configuring Comparison Rate for Turbo Comparator Mode

CLK_DIV[3:0]	OSC_SEL = 0		OSC_SEL = 1	
	COMPARISON RATE, $f_{COMPARISON}$ (kSPS)	CYCLE TIME, t_{CYCLE_COMP} (µs)	COMPARISON RATE, $f_{COMPARISON}$ (kSPS)	CYCLE TIME, t_{CYCLE_COMP} (µs)
0000b	3200	0.3125	100	10
0001b	2133.3	0.46875	66.7	15
0010b	1600	0.625	50	20
0011b	1066.7	0.9375	33.3	30
0100b	800	1.25	25	40
0101b	533.3	1.875	16.67	60
0110b	400	2.5	3.91	80
0111b	266.7	3.75	2.60	120
1000b	200	5	1.95	160
1001b	133.3	7.5	1.3	240
1010b	100	10	0.98	320
1011b	66.7	15	0.65	480
1100b	50	20	0.49	640
1101b	33.3	30	0.33	960
1110b	25	40	0.24	1280
1111b	16.67	60	0.16	1920

8.3.6 General-Purpose I/Os

The eight channels of the ADS7038-Q1 can be independently configured as analog inputs, digital inputs, or digital outputs. The device channels, as described in 表 8-4, can be configured as analog inputs or GPIOs using the PIN_CFG and GPIO_CFG registers.

表 8-4. Configuring Channels as Analog Inputs or GPIOs

PIN_CFG[7:0]	GPIO_CFG[7:0]	GPO_DRIVE_CFG[7:0]	CHANNEL CONFIGURATION
0	x	x	Analog input (default)
1	0	x	Digital input
1	1	0	Digital output; open-drain driver
1	1	1	Digital output; push-pull driver

Digital outputs can be configured to logic 1 or 0 by writing to the GPO_VALUE register. Digital outputs can also be updated in response to event flags set by the digital window comparator (see the *Triggering Digital Outputs With Digital Window Comparator* section for more details). Reading the GPI_VALUE register returns the logic level for all channels configured as analog inputs, digital inputs, and digital outputs.

8.3.7 Programmable Averaging Filter

The ADS7038-Q1 features a built-in oversampling (OSR) module that can be used to average several samples. The averaging filter can be enabled by programming the OSR[2:0] bits in the OSR_CFG register. The averaging filter configuration is common to all analog input channels. As shown in 図 8-3, the averaging filter module output is 16 bits long. Only the first conversion for the selected analog input channel must be initiated by the host. Any remaining conversions for the selected averaging factor are generated internally. The time (t_{AVG}) required to complete the averaging operation is determined by the sampling speed and number of samples to be averaged; see the *Oscillator and Timing Control* section for more details. The 16-bit result can be read out after the averaging operation completes. For more information about programmable averaging filters and performance results see the *Resolution-Boosting ADS7138 Using Programmable Averaging Filter* application report.

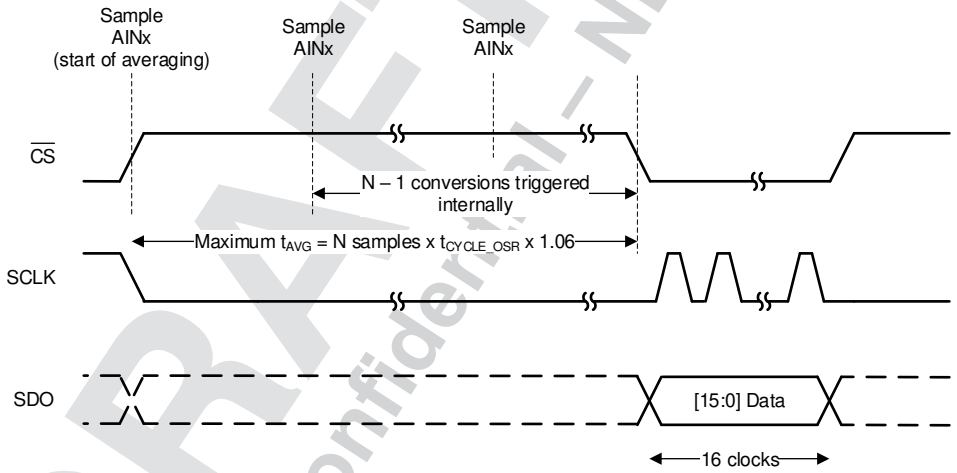


図 8-3. Averaged Output Data

In autonomous mode of operation, samples from analog input channels that are enabled in the AUTO_SEQ_CH_SEL register are averaged sequentially; see the *Autonomous Mode* section. The digital window comparator compares the top 12 bits of the 16-bit average result with the thresholds.

式 2 provides the LSB value of the 16-bit average result.

$$1\ LSB = \frac{AVDD}{2^{16}} \quad (2)$$

8.3.8 CRC on Data Interface

The cyclic redundancy check (CRC) is an error checking code that detects errors in communication between the device and the host. The CRC module is optional and can be enabled by the CRC_EN bit in the GENERAL_CFG register.

The CRC data byte is the 8-bit remainder of the bitwise exclusive-OR (XOR) operation of the argument by a CRC polynomial. The CRC polynomial is based on the CRC-8-CCITT: $X^8 + X^2 + X + 1$. The nine binary polynomial coefficients are 100000111. The CRC calculation is preset with 0 data values.

8.3.8.1 Input CRC (From Host To Device)

The host must compute and append the appropriate 8-bit CRC to the command string in the same SPI frame (see *Register Read With CRC*). The ADC also computes the expected 8-bit CRC corresponding to the 24-bit payload received from the host and compares the calculated CRC code to the CRC received from the host. If a communication error is detected, the CRCERR_IN bit in the SYSTEM_STATUS register is set to 1b. The CRCERR_IN bit is set in the following scenarios:

- The SPI communication frame did not have 32 clocks exactly, corresponding to a 24-bit data payload and an 8-bit CRC.
- The CRC calculated by the ADC over the received 24-bit payload does not match with the corresponding 8-bit CRC received from the host.

If a CRC error is detected by the device, the command does not execute and the CRCERR_IN flag is set to 1b. ADC conversion data read and register read, with a valid CRC from the host, are still supported. The error condition can be detected, as listed in 表 8-5, by either status flags or by a register read. Further register writes to the device are blocked until CRCERR_IN flag is cleared to 0b. Register write operation, with valid CRC from the host, to the SYSTEM_STATUS and GENERAL_CFG registers is still supported.

The device can be configured to set all channels to analog inputs on detecting a CRC error by setting CH_RST bit to 1b. This would ensure that channels which were configured as digital outputs are not driven by the device when CRC error is detected. All channels will be reset as per the configuration in the PIN_CFG and GPIO_CFG registers when CRCERR_IN flag is cleared.

The device can be configured to abort further conversions in autonomous and turbo comparator modes (see the *Autonomous Mode* and *Turbo Comparator Mode* sections), on detecting a CRC error, by setting CONV_ON_ERR = 1b.

表 8-5. Configuring Notifications when CRC Error is Detected

CRC ERROR NOTIFICATION	CONFIGURATION	DESCRIPTION
ALERT	ALERT_CRCIN = 1b	ALERT (internal signal) is asserted if a CRC error is detected.
Status flags	APPEND_STATUS = 10b	See *Status Flags* for details.
Register read	—	Read the CRCERR_IN bit to check if a CRC error was detected.

8.3.8.2 Output CRC (From Device to Host)

The device appends an 8-bit CRC to the output data packet when the CRC module is enabled. The output data packet length can be one of the following:

- An 8-bit for register reads (see the *Register Read With CRC* section for more details).
- A 16-bit or 24-bit for ADC conversion result reads (see 表 8-6 for more details).

The SPI frame must be exactly 32 bits long when the CRC module is enabled.

8.3.9 Output Data Format

図 8-4 depicts various SPI frames for reading data from the device. The data output is MSB aligned. If averaging is enabled the output data from the ADC are 16 bits long, otherwise the output data are 12 bits long. Optionally, a 4-bit channel ID or status flags can be appended at the end of the output data by configuring the APPEND_STATUS field.

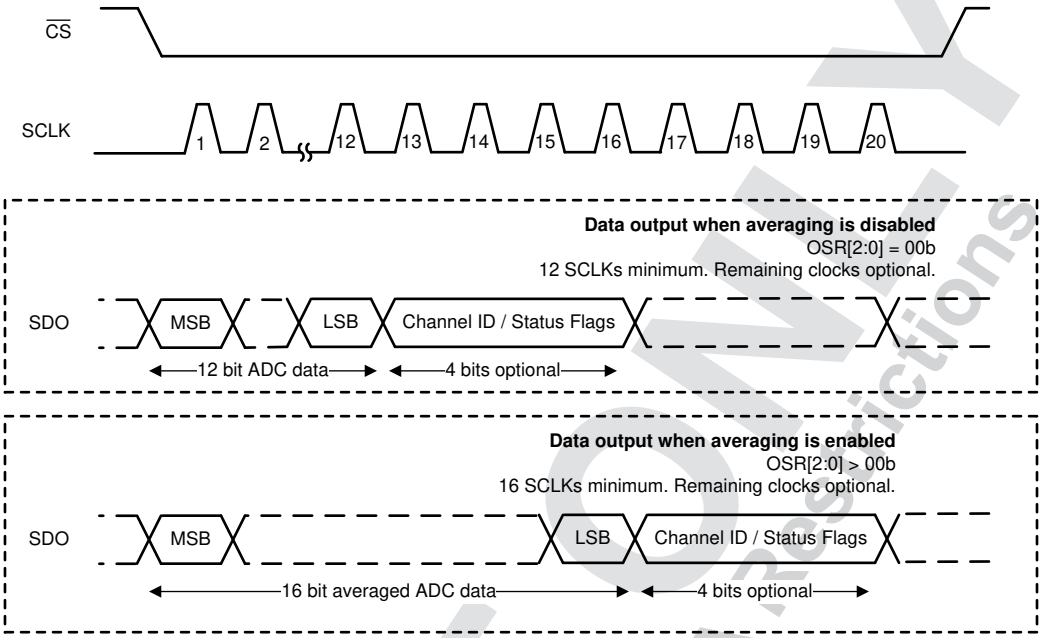


図 8-4. SPI Frames for Reading Data

表 8-6. Output Data Frames

CRC_EN	OSR[2:0]	APPEND_STATUS[1:0]	OUTPUT DATA FRAME
CRC module disabled (CRC_EN = 0)	No averaging	No flags (00b or 11b)	{Conversion result [11:0]}
		Channel ID (01b)	{Conversion result [11:0], CHID[3:0]}
		Status flags (10b)	{Conversion result [11:0], status flags[3:0]}
	Averaging enabled	No flags (00b or 11b)	{Conversion result [15:0]}
		Channel ID (01b)	{Conversion result [15:0], CHID[3:0]}
		Status flags (10b)	{Conversion result [15:0], status flags[3:0]}
CRC module enabled(1) (CRC_EN = 1)	No averaging	No flags (00b or 11b)	{Conversion result [11:0], 4'b0, CRC[7:0], 8'b0}
		Channel ID (01b)	{Conversion result [11:0], CHID[3:0], CRC[7:0], 8'b0}
		Status flags (10b)	{Conversion result [11:0], status flags[3:0], CRC[7:0], 8'b0}
	Averaging enabled	No flags (00b or 11b)	{Conversion result [15:0], CRC[7:0], 8'b0}
		Channel ID (01b)	{Conversion result [15:0], CHID[3:0], 4'b0, CRC[7:0]}
		Status flags (10b)	{Conversion result [15:0], status flags[3:0], 4'b0, CRC[7:0]}

(1) The SPI frame must be 32 bits long when the CRC module is enabled; see the *CRC on Data Interface* section for more details.

8.3.9.1 Status Flags

Status flags can be appended to the ADC output by setting APPEND_STATUS = 10b. Status flags are not appended to data corresponding to a register read operation or when FIX_PAT = 1b. The 4-bit status flag field is constructed as follows:

Status flag[3:0] = { 1, 0, CRCERR_IN, ALERT }

- CRCERR_IN: This flag is the same as the CRCERR_IN bit in the SYSTEM_STATUS register.
- ALERT: This flag indicates if any of the event flags are set in the EVENT_FLAG register.

8.3.10 Digital Window Comparator

The digital window comparator (DWC) compares the conversion result for an analog input channel with programmable high and low thresholds with hysteresis. As shown in 図 8-5, the DWC sets the EVENT_HIGH_FLAG and EVENT_LOW_FLAG registers based on the comparison result. The logical OR of the EVENT_HIGH_FLAG and EVENT_LOW_FLAG registers is available in the EVENT_FLAG register. An internal ALERT signal is generated when a bit in the EVENT_FLAG register is high and the corresponding bit in the ALERT_CH_SEL register is enabled. The internal ALERT signal can be output on any one of the digital output channels by configuring the ALERT_PIN register.

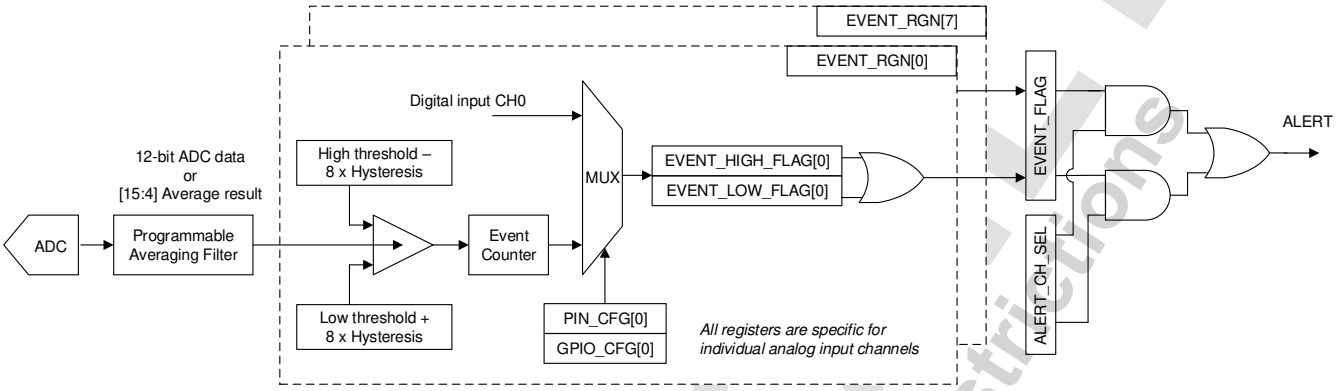


図 8-5. Digital Window Comparator Block Diagram

The low-side threshold, high-side threshold, event counter, and hysteresis parameters are independently programmable for each input channel. 図 8-6 illustrates that the window comparator can monitor events for every analog input channel.

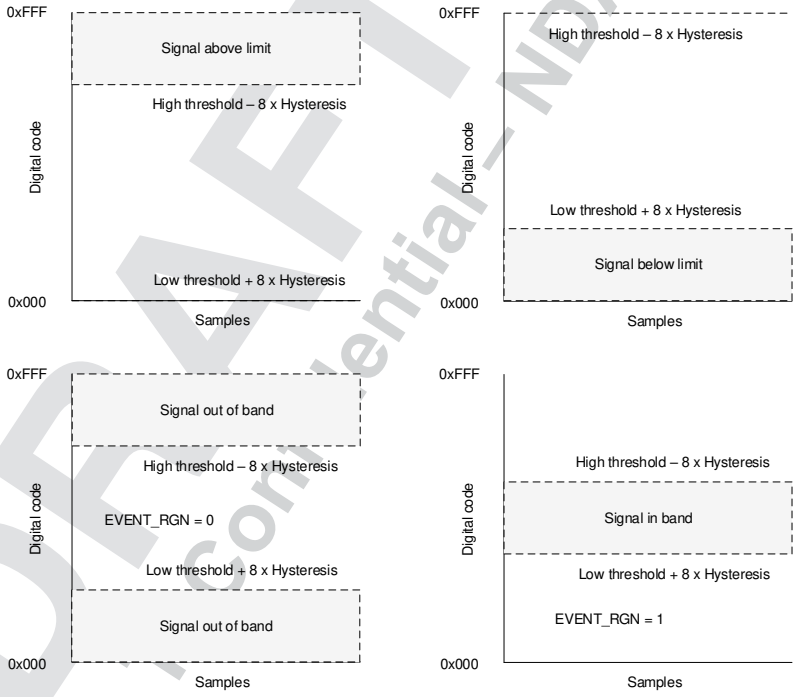


図 8-6. Event Monitoring With the Window Comparator

To enable the digital window comparator, set the DWC_EN bit in the GENERAL_CFG register. By default, hysteresis = 0, high threshold = 0xFFF, and low threshold = 0x000. Configure the EVENT_RGN register to detect when a signal is within a band defined by high and low thresholds. In each of the cases shown in 図 8-6, either or both the EVENT_HIGH_FLAG and EVENT_LOW_FLAG can be set.

The device features a programmable event counter that counts consecutive threshold violations before either EVENT_HIGH_FLAG or EVENT_LOW_FLAG are set. An example is shown in 図 8-7 where the EVENT_HIGH_FLAG is not set until eight consecutive conversion results of the corresponding analog input channel exceed the threshold configuration. The event count can be set to a higher value to avoid transients in the input signal from setting the event flags.

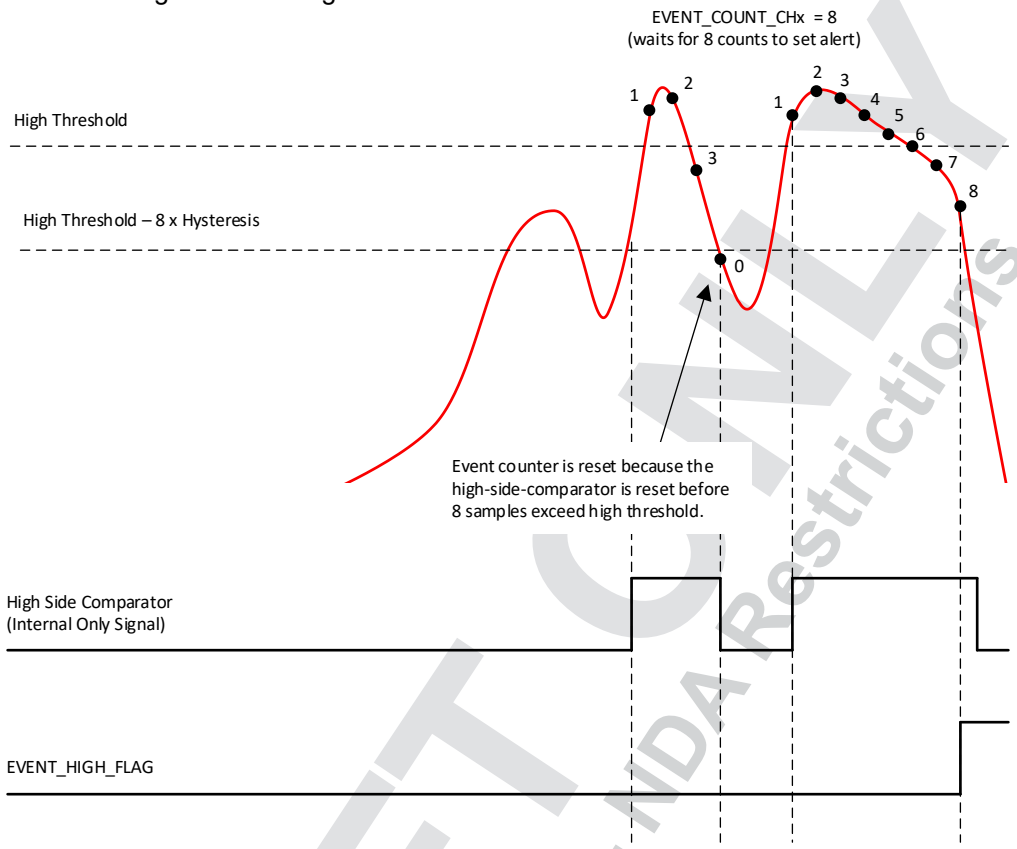


図 8-7. False Trigger Avoidance Using the Event Counter

To assert the ALERT signal, when either or both the EVENT_HIGH_FLAG and EVENT_LOW_FLAG are set for a particular analog input channel, set the corresponding bit in the ALERT_CH_SEL register.

8.3.10.1 Interrupts From Digital Inputs

Rising edge or falling edge events can be detected on channels configured as digital inputs. As described in 表 8-7, configure the EVENT_RGN register to select either a rising edge or falling edge event.

表 8-7. Configuring Interrupts from Digital Inputs

PIN_CFG[7:0]	GPIO_CFG[7:0]	EVENT_RGN[7:0]	EVENT DESCRIPTION
1	0	0	A rising edge on the digital input sets the corresponding flag in the EVENT_HIGH_FLAG register.
1	0	1	A falling edge on the digital input sets the corresponding flag in the EVENT_LOW_FLAG register.

8.3.10.2 Triggering Digital Outputs With Digital Window Comparator

As shown in 図 8-8, the output value of channels configured as digital outputs can be updated in response to one or more flags being set in the EVENT_FLAG register.

The following procedure enables updating the output value of a digital output in response to event flags:

1. Configure the device channels as either analog inputs (default), digital inputs, or digital outputs.
2. Configure the digital outputs as either open-drain (default) or push-pull outputs.
3. Configure the digital window comparator for the input channels. The digital window comparator updates the flags in the EVENT_FLAG register corresponding to individual channels. See the *Digital Window Comparator* section for more details.
4. Select the bits corresponding to the input channels that are to be enabled for triggering the digital output in the GPOx_EVENT_SEL register (where x is the digital output channel number).
5. The default output value of the digital output, when no event flag is set, is configured in the GPO_VALUE register. The output value of the digital output, when event flags are set, is configured in the GPO_VALUE_ON_EVENT register.
6. Configure the GPO_UPDATE_ON_EVENT register to enable the logic to update the selected digital output in response to event flags.

The configuration in GPO_VALUE sets the output value of a dgital output when either no event flags are set or when event flags are reset in the EVENT_FLAG register corresponding to channels selected in the GPOx_EVENT_SEL register.

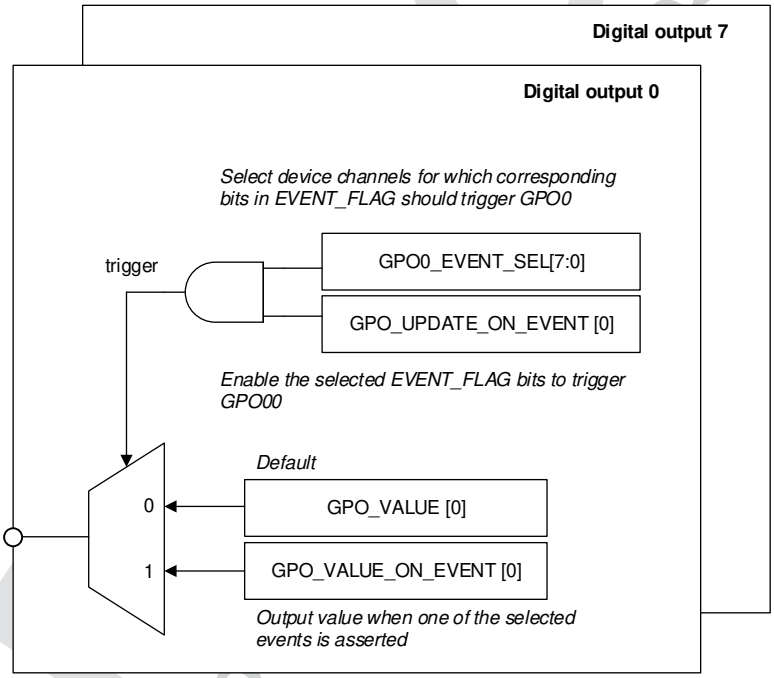


図 8-8. Block Diagram of the Digital Output Logic

8.3.11 Minimum, Maximum, and Latest Data Registers

The ADS7038-Q1 can record the minimum, maximum, and latest conversion result (statistics registers) for every analog input channel. To enable or re-enable recording statistics, set the STATS_EN bit in the GENERAL_CFG register. Writing 1b to the STATS_EN bit reinitializes the statistics module. Previous values can be read from the statistics registers until a new conversion result is available. Set STATS_EN = 0b to prevent any updates to this block of registers before reading the statistics registers.

8.3.12 Device Programming

8.3.12.1 Enhanced-SPI Interface

The device features an enhanced-SPI interface that allows the host controller to operate at slower SCLK speeds and still achieve full throughput. As described in 表 8-8, the host controller can use any of the four SPI-compatible protocols (SPI-00, SPI-01, SPI-10, or SPI-11) to access the device.

表 8-8. SPI Protocols for Configuring the Device

PROTOCOL	SCLK POLARITY (At the $\overline{CS}$ Falling Edge)	SCLK PHASE (Capture Edge)	CPOL_CPHA[1:0]	DIAGRAM
SPI-00	Low	Rising	00b	図 8-9
SPI-01	Low	Falling	01b	図 8-10
SPI-10	High	Falling	10b	図 8-9
SPI-11	High	Rising	11b	図 8-10

On power-up or after coming out of any asynchronous reset, the device supports the SPI-00 protocol for data read and data write operations. To select a different SPI-compatible protocol, program the CPOL_CPHA[1:0] field. This first write operation must adhere to the SPI-00 protocol. Any subsequent data transfer frames must adhere to the newly-selected protocol.

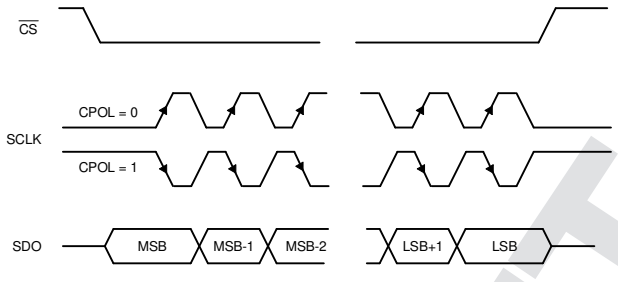


図 8-9. Standard SPI Timing Protocol (CPHA = 0)

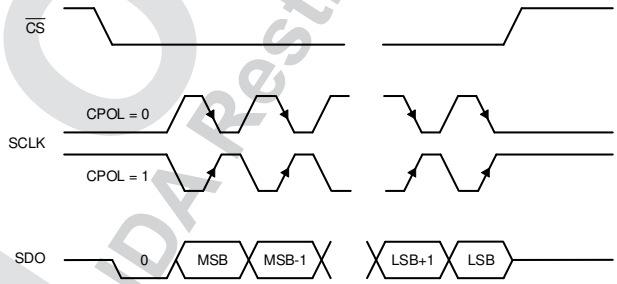


図 8-10. Standard SPI Timing Protocol (CPHA = 1)

8.3.12.2 Register Read/Write Operation

The device supports the commands listed in 表 8-9 to access the internal configuration registers.

表 8-9. Opcodes for Commands

OPCODE	COMMAND DESCRIPTION
0000 0000b	No operation
0001 0000b	Single register read
0000 1000b	Single register write
0001 1000b	Set bit
0010 0000b	Clear bit

8.3.12.2.1 Register Write

A 24-bit SPI frame is required for writing data to configuration registers. The 24-bit data on SDI, as shown in 図 8-11, consists of an 8-bit write command (0000 1000b), an 8-bit register address, and 8-bit data. The write command is decoded on the $\overline{CS}$ rising edge and the specified register is updated with the 8-bit data specified during the register write operation.

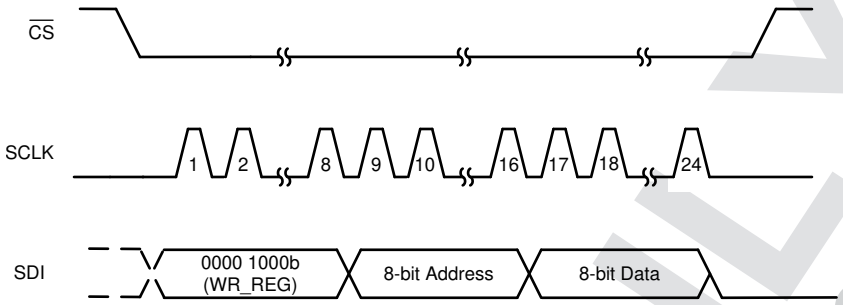


図 8-11. Register Write Operation

8.3.12.2.2 Register Read

Register read operation consists of two SPI frames: the first SPI frame initiates a register read and the second SPI frame reads data from the register address provided in the first frame. As shown in 図 8-12, the 8-bit register address and the 8-bit dummy data are sent over the SDI pin during the first 24-bit frame with the read command (0001 0000b). On the rising edge of $\overline{CS}$, the read command is decoded and the requested register data are available for reading during the next frame. During the second frame, the first eight bits on SDO correspond to the requested register read. During the second frame, SDI can be used to initiate another operation or can be set to 0.

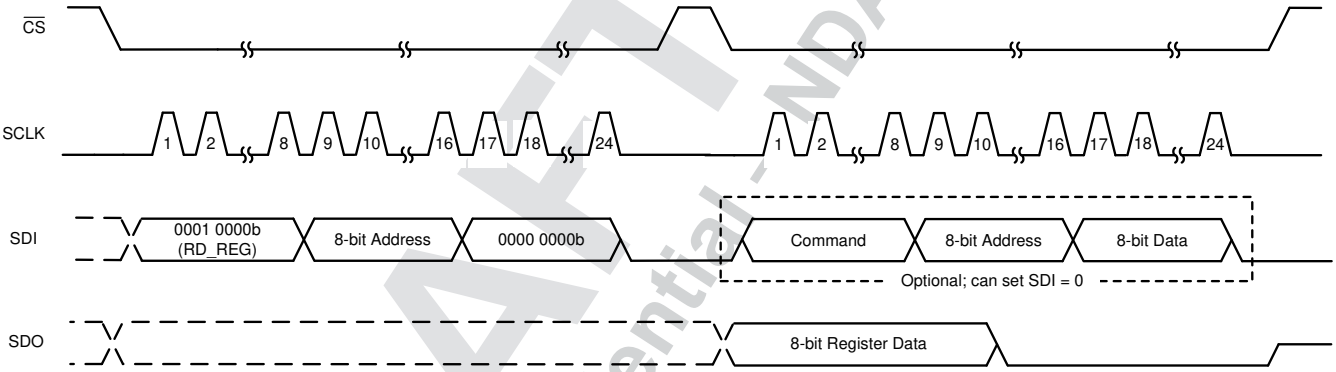


図 8-12. Register Read Operation

8.3.12.2.2.1 Register Read With CRC

A register read consists of two SPI frames, as described in the *Register Read* section. As shown in 図 8-13, the device appends an 8-bit output CRC byte along with 8-bit register data when the CRC module is enabled during a register read. The output CRC is computed by the device on 8-bit register data.

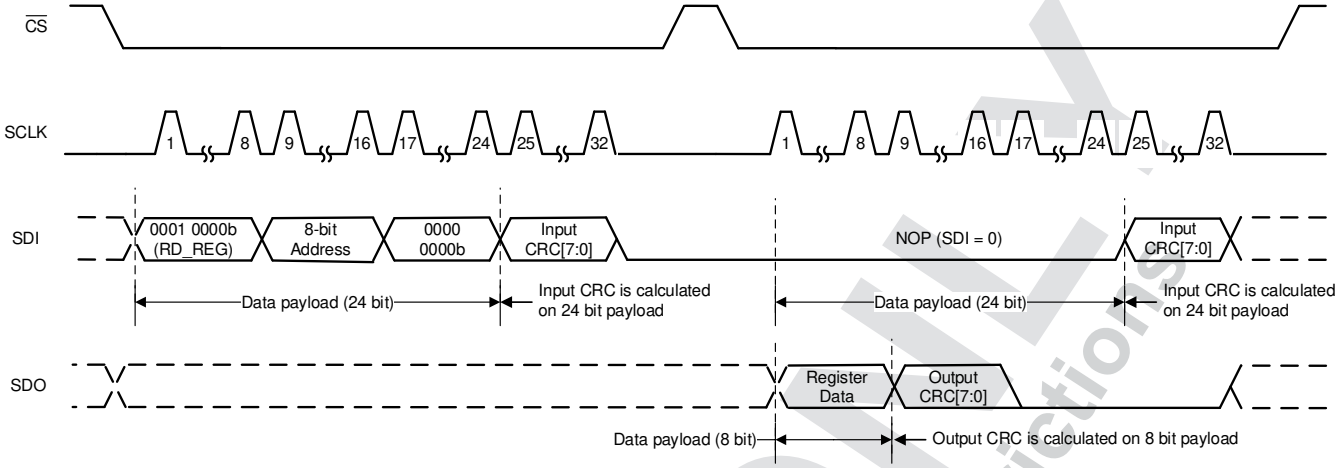


図 8-13. Register Read With CRC

8.4 Device Functional Modes

表 8-10 lists the functional modes supported by the ADS7038-Q1. The device powers up in manual mode and can be configured into either of these modes by writing the configuration registers for the desired mode.

表 8-10. Functional Modes

FUNCTIONAL MODE	CONVERSION CONTROL	MUX CONTROL	CONV_MODE[1:0]	SEQ_MODE[1:0]
Manual	$\overline{CS}$ rising edge	Register write to MANUAL_CHID	00b	00b
On-the-fly	$\overline{CS}$ rising edge	First 5 bits after the $\overline{CS}$ falling edge	00b	10b
Auto-sequence	$\overline{CS}$ rising edge	Channel sequencer	00b	01b
Autonomous	Internal to the device	Channel sequencer	01b	01b
Turbo comparator	Internal to the device	Channel sequencer	10b	01b

8.4.1 Device Power-Up and Reset

On power-up, the BOR bit is set indicating a power-cycle or reset event. The device can be reset by setting the RST bit or by recycling power on the AVDD pin.

8.4.2 Manual Mode

Manual mode allows the external host processor to directly select the analog input channel. 図 8-14 shows the steps for operating the device in manual mode.

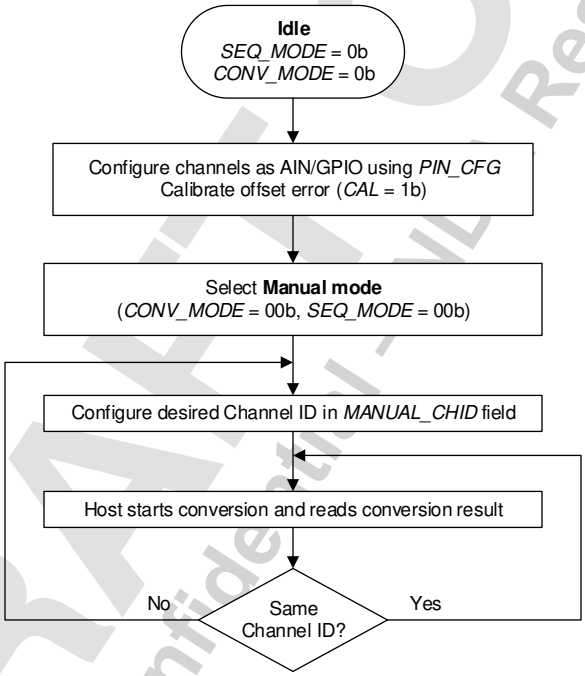


図 8-14. Device Operation in Manual Mode

In manual mode, the command to switch to a new channel (indicated by cycle N in 図 8-15) is decoded by the device on the $\overline{CS}$ rising edge. The $\overline{CS}$ rising edge is also the start of the conversion signal, and therefore the device samples the previously selected MUX channel in cycle N+1. The newly selected analog input channel data are available in cycle N+2. For switching the analog input channel, a register write to the MANUAL_CHID field requires 24 clocks; see the *Register Write* section for more details. After a channel is selected, the number of clocks required for reading the output data depends on the device output data frame size; see the *Output Data Format* section for more details.

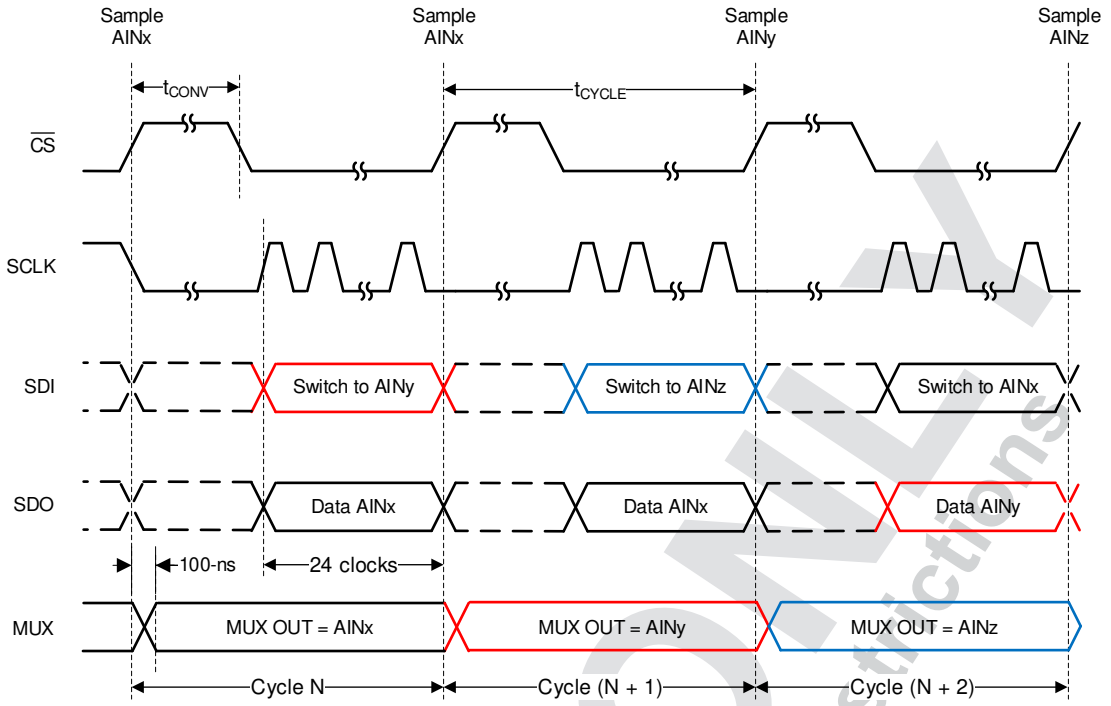


図 8-15. Starting Conversions and Reading Data in Manual Mode

8.4.3 On-the-Fly Mode

In the on-the-fly mode of operation, the analog input channel is selected, as shown in 図 8-16, using the first five bits on SDI without waiting for the $\overline{CS}$ rising edge. Thus, the ADC samples the newly selected channel on the $\overline{CS}$ rising edge and there is no latency between the channel selection and the ADC output data.

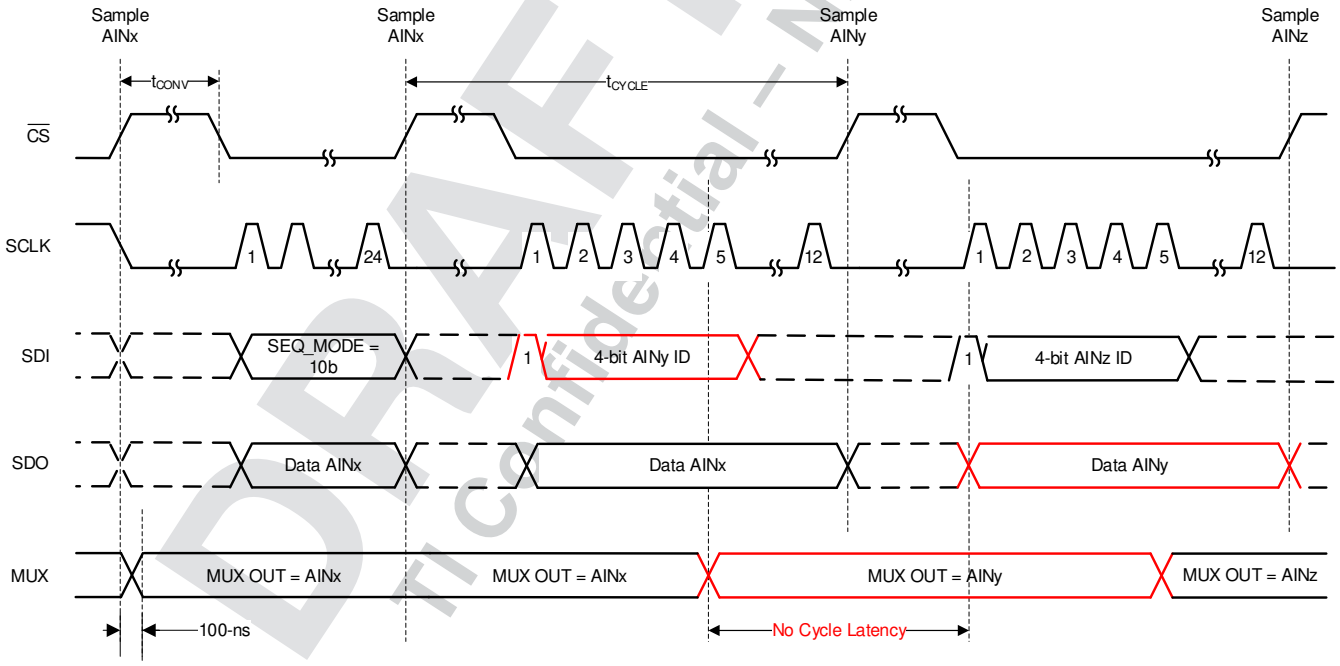


図 8-16. Starting Conversions and Reading Data in On-the-Fly Mode

The number of clocks required for reading the output data depends on the device output data frame size; see the *Output Data Format* section for more details.

8.4.4 Auto-Sequence Mode

In auto-sequence mode, the internal channel sequencer switches the multiplexer to the next analog input channel after every conversion. The desired analog input channels can be configured for sequencing in the AUTO_SEQ_CH_SEL register. To enable the channel sequencer, set SEQ_START = 1b. After every conversion, the channel sequencer switches the multiplexer to the next analog input in ascending order. To stop the channel sequencer from selecting channels, set SEQ_START = 0b.

In the example shown in 図 8-17, AIN2 and AIN6 are enabled for sequencing in AUTO_SEQ_CH_SEL. The channel sequencer loops through AIN2 and AIN6 and repeats until SEQ_START is set to 0b. The number of clocks required for reading the output data depends on the device output data frame size; see the *Output Data Format* section for more details.

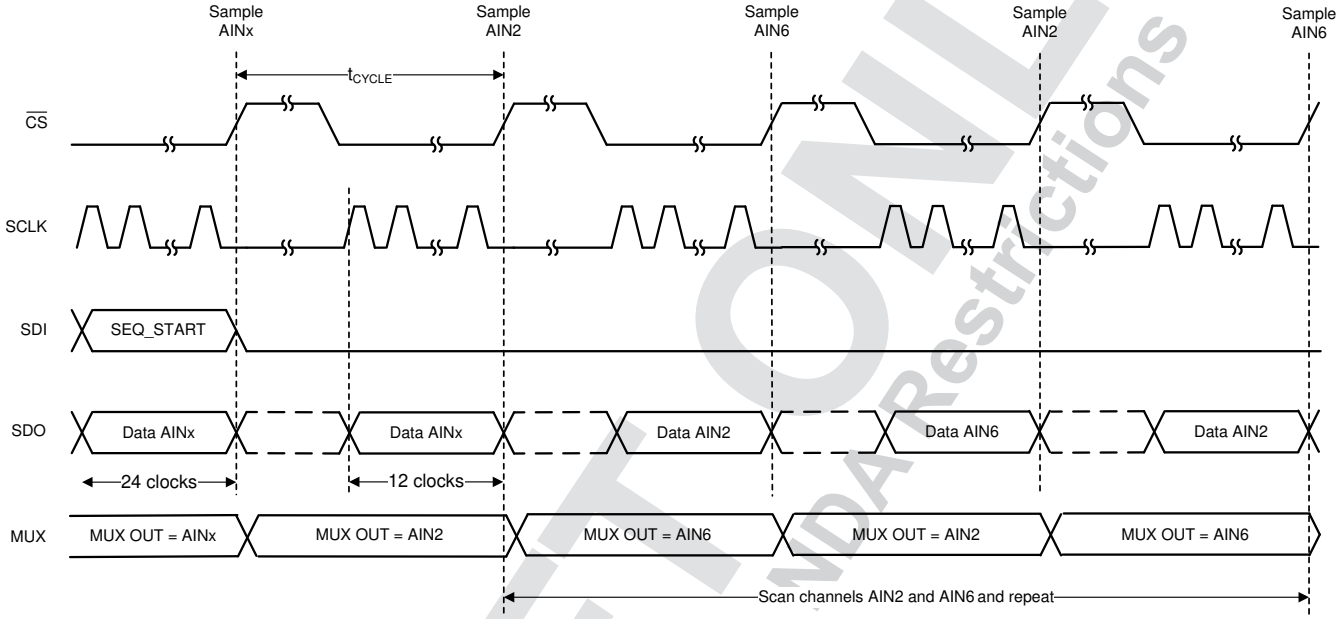


図 8-17. Starting Conversions and Reading Data in Auto-Sequence Mode

8.4.5 Autonomous Mode

In autonomous mode, the device can be programmed to monitor the voltage applied on the analog input pins of the device and generate an ALERT signal internal to the device when the programmable high or low thresholds are crossed (see the *Digital Window Comparator* section for more details).

In autonomous mode, the device generates the start of conversion using the internal oscillator. The first start of conversion must be provided by the host and the device generates the subsequent start of conversions. The device does not output conversion data when autonomous mode is enabled. Conversion results can be accessed using the register read operation described in the *Minimum, Maximum, and Latest Data Registers* section by configuring STATS_EN = 1b in the GENERAL_CFG register.

図 8-18 shows the steps for configuring the functional mode to autonomous mode. Abort the ongoing sequence by setting SEQ_START to 0b before changing the functional mode or device configuration.

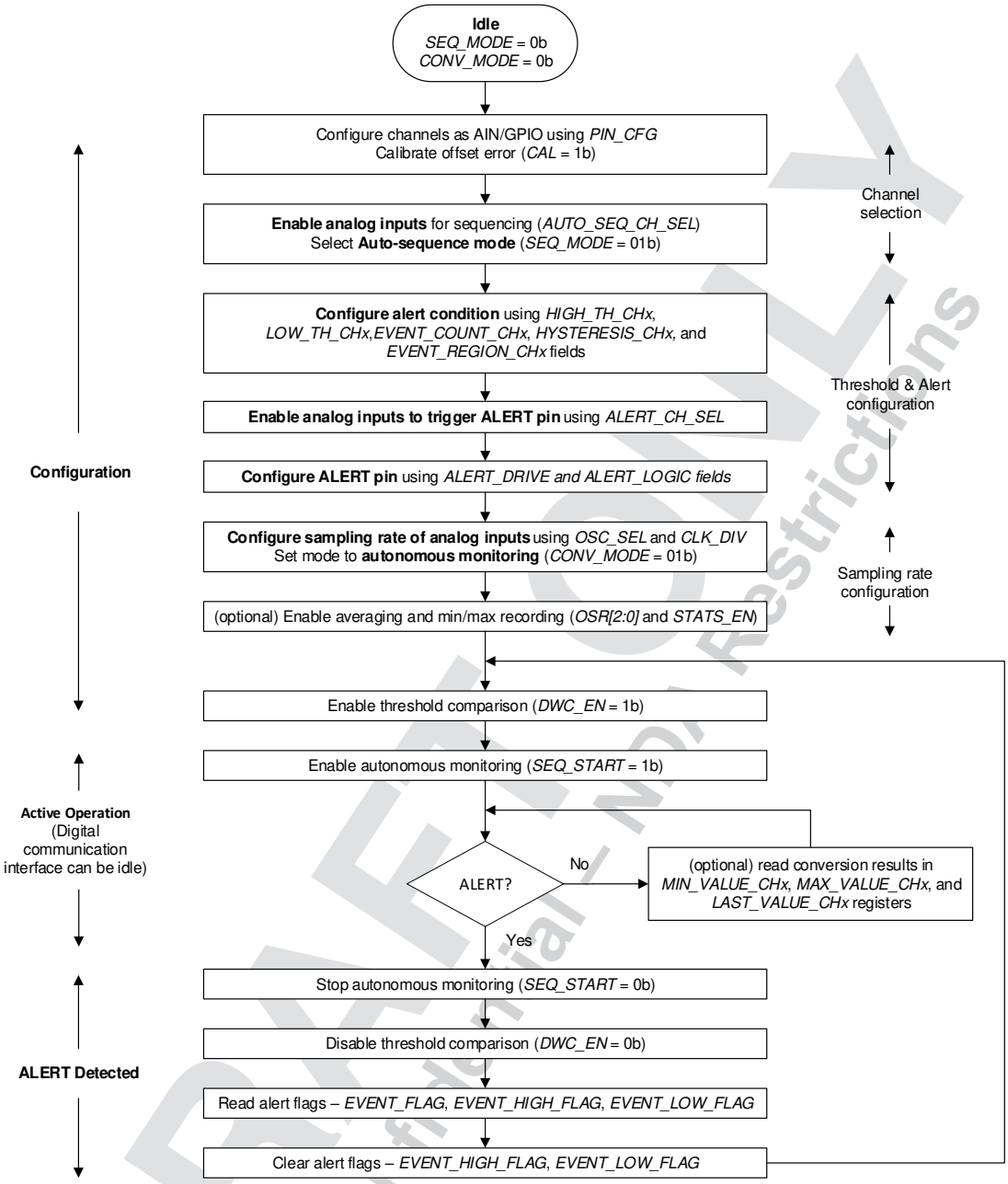


図 8-18. Configuring the Device in Autonomous Mode

8.4.6 Turbo Comparator Mode

Turbo comparator mode allows fast comparison with high/low thresholds using the digital window comparator. ADC output data is not available in this mode.

図 8-19 lists the comparison start and read frames for turbo comparator mode. The desired analog input channels can be configured for sequencing in the AUTO_SEQ_CH_SEL register. To enable the channel sequencer, set SEQ_START to 1b. After every comparison, the channel sequencer switches the multiplexer to the next analog input in ascending order. To stop the channel sequencer from selecting channels, set SEQ_START to 0b. See sction on *Oscillator and Timing Control* for more details on configuring speed in turbo comparator mode.

Abort the ongoing sequence by setting SEQ_START to 0b before changing the functional mode or device configuration.

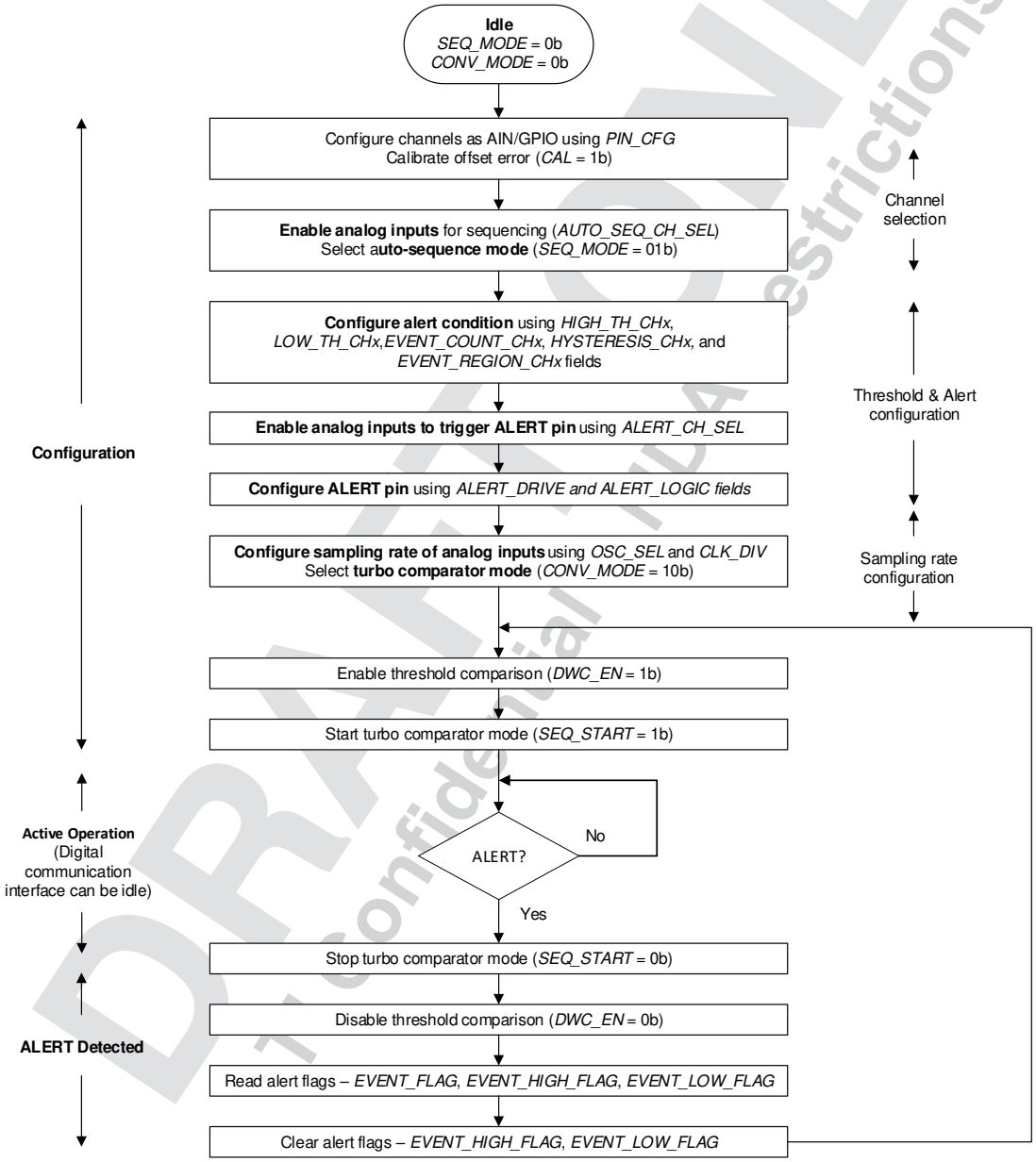


図 8-19. Device Operation in Turbo Comparator Mode

8.5 ADS7038-Q1 Registers

表 8-11 lists the memory-mapped registers for the ADS7038-Q1 registers. All register offset addresses not listed in 表 8-11 should be considered as reserved locations and the register contents should not be modified.

表 8-11. ADS7038-Q1 Registers

Address	Acronym	Register Name	Section
0x0	SYSTEM_STATUS		セクション 8.5.1
0x1	GENERAL_CFG		セクション 8.5.2
0x2	DATA_CFG		セクション 8.5.3
0x3	OSR_CFG		セクション 8.5.4
0x4	OPMODE_CFG		セクション 8.5.5
0x5	PIN_CFG		セクション 8.5.6
0x7	GPIO_CFG		セクション 8.5.7
0x9	GPO_DRIVE_CFG		セクション 8.5.8
0xB	GPO_VALUE		セクション 8.5.9
0xD	GPI_VALUE		セクション 8.5.10
0x10	SEQUENCE_CFG		セクション 8.5.11
0x11	MANUAL_CH_SEL		セクション 8.5.12
0x12	AUTO_SEQ_CH_SEL		セクション 8.5.13
0x14	ALERT_CH_SEL		セクション 8.5.14
0x16	ALERT_FUNC_SEL		セクション 8.5.15
0x17	ALERT_PIN_CFG		セクション 8.5.16
0x18	EVENT_FLAG		セクション 8.5.17
0x1A	EVENT_HIGH_FLAG		セクション 8.5.18
0x1C	EVENT_LOW_FLAG		セクション 8.5.19
0x1E	EVENT_RGN		セクション 8.5.20
0x20	HYSTERESIS_CH0		セクション 8.5.21
0x21	HIGH_TH_CH0		セクション 8.5.22
0x22	EVENT_COUNT_CH0		セクション 8.5.23
0x23	LOW_TH_CH0		セクション 8.5.24
0x24	HYSTERESIS_CH1		セクション 8.5.25
0x25	HIGH_TH_CH1		セクション 8.5.26
0x26	EVENT_COUNT_CH1		セクション 8.5.27
0x27	LOW_TH_CH1		セクション 8.5.28
0x28	HYSTERESIS_CH2		セクション 8.5.29
0x29	HIGH_TH_CH2		セクション 8.5.30
0x2A	EVENT_COUNT_CH2		セクション 8.5.31
0x2B	LOW_TH_CH2		セクション 8.5.32
0x2C	HYSTERESIS_CH3		セクション 8.5.33
0x2D	HIGH_TH_CH3		セクション 8.5.34
0x2E	EVENT_COUNT_CH3		セクション 8.5.35
0x2F	LOW_TH_CH3		セクション 8.5.36
0x30	HYSTERESIS_CH4		セクション 8.5.37
0x31	HIGH_TH_CH4		セクション 8.5.38
0x32	EVENT_COUNT_CH4		セクション 8.5.39
0x33	LOW_TH_CH4		セクション 8.5.40
0x34	HYSTERESIS_CH5		セクション 8.5.41
0x35	HIGH_TH_CH5		セクション 8.5.42

表 8-11. ADS7038-Q1 Registers (continued)

Address	Acronym	Register Name	Section
0x36	EVENT_COUNT_CH5		セクション 8.5.43
0x37	LOW_TH_CH5		セクション 8.5.44
0x38	HYSTERESIS_CH6		セクション 8.5.45
0x39	HIGH_TH_CH6		セクション 8.5.46
0x3A	EVENT_COUNT_CH6		セクション 8.5.47
0x3B	LOW_TH_CH6		セクション 8.5.48
0x3C	HYSTERESIS_CH7		セクション 8.5.49
0x3D	HIGH_TH_CH7		セクション 8.5.50
0x3E	EVENT_COUNT_CH7		セクション 8.5.51
0x3F	LOW_TH_CH7		セクション 8.5.52
0x60	MAX_CH0_LSB		セクション 8.5.53
0x61	MAX_CH0_MSB		セクション 8.5.54
0x62	MAX_CH1_LSB		セクション 8.5.55
0x63	MAX_CH1_MSB		セクション 8.5.56
0x64	MAX_CH2_LSB		セクション 8.5.57
0x65	MAX_CH2_MSB		セクション 8.5.58
0x66	MAX_CH3_LSB		セクション 8.5.59
0x67	MAX_CH3_MSB		セクション 8.5.60
0x68	MAX_CH4_LSB		セクション 8.5.61
0x69	MAX_CH4_MSB		セクション 8.5.62
0x6A	MAX_CH5_LSB		セクション 8.5.63
0x6B	MAX_CH5_MSB		セクション 8.5.64
0x6C	MAX_CH6_LSB		セクション 8.5.65
0x6D	MAX_CH6_MSB		セクション 8.5.66
0x6E	MAX_CH7_LSB		セクション 8.5.67
0x6F	MAX_CH7_MSB		セクション 8.5.68
0x80	MIN_CH0_LSB		セクション 8.5.69
0x81	MIN_CH0_MSB		セクション 8.5.70
0x82	MIN_CH1_LSB		セクション 8.5.71
0x83	MIN_CH1_MSB		セクション 8.5.72
0x84	MIN_CH2_LSB		セクション 8.5.73
0x85	MIN_CH2_MSB		セクション 8.5.74
0x86	MIN_CH3_LSB		セクション 8.5.75
0x87	MIN_CH3_MSB		セクション 8.5.76
0x88	MIN_CH4_LSB		セクション 8.5.77
0x89	MIN_CH4_MSB		セクション 8.5.78
0x8A	MIN_CH5_LSB		セクション 8.5.79
0x8B	MIN_CH5_MSB		セクション 8.5.80
0x8C	MIN_CH6_LSB		セクション 8.5.81
0x8D	MIN_CH6_MSB		セクション 8.5.82
0x8E	MIN_CH7_LSB		セクション 8.5.83
0x8F	MIN_CH7_MSB		セクション 8.5.84
0xA0	RECENT_CH0_LSB		セクション 8.5.85
0xA1	RECENT_CH0_MSB		セクション 8.5.86
0xA2	RECENT_CH1_LSB		セクション 8.5.87

表 8-11. ADS7038-Q1 Registers (continued)

Address	Acronym	Register Name	Section
0xA3	RECENT_CH1_MSB		セクション 8.5.88
0xA4	RECENT_CH2_LSB		セクション 8.5.89
0xA5	RECENT_CH2_MSB		セクション 8.5.90
0xA6	RECENT_CH3_LSB		セクション 8.5.91
0xA7	RECENT_CH3_MSB		セクション 8.5.92
0xA8	RECENT_CH4_LSB		セクション 8.5.93
0xA9	RECENT_CH4_MSB		セクション 8.5.94
0xAA	RECENT_CH5_LSB		セクション 8.5.95
0xAB	RECENT_CH5_MSB		セクション 8.5.96
0xAC	RECENT_CH6_LSB		セクション 8.5.97
0xAD	RECENT_CH6_MSB		セクション 8.5.98
0xAE	RECENT_CH7_LSB		セクション 8.5.99
0xAF	RECENT_CH7_MSB		セクション 8.5.100
0xC3	GPO0_EVENT_CFG		セクション 8.5.101
0xC5	GPO1_EVENT_CFG		セクション 8.5.102
0xC7	GPO2_EVENT_CFG		セクション 8.5.103
0xC9	GPO3_EVENT_CFG		セクション 8.5.104
0xCB	GPO4_EVENT_CFG		セクション 8.5.105
0xCD	GPO5_EVENT_CFG		セクション 8.5.106
0xCF	GPO6_EVENT_CFG		セクション 8.5.107
0xD1	GPO7_EVENT_CFG		セクション 8.5.108
0xE9	GPO_UPDATE_ON_EVENT		セクション 8.5.109
0xEB	GPO_VALUE_ON_EVENT		セクション 8.5.110

Complex bit access types are encoded to fit into small table cells. 表 8-12 shows the codes that are used for access types in this section.

表 8-12. ADS7038-Q1 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value
Register Array Variables		
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.

表 8-12. ADS7038-Q1 Access Type Codes (continued)

Access Type	Code	Description
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

8.5.1 SYSTEM_STATUS Register (Address = 0x0) [Reset = 0x81]

SYSTEM_STATUS is shown in 図 8-18 and described in 表 8-13.

Return to the 表 8-11.

図 8-18. SYSTEM_STATUS Register

7	6	5	4	3	2	1	0
RSVD	SEQ_STATUS	RESERVED		OSR_DONE	CRCERR_FUSE	CRCERR_IN	BOR
R-1b	R-0b	R-0b		R/W-0b	R-0b	R/W-0b	R/W-1b

表 8-13. SYSTEM_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	1b	Reads return 1b.
6	SEQ_STATUS	R	0b	Status of the channel sequencer. 0b = Sequence stopped 1b = Sequence in progress
5-4	RESERVED	R	0b	Reserved Bit
3	OSR_DONE	R/W	0b	Averaging status. Clear this bit by writing 1b to this bit. 0b = Averaging in progress or not started; average result is not ready. 1b = Averaging complete; average result is ready.
2	CRCERR_FUSE	R	0b	Device power-up configuration CRC check status. To re-evaluate this bit, software reset the device or power cycle AVDD. 0b = No problems detected in power-up configuration. 1b = Device configuration not loaded correctly.
1	CRCERR_IN	R/W	0b	Status of CRC check on incoming data. Write 1b to clear this error flag. 0b = No CRC error. 1b = CRC error detected. All register writes, except to addresses 0x00 and 0x01, are blocked.
0	BOR	R/W	1b	Brown out reset indicator. This bit is set if brown out condition occurs or device is power cycled. Write 1b to this bit to clear the flag. 0b = No brown out condition detected from the last time this bit was cleared. 1b = Brown out condition detected or device power cycled.

8.5.2 GENERAL_CFG Register (Address = 0x1) [Reset = 0x0]

GENERAL_CFG is shown in 図 8-19 and described in 表 8-14.

Return to the 表 8-11.

図 8-19. GENERAL_CFG Register

7	6	5	4	3	2	1	0
RESERVED	CRC_EN	STATS_EN	DWC_EN	RESERVED	CH_RST	CAL	RST
R-0b	R/W-0b	R/W-0b	R/W-0b	R-0b	R/W-0b	R/W-0b	W-0b

表 8-14. GENERAL_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0b	Reserved Bit
6	CRC_EN	R/W	0b	Enable or disable the CRC on device interface. 0b = CRC module disabled. 1b = CRC appended to data output. CRC check is enabled on incoming data.
5	STATS_EN	R/W	0b	Enable or disable the statistics module. 0b = Minimum, maximum, and recent value registers are not updated. 1b = Clear minimum, maximum, and recent value registers and conitnue updating with new conversion results.
4	DWC_EN	R/W	0b	Enable or disable the digital window comparator. 0b = Reset or disable the digital window comparator. 1b = Enable digital window comparator.
3	RESERVED	R	0b	Reserved Bit
2	CH_RST	R/W	0b	Force all channels to be analog inputs. 0b = Normal operation. 1b = All channels will be set as analog inputs irrespective of configuration in other registers.
1	CAL	R/W	0b	Calibrate ADC offset. 0b = Normal operation. 1b = ADC offset is calibrated. After calibration is complete, this bit is set to 0b by the device.
0	RST	W	0b	Software reset all registers to default values. 0b = Normal operation. 1b = Device is reset. After reset is complete, this bit is set to 0b and BOR bit is set to 1b by the device.

8.5.3 DATA_CFG Register (Address = 0x2) [Reset = 0x0]

DATA_CFG is shown in 図 8-20 and described in 表 8-15.

Return to the 表 8-11.

図 8-20. DATA_CFG Register

7	6	5	4	3	2	1	0
FIX_PAT	RESERVED	APPEND_STATUS[1:0]		RESERVED		CPOL_CPHA[1:0]	
R/W-0b	R-0b	R/W-0b		R-0b		R/W-0b	

表 8-15. DATA_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FIX_PAT	R/W	0b	Device outputs fixed data bits which can be helpful for debugging communication with the device. 0b = Normal operation. 1b = Device outputs fixed code 0xA5A repeatitively when reading data from the device.
6	RESERVED	R	0b	Reserved Bit
5-4	APPEND_STATUS[1:0]	R/W	0b	Append 4-bit channel ID or status flags to output data. 00b: 01b: 10b: 11b: 0b = Channel ID and status flags are not appended to ADC data. 1b = 4-bit channel ID is appended to ADC data. 10b = 4-bit status flags are appended to ADC data. 11b = Reserved.
3-2	RESERVED	R	0b	Reserved Bit

表 8-15. DATA_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	CPOL_CPHA[1:0]	R/W	0b	This field sets the polarity and phase of SPI communication. 0b = CPOL = 0, CPHA = 0. 1b = CPOL = 0, CPHA = 1. 10b = CPOL = 1, CPHA = 0. 11b = CPOL = 1, CPHA = 1.

8.5.4 OSR_CFG Register (Address = 0x3) [Reset = 0x0]

OSR_CFG is shown in 図 8-21 and described in 表 8-16.

Return to the 表 8-11.

図 8-21. OSR_CFG Register

7	6	5	4	3	2	1	0
RESERVED					OSR[2:0]		
R-0b					R/W-0b		

表 8-16. OSR_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0b	Reserved Bit
2-0	OSR[2:0]	R/W	0b	Selects the oversampling ratio for ADC conversion result. 0b = No averaging 1b = 2 samples 10b = 4 samples 11b = 8 samples 100b = 16 samples 101b = 32 samples 110b = 64 samples 111b = 128 samples

8.5.5 OPMODE_CFG Register (Address = 0x4) [Reset = 0x0]

OPMODE_CFG is shown in 図 8-22 and described in 表 8-17.

Return to the 表 8-11.

図 8-22. OPMODE_CFG Register

7	6	5	4	3	2	1	0
CONV_ON_ERR	CONV_MODE[1:0]		OSC_SEL	CLK_DIV[3:0]			
R/W-0b	R/W-0b		R/W-0b	R/W-0b			

表 8-17. OPMODE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CONV_ON_ERR	R/W	0b	Control continuation of autonomous and turbo comparator modes if CRC error is detected on communication interface. 0b = If CRC error is detected, device continues channel sequencing and pin configuration is retained. See the CRCERR_IN bit for more details. 1b = If CRC error is detected, device changes all channels to analog inputs and channel sequencing is paused until CRCERR_IN flag is cleared. After clearing CRCERR_IN flag, device resumes channel sequencing and pin confguration is restored.

表 8-17. OPMODE_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-5	CONV_MODE[1:0]	R/W	0b	These bits set the mode of conversion of the ADC. 0b = Manual mode; conversions are initiated by host. 1b = Autonomous mode; conversions are initiated by the internal state machine. 10b = Turbo mode; comparisons are initiated by internal state machine.
4	OSC_SEL	R/W	0b	Selects the oscillator for internal timing generation. 0b = High-speed oscillator. 1b = Low-power oscillator.
3-0	CLK_DIV[3:0]	R/W	0b	Sampling speed control in autonomous monitoring mode (CONV_MODE = 01b). See the section on Oscillator and Timing Control for details.

8.5.6 PIN_CFG Register (Address = 0x5) [Reset = 0x0]

PIN_CFG is shown in 図 8-23 and described in 表 8-18.

Return to the 表 8-11.

図 8-23. PIN_CFG Register

7	6	5	4	3	2	1	0
PIN_CFG[7:0]							
R/W-0b							

表 8-18. PIN_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PIN_CFG[7:0]	R/W	0b	Configure device channels AIN / GPIO [7:0] as analog inputs or GPIOs. 0b = Channel is configured as an analog input. 1b = Channel is configured as a GPIO.

8.5.7 GPIO_CFG Register (Address = 0x7) [Reset = 0x0]

GPIO_CFG is shown in 図 8-24 and described in 表 8-19.

Return to the 表 8-11.

図 8-24. GPIO_CFG Register

7	6	5	4	3	2	1	0
GPIO_CFG[7:0]							
R/W-0b							

表 8-19. GPIO_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPIO_CFG[7:0]	R/W	0b	Configure GPIO[7:0] as either digital inputs or digital outputs. 0b = GPIO is configured as digital input. 1b = GPIO is configured as digital output.

8.5.8 GPO_DRIVE_CFG Register (Address = 0x9) [Reset = 0x0]

GPO_DRIVE_CFG is shown in 図 8-25 and described in 表 8-20.

Return to the 表 8-11.

図 8-25. GPO_DRIVE_CFG Register

7	6	5	4	3	2	1	0
GPO_DRIVE_CFG[7:0]							
R/W-0b							

表 8-20. GPO_DRIVE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPO_DRIVE_CFG[7:0]	R/W	0b	Configure digital outputs GPO[7:0] as open-drain or push-pull outputs. 0b = Digital output is open-drain; connect external pullup resistor. 1b = Push-pull driver is used for digital output.

8.5.9 GPO_VALUE Register (Address = 0xB) [Reset = 0x0]

GPO_VALUE is shown in 図 8-26 and described in 表 8-21.

Return to the 表 8-11.

図 8-26. GPO_VALUE Register

7	6	5	4	3	2	1	0
GPO_VALUE[7:0]							
R/W-0b							

表 8-21. GPO_VALUE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPO_VALUE[7:0]	R/W	0b	Logic level to be set on digital outputs GPO[7:0]. 0b = Digital output is set to logic 0. 1b = Digital output is set to logic 1.

8.5.10 GPI_VALUE Register (Address = 0xD) [Reset = 0x0]

GPI_VALUE is shown in 図 8-27 and described in 表 8-22.

Return to the 表 8-11.

図 8-27. GPI_VALUE Register

7	6	5	4	3	2	1	0
GPI_VALUE[7:0]							
R-0b							

表 8-22. GPI_VALUE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPI_VALUE[7:0]	R	0b	Readback the logic level on AIN/GPIO[7:0]. This field returns the readback value of logic level on all channels configured as analog inputs, digital inputs, and digital outputs. 0b = GPIO is at logic 0. 1b = GPIO is at logic 1.

8.5.11 SEQUENCE_CFG Register (Address = 0x10) [Reset = 0x0]

SEQUENCE_CFG is shown in 図 8-28 and described in 表 8-23.

Return to the 表 8-11.

図 8-28. SEQUENCE_CFG Register

7	6	5	4	3	2	1	0
RESERVED			SEQ_START	RESERVED		SEQ_MODE[1:0]	
R-0b			R/W-0b	R-0b		R/W-0b	

表 8-23. SEQUENCE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0b	Reserved Bit
4	SEQ_START	R/W	0b	Control for start of channel sequence when using auto sequence mode (SEQ_MODE = 01b). 0b = Stop channel sequencing. 1b = Start channel sequencing in ascending order for channels enabled in AUTO_SEQ_CH_SEL register.
3-2	RESERVED	R	0b	Reserved Bit
1-0	SEQ_MODE[1:0]	R/W	0b	Selects the mode of scanning of analog input channels. 0b = Manual sequence mode; channel selected by MANUAL_CHID field. 1b = Auto sequence mode; channel selected by AUTO_SEQ_CH_SEL. 10b = On-the-fly sequence mode. 11b = Reserved.

8.5.12 MANUAL_CH_SEL Register (Address = 0x11) [Reset = 0x0]

MANUAL_CH_SEL is shown in 図 8-29 and described in 表 8-24.

Return to the 表 8-11.

図 8-29. MANUAL_CH_SEL Register

7	6	5	4	3	2	1	0
RESERVED				MANUAL_CHID[3:0]			
R-0b				R/W-0b			

表 8-24. MANUAL_CH_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0b	Reserved Bit
3-0	MANUAL_CHID[3:0]	R/W	0b	In manual mode (SEQ_MODE = 00b), this field contains the 4-bit channel ID of the analog input channel for next ADC conversion. For valid ADC data, the selected channel must not be configured as GPIO in PIN_CFG register. 1xxx = Reserved. 0b = AIN0 1b = AIN1 10b = AIN2 11b = AIN3 100b = AIN4 101b = AIN5 110b = AIN6 111b = AIN7

8.5.13 AUTO_SEQ_CH_SEL Register (Address = 0x12) [Reset = 0x0]

AUTO_SEQ_CH_SEL is shown in 図 8-30 and described in 表 8-25.

Return to the 表 8-11.

図 8-30. AUTO_SEQ_CH_SEL Register

7	6	5	4	3	2	1	0

図 8-30. AUTO_SEQ_CH_SEL Register (continued)

AUTO_SEQ_CH_SEL[7:0]
R/W-0b

表 8-25. AUTO_SEQ_CH_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	AUTO_SEQ_CH_SEL[7:0]	R/W	0b	Select device channels AIN/GPIO[7:0] for auto sequencing mode. 0b = Device channel is not enabled in scanning sequence. 1b = Device channel is enabled in scanning sequence.

8.5.14 ALERT_CH_SEL Register (Address = 0x14) [Reset = 0x0]

ALERT_CH_SEL is shown in 図 8-31 and described in 表 8-26.

Return to the 表 8-11.

図 8-31. ALERT_CH_SEL Register

7	6	5	4	3	2	1	0
ALERT_CH_SEL[7:0]							
R/W-0b							

表 8-26. ALERT_CH_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ALERT_CH_SEL[7:0]	R/W	0b	Select channels for which the corresponding bits in the EVENT_FLAG register can assert the internal ALERT signal. The ALERT signal can be mapped to the digital output channel configured in the ALERT_PIN[3:0] field. 0b = Event flags for this channel do not assert the ALERT pin. 1b = Event flags for this channel assert the ALERT pin.

8.5.15 ALERT_FUNC_SEL Register (Address = 0x16) [Reset = 0x0]

ALERT_FUNC_SEL is shown in 図 8-32 and described in 表 8-27.

Return to the 表 8-11.

図 8-32. ALERT_FUNC_SEL Register

7	6	5	4	3	2	1	0
RESERVED							ALERT_CRCIN
R-0b							R/W-0b

表 8-27. ALERT_FUNC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0b	Reserved Bit
0	ALERT_CRCIN	R/W	0b	Enable or disable the alert notification for CRC error on input data (CRCERR_IN = 1b). 0b = ALERT signal is not asserted when CRCERR_IN = 1b. 1b = ALERT signal is asserted when CRCERR_IN = 1b. Clear CRCERR_IN for deasserting the ALERT pin.

8.5.16 ALERT_PIN_CFG Register (Address = 0x17) [Reset = 0x0]

ALERT_PIN_CFG is shown in 図 8-33 and described in 表 8-28.

Return to the 表 8-11.

図 8-33. ALERT_PIN_CFG Register

7	6	5	4	3	2	1	0
ALERT_PIN[3:0]				RESERVED		ALERT_LOGIC[1:0]	
R/W-0b				R-0b		R/W-0b	

表 8-28. ALERT_PIN_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	ALERT_PIN[3:0]	R/W	0b	Internal ALERT output of the digital window comparator will be output on this channel. This channel must be configured as digital output.
3-2	RESERVED	R	0b	Reserved Bit
1-0	ALERT_LOGIC[1:0]	R/W	0b	Configure how the ALERT signal is asserted. 0b = Active low. 1b = Active high. 10b = Pulsed low (one logic low pulse). 11b = Pulsed high (one logic high pulse).

8.5.17 EVENT_FLAG Register (Address = 0x18) [Reset = 0x0]

EVENT_FLAG is shown in 図 8-34 and described in 表 8-29.

Return to the 表 8-11.

図 8-34. EVENT_FLAG Register

7	6	5	4	3	2	1	0
EVENT_FLAG[7:0]							
R-0b							

表 8-29. EVENT_FLAG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EVENT_FLAG[7:0]	R	0b	Event flags indicating digital window comparator status for AIN/GPIO[7:0]. Clear individual bits of EVENT_HIGH_FLAG or EVENT_LOW_FLAG registers to clear the corresponding bit in this register. 0b = Event condition not detected. 1b = Event condition detected.

8.5.18 EVENT_HIGH_FLAG Register (Address = 0x1A) [Reset = 0x0]

EVENT_HIGH_FLAG is shown in 図 8-35 and described in 表 8-30.

Return to the 表 8-11.

図 8-35. EVENT_HIGH_FLAG Register

7	6	5	4	3	2	1	0
EVENT_HIGH_FLAG[7:0]							
R/W-0b							

表 8-30. EVENT_HIGH_FLAG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EVENT_HIGH_FLAG[7:0]	R/W	0b	Event flag corresponding to high threshold of analog input or rising edge of digital input on AIN/GPIO[7:0]. Write 1b to clear this flag. 0b = No alert condition detected. 1b = Either high threshold was exceeded (analog input) or rising edge was detected (digital input).

8.5.19 EVENT_LOW_FLAG Register (Address = 0x1C) [Reset = 0x0]

EVENT_LOW_FLAG is shown in 図 8-36 and described in 表 8-31.

Return to the 表 8-11.

図 8-36. EVENT_LOW_FLAG Register

7	6	5	4	3	2	1	0
EVENT_LOW_FLAG[7:0]							
R/W-0b							

表 8-31. EVENT_LOW_FLAG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EVENT_LOW_FLAG[7:0]	R/W	0b	Event flag corresponding to low threshold of analog input or falling edge of digital input on AIN/GPIO[7:0]. Write 1b to clear this flag. 0b = No Event condition detected. 1b = Either low threshold was exceeded (analog input) or falling edge was detected (digital input).

8.5.20 EVENT_RGN Register (Address = 0x1E) [Reset = 0x0]

EVENT_RGN is shown in 図 8-37 and described in 表 8-32.

Return to the 表 8-11.

図 8-37. EVENT_RGN Register

7	6	5	4	3	2	1	0
EVENT_RGN[7:0]							
R/W-0b							

表 8-32. EVENT_RGN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EVENT_RGN[7:0]	R/W	0b	Choice of region used in monitoring analog/digital inputs CH[7:0]. 0b = Event flag is set if: (conversion result < low threshold) or (conversion result > high threshold). For digital inputs, logic 1 sets the alert flag. 1b = Event flag is set if: (low threshold > conversion result < high threshold). For digital inputs, logic 0 sets the event flag.

8.5.21 HYSTERESIS_CH0 Register (Address = 0x20) [Reset = 0xF0]

HYSTERESIS_CH0 is shown in 図 8-38 and described in 表 8-33.

Return to the 表 8-11.

図 8-38. HYSTERESIS_CH0 Register

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH0_LSB[3:0]				HYSTERESIS_CH0[3:0]			
R/W-1111b				R/W-0b			

表 8-33. HYSTERESIS_CH0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	HIGH_THRESHOLD_CH0_LSB[3:0]	R/W	1111b	Lower 4-bits of high threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.

表 8-33. HYSTERESIS_CH0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	HYSTERESIS_CH0[3:0]	R/W	0b	4-bit hysteresis for high and low thresholds. This 4-bit hysteris is left shifted 3 times and applied on the lower 7-bits of the threshold. Total hysteresis = 7-bits [4-bits, 000b]

8.5.22 HIGH_TH_CH0 Register (Address = 0x21) [Reset = 0xFF]

HIGH_TH_CH0 is shown in 図 8-39 and described in 表 8-34.

Return to the 表 8-11.

図 8-39. HIGH_TH_CH0 Register

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH0_MSB[7:0]							
R/W-11111111b							

表 8-34. HIGH_TH_CH0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HIGH_THRESHOLD_CH0_MSB[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.5.23 EVENT_COUNT_CH0 Register (Address = 0x22) [Reset = 0x0]

EVENT_COUNT_CH0 is shown in 図 8-40 and described in 表 8-35.

Return to the 表 8-11.

図 8-40. EVENT_COUNT_CH0 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH0_LSB[3:0]				EVENT_COUNT_CH0[3:0]			
R/W-0b				R/W-0b			

表 8-35. EVENT_COUNT_CH0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	LOW_THRESHOLD_CH0_LSB[3:0]	R/W	0b	Lower 4-bits of low threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	EVENT_COUNT_CH0[3:0]	R/W	0b	Configuration for checking 'n+1' consecutive samples above threshold before setting alert flag.

8.5.24 LOW_TH_CH0 Register (Address = 0x23) [Reset = 0x0]

LOW_TH_CH0 is shown in 図 8-41 and described in 表 8-36.

Return to the 表 8-11.

図 8-41. LOW_TH_CH0 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH0_MSB[7:0]							
R/W-0b							

表 8-36. LOW_TH_CH0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LOW_THRESHOLD_CH0_MSB[7:0]	R/W	0b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.5.25 HYSTERESIS_CH1 Register (Address = 0x24) [Reset = 0xF0]

HYSTERESIS_CH1 is shown in 図 8-42 and described in 表 8-37.

Return to the 表 8-11.

図 8-42. HYSTERESIS_CH1 Register

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH1_LSB[3:0]				HYSTERESIS_CH1[3:0]			
R/W-1111b				R/W-0b			

表 8-37. HYSTERESIS_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	HIGH_THRESHOLD_CH1_LSB[3:0]	R/W	1111b	Lower 4-bits of high threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	HYSTERESIS_CH1[3:0]	R/W	0b	4-bit hysteresis for high and low thresholds. This 4-bit hysteris is left shifted 3 times and applied on the lower 7-bits of the threshold. Total hysteresis = 7-bits [4-bits, 000b]

8.5.26 HIGH_TH_CH1 Register (Address = 0x25) [Reset = 0xFF]

HIGH_TH_CH1 is shown in 図 8-43 and described in 表 8-38.

Return to the 表 8-11.

図 8-43. HIGH_TH_CH1 Register

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH1_MSB[7:0]							
R/W-11111111b							

表 8-38. HIGH_TH_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HIGH_THRESHOLD_CH1_MSB[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.5.27 EVENT_COUNT_CH1 Register (Address = 0x26) [Reset = 0x0]

EVENT_COUNT_CH1 is shown in 図 8-44 and described in 表 8-39.

Return to the 表 8-11.

図 8-44. EVENT_COUNT_CH1 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH1_LSB[3:0]				EVENT_COUNT_CH1[3:0]			
R/W-0b				R/W-0b			

表 8-39. EVENT_COUNT_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	LOW_THRESHOLD_CH1_LSB[3:0]	R/W	0b	Lower 4-bits of low threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	EVENT_COUNT_CH1[3:0]	R/W	0b	Configuration for checking 'n+1' consecutive samples above threshold before setting alert flag.

8.5.28 LOW_TH_CH1 Register (Address = 0x27) [Reset = 0x0]

LOW_TH_CH1 is shown in 図 8-45 and described in 表 8-40.

Return to the 表 8-11.

図 8-45. LOW_TH_CH1 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH1_MSB[7:0]							
R/W-0b							

表 8-40. LOW_TH_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LOW_THRESHOLD_CH1_MSB[7:0]	R/W	0b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.5.29 HYSTERESIS_CH2 Register (Address = 0x28) [Reset = 0xF0]

HYSTERESIS_CH2 is shown in 図 8-46 and described in 表 8-41.

Return to the 表 8-11.

図 8-46. HYSTERESIS_CH2 Register

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH2_LSB[3:0]				HYSTERESIS_CH2[3:0]			
R/W-1111b				R/W-0b			

表 8-41. HYSTERESIS_CH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	HIGH_THRESHOLD_CH2_LSB[3:0]	R/W	1111b	Lower 4-bits of high threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	HYSTERESIS_CH2[3:0]	R/W	0b	4-bit hysteresis for high and low thresholds. This 4-bit hysteris is left shifted 3 times and applied on the lower 7-bits of the threshold. Total hysteresis = 7-bits [4-bits, 000b]

8.5.30 HIGH_TH_CH2 Register (Address = 0x29) [Reset = 0xFF]

HIGH_TH_CH2 is shown in 図 8-47 and described in 表 8-42.

Return to the 表 8-11.

図 8-47. HIGH_TH_CH2 Register

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH2_MSB[7:0]							
R/W-11111111b							

表 8-42. HIGH_TH_CH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HIGH_THRESHOLD_CH2_MSB[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.5.31 EVENT_COUNT_CH2 Register (Address = 0x2A) [Reset = 0x0]

EVENT_COUNT_CH2 is shown in 図 8-48 and described in 表 8-43.

Return to the 表 8-11.

図 8-48. EVENT_COUNT_CH2 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH2_LSB[3:0]				EVENT_COUNT_CH2[3:0]			
R/W-0b				R/W-0b			

表 8-43. EVENT_COUNT_CH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	LOW_THRESHOLD_CH2_LSB[3:0]	R/W	0b	Lower 4-bits of low threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	EVENT_COUNT_CH2[3:0]	R/W	0b	Configuration for checking 'n+1' consecutive samples above threshold before setting alert flag.

8.5.32 LOW_TH_CH2 Register (Address = 0x2B) [Reset = 0x0]

LOW_TH_CH2 is shown in 図 8-49 and described in 表 8-44.

Return to the 表 8-11.

図 8-49. LOW_TH_CH2 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH2_MSB[7:0]							
R/W-0b							

表 8-44. LOW_TH_CH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LOW_THRESHOLD_CH2_MSB[7:0]	R/W	0b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.5.33 HYSTERESIS_CH3 Register (Address = 0x2C) [Reset = 0xF0]

HYSTERESIS_CH3 is shown in 図 8-50 and described in 表 8-45.

Return to the 表 8-11.

図 8-50. HYSTERESIS_CH3 Register

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH3_LSB[3:0]				HYSTERESIS_CH3[3:0]			
R/W-1111b				R/W-0b			

表 8-45. HYSTERESIS_CH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	HIGH_THRESHOLD_CH3_LSB[3:0]	R/W	1111b	Lower 4-bits of high threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.

表 8-45. HYSTERESIS_CH3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	HYSTERESIS_CH3[3:0]	R/W	0b	4-bit hysteresis for high and low thresholds. This 4-bit hysteris is left shifted 3 times and applied on the lower 7-bits of the threshold. Total hysteresis = 7-bits [4-bits, 000b]

8.5.34 HIGH_TH_CH3 Register (Address = 0x2D) [Reset = 0xFF]

HIGH_TH_CH3 is shown in 図 8-51 and described in 表 8-46.

Return to the 表 8-11.

図 8-51. HIGH_TH_CH3 Register

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH3_MSB[7:0]							
R/W-11111111b							

表 8-46. HIGH_TH_CH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HIGH_THRESHOLD_CH3_MSB[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.5.35 EVENT_COUNT_CH3 Register (Address = 0x2E) [Reset = 0x0]

EVENT_COUNT_CH3 is shown in 図 8-52 and described in 表 8-47.

Return to the 表 8-11.

図 8-52. EVENT_COUNT_CH3 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH3_LSB[3:0]				EVENT_COUNT_CH3[3:0]			
R/W-0b				R/W-0b			

表 8-47. EVENT_COUNT_CH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	LOW_THRESHOLD_CH3_LSB[3:0]	R/W	0b	Lower 4-bits of low threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	EVENT_COUNT_CH3[3:0]	R/W	0b	Configuration for checking 'n+1' consecutive samples above threshold before setting alert flag.

8.5.36 LOW_TH_CH3 Register (Address = 0x2F) [Reset = 0x0]

LOW_TH_CH3 is shown in 図 8-53 and described in 表 8-48.

Return to the 表 8-11.

図 8-53. LOW_TH_CH3 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH3_MSB[7:0]							
R/W-0b							

表 8-48. LOW_TH_CH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LOW_THRESHOLD_CH3_MSB[7:0]	R/W	0b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.5.37 HYSTERESIS_CH4 Register (Address = 0x30) [Reset = 0xF0]

HYSTERESIS_CH4 is shown in 図 8-54 and described in 表 8-49.

Return to the 表 8-11.

図 8-54. HYSTERESIS_CH4 Register

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH4_LSB[3:0]				HYSTERESIS_CH4[3:0]			
R/W-1111b				R/W-0b			

表 8-49. HYSTERESIS_CH4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	HIGH_THRESHOLD_CH4_LSB[3:0]	R/W	1111b	Lower 4-bits of high threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	HYSTERESIS_CH4[3:0]	R/W	0b	4-bit hysteresis for high and low thresholds. This 4-bit hysteris is left shifted 3 times and applied on the lower 7-bits of the threshold. Total hysteresis = 7-bits [4-bits, 000b]

8.5.38 HIGH_TH_CH4 Register (Address = 0x31) [Reset = 0xFF]

HIGH_TH_CH4 is shown in 図 8-55 and described in 表 8-50.

Return to the 表 8-11.

図 8-55. HIGH_TH_CH4 Register

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH4_MSB[7:0]							
R/W-11111111b							

表 8-50. HIGH_TH_CH4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HIGH_THRESHOLD_CH4_MSB[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.5.39 EVENT_COUNT_CH4 Register (Address = 0x32) [Reset = 0x0]

EVENT_COUNT_CH4 is shown in 図 8-56 and described in 表 8-51.

Return to the 表 8-11.

図 8-56. EVENT_COUNT_CH4 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH4_LSB[3:0]				EVENT_COUNT_CH4[3:0]			
R/W-0b				R/W-0b			

表 8-51. EVENT_COUNT_CH4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	LOW_THRESHOLD_CH4_LSB[3:0]	R/W	0b	Lower 4-bits of low threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	EVENT_COUNT_CH4[3:0]	R/W	0b	Configuration for checking 'n+1' consecutive samples above threshold before setting alert flag.

8.5.40 LOW_TH_CH4 Register (Address = 0x33) [Reset = 0x0]

LOW_TH_CH4 is shown in 図 8-57 and described in 表 8-52.

Return to the 表 8-11.

図 8-57. LOW_TH_CH4 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH4_MSB[7:0]							
R/W-0b							

表 8-52. LOW_TH_CH4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LOW_THRESHOLD_CH4_MSB[7:0]	R/W	0b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.5.41 HYSTERESIS_CH5 Register (Address = 0x34) [Reset = 0xF0]

HYSTERESIS_CH5 is shown in 図 8-58 and described in 表 8-53.

Return to the 表 8-11.

図 8-58. HYSTERESIS_CH5 Register

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH5_LSB[3:0]				HYSTERESIS_CH5[3:0]			
R/W-1111b				R/W-0b			

表 8-53. HYSTERESIS_CH5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	HIGH_THRESHOLD_CH5_LSB[3:0]	R/W	1111b	Lower 4-bits of high threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	HYSTERESIS_CH5[3:0]	R/W	0b	4-bit hysteresis for high and low thresholds. This 4-bit hysteris is left shifted 3 times and applied on the lower 7-bits of the threshold. Total hysteresis = 7-bits [4-bits, 000b]

8.5.42 HIGH_TH_CH5 Register (Address = 0x35) [Reset = 0xFF]

HIGH_TH_CH5 is shown in 図 8-59 and described in 表 8-54.

Return to the 表 8-11.

図 8-59. HIGH_TH_CH5 Register

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH5_MSB[7:0]							
R/W-11111111b							

表 8-54. HIGH_TH_CH5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HIGH_THRESHOLD_CH5_MSB[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.5.43 EVENT_COUNT_CH5 Register (Address = 0x36) [Reset = 0x0]

EVENT_COUNT_CH5 is shown in 図 8-60 and described in 表 8-55.

Return to the 表 8-11.

図 8-60. EVENT_COUNT_CH5 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH5_LSB[3:0]				EVENT_COUNT_CH5[3:0]			
R/W-0b				R/W-0b			

表 8-55. EVENT_COUNT_CH5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	LOW_THRESHOLD_CH5_LSB[3:0]	R/W	0b	Lower 4-bits of low threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	EVENT_COUNT_CH5[3:0]	R/W	0b	Configuration for checking 'n+1' consecutive samples above threshold before setting alert flag.

8.5.44 LOW_TH_CH5 Register (Address = 0x37) [Reset = 0x0]

LOW_TH_CH5 is shown in 図 8-61 and described in 表 8-56.

Return to the 表 8-11.

図 8-61. LOW_TH_CH5 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH5_MSB[7:0]							
R/W-0b							

表 8-56. LOW_TH_CH5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LOW_THRESHOLD_CH5_MSB[7:0]	R/W	0b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.5.45 HYSTERESIS_CH6 Register (Address = 0x38) [Reset = 0xF0]

HYSTERESIS_CH6 is shown in 図 8-62 and described in 表 8-57.

Return to the 表 8-11.

図 8-62. HYSTERESIS_CH6 Register

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH6_LSB[3:0]				HYSTERESIS_CH6[3:0]			
R/W-1111b				R/W-0b			

表 8-57. HYSTERESIS_CH6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	HIGH_THRESHOLD_CH6_LSB[3:0]	R/W	1111b	Lower 4-bits of high threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.

表 8-57. HYSTERESIS_CH6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	HYSTERESIS_CH6[3:0]	R/W	0b	4-bit hysteresis for high and low thresholds. This 4-bit hysteris is left shifted 3 times and applied on the lower 7-bits of the threshold. Total hysteresis = 7-bits [4-bits, 000b]

8.5.46 HIGH_TH_CH6 Register (Address = 0x39) [Reset = 0xFF]

HIGH_TH_CH6 is shown in 図 8-63 and described in 表 8-58.

Return to the 表 8-11.

図 8-63. HIGH_TH_CH6 Register

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH6_MSB[7:0]							
R/W-11111111b							

表 8-58. HIGH_TH_CH6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HIGH_THRESHOLD_CH6_MSB[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.5.47 EVENT_COUNT_CH6 Register (Address = 0x3A) [Reset = 0x0]

EVENT_COUNT_CH6 is shown in 図 8-64 and described in 表 8-59.

Return to the 表 8-11.

図 8-64. EVENT_COUNT_CH6 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH6_LSB[3:0]				EVENT_COUNT_CH6[3:0]			
R/W-0b				R/W-0b			

表 8-59. EVENT_COUNT_CH6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	LOW_THRESHOLD_CH6_LSB[3:0]	R/W	0b	Lower 4-bits of low threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	EVENT_COUNT_CH6[3:0]	R/W	0b	Configuration for checking 'n+1' consecutive samples above threshold before setting alert flag.

8.5.48 LOW_TH_CH6 Register (Address = 0x3B) [Reset = 0x0]

LOW_TH_CH6 is shown in 図 8-65 and described in 表 8-60.

Return to the 表 8-11.

図 8-65. LOW_TH_CH6 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH6_MSB[7:0]							
R/W-0b							

表 8-60. LOW_TH_CH6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LOW_THRESHOLD_CH6_MSB[7:0]	R/W	0b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.5.49 HYSTERESIS_CH7 Register (Address = 0x3C) [Reset = 0xF0]

HYSTERESIS_CH7 is shown in 図 8-66 and described in 表 8-61.

Return to the 表 8-11.

図 8-66. HYSTERESIS_CH7 Register

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH7_LSB[3:0]				HYSTERESIS_CH7[3:0]			
R/W-1111b				R/W-0b			

表 8-61. HYSTERESIS_CH7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	HIGH_THRESHOLD_CH7_LSB[3:0]	R/W	1111b	Lower 4-bits of high threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	HYSTERESIS_CH7[3:0]	R/W	0b	4-bit hysteresis for high and low thresholds. This 4-bit hysteris is left shifted 3 times and applied on the lower 7-bits of the threshold. Total hysteresis = 7-bits [4-bits, 000b]

8.5.50 HIGH_TH_CH7 Register (Address = 0x3D) [Reset = 0xFF]

HIGH_TH_CH7 is shown in 図 8-67 and described in 表 8-62.

Return to the 表 8-11.

図 8-67. HIGH_TH_CH7 Register

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH7_MSB[7:0]							
R/W-11111111b							

表 8-62. HIGH_TH_CH7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HIGH_THRESHOLD_CH7_MSB[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.5.51 EVENT_COUNT_CH7 Register (Address = 0x3E) [Reset = 0x0]

EVENT_COUNT_CH7 is shown in 図 8-68 and described in 表 8-63.

Return to the 表 8-11.

図 8-68. EVENT_COUNT_CH7 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH7_LSB[3:0]				EVENT_COUNT_CH7[3:0]			
R/W-0b				R/W-0b			

表 8-63. EVENT_COUNT_CH7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	LOW_THRESHOLD_CH7_LSB[3:0]	R/W	0b	Lower 4-bits of low threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	EVENT_COUNT_CH7[3:0]	R/W	0b	Configuration for checking 'n+1' consecutive samples above threshold before setting alert flag.

8.5.52 LOW_TH_CH7 Register (Address = 0x3F) [Reset = 0x0]

LOW_TH_CH7 is shown in 図 8-69 and described in 表 8-64.

Return to the 表 8-11.

図 8-69. LOW_TH_CH7 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH7_MSB[7:0]							
R/W-0b							

表 8-64. LOW_TH_CH7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LOW_THRESHOLD_CH7_MSB[7:0]	R/W	0b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.5.53 MAX_CH0_LSB Register (Address = 0x60) [Reset = 0x0]

MAX_CH0_LSB is shown in 図 8-70 and described in 表 8-65.

Return to the 表 8-11.

図 8-70. MAX_CH0_LSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH0_LSB[7:0]							
R-0b							

表 8-65. MAX_CH0_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH0_LSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

8.5.54 MAX_CH0_MSB Register (Address = 0x61) [Reset = 0x0]

MAX_CH0_MSB is shown in 図 8-71 and described in 表 8-66.

Return to the 表 8-11.

図 8-71. MAX_CH0_MSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH0_MSB[7:0]							
R-0b							

表 8-66. MAX_CH0_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH0_MSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

8.5.55 MAX_CH1_LSB Register (Address = 0x62) [Reset = 0x0]

MAX_CH1_LSB is shown in 図 8-72 and described in 表 8-67.

Return to the 表 8-11.

図 8-72. MAX_CH1_LSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH1_LSB[7:0]							
R-0b							

表 8-67. MAX_CH1_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH1_LSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

8.5.56 MAX_CH1_MSB Register (Address = 0x63) [Reset = 0x0]

MAX_CH1_MSB is shown in 図 8-73 and described in 表 8-68.

Return to the 表 8-11.

図 8-73. MAX_CH1_MSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH1_MSB[7:0]							
R-0b							

表 8-68. MAX_CH1_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH1_MSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

8.5.57 MAX_CH2_LSB Register (Address = 0x64) [Reset = 0x0]

MAX_CH2_LSB is shown in 図 8-74 and described in 表 8-69.

Return to the 表 8-11.

図 8-74. MAX_CH2_LSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH2_LSB[7:0]							
R-0b							

表 8-69. MAX_CH2_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH2_LSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

8.5.58 MAX_CH2_MSB Register (Address = 0x65) [Reset = 0x0]

MAX_CH2_MSB is shown in 図 8-75 and described in 表 8-70.

Return to the 表 8-11.

図 8-75. MAX_CH2_MSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH2_MSB[7:0]							
R-0b							

表 8-70. MAX_CH2_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH2_MSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

8.5.59 MAX_CH3_LSB Register (Address = 0x66) [Reset = 0x0]

MAX_CH3_LSB is shown in 図 8-76 and described in 表 8-71.

Return to the 表 8-11.

図 8-76. MAX_CH3_LSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH3_LSB[7:0]							
R-0b							

表 8-71. MAX_CH3_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH3_LSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

8.5.60 MAX_CH3_MSB Register (Address = 0x67) [Reset = 0x0]

MAX_CH3_MSB is shown in 図 8-77 and described in 表 8-72.

Return to the 表 8-11.

図 8-77. MAX_CH3_MSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH3_MSB[7:0]							
R-0b							

表 8-72. MAX_CH3_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH3_MSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

8.5.61 MAX_CH4_LSB Register (Address = 0x68) [Reset = 0x0]

MAX_CH4_LSB is shown in 図 8-78 and described in 表 8-73.

Return to the 表 8-11.

図 8-78. MAX_CH4_LSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH4_LSB[7:0]							
R-0b							

表 8-73. MAX_CH4_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH4_LSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

8.5.62 MAX_CH4_MSB Register (Address = 0x69) [Reset = 0x0]

MAX_CH4_MSB is shown in 図 8-79 and described in 表 8-74.

Return to the 表 8-11.

図 8-79. MAX_CH4_MSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH4_MSB[7:0]							
R-0b							

表 8-74. MAX_CH4_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH4_MSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

8.5.63 MAX_CH5_LSB Register (Address = 0x6A) [Reset = 0x0]

MAX_CH5_LSB is shown in 図 8-80 and described in 表 8-75.

Return to the 表 8-11.

図 8-80. MAX_CH5_LSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH5_LSB[7:0]							
R-0b							

表 8-75. MAX_CH5_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH5_LSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

8.5.64 MAX_CH5_MSB Register (Address = 0x6B) [Reset = 0x0]

MAX_CH5_MSB is shown in 図 8-81 and described in 表 8-76.

Return to the 表 8-11.

図 8-81. MAX_CH5_MSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH5_MSB[7:0]							
R-0b							

表 8-76. MAX_CH5_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH5_MSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

8.5.65 MAX_CH6_LSB Register (Address = 0x6C) [Reset = 0x0]

MAX_CH6_LSB is shown in 図 8-82 and described in 表 8-77.

Return to the 表 8-11.

図 8-82. MAX_CH6_LSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH6_LSB[7:0]							
R-0b							

表 8-77. MAX_CH6_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH6_LSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

8.5.66 MAX_CH6_MSB Register (Address = 0x6D) [Reset = 0x0]

MAX_CH6_MSB is shown in 図 8-83 and described in 表 8-78.

Return to the 表 8-11.

図 8-83. MAX_CH6_MSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH6_MSB[7:0]							
R-0b							

表 8-78. MAX_CH6_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH6_MSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

8.5.67 MAX_CH7_LSB Register (Address = 0x6E) [Reset = 0x0]

MAX_CH7_LSB is shown in 図 8-84 and described in 表 8-79.

Return to the 表 8-11.

図 8-84. MAX_CH7_LSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH7_LSB[7:0]							
R-0b							

表 8-79. MAX_CH7_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH7_LSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

8.5.68 MAX_CH7_MSB Register (Address = 0x6F) [Reset = 0x0]

MAX_CH7_MSB is shown in 図 8-85 and described in 表 8-80.

Return to the 表 8-11.

図 8-85. MAX_CH7_MSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH7_MSB[7:0]							
R-0b							

表 8-80. MAX_CH7_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH7_MSB[7:0]	R	0b	Maximum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0.

8.5.69 MIN_CH0_LSB Register (Address = 0x80) [Reset = 0xFF]

MIN_CH0_LSB is shown in 図 8-86 and described in 表 8-81.

Return to the 表 8-11.

図 8-86. MIN_CH0_LSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH0_LSB[7:0]							
R-11111111b							

表 8-81. MIN_CH0_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH0_LSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

8.5.70 MIN_CH0_MSB Register (Address = 0x81) [Reset = 0xFF]

MIN_CH0_MSB is shown in 図 8-87 and described in 表 8-82.

Return to the 表 8-11.

図 8-87. MIN_CH0_MSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH0_MSB[7:0]							
R-11111111b							

表 8-82. MIN_CH0_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH0_MSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

8.5.71 MIN_CH1_LSB Register (Address = 0x82) [Reset = 0xFF]

MIN_CH1_LSB is shown in 図 8-88 and described in 表 8-83.

Return to the 表 8-11.

図 8-88. MIN_CH1_LSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH1_LSB[7:0]							
R-11111111b							

表 8-83. MIN_CH1_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH1_LSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

8.5.72 MIN_CH1_MSB Register (Address = 0x83) [Reset = 0xFF]

MIN_CH1_MSB is shown in 図 8-89 and described in 表 8-84.

Return to the 表 8-11.

図 8-89. MIN_CH1_MSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH1_MSB[7:0]							
R-11111111b							

表 8-84. MIN_CH1_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH1_MSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

8.5.73 MIN_CH2_LSB Register (Address = 0x84) [Reset = 0xFF]

MIN_CH2_LSB is shown in 図 8-90 and described in 表 8-85.

Return to the 表 8-11.

図 8-90. MIN_CH2_LSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH2_LSB[7:0]							
R-11111111b							

表 8-85. MIN_CH2_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH2_LSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

8.5.74 MIN_CH2_MSB Register (Address = 0x85) [Reset = 0xFF]

MIN_CH2_MSB is shown in 図 8-91 and described in 表 8-86.

Return to the 表 8-11.

図 8-91. MIN_CH2_MSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH2_MSB[7:0]							
R-11111111b							

表 8-86. MIN_CH2_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH2_MSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

8.5.75 MIN_CH3_LSB Register (Address = 0x86) [Reset = 0xFF]

MIN_CH3_LSB is shown in 図 8-92 and described in 表 8-87.

Return to the 表 8-11.

図 8-92. MIN_CH3_LSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH3_LSB[7:0]							
R-11111111b							

表 8-87. MIN_CH3_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH3_LSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

8.5.76 MIN_CH3_MSB Register (Address = 0x87) [Reset = 0xFF]

MIN_CH3_MSB is shown in 図 8-93 and described in 表 8-88.

Return to the 表 8-11.

図 8-93. MIN_CH3_MSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH3_MSB[7:0]							
R-11111111b							

表 8-88. MIN_CH3_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH3_MSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

8.5.77 MIN_CH4_LSB Register (Address = 0x88) [Reset = 0xFF]

MIN_CH4_LSB is shown in 図 8-94 and described in 表 8-89.

Return to the 表 8-11.

図 8-94. MIN_CH4_LSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH4_LSB[7:0]							
R-11111111b							

表 8-89. MIN_CH4_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH4_LSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

8.5.78 MIN_CH4_MSB Register (Address = 0x89) [Reset = 0xFF]

MIN_CH4_MSB is shown in 図 8-95 and described in 表 8-90.

Return to the 表 8-11.

図 8-95. MIN_CH4_MSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH4_MSB[7:0]							
R-11111111b							

表 8-90. MIN_CH4_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH4_MSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

8.5.79 MIN_CH5_LSB Register (Address = 0x8A) [Reset = 0xFF]

MIN_CH5_LSB is shown in 図 8-96 and described in 表 8-91.

Return to the 表 8-11.

図 8-96. MIN_CH5_LSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH5_LSB[7:0]							
R-11111111b							

表 8-91. MIN_CH5_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH5_LSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

8.5.80 MIN_CH5_MSB Register (Address = 0x8B) [Reset = 0xFF]

MIN_CH5_MSB is shown in 図 8-97 and described in 表 8-92.

Return to the 表 8-11.

図 8-97. MIN_CH5_MSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH5_MSB[7:0]							
R-11111111b							

表 8-92. MIN_CH5_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH5_MSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

8.5.81 MIN_CH6_LSB Register (Address = 0x8C) [Reset = 0xFF]

MIN_CH6_LSB is shown in 図 8-98 and described in 表 8-93.

Return to the 表 8-11.

図 8-98. MIN_CH6_LSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH6_LSB[7:0]							
R-11111111b							

表 8-93. MIN_CH6_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH6_LSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

8.5.82 MIN_CH6_MSB Register (Address = 0x8D) [Reset = 0xFF]

MIN_CH6_MSB is shown in 図 8-99 and described in 表 8-94.

Return to the 表 8-11.

図 8-99. MIN_CH6_MSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH6_MSB[7:0]							
R-11111111b							

表 8-94. MIN_CH6_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH6_MSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

8.5.83 MIN_CH7_LSB Register (Address = 0x8E) [Reset = 0xFF]

MIN_CH7_LSB is shown in 図 8-100 and described in 表 8-95.

Return to the 表 8-11.

図 8-100. MIN_CH7_LSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH7_LSB[7:0]							
R-11111111b							

表 8-95. MIN_CH7_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH7_LSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

8.5.84 MIN_CH7_MSB Register (Address = 0x8F) [Reset = 0xFF]

MIN_CH7_MSB is shown in 図 8-101 and described in 表 8-96.

Return to the 表 8-11.

図 8-101. MIN_CH7_MSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH7_MSB[7:0]							
R-11111111b							

表 8-96. MIN_CH7_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH7_MSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register will reset the value to 0xFF.

8.5.85 RECENT_CH0_LSB Register (Address = 0xA0) [Reset = 0x0]

RECENT_CH0_LSB is shown in 図 8-102 and described in 表 8-97.

Return to the 表 8-11.

図 8-102. RECENT_CH0_LSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH0_LSB[7:0]							
R-0b							

表 8-97. RECENT_CH0_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH0_LSB[7:0]	R	0b	Next 8 bits of the last result for this analog input channel.

8.5.86 RECENT_CH0_MSB Register (Address = 0xA1) [Reset = 0x0]

RECENT_CH0_MSB is shown in 図 8-103 and described in 表 8-98.

Return to the 表 8-11.

図 8-103. RECENT_CH0_MSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH0_MSB[7:0]							
R-0b							

表 8-98. RECENT_CH0_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH0_MSB[7:0]	R	0b	MSB aligned first 8 bits of the last result for this analog input channel.

8.5.87 RECENT_CH1_LSB Register (Address = 0xA2) [Reset = 0x0]

RECENT_CH1_LSB is shown in 図 8-104 and described in 表 8-99.

Return to the 表 8-11.

図 8-104. RECENT_CH1_LSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH1_LSB[7:0]							
R-0b							

表 8-99. RECENT_CH1_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH1_LSB[7:0]	R	0b	Next 8 bits of the last result for this analog input channel.

8.5.88 RECENT_CH1_MSB Register (Address = 0xA3) [Reset = 0x0]

RECENT_CH1_MSB is shown in 図 8-105 and described in 表 8-100.

Return to the 表 8-11.

図 8-105. RECENT_CH1_MSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH1_MSB[7:0]							
R-0b							

表 8-100. RECENT_CH1_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH1_MSB[7:0]	R	0b	MSB aligned first 8 bits of the last result for this analog input channel.

8.5.89 RECENT_CH2_LSB Register (Address = 0xA4) [Reset = 0x0]

RECENT_CH2_LSB is shown in 図 8-106 and described in 表 8-101.

Return to the 表 8-11.

図 8-106. RECENT_CH2_LSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH2_LSB[7:0]							
R-0b							

表 8-101. RECENT_CH2_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH2_LSB[7:0]	R	0b	Next 8 bits of the last result for this analog input channel.

8.5.90 RECENT_CH2_MSB Register (Address = 0xA5) [Reset = 0x0]

RECENT_CH2_MSB is shown in 図 8-107 and described in 表 8-102.

Return to the 表 8-11.

図 8-107. RECENT_CH2_MSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH2_MSB[7:0]							
R-0b							

表 8-102. RECENT_CH2_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH2_MSB[7:0]	R	0b	MSB aligned first 8 bits of the last result for this analog input channel.

8.5.91 RECENT_CH3_LSB Register (Address = 0xA6) [Reset = 0x0]

RECENT_CH3_LSB is shown in 図 8-108 and described in 表 8-103.

Return to the 表 8-11.

図 8-108. RECENT_CH3_LSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH3_LSB[7:0]							
R-0b							

表 8-103. RECENT_CH3_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH3_LSB[7:0]	R	0b	Next 8 bits of the last result for this analog input channel.

8.5.92 RECENT_CH3_MSB Register (Address = 0xA7) [Reset = 0x0]

RECENT_CH3_MSB is shown in 図 8-109 and described in 表 8-104.

Return to the 表 8-11.

図 8-109. RECENT_CH3_MSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH3_MSB[7:0]							
R-0b							

表 8-104. RECENT_CH3_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH3_MSB[7:0]	R	0b	MSB aligned first 8 bits of the last result for this analog input channel.

8.5.93 RECENT_CH4_LSB Register (Address = 0xA8) [Reset = 0x0]

RECENT_CH4_LSB is shown in 図 8-110 and described in 表 8-105.

Return to the 表 8-11.

図 8-110. RECENT_CH4_LSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH4_LSB[7:0]							
R-0b							

表 8-105. RECENT_CH4_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH4_LSB[7:0]	R	0b	Next 8 bits of the last result for this analog input channel.

8.5.94 RECENT_CH4_MSB Register (Address = 0xA9) [Reset = 0x0]

RECENT_CH4_MSB is shown in 図 8-111 and described in 表 8-106.

Return to the 表 8-11.

図 8-111. RECENT_CH4_MSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH4_MSB[7:0]							
R-0b							

表 8-106. RECENT_CH4_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH4_MSB[7:0]	R	0b	MSB aligned first 8 bits of the last result for this analog input channel.

8.5.95 RECENT_CH5_LSB Register (Address = 0xAA) [Reset = 0x0]

RECENT_CH5_LSB is shown in 図 8-112 and described in 表 8-107.

Return to the 表 8-11.

図 8-112. RECENT_CH5_LSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH5_LSB[7:0]							
R-0b							

表 8-107. RECENT_CH5_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH5_LSB[7:0]	R	0b	Next 8 bits of the last result for this analog input channel.

8.5.96 RECENT_CH5_MSB Register (Address = 0xAB) [Reset = 0x0]

RECENT_CH5_MSB is shown in 図 8-113 and described in 表 8-108.

Return to the 表 8-11.

図 8-113. RECENT_CH5_MSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH5_MSB[7:0]							
R-0b							

表 8-108. RECENT_CH5_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH5_MSB[7:0]	R	0b	MSB aligned first 8 bits of the last result for this analog input channel.

8.5.97 RECENT_CH6_LSB Register (Address = 0xAC) [Reset = 0x0]

RECENT_CH6_LSB is shown in 図 8-114 and described in 表 8-109.

Return to the 表 8-11.

図 8-114. RECENT_CH6_LSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH6_LSB[7:0]							
R-0b							

表 8-109. RECENT_CH6_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH6_LSB[7:0]	R	0b	Next 8 bits of the last result for this analog input channel.

8.5.98 RECENT_CH6_MSB Register (Address = 0xAD) [Reset = 0x0]

RECENT_CH6_MSB is shown in 図 8-115 and described in 表 8-110.

Return to the 表 8-11.

図 8-115. RECENT_CH6_MSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH6_MSB[7:0]							
R-0b							

表 8-110. RECENT_CH6_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH6_MSB[7:0]	R	0b	MSB aligned first 8 bits of the last result for this analog input channel.

8.5.99 RECENT_CH7_LSB Register (Address = 0xAE) [Reset = 0x0]

RECENT_CH7_LSB is shown in 図 8-116 and described in 表 8-111.

Return to the 表 8-11.

図 8-116. RECENT_CH7_LSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH7_LSB[7:0]							
R-0b							

表 8-111. RECENT_CH7_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH7_LSB[7:0]	R	0b	Next 8 bits of the last result for this analog input channel.

8.5.100 RECENT_CH7_MSB Register (Address = 0xAF) [Reset = 0x0]

RECENT_CH7_MSB is shown in 図 8-117 and described in 表 8-112.

Return to the 表 8-11.

図 8-117. RECENT_CH7_MSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH7_MSB[7:0]							
R-0b							

表 8-112. RECENT_CH7_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH7_MSB[7:0]	R	0b	MSB aligned first 8 bits of the last result for this analog input channel.

8.5.101 GPO0_EVENT_CFG Register (Address = 0xC3) [Reset = 0x0]

GPO0_EVENT_CFG is shown in 図 8-118 and described in 表 8-113.

Return to the 表 8-11.

図 8-118. GPO0_EVENT_CFG Register

7	6	5	4	3	2	1	0
GPO0_EVENT_CFG[7:0]							
R/W-0b							

表 8-113. GPO0_EVENT_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPO0_EVENT_CFG[7:0]	R/W	0b	Select the inputs AIN/GPIO[7:0], analog or digital, which can trigger an event based update on GPO0. 0b = Event flags for the AIN/GPIO corresponding to this bit do not trigger GPO0 output. 1b = Event flags for the AIN/GPIO corresponding to this bit trigger GPO0 output.

8.5.102 GPO1_EVENT_CFG Register (Address = 0xC5) [Reset = 0x0]

GPO1_EVENT_CFG is shown in 図 8-119 and described in 表 8-114.

Return to the 表 8-11.

図 8-119. GPO1_EVENT_CFG Register

7	6	5	4	3	2	1	0
GPO1_EVENT_CFG[7:0]							
R/W-0b							

表 8-114. GPO1_EVENT_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPO1_EVENT_CFG[7:0]	R/W	0b	Select the inputs AIN/GPIO[7:0], analog or digital, which can trigger an event based update on GPO1. 0b = Event flags for the AIN/GPIO corresponding to this bit do not trigger GPO1 output. 1b = Event flags for the AIN/GPIO corresponding to this bit trigger GPO1 output.

8.5.103 GPO2_EVENT_CFG Register (Address = 0xC7) [Reset = 0x0]

GPO2_EVENT_CFG is shown in 図 8-120 and described in 表 8-115.

Return to the 表 8-11.

図 8-120. GPO2_EVENT_CFG Register

7	6	5	4	3	2	1	0
GPO2_EVENT_CFG[7:0]							
R/W-0b							

表 8-115. GPO2_EVENT_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPO2_EVENT_CFG[7:0]	R/W	0b	Select the inputs AIN/GPIO[7:0], analog or digital, which can trigger an event based update on GPO2. 0b = Event flags for the AIN/GPIO corresponding to this bit do not trigger GPO2 output. 1b = Event flags for the AIN/GPIO corresponding to this bit trigger GPO2 output.

8.5.104 GPO3_EVENT_CFG Register (Address = 0xC9) [Reset = 0x0]

GPO3_EVENT_CFG is shown in 図 8-121 and described in 表 8-116.

Return to the 表 8-11.

図 8-121. GPO3_EVENT_CFG Register

7	6	5	4	3	2	1	0
GPO3_EVENT_CFG[7:0]							
R/W-0b							

表 8-116. GPO3_EVENT_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPO3_EVENT_CFG[7:0]	R/W	0b	Select the inputs AIN/GPIO[7:0], analog or digital, which can trigger an event based update on GPO3. 0b = Event flags for the AIN/GPIO corresponding to this bit do not trigger GPO3 output. 1b = Event flags for the AIN/GPIO corresponding to this bit trigger GPO3 output.

8.5.105 GPO4_EVENT_CFG Register (Address = 0xCB) [Reset = 0x0]

GPO4_EVENT_CFG is shown in 図 8-122 and described in 表 8-117.

Return to the 表 8-11.

図 8-122. GPO4_EVENT_CFG Register

7	6	5	4	3	2	1	0
GPO4_EVENT_CFG[7:0]							
R/W-0b							

表 8-117. GPO4_EVENT_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPO4_EVENT_CFG[7:0]	R/W	0b	Select the inputs AIN/GPIO[7:0], analog or digital, which can trigger an event based update on GPO4. 0b = Event flags for the AIN/GPIO corresponding to this bit do not trigger GPO4 output. 1b = Event flags for the AIN/GPIO corresponding to this bit trigger GPO4 output.

8.5.106 GPO5_EVENT_CFG Register (Address = 0xCD) [Reset = 0x0]

GPO5_EVENT_CFG is shown in 図 8-123 and described in 表 8-118.

Return to the 表 8-11.

図 8-123. GPO5_EVENT_CFG Register

7	6	5	4	3	2	1	0
GPO5_EVENT_CFG[7:0]							
R/W-0b							

表 8-118. GPO5_EVENT_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPO5_EVENT_CFG[7:0]	R/W	0b	Select the inputs AIN/GPIO[7:0], analog or digital, which can trigger an event based update on GPO5. 0b = Event flags for the AIN/GPIO corresponding to this bit do not trigger GPO5 output. 1b = Event flags for the AIN/GPIO corresponding to this bit trigger GPO5 output.

8.5.107 GPO6_EVENT_CFG Register (Address = 0xCF) [Reset = 0x0]

GPO6_EVENT_CFG is shown in 図 8-124 and described in 表 8-119.

Return to the 表 8-11.

図 8-124. GPO6_EVENT_CFG Register

7	6	5	4	3	2	1	0
GPO6_EVENT_CFG[7:0]							
R/W-0b							

表 8-119. GPO6_EVENT_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPO6_EVENT_CFG[7:0]	R/W	0b	Select the inputs AIN/GPIO[7:0], analog or digital, which can trigger an event based update on GPO6. 0b = Event flags for the AIN/GPIO corresponding to this bit do not trigger GPO6 output. 1b = Event flags for the AIN/GPIO corresponding to this bit trigger GPO6 output.

8.5.108 GPO7_EVENT_CFG Register (Address = 0xD1) [Reset = 0x0]

GPO7_EVENT_CFG is shown in 図 8-125 and described in 表 8-120.

Return to the 表 8-11.

図 8-125. GPO7_EVENT_CFG Register

7	6	5	4	3	2	1	0
GPO7_EVENT_CFG[7:0]							
R/W-0b							

表 8-120. GPO7_EVENT_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPO7_EVENT_CFG[7:0]	R/W	0b	Select the inputs AIN/GPIO[7:0], analog or digital, which can trigger an event based update on GPO7. 0b = Event flags for the AIN/GPIO corresponding to this bit do not trigger GPO7 output. 1b = Event flags for the AIN/GPIO corresponding to this bit trigger GPO7 output.

8.5.109 GPO_UPDATE_ON_EVENT Register (Address = 0xE9) [Reset = 0x0]

GPO_UPDATE_ON_EVENT is shown in 図 8-126 and described in 表 8-121.

Return to the 表 8-11.

図 8-126. GPO_UPDATE_ON_EVENT Register

7	6	5	4	3	2	1	0

図 8-126. GPO_UPDATE_ON_EVENT Register (continued)

GPO_UPDATE_ON_EVENT[7:0]
R/W-0b

表 8-121. GPO_UPDATE_ON_EVENT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPO_UPDATE_ON_EVENT[7:0]	R/W	0b	Update digital outputs GPO[7:0] when the corresponding trigger is set. 0b = Digital output is not updated in response to the alert flags. 1b = Digital output is updated when the corresponding alert flags are set. Configure GPOx_TRIG_EVENT_SEL register to select which alert flags can trigger an update on the desired GPO.

8.5.110 GPO_VALUE_ON_EVENT Register (Address = 0xEB) [Reset = 0x0]

GPO_VALUE_ON_EVENT is shown in 図 8-127 and described in 表 8-122.

Return to the 表 8-11.

図 8-127. GPO_VALUE_ON_EVENT Register

7	6	5	4	3	2	1	0
GPO_VALUE_ON_EVENT[7:0]							
R/W-0b							

表 8-122. GPO_VALUE_ON_EVENT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPO_VALUE_ON_EVENT[7:0]	R/W	0b	Value to be set on digital outputs GPO[7:0] when the corresponding trigger occurs. GPO update on alert flags must be enabled in the corresponding bit in the GPO_TRIGGER_CFG register. 0b = Digital output is set to logic 0. 1b = Digital output is set to logic 1.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The two primary circuits required to maximize the performance of a high-precision, successive approximation register analog-to-digital converter (SAR ADC) are the input driver and the reference driver circuits. This section details some general principles for designing the input driver circuit, reference driver circuit, and provides some application circuits designed for the ADS7038-Q1.

9.2 Typical Applications

9.2.1 Mixed-Channel Configuration

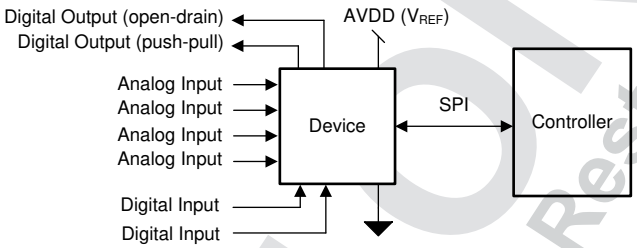


図 9-1. DAQ Circuit: Single-Supply DAQ

9.2.1.1 Design Requirements

The goal of this application is to configure some channels of the ADS7038-Q1 as digital inputs, open-drain digital outputs, and push-pull digital outputs.

9.2.1.2 Detailed Design Procedure

The ADS7038-Q1 can support GPIO functionality at each input pin. Any analog input pin can be independently configured as a digital input, a digital open-drain output, or a digital push-pull output though the PIN_CFG and GPIO_CFG registers; see 表 8-4.

9.2.1.2.1 Digital Input

The digital input functionality can be used to monitor a signal within the system. 図 9-2 illustrates that the state of the digital input can be read from the GPI_VALUE register.

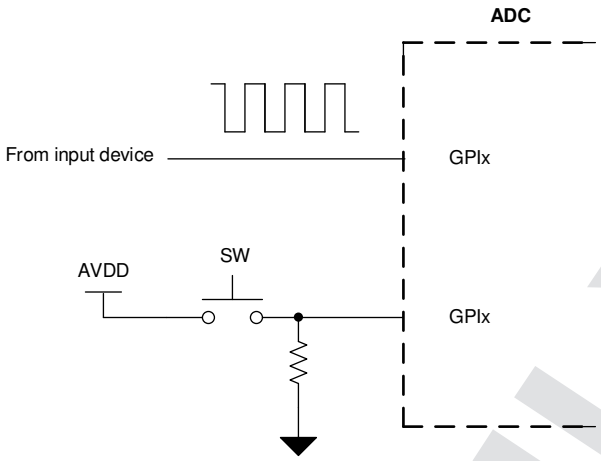


図 9-2. Digital Input

9.2.1.2.2 Digital Open-Drain Output

The channels of the ADS7038-Q1 can be configured as digital open-drain outputs supporting an output voltage up to 5.5 V. An open-drain output, as shown in 図 9-3, consists of an internal FET (Q) connected to ground. The output is idle when not driven by the device, which means Q is off and the pullup resistor, R_{PULL_UP}, connects the GPOx node to the desired output voltage. The output voltage can range anywhere up to 5.5 V, depending on the external voltage that the GPIOx is pulled up to. When the device is driving the output, Q turns on, thus connecting the pullup resistor to ground and bringing the node voltage at GPOx low.

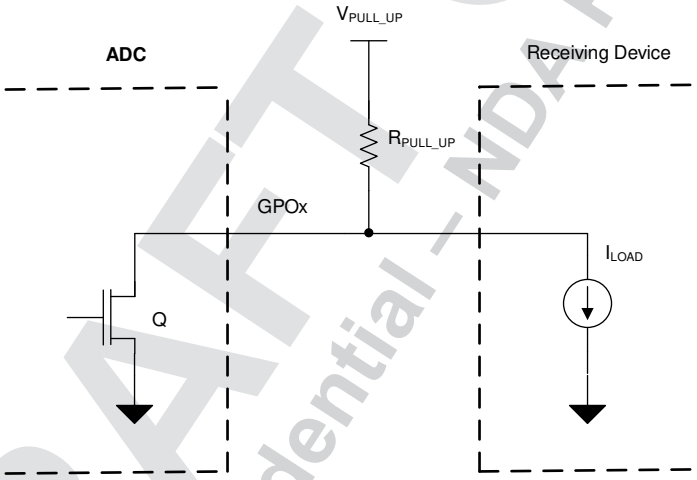


図 9-3. Digital Open-Drain Output

The minimum value of the pullup resistor, as calculated in 式 3, is given by the ratio of V_{PULL_UP} and the maximum current supported by the device digital output (5 mA).

$$R_{MIN} = (V_{PULL\_UP} / 5\ mA) \quad (3)$$

The maximum value of the pullup resistor, as calculated in 式 4, depends on the minimum input current requirement, I_{LOAD}, of the receiving device driven by this GPIO.

$$R_{MAX} = (V_{PULL\_UP} / I_{LOAD}) \quad (4)$$

Select R_{PULL_UP} such that $R_{MIN} < R_{PULL\_UP} < R_{MAX}$.

9.2.1.3 Application Curve

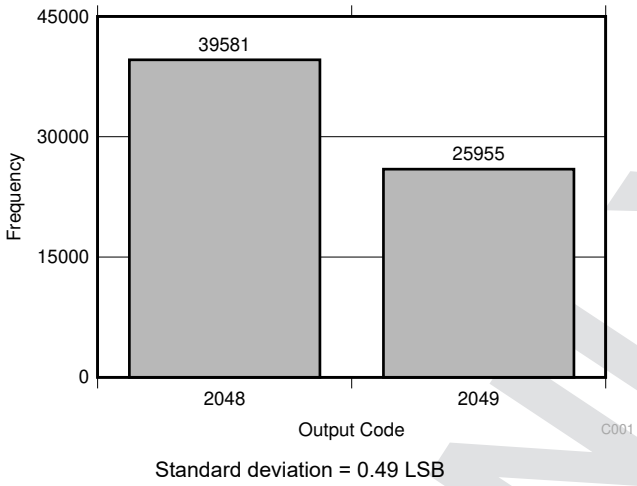


図 9-4. DC Input Histogram

9.2.2 Digital Push-Pull Output Configuration

The channels of the ADS7038-Q1 can be configured as digital push-pull outputs supporting an output voltage up to AVDD. As shown in 図 9-5, a push-pull output consists of two mirrored opposite bipolar transistors, Q1 and Q2. The device can both source and sink current because only one transistor is on at a time (either Q2 is on and pulls the output low, or Q1 is on and sets the output high). A push-pull configuration always drives the line opposed to an open-drain output where the line is left floating.

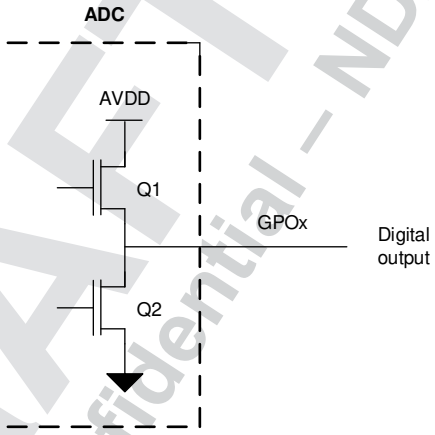


図 9-5. Digital Push-Pull Output

10 Power Supply Recommendations

10.1 AVDD and DVDD Supply Recommendations

The ADS7038-Q1 has two separate power supplies: AVDD and DVDD. The device operates on AVDD; DVDD is used for the interface circuits. For supplies greater than 2.35 V, AVDD and DVDD can be shorted externally if single-supply operation is desired. The AVDD supply also defines the full-scale input range of the device. Decouple the AVDD and DVDD pins individually, as shown in 図 10-1, with 1-µF ceramic decoupling capacitors. The minimum capacitor value required for AVDD and DVDD is 200 nF and 20 nF, respectively. If both supplies are powered from the same source, a minimum capacitor value of 220 nF is required for decoupling.

Connect 1-µF ceramic decoupling capacitors between the DECAP and GND pins.

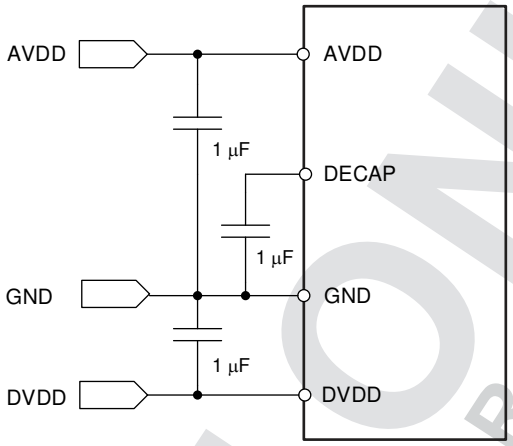


図 10-1. Power-Supply Decoupling

11 Layout

11.1 Layout Guidelines

図 11-1 shows a board layout example for the ADS7038-Q1. Avoid crossing digital lines with the analog signal path and keep the analog input signals and the AVDD supply away from noise sources.

Use 1-µF ceramic bypass capacitors in close proximity to the analog (AVDD) and digital (DVDD) power-supply pins. Avoid placing vias between the AVDD and DVDD pins and the bypass capacitors. Connect the GND pin to the ground plane using short, low-impedance paths. The AVDD supply voltage also functions as the reference voltage for the ADS7038-Q1. Place the decoupling capacitor for AVDD close to the device AVDD and GND pins and connect the decoupling capacitor to the device pins with thick copper tracks.

11.2 Layout Example

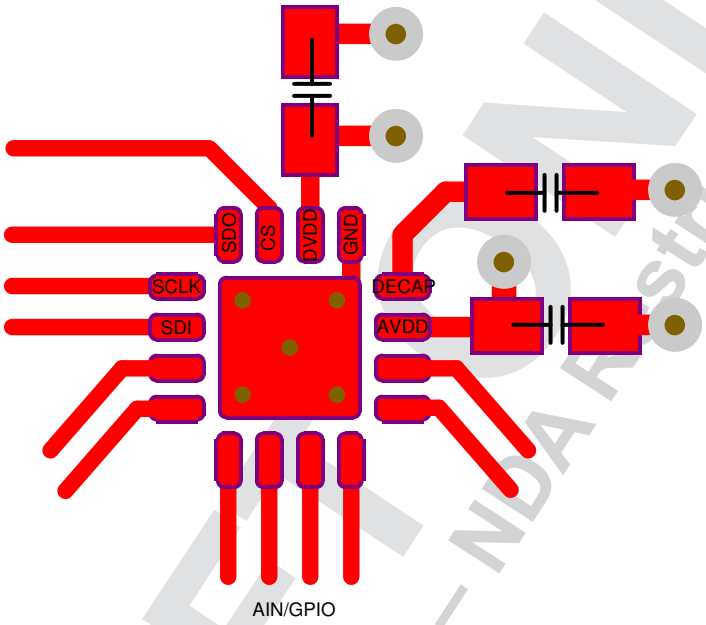


図 11-1. Example Layout

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 Trademarks

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12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7038QRTERQ1	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7038Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

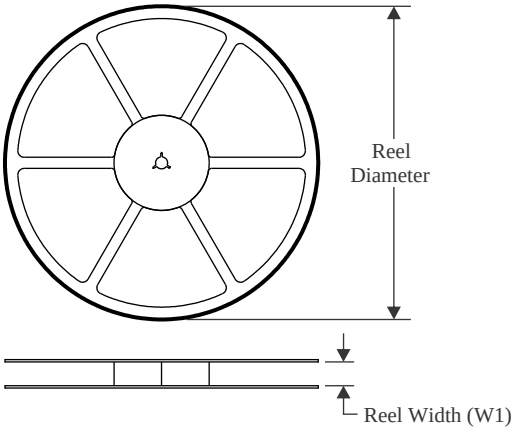
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

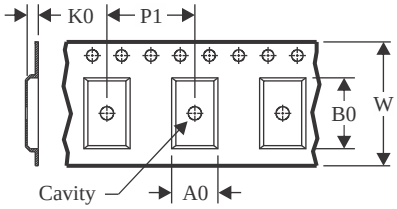
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

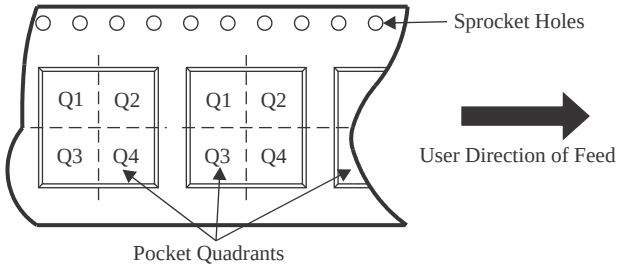


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

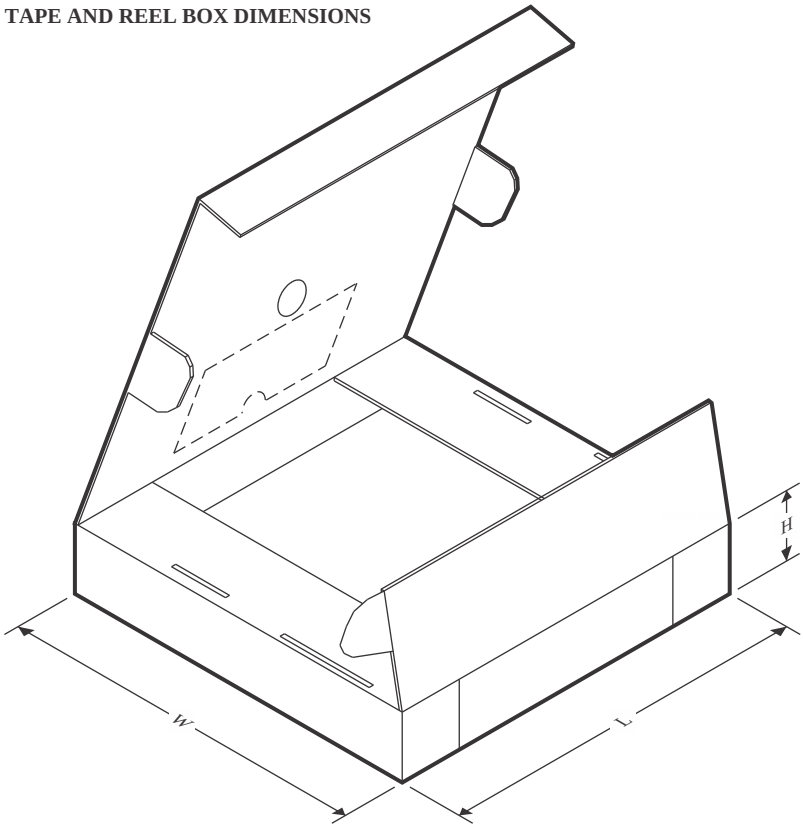
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7038QRTERQ1	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7038QRTERQ1	WQFN	RTE	16	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

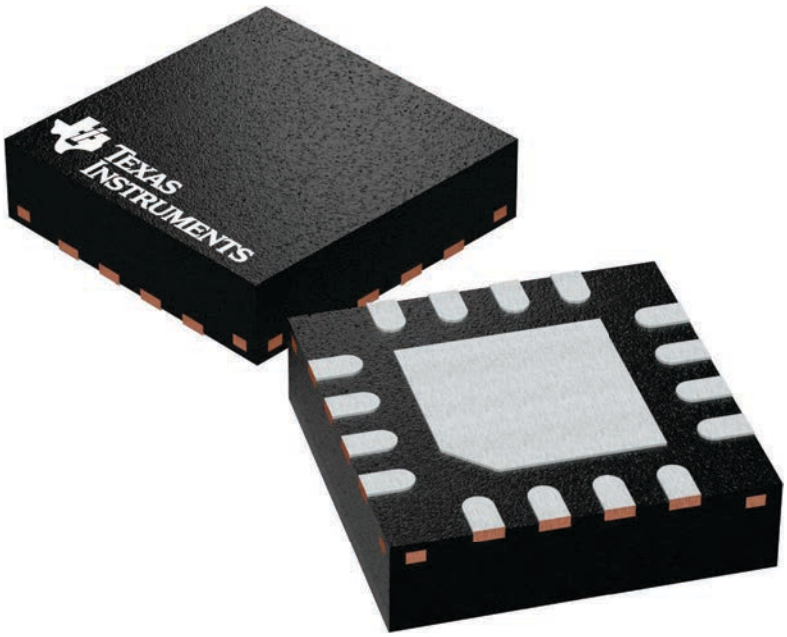
RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

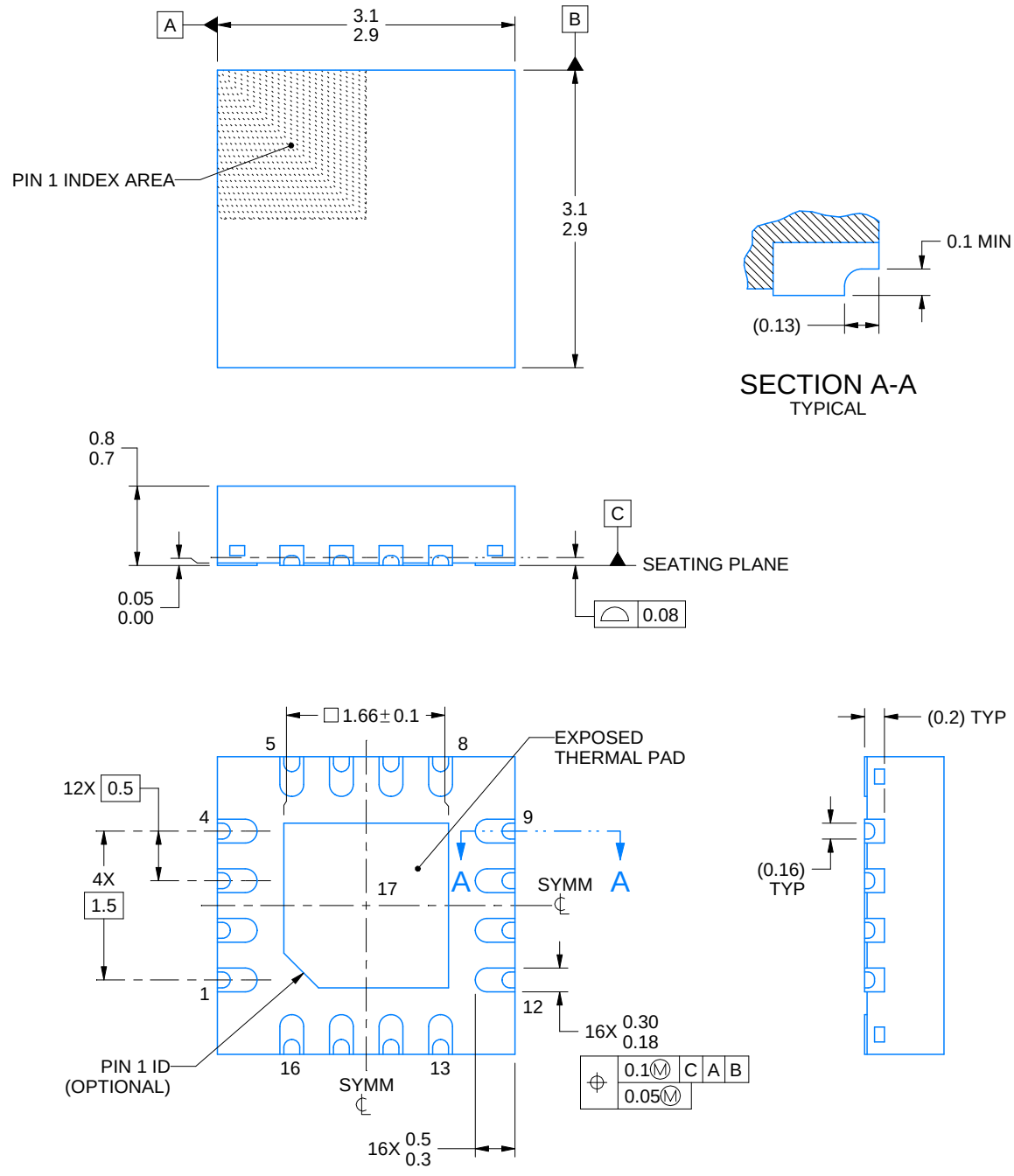


RTE0016K

PACKAGE OUTLINE

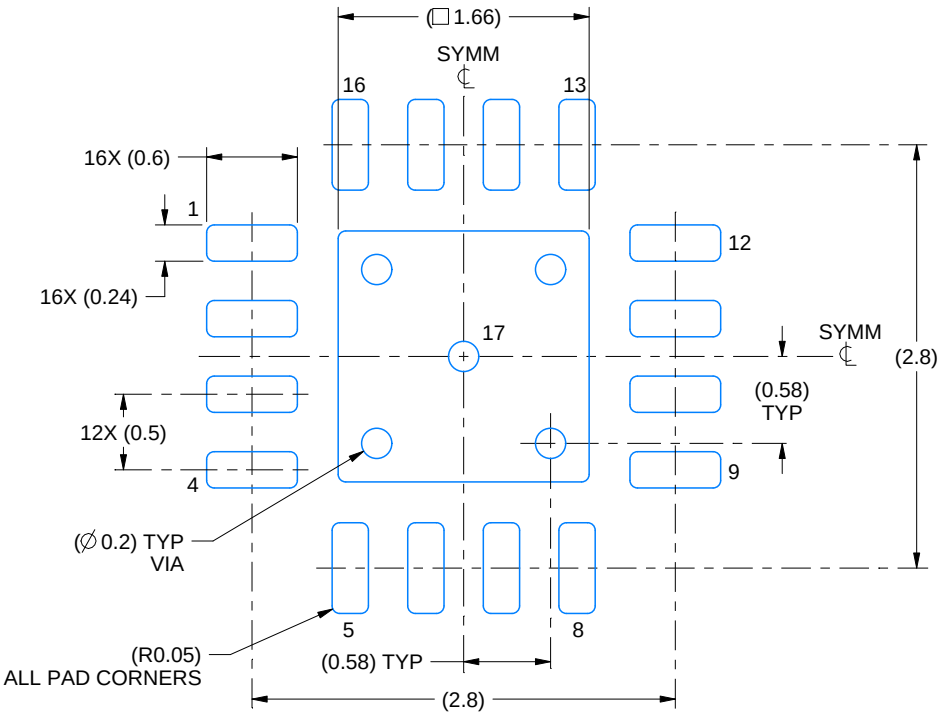
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

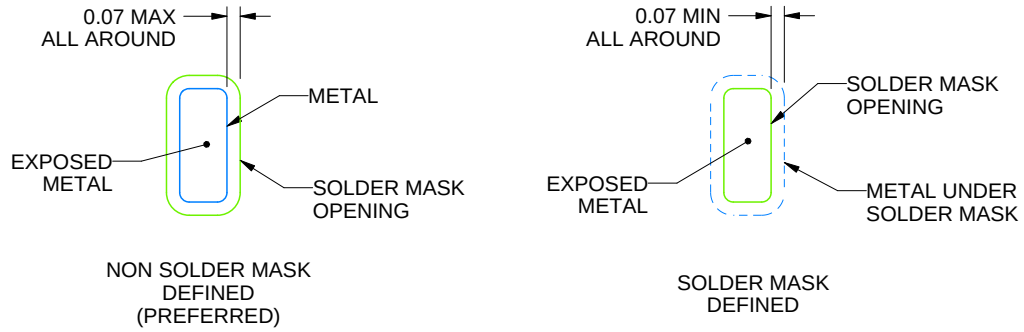


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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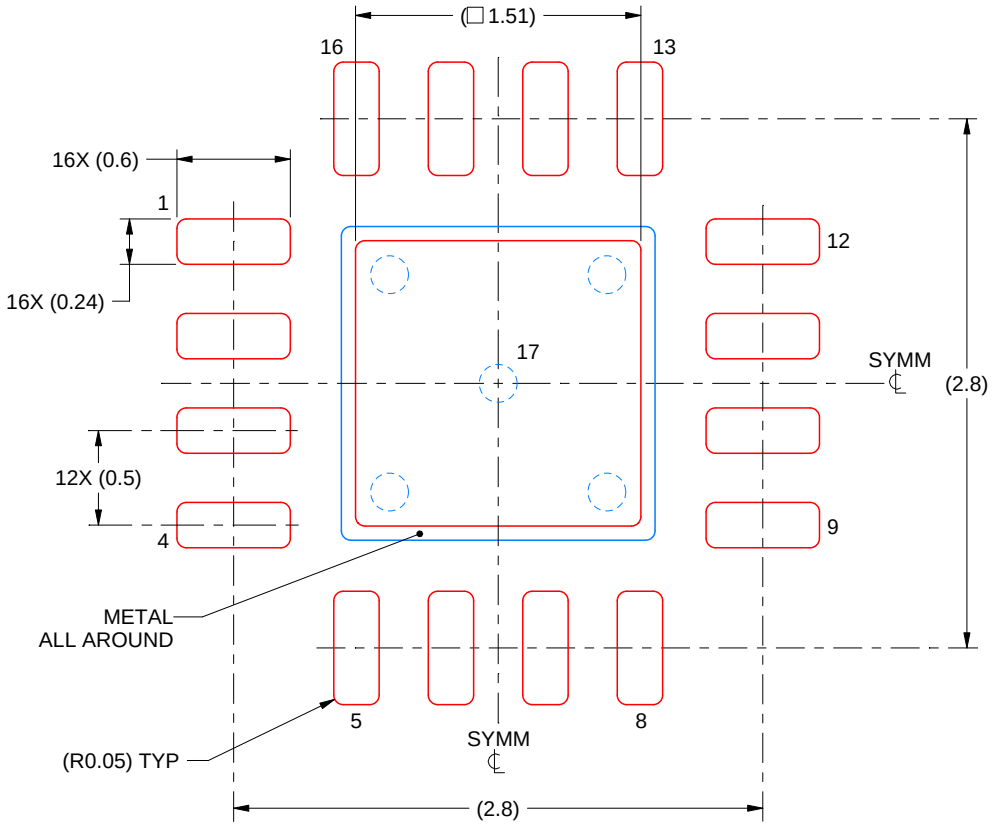
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
84% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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