AFE790 6 チャネル、5MHz～12GHz RF サンプリング・レシーバ、3GSPS ADC 付き

1 特長

- データシート全体のご請求
- 6 個の RF サンプリング、14 ビット、3GSPS の ADC
- 最大 RF 信号帯域幅:
  - 4 つの ADC:ADC ごとに 1200MHz
  - 6 つの ADC:ADC ごとに 600MHz
- RF 周波数範囲:5MHz～12GHz
- デジタル・ステップ・アッテネータ (DSA):25dB レンジ、0.5dB ステップ
- シングル DDC (6 チャネルの場合) またはデュアルバンド DDC (4 チャネルの場合)
- DDC チャネルごとに 16 個の NCO
- ADC クロック用の内部 PLL / VCO、または ADC サンプル・レートでの外部クロックを選択可能
- Sysref アライメント検出器
- SerDes データ・インターフェイス:
  - JESD204B、JESD204C 適合
  - 8 つの SerDes トランスミッタ (最高 29.5Gbps)
  - サブクラス 1 のマルチデバイス同期
- パッケージ:17mm × 17mm FCBGA、0.8mm ピッチ

2 アプリケーション

- レーダー
- 追尾フロント・エンド
- 防衛無線
- ワイヤレス通信テスト

3 概要

AFE7906 は、高性能、広帯域幅のマルチチャネル・レシーバで、6 つの RF サンプリング ADC を内蔵しています。このデバイスは、最大 12GHz で動作するため、追加の周波数変換段を必要とせず、L、S、C、X バンドの周波数範囲について直接 RF サンプリングが可能です。密度と柔軟性の向上により、多くのチャネル数を持つマルチミッション・システムが可能になります。

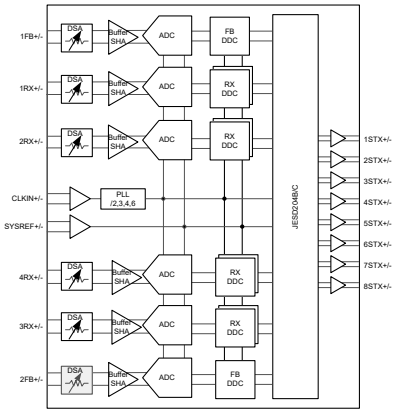
各レシーバ・チェーンは、3GSPS の ADC (A/D コンバータ) に接続された 25dB レンジの DSA (デジタル・ステップ・アッテネータ) を備えています。4 つのレシーバ・チャネルは、外部または内部の自律的な AGC (自動ゲイン制御) を補助するためのアナログ・ピーク電力検出器とさまざまなデジタル電力検出器、およびデバイスの信頼性を確保するための RF 過負荷検出器を備えています。柔軟なデシメーション・オプションによりデータ帯域幅を 4 つの RX では最高 1200MHz、または 600MHz で最適化できます。

SYSREF タイミング検出器を搭載しているため、デバイス・クロックを基準とした SYSREF 入力タイミングの最適化が可能です。

パッケージ情報

部品番号	パッケージ (1)	パッケージ・サイズ (2)
AFE7906	FC-BGA	17.00mm × 17.00mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。
(2) パッケージ・サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



機能ブロック図

Table of Contents

4 概要 (続き)

各レシーバ・チェーンは、3GSPS の ADC (A/D コンバータ) に接続された 25dB レンジの DSA (デジタル・ステップ・アッテネータ) を備えています。各レシーバ・チャネルは、外部または内部の自律的な AGC (自動ゲイン制御) を補助するためのアナログ・ピーク電力検出器とさまざまなデジタル電力検出器、およびデバイスの信頼性を確保するための RF 過負荷検出器を備えています。柔軟なデシメーション・オプションによりデータ帯域幅を最適化でき、FB パスなしの 4 つの RX では最高 1200MHz 、2 つの FB パス付き (それぞれ 1200MHz の帯域幅) では最高 600MHz が得られます。

SYSREF タイミング検出器を搭載しているため、デバイス・クロックを基準とした SYSREF 入力タイミングの最適化が可能です。

5 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from July 9, 2022 to May 30, 2023 (from Revision B (July 2022) to Revision C (May 2023)) **Page**

- 「製品情報」表を「パッケージ情報」表に変更 1
- Changed I_{IH} and I_{IL} units to µA..... 14

Changes from March 11, 2022 to July 8, 2022 (from Revision A (March 2022) to Revision B (July 2022)) **Page**

- Deleted ABJ from the Thermal Information table. The table applies to both ABJ and the ALK packages..... 4
- Changed 0RX - 3RX to 1RX - 4RX in several plots..... 41
- Changed 0RX - 3RX to 1RX - 4RX in several plots..... 46

Changes from Revision * (January 2022) to Revision A (March 2022) **Page**

- 「データシート全体のご請求」に「特長」を追加..... 1
- Added the Specification tables to the data sheet..... 4
- Changed Power Mode 4 to f_{RX} = 2.25 GHz..... 15
- Added the Typical Characteristics section to the data sheet..... 19

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply Voltage Range	DVDD0P9, VDDT0P9	–0.3	1.2	V
	VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2PLL, VDD1P2PLLCLKREF, VDD1P2FB, VDD1P2FBCML, VDD1P2RXCML	–0.3	1.4	V
	VDD1P8RX, VDD1P8RXCLK, VDD1P8TX, VDD1P8TXDAC, VDD1P8TXENC, VDD1P8PLL, VDD1P8PLLVCO, VDD1P8FB, VDD1P8FBCLK, VDD1P8GPIO, VDDA1P8	–0.5	2.1	V
Pin Volatge Range	{1/2/3/4}RXIN+/-	–0.5	VDDRX1P8+0.3	V
	1FBIN+/-, 2FB+/-	–0.5	VDDFB1P8+0.3	V
	REFCLK+/-, SYSREF+/-	–0.3	1.4	V
	{1:8}STX+/-	–0.3	1.4	V
	GPIO{B/C/D/E}x, SPICLK, SPISDIO, SPISDO, SPISEN, RESETZ, BISTB0, BISTB1	–0.5	VDD1P8GPIO + 0.3	V
	IFORCE, VSENSE	–0.3	VDDCLK1P8 + 0.3	V
	SRDAMUX1, SRDAMUX2	–0.3	VDDA1P8+0.3	V
Peak Input Current	any input		20	mA
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	1000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	150	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible if necessary precautions are taken.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
DVDD0P9, VDDT0P9	Supply voltage 0.9V	0.9	0.925	0.95	V
VDD1P2{RX/TXCLK/TXENC/FB/PLL/PLLCLKREF/FBCML/RXCML}	Supply voltage 1.2V	1.15	1.2	1.25	V
VDD1P8{RX/RXCLK/TX/TXDAC/TXENC/PLL/PLLVCO/FB/FBCLK/GPIO}, VDDA1P8	Supply voltage 1.8V	1.75	1.8	1.85	V
T_A	Ambient temperature	–40		85	°C
T_J	Operating Junction Temperature			110(1)	°C
	Maximum Operating Junction Temperature	125			°C

(1) Prolonged use at or above this junction temperature can increase the device failure-in-time (FIT) rate. Refer to SBAA403 application note for additional details

6.4 Thermal Information

THERMAL METRIC(1)		AFE7906 FC-BGA 400 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	16.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.42	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	4.85	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.12	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	4.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 RF ADC Electrical Characteristics

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; RX Output Rate = 491.52MSPS below 6GHz input frequency and 1500MSPS above 6GHz input frequency, f_{ADC} = 2949.12MSPS; PLL clock mode with f_{REF} = 491.52MHz below 6GHz input frequency and External clock mode with f_{CLK} = 2949.12MHz above 6GHz input frequency; nominal power supplies; DSA Setting =3dB; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC_{RES}	ADC resolution			14		bits
F_{RFin}	RF input frequency range		5		12000	MHz
$P_{FS\_CW,min}$	Min Full scale input power, at device pins (1)	f_{IN} = 5 MHz, DSA=0dB, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-0.4		dBm
		f_{IN} = 30 MHz, DSA=0dB, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		-2.2		
		f_{IN} = 410 MHz, DSA=0dB, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 12		-2.5		
		f_{IN} = 830 MHz, DSA=0dB		-2.9		
		f_{IN} = 1760 MHz, DSA=0dB		-2.8		
		f_{IN} = 2610 MHz, DSA=0dB		-1.8		
		f_{IN} = 3610 MHz, DSA=0dB		-0.4		
		f_{IN} = 4910 MHz, DSA=0dB		0.1		
		f_{IN} = 8150 MHz, DSA=0dB		2.1		
		f_{IN} = 9610 MHz, DSA=0dB		4.3		
$P_{FS\_CW,MAX}$	MAX Full scale input power - reliability limited, at device pins	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		19.7		dBm
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		17.8		
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		17.6		
		f_{IN} = 830 MHz		16.7		
		f_{IN} = 1760 MHz		17.0		
		f_{IN} = 2610 MHz		18		
		f_{IN} = 3610 MHz		18.5		
		f_{IN} = 4910 MHz		19.3		
		f_{IN} = 8150 MHz		21.3		
		f_{IN} = 9610 MHz		23.5		
R_{TERM}	Input reference impedance			100.0		Ω
ATT_{range}	DSA Attenuation range			25.0		dB
ATT_{step}	DSA Attenuation step			0.5		dB
	DSA Attenuation step accuracy	Delta=Gatt(X)-Gatt(X-1), F_{in}=3610MHz, after calibration		0.1		
	DSA Gain Steps Phase accuracy any 8dB range	F_{in}=3610MHz, after calibration		0.9		deg
	DSA Gain Steps Phase accuracy any 8dB range	F_{in}=4910MHz, after calibration		1.8		
G_{flat}	Gain flatness	Measured Over 80MHz BW		0.2		dB
		Measured Over 200MHz BW		0.5		
		Measured Over 400MHz BW		1.1		

6.5 RF ADC Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; RX Output Rate = 491.52MSPS below 6GHz input frequency and 1500MSPS above 6GHz input frequency, f_{ADC} = 2949.12MSPS; PLL clock mode with f_{REF} = 491.52MHz below 6GHz input frequency and External clock mode with f_{CLK} = 2949.12MHz above 6GHz input frequency; nominal power supplies; DSA Setting =3dB; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NSD	Noise Density (small signal = -30dBFS)	f_{IN} = 5 MHz, DSA = 3dB, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-147.1		dBFS/Hz
		f_{IN} = 30 MHz, DSA = 3dB, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		-150.7		
		f_{IN} = 410 MHz, DSA = 3dB, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		-155.4		
		f_{IN} = 830 MHz, DSA = 3dB(3)		-156.2		
		f_{IN} = 1760 MHz, DSA = 3dB(3)		-156.0		
		f_{IN} = 2610 MHz, DSA = 3dB(3)		-155.4		
		f_{IN} = 3610 MHz, DSA = 3dB(3)		-155.1		
		f_{IN} = 4910 MHz, DSA = 3dB(3)		-155.1		
		f_{IN} = 8110 MHz, DSA = 3dB(3)		-152		
		f_{IN} = 9610 MHz, DSA = 3dB(3)		-151		
		f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48, 3<=Atten<=22		-147.8		
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24, 3<=Atten<=22		-151.5		
		f_{IN} = 410 MHz, 3<=Atten<=22, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		-156.6		
		f_{IN} = 830 MHz, 3<=Atten<=22		-156.0		
		f_{IN} = 1760 MHz, 3<=Atten<=25		-155.8		
		f_{IN} = 2610 MHz, 3<=Atten<=25		-155.7		
		f_{IN} = 3610 MHz, 3<=Atten<=25		-155.4		
		f_{IN} = 4910 MHz, 3<=Atten<=25		-155.8		
		f_{IN} = 8150 MHz, 3<=Atten<=25		-152.5		
		f_{IN} = 9610 MHz, 3<=Atten<=25		-152.5		
NF_{min}	Noise Figure min DSA Atten=0 - 3dB	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		29.4		dB
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		24.5		
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		19.3		
		f_{IN} = 830 MHz		19.1		
		f_{IN} = 1760 MHz		19.0		
		f_{IN} = 2610 MHz		20.9		
		f_{IN} = 3610 MHz		22.8		
		f_{IN} = 4910 MHz		22.4		
		f_{IN} = 8150 MHz		27.3		
		f_{IN} = 9610 MHz		30		

6.5 RF ADC Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; RX Output Rate = 491.52MSPS below 6GHz input frequency and 1500MSPS above 6GHz input frequency, f_{ADC} = 2949.12MSPS; PLL clock mode with f_{REF} = 491.52MHz below 6GHz input frequency and External clock mode with f_{CLK} = 2949.12MHz above 6GHz input frequency; nominal power supplies; DSA Setting =3dB; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NF	Noise Figure[4] DSA Atten=4dB	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		30.6		dB
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		25.1		
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		20.1		
		f_{IN} = 830 MHz		20.0		
		f_{IN} = 1760 MHz		20.6		
		f_{IN} = 2610 MHz		21.9		
		f_{IN} = 3610 MHz		23.5		
		f_{IN} = 4910 MHz		22.3		
		f_{IN} = 8150 MHz		27.9		
		f_{IN} = 9610 MHz		30.7		
NF_{max}	Noise Figure[4] DSA Atten=20dB	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		45.9		dB
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		40.2		
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		35.0		
		f_{IN} = 830 MHz		34.7		
		f_{IN} = 1760 MHz		35.2		
		f_{IN} = 2610 MHz		36.0		
		f_{IN} = 3610 MHz		37.3		
		f_{IN} = 4910 MHz		37.6		
		f_{IN} = 8150 MHz		42.8		
		f_{IN} = 9610 MHz		45		
IMD3	3rd order intermodulation 2 tones at at f_{IN} ± 10MHz -7dBFS each tone	f_{IN} = 30±1 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		-82		dBc
		f_{IN} = 400MHz and 405MHz, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		-75		
		f_{IN} = 840 MHz, 3<=Atten<=12		-82		
		f_{IN} = 1770 MHz, 3<=Atten<=12		-84		
		f_{IN} = 2610 MHz, 3<=Atten<=12		-74		
		f_{IN} = 3610 MHz, 3<=Atten<=12		-77		
		f_{IN} = 4920 MHz, 3<=Atten<=12		-76		
		f_{IN} = 8150 MHz, 3<=Atten<=12, 25MHz tone spacing		-59		
		f_{IN} = 9610 MHz, 3<=Atten<=12, 25MHz tone spacing		-60		

6.5 RF ADC Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; RX Output Rate = 491.52MSPS below 6GHz input frequency and 1500MSPS above 6GHz input frequency, f_{ADC} = 2949.12MSPS; PLL clock mode with f_{REF} = 491.52MHz below 6GHz input frequency and External clock mode with f_{CLK} = 2949.12MHz above 6GHz input frequency; nominal power supplies; DSA Setting =3dB; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SFDR	Spurious Free Dynamic Range within output bandwidth, A_{IN} = -3 dBFS	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		78		dBFS
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		100		
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		94		
		f_{IN} = 830 MHz		88		
		f_{IN} = 1760 MHz		81		
		f_{IN} = 2610 MHz		88		
		f_{IN} = 3610 MHz		84		
		f_{IN} = 4910 MHz		79		
		f_{IN} = 8150 MHz		78		
		f_{IN} = 9610 MHz		71		
HD2	2nd Harmonic Distortion A_{IN} = -3 dBFS(2)	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-84		dBFS
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, Bypass Mode (TI only test mode)		-91		
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, Bypass Mode (TI only test mode)		-90		
		f_{IN} = 830 MHz		-86		
		f_{IN} = 1760 MHz		-90		
		f_{IN} = 2610 MHz		-88		
		f_{IN} = 3610 MHz		-87		
		f_{IN} = 4910 MHz		-84		
		f_{IN} = 8150 MHz		-70		
		f_{IN} = 9610 MHz		-70		
HD3	3rd Harmonic Distortion A_{IN} = -3 dBFS	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-78		dBFS
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, Bypass Mode (TI only test mode)		-96		
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, Bypass Mode (TI only test mode)		-94		
		f_{IN} = 830 MHz		-80		
		f_{IN} = 1760 MHz		-85		
		f_{IN} = 2610 MHz		-86		
		f_{IN} = 3610 MHz		-78		
		f_{IN} = 4910 MHz		-75		
		f_{IN} = 8150 MHz		-70		
		f_{IN} = 9610 MHz		-70		

6.5 RF ADC Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; RX Output Rate = 491.52MSPS below 6GHz input frequency and 1500MSPS above 6GHz input frequency, f_{ADC} = 2949.12MSPS; PLL clock mode with f_{REF} = 491.52MHz below 6GHz input frequency and External clock mode with f_{CLK} = 2949.12MHz above 6GHz input frequency; nominal power supplies; DSA Setting =3dB; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HDn, n>3	SFDR excl. HD2 and HD3 A_{IN} = -3 dBFS	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-94		dBFS
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		-94		
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		-94		
		f_{IN} = 830 MHz		-88		
		f_{IN} = 1760 MHz		-81		
		f_{IN} = 2610 MHz		-88		
		f_{IN} = 3610 MHz		-84		
		f_{IN} = 4910 MHz		-82		
		f_{IN} = 8150 MHz		-78		
		f_{IN} = 9610 MHz		-71		
SFDR	Spurious Free Dynamic Range A_{IN} = -13 dBFS	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		101		dBFS
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		105		
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		95		
		f_{IN} = 830 MHz		89		
		f_{IN} = 1760 MHz		89		
		f_{IN} = 2610 MHz		95		
		f_{IN} = 3610 MHz		87		
		f_{IN} = 4910 MHz		90		
		f_{IN} = 8150 MHz		83		
		f_{IN} = 9610 MHz		80		
HD2	2nd Harmonic Distortion(2) A_{IN} = -13 dBFS	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-104		dBFS
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, Bypass Mode (TI only test mode)		-91		
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, Bypass Mode (TI only test mode)		-104		
		f_{IN} = 830 MHz, with board trim		-79		
		f_{IN} = 1760 MHz, with board trim		-102		
		f_{IN} = 2610 MHz, with board trim		-100		
		f_{IN} = 3610 MHz, with board trim		-101		
		f_{IN} = 4910 MHz, with board trim		-99		
		f_{IN} = 8150 MHz, with board trim		-107		
		f_{IN} = 9610 MHz, with board trim		-107		

6.5 RF ADC Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; RX Output Rate = 491.52MSPS below 6GHz input frequency and 1500MSPS above 6GHz input frequency, f_{ADC} = 2949.12MSPS; PLL clock mode with f_{REF} = 491.52MHz below 6GHz input frequency and External clock mode with f_{CLK} = 2949.12MHz above 6GHz input frequency; nominal power supplies; DSA Setting =3dB; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HD3	3rd Harmonic Distortion A_{IN} = -13 dBFS	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-103		dBFS
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, Bypass Mode (TI only test mode)		-84		
		f_{IN} = 381 MHz, f_{ADC} = 3000MSPS, Bypass Mode (TI only test mode)		-91		
		f_{IN} = 830 MHz		-95		
		f_{IN} = 1760 MHz		-95		
		f_{IN} = 2610 MHz		-98		
		f_{IN} = 3610 MHz		-97		
		f_{IN} = 4910 MHz		-94		
		f_{IN} = 8150 MHz		-100		
		f_{IN} = 9610 MHz		-102		
HDn, n>3	SFDR excl. HD2 and HD3 A_{IN} = -13 dBFS	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-104		dBFS
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		-105		
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		-95		
		f_{IN} = 830 MHz		-89		
		f_{IN} = 1760 MHz		-89		
		f_{IN} = 2610 MHz		-95		
		f_{IN} = 3610 MHz		-90		
		f_{IN} = 4910 MHz		-90		
		f_{IN} = 8150 MHz		-83		
		f_{IN} = 9610 MHz		-80		
RX-RX/FB Isolation	Near Channel: 1RXIN to 2RXIN 3RXIN to 4RXIN 1FBIN to 1RXIN 2FBIN to 3RXIN	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-98		dB
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		-98		
		f_{IN} = 400 MHz		-88		
		f_{IN} = 830 MHz		-77		
		f_{IN} = 1760 MHz		-71		
		f_{IN} = 2610 MHz		-74		
		f_{IN} = 3610 MHz		-77		
		f_{IN} = 4910 MHz		-65		
		f_{IN} = 8150 MHz		-68		
		f_{IN} = 9610 MHz		-68		

(1) The input fullscale at minimum attenuation can be reduce by adding a digital gain range to the DSA, extending the useful range of the DSA. The noise figure remains constant over the digital gain range.
(2) After HD2 trim on specific printed circuit board.
(3) From DSA = 3dB down to 0dB, NSD increases 1dB per DSA dB
(4) NF increase 1dB per DSA 1dB above DSA = 3dB

6.6 PLL/VCO/Clock Electrical Characteristics

Typical values at TA = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; Reference clock input frequency 491.52MHz (unless otherwise noted), phase noise normalized to f_{VCO}.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{VCO1}	VCO1 min frequency				7.2	GHz
	VCO1 max frequency		7.68			GHz
f_{VCO2}	VCO2 min frequency				8.848	GHz
	VCO2 max frequency		9.216			GHz
f_{VCO3}	VCO3 min frequency				9.8304	GHz
	VCO3 max frequency		10.24			GHz
f_{VCO4}	VCO4 min frequency				11.7965	GHz
	VCO4 max frequency		12.288			GHz
DIV_{FBADC}	ADC sample rate divider from VCO rate			1, 2, 3, 4, 6 or 8		
DIV_{RXADC}	ADC sample rate divider			1, 2, 3, 4, 6 or 8		
PN_{VCO}	Closed Loop Phase Noise F_{PLL} = 11.79848 GHz F_{REF}=491.52MHz	600kHz		-113		dBc/Hz
		800kHz		-116		dBc/Hz
		1MHz		-119		dBc/Hz
		1.8MHz		-125		dBc/Hz
		5MHz		-133		dBc/Hz
		50MHz		–141		dBc/Hz
	Closed Loop Phase Noise F_{PLL}=8.84736 GHz F_{REF}=491.52MHz	600kHz		-114		dBc/Hz
		800kHz		–118		dBc/Hz
		1MHz		–120		dBc/Hz
		1.8MHz		–127		dBc/Hz
		5MHz		–135		dBc/Hz
		50MHz		–142		dBc/Hz
	Closed Loop Phase Noise F_{PLL}= 9.8403 GHz F_{REF}=491.52MHz	600kHz		–113		dBc/Hz
		800kHz		–116		dBc/Hz
		1MHz		–119		dBc/Hz
		1.8MHz		–125		dBc/Hz
		5MHz		–134		dBc/Hz
		50MHz		–140		dBc/Hz
	Closed Loop Phase Noise F_{PLL}= 7.86432GHz F_{REF}=491.52MHz	600kHz		–116		dBc/Hz
		800kHz		–119		dBc/Hz
		1MHz		–122		dBc/Hz
		1.8MHz		–127		dBc/Hz
		5MHz		–136		dBc/Hz
		50MHz		–143		dBc/Hz
F_{rms}	Clock PLL integrated phase error(1)	f_{PLL}=11.79848 GHz, [1KHz, 100MHz]		-43.4		dBc/Hz
		f_{PLL}=8.8536 GHz, [1KHz, 100MHz]		-47.6		dBc/Hz
		f_{PLL}=9.8304 GHz, [1KHz, 100MHz]		-46.2		dBc/Hz
f_{PFD}	PFD frequency		100		500	MHz
PN_{pll_flat}	Normalized PLL flat Noise	f_{VCO} = 11796.48MHz		–226.5		dBc/Hz
F_{REF}	Input Clock frequency		0.1		12	GHz
V_{SS}	Input Clock level		0.6		1.8	Vppdiff

6.6 PLL/VCO/Clock Electrical Characteristics (continued)

Typical values at TA = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; Reference clock input frequency 491.52MHz (unless otherwise noted), phase noise normalized to f_{VCO}.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Coupling				AC Coupling Only		
	REFCLK input impedance(2)	Parallel resistance		100		Ω
		Parallel capacitance		0.5		pF

(1) Single Sideband, not including the reference clock contribution
(2) Refer to S11 data available from TI for impedance vs frequency

6.7 Digital Electrical Characteristics

Typical values at TA = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CML SerDes Outputs [8:1]STX+/-						
F_{SerDes}	SerDes Bit Rate	Full rate mode	19		29.5	Gbps
		Half rate mode	9.5		16.25	
		Quarter rate mode	4.75		8.125	
		1/8th rate mode	2.375		4.062	
		1/16th rate mode	1.1875		2.031	
TJ	Total Jitter Tolerance				0.42	UI
V_{STDIFF}	SerDes Transmitter Output Amplitude	differential	500		1000	mVpp
V_{STCOM}	SerDes Output Common Mode		0.4	0.45	0.55	V
Z_{STdiff}	SerDes Output Impedance			100		Ω
TRF	Output rise and fall time	20-80%	8			ps
TTJ	Output total jitter				0.21	UI
CMOS I/O: GPIO{B/C/D/E}x, SPICLK, SPISDIO, SPISDO, SPISEN, RESETZ, BISTB0, BISTB1						
V_{IH}	High-Level Input Voltage		0.6×VDD1 P8GPIO			V
V_{IL}	Low-Level Input Voltage				0.4×VDD1 P8GPIO	V
I_{IH}	High-Level Input Current		–250		250	µA
I_{IL}	Low-Level Input Current		–250		250	µA
C_L	CMOS input capacitance			2		pF
V_{OH}	High-Level Output Voltage		VDD1P8G PIO–0.2			V
V_{OL}	Low-Level Output Voltage				0.2	V
Differential Inputs: SYSREF+/- Mode A						
$F_{SYSREFMAX}$	SYSREF Input Frequency Maximum			40		MHz
$V_{SWINGSRMAX}$	SYSREF Input Swing Maximum			1.8		Vppdiff(2)
$V_{SWINGSRMIN}$	SYSREF Input Swing Minimum	f_{REF} < 500MHz		0.3		Vppdiff(2)
$V_{SWINGSRMIN}$	SYSREF Input Swing Minimum	f_{REF} > 500MHz		0.6		Vppdiff(2)
$V_{COMSRMAX}$	SYSREF Input Common Mode Voltage Maximum			0.8		V
$V_{COMSRMIN}$	SYSREF Input Common Mode Voltage Minimum			0.6		V
Z_T	Input termination	differential		100 (1)		Ω
C_L	Input capacitance	Each pin to GND		0.5		pF
LVDS Inputs: 0SYNCIN+/- and 1SYNCIN+/-						
V_{ICOM}	Input Common Voltage			1.2		V
V_{ID}	Differential Input Voltage swing			450		Vppdiff(2)
Z_T	Input termination	differential		100		Ω
LVDS Outputs: 0SYNCOUT+/- and 1SYNCOUT+/-						
V_{OCOM}	Output Common Voltage			1.2		V
V_{OD}	Differential Output Voltage swing			500		Vppdiff(2)
Z_T	Internal Termination			100		Ω

(1) SYSREF termination is programmable between 100Ω, 150Ω and 300Ω
(2) Vppdiff is the difference between the maximum differential voltage (positive value) and minimum differential voltage (negative value).

6.8 Power Supply Electrical Characteristics

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; f_{ADC} = 2949.12MSPS; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 1: 4R, f_{ADC} = 3 GSPS, DDC_{RX} = 6x Decimation, f_{RX} = 1.85 GHz, 8b/10b coding, 20 Gbps, RX: 4-8-4-1		673		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			376		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			17.5		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			557		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			75		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			68		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			1582		mA
P_{diss}	Power Dissipation			4208		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 2: 4R2F, f_{ADC} = 3 GSPS, DDC_{FB} = DDC_{RX} = 6x Decimation, f_{RX} = 1.85 GHz, 8b/10b coding, 20 Gbps, RX: 4-8-4-1, FB: 2-4-4-1		1006		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			548		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			17.5		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			839		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			92		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			68		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			2174		mA
P_{diss}	Power Dissipation			5996		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 4: 4R, f_{ADC} = 3 GSPS, DDC_{RX} = 2x Decimation , f_{RX} = 2.25 GHz, 64/66 coding, 24.75 Gbps, RX: 8-8-2-1		672		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			506		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			17.5		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			552		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			76		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			68		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			1613		mA
P_{diss}	Power Dissipation			4468		mW

6.8 Power Supply Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; f_{ADC} = 2949.12MSPS; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 5: 4R2F, f_{ADC} = 3 GSPS, DDC_{RX} = 12x Decimation Dual Channel, DDC_{FB} = 3x Decimation, f_{RX} = 1.85 and 2.65 GHz, 8b/10b coding, 20 Gbps, RX: 4-16-8-1, FB: 4-4-4-1		1005		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			562		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			17.5		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			837		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			92		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			68		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			2359		mA
P_{diss}	Power Dissipation			6195		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 6: 4R, f_{ADC} = 3 GSPS, DDC_{RX} = 12x Decimation Dual Channel, f_{RX} = 1.85 and 2.65 GHz, 8b/10b coding, 20 Gbps, RX: 4-16-8-1		671		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			374		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			17.5		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			555		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			75		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			67		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			1702		mA
P_{diss}	Power Dissipation			4305		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 7: same configuration as mode 2, Sleep Mode. SLEEP pin is pull high.		16		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			295		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			12		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			4		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			24		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			45		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			156		mA
P_{diss}	Power Dissipation			818		mW

6.9 Timing Requirements

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; f_{ADC} = 2949.12MSPS; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

		MIN	NOM	MAX	UNIT
Timing: SYSREF+/-					
$t_{s(SYSREF)}$	Setup Time, SYSREF+/- Valid to Rising Edge of CLK+/-		50		ps
$t_{h(SYSREF)}$	Hold Time, SYSREF+/- Valid after Rising Edge of CLK+/-		50		ps
Timing: Serial ports					
$t_{s(SENB)}$	Setup Time, SENB to Rising Edge of SCLK		15		ns
$t_{h(SENB)}$	Hold Time, SENB after last Rising Edge of SCLK (1)		5 + t_{SCLK}		ns
$t_{s(SDIO)}$	Setup Time, SDIO valid to Rising Edge of SCLK		15		ns
$t_{h(SDIO)}$	Hold Time, SDIO valid after Rising Edge of SCLK		5		ns
$t_{(SCLK)\_W}$	Minimum SCLK period: registers write		25		ns
$t_{(SCLK)\_R}$	Minimum SCLK period: registers read		50		ns
$t_{d(data\_out)}$	Minimum Data Output delay after Falling Edge of SCLK		0		ns
	Maximum Data Output delay after Falling Edge of SCLK		15		ns
t_{RESET}	Minimum RESETZ Pulse Width		1		ms

(1) SDEN\\ need to be held one more extra clock cycle with the last SCLK edge

6.10 Switching Characteristics

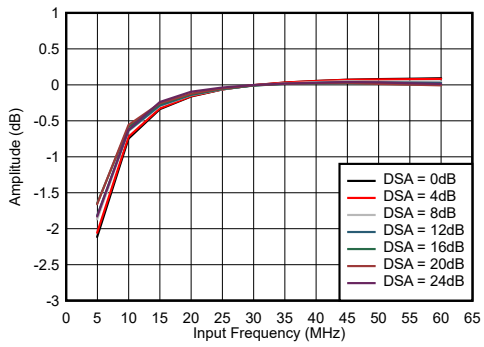
Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; f_{ADC} = 2949.12MSPS; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RX Channel Latency						
t_{JESDRX}	RX input to JESD output Latency	LMFS=2-16-16-1, 122.88 MSPS, 24x Decimation, Serdes rate = 16.22Gbps (JESD204C)		92		interface clock cycles(1)
		LMFS=4-16-8-1, 245.76 MSPS, 12x Decimation, Serdes rate = 16.22Gbps (JESD204C)		108		
		LMFS=2-8-8-1, 368.64 MSPS, 8x Decimation, Serdes rate = 16.22Gbps (JESD204C)		118		
		LMFS=4-8-4-1, 491.52 MSPS, 6x Decimation, Serdes rate = 16.22Gbps (JESD204C)		153		
FB Channel Latency						
	SerDes Transmitter Analog Delay			3.6		ns
t_{JESDFB}	FB input to JESD output Latency	LMFS=1-2-8-1, 368.64 MSPS, 8x Decimation		151		interface clock cycles(1)
		LMFS=2-4-4-1, 491.52 MSPS, 6x Decimation		177		

(1) Interface clock cycles is the period of the digital interface clock rate, e.g. 1GSPS = 1ns.

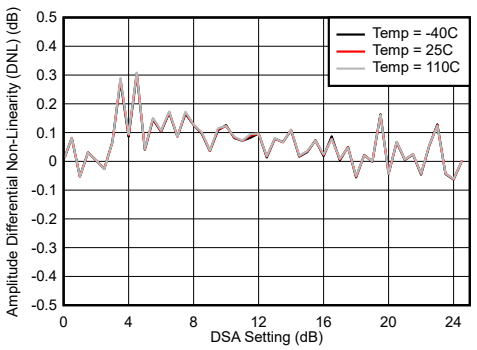
6.11.1 RX Typical Characteristics 30 MHz and 400 MHz

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB.



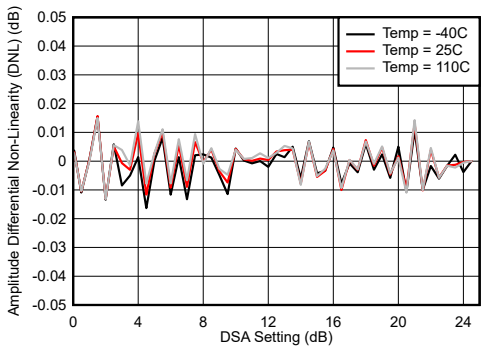
Normalized to 30 MHz

図 6-1. RX In-Band Gain Flatness, f_{IN} = 30 MHz



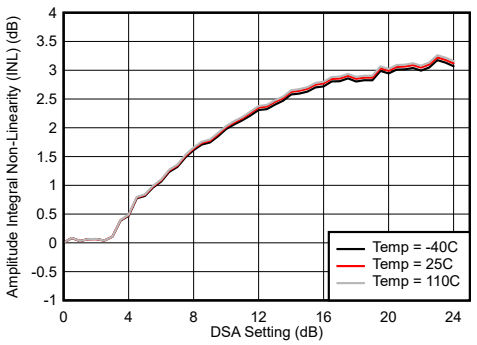
Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

図 6-2. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 30 MHz



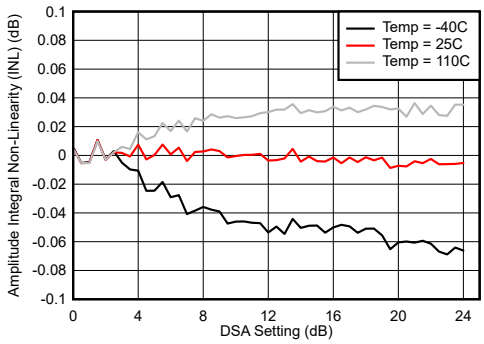
Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

図 6-3. RX Calibrated Differential Amplitude Error vs DSA Setting at 30 MHz



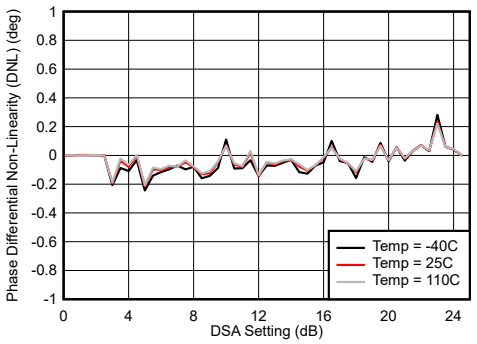
Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

図 6-4. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 30 MHz



Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

図 6-5. RX Calibrated Integrated Amplitude Error vs DSA Setting at 30 MHz

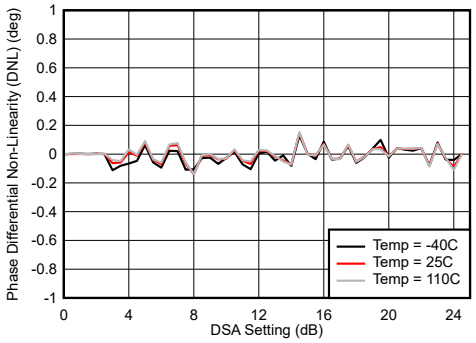


Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

図 6-6. RX Uncalibrated Differential Phase Error vs DSA Setting at 30 MHz

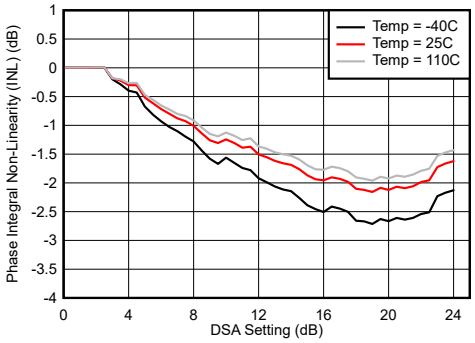
6.11.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB.



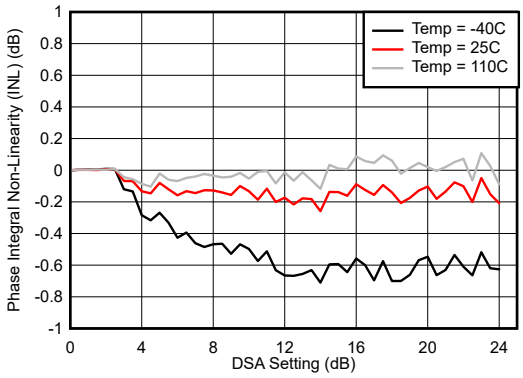
Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

図 6-7. RX Calibrated Differential Phase Error vs DSA Setting at 30 MHz



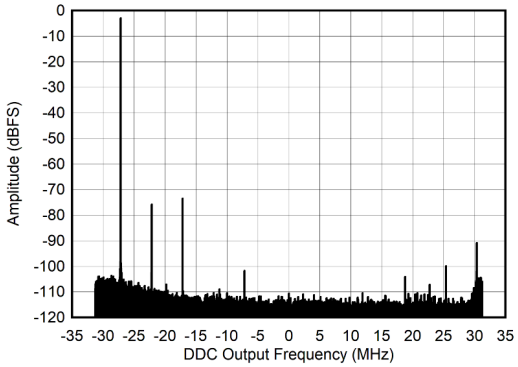
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 6-8. RX Uncalibrated Integrated Phase Error vs DSA Setting at 30 MHz



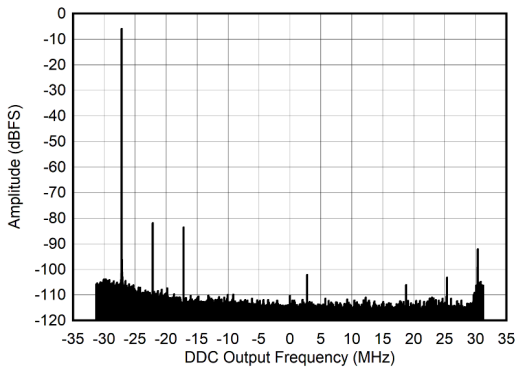
With 0.8 GHz matching
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 6-9. RX Calibrated Integrated Phase Error vs DSA Setting at 30 MHz



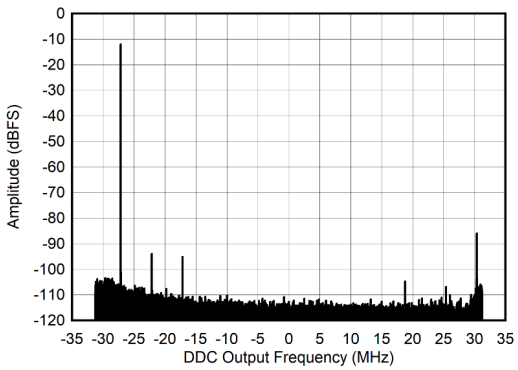
A_{IN} = -3 dBFS, f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 6-10. RX Output FFT at 5 MHz



A_{IN} = -6 dBFS, f_{ADC} = 1500 MSPS, f_{NCO} = 32. , Decimate by 24x

図 6-11. RX Output FFT at 5 MHz

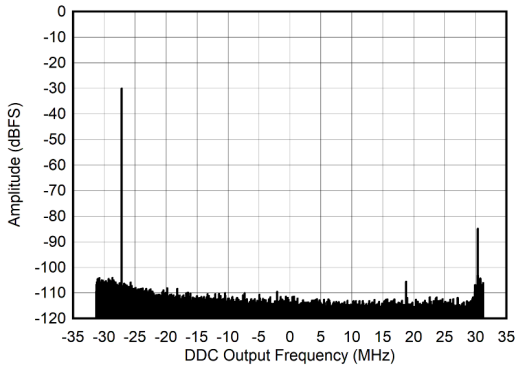


A_{IN} = -12 dBFS, f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 6-12. RX Output FFT at 5 MHz

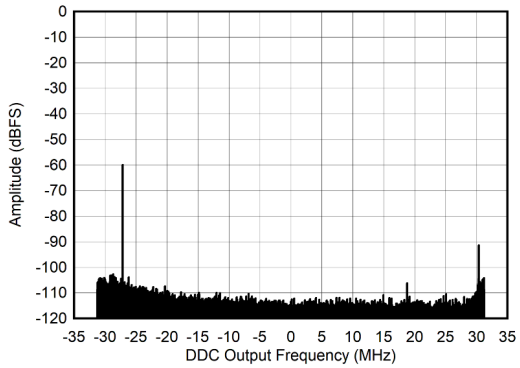
6.11.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB.



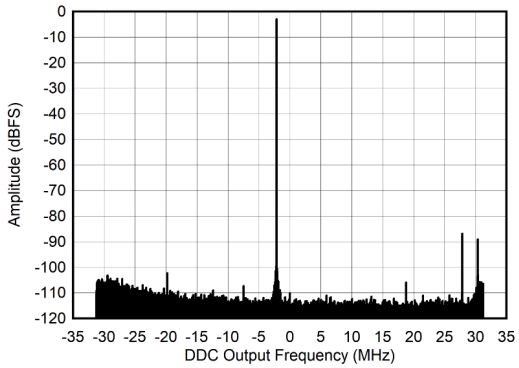
A_{IN} = -30 dBFS, f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 6-13. RX Output FFT at 5 MHz



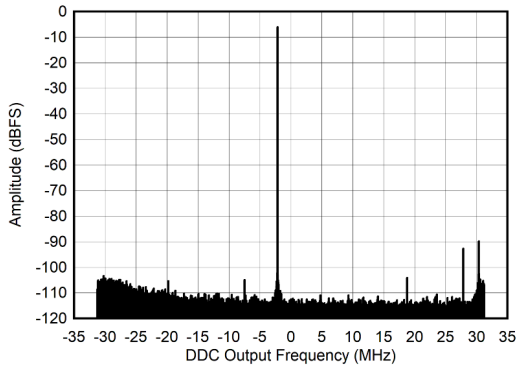
A_{IN} = -60 dBFS, f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 6-14. RX Output FFT at 5 MHz



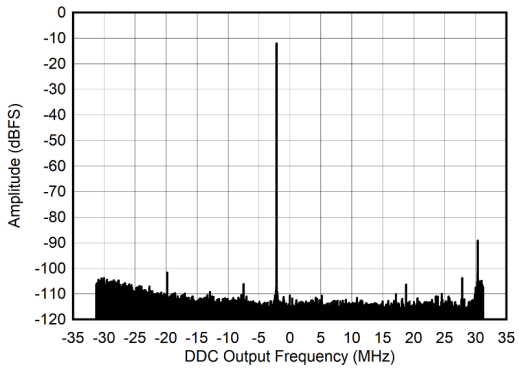
A_{IN} = -3 dBFS, f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 6-15. RX Output FFT at 30 MHz



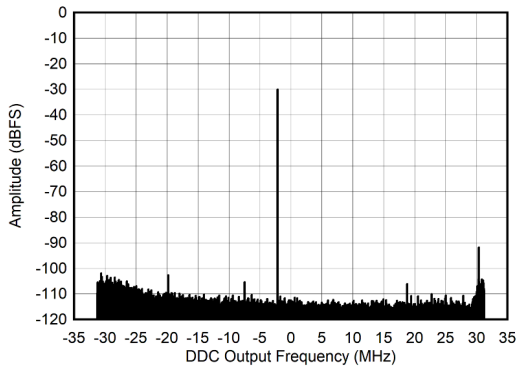
A_{IN} = -6 dBFS, f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 6-16. RX Output FFT at 30 MHz



A_{IN} = -12 dBFS, f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 6-17. RX Output FFT at 30 MHz

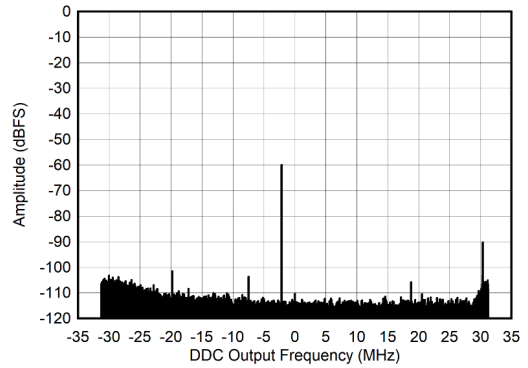


A_{IN} = -30 dBFS, f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 6-18. RX Output FFT at 30 MHz

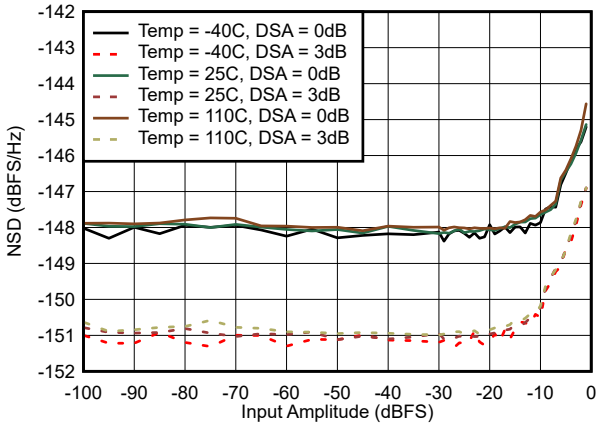
6.11.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB.



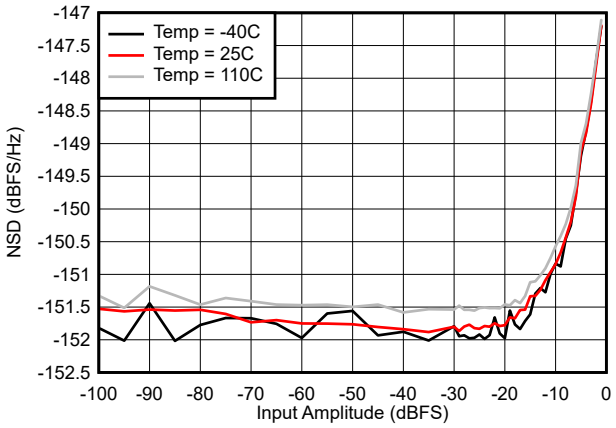
A_{IN} = -60 dBFS, f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 6-19. RX Output FFT at 30 MHz



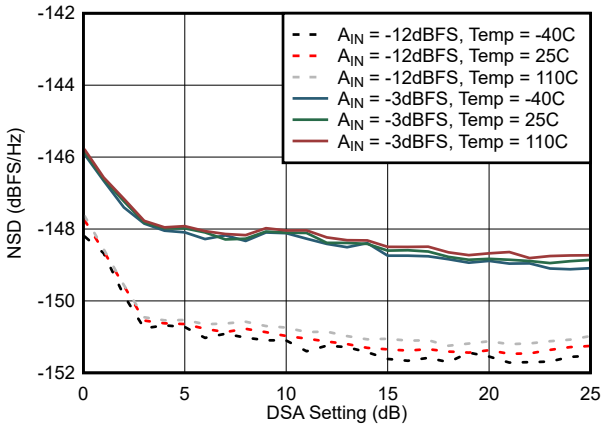
f_{ADC} = 1500MSPS, f_{NCO} = 32.13MHz, Decimate by 24x

図 6-20. NSD vs Input Amplitude at 30 MHz with DSA = 0 and 3dB



f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 6-21. NSD vs Input Amplitude at 30 MHz with DSA = 12

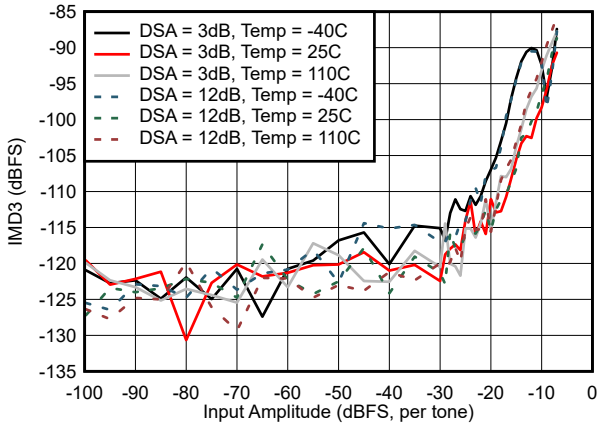


f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 6-22. NSD vs DSA Attenuation at 30 MHz

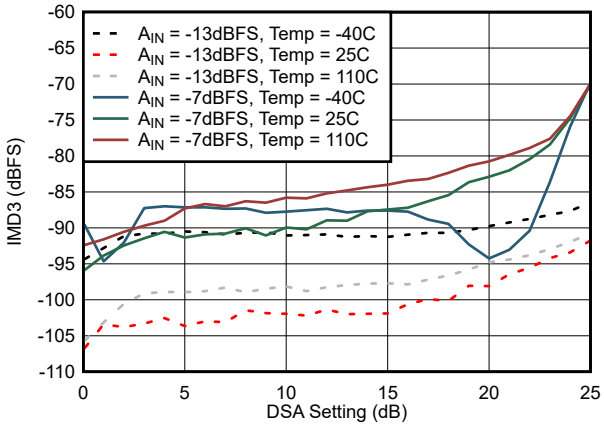
6.11.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB.



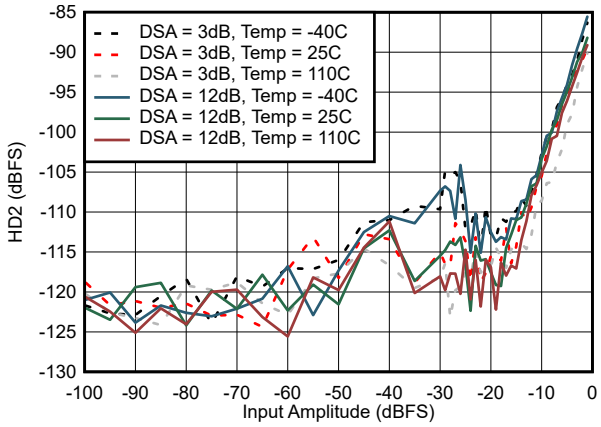
f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 6-23. IMD3 vs Input Amplitude at 30 MHz



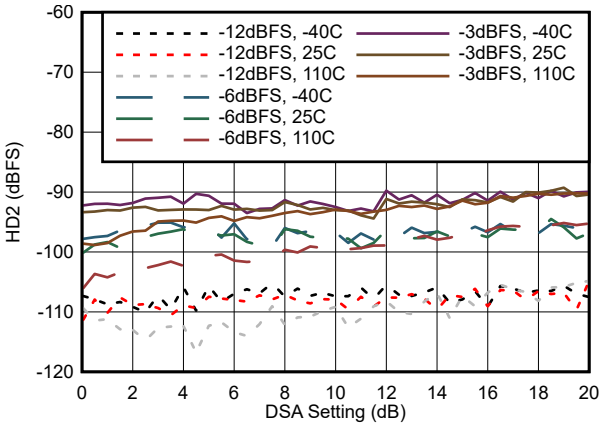
f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 6-24. IMD3 vs DSA Setting at 30 MHz



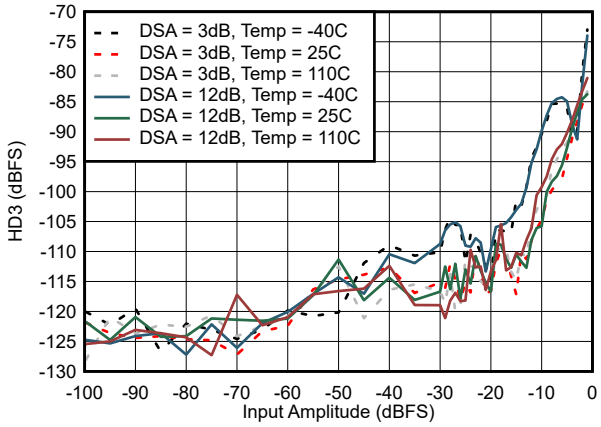
f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 6-25. HD2 vs Input Amplitude at 30 MHz



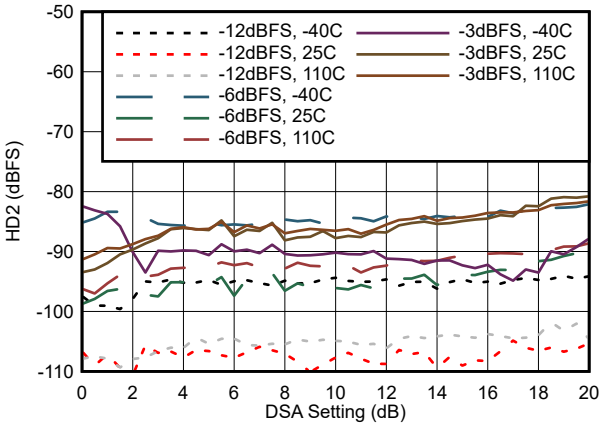
f_{ADC} = 1500 MSPS, f_{NCO} = 32. , Decimate by 24x

図 6-26. HD2 vs DSA Setting at 30 MHz



f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 6-27. HD3 vs Input Amplitude at 30 MHz

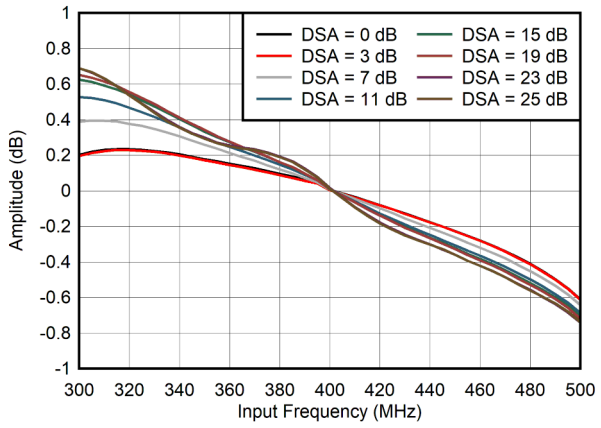


f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 6-28. HD3 vs DSA Setting at 30 MHz

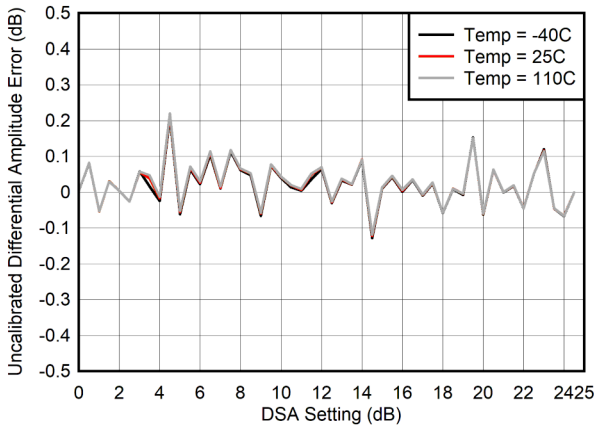
6.11.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB.



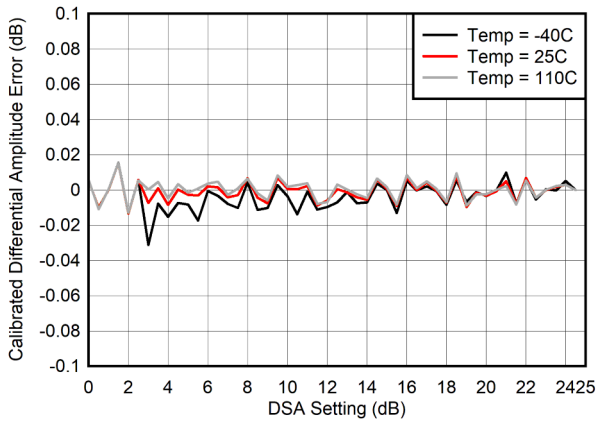
Normalized to 4000 MHz

図 6-29. RX In-Band Gain Flatness, f_{IN} = 400 MHz



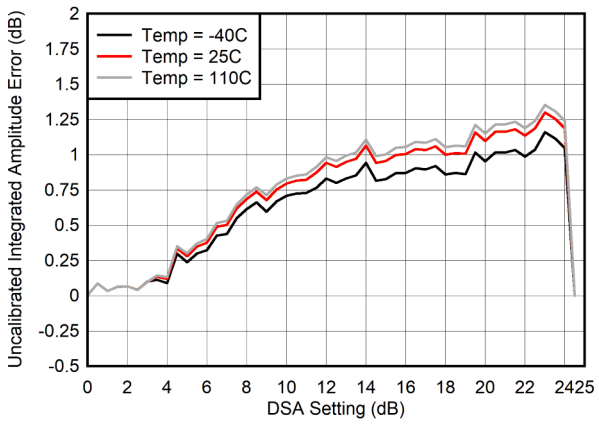
Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

図 6-30. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 30 MHz



Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

図 6-31. RX Calibrated Differential Amplitude Error vs DSA Setting at 400 MHz

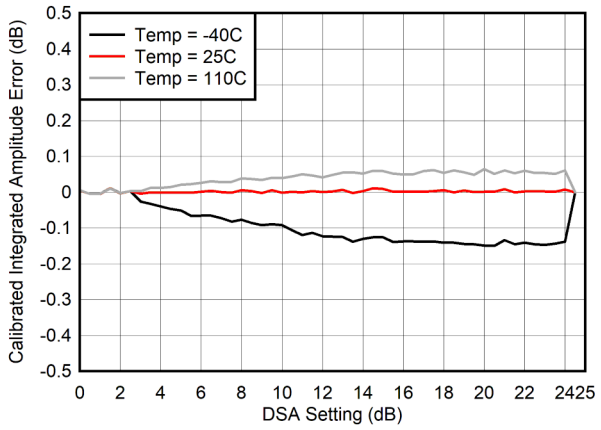


Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

図 6-32. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 400 MHz

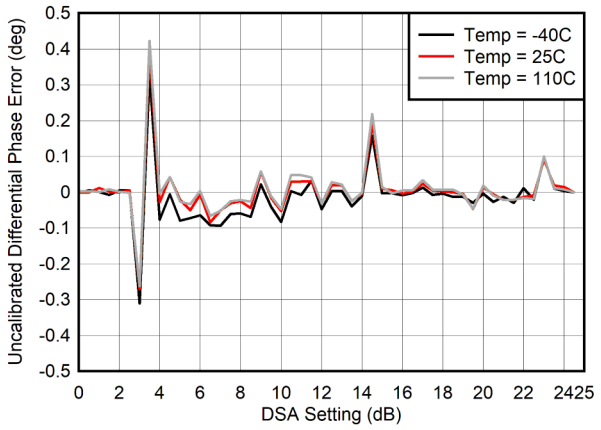
6.11.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB.



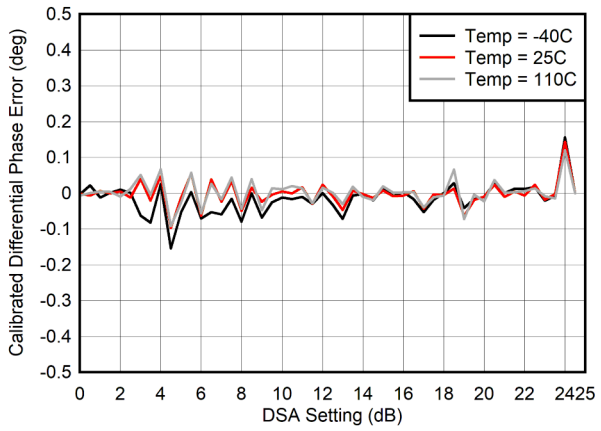
Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

図 6-33. RX Calibrated Integrated Amplitude Error vs DSA Setting at 400 MHz



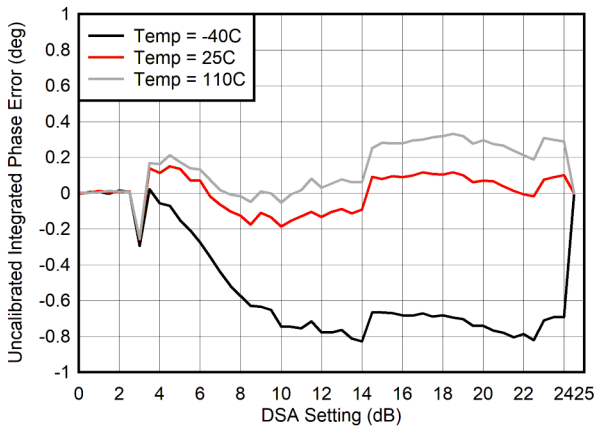
Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

図 6-34. RX Uncalibrated Differential Phase Error vs DSA Setting at 400 MHz



Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

図 6-35. RX Calibrated Differential Phase Error vs DSA Setting at 400 MHz

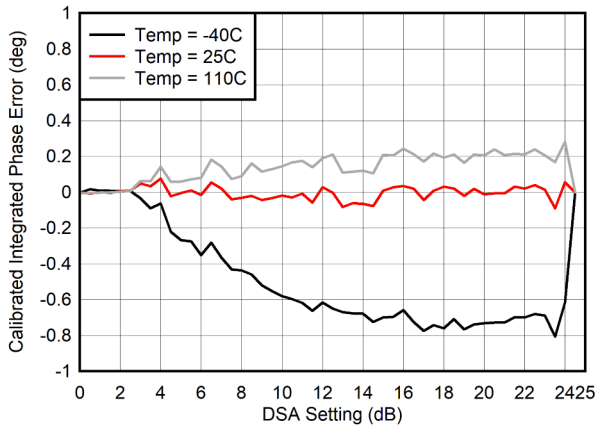


Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 6-36. RX Uncalibrated Integrated Phase Error vs DSA Setting at 400 MHz

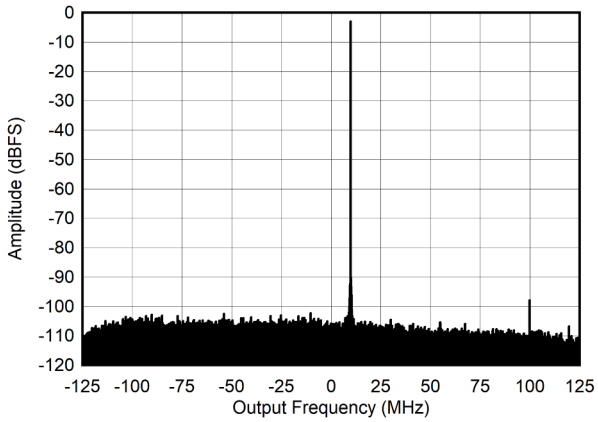
6.11.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB.



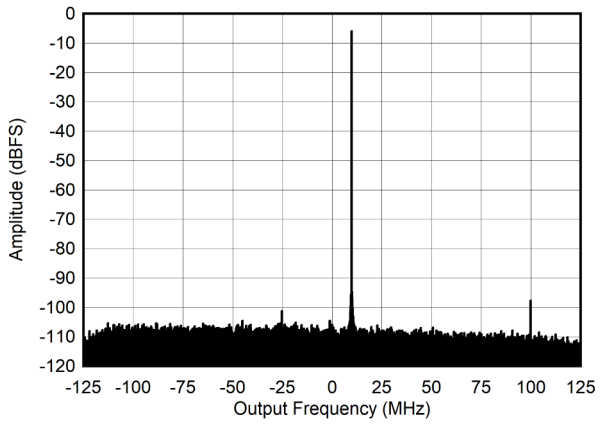
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 6-37. RX Calibrated Integrated Phase Error vs DSA Setting at 400 MHz



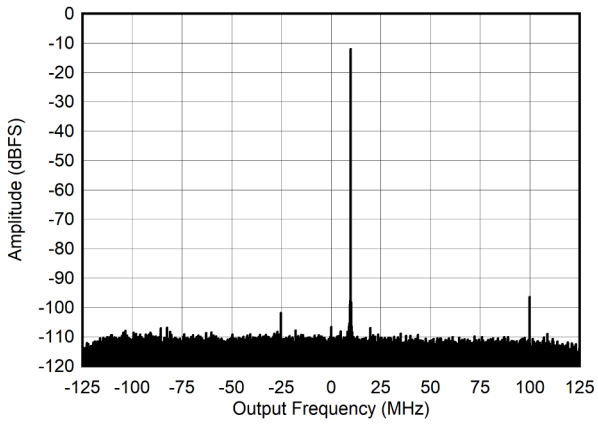
f_{NCO} = 400MHz

図 6-38. RX Output FFT at 405 MHz and -3dBFS



f_{NCO} = 400MHz

図 6-39. RX Output FFT at 405 MHz and -6dBFS

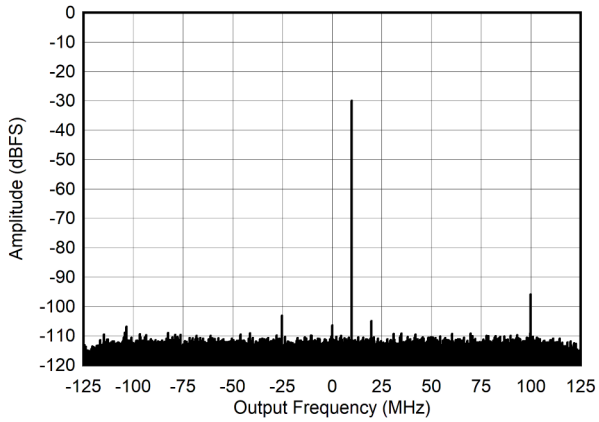


f_{NCO} = 400MHz

図 6-40. RX Output FFT at 405 MHz and -12dBFS

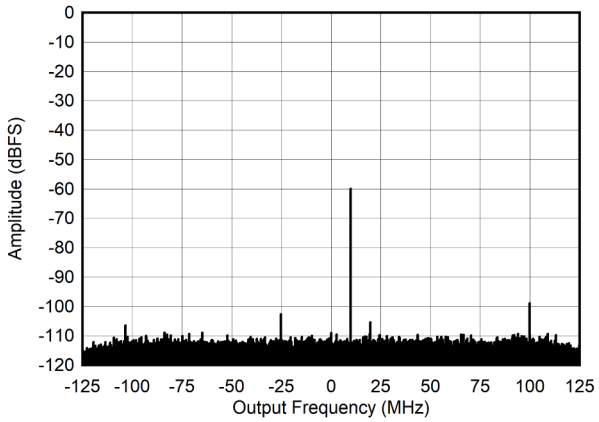
6.11.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB.



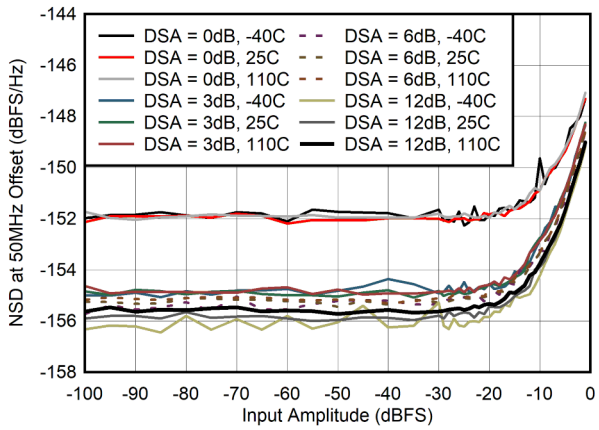
f_{NCO} = 400MHz

図 6-41. RX Output FFT at 405 MHz and -30dBFS



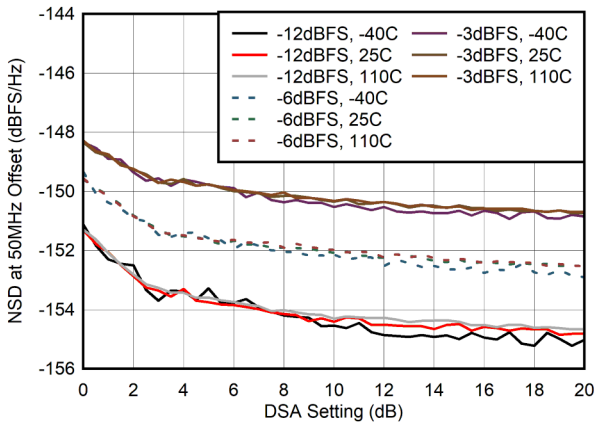
f_{NCO} = 400MHz

図 6-42. RX Output FFT at 405 MHz and -60dBFS



f_{OFFSET} = 50MHz

図 6-43. NSD vs Input Amplitude at 400MHz



f_{OFFSET} = 50MHz

図 6-44. NSD vs DSA Setting at 400MHz

6.11.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB.

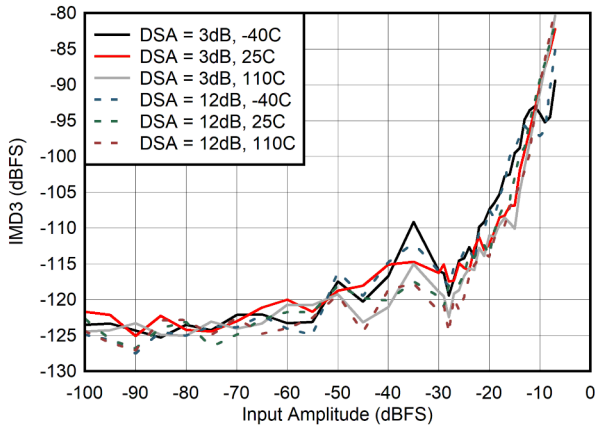


図 6-45. IMD3 vs Input Amplitude at 400MHz

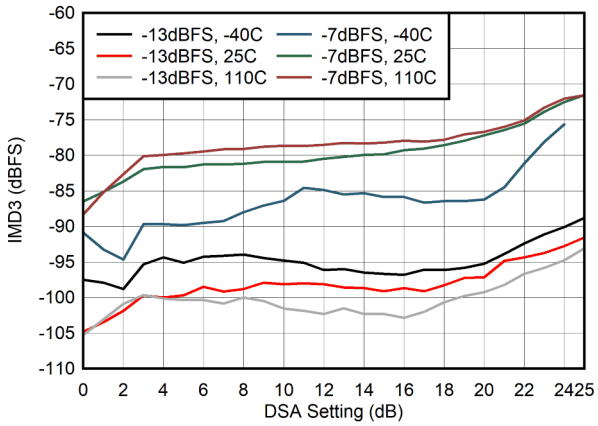


図 6-46. IMD3 vs DSA Setting at 400MHz

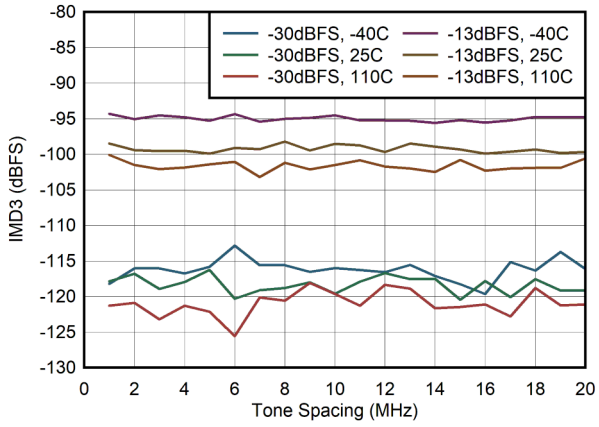


図 6-47. IMD3 vs Tone Spacing at 400MHz

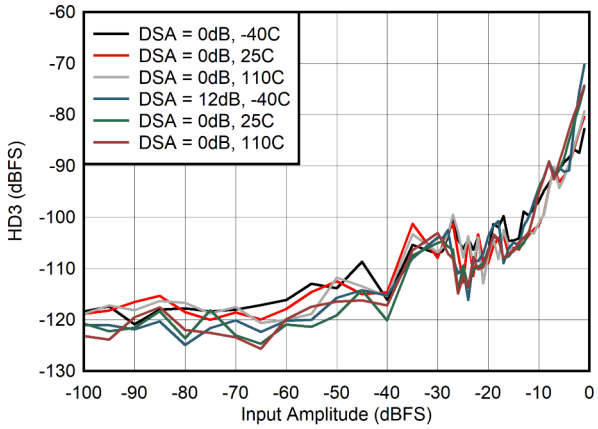


図 6-48. HD3 vs Input Amplitude at 400MHz

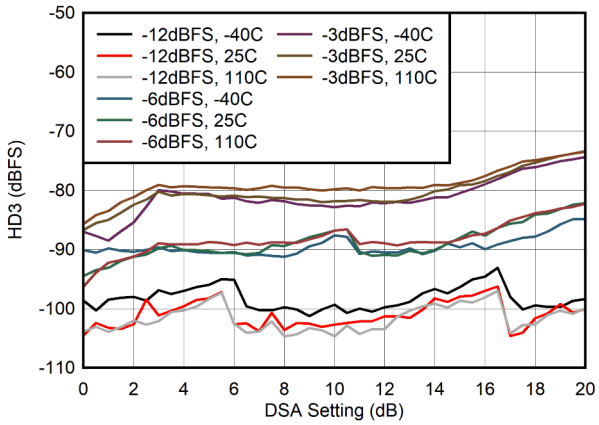
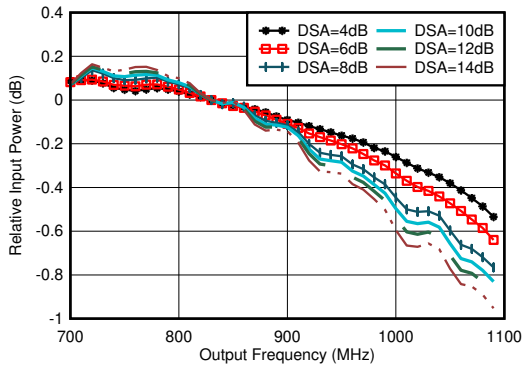


図 6-49. HD3 vs DSA Setting at 400MHz

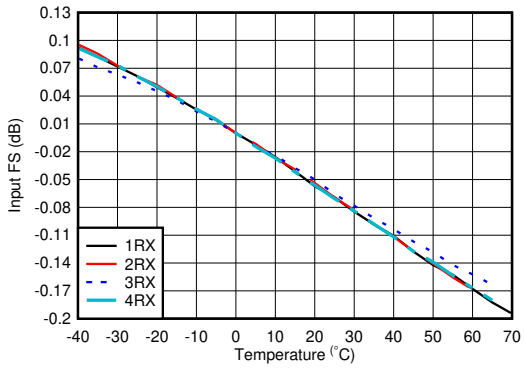
6.11.2 RX Typical Characteristics at 800MHz

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



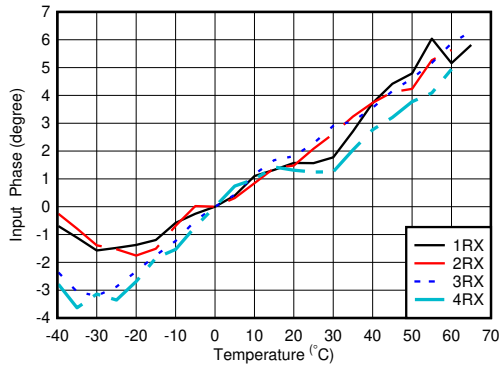
With 0.8 GHz matching, normalized to 830 MHz

図 6-50. RX In-Band Gain Flatness for Channel 1RX, f_{IN} = 830 MHz



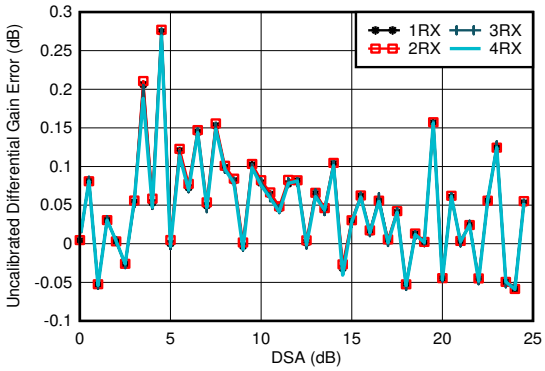
With 0.8 GHz matching, normalized to fullscale at 25°C for each channel

図 6-51. RX Input Fullscale vs Temperature and Channel at 800MHz



With 0.8 GHz matching, normalized to phase at 25°C

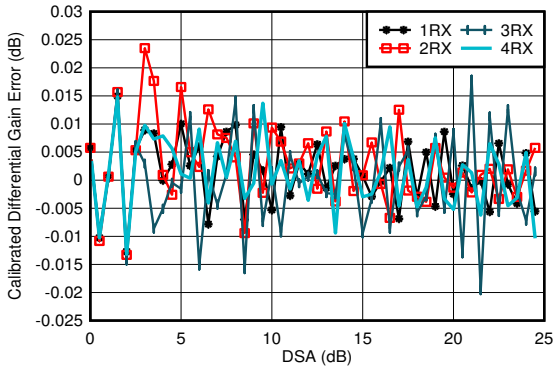
図 6-52. RX Input Phase vs Temperature and DSA at f_{OUT} = 0.8 GHz



With 0.8 GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

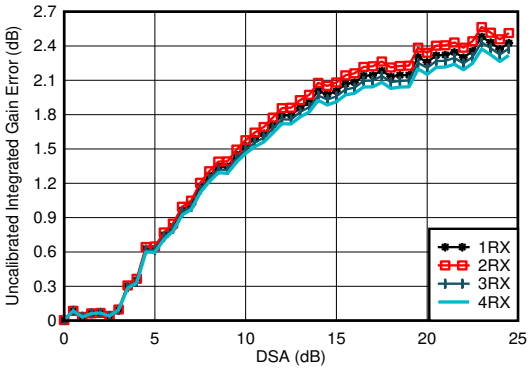
図 6-53. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 0.8 GHz



With 0.8 GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

図 6-54. RX Calibrated Differential Amplitude Error vs DSA Setting at 0.8 GHz



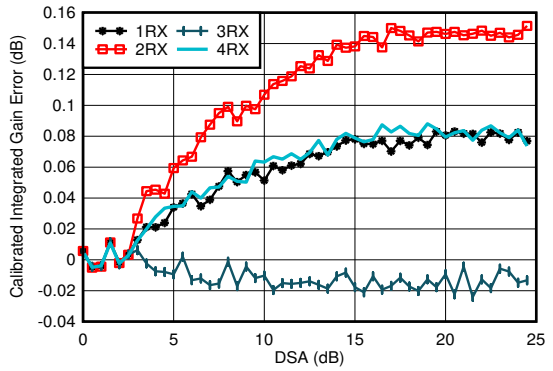
With 0.8 GHz matching

Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

図 6-55. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 0.8 GHz

6.11.2 RX Typical Characteristics at 800MHz (continued)

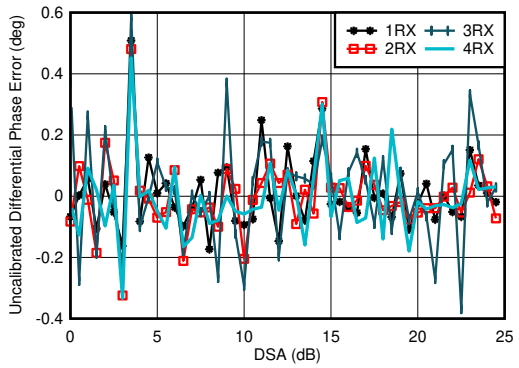
Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



With 0.8 GHz matching

Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

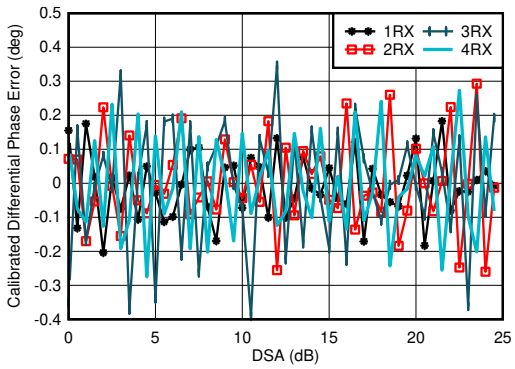
図 6-56. RX Calibrated Integrated Amplitude Error vs DSA Setting at 2.6 GHz



With 0.8 GHz matching

Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

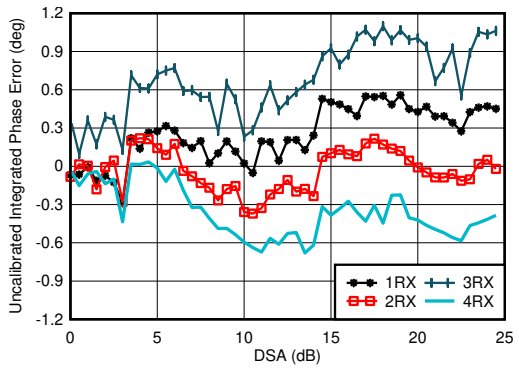
図 6-57. RX Uncalibrated Differential Phase Error vs DSA Setting at 0.8 GHz



With 0.8 GHz matching

Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

図 6-58. RX Calibrated Differential Phase Error vs DSA Setting at 0.8 GHz



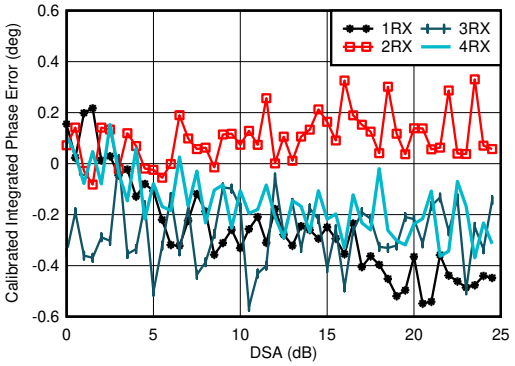
With 0.8 GHz matching

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 6-59. RX Uncalibrated Integrated Phase Error vs DSA Setting at 0.8 GHz

6.11.2 RX Typical Characteristics at 800MHz (continued)

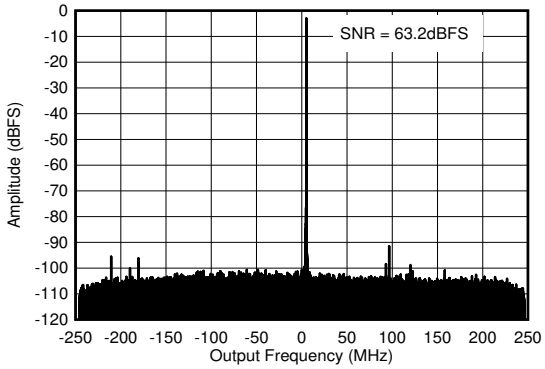
Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



With 0.8 GHz matching

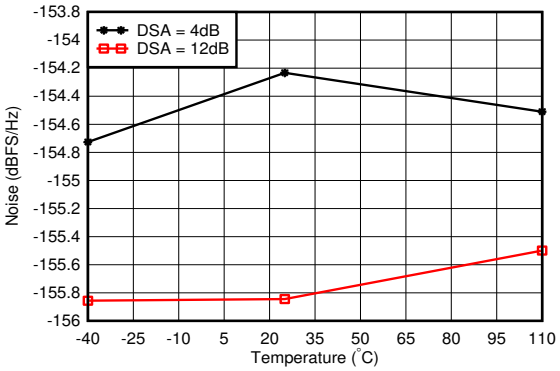
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 6-60. RX Calibrated Integrated Phase Error vs DSA Setting at 0.8 GHz



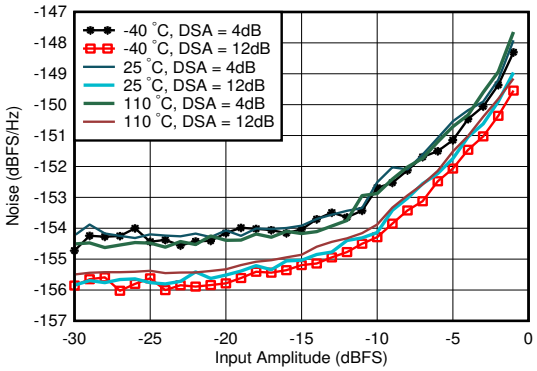
With 0.8 GHz matching, f_{IN} = 840 MHz, A_{IN}= –3 dBFS

図 6-61. RX Output FFT at 0.8 GHz



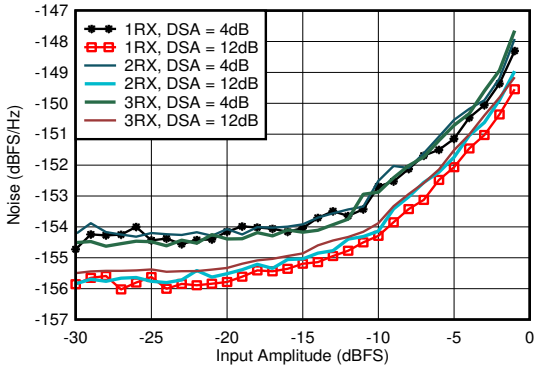
With 0.8 GHz matching, 12.5-MHz offset from tone

図 6-62. RX Noise Spectral Density vs Temperature at 0.8 GHz



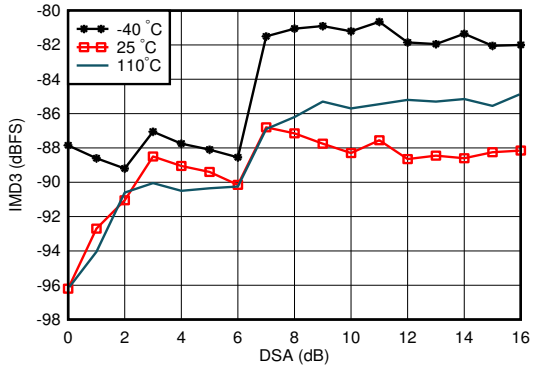
With 0.8 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

図 6-63. RX Noise Spectral Density vs Input Amplitude and Temperature at 0.8 GHz



With 0.8 GHz matching, 12.5-MHz offset from tone

図 6-64. RX Noise Spectral Density vs Input Amplitude and Channel at 0.8 GHz

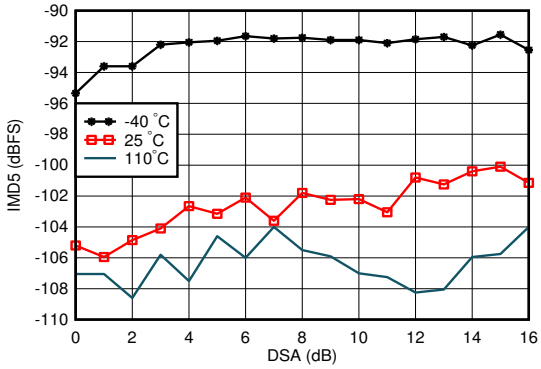


A. With 0.8 GHz matching, each tone –7 dBFS, tone spacing = 20 MHz

図 6-65. RX IMD3 vs DSA Setting and Temperature at 0.8 GHz

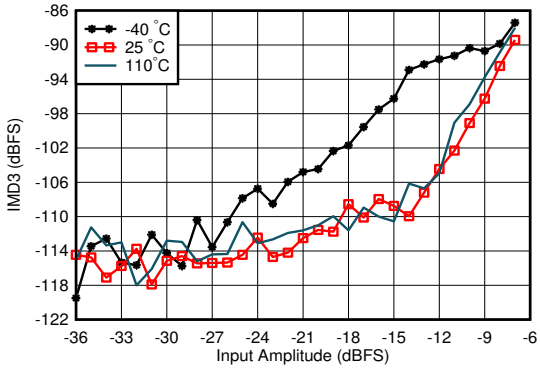
6.11.2 RX Typical Characteristics at 800MHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



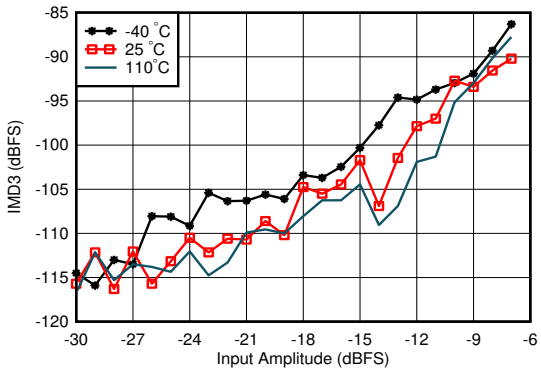
With 0.8 GHz matching, each tone –7 dBFS, tone spacing = 20 MHz

図 6-66. RX IMD5 vs DSA Setting and Temperature at 0.8 GHz



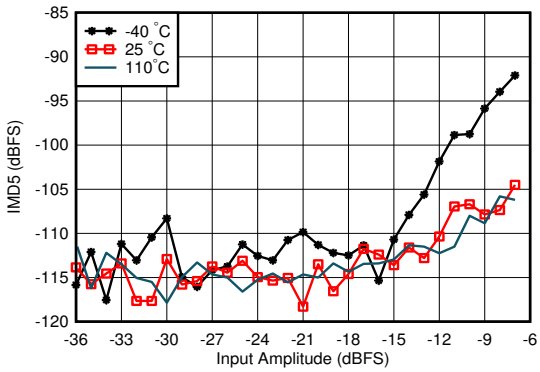
With 0.8 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

図 6-67. RX IMD3 vs Input Level and Temperature at 0.8 GHz



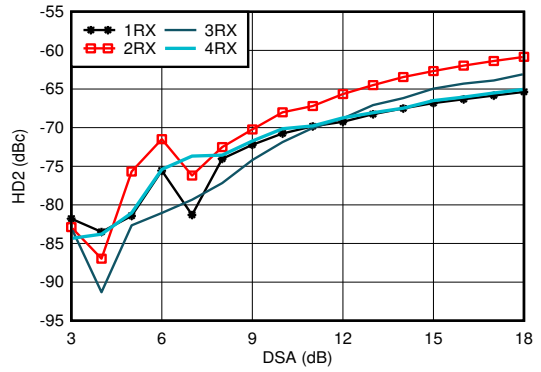
With 0.8 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

図 6-68. RX IMD3 vs Input Level and Temperature at 0.8 GHz



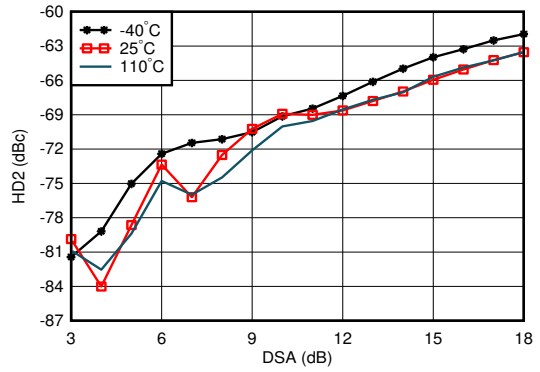
With 0.8 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

図 6-69. RX IMD5 vs Input Level and Temperature at 0.8 GHz



With 0.8 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

図 6-70. RX HD2 vs DSA Setting and Channel at 0.8 GHz

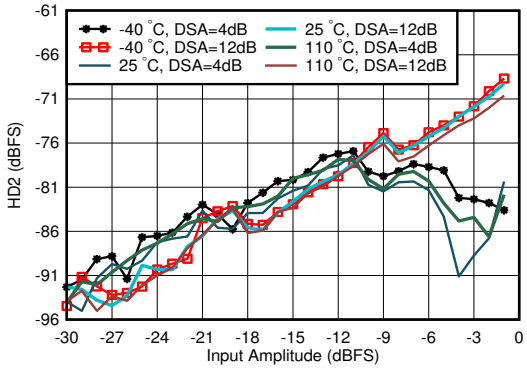


With 0.8 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

図 6-71. RX HD2 vs DSA Setting and Temperature at 0.8 GHz

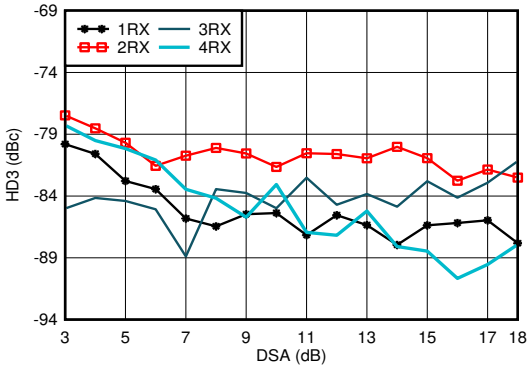
6.11.2 RX Typical Characteristics at 800MHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



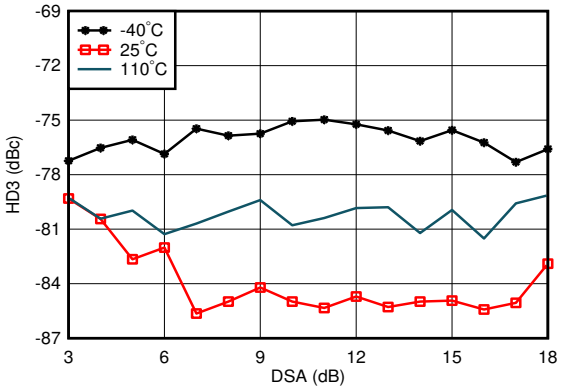
With 0.8 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

図 6-72. RX HD2 vs Input Level and Temperature at 0.8 GHz



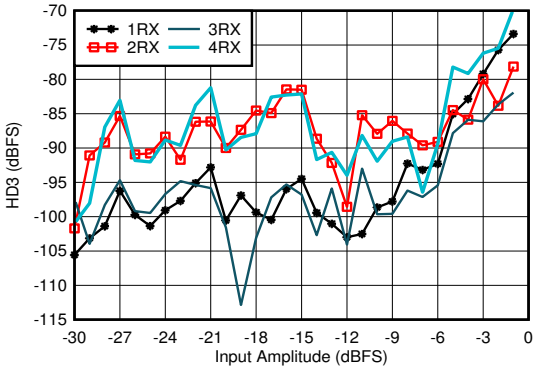
With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

図 6-73. RX HD3 vs DSA Setting and Channel at 0.8 GHz



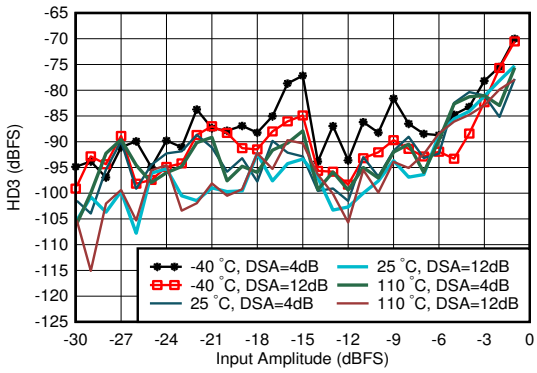
With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

図 6-74. RX HD3 vs DSA Setting and Temperature at 0.8 GHz



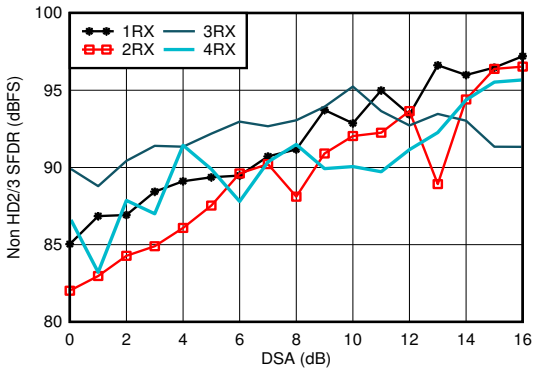
With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

図 6-75. RX HD3 vs Input Level and Channel at 0.8 GHz



With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

図 6-76. RX HD3 vs Input Level and Temperature at 0.8 GHz

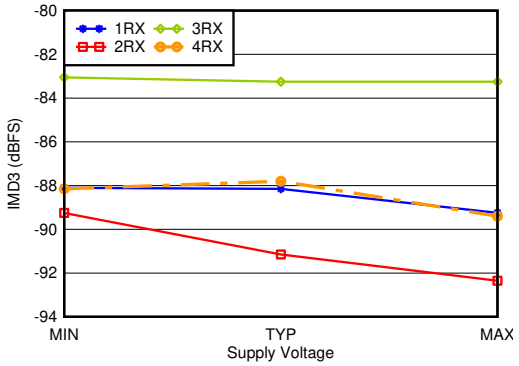


With 0.8 GHz matching

図 6-77. RX Non-HD2/3 vs DSA Setting at 0.8 GHz

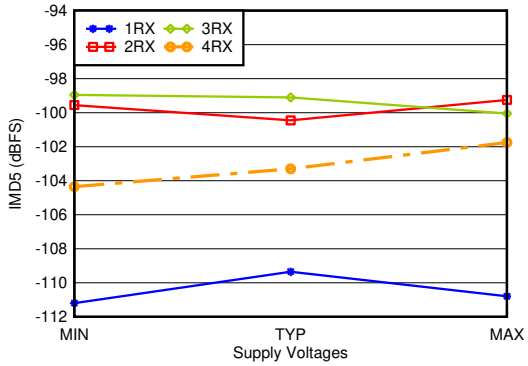
6.11.2 RX Typical Characteristics at 800MHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



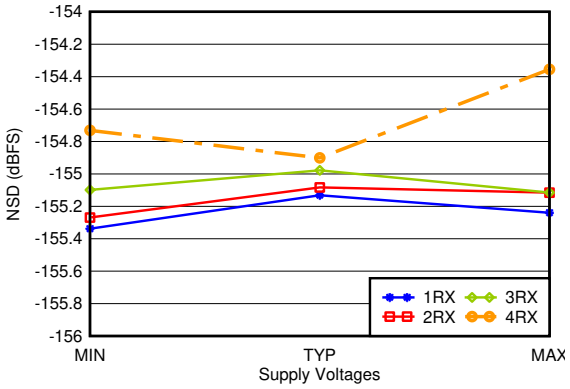
With 0.8 GHz matching, –7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

図 6-78. RX IMD3 vs Supply and Channel at 0.8 GHz



With 0.8 GHz matching, –7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

図 6-79. RX IMD5 vs Supply and Channel at 0.8 GHz

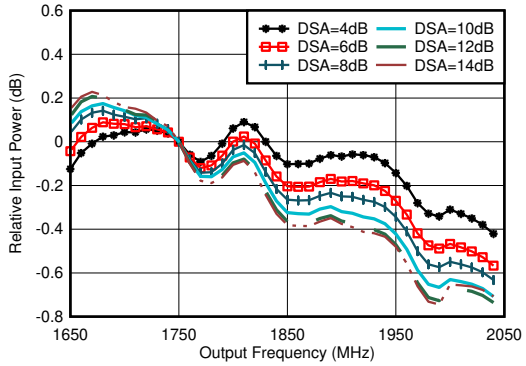


With 0.8 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

図 6-80. RX Noise Spectral Density vs Supply and Channel at 0.8 GHz

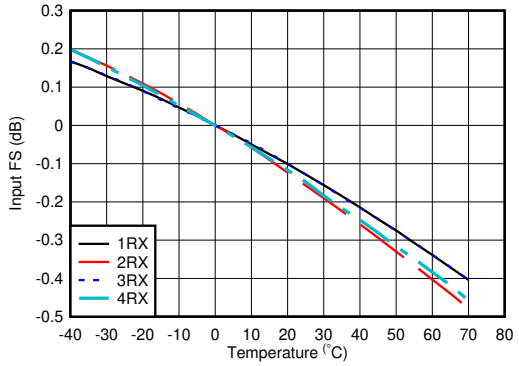
6.11.3 RX Typical Characteristics 1.75GHz to 1.9GHz

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



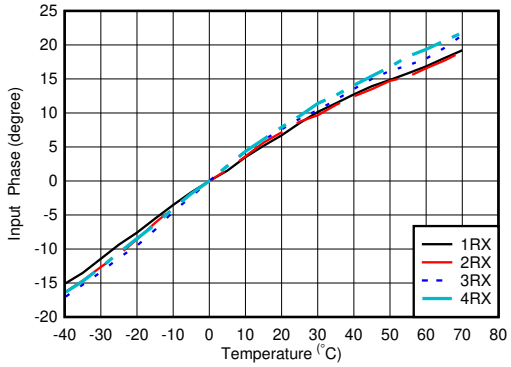
With 1.8 GHz matching, normalized to 1.75 GHz

図 6-81. RX In-Band Gain Flatness, f_{IN} = 1750 MHz



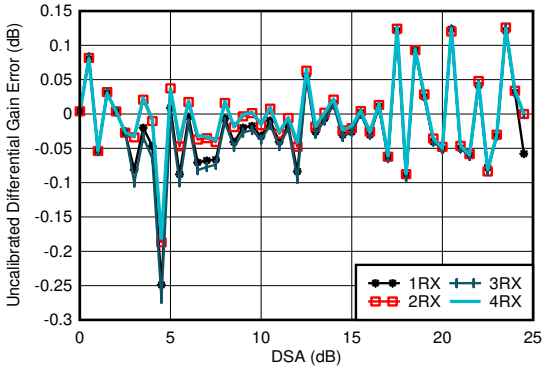
With 1.8 GHz matching, normalized to fullscale at 25°C for each channel

図 6-82. RX Input Fullscale vs Temperature and Channel at 1.75 GHz



With 2.6 GHz matching, normalized to phase at 25°C

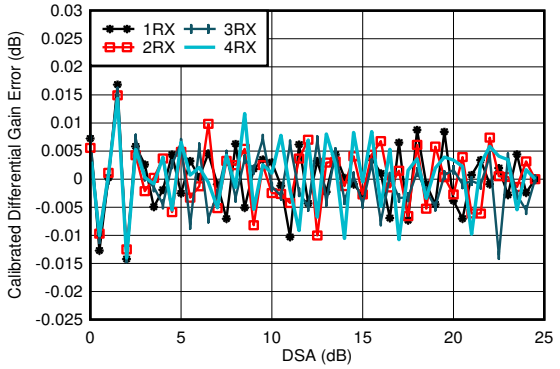
図 6-83. RX Input Phase vs Temperature and DSA at f_{IN} = 1.75 GHz



With 1.8 GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

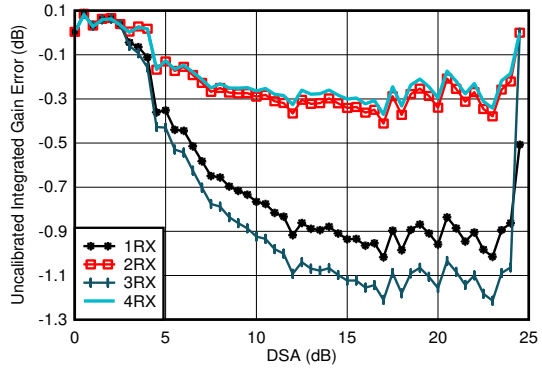
図 6-84. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 1.75 GHz



With 1.8 GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

図 6-85. RX Calibrated Differential Amplitude Error vs DSA Setting at 1.75 GHz



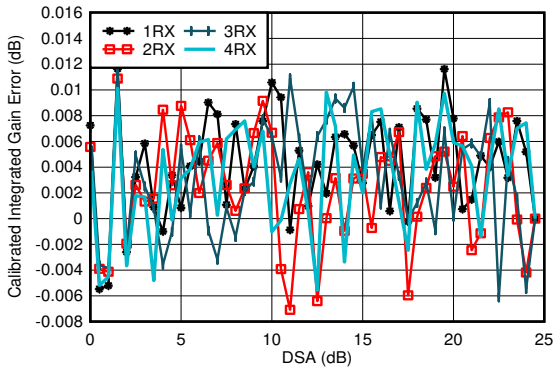
With 1.8 GHz matching

Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

図 6-86. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 1.75 GHz

6.11.3 RX Typical Characteristics 1.75GHz to 1.9GHz (continued)

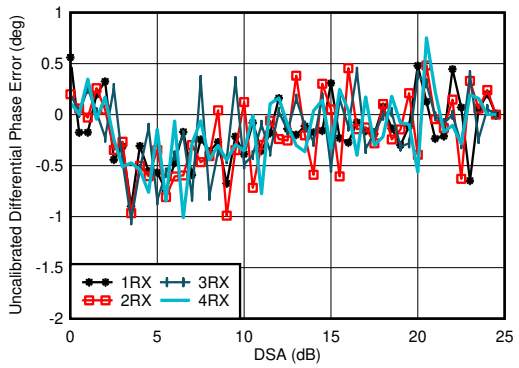
Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



With 1.8 GHz matching

Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

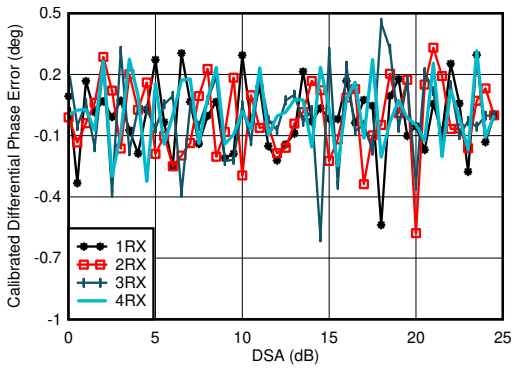
図 6-87. RX Calibrated Integrated Amplitude Error vs DSA Setting at 1.75 GHz



With 1.8 GHz matching

Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

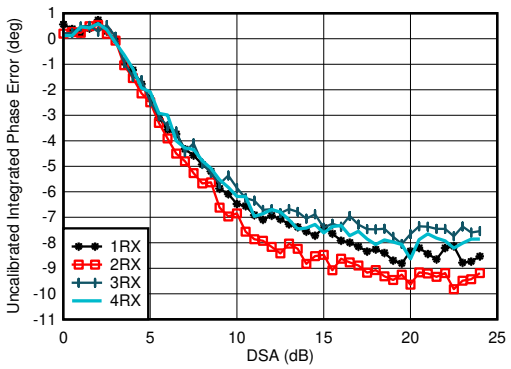
図 6-88. RX Uncalibrated Differential Phase Error vs DSA Setting at 1.75 GHz



With 1.8 GHz matching

Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

図 6-89. RX Calibrated Differential Phase Error vs DSA Setting at 1.75 GHz



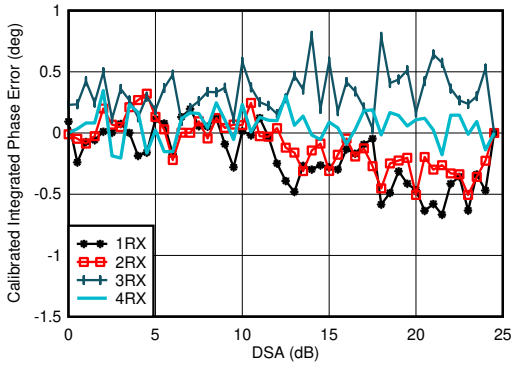
With 1.8 GHz matching

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 6-90. RX Uncalibrated Integrated Phase Error vs DSA Setting at 1.75 GHz

6.11.3 RX Typical Characteristics 1.75GHz to 1.9GHz (continued)

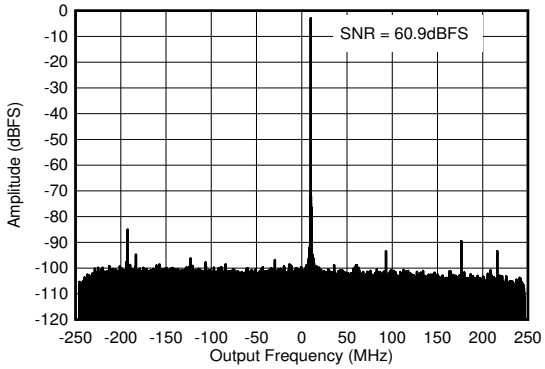
Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



With 1.8 GHz matching

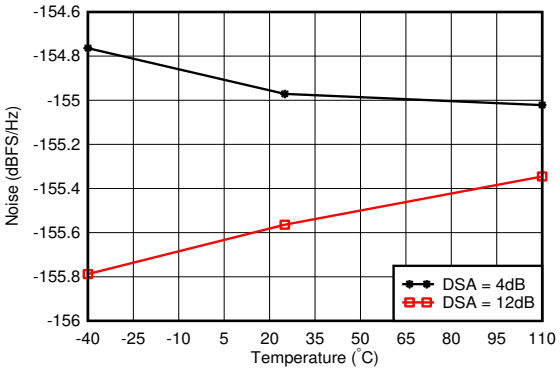
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 6-91. RX Calibrated Integrated Phase Error vs DSA Setting at 1.75 GHz



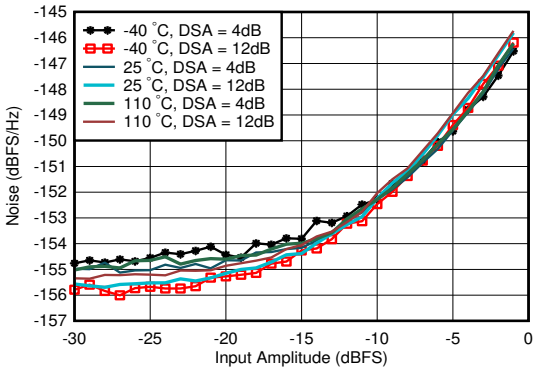
With 1.8 GHz matching, f_{IN} = 2610 MHz, A_{IN}= –3 dBFS

図 6-92. RX Output FFT at 1.75 GHz



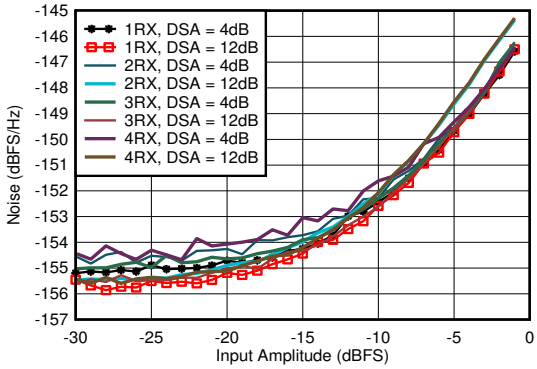
With 1.8 GHz matching, 12.5-MHz offset from tone

図 6-93. RX Noise Spectral Density vs Temperature at 1.75 GHz



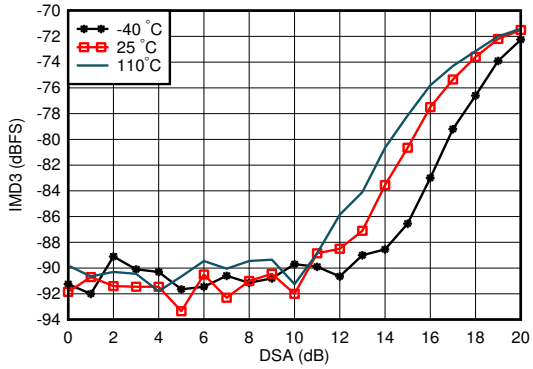
With 1.8 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

図 6-94. RX Noise Spectral Density vs Input Amplitude and Temperature at 1.75 GHz



With 1.8 GHz matching, 12.5-MHz offset from tone

図 6-95. RX Noise Spectral Density vs Input Amplitude and Channel at 1.75 GHz

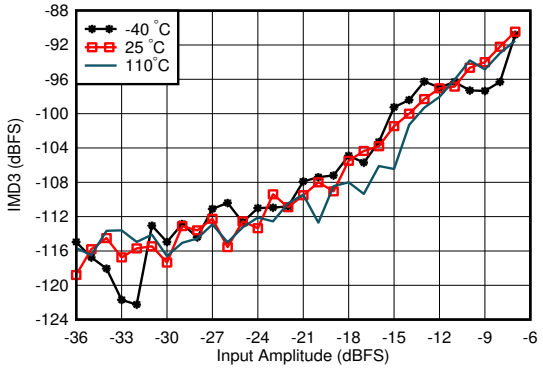


With 1.8 GHz matching, each tone –7 dBFS, tone spacing = 20 MHz

図 6-96. RX IMD3 vs DSA Setting and Temperature at 1.75 GHz

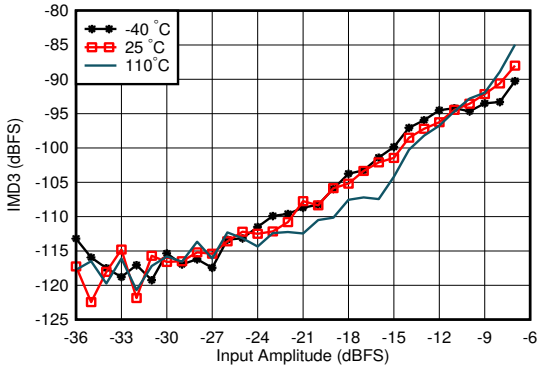
6.11.3 RX Typical Characteristics 1.75GHz to 1.9GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



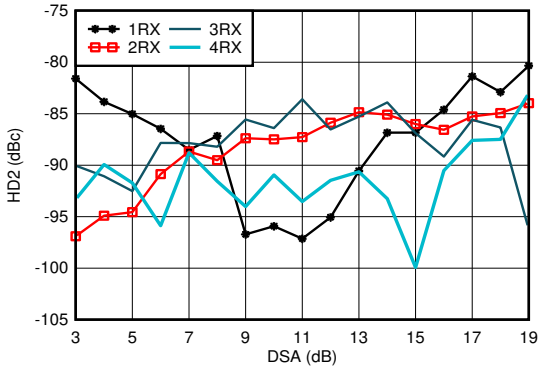
With 1.8 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

図 6-97. RX IMD3 vs Input Level and Temperature at 1.75 GHz



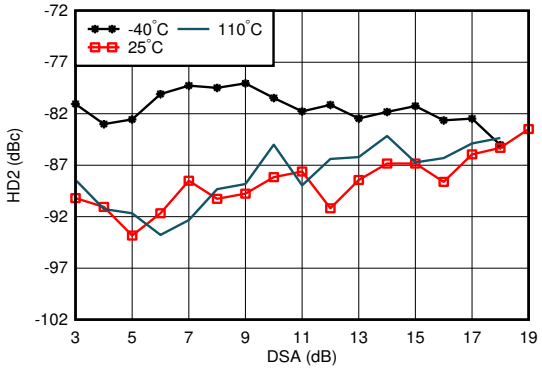
With 1.8 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

図 6-98. RX IMD3 vs Input Level and Temperature at 1.75 GHz



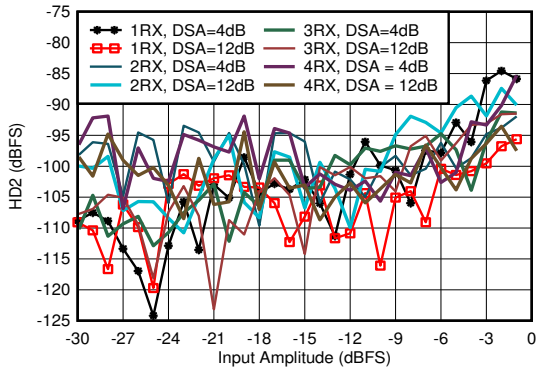
With 1.8 GHz matching, f_{in} = 1900MHz, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

図 6-99. RX HD2 vs DSA Setting and Channel at 1.9 GHz



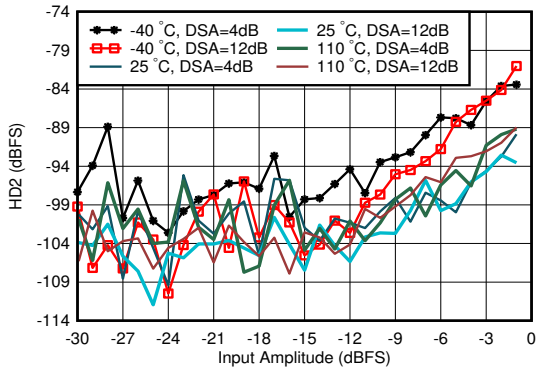
With 1.8 GHz matching, f_{in} = 1900MHz, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

図 6-100. RX HD2 vs DSA Setting and Temperature at 1.9 GHz



With 1.8 GHz matching, f_{in} = 1900MHz, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

図 6-101. RX HD2 vs Input Amplitude and Channel at 1.9 GHz

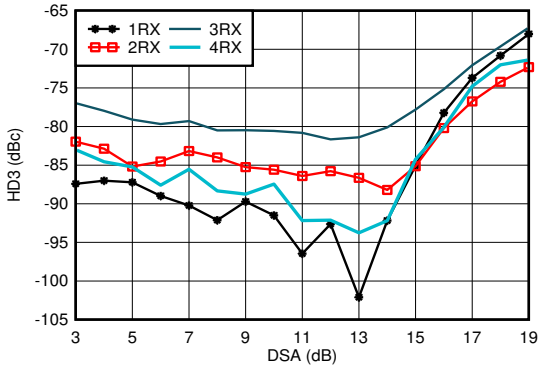


With 1.8 GHz matching, f_{in} = 1900MHz, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

図 6-102. RX HD2 vs Input Amplitude and Temperature at 1.9 GHz

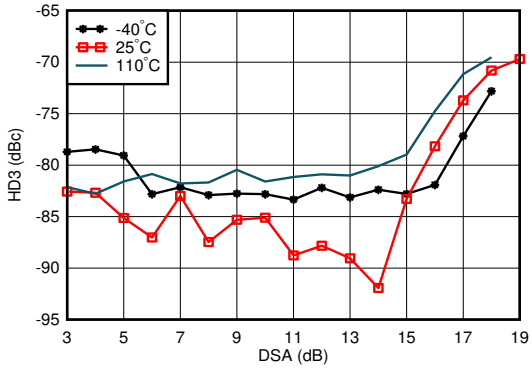
6.11.3 RX Typical Characteristics 1.75GHz to 1.9GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



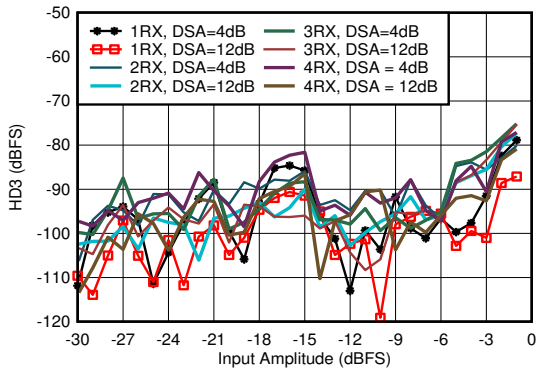
With 1.8 GHz matching, f_{in} = 1900MHz, DDC bypass mode (TI only mode for characterization)

図 6-103. RX HD3 vs DSA Setting and Channel at 1.9 GHz



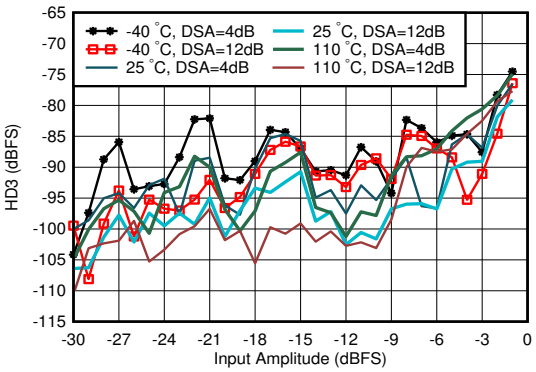
With 1.8 GHz matching, f_{in} = 1900MHz, DDC bypass mode (TI only mode for characterization)

図 6-104. RX HD3 vs DSA Setting and Temperature at 1.9 GHz



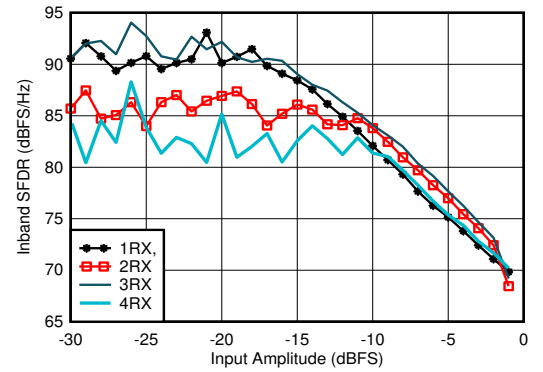
With 1.8 GHz matching, f_{in} = 1900MHz, DDC bypass mode (TI only mode for characterization)

図 6-105. RX HD3 vs Input Level and Channel at 1.9 GHz



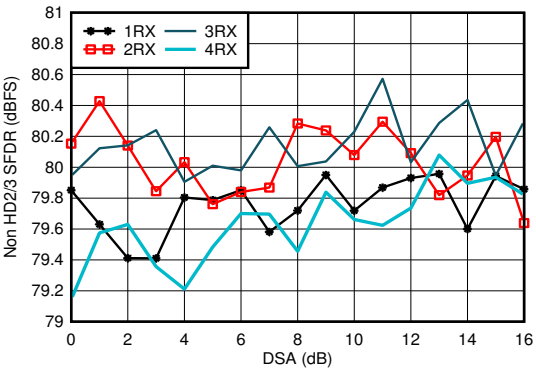
With 1.8 GHz matching, f_{in} = 1900MHz, DDC bypass mode (TI only mode for characterization)

図 6-106. RX HD3 vs Input Level and Temperature at 1.9 GHz



With 1.8 GHz matching, decimated by 3

図 6-107. RX In-Band SFDR (±400 MHz) vs Input Amplitude at 1.75 GHz

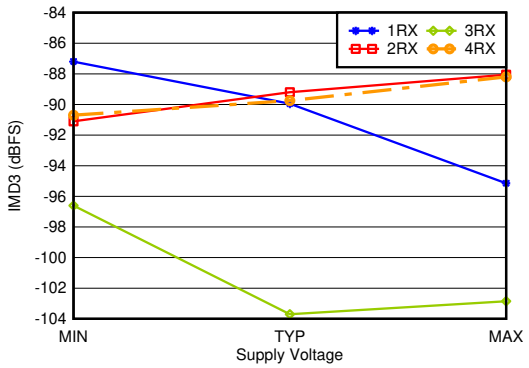


With 1.8 GHz matching

図 6-108. RX Non-HD2/3 vs DSA Setting at 1.75 GHz

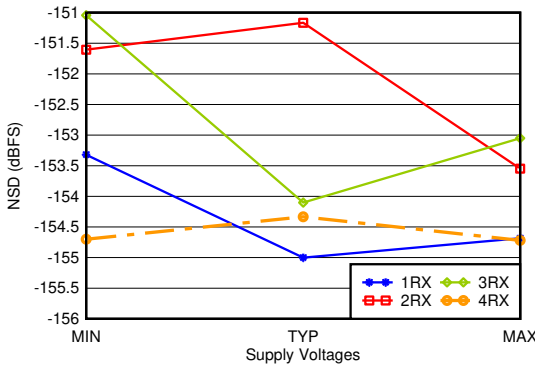
6.11.3 RX Typical Characteristics 1.75GHz to 1.9GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



With 1.8 GHz matching, –7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

図 6-109. RX IMD3 vs Supply and Channel at 1.75 GHz

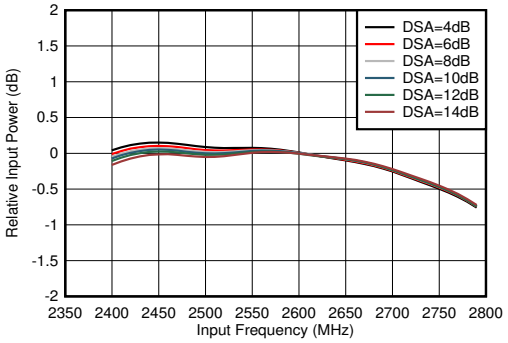


With 1.8 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

図 6-110. RX Noise Spectral Density vs Supply and Channel at 1.75 GHz

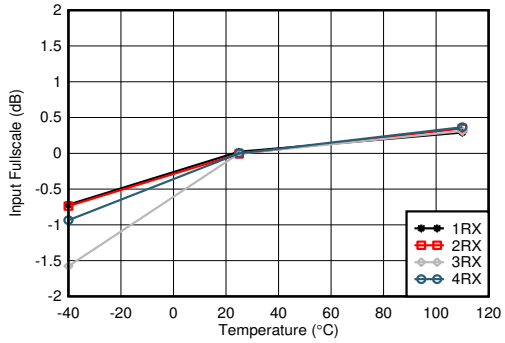
6.11.4 RX Typical Characteristics 2.6GHz

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



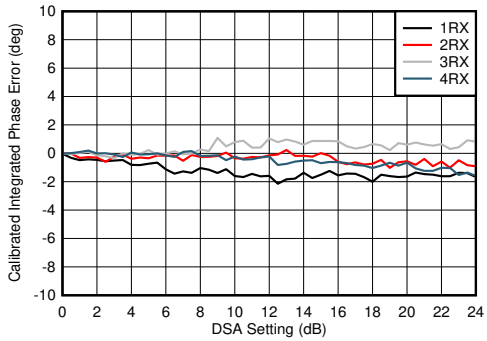
With matching, normalized to power at 2.6 GHz for each DSA setting

図 6-111. RX Inband Gain Flatness, f_{IN} = 2600 MHz



With 2.6 GHz matching, normalized to fullscale at 25°C for each channel

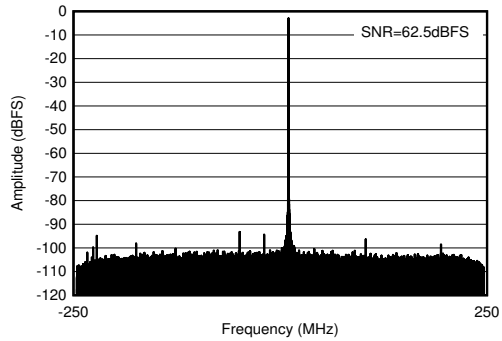
図 6-112. RX Input Fullscale vs Temperature and Channel at 2.6 GHz



With 2.6 GHz matching

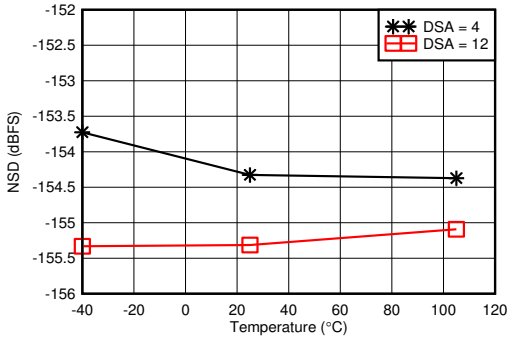
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 6-113. RX Calibrated Integrated Phase Error vs DSA Setting at 2.6 GHz



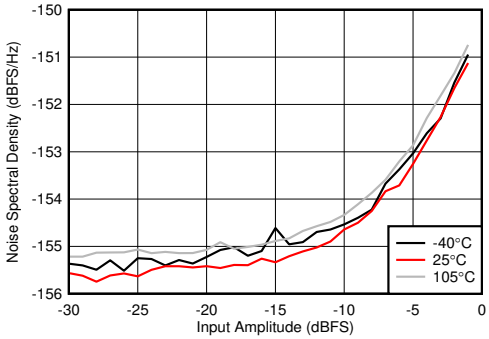
With 2.6 GHz matching, f_{IN} = 2610 MHz, A_{IN}= –3 dBFS

図 6-114. RX Output FFT at 2.6 GHz



With 2.6 GHz matching, 12.5-MHz offset from tone

図 6-115. RX Noise Spectral Density vs Temperature at 2.6 GHz

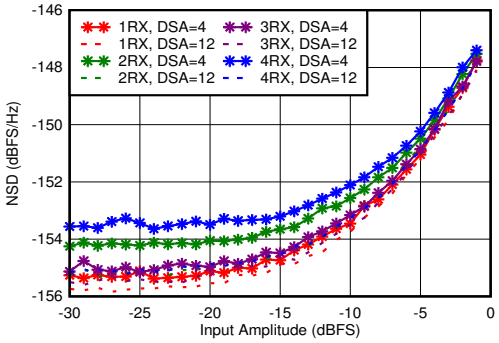


With 2.6 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

図 6-116. RX Noise Spectral Density vs Input Amplitude and Temperature at 2.6 GHz

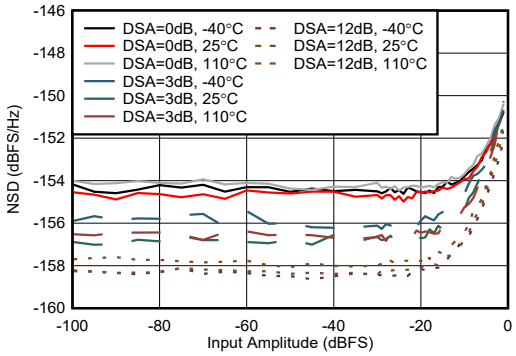
6.11.4 RX Typical Characteristics 2.6GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



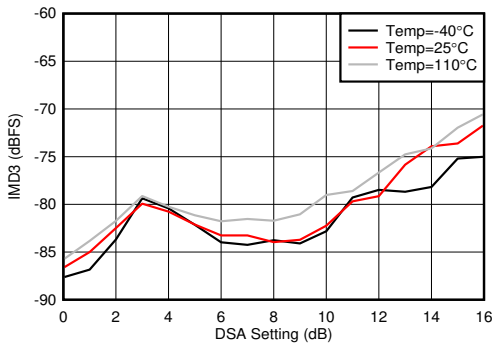
With 2.6 GHz matching, 12.5-MHz offset from tone

図 6-117. RX Noise Spectral Density vs Input Amplitude and Channel at 2.6 GHz



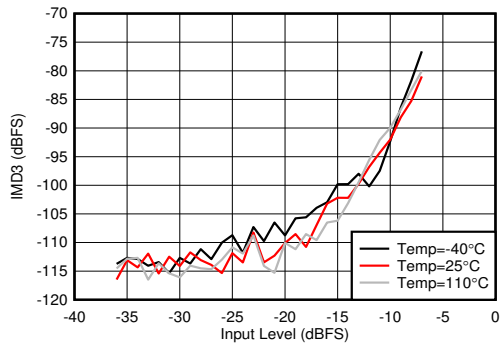
50-MHz offset from tone, external clock mode

図 6-118. RX Noise Spectral Density vs Input Amplitude at 2.61 GHz (Ext. Clock)



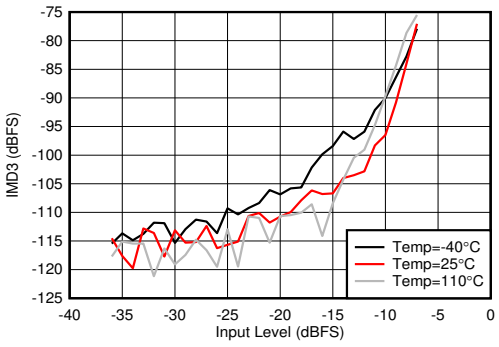
With 2.6 GHz matching, each tone –7 dBFS, tone spacing = 20 MHz

図 6-119. RX IMD3 vs DSA Setting and Temperature at 2.6 GHz



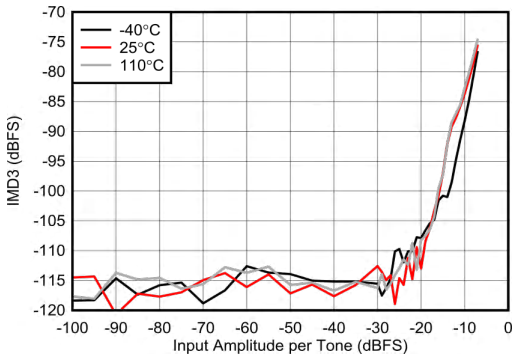
With 2.6 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

図 6-120. RX IMD3 vs Input Level and Temperature at 2.6 GHz



With 2.6 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

図 6-121. RX IMD3 vs Input Level and Temperature at 2.6 GHz

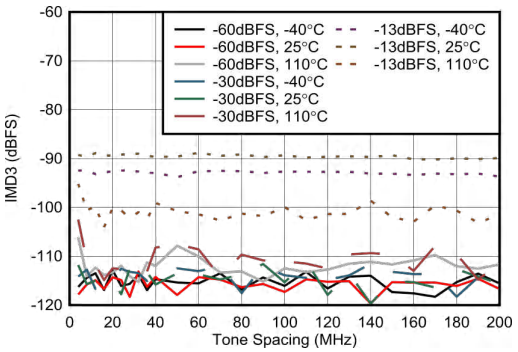


Tone spacing = 50 MHz, External clock mode

図 6-122. RX IMD3 vs Input Level at 2.6 GHz (Ext. Clock)

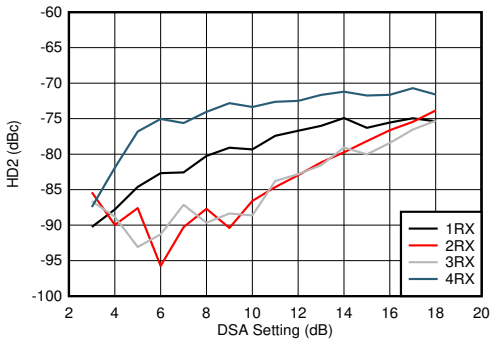
6.11.4 RX Typical Characteristics 2.6GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



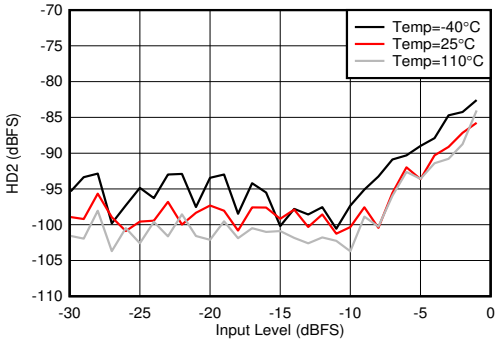
External clock mode

図 6-123. RX IMD3 vs Tone Spacing at 2.6 GHz (Ext. Clock)



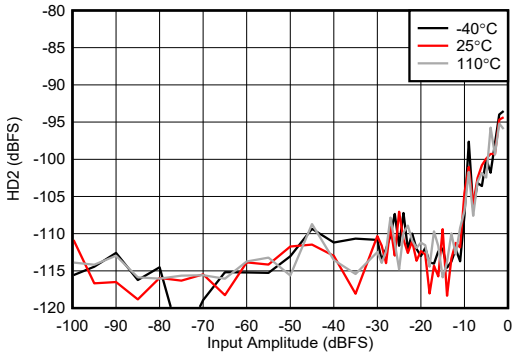
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

図 6-124. RX HD2 vs DSA Setting and Channel at 2.6 GHz



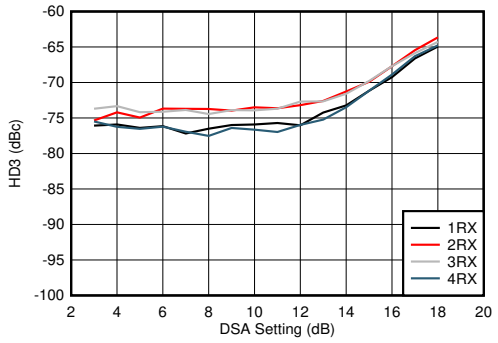
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

図 6-125. RX HD2 vs Input Level and Temperature at 2.6 GHz



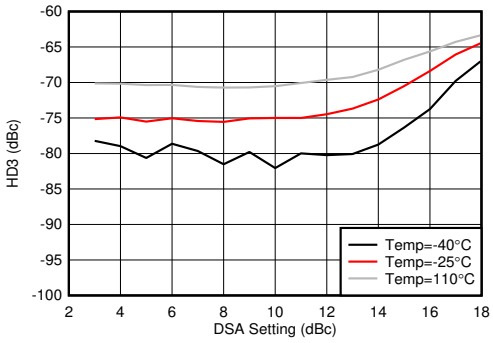
External clock mode

図 6-126. RX HD2 vs Input Level and Temperature at 2.6 GHz



With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

図 6-127. RX HD3 vs DSA Setting and Channel at 2.6 GHz

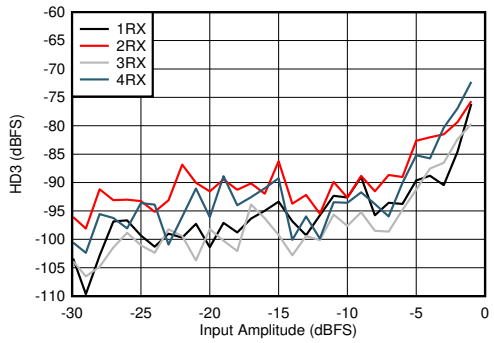


With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

図 6-128. RX HD3 vs DSA Setting and Temperature at 2.6 GHz

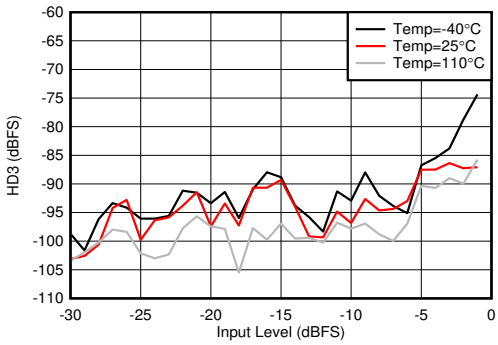
6.11.4 RX Typical Characteristics 2.6GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



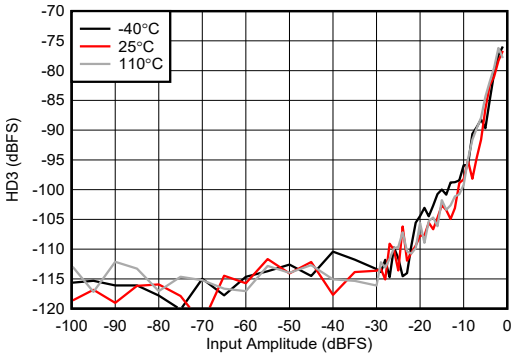
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

図 6-129. RX HD3 vs Input Level and Channel at 2.6 GHz



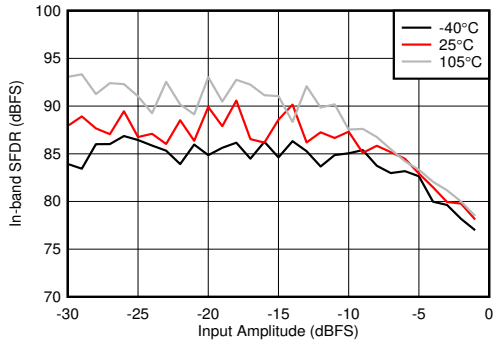
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

図 6-130. RX HD3 vs Input Level and Temperature at 2.6 GHz



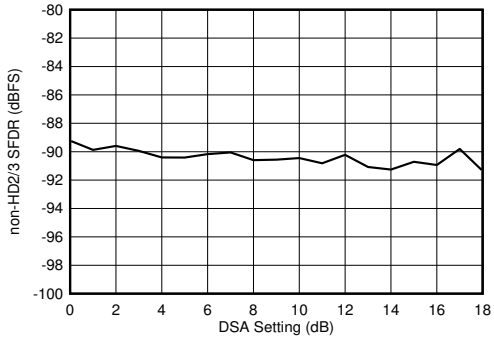
External clock mode

図 6-131. RX HD3 vs Input Level and Temperature at 2.6 GHz



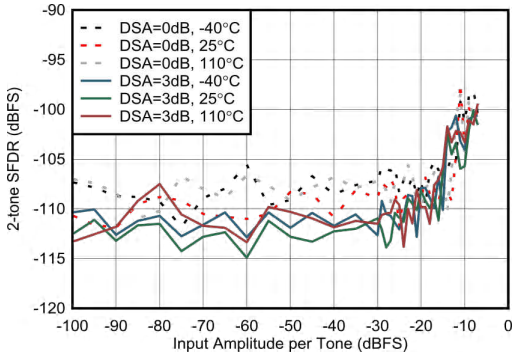
With 2.6 GHz matching, decimate by 4

図 6-132. RX In-Band SFDR (±300 MHz) vs Input Amplitude and Temperature at 2.6 GHz



With 2.6 GHz matching

図 6-133. RX Non-HD2/3 vs DSA Setting at 2.6 GHz

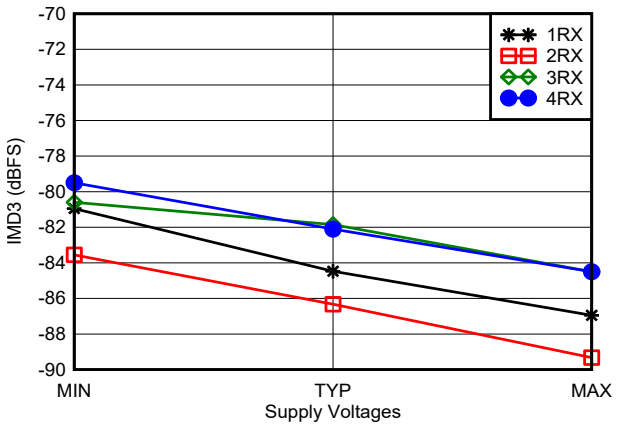


External clock mode, 50MHz tone spacing, excluding 3rd order distortion

図 6-134. RX 2-tone SFDR vs Input Amplitude at 2.6 GHz

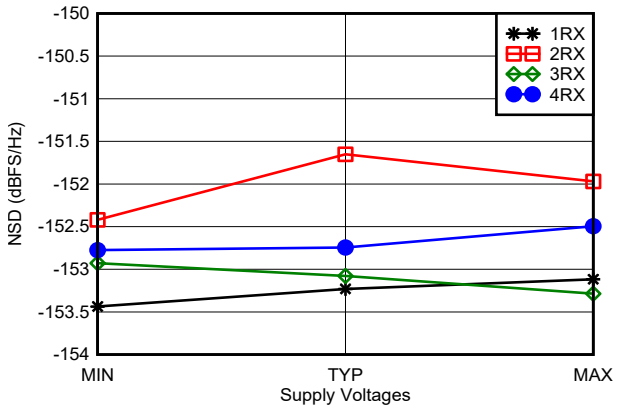
6.11.4 RX Typical Characteristics 2.6GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



With 2.6 GHz matching, –7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

図 6-135. RX IMD3 vs Supply and Channel at 2.6 GHz

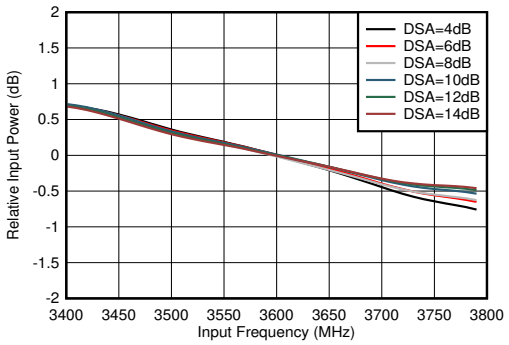


With 2.6 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

図 6-136. RX Noise Spectral Density vs Supply and Channel at 2.6 GHz

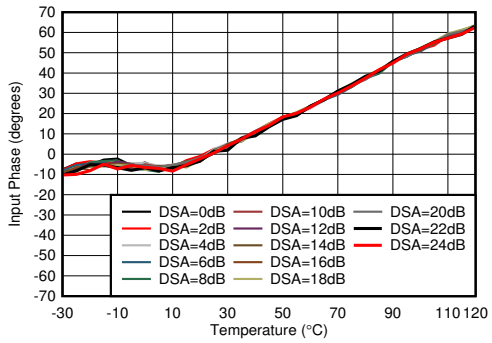
6.11.5 RX Typical Characteristics 3.5GHz

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



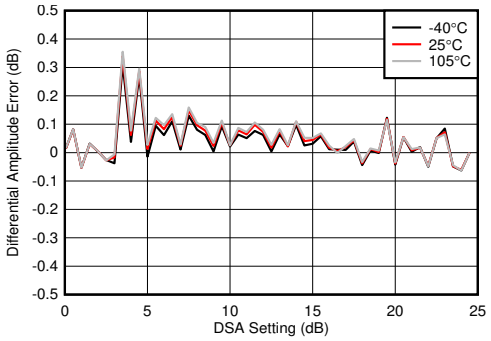
With 3.6 GHz matching, normalized to 3.6 GHz

図 6-137. RX In-Band Gain Flatness, f_{IN} = 3600 MHz



With 3.6 GHz matching, normalized to phase at 25°C

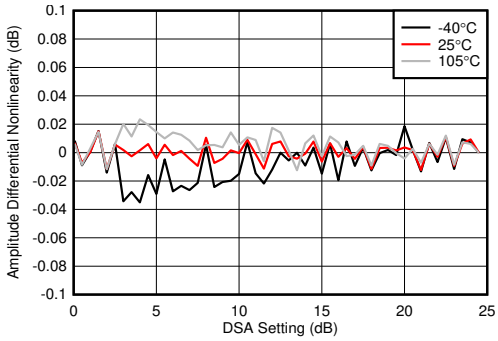
図 6-138. RX Input Phase vs Temperature at 3.6 GHz



With 3.6 GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

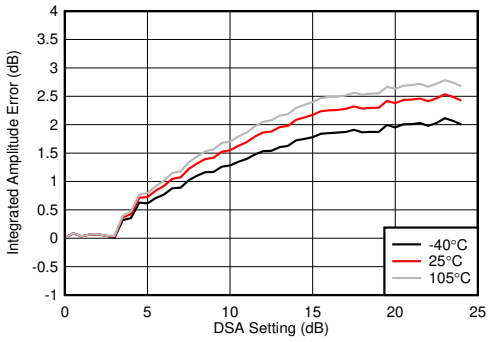
図 6-139. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

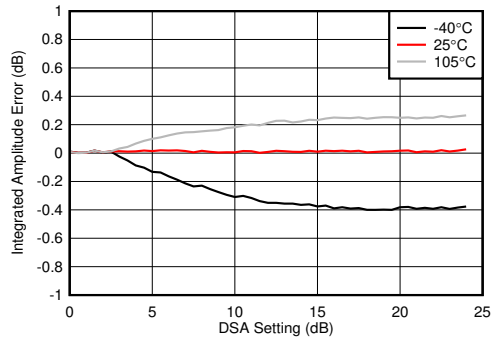
図 6-140. RX Calibrated Differential Amplitude Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching

Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

図 6-141. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 3.6 GHz



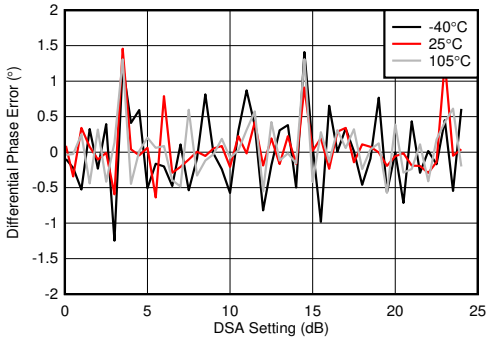
With 3.6 GHz matching

Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

図 6-142. RX Calibrated Integrated Amplitude Error vs DSA Setting at 3.6 GHz

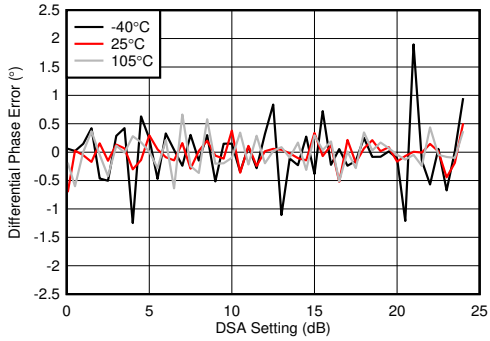
6.11.5 RX Typical Characteristics 3.5GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



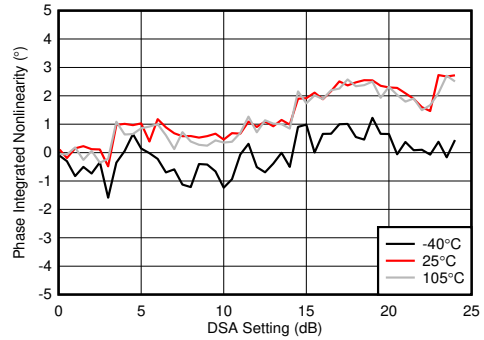
With 3.6 GHz matching
Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

図 6-143. RX Uncalibrated Phase Error vs DSA Setting at 3.6 GHz



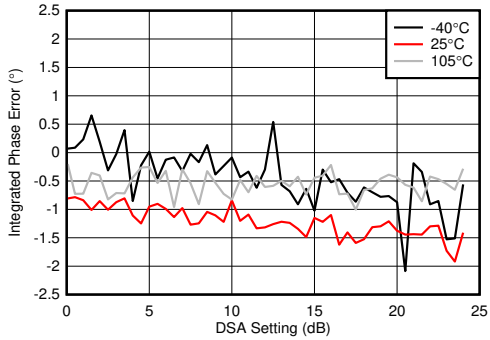
With 3.6 GHz matching
Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

図 6-144. RX Calibrated Differential Phase Error vs DSA Setting at 3.6 GHz



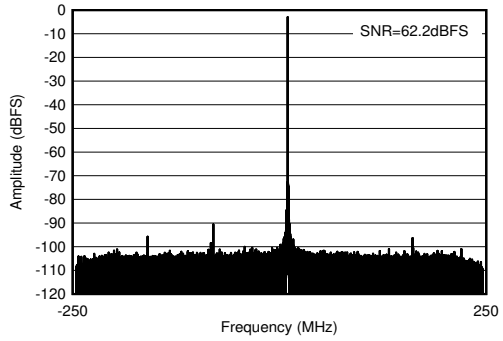
With 3.6 GHz matching
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 6-145. RX Uncalibrated Integrated Phase Error vs DSA Setting at 3.6 GHz



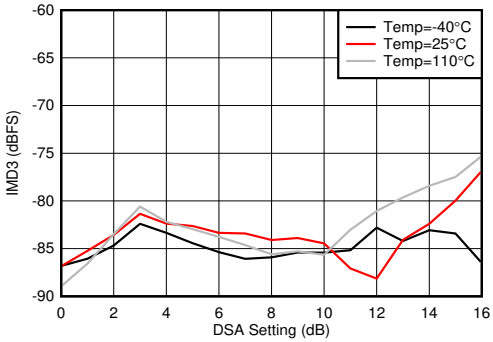
With 3.6 GHz matching
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 6-146. RX Calibrated Integrated Phase Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching , f_{IN} = 3610 MHz, A_{IN} = –3 dBFS

図 6-147. RX Output FFT at 3.6 GHz

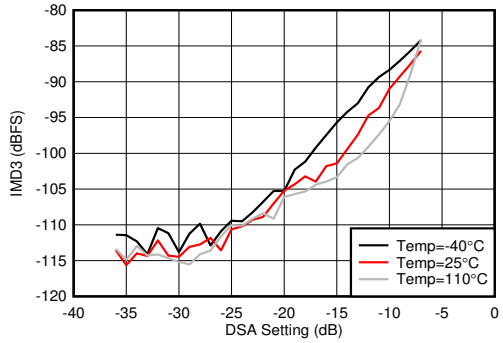


With 3.5 GHz matching, each tone at –7 dBFS, 20-MHz tone spacing

図 6-148. RX IMD3 vs DSA Setting and Temperature at 3.6 GHz

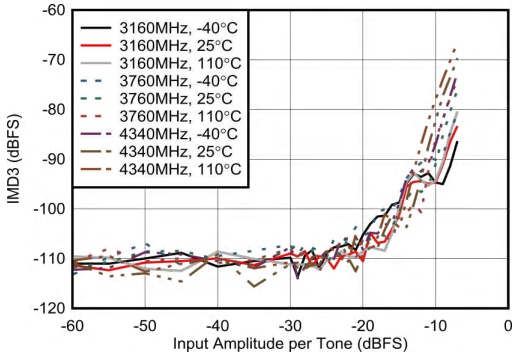
6.11.5 RX Typical Characteristics 3.5GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



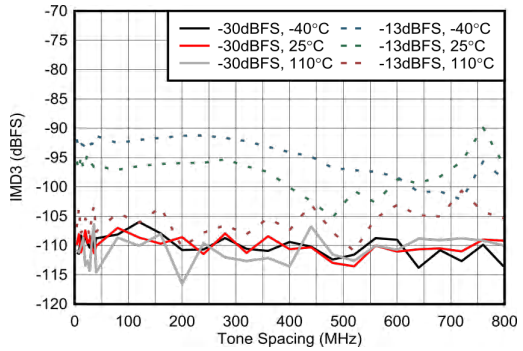
With 3.5 GHz matching, 20-MHz tone spacing

図 6-149. RX IMD3 vs Input Level and Temperature at 3.6 GHz



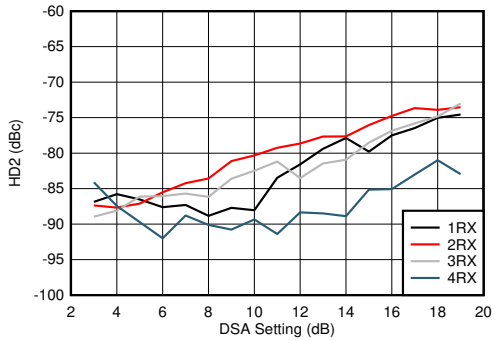
External clock mode, 20-MHz tone spacing, 2x Decimation

図 6-150. RX IMD3 vs Input Level



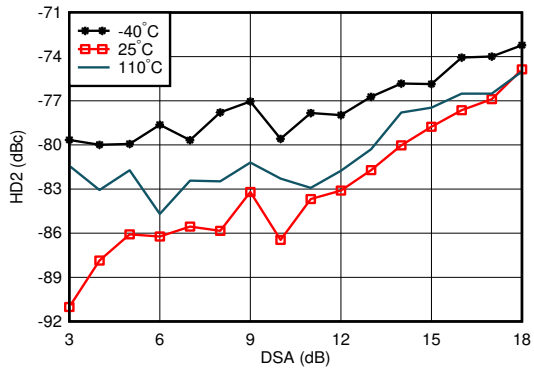
External clock mode, 2x Decimation

図 6-151. RX IMD3 vs Tone Spacing at 3.76GHz



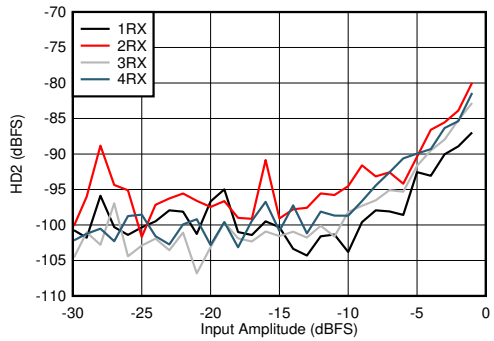
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

図 6-152. RX HD2 vs DSA Setting and Channel at 3.6 GHz



With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

図 6-153. RX HD2 vs DSA Setting and Temperature at 3.6 GHz

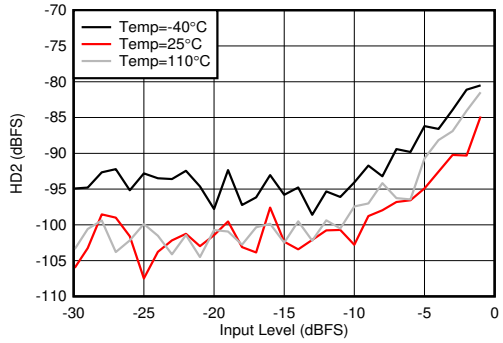


With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

図 6-154. RX HD2 vs Input Level and Channel at 3.6 GHz

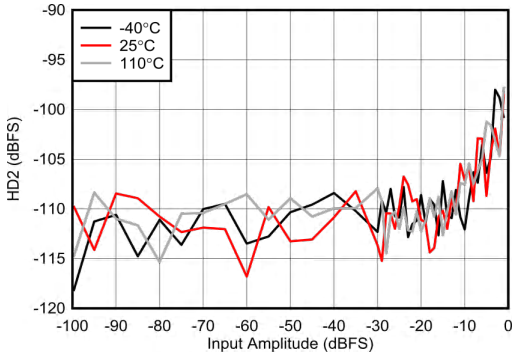
6.11.5 RX Typical Characteristics 3.5GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



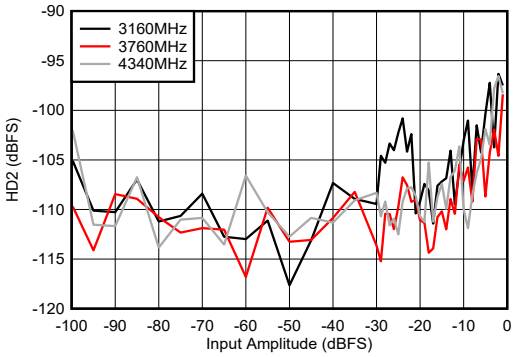
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

図 6-155. RX HD2 vs Input Level and Temperature at 3.6 GHz



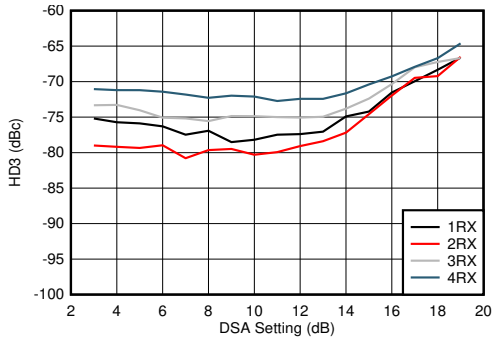
External clock mode, 2x Decimation

図 6-156. RX HD2 vs Input Level at 3.76 GHz



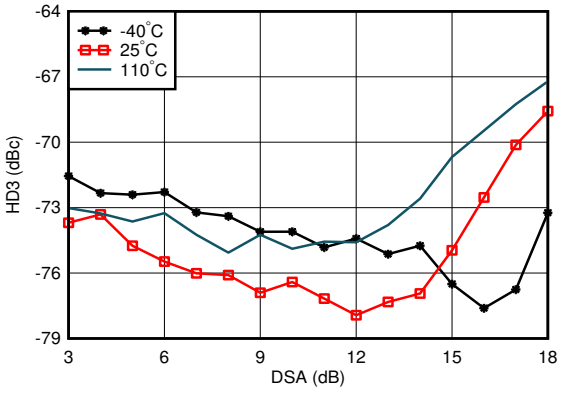
External clock mode, 25°C, 2x Decimation

図 6-157. RX HD2 vs Input Level



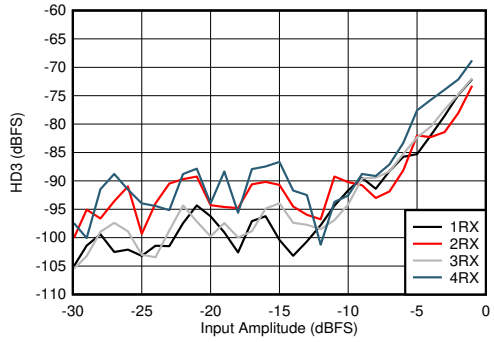
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

図 6-158. RX HD3 vs DSA Setting and Channel at 3.6 GHz



With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

図 6-159. RX HD3 vs DSA Setting and Temperature at 3.6 GHz

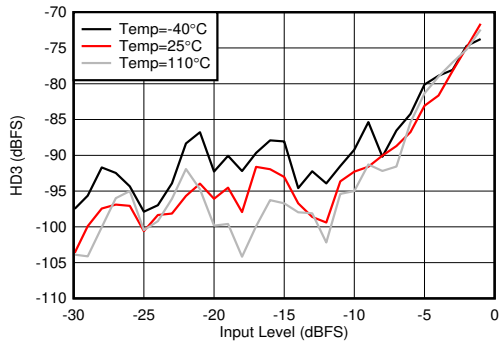


With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

図 6-160. RX HD3 vs Input Level and Channel at 3.6 GHz

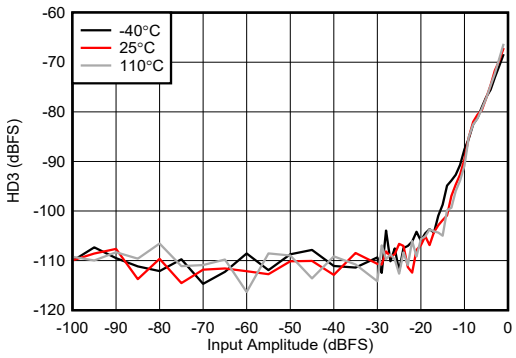
6.11.5 RX Typical Characteristics 3.5GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



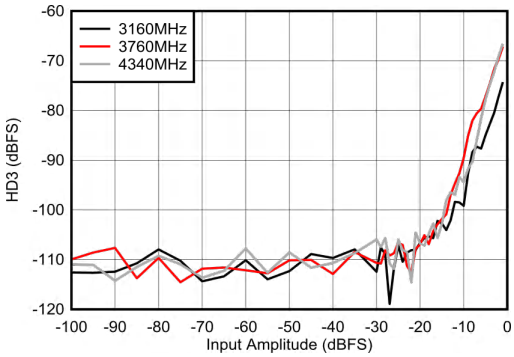
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

図 6-161. RX HD3 vs Input Level and Temperature at 3.6 GHz



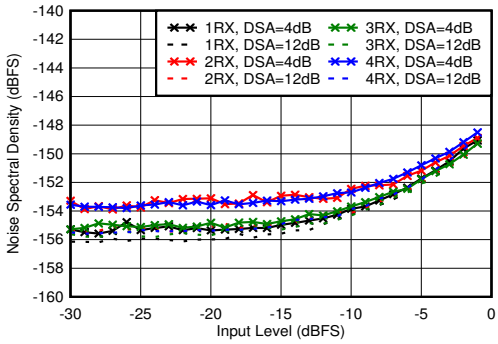
External clock mode, 2x Decimation

図 6-162. RX HD3 vs Input Level at 3.76GHz



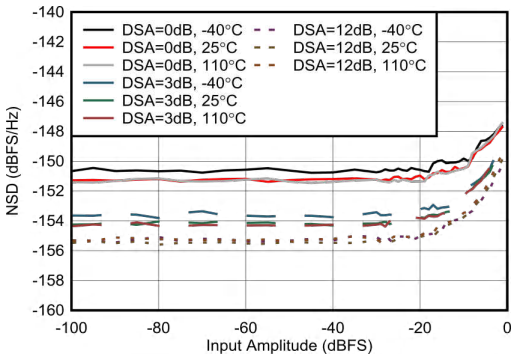
External clock mode, 25°C, 2x Decimation

図 6-163. RX HD3 vs Input Level



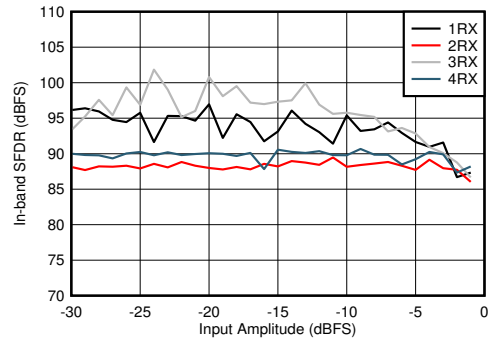
With 3.5 GHz matching, 12.5-MHz offset from tone

図 6-164. RX Noise Spectral Density vs Input Level and DSA Setting at 3.6 GHz



External clock mode, 25°C, 2x Decimation

図 6-165. RX Noise Spectral Density vs Input Level at 3.76GHz

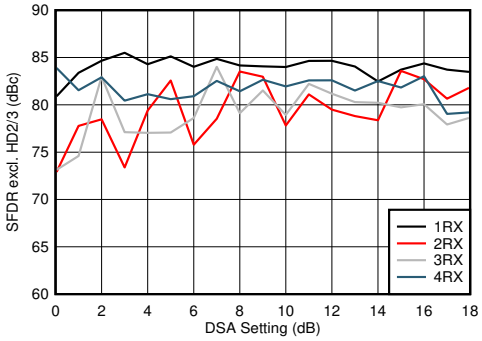


With 3.5 GHz matching

図 6-166. RX In-Band SFDR (±200 MHz) vs Input Level and Channel at 3.6 GHz

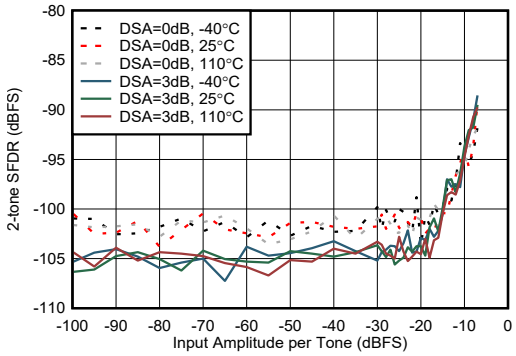
6.11.5 RX Typical Characteristics 3.5GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



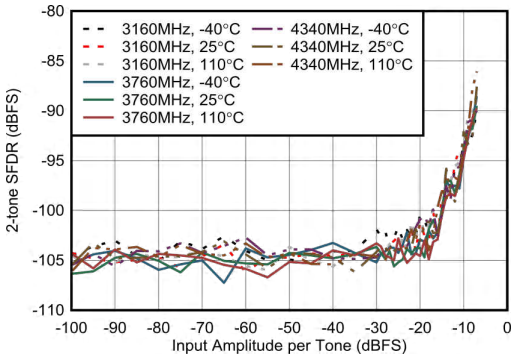
With 3.5 GHz matching

図 6-167. RX SFDR Excluding HD2/3 vs DSA Setting and Channel at 3.6 GHz



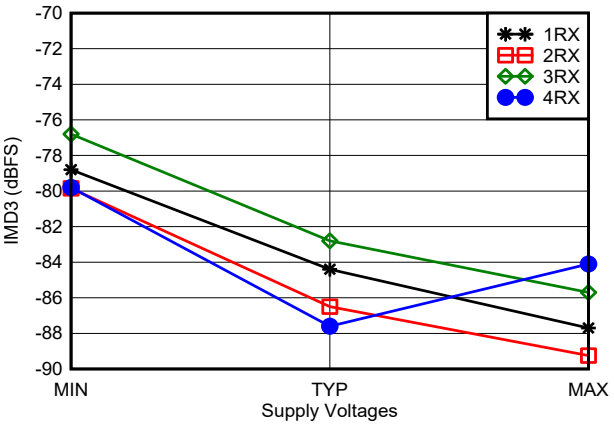
External clock mode, 20MHz tone spacing, excluding 3rd order distortion

図 6-168. RX 2-tone SFDR vs Input Amplitude and DSA Setting at 3.7 GHz



External clock mode, 20MHz tone spacing, excluding 3rd order distortion

図 6-169. RX 2-tone SFDR vs Input Amplitude and Frequency at 3.7 GHz

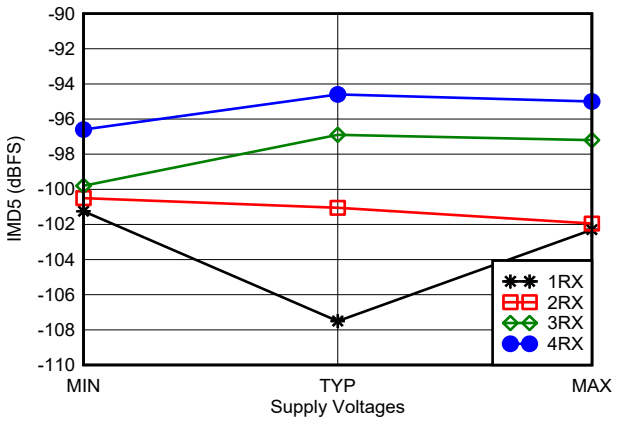


With 3.6 GHz matching, –7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

図 6-170. RX IMD3 vs Supply Voltage and Channel at 3.6 GHz

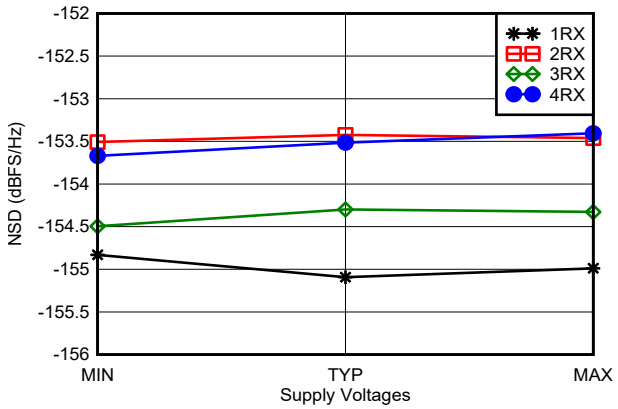
6.11.5 RX Typical Characteristics 3.5GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



With 3.6 GHz matching, –7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

図 6-171. RX IMD5 vs Supply Voltage and Channel at 3.6 GHz

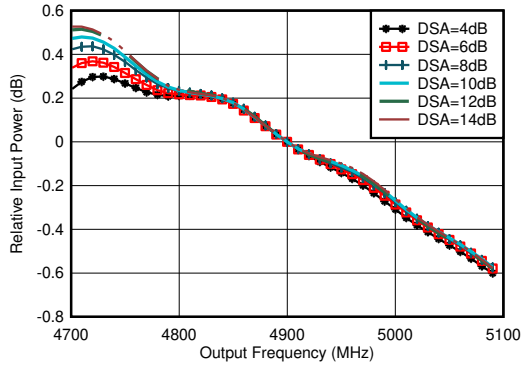


With 3.6 GHz matching, tone at –20 dBFS, 12.5-MHz offset frequency, all supplies at MIN, TYP, or MAX recommended operating voltages

図 6-172. RX Noise Spectral Density vs Supply Voltage and Channel at 3.6 GHz

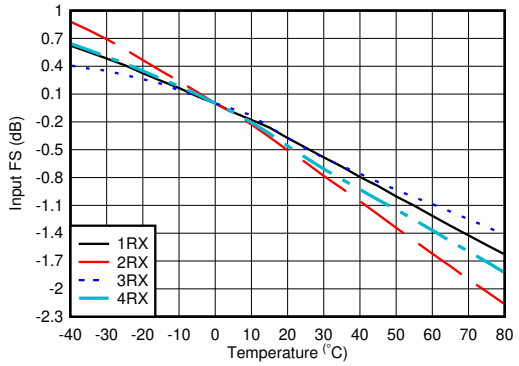
6.11.6 RX Typical Characteristics 4.9GHz

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



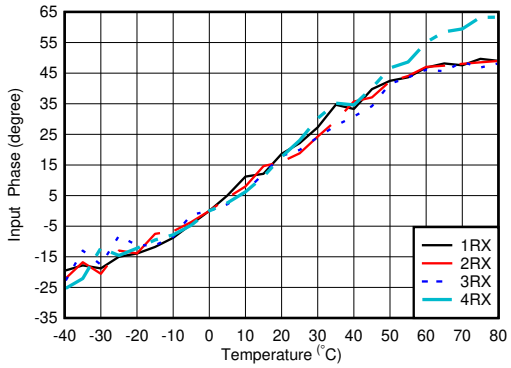
With matching, normalized to power at 4.9GHz for each DSA setting

図 6-173. RX Inband Gain Flatness, f_{IN} = 4900 MHz



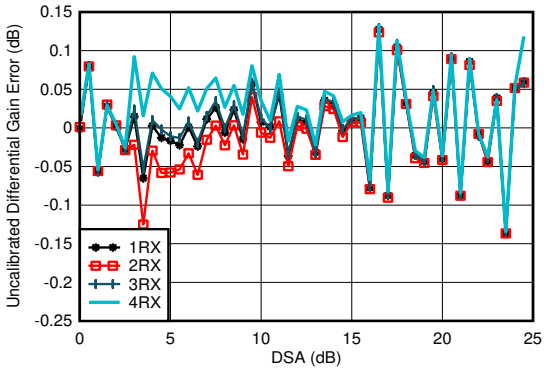
With 4.9 GHz matching, normalized to fullscale at 25°C for each channel

図 6-174. RX Input Fullscale vs Temperature and Channel at 4.9 GHz



With 4.9 GHz matching, normalized to phase at 25°C

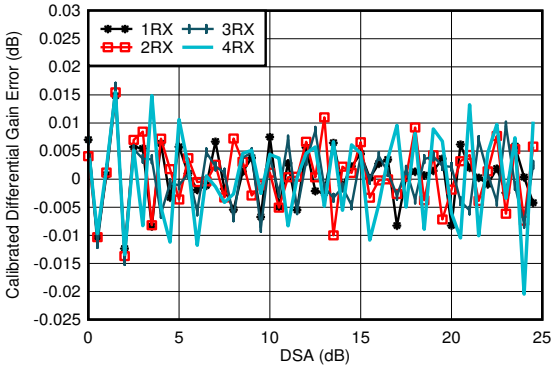
図 6-175. RX Input Phase vs Temperature and DSA at f_{OUT} = 4.9 GHz



With 4.9 GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

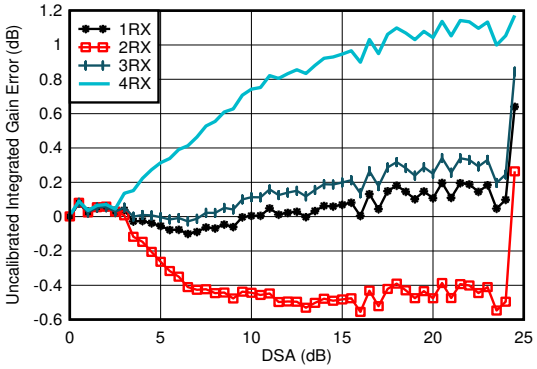
図 6-176. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 4.9 GHz



With 4.9 GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

図 6-177. RX Calibrated Differential Amplitude Error vs DSA Setting at 4.9 GHz



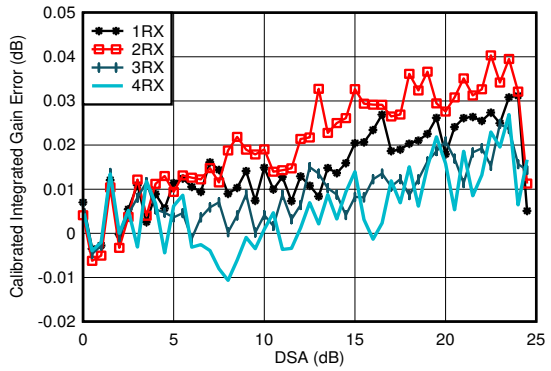
With 4.9 GHz matching

Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

図 6-178. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 4.9 GHz

6.11.6 RX Typical Characteristics 4.9GHz (continued)

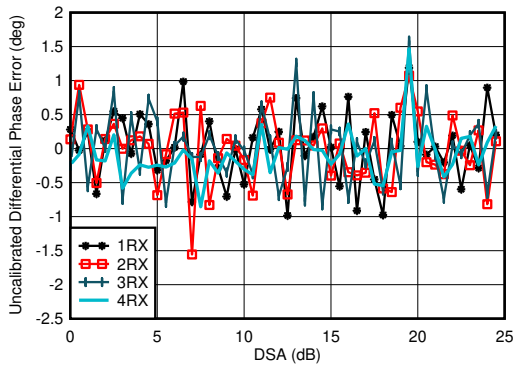
Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



With 4.9 GHz matching

Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

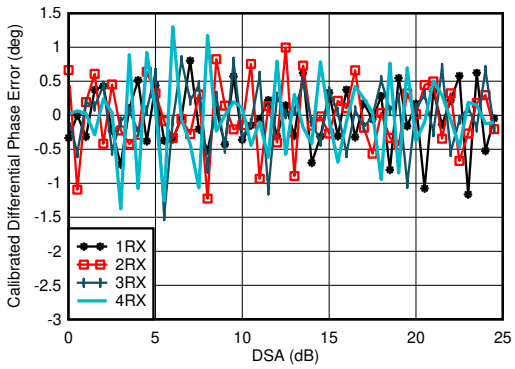
図 6-179. RX Calibrated Integrated Amplitude Error vs DSA Setting at 4.9 GHz



With 4.9 GHz matching

Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

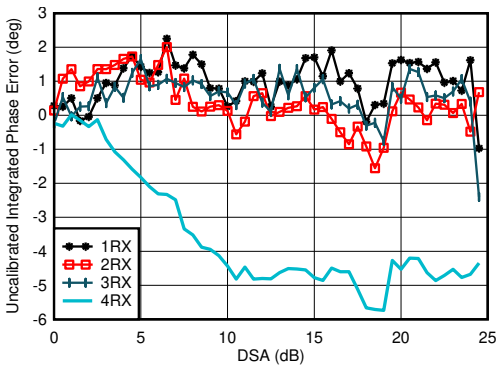
図 6-180. RX Uncalibrated Differential Phase Error vs DSA Setting at 4.9 GHz



With 4.9 GHz matching

Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

図 6-181. RX Calibrated Differential Phase Error vs DSA Setting at 4.9 GHz



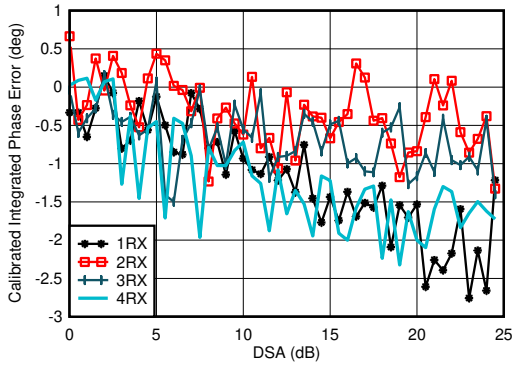
With 4.9 GHz matching

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 6-182. RX Uncalibrated Integrated Phase Error vs DSA Setting at 4.9 GHz

6.11.6 RX Typical Characteristics 4.9GHz (continued)

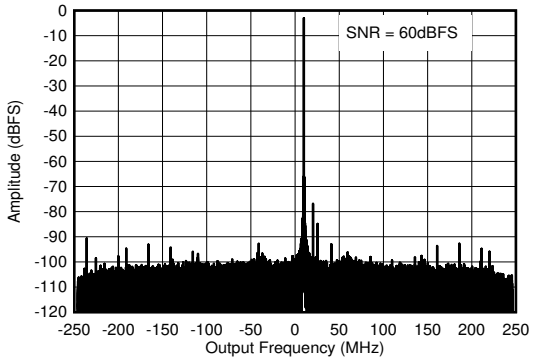
Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



With 4.9 GHz matching

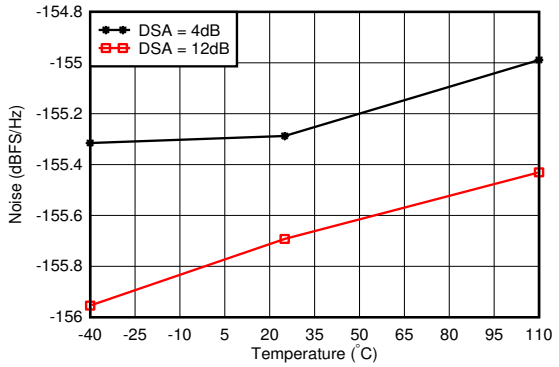
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 6-183. RX Calibrated Integrated Phase Error vs DSA Setting at 4.9 GHz



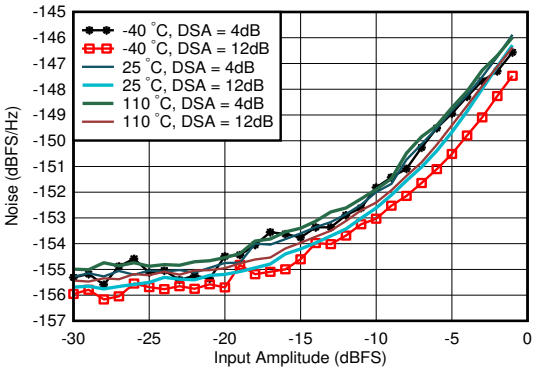
With 4.9 GHz matching, f_{IN} = 4910 MHz, A_{IN}= –3 dBFS

図 6-184. RX Output FFT at 4.9 GHz



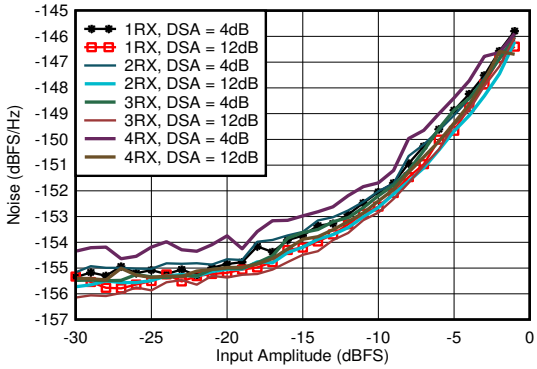
With 4.9 GHz matching, 12.5-MHz offset from tone

図 6-185. RX Noise Spectral Density vs Temperature at 4.9 GHz



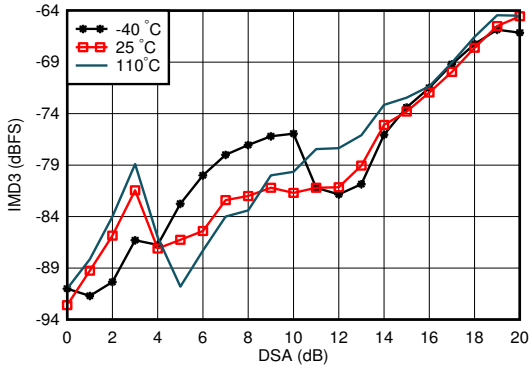
With 4.9 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

図 6-186. RX Noise Spectral Density vs Input Amplitude and Temperature at 4.9 GHz



With 4.9 GHz matching, 12.5-MHz offset from tone

図 6-187. RX Noise Spectral Density vs Input Amplitude and Channel at 4.9 GHz

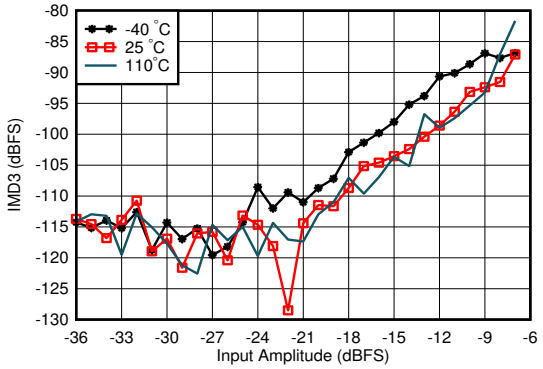


With 4.9 GHz matching, each tone –7 dBFS, tone spacing = 20 MHz

図 6-188. RX IMD3 vs DSA Setting and Temperature at 4.9 GHz

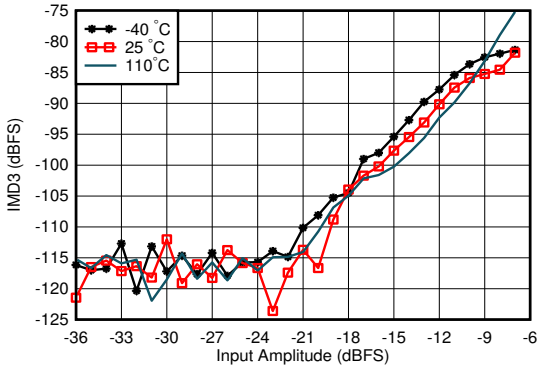
6.11.6 RX Typical Characteristics 4.9GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



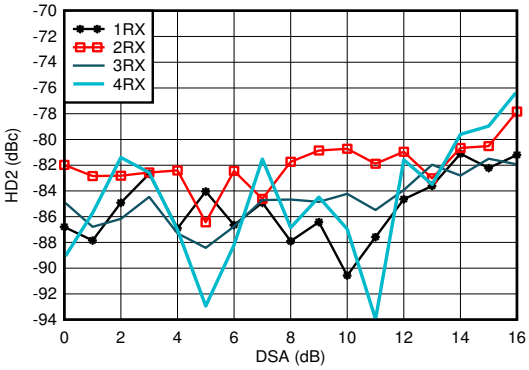
With 4.9 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

図 6-189. RX IMD3 vs Input Level and Temperature at 4.9 GHz



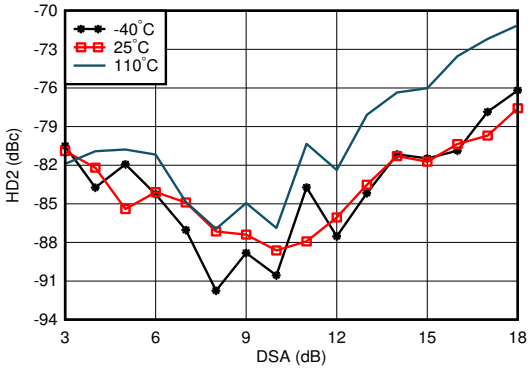
With 4.9 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

図 6-190. RX IMD3 vs Input Level and Temperature at 4.9 GHz



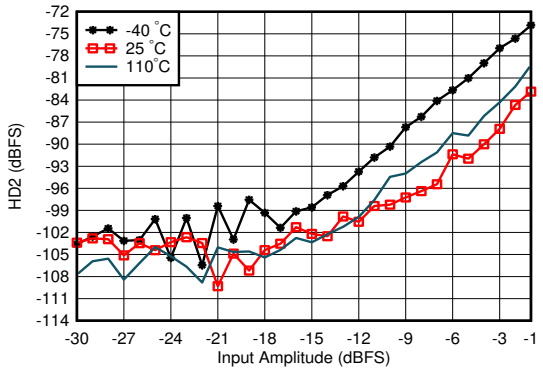
With 4.9 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

図 6-191. RX HD2 vs DSA Setting and Channel at 4.9 GHz



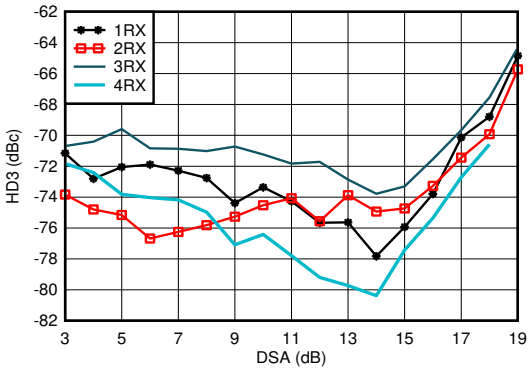
With 4.9 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

図 6-192. RX HD2 vs DSA and Temperature at 4.9 GHz



With 4.9 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

図 6-193. RX HD2 vs Input Level and Temperature at 4.9 GHz

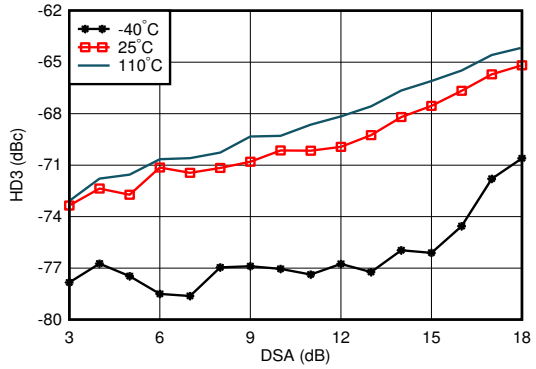


With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

図 6-194. RX HD3 vs DSA Setting and Channel at 4.9 GHz

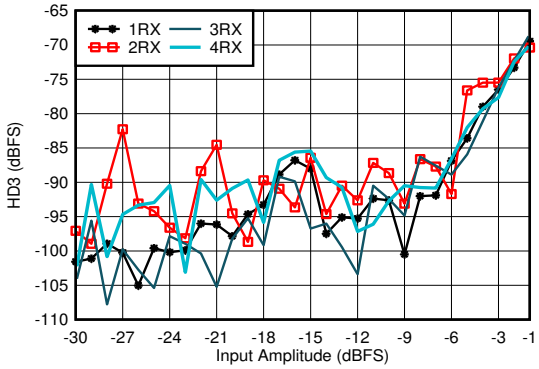
6.11.6 RX Typical Characteristics 4.9GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



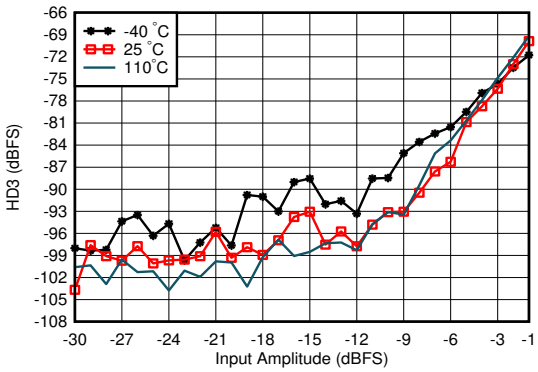
With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

図 6-195. RX HD3 vs DSA Setting and Temperature at 4.9 GHz



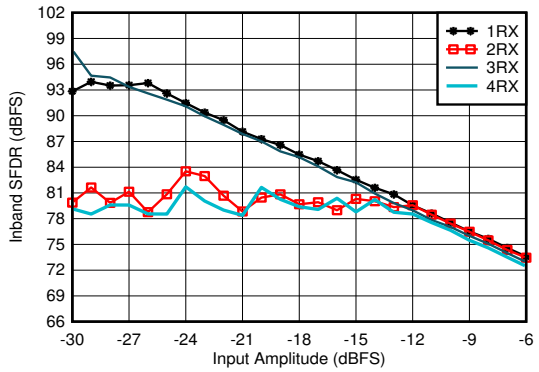
With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

図 6-196. RX HD3 vs Input Level and Channel at 4.9 GHz



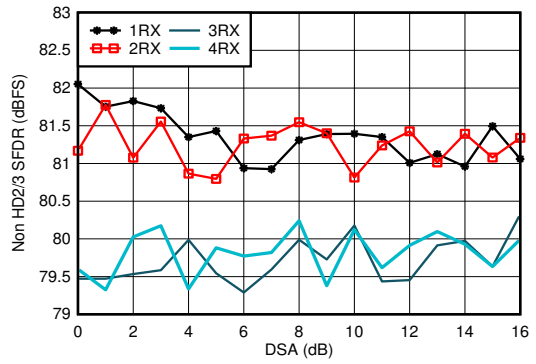
With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

図 6-197. RX HD3 vs Input Level and Temperature at 4.9 GHz



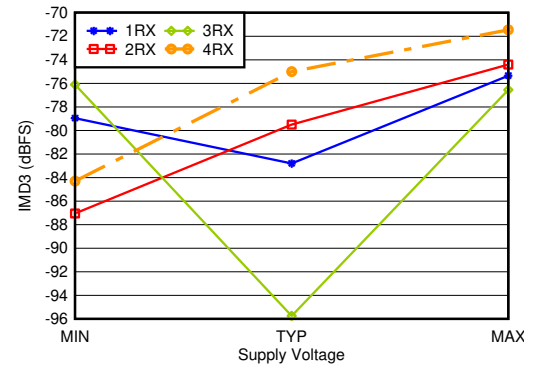
With 4.9 GHz matching, decimate by 3

図 6-198. RX In-Band SFDR (±400 MHz) vs Input Amplitude and Channel at 4.9 GHz



With 4.9 GHz matching

図 6-199. RX Non-HD2/3 vs DSA Setting at 4.9 GHz

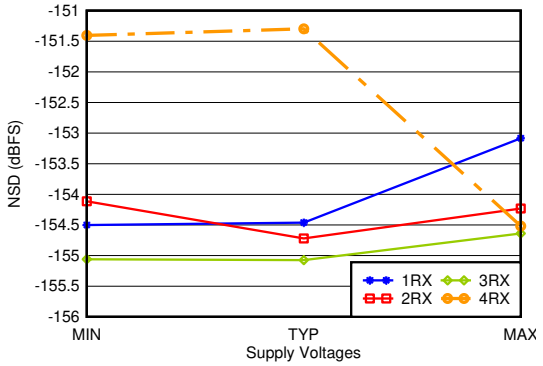


With 4.9 GHz matching, –7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

図 6-200. RX IMD3 vs Supply and Channel at 4.9 GHz

6.11.6 RX Typical Characteristics 4.9GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.

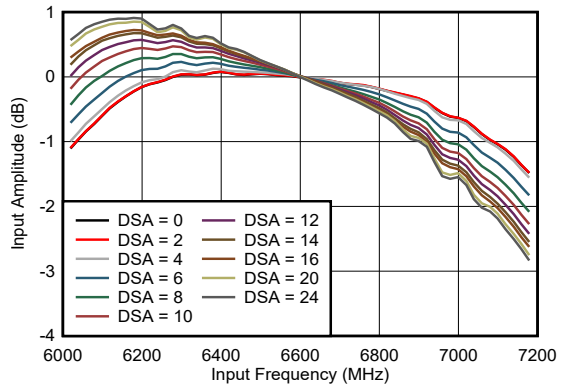


With 4.9 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

図 6-201. RX Noise Spectral Density vs Supply and Channel at 4.9 GHz

6.11.7 RX Typical Characteristics 6.8GHz

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 3000MSPS, output sample rate = 1500MSPS (decimate by 2x), External clock mode , A_{IN} = –3 dBFS, DSA setting = 3 dB.



Normalized to 6.6GHz

図 6-202. RX In-Band Gain Flatness

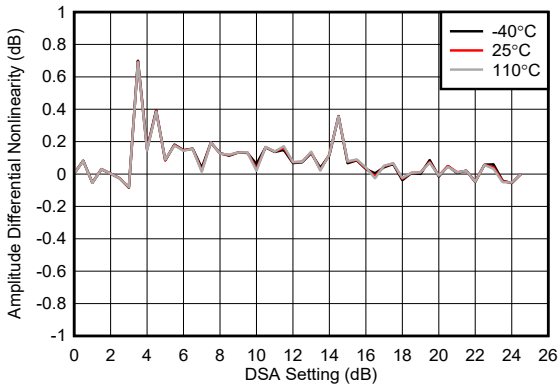
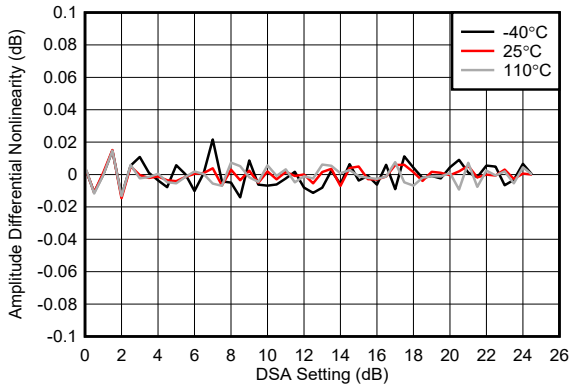


図 6-203. RX Uncalibrated Differential Amplitude Error at 6.851GHz



Calibrated at 25°C, held at -40 and 110°C

図 6-204. RX Calibrated Differential Amplitude Error at 6.851GHz

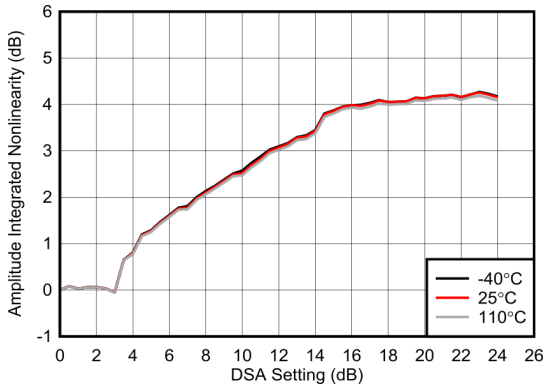
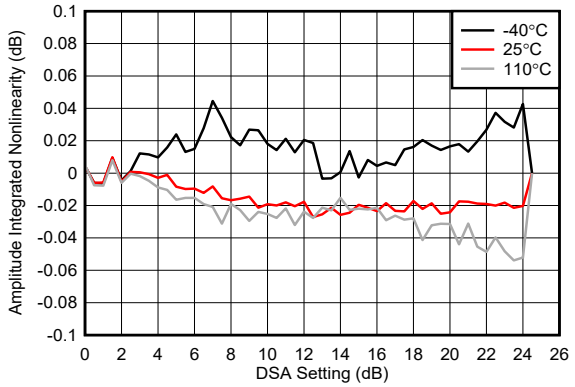


図 6-205. RX Uncalibrated Integrated Amplitude Error at 6.851GHz

6.11.7 RX Typical Characteristics 6.8GHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 3000MSPS, output sample rate = 1500MSPS (decimate by 2x), External clock mode , A_{IN} = –3 dBFS, DSA setting = 3 dB.



Calibrated at 25°C, held at -40 and 110°C

図 6-206. RX Calibrated Integrated Amplitude Error at 6.851GHz

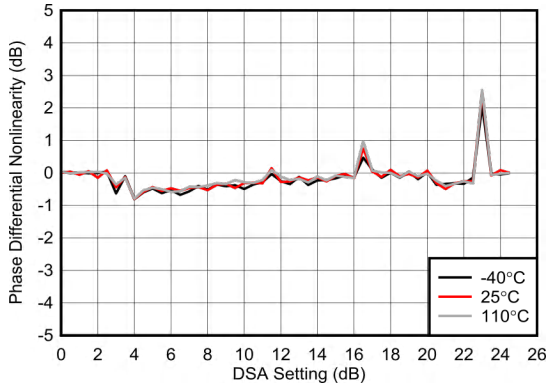
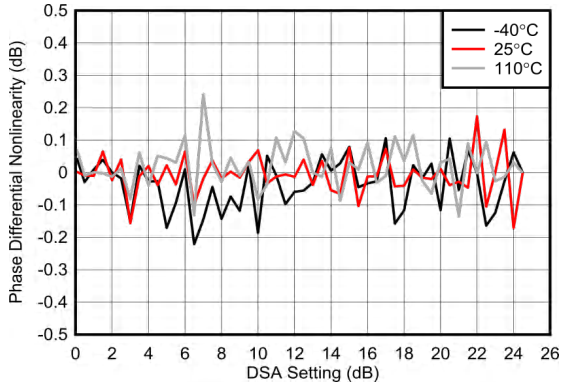


図 6-207. RX Uncalibrated Differential Phase Error at 6.851GHz



Calibrated at 25°C, held at -40 and 110°C

図 6-208. RX Calibrated Differential Phase Error at 6.851GHz

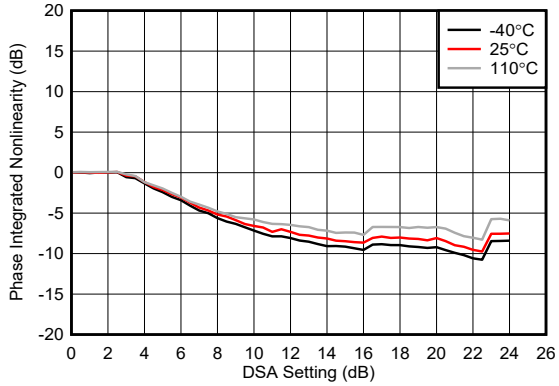
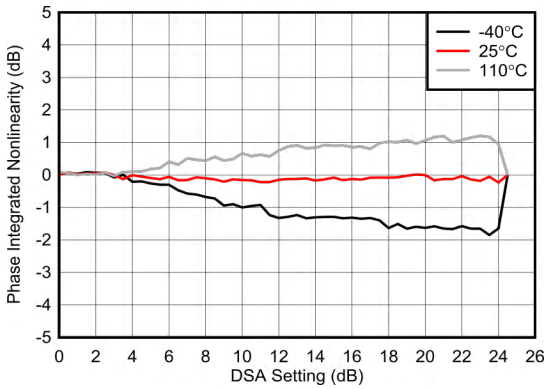
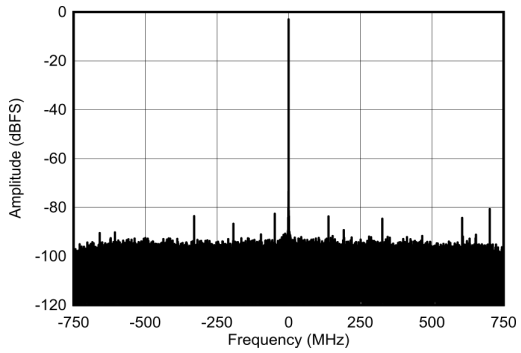


図 6-209. RX Uncalibrated Integrated Phase Error at 6.851GHz



Calibrated at 25°C, held at -40 and 110°C

図 6-210. RX Calibrated Integrated Phase Error at 6.851GHz

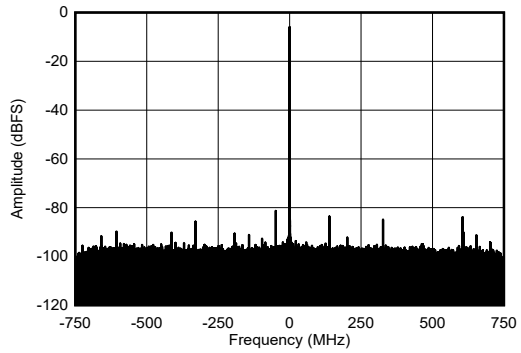


F_{NCO} = 6.851GHz, F_{IN} offset -130kHz

図 6-211. RX Output FFT at 6.851GHz and -3dBFS

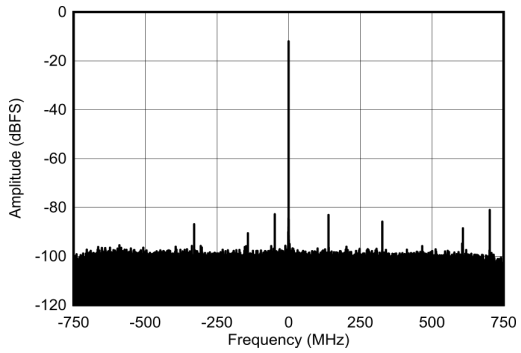
6.11.7 RX Typical Characteristics 6.8GHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 3000MSPS, output sample rate = 1500MSPS (decimate by 2x), External clock mode , A_{IN} = –3 dBFS, DSA setting = 3 dB.



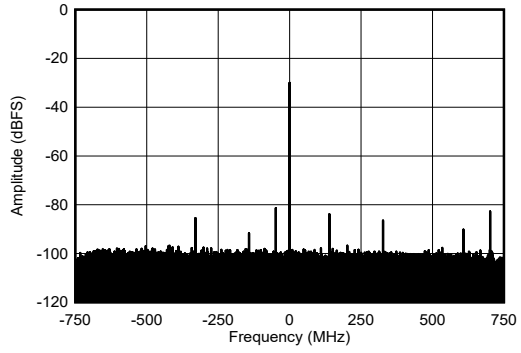
F_{NCO} = 6.851GHz, F_{IN} offset -130kHz

図 6-212. RX Output FFT at 6.851GHz and -6dBFS



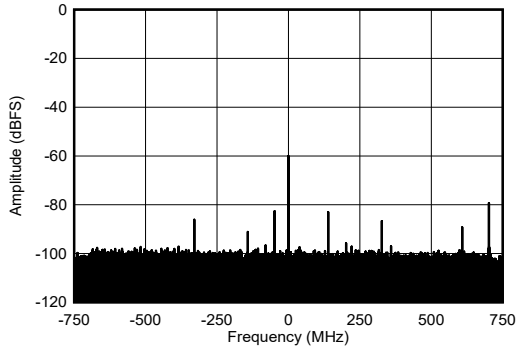
F_{NCO} = 6.851GHz, F_{IN} offset -130kHz

図 6-213. RX Output FFT at 6.851GHz and -12dBFS



F_{NCO} = 6.851GHz, F_{IN} offset -130kHz

図 6-214. RX Output FFT at 6.851GHz and -30dBFS



F_{NCO} = 6.851GHz, F_{IN} offset -130kHz

図 6-215. RX Output FFT at 6.851GHz and -60dBFS

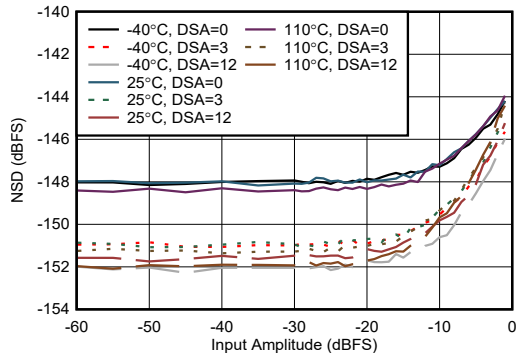
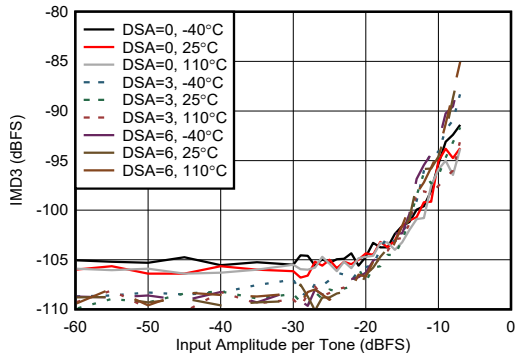


図 6-216. RX NSD vs Input Amplitude at 6.851GHz

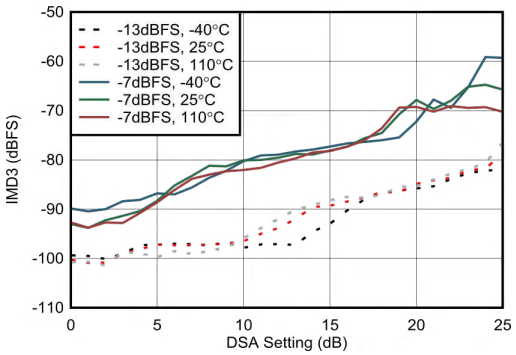


100MHz Tone Spacing

図 6-217. RX IMD3 vs Input Amplitude at 6.851GHz

6.11.7 RX Typical Characteristics 6.8GHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 3000MSPS, output sample rate = 1500MSPS (decimate by 2x), External clock mode , A_{IN} = –3 dBFS, DSA setting = 3 dB.



100MHz Tone Spacing

図 6-218. RX IMD3 vs DSA Setting at 6.851GHz

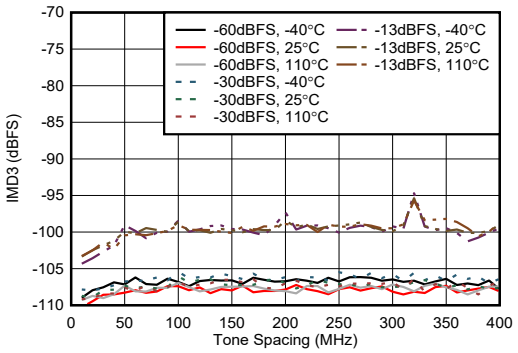


図 6-219. RX IMD3 vs Tone Spacing at 6.851GHz

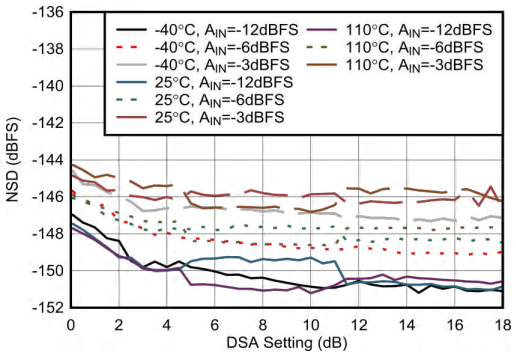


図 6-220. RX NSD vs DSA Setting at 6.851GHz

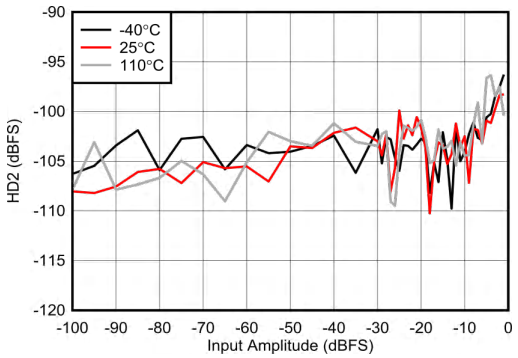
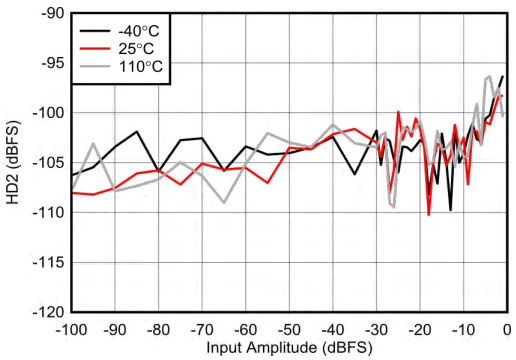
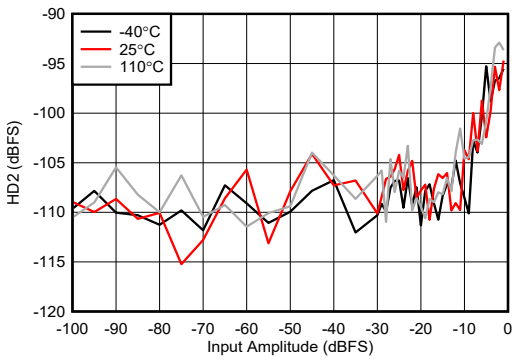


図 6-221. RX HD2 vs Input Amplitude at 6.851GHz



DSA = 0dB

図 6-222. RX HD2 vs Input Amplitude at 6.851GHz



DSA = 12dB

図 6-223. RX HD2 vs Input Amplitude at 6.851GHz

6.11.7 RX Typical Characteristics 6.8GHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 3000MSPS, output sample rate = 1500MSPS (decimate by 2x), External clock mode , A_{IN} = –3 dBFS, DSA setting = 3 dB.

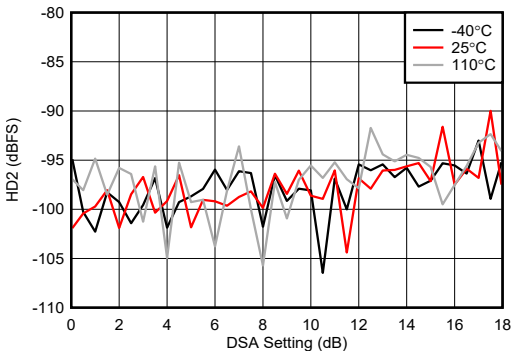


図 6-224. RX HD2 vs DSA Setting at 6.851GHz

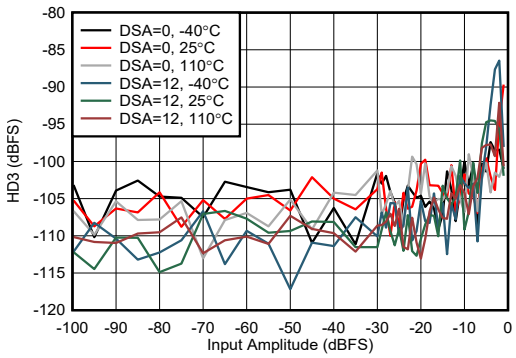


図 6-225. RX HD3 vs Input Amplitude at 6.851GHz

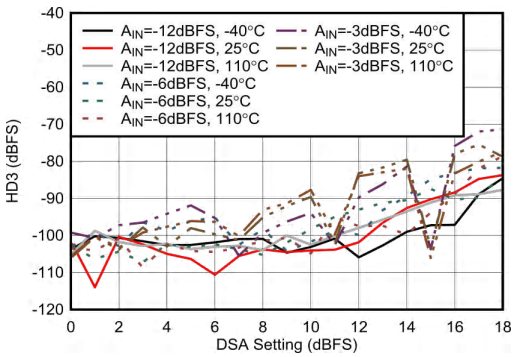
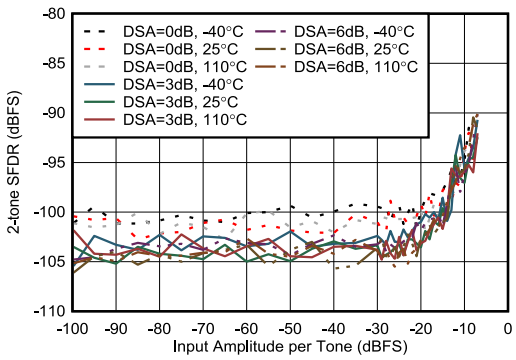


図 6-226. RX HD3 vs DSA Setting at 6.851GHz



100MHz tone spacing, excluding 3rd order distortion

図 6-227. RX 2-tone SFDR vs Input Amplitude at 6.85GHz

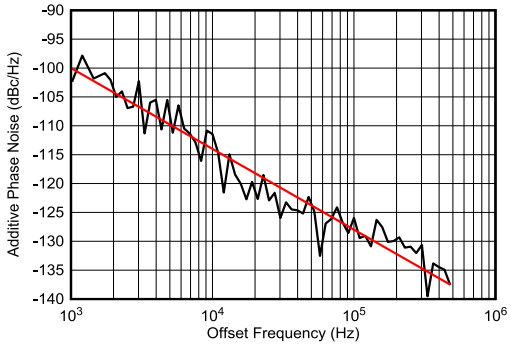
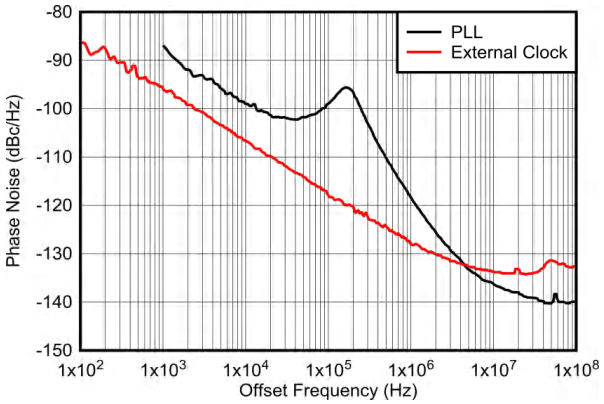


図 6-228. RX Additive Phase Noise at 6.85GHz

6.11.8 PLL and Clock Typical Characteristics

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, f_{REF} = 491.52 MHz, Phase noise measured at TX output



measured at TX output, normalized to 12GHz by 20*log10(12GHz/F_{OUT})

図 6-229. Phase Noise vs Offset Frequency for PLL and External Clock at 12GHz

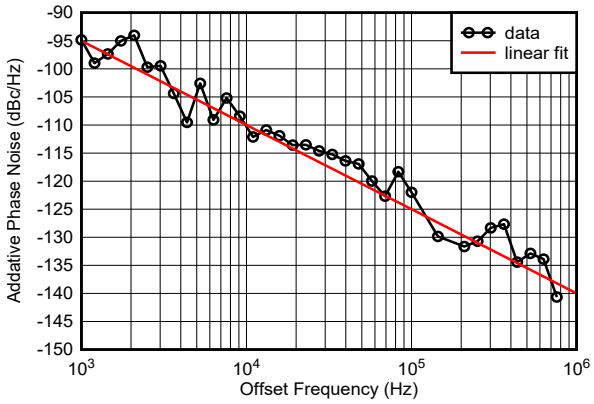
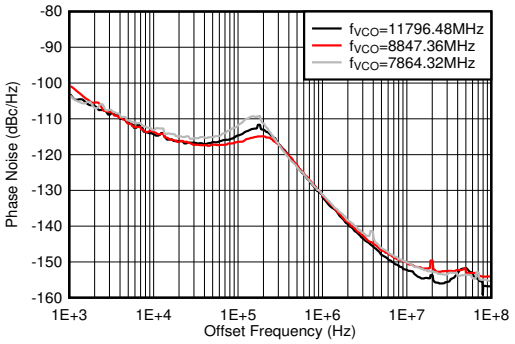
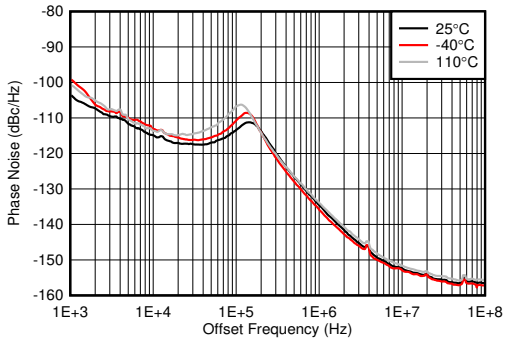


図 6-230. RX Addative Phase Noise at 9.61GHz



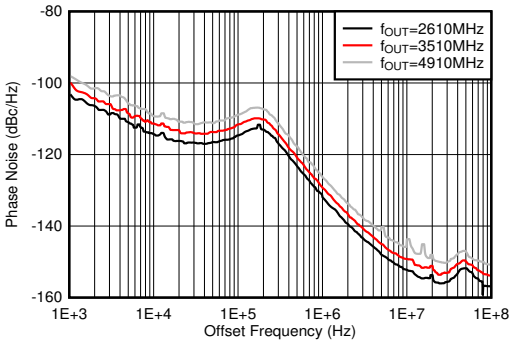
PLL enabled, f_{REF} = 491.52MSPS, measured at 2TXOUT

図 6-231. Phase Noise vs Offset Frequency and f_{VCO} at f_{OUT} = 2610 MHz



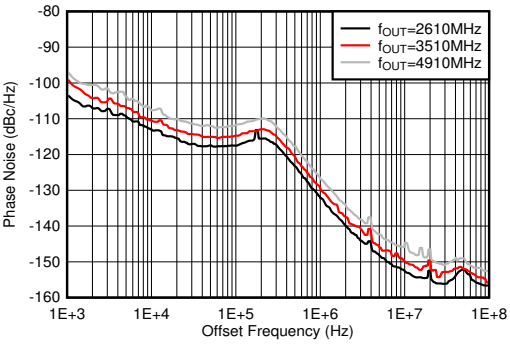
PLL enabled, f_{VCO} = 11796.48 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

図 6-232. Phase Noise for 12-GHz VCO vs Offset Frequency and Temperature at f_{OUT} = 1910 MHz



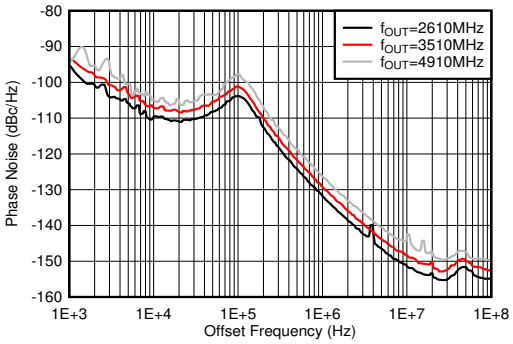
PLL enabled, f_{VCO} = 11796.48 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

図 6-233. Phase Noise for 12-GHz VCO vs Offset Frequency and f_{OUT} at 25°C



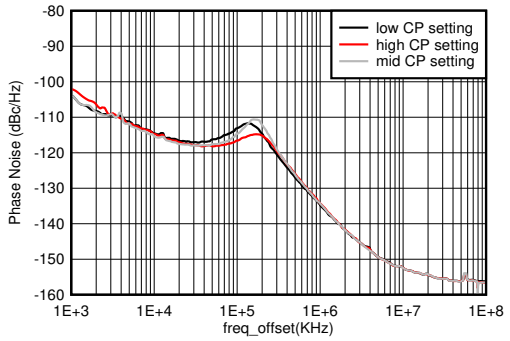
PLL enabled, f_{VCO} = 11796.48 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

図 6-234. Phase Noise for 12-GHz VCO vs Offset Frequency and f_{OUT} at –40°C



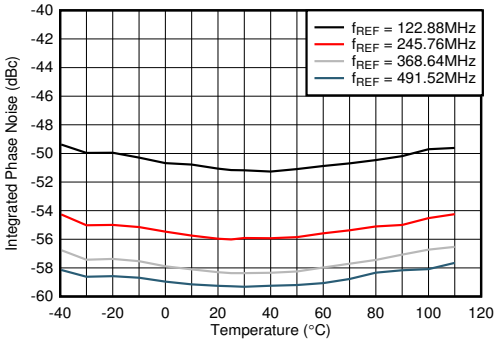
PLL enabled, f_{VCO} = 11796.48 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

図 6-235. Phase Noise for 12-GHz VCO vs Offset Frequency and f_{OUT} at 110°C



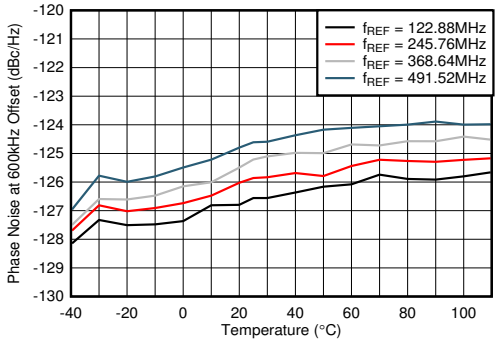
PLL enabled, f_{VCO} = 11796.48 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

図 6-236. Phase Noise for 12-GHz VCO vs Offset Frequency and CP Setting at f_{OUT} = 2.6 GHz



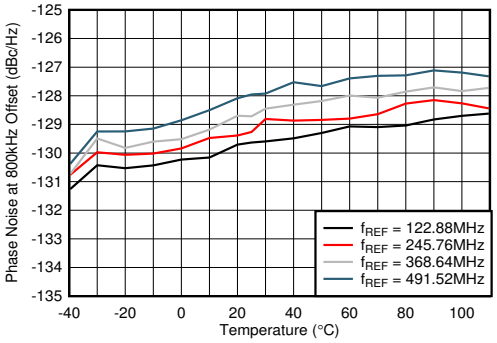
PLL enabled, f_{VCO} = 11796.48 MHz, 1-kHz to 100-MHz, single-sided integration bandwidth, measured at 2TXOUT

図 6-237. Integrated Phase Noise for 12-GHz VCO vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



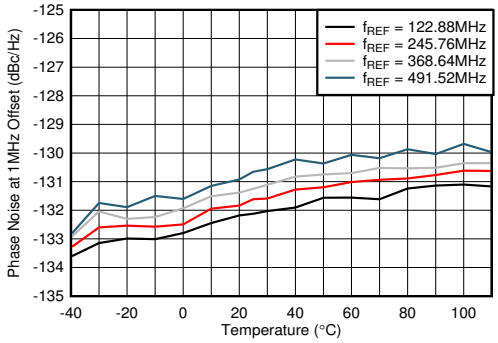
PLL enabled, f_{VCO} = 11796.48 MHz, measured at 2TXOUT

図 6-238. Phase Noise for 12-GHz VCO at 600kHz Offset vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



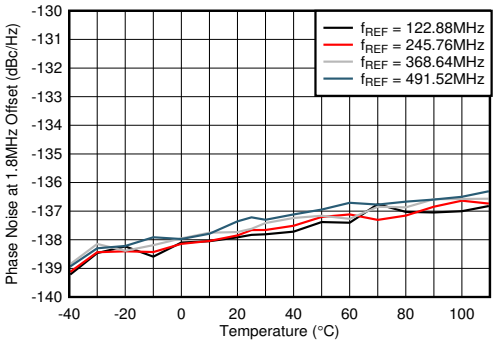
A. PLL enabled, f_{VCO} = 11796.48 MHz, measured at 2TXOUT

図 6-239. Phase Noise for 12-GHz VCO at 800-kHz Offset vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



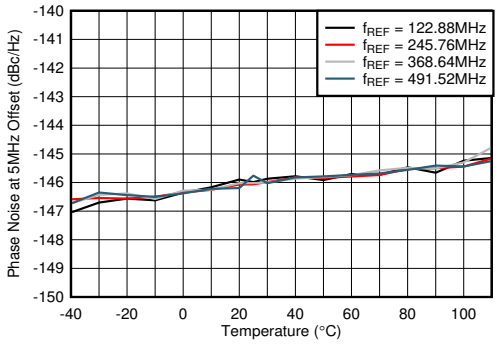
PLL enabled, f_{VCO} = 11796.48 MHz, measured at 2TXOUT

図 6-240. Phase Noise for 12-GHz VCO at 1-MHz Offset vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



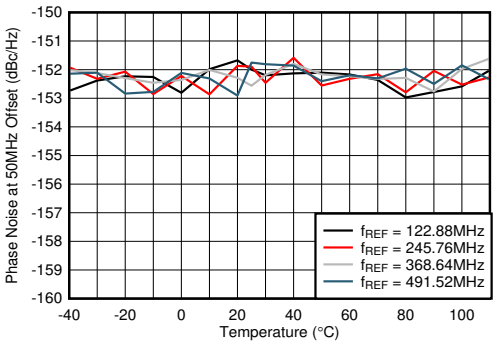
PLL enabled, f_{VCO} = 11796.48 MHz, measured at 2TXOUT

図 6-241. Phase Noise for 12-GHz VCO at 1.8-MHz Offset vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



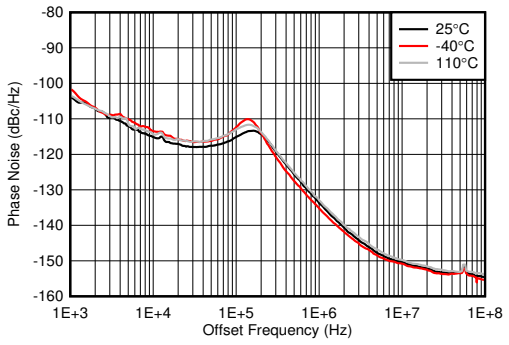
PLL enabled, f_{VCO} = 11796.48 MHz, measured at 2TXOUT

図 6-242. Phase Noise for 12-GHz VCO at 5-MHz Offset vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



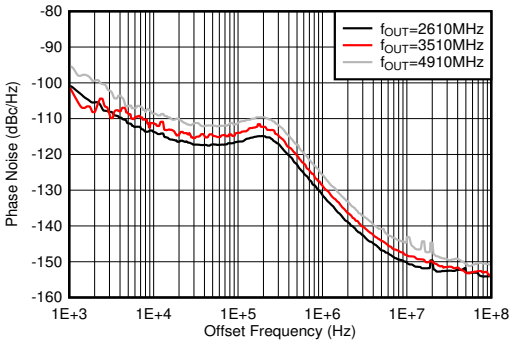
PLL enabled, f_{VCO} = 11796.48 MHz, measured at 2TXOUT

図 6-243. Phase Noise for 12-GHz VCO at 50-MHz Offset vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



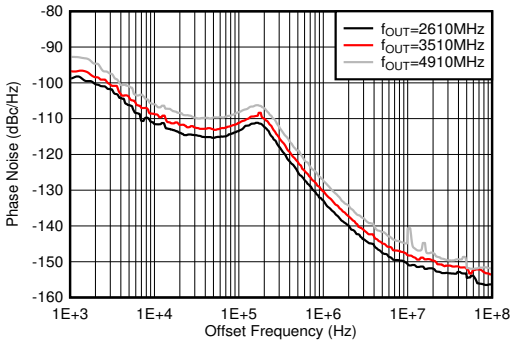
PLL enabled, f_{VCO} = 9830.4 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

図 6-244. Phase Noise for 10-GHz VCO vs Offset Frequency and Temperature at f_{OUT} = 1910 MHz



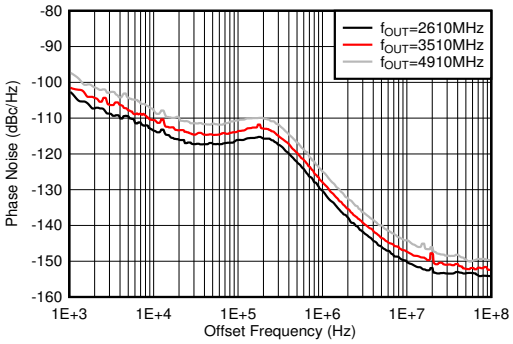
PLL enabled, f_{VCO} = 9830.4 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

図 6-245. Phase Noise for 10-GHz VCO vs Offset Frequency and f_{OUT} at 25°C



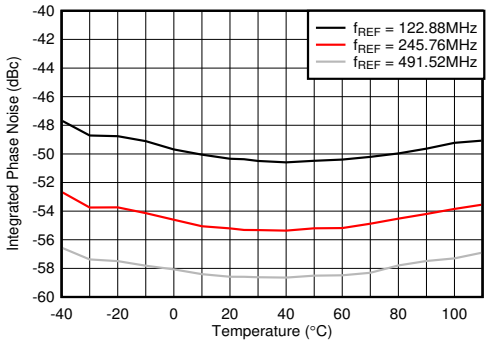
PLL enabled, f_{VCO} = 9830.4 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

図 6-246. Phase Noise for 10-GHz VCO vs Offset Frequency and f_{OUT} at –40°C



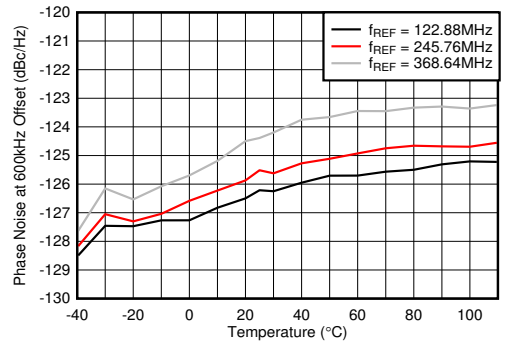
PLL enabled, f_{VCO} = 9830.4 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

図 6-247. Phase Noise for 10-GHz VCO vs Offset Frequency and f_{OUT} at 110°C



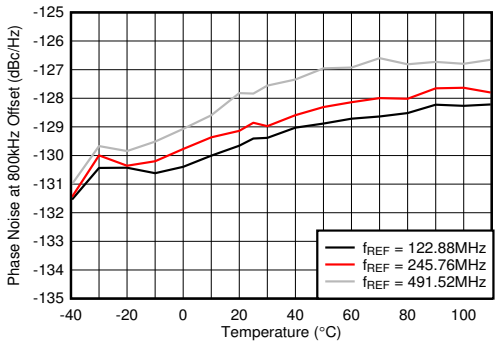
PLL enabled, f_{VCO} = 9830.4 MHz, 1-kHz to 100-MHz, single-sided integration bandwidth, measured at 2TXOUT

図 6-248. Integrated Phase Noise for 10-GHz VCO vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



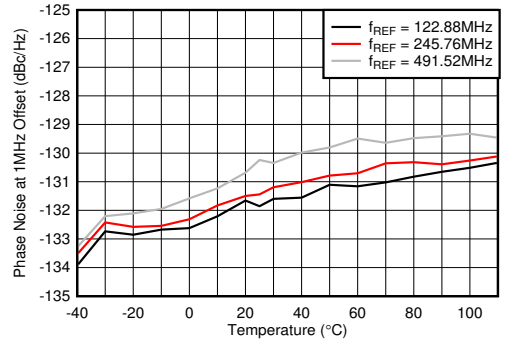
PLL enabled, f_{VCO} = 9830.4 MHz, measured at 2TXOUT

図 6-249. Phase Noise for 10-GHz VCO at 600 kHz vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



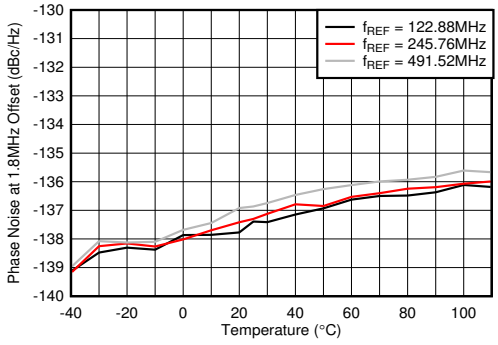
PLL enabled, f_{VCO} = 9830.4 MHz, measured at 2TXOUT

図 6-250. Phase Noise for 10-GHz VCO at 800 kHz vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



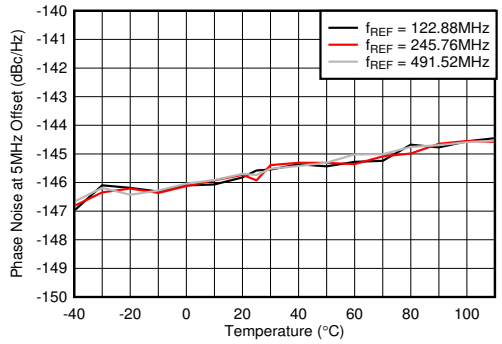
PLL enabled, f_{VCO} = 9830.4 MHz, measured at 2TXOUT

図 6-251. Phase Noise for 10-GHz VCO at 1 MHz vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



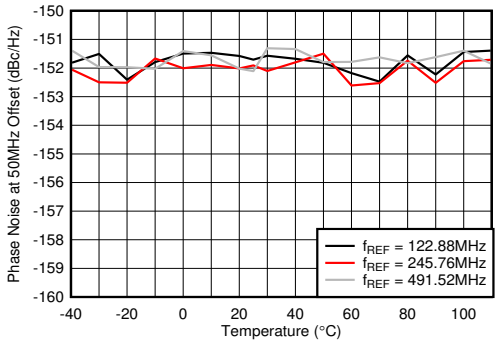
PLL enabled, f_{VCO} = 9830.4 MHz, measured at 2TXOUT

図 6-252. Phase Noise for 10-GHz VCO at 1.8 MHz vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



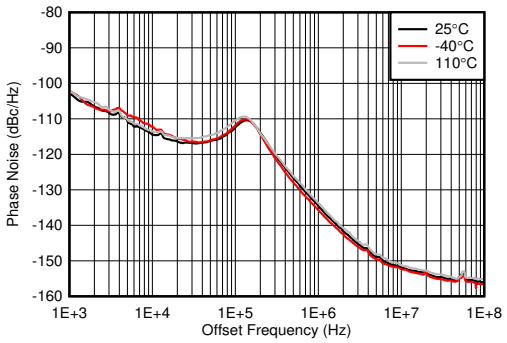
PLL enabled, f_{VCO} = 9830.4 MHz, measured at 2TXOUT

図 6-253. Phase Noise for 10-GHz VCO at 5 MHz vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



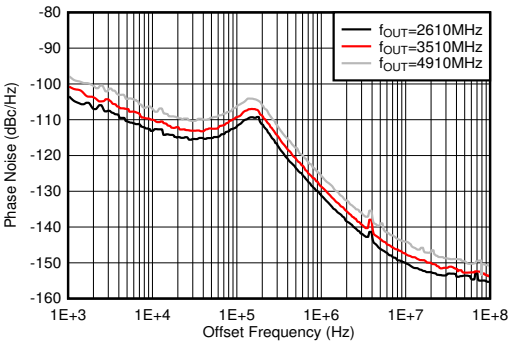
PLL enabled, f_{VCO} = 9830.4 MHz, measured at 2TXOUT

図 6-254. Phase Noise for 10-GHz VCO at 50 MHz vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



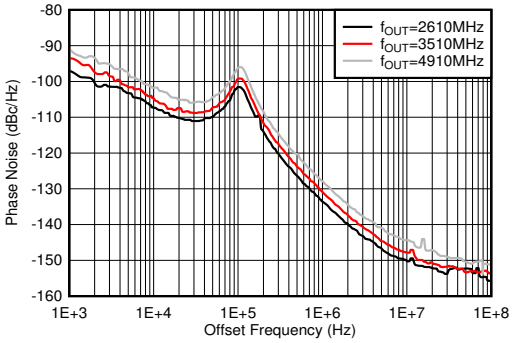
PLL enabled, f_{VCO} = 8847.36 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

図 6-255. Phase Noise for 9-GHz VCO vs Offset Frequency and Temperature at f_{OUT} = 1910 MHz



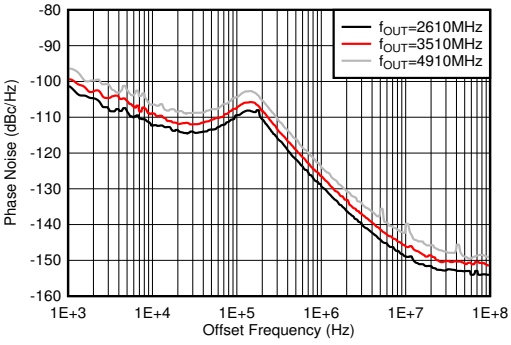
PLL enabled, f_{VCO} = 8847.36 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

図 6-256. Phase Noise for 9-GHz VCO vs Offset Frequency and f_{OUT} at 25°C



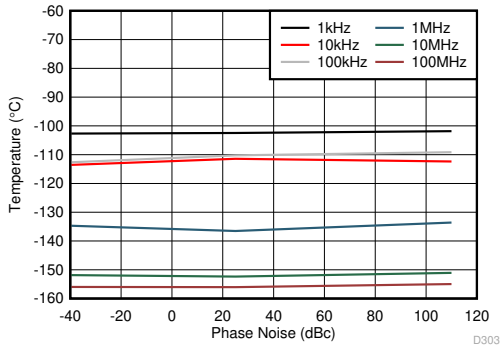
PLL enabled, f_{VCO} = 8847.36 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

図 6-257. Phase Noise for 9-GHz VCO vs Offset Frequency and f_{OUT} at –40°C



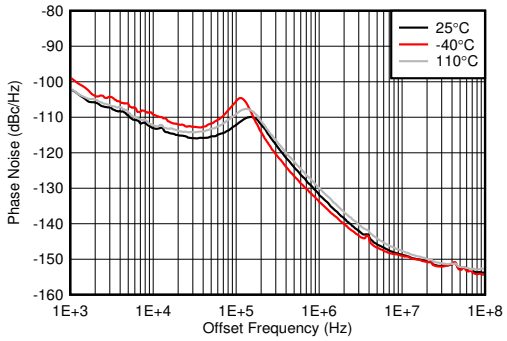
PLL enabled, f_{VCO} = 8847.36 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

図 6-258. Phase Noise for 9-GHz VCO vs Offset Frequency and f_{OUT} at 110°C



PLL enabled, f_{VCO} = 8847.36 MHz, f_{REF} = 491.52MSPS, minimum LPF BW, measured at 2TXOUT

図 6-259. Phase Noise for 9-GHz VCO vs Temperature Over Offset Frequency at f_{OUT} = 2.6 GHz



PLL enabled, f_{VCO} = 7864.32 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

図 6-260. Phase Noise for 8-GHz VCO vs Offset Frequency and Temperature at f_{OUT} = 1910 MHz

7 Device and Documentation Support

7.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

7.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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7.3 Trademarks

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7.4 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

7.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AFE7906IABJ	ACTIVE	FCBGA	ABJ	400	90	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85	AFE7906I	Samples
AFE7906IALK	ACTIVE	FCBGA	ALK	400	90	Non-RoHS & Green	Call TI	Level-3-220C-168 HR	-40 to 85	AFE7906 SNPB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

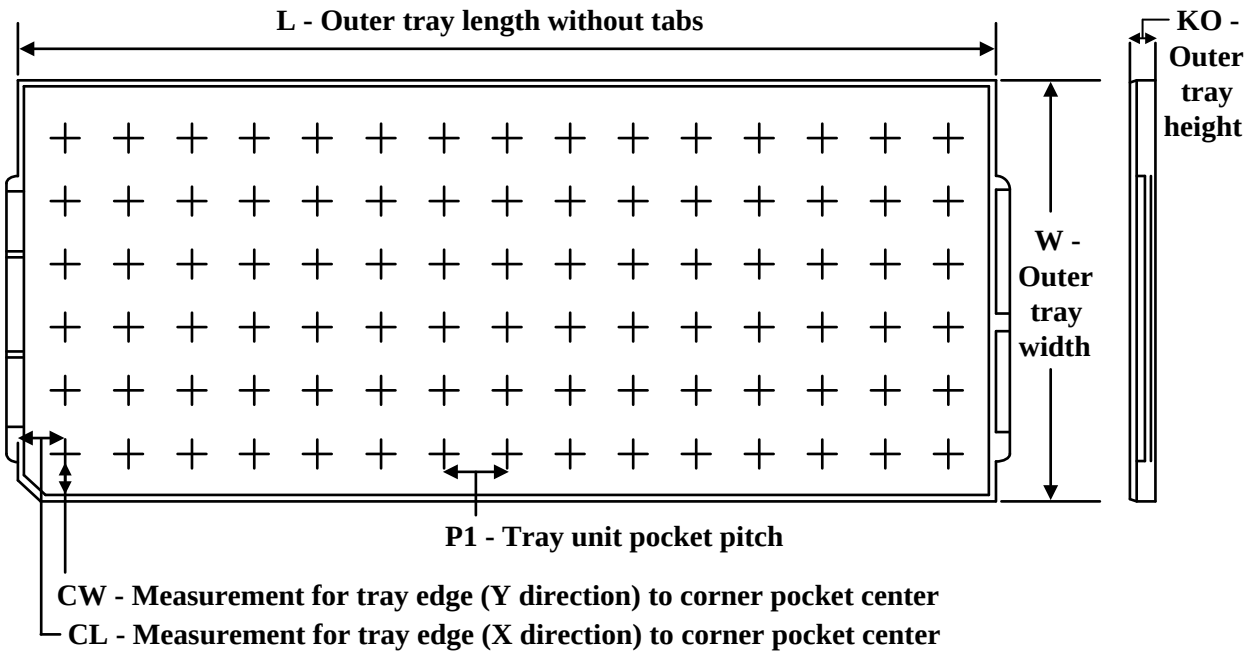
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

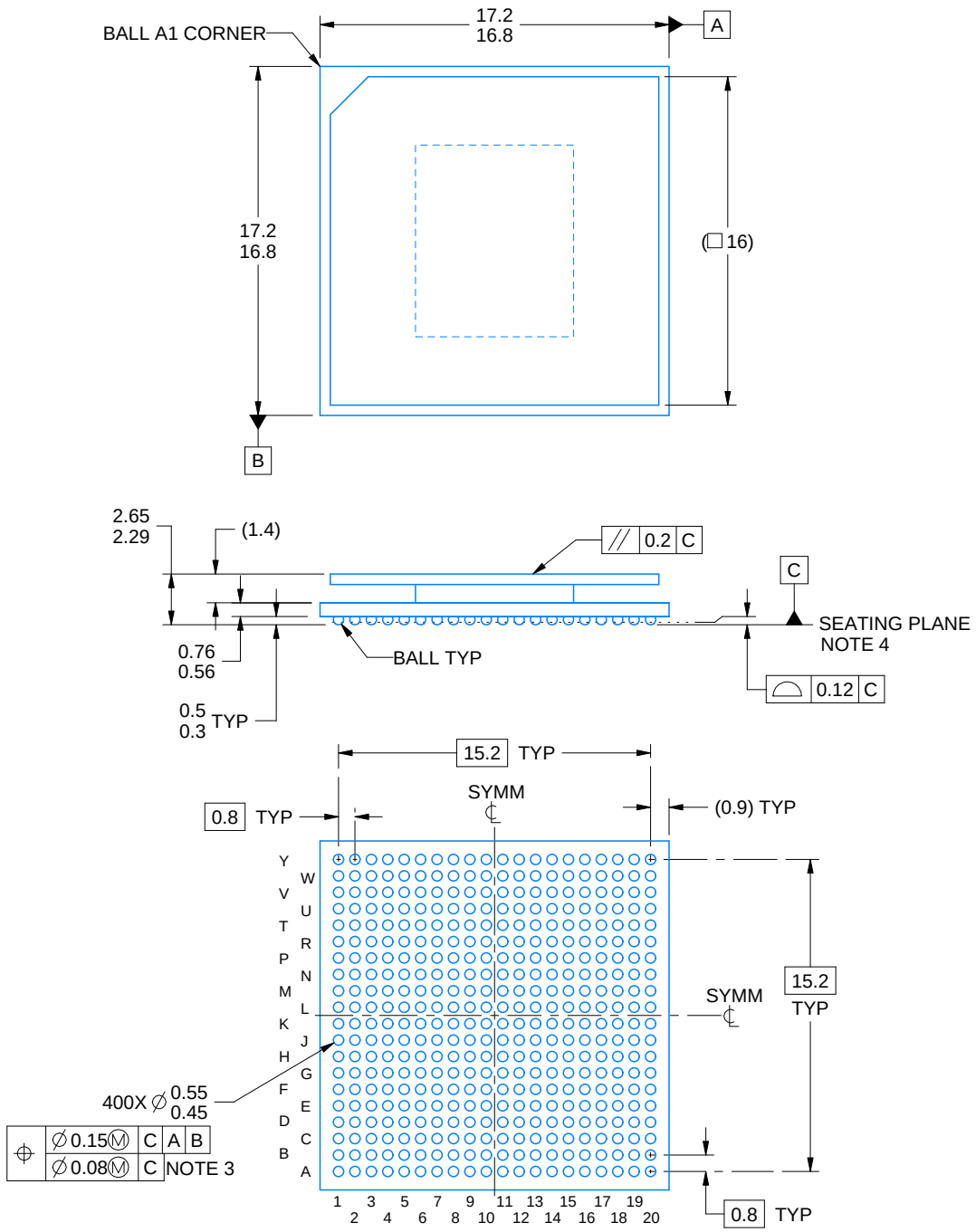
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
AFE7906IABJ	ABJ	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2
AFE7906IABJ	ABJ	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2
AFE7906IALK	ALK	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2
AFE7906IALK	ALK	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2

ALK0400A

PACKAGE OUTLINE

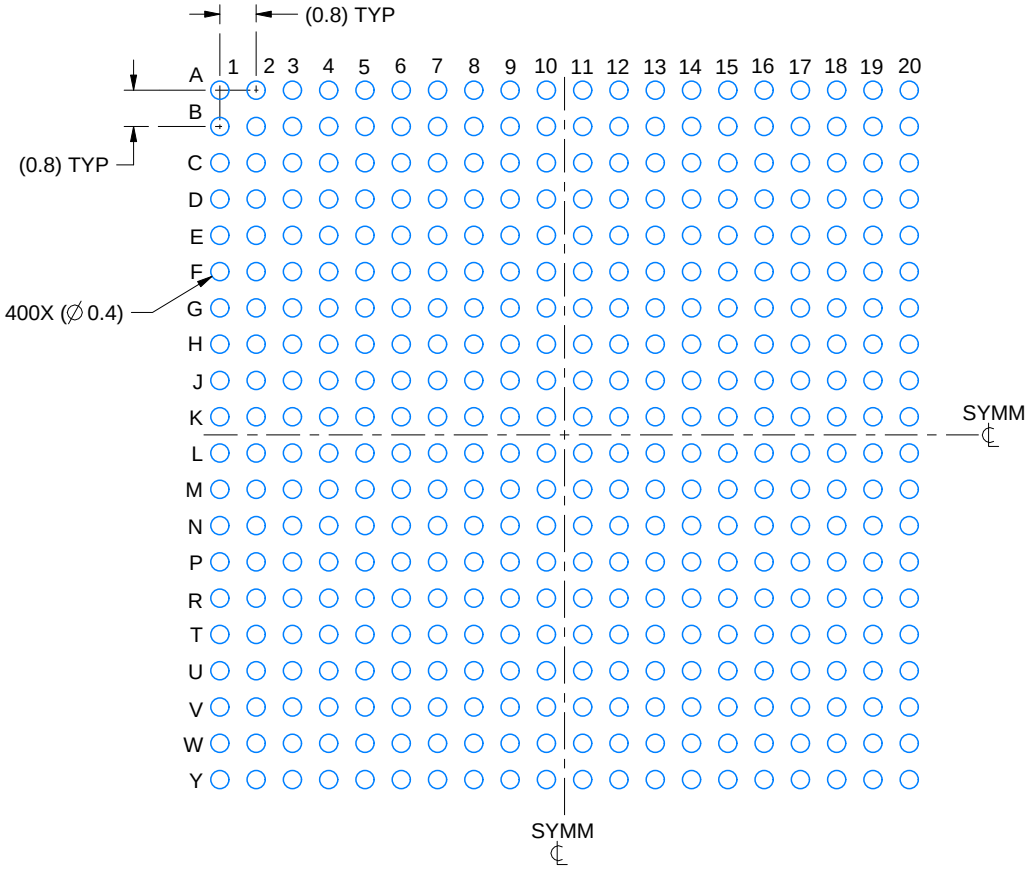
FCBGA - 2.65 mm max height

BALL GRID ARRAY

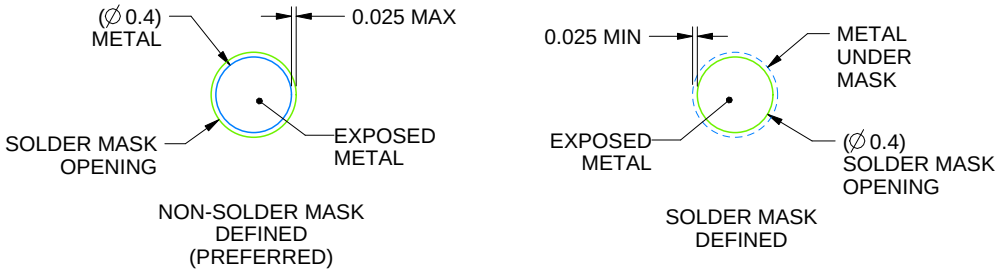


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
5. Pb-Free die bump and SnPb solder ball.
6. The lids are electrically floating (e.g. not tied to GND).



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

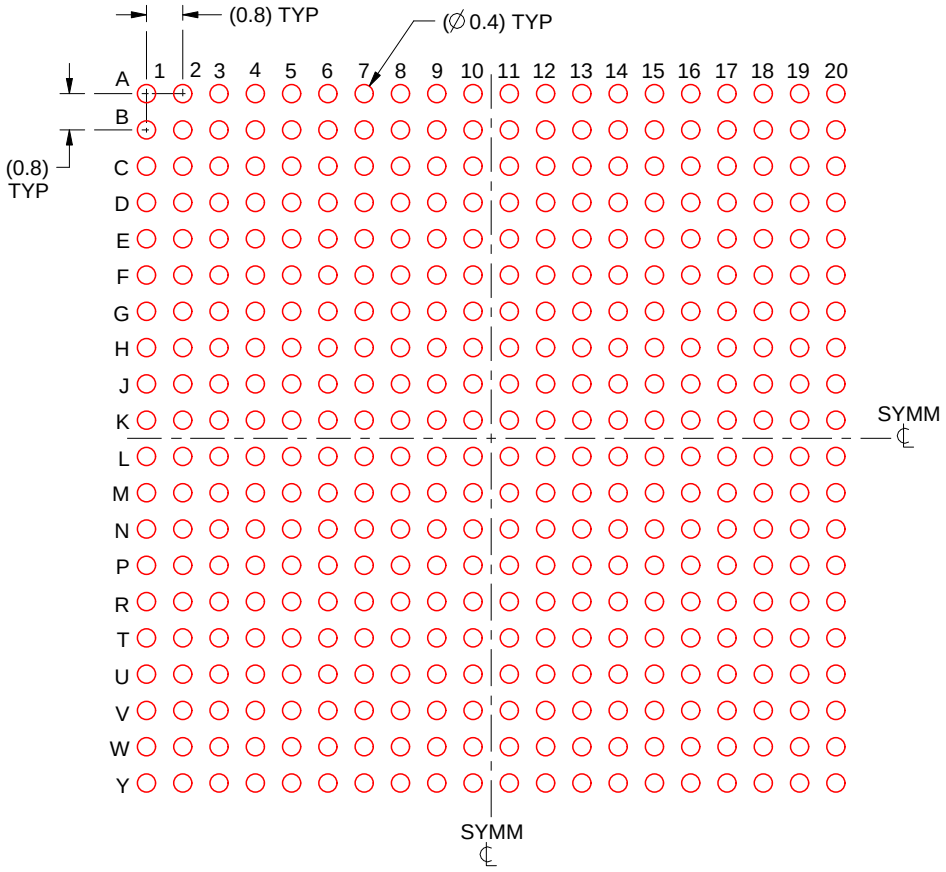


SOLDER MASK DETAILS
NOT TO SCALE

4225930/C 03/2023

NOTES: (continued)

7. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 (www.ti.com/lit/spru811).



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:6X

4225930/C 03/2023

NOTES: (continued)

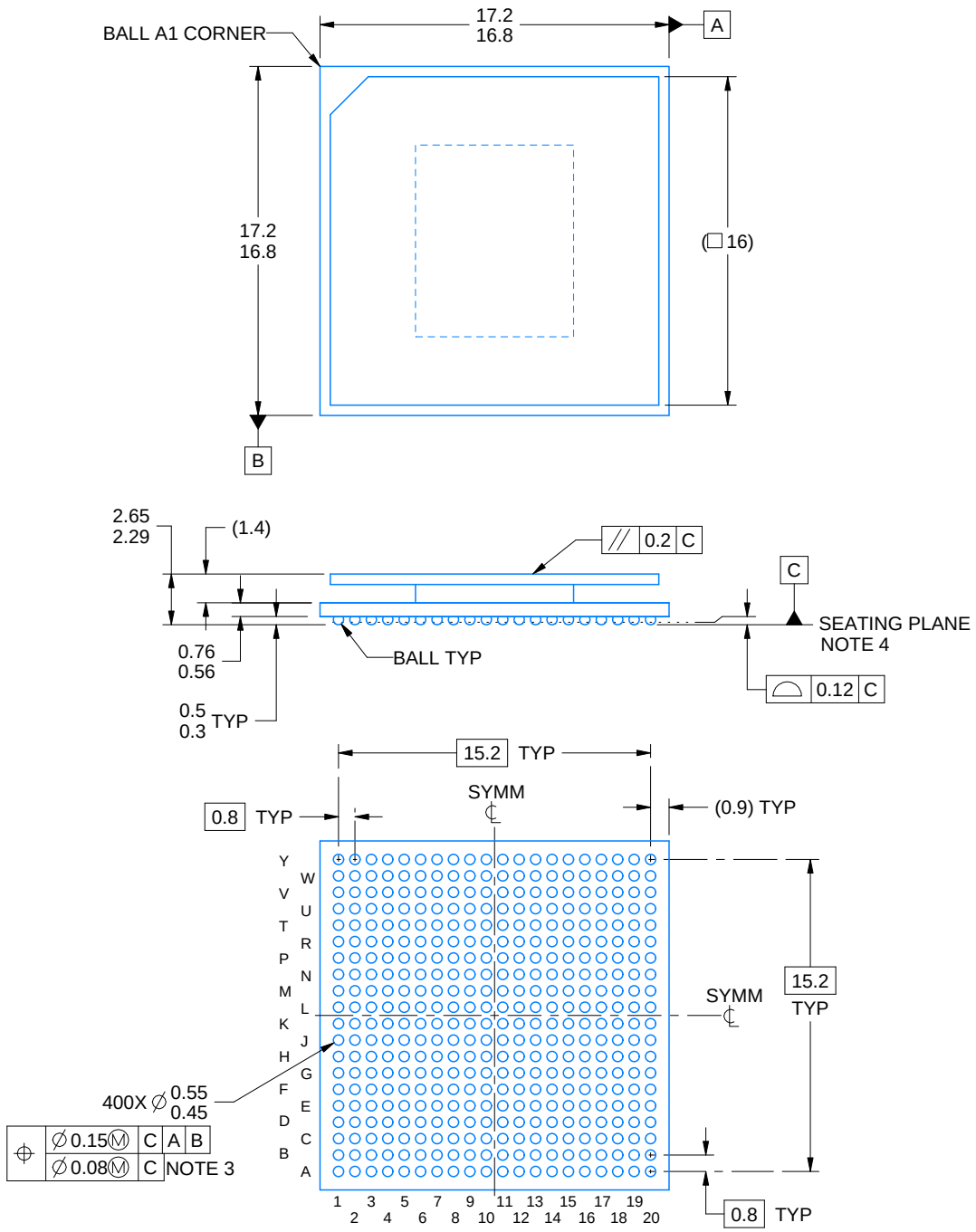
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

ABJ0400A

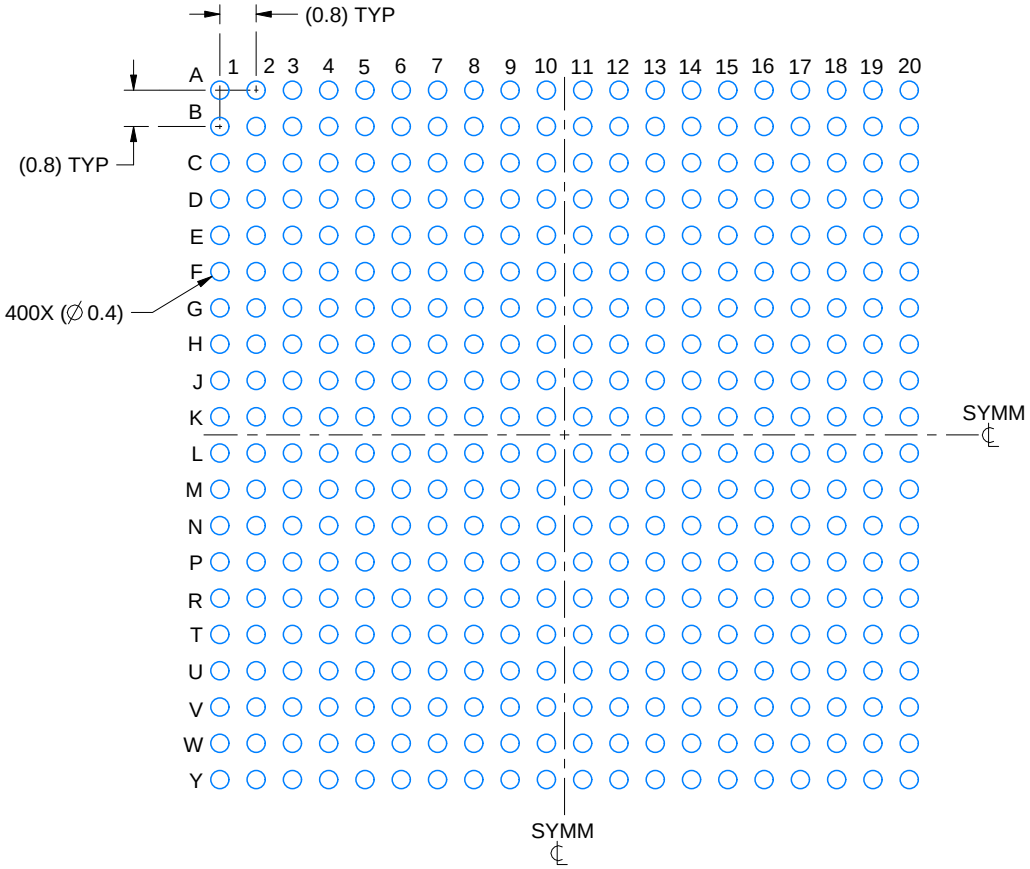
FCBGA - 2.65 mm max height

BALL GRID ARRAY

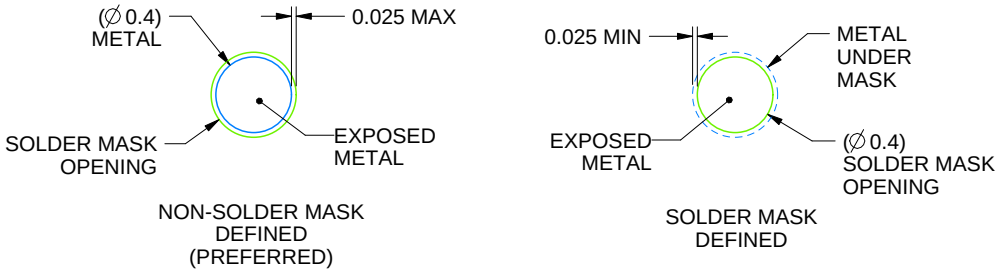


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
5. The lids are electrically floating (e.g. not tied to GND).



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

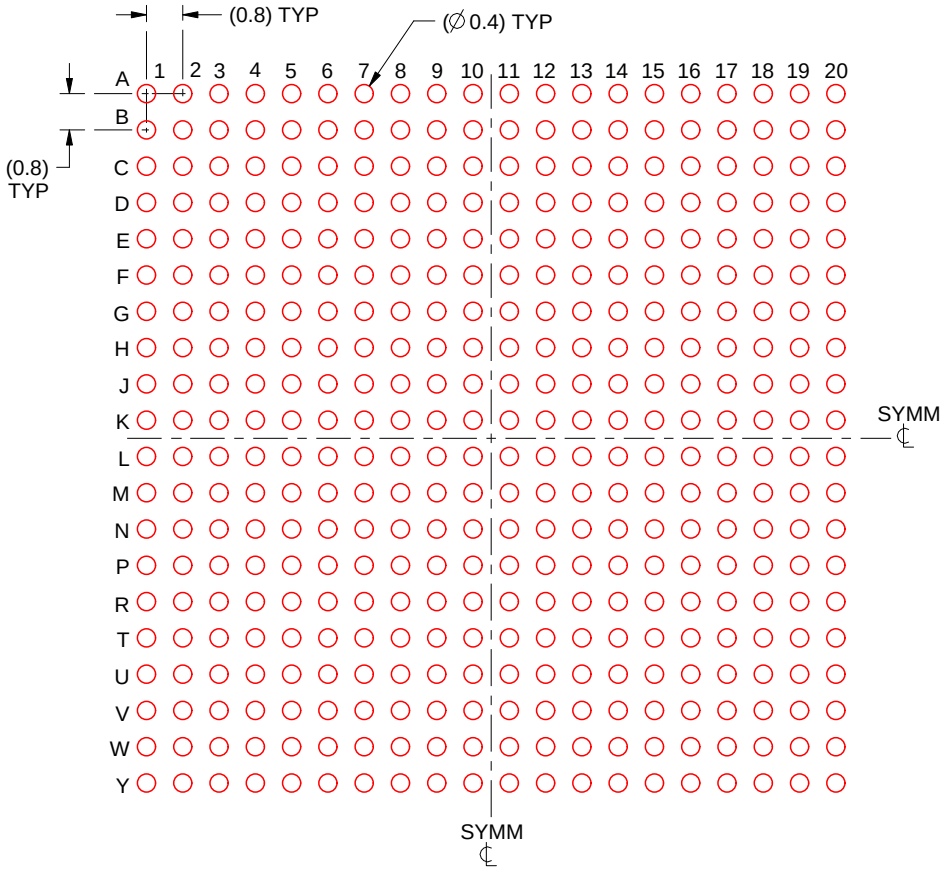


SOLDER MASK DETAILS
NOT TO SCALE

4221311/D 03/2023

NOTES: (continued)

6. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 (www.ti.com/lit/spru811).



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:6X

4221311/D 03/2023

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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