

# AM26C31 クワッド差動ラインドライバ

## 1 特長

- TIA/EIA-422-B と ITU 勧告 V.11 の要件を満たす、または上回る性能
- 低消費電力、 $I_{CC} = 100\mu\text{A}$  (標準値)
- 5V 単一電源で動作
- 高速、 $t_{PLH} = t_{PHL} = 7\text{ns}$  (標準値)
- 小さいパルス歪み、 $t_{sk(p)} = 0.5\text{ns}$  (標準値)
- 電源オフ状況での高い出力インピーダンス
- AM26LS31 デバイスの改良代替品
- 車載対応 Q-Temp で利用可能
  - 高信頼性の車載用アプリケーション
  - 構成制御と印刷のサポート
  - 車載用規格の認定
- MIL-PRF-38535 準拠の製品については、特に記述のない限り、すべてのパラメータはテスト済みです。その他のすべての製品については、量産プロセスにすべてのパラメータのテストが含まれているとは限りません。

## 2 アプリケーション

- 化学およびガス センサ
- フィールドトランスミッタ: 温度センサおよび圧力センサ
- 軍事: レーダー / ソナー
- モータ制御: ブラシレス DC およびブラシ付き DC
- 軍事 / 航空電子機器用の画像処理
- Modbus 使用の温度センサおよびコントローラ

## 3 概要

AM26C31 デバイスは、相補出力を備えた差動ラインドライバであり、TIA/EIA-422-B と ITU (以前の CCITT) の要件を満たすように設計されています。3 ステート出力は、ツイストペアまたは平行線伝送線路などの平衡ラインを駆動するための大電流能力を備え、電源オフ時には高インピーダンス状態になります。イネーブル機能は 4 つのドライバのすべてに共通しており、アクティブ High またはアクティブ Low のイネーブル ( $\overline{G}$ ,  $\overline{G}$ ) 入力を選択できます。BiCMOS 回路により、速度を犠牲にすることなく消費電力を低減しています。

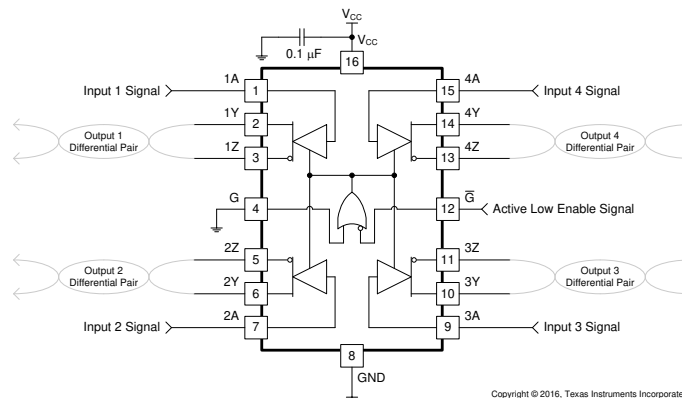
AM26C31C デバイスは  $0^{\circ}\text{C} \sim +70^{\circ}\text{C}$  で動作特性が規定されており、AM26C31I デバイスは  $-40^{\circ}\text{C} \sim +85^{\circ}\text{C}$  で動作特性が規定されています。AM26C31Q デバイスは車載温度範囲 ( $-40^{\circ}\text{C} \sim +125^{\circ}\text{C}$ ) で動作特性が規定されており、AM26C31M デバイスは防衛用温度範囲 ( $-55^{\circ}\text{C} \sim +125^{\circ}\text{C}$ ) で動作特性が規定されています。

### パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ (2)
AM26C31	CDIP (J, 16)	19.56mm × 6.92mm
	PDIP (N, 16)	19.3mm × 6.35mm
	SO (NS, 16)	10.3mm × 5.3mm
	CFP (W, 16)	10.3mm × 6.73mm
	SOIC (D, 16)	9.9mm × 3.91mm
	SSOP (DB, 16)	6.2mm × 5.3mm
	TSSOP (PW, 16)	5.0mm × 4.4mm
	LCCC (FK, 20)	8.89mm × 8.89mm

(1) 詳細については、[セクション 11](#) を参照してください。

(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



一般的なアプリケーション図



## Table of Contents

<b>1 特長</b> .....	<b>1</b>	<b>7 Detailed Description</b> .....	<b>11</b>
<b>2 アプリケーション</b> .....	<b>1</b>	7.1 Overview.....	11
<b>3 概要</b> .....	<b>1</b>	7.2 Functional Block Diagrams.....	11
<b>4 Pin Configuration and Functions</b> .....	<b>3</b>	7.3 Feature Description.....	12
<b>5 Specifications</b> .....	<b>4</b>	7.4 Device Functional Modes.....	12
5.1 Absolute Maximum Ratings.....	4	<b>8 Application Information Disclaimer</b> .....	<b>13</b>
5.2 ESD Ratings.....	4	8.1 Application Information.....	13
5.3 Recommended Operating Conditions.....	4	8.2 Typical Application.....	13
5.4 Thermal Information.....	5	8.3 Power Supply Recommendations.....	14
5.5 Electrical Characteristics: AM26C31C and AM26C31I.....	5	8.4 Layout.....	14
5.6 Electrical Characteristics: AM26C31Q and AM26C31M.....	6	<b>9 Device and Documentation Support</b> .....	<b>16</b>
5.7 Switching Characteristics: AM26C31C and AM26C31I.....	6	9.1 ドキュメントの更新通知を受け取る方法.....	16
5.8 Switching Characteristics: AM26C31Q and AM26C31M.....	7	9.2 サポート・リソース.....	16
5.9 Typical Characteristics.....	7	9.3 Trademarks.....	16
<b>6 Parameter Measurement Information</b> .....	<b>8</b>	9.4 静電気放電に関する注意事項.....	16
		9.5 用語集.....	16
		<b>10 Revision History</b> .....	<b>16</b>
		<b>11 Mechanical, Packaging, and Orderable Information</b> .....	<b>17</b>

## 4 Pin Configuration and Functions

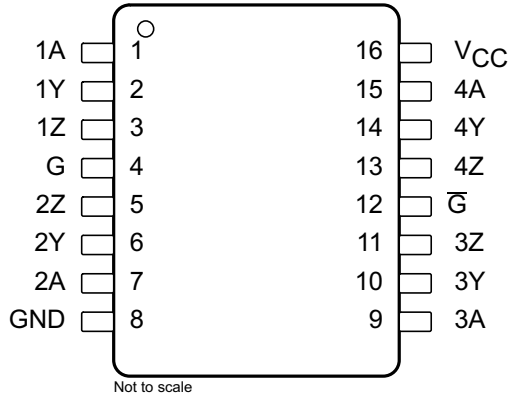


図 4-1. J (CDIP), W (CFP), D (SOIC), DB (SSOP), NS (SO), N (PDIP), or PW (TSSOP) Package 16-Pin (Top View)

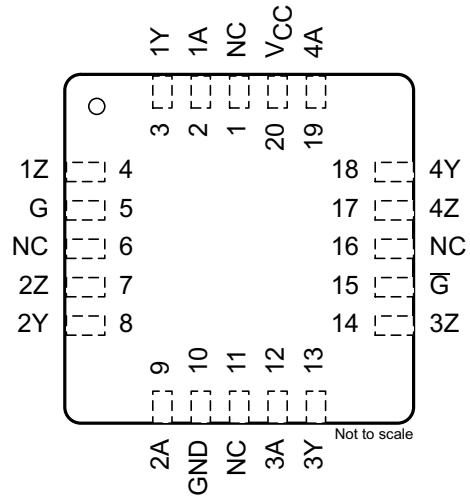


図 4-2. FK (LCCC) Package, 20-Pin (Top View)

表 4-1. Pin Functions

NAME	PIN		TYPE	DESCRIPTION
	CDIP, CFP, SOIC, SSOP, SO, PDIP, TSSOP	LCCC		
1A	1	2	I	Driver 1 input
1Y	2	3	O	Driver 1 output
1Z	3	4	O	Driver 1 inverted output
2A	7	9	I	Driver 2 input
2Y	6	8	O	Driver 2 output
2Z	5	7	O	Driver 2 inverted output
3A	9	12	I	Driver 3 input
3Y	10	13	O	Driver 3 output
3Z	11	14	O	Driver 3 inverted output
4A	15	19	I	Driver 3 input
4Y	14	18	O	Driver 3 output
4Z	13	17	O	Driver 3 inverted output
G	4	5	I	Active high enable
G-bar	12	15	I	Active low enable
GND	8	10	—	Ground pin
NC <sup>(1)</sup>	—	1, 6, 11, 16	—	No internal connection
V <sub>CC</sub>	16	20	—	Power pin

(1) NC – No connection

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage <sup>(2)</sup>	-0.5	7	V
V <sub>I</sub>	Input voltage	-0.5	V <sub>CC</sub> + 0.5	V
V <sub>ID</sub>	Differential input voltage	-14	14	V
V <sub>O</sub>	Output voltage	-0.5	7	V
I <sub>IK</sub> I <sub>OK</sub>	Input or output clamp current		±20	mA
I <sub>O</sub>	Output current		±150	mA
	V <sub>CC</sub> current		200	mA
	GND current	-200		mA
T <sub>J</sub>	Operating virtual junction temperature		150	°C
T <sub>stg</sub>	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to the network ground terminal.

### 5.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage		4.5	5	5.5	V
V <sub>ID</sub>	Differential input voltage			±7		V
V <sub>IH</sub>	High-level input voltage		2			V
V <sub>IL</sub>	Low-level input voltage				0.8	V
I <sub>OH</sub>	High-level output current				-20	mA
I <sub>OL</sub>	Low-level output current				20	mA
T <sub>A</sub>	Operating free-air temperature	AM26C31C	0		70	°C
		AM26C31I	-40		85	
		AM26C31Q	-40		125	
		AM26C31M	-55		125	

## 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	AM26C31									UNIT
	D (SOIC)	DB (SSOP)	PW (TSSOP)	NS (SO)	N (PDIP)	J (CDIP)	W (CFP)	FK (LCCC)		
	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance <sup>(2) (3)</sup>	84.6	102.6	107.5	88.5	60.6	—	—	—	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	43.5	48.7	38.4	46.2	48.1	39.3 <sup>(4)</sup>	58.9 <sup>(4)</sup>	37.1 <sup>(4)</sup>	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	43.2	54.3	53.7	50.7	40.6	56.4 <sup>(4)</sup>	109.3 <sup>(4)</sup>	36.2 <sup>(4)</sup>	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	10.4	11.8	3.2	13.5	27.5	—	—	—	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	42.8	53.5	53.1	50.3	40.3	—	—	—	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	n/a	n/a	12 <sup>(4)</sup>	5.7 <sup>(4)</sup>	4.3 <sup>(4)</sup>	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.
- (2) Maximum power dissipation is a function of T<sub>J(max)</sub>, R<sub>θJA</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any allowable ambient temperature is P<sub>D</sub> = (T<sub>J(max)</sub> – T<sub>A</sub>) / R<sub>θJA</sub>. Operating at the absolute maximum T<sub>J</sub> of 150°C can affect reliability.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.
- (4) Modelling assumption: MIL-STD-883 for R<sub>θJC(top)</sub> and R<sub>θJC(bot)</sub> JESD51 for R<sub>θJB</sub>.

## 5.5 Electrical Characteristics: AM26C31C and AM26C31I

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP <sup>(1)</sup>	MAX	UNIT	
V <sub>OH</sub>	High-level output voltage	I <sub>O</sub> = –20mA		2.4	3.4		V	
V <sub>OL</sub>	Low-level output voltage	I <sub>O</sub> = 20mA			0.2	0.4	V	
V <sub>OD</sub>	Differential output voltage magnitude	R <sub>L</sub> = 100Ω, see <a href="#">6-1</a>		2	3.1		V	
Δ V <sub>OD</sub>	Change in magnitude of differential output voltage <sup>(2)</sup>	R <sub>L</sub> = 100Ω, see <a href="#">6-1</a>				±0.4	V	
V <sub>OC</sub>	Common-mode output voltage	R <sub>L</sub> = 100Ω, see <a href="#">6-1</a>				3	V	
Δ V <sub>OC</sub>	Change in magnitude of common-mode output voltage <sup>(2)</sup>	R <sub>L</sub> = 100Ω, see <a href="#">6-1</a>				±0.4	V	
I <sub>I</sub>	Input current	V <sub>I</sub> = V <sub>CC</sub> or GND				±1	μA	
I <sub>O(off)</sub>	Driver output current with power off	V <sub>CC</sub> = 0	V <sub>O</sub> = 6V			100	μA	
			V <sub>O</sub> = –0.25V			–100		
I <sub>OS</sub>	Driver output short-circuit current	V <sub>O</sub> = 0		–30		–150	mA	
I <sub>OZ</sub>	High-impedance off-state output current	V <sub>O</sub> = 2.5V				20	μA	
		V <sub>O</sub> = 0.5V				–20		
I <sub>CC</sub>	Quiescent supply current	I <sub>O</sub> = 0	V <sub>I</sub> = 0 or 5V			100	μA	
			V <sub>I</sub> = 2.4V or 0.5V <sup>(3)</sup>			1.5	3	mA
C <sub>i</sub>	Input capacitance					6	pF	

- (1) All typical values are at V<sub>CC</sub> = 5V and T<sub>A</sub> = 25°C.
- (2) Δ|V<sub>OD</sub>| and Δ|V<sub>OC</sub>| are the changes in magnitude of V<sub>OD</sub> and V<sub>OC</sub>, respectively, that occur when the input is changed from a high level to a low level.
- (3) This parameter is measured per input. All other inputs are at 0V or 5V.

## 5.6 Electrical Characteristics: AM26C31Q and AM26C31M

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>OH</sub>	High-level output voltage	I <sub>O</sub> = -20mA	2.2	3.4		V
V <sub>OL</sub>	Low-level output voltage	I <sub>O</sub> = 20mA		0.2	0.4	V
V <sub>OD</sub>	Differential output voltage magnitude	R <sub>L</sub> = 100Ω, see <a href="#">6-1</a>	2	3.1		V
Δ V <sub>OD</sub>	Change in magnitude of differential output voltage <sup>(2)</sup>	R <sub>L</sub> = 100Ω, see <a href="#">6-1</a>			±0.4	V
V <sub>OC</sub>	Common-mode output voltage	R <sub>L</sub> = 100Ω, see <a href="#">6-1</a>			3	V
Δ V <sub>OC</sub>	Change in magnitude of common-mode output voltage <sup>(2)</sup>	R <sub>L</sub> = 100Ω, see <a href="#">6-1</a>			±0.4	V
I <sub>I</sub>	Input current	V <sub>I</sub> = V <sub>CC</sub> or GND			±1	μA
I <sub>O(off)</sub>	Driver output current with power off	V <sub>CC</sub> = 0		V <sub>O</sub> = 6V	100	μA
				V <sub>O</sub> = -0.25V	-100	
I <sub>OS</sub>	Driver output short-circuit current	V <sub>O</sub> = 0			-170	mA
I <sub>OZ</sub>	High-impedance off-state output current	V <sub>O</sub> = 2.5V			20	μA
		V <sub>O</sub> = 0.5V			-20	
I <sub>CC</sub>	Quiescent supply current	I <sub>O</sub> = 0		V <sub>I</sub> = 0 or 5V	100	μA
				V <sub>I</sub> = 2.4V or 0.5V <sup>(3)</sup>	3.2	
C <sub>i</sub>	Input capacitance			6		pF

(1) All typical values are at V<sub>CC</sub> = 5V and T<sub>A</sub> = 25°C.

(2) Δ|V<sub>OD</sub>| and Δ|V<sub>OC</sub>| are the changes in magnitude of V<sub>OD</sub> and V<sub>OC</sub>, respectively, that occur when the input is changed from a high level to a low level.

(3) This parameter is measured per input. All other inputs are at 0V or 5V.

## 5.7 Switching Characteristics: AM26C31C and AM26C31I

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
t <sub>PLH</sub>	Propagation delay time, low-to-high-level output	S1 is open, see <a href="#">6-2</a>	3	7	12	ns
t <sub>PHL</sub>	Propagation delay time, high-to-low-level output		3	7	12	
t <sub>sk(p)</sub>	Pulse skew time ( t <sub>PLH</sub> - t <sub>PHL</sub>  )	S1 is open, see <a href="#">6-2</a>		0.5	4	ns
t <sub>r(OD)</sub> , t <sub>f(OD)</sub>	Differential output rise and fall times	S1 is open, see <a href="#">6-3</a>		5	10	ns
t <sub>PZH</sub>	Output enable time to high level	S1 is closed, see <a href="#">6-4</a>		10	19	ns
t <sub>PZL</sub>	Output enable time to low level		10	19		
t <sub>PHZ</sub>	Output disable time from high level	S1 is closed, see <a href="#">6-4</a>		7	16	ns
t <sub>PLZ</sub>	Output disable time from low level		7	16		
C <sub>pd</sub>	Power dissipation capacitance (each driver) <sup>(2)</sup>	S1 is open, see <a href="#">6-2</a>		170		pF

(1) All typical values are at V<sub>CC</sub> = 5V and T<sub>A</sub> = 25°C.

(2) C<sub>pd</sub> is used to estimate the switching losses according to P<sub>D</sub> = C<sub>pd</sub> × V<sub>CC</sub><sup>2</sup> × f, where f is the switching frequency.

## 5.8 Switching Characteristics: AM26C31Q and AM26C31M

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$t_{PLH}$	Propagation delay time, low-to-high-level output	S1 is open, see <a href="#">6-2</a>		7	12	ns
$t_{PHL}$	Propagation delay time, high-to-low-level output			6.5	12	
$t_{sk(p)}$	Pulse skew time ( $t_{PLH} - t_{PHL}$ )	S1 is open, see <a href="#">6-2</a>		0.5	4	ns
$t_{r(OD)}, t_{f(OD)}$	Differential output rise and fall times	S1 is open, see <a href="#">6-3</a>		5	12	ns
$t_{PZH}$	Output enable time to high level	S1 is closed, see <a href="#">6-4</a>		10	19	ns
$t_{PZL}$	Output enable time to low level			10	19	
$t_{PHZ}$	Output disable time from high level	S1 is closed, see <a href="#">6-4</a>		7	16	ns
$t_{PLZ}$	Output disable time from low level			7	16	
$C_{pd}$	Power dissipation capacitance (each driver) <sup>(2)</sup>	S1 is open, see <a href="#">6-2</a>		100		pF

(1) All typical values are at  $V_{CC} = 5V$  and  $T_A = 25^\circ C$ .

(2)  $C_{pd}$  is used to estimate the switching losses according to  $P_D = C_{pd} \times V_{CC}^2 \times f$ , where  $f$  is the switching frequency.

## 5.9 Typical Characteristics

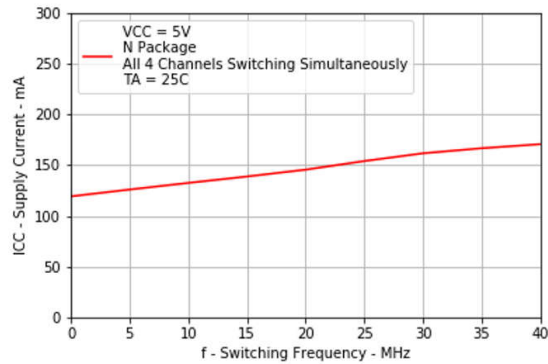


Figure 5-1. Supply Current vs Switching Frequency

## 6 Parameter Measurement Information

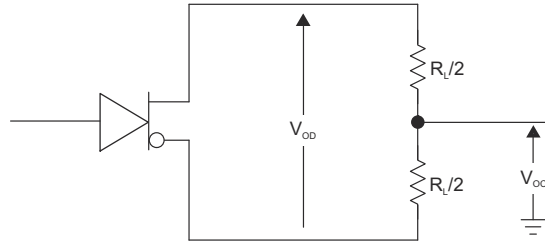
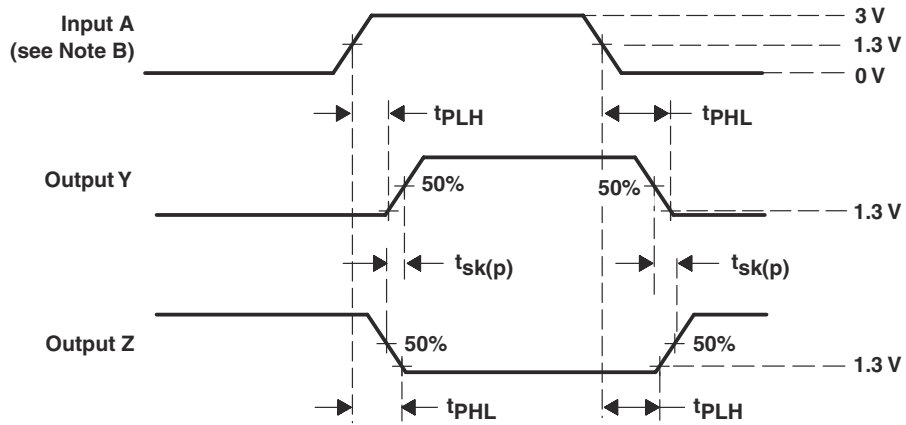
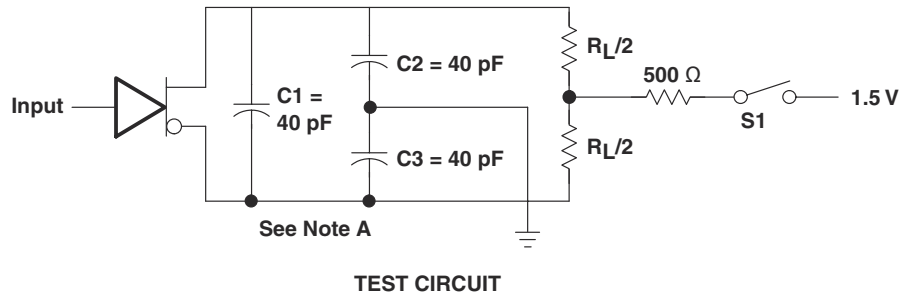


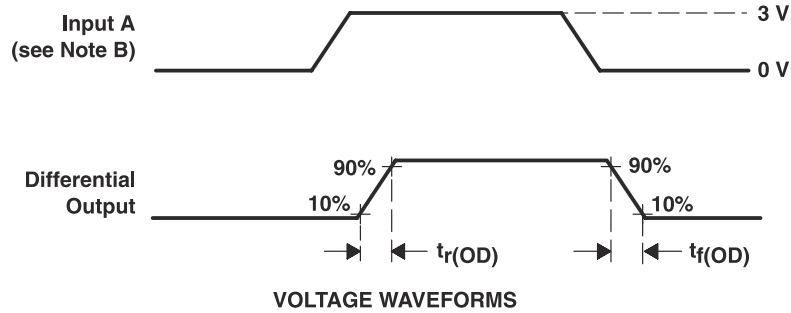
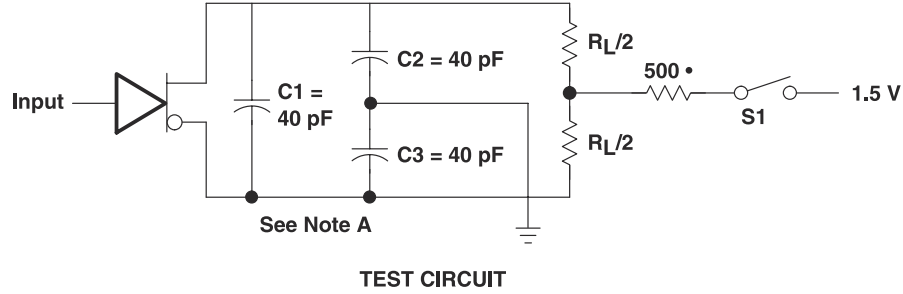
図 6-1. Differential and Common-Mode Output Voltages



- A. C1, C2, and C3 include probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, duty cycle ≤ 50%, and  $t_r, t_f \leq 6\text{ns}$ .

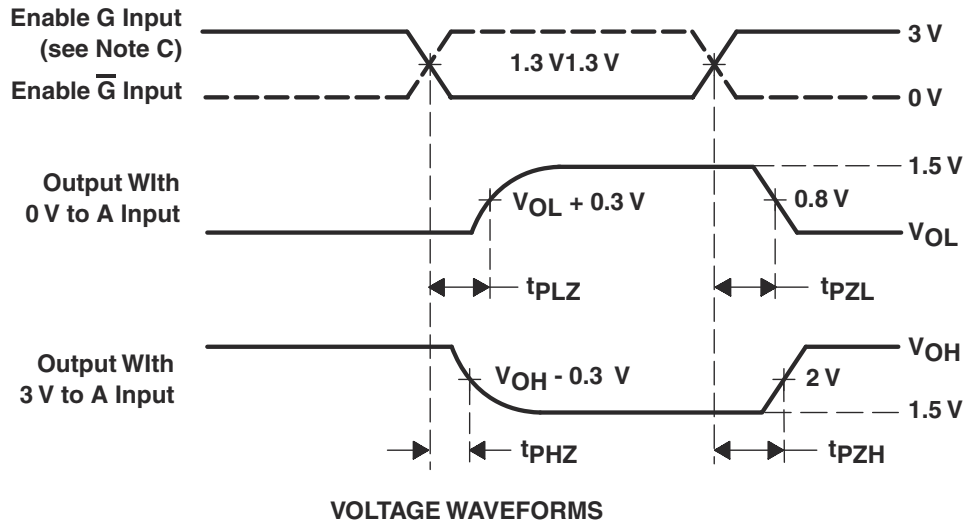
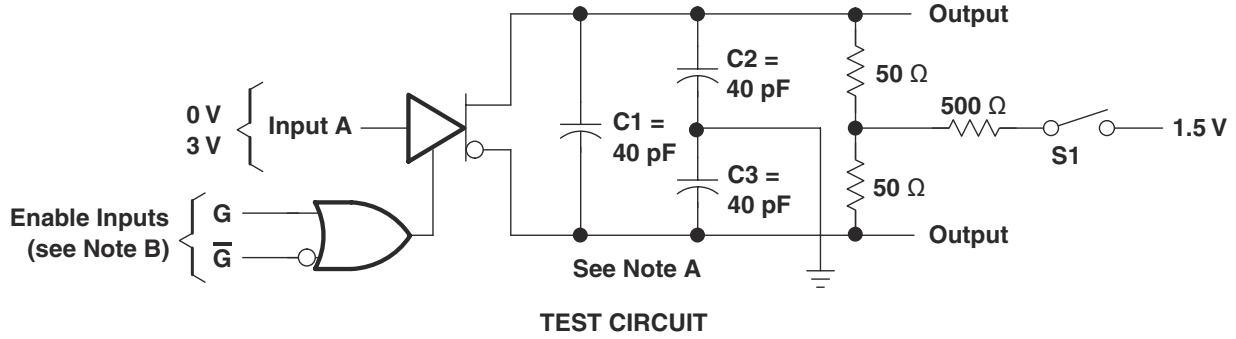
図 6-2. Propagation Delay Time and Skew Waveforms and Test Circuit





- A. C1, C2, and C3 include probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, duty cycle ≤ 50%, and  $t_r, t_f \leq 6\text{ns}$ .

**图 6-3. Differential-Output Rise and Fall-Time Waveforms and Test Circuit**



- A. C1, C2, and C3 include probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, duty cycle ≤ 50%, and  $t_r, t_f \leq 6\text{ns}$ .
- C. Each enable is tested separately.

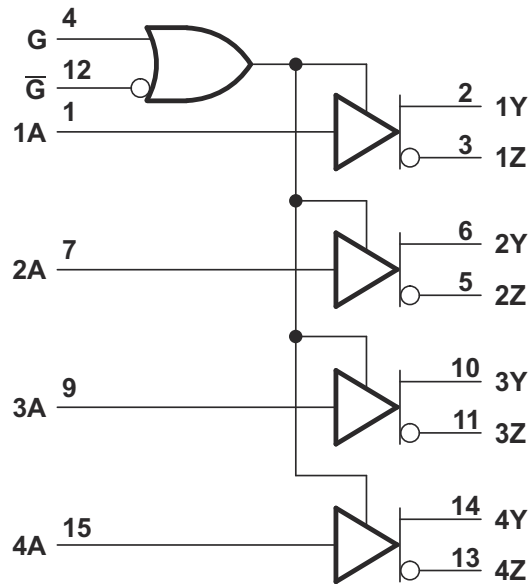
**图 6-4. Output Enable and Disable Time Waveforms and Test Circuit**

## 7 Detailed Description

### 7.1 Overview

The AM26C31 is a quadruple differential line driver with complementary outputs. The device is designed to meet the requirements of TIA/EIA-422-B and ITU (formerly CCITT), and it is generally used to communicate over relatively long wires in noisy environments.

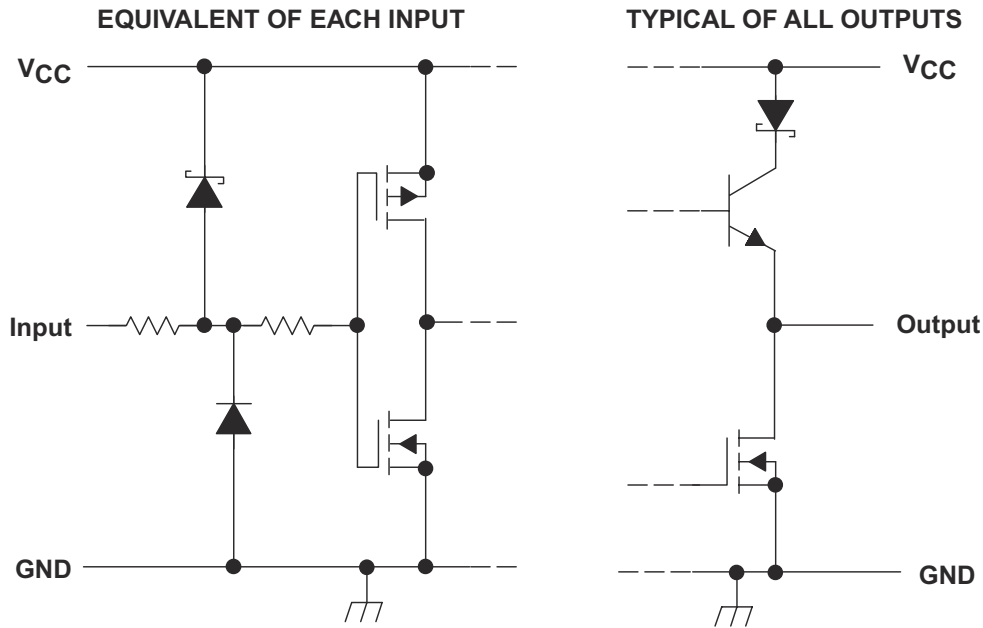
### 7.2 Functional Block Diagrams



Copyright © 2016, Texas Instruments Incorporated

Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

**图 7-1. Logic Diagram (Positive Logic)**



Copyright © 2016, Texas Instruments Incorporated

図 7-2. Schematics of Inputs and Outputs

## 7.3 Feature Description

### 7.3.1 Active-High and Active-Low

The device can be configured using the  $G$  and  $\bar{G}$  logic inputs to select transmitter output. A logic high on the  $G$  pin or a logic low on the  $\bar{G}$  pin enables the device to operate. These pins are simply a way to configure the logic to match that of the receiving or transmitting controller or microprocessor.

### 7.3.2 Operates From a Single 5V Supply

Both the logic and transmitters operate from a single 5V rail, making designs much more simple. The line drivers and receivers can operate off the same rail as the host controller or a similar low voltage supply, thus simplifying power structure.

## 7.4 Device Functional Modes

表 7-1 lists the functional modes of the AM26C31.

表 7-1. Function Table (Each Driver)<sup>(1)</sup>

INPUT A	ENABLES		OUTPUTS	
	G	$\bar{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

- (1) H = High level,  
L = Low level,  
X = Irrelevant,  
Z = High impedance (off)

## 8 Application Information Disclaimer

### 注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

### 8.1 Application Information

When designing a system that uses drivers, receivers, and transceivers that comply with RS-422, proper cable termination is essential for highly reliable applications with reduced reflections in the transmission line. Because RS-422 allows only one driver on the bus, if termination is used, it is placed only at the end of the cable near the last receiver. Factors to consider when determining the type of termination usually are performance requirements of the application and the ever-present factor, cost. The different types of termination techniques discussed are unterminated lines, parallel termination, AC termination, and multipoint termination. For laboratory experiments, 100 feet of 100Ω, 24-AWG, twisted-pair cable (Bertek) was used. A single driver and receiver, TI AM26C31C and AM26C32C, respectively, were tested at room temperature with a 5V supply voltage. To show voltage waveforms related to transmission-line reflections, the first plot shows output waveforms from the driver at the start of the cable (A/B); the second plot shows input waveforms to the receiver at the far end of the cable (Y).

### 8.2 Typical Application

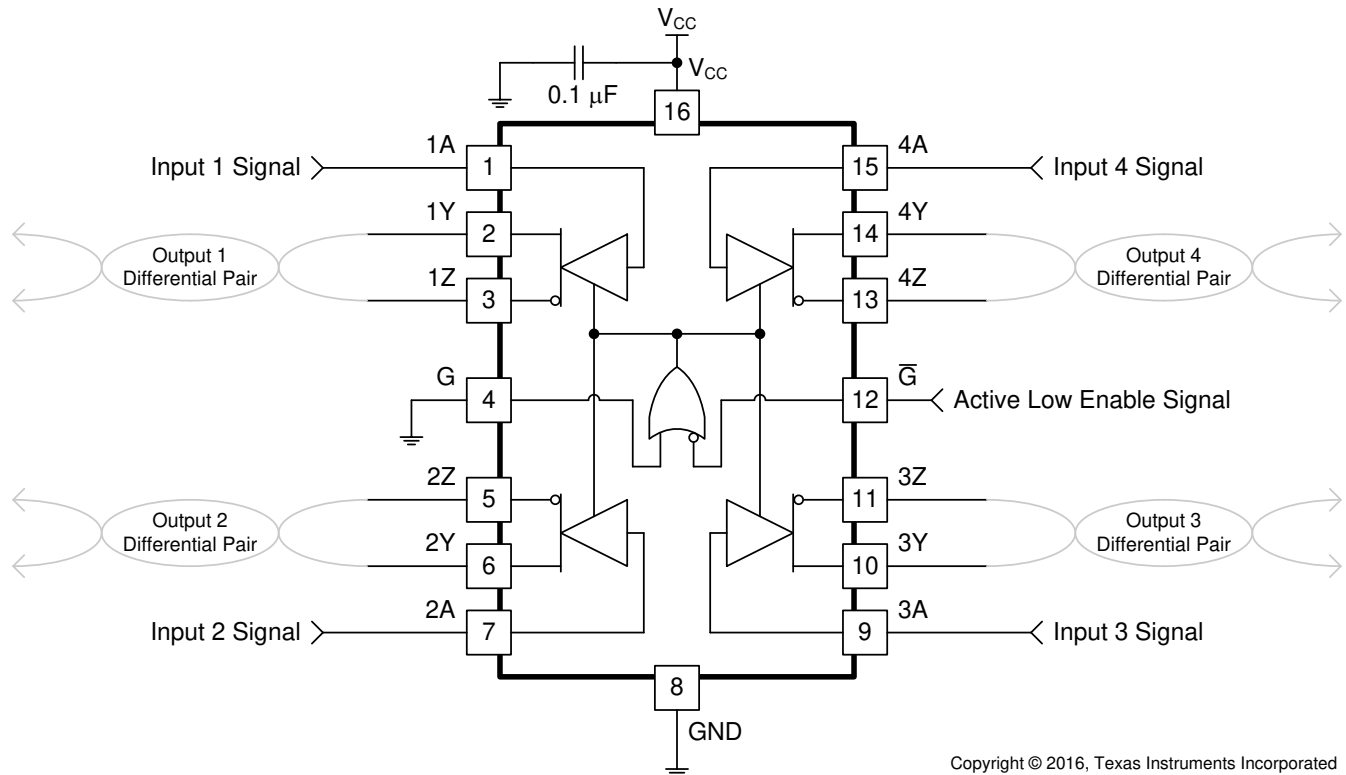


図 8-1. Differential Terminated Configuration With All Channels and Active Low Enable Used

#### 8.2.1 Design Requirements

Resistor and capacitor (if used) termination values are shown for each laboratory experiment, but vary from system to system. For example, the termination resistor,  $R_T$ , must be within 20% of the characteristic impedance,  $Z_0$ , of the cable and can vary from about 80Ω to 120Ω.

## 8.2.2 Detailed Design Procedure

Ensure values in [Absolute Maximum Ratings](#) are not exceeded.

Supply voltage,  $V_{IH}$ , and  $V_{IL}$  must comply with [Recommended Operating Conditions](#).

## 8.2.3 Application Curve

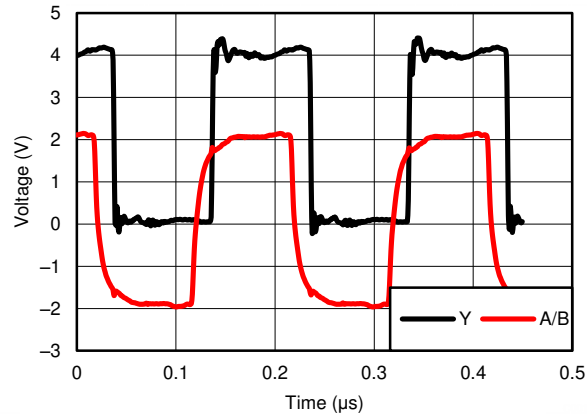


图 8-2. Differential 120Ω Terminated Output Waveforms (Cat 5E Cable)

## 8.3 Power Supply Recommendations

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies.

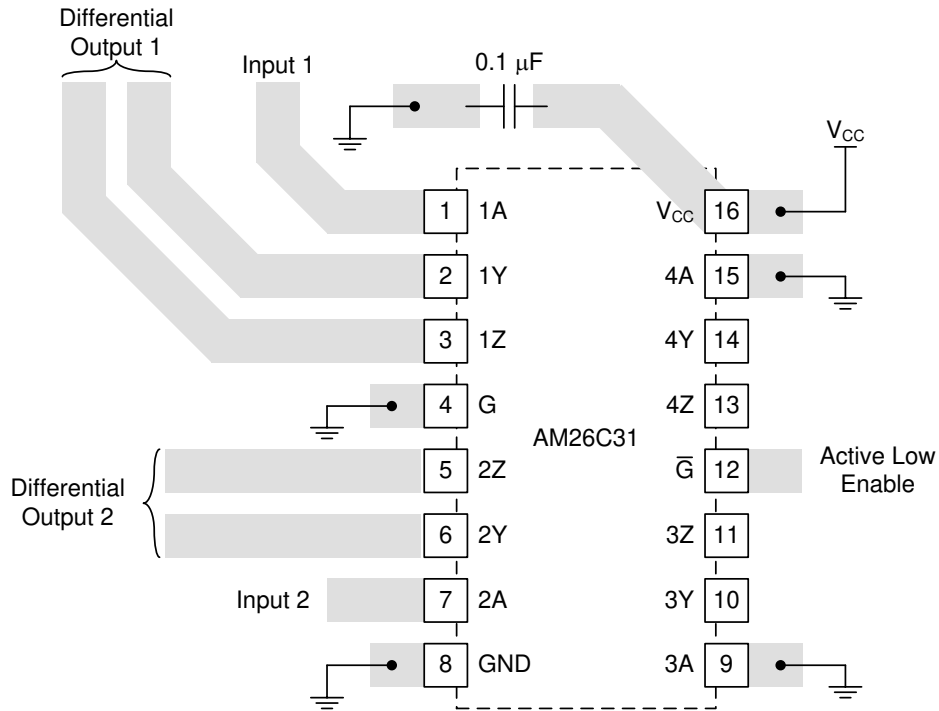
## 8.4 Layout

### 8.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from  $V+$  to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

### 8.4.2 Layout Example




**8-3. Trace Layout on PCB and Recommendations**

## 9 Device and Documentation Support

### 9.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[www.tij.co.jp](http://www.tij.co.jp) のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

### 9.2 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの[使用条件](#)を参照してください。

### 9.3 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

### 9.4 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 9.5 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision O (June 2016) to Revision P (March 2024)	Page
• 「製品情報」表を「パッケージ情報」表に変更.....	1
• Changed <i>Thermal Information</i> table.....	5
• Changed <a href="#">図 5-1</a> .....	7
• Changed <a href="#">図 6-1</a> .....	8

Changes from Revision N (October 2011) to Revision O (February 2014)	Page
• 「特長」セクションを更新。「アプリケーション」セクション、「デバイス情報」表、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 .....	1
• 「注文情報」表を削除 (データシートの末尾にある POA を参照) .....	1
• Changed <i>Thermal Information</i> table.....	5



---

<b>Changes from Revision M (June 2008) to Revision N (October 2011)</b>	<b>Page</b>
• Changed units to mA from $\mu$ A to fix units typo.....	<b>4</b>

---

## **11 Mechanical, Packaging, and Orderable Information**

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

## 重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ(データシートを含みます)、設計リソース(リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適したテキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されているテキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、[テキサス・インスツルメンツの販売条件](#)、または [ti.com](https://www.ti.com) やかかるテキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2024, Texas Instruments Incorporated

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9163901M2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9163901M2A AM26C31M	<a href="#">Samples</a>
5962-9163901MEA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9163901ME A AM26C31M	<a href="#">Samples</a>
5962-9163901MFA	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9163901MF A AM26C31M	<a href="#">Samples</a>
5962-9163901Q2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9163901Q2A AM26C31 MFKB	<a href="#">Samples</a>
5962-9163901QEA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9163901QE A AM26C31MJB	<a href="#">Samples</a>
5962-9163901QFA	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9163901QF A AM26C31MWB	<a href="#">Samples</a>
AM26C31CD	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	0 to 70	AM26C31C	
AM26C31CDBR	OBSOLETE	SSOP	DB	16		TBD	Call TI	Call TI	0 to 70	26C31	
AM26C31CDR	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	0 to 70	AM26C31C	
AM26C31CN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	AM26C31CN	<a href="#">Samples</a>
AM26C31CNSR	ACTIVE	SOP	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	26C31	<a href="#">Samples</a>
AM26C31IDBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	26C31I	<a href="#">Samples</a>
AM26C31IDBRE4	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	26C31I	<a href="#">Samples</a>
AM26C31IDR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AM26C31I	<a href="#">Samples</a>
AM26C31IDRG4	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 85	AM26C31I	
AM26C31IN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	AM26C31IN	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AM26C31INE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	AM26C31IN	<a href="#">Samples</a>
AM26C31INSR	ACTIVE	SOP	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	26C31I	<a href="#">Samples</a>
AM26C31IPW	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-40 to 85	26C31I	
AM26C31IPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	26C31I	<a href="#">Samples</a>
AM26C31IPWRG4	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-40 to 85	26C31I	
AM26C31MFKB	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9163901Q2A AM26C31 MFKB	<a href="#">Samples</a>
AM26C31MJB	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9163901QE A AM26C31MJB	<a href="#">Samples</a>
AM26C31MWB	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9163901QF A AM26C31MWB	<a href="#">Samples</a>
AM26C31QD	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 125	AM26C31Q	
AM26C31QDG4	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 125	26C31Q	
AM26C31QDR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AM26C31Q	<a href="#">Samples</a>
AM26C31QDRG4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	26C31Q	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

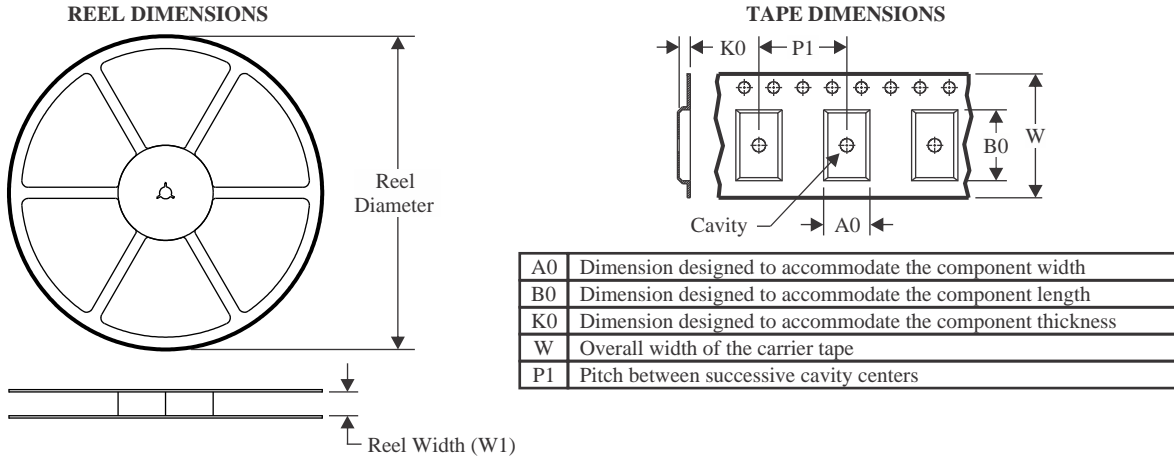
**OTHER QUALIFIED VERSIONS OF AM26C31, AM26C31M :**

- Catalog : [AM26C31](#)
  
- Enhanced Product : [AM26C31-EP](#), [AM26C31-EP](#)
  
- Military : [AM26C31M](#)

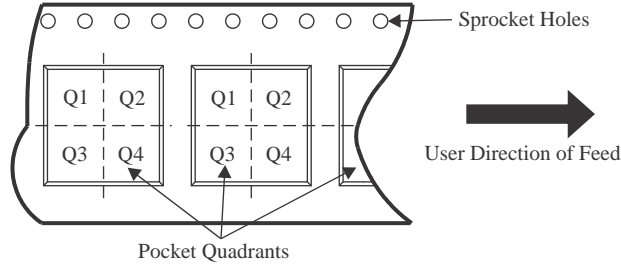
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
  
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
  
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AM26C31CNSR	SOP	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
AM26C31CNSR	SOP	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
AM26C31IDBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
AM26C31IDBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
AM26C31IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26C31IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26C31INSR	SOP	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
AM26C31INSR	SOP	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
AM26C31IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
AM26C31IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
AM26C31QDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26C31QDRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AM26C31CNSR	SOP	NS	16	2000	353.0	353.0	32.0
AM26C31CNSR	SOP	NS	16	2000	356.0	356.0	35.0
AM26C31IDBR	SSOP	DB	16	2000	356.0	356.0	35.0
AM26C31IDBR	SSOP	DB	16	2000	353.0	353.0	32.0
AM26C31IDR	SOIC	D	16	2500	353.0	353.0	32.0
AM26C31IDR	SOIC	D	16	2500	340.5	336.1	32.0
AM26C31INSR	SOP	NS	16	2000	353.0	353.0	32.0
AM26C31INSR	SOP	NS	16	2000	356.0	356.0	35.0
AM26C31IPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
AM26C31IPWR	TSSOP	PW	16	2000	353.0	353.0	32.0
AM26C31QDR	SOIC	D	16	2500	353.0	353.0	32.0
AM26C31QDRG4	SOIC	D	16	2500	353.0	353.0	32.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9163901M2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9163901MFA	W	CFP	16	25	506.98	26.16	6220	NA
5962-9163901Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9163901QFA	W	CFP	16	25	506.98	26.16	6220	NA
AM26C31CN	N	PDIP	16	25	506	13.97	11230	4.32
AM26C31IN	N	PDIP	16	25	506	13.97	11230	4.32
AM26C31INE4	N	PDIP	16	25	506	13.97	11230	4.32
AM26C31MFKB	FK	LCCC	20	55	506.98	12.06	2030	NA
AM26C31MWB	W	CFP	16	25	506.98	26.16	6220	NA





# PACKAGE OUTLINE

## NS0016A

### SOP - 2.00 mm max height

SOP



4220735/A 12/2021

#### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

# EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# DB0016A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4220763/A 05/2022

**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



# EXAMPLE BOARD LAYOUT

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP2-F16

## GENERIC PACKAGE VIEW

**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

## 重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス・デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、または [ti.com](#) やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所 : Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2024, Texas Instruments Incorporated