

# BQ25504 エネルギー・ハーベスト・アプリケーション用の超低消費電力昇圧コンバータ、バッテリー管理機能付き

## 1 特長

- 高効率の DC/DC 昇圧コンバータ / 充電器を使用した超低消費電力
  - 低入力電力源からの継続的なエネルギー・ハーベスト:  $V_{IN} = 130\text{mV}$  (代表値) に変更
  - 超低静止電流:  $I_Q = 330\text{nA}$  (代表値)
  - コールドスタート電圧:  $V_{IN} = 600\text{mV}$  (代表値)
- プログラム可能な動的最大電力点追従 (MPPT)
  - 動的最大電力点追従機能を内蔵することで、各種のエネルギー源からエネルギーを効率よく抽出
  - 入力電圧レギュレーションにより入力源の過度の電圧低下を防止
- エネルギー・ストレージ
  - 充電可能なリチウムイオン・バッテリー、薄膜バッテリー、スーパーキャパシタ、従来型コンデンサにエネルギーを蓄積可能
- バッテリーの充電と保護
  - ユーザーが低電圧および過電圧レベルをプログラム可能
  - 過熱シャットオフをプログラム可能なオンチップ温度センサ
- バッテリー・ステータス出力
  - バッテリー・グッド出力ピン
  - スレッシュホールドとヒステリシスをプログラム可能
  - 接続されたマイクロコントローラに電源喪失を未然に警告
  - システム負荷のイネーブル / ディセーブルに使用可能

## 2 アプリケーション

- エネルギー・ハーベスト (環境発電)
- ソーラー充電器
- 熱電発電器 (TEG) によるハーベスト
- ワイヤレス・センサ・ネットワーク (WSN)
- 産業機器監視
- 環境監視
- 橋梁および構造健全性監視 (SHM)
- スマート・ビルディング制御
- 携帯およびウェアラブルの健康機器
- エンターテインメント・システムのリモート制御

## 3 概要

BQ25504 デバイスは、超低消費電力アプリケーションの特殊な要件を満たすのに適したインテリジェント統合エネルギー・ハーベスト・ナノパワー管理ソリューションの新しいファミリに属する最初の製品です。このデバイスは、光電池 (ソーラーパネル) や熱電発電器などの各種 DC 源から生

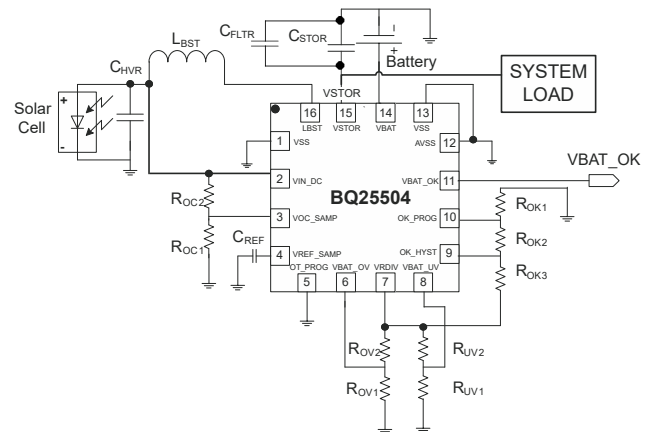
成されたマイクロワット ( $\mu\text{W}$ ) からミリワット ( $\text{mW}$ ) 級の電力を、効率的に取得し、管理することに特化して設計されています。BQ25504 は、この種のデバイスとしては初めて、電力と運用に関する要求が厳しいワイヤレス・センサ・ネットワーク (WSN) などの製品およびシステム向けに高効率昇圧コンバータ / 充電器を実装しています。BQ25504 の設計は、動作を開始するのに数マイクロワットの電力しか必要としない DC-DC 昇圧コンバータ / 充電器を基盤としています。

この昇圧コンバータ / 充電器は起動後、熱電発電器 (TEG) や 1~2 セル・ソーラー・パネルなどの低電圧出力ハーベスタから効果的に電力を抽出できます。昇圧コンバータは最小  $600\text{mV}$  の  $V_{IN}$  で起動でき、起動後は最小  $130\text{mV}$  の  $V_{IN}$  でエネルギー・ハーベストを継続できます。

### 製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
BQ25504	VQFN (16)	3.00mm × 3.00mm

- (1) 利用可能なパッケージについては、データシートの末尾にある注文情報を参照してください。



ソーラー・アプリケーション回路



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## 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

<b>Changes from Revision F (November 2019) to Revision G (August 2023)</b> .....	<b>Page</b>
• Added "Connect to thermal pad." to AVSS and VSS pin descriptions in <i>Pin Functions</i> table.....	5
• Added lines from AVSS and VSS to GND in <a href="#">図 11-1</a> .....	29
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• 「新規設計での使用を推奨しません」を削除.....	1
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• 「特長」を以下のように変更: $V_{IN} \geq 80\text{mV}$ (代表値) から $V_{IN} = 130\text{mV}$ (代表値).....	1
• 「概要」の最小 330mV の $V_{IN}$ を最小 600mV の $V_{IN}$ に変更 .....	1
• 「概要」の「最小 80mV の $V_{IN}$ でエネルギー・ハーベストを」を「最小 130mV の $V_{IN}$ でエネルギー・ハーベストを」に変更 .....	1
• Changed From: "330 mV typical,.. " To: "600 mV typical,.. " in the second paragraph of the <i>Overview</i> section.....	11
• Changed <a href="#">図 8-1</a> .....	13
• Changed From: "VIN(CS) = 330 mV typical." To: "VIN(CS) = 600 mV typical." in the second paragraph of the <i>Cold-Start Operation</i> section.....	15
<b>Changes from Revision C (June 2015) to Revision D (December 2018)</b> .....	<b>Page</b>
• 「特長」のコールドスタート電圧: $V_{IN} \geq 330\text{mV}$ (代表値) からコールドスタート電圧: $V_{IN} = 600\text{mV}$ (代表値) に変更... 1	1
• Changed the RGT Package appearance .....	5
• Moved $T_{sig}$ to the <i>Absolute Maximum Ratings</i> table.....	6
• Changed Handling Ratings To: <i>ESD Ratings</i> .....	6
• Increased $V_{IN(CS)}$ From: TYP = 330 mV and MAX = 450 mV To: TYP = 600 mV and MAX = 700 mV in <a href="#">セクション 7.5</a> table.....	7
<b>Changes from Revision B (December 2014) to Revision C (June 2015)</b> .....	<b>Page</b>
• Changed the Test Condition for $P_{IN(CS)}$ in the <a href="#">セクション 7.5</a> .....	7

• Changed the values for P <sub>IN(CS)</sub> in the セクション 7.5 From: TYP = 10, MAX = 50 To: TYP = 15, MAX deleted .....	7
• Changed C <sub>FLTR</sub> To: C <sub>BYP</sub> ☒ 9-1 .....	20
• Changed CBYP = 0.1 μF To: CBYP = 0.01 μF in セクション 9.2.1.2 .....	20
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<b>Changes from Revision A (September 2012) to Revision B (December 2014)</b>	<b>Page</b>
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• 「取り扱い定格」の表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 .....	1
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<b>Changes from Revision * (October 2011) to Revision A (September 2012)</b>	<b>Page</b>
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• Changed the <i>Cold -Start Operation</i> section.....	15
• Changed the Boost Converter, Charger Operation section.....	16
• Changed the Storage Element section.....	16
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• Added C <sub>FLTR</sub> and Notes 1 and 2 to ☒ 9-1 .....	20
• Added C <sub>FLTR</sub> and Notes 1 and 2 to ☒ 9-8 .....	23
• Added C <sub>FLTR</sub> and Notes 1 and 2 to ☒ 9-15 .....	25

## 5 概要 (続き)

また、BQ25504 は、デバイスへの電力の伝達を最適化するため、プログラム可能な最大電力点追従サンプリング・ネットワークも実装しています。VIN\_DC の開路電圧のサンプリングは、外付け抵抗で設定され、外付けコンデンサ(C<sub>REF</sub>)により保持されます。

たとえば、開路電圧の 80% の最大電力点(MPP)で動作するソーラー・セルの場合、分圧抵抗回路を VIN\_DC 電圧の 80% に設定することで、サンプリングされた基準電圧近くで動作するように VIN\_DC が制御されます。または、MCU から外部基準電圧を供給し、より複雑な MTPP アルゴリズムを実現することもできます。

BQ25504 は、各種のエネルギー蓄積素子を柔軟にサポートするように設計されています。ハーベスタのエネルギー抽出源の利用可能性は、多くの場合、散発的であるか時間によって変動します。システムには通常、充電可能バッテリー、スーパーキャパシタ、従来型コンデンサなど、何らかの種類のエネルギー蓄積素子が必要です。この蓄積素子により、システムが必要としたときに一定の電力が利用できるようにします。また、この蓄積素子によりシステムは、入力源からは直接得ることができないピーク電流に対応できます。

蓄積素子を損傷させないように、ユーザーがプログラムした低電圧(UV)および過電圧(OV)レベルに対して、最高および最低電圧が監視されます。

さらに、エネルギー収支を厳密に管理するユーザーを支援するため、エネルギーを蓄積するバッテリーまたはコンデンサの電圧が、プリセットされた臨界値を下回った場合、BQ25504 はバッテリー・グッド・フラグを切り替え、接続されているマイクロプロセッサに通知します。この警告により、システムが低電圧条件に入らないように負荷電流制限がトリガされます。OV、UV、バッテリー・グッドのスレッシュホールドは、別々にプログラム可能です。

BQ25504 のすべての機能は、省スペース型の 16 ピン、3mm × 3mm VQFN パッケージに納められています。

## 6 Pin Configuration and Functions

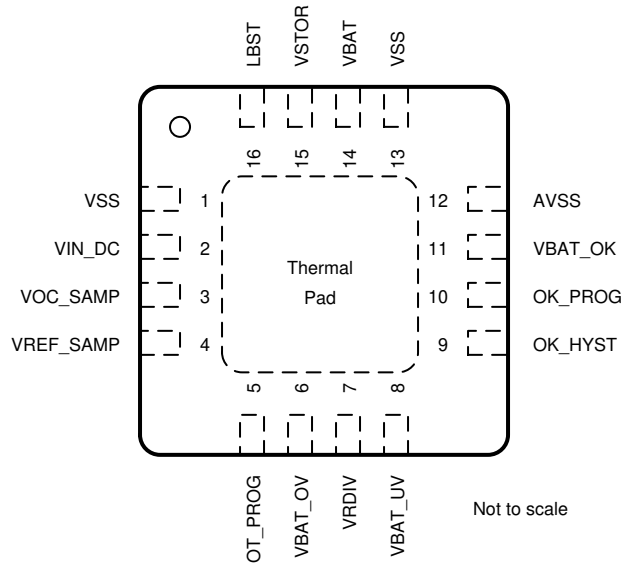


图 6-1. RGT Package 16 Pins Top View

表 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AVSS	12	Supply	Signal ground connection for the device. Connect to thermal pad.
LBST	16	Input	Inductor connection for the boost charger switching node. Connect a 22 $\mu$ H inductor between this pin and pin 2 (VIN_DC).
OK_HYST	9	Input	Connect to the mid-point of external resistor divider between VRDIV and GND for setting the VBAT_OK hysteresis threshold. If not used, connect this pin to GND.
OK_PROG	10	Input	Connect to the mid-point of external resistor divider between VRDIV and GND for setting the VBAT_OK threshold. If not used, connect this pin to GND.
OT_PROG	5	Input	Digital Programming input for IC overtemperature threshold. Connect to GND for 60 C threshold or VSTOR for 120 C threshold.
VBAT	14	I/O	Connect a rechargeable storage element with at least 100 $\mu$ F of equivalent capacitance to this pin.
VBAT_OK	11	Output	Digital output for battery good indicator. Internally referenced to the VSTOR voltage. Leave floating if not used.
VBAT_OV	6	Input	Connect to the mid-point of external resistor divider between VRDIV and GND for setting the VSTOR = VBAT overvoltage threshold.
VBAT_UV	8	Input	Connect to the mid-point of external resistor divider between VRDIV and GND for setting the VBAT undervoltage threshold. The PFET between VBAT and VSTOR opens if the voltage on VSTOR is below this threshold.
VIN_DC	2	Input	DC voltage input from energy harvesters. Connect at least a 4.7 $\mu$ F capacitor as close as possible between this pin and pin 1.
VOC_SAMP	3	Input	Sampling pin for MPPT network. Connect to the mid-point of external resistor divider between VIN_DC and GND for setting the MPP threshold voltage which will be stored on the VREF_SAMP pin. To disable the MPPT sampling circuit, connect to VSTOR.
VRDIV	7	Output	Resistor divider biasing voltage.
VREF_SAMP	4	Input	Connect a 0.01 $\mu$ F low leakage capacitor from this pin to GND to store the voltage to which VIN_DC will be regulated. This voltage is provided by the MPPT sample circuit. When MPPT is disabled, either use an external voltage source to provide this voltage or tie this pin to GND to disable input voltage regulation (i.e. operate from a low impedance power supply).
VSS	1	Input	General ground connection for the device. Connect to thermal pad.
VSS	13	Supply	General ground connection for the device. Connect to thermal pad.
VSTOR	15	Output	Connection for the output of the boost charger, which is typically connected to the system load. Connect at least a 4.7 $\mu$ F capacitor in parallel with a 0.1 $\mu$ F capacitor as close as possible to between this pin and pin 1 (VSS).

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Input voltage	VIN_DC, VOC_SAMP, VREF_SAMP, VBAT_OV, VBAT_UV, VRDIV,	-0.3	5.5	V
Peak Input Power, P <sub>IN_PK</sub>	OK_HYST, OK_PROG, VBAT_OK, VBAT, VSTOR, LBST <sup>(2)</sup>		400	mW
Operating junction temperature range, T <sub>J</sub>		-40	125	°C
Storage temperature range, T <sub>stg</sub>		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to V<sub>SS</sub>/ground terminal.

### 7.2 ESD Ratings

			MIN	MAX	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>		2	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>		500	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V <sub>IN(DC)</sub>	DC input voltage into VIN_DC <sup>(1)</sup>	0.13		3	V
VBAT	Battery voltage range <sup>(2)</sup>	2.5		5.25	V
C <sub>HVR</sub>	Input capacitance	4.23	4.7	5.17	μF
C <sub>STOR</sub>	Storage capacitance	4.23	4.7	5.17	μF
C <sub>BAT</sub>	Battery pin capacitance or equivalent battery capacity	100			μF
C <sub>REF</sub>	Sampled reference storage capacitance	9	10	11	nF
R <sub>OC1</sub> + R <sub>OC2</sub>	Total resistance for setting for MPPT reference.	18	20	22	MΩ
R <sub>OK1</sub> + R <sub>OK2</sub> + R <sub>OK3</sub>	Total resistance for setting reference voltage.	9	10	11	MΩ
R <sub>UV1</sub> + R <sub>UV2</sub>	Total resistance for setting reference voltage.	9	10	11	MΩ
R <sub>OV1</sub> + R <sub>OV2</sub>	Total resistance for setting reference voltage.	9	10	11	MΩ
L <sub>BST</sub>	Input inductance	19.8	22	24.2	μH
T <sub>A</sub>	Operating free air ambient temperature	-40		85	°C
T <sub>J</sub>	Operating junction temperature	-40		105	°C

- (1) Maximum input power ≤ 300 mW. Cold start has been completed
- (2) VBAT\_OV setting must be higher than VIN\_DC

## 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		BQ25504	UNIT
		RGT (QFN)	
		16 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	48.5	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	63.9	
R <sub>θJB</sub>	Junction-to-board thermal resistance	22	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	1.8	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	22	
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	6.5	

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report, .

## 7.5 Electrical Characteristics

Over recommended temperature range, typical values are at T<sub>A</sub> = 25°C. Unless otherwise noted, specifications apply for conditions of V<sub>IN\_DC</sub> = 1.2V, V<sub>BAT</sub> = V<sub>STOR</sub> = 3V. External components L<sub>BST</sub> = 22 μH, C<sub>HVR</sub> = 4.7 μF C<sub>STOR</sub> = 4.7 μF.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>BOOST CONVERTER \ CHARGER STAGE</b>						
V <sub>IN(DC)</sub>	DC input voltage into V <sub>IN_DC</sub>	Cold-start completed	130		3000	mV
I <sub>IN(DC)</sub>	Peak Current flowing from V <sub>IN</sub> into V <sub>IN_DC</sub> input	0.5V < V <sub>IN</sub> < 3 V; V <sub>STOR</sub> = 4.2 V		200	300	mA
P <sub>IN</sub>	Input power range for normal charging	V <sub>BAT</sub> > V <sub>IN_DC</sub> ; V <sub>IN_DC</sub> = 0.5 V	0.01		300	mW
V <sub>IN(CS)</sub>	Cold-start Voltage. Input voltage that will start charging of V <sub>STOR</sub>	V <sub>BAT</sub> < V <sub>BAT_UV</sub> ; V <sub>STOR</sub> = 0 V; 0°C < T <sub>A</sub> < 85°C		600	700	mV
P <sub>IN(CS)</sub>	Minimum cold-start input power to start normal charging	V <sub>BAT</sub> < V <sub>STOR(CHGEN)</sub> V <sub>IN_DC</sub> clamped to V <sub>IN_CS</sub> by cold start circuit V <sub>BAT</sub> = 100 μF ceramic		15		μW
V <sub>STOR_CHGEN</sub>	Voltage on V <sub>STOR</sub> when cold start operation ends and normal charger operation begins		1.6	1.77	1.95	V
R <sub>BAT(on)</sub>	Resistance of switch between V <sub>BAT</sub> and V <sub>STOR</sub> when turned on.	V <sub>BAT</sub> = 4.2 V; V <sub>STOR</sub> load = 50 mA			2	Ω
R <sub>DS(on)</sub>	Charger Low Side switch ON resistance	V <sub>BAT</sub> = 2.1 V			2	Ω
		V <sub>BAT</sub> = 4.2 V			2	
R <sub>DS(on)</sub>	Charger rectifier High Side switch ON resistance	V <sub>BAT</sub> = 2.1 V			5	Ω
		V <sub>BAT</sub> = 4.2 V			5	
f <sub>SW_BST</sub>	Boost converter mode switching frequency				1	MHz
<b>BATTERY MANAGEMENT</b>						
I <sub>VBAT</sub>	Leakage on V <sub>BAT</sub> pin	V <sub>BAT</sub> = 2.1 V; V <sub>BAT_UV</sub> = 2.3 V, T <sub>J</sub> = 25°C V <sub>STOR</sub> = 0 V		1	5	nA
		V <sub>BAT</sub> = 2.1 V; V <sub>BAT_UV</sub> = 2.3 V, -40°C < T <sub>J</sub> < 65°C, V <sub>STOR</sub> = 0 V			80	nA
I <sub>VSTOR</sub>	V <sub>STOR</sub> Quiescent current Charger Shutdown in UV Condition	V <sub>IN_DC</sub> = 0V; V <sub>BAT</sub> < V <sub>BAT_UV</sub> = 2.4V; V <sub>STOR</sub> = 2.2V, No load on V <sub>BAT</sub>		330	750	nA
	V <sub>STOR</sub> Quiescent current Charger Shutdown in OV Condition	V <sub>IN_DC</sub> = 0V, V <sub>BAT</sub> > V <sub>BAT_OV</sub> , V <sub>STOR</sub> = 4.25, No load on V <sub>BAT</sub>		570	1400	nA
V <sub>BAT_OV</sub>	Programmable voltage range for overvoltage threshold (Battery voltage is rising)	V <sub>STOR</sub> increasing	2.5		5.25	V
V <sub>BAT_OV_HYST</sub>	Battery voltage overvoltage hysteresis threshold (Battery voltage is falling), internal threshold	V <sub>STOR</sub> decreasing	18	35	89	mV
V <sub>BAT_UV</sub>	Programmable voltage range for under voltage threshold (Battery voltage is falling)	V <sub>STOR</sub> decreasing; V <sub>BAT_UV</sub> > V <sub>Bias</sub>	2.2		V <sub>BAT_OV</sub>	V
V <sub>BAT_UV_HYST</sub>	Battery under voltage threshold hysteresis, internal threshold	V <sub>STOR</sub> increasing	40	80	125	mV
V <sub>BAT_OK</sub>	Programmable voltage range for threshold voltage for high to low transition of digital signal indicating battery is OK,	V <sub>STOR</sub> decreasing		V <sub>BAT_UV</sub>	V <sub>BAT_OV</sub>	V
V <sub>BAT_OK_HYST</sub>	Programmable voltage range for threshold voltage for low to high transition of digital signal indicating battery is OK,	V <sub>STOR</sub> increasing	50		V <sub>BAT_OV</sub> - V <sub>BAT_UV</sub>	mV
V <sub>BAT_ACCURACY</sub>	Overall Accuracy for threshold values, UV, OV, V <sub>BAT_OK</sub>	Selected resistors are 0.1% tolerance	-5%		5%	



## 7.5 Electrical Characteristics (continued)

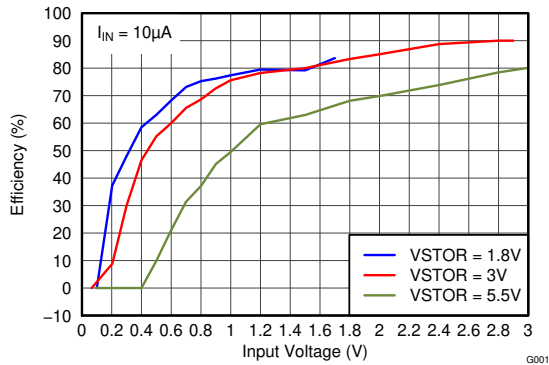
Over recommended temperature range, typical values are at  $T_A = 25^\circ\text{C}$ . Unless otherwise noted, specifications apply for conditions of  $V_{IN\_DC} = 1.2\text{V}$ ,  $V_{BAT} = V_{STOR} = 3\text{V}$ . External components  $L_{BST} = 22\ \mu\text{H}$ ,  $C_{HVR} = 4.7\ \mu\text{F}$ ,  $C_{STOR} = 4.7\ \mu\text{F}$ .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{BAT\_OKH}$	VBAT OK (High) threshold voltage	Load = 10 $\mu\text{A}$			$V_{STOR}-200\text{mV}$	V
$V_{BAT\_OKL}$	VBAT OK (Low) threshold voltage	Load = 10 $\mu\text{A}$			100	mV
TSD_PROTL	The temperature at which the boost converter is disabled and the switch between VBAT and VSTOR is disconnected to protect the battery	OT_Prog = LO		65		$^\circ\text{C}$
TSD_PROTH		OT_Prog = HI		120		
OT_Prog	Voltage for OT_PROG High setting		2			V
	Voltage for OT_PROG Low setting				0.3	V
<b>BIAS and MPPT CONTROL STAGE</b>						
VOC_sample	Sampling period of $V_{IN\_DC}$ open circuit voltage			16		s
VOC_Settling	Sampling period of $V_{IN\_DC}$ open circuit voltage			256		ms
$V_{IN\_Reg}$	Regulation of $V_{IN\_DC}$ during charging	$0.5\text{V} < V_{IN} < 3\text{V}$ ; $I_{IN}(\text{DC}) = 10\text{mA}$	-10%		10%	
$V_{IN\_shutoff}$	DC input voltage into $V_{IN\_DC}$ when charger is turned off		40	80	130	mV
MPPT_Disable	Threshold on VOC_SAMP to disable MPPT functionality			$V_{STOR}-15\text{mV}$		V
VBIAS	Voltage node which is used as reference for the programmable voltage thresholds	$V_{IN\_DC} \geq 0.5\text{V}$ ; $V_{STOR} \geq 1.8\text{V}$	1.21	1.25	1.27	V



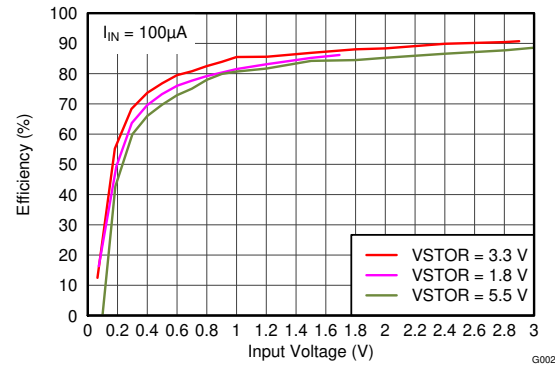
## 7.6 Typical Characteristics

VSTOR = Keithley Sourcemeter configured to measure current and voltage source set to hold the VSTOR voltage = 1.8 V, 3.0 V or 5.5 V; VBAT\_OV = 5.5 V and measurement taken between MPPT measurements.



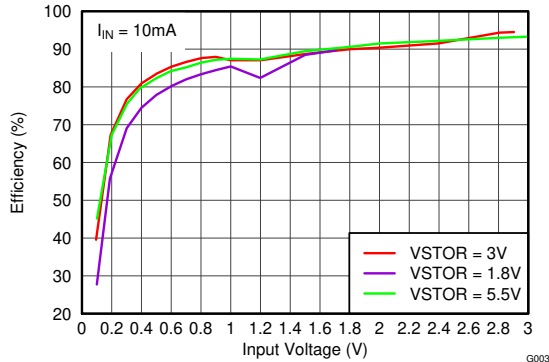
VIN\_DC = Keithley Source Meter configured with I<sub>COMP</sub> = 10 µA and outputting 0 to 3.0 V

**7-1. Efficiency vs Input Voltage**



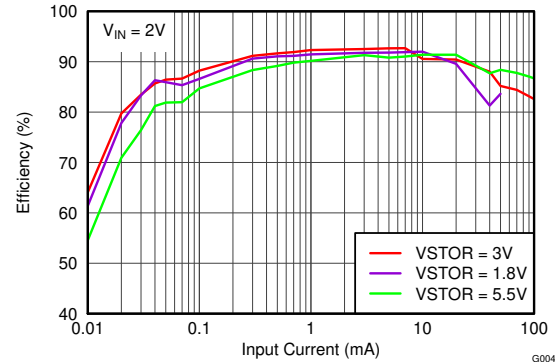
VIN\_DC = Keithley Source Meter configured with I<sub>COMP</sub> = 100 µA and voltage source varied from 0.1 V to 3.0 V

**7-2. Efficiency vs Input Voltage**



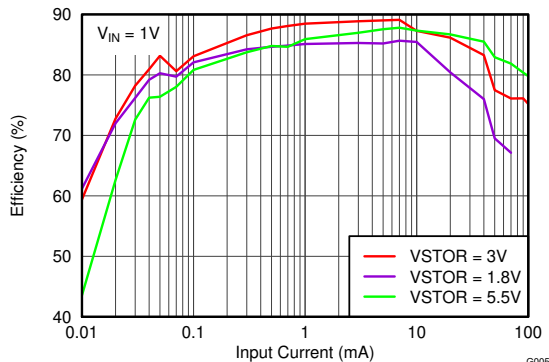
VIN\_DC = Keithley Source Meter configured with I<sub>COMP</sub> = 10 mA and voltage source varied from 0.1 V to 3.0 V

**7-3. Efficiency vs Input Voltage**



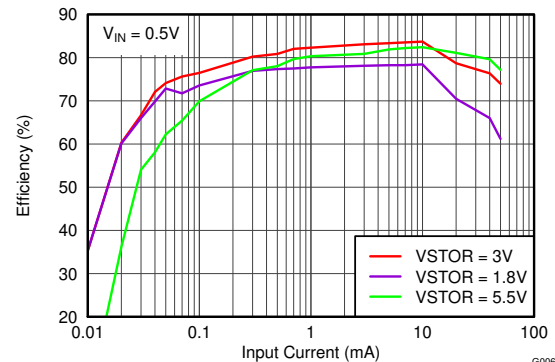
VIN\_DC = Keithley Source Meter configured with voltage source = 2.0 V and I<sub>COMP</sub> varied from 0.01 mA to 100 mA

**7-4. Efficiency vs Input Current**



VIN\_DC = Keithley Source Meter configured with voltage source = 1.0 V and I<sub>COMP</sub> varied from 0.01 mA to 100 mA

**7-5. Efficiency vs Input Current**

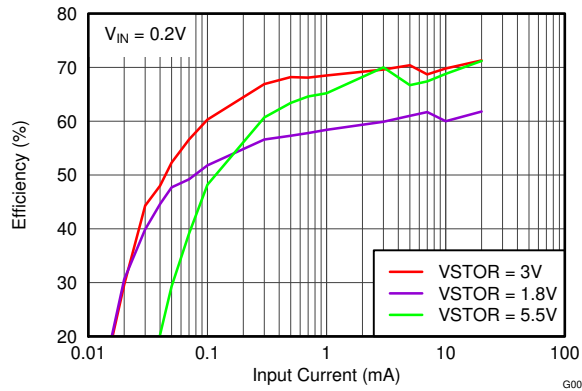


VIN\_DC = Keithley Source Meter configured with voltage source = 0.5 V and I<sub>COMP</sub> varied from 0.01 mA to 100 mA

**7-6. Efficiency vs Input Current**

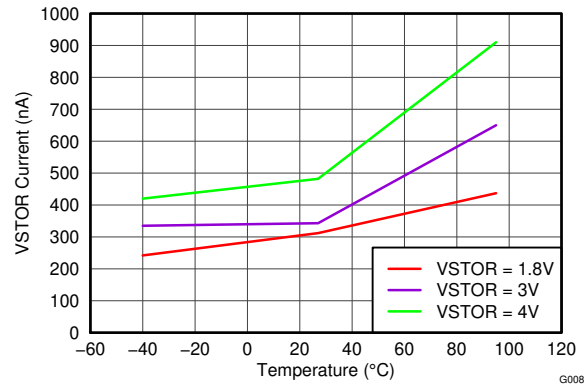
### 7.6 Typical Characteristics (continued)

VSTOR = Keithley Sourcemeter configured to measure current and voltage source set to hold the VSTOR voltage = 1.8 V, 3.0 V or 5.5 V; VBAT\_OV = 5.5 V and measurement taken between MPPT measurements.



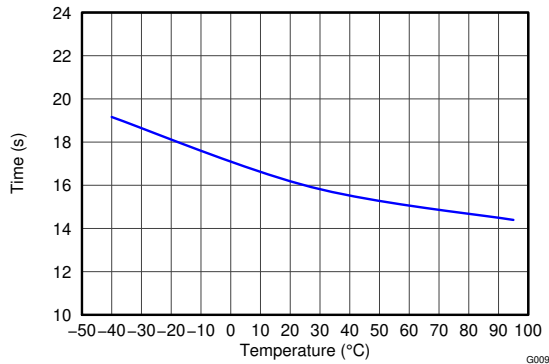
VIN\_DC = Keithley Source Meter configured with voltage source = 0.2 V and I<sub>COMP</sub> varied from 0.01 mA to 100 mA  
VSTOR = Keithley Source Meter configured to measure current and voltage source set to hold the VSTOR voltage = 2.0 V, 3.0 V or 5.5 V

**7-7. Efficiency vs Input Current**

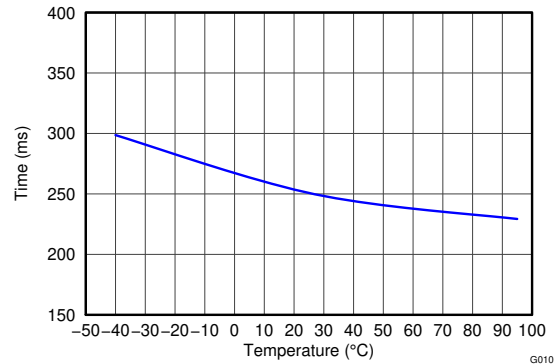


VIN\_DC = floating  
VBAT = Keithley Sourcemeter configured to measure current and voltage source varied from 1.8 V, 3 V, or 4 V

**7-8. VSTOR Quiescent Current vs Temperature**



**7-9. Sample Period vs Temperature**



**7-10. Settling Period vs Temperature**

## 8 Detailed Description

### 8.1 Overview

The BQ25504 is the first of a new family of intelligent integrated energy harvesting Nano-Power management solutions that are well suited for meeting the special needs of ultra low power applications. The product is specifically designed to efficiently acquire and manage the microwatts ( $\mu\text{W}$ ) to milliwatts (mW) of power generated from a variety of DC sources like photovoltaic (solar) or thermal electric generators (TEGs). The BQ25504 is a highly efficient boost charger targeted toward products and systems, such as wireless sensor networks (WSN) which have stringent power and operational demands. The design of the BQ25504 starts with a DCDC boost charger that requires only microwatts of power to begin operating.

Once the VSTOR voltage is above VSTOR\_CHGEN (1.8 V typical), for example, after a partially discharged battery is attached to VBAT, the boost charger can effectively extract power from low voltage output harvesters such as TEGs or single or dual cell solar panels outputting voltages down to VIN(DC) (130 mV minimum). When starting from VSTOR = VBAT < 100 mV, the cold start circuit needs at least VIN(CS), 600 mV typical, to charge VSTOR up to 1.8 V.

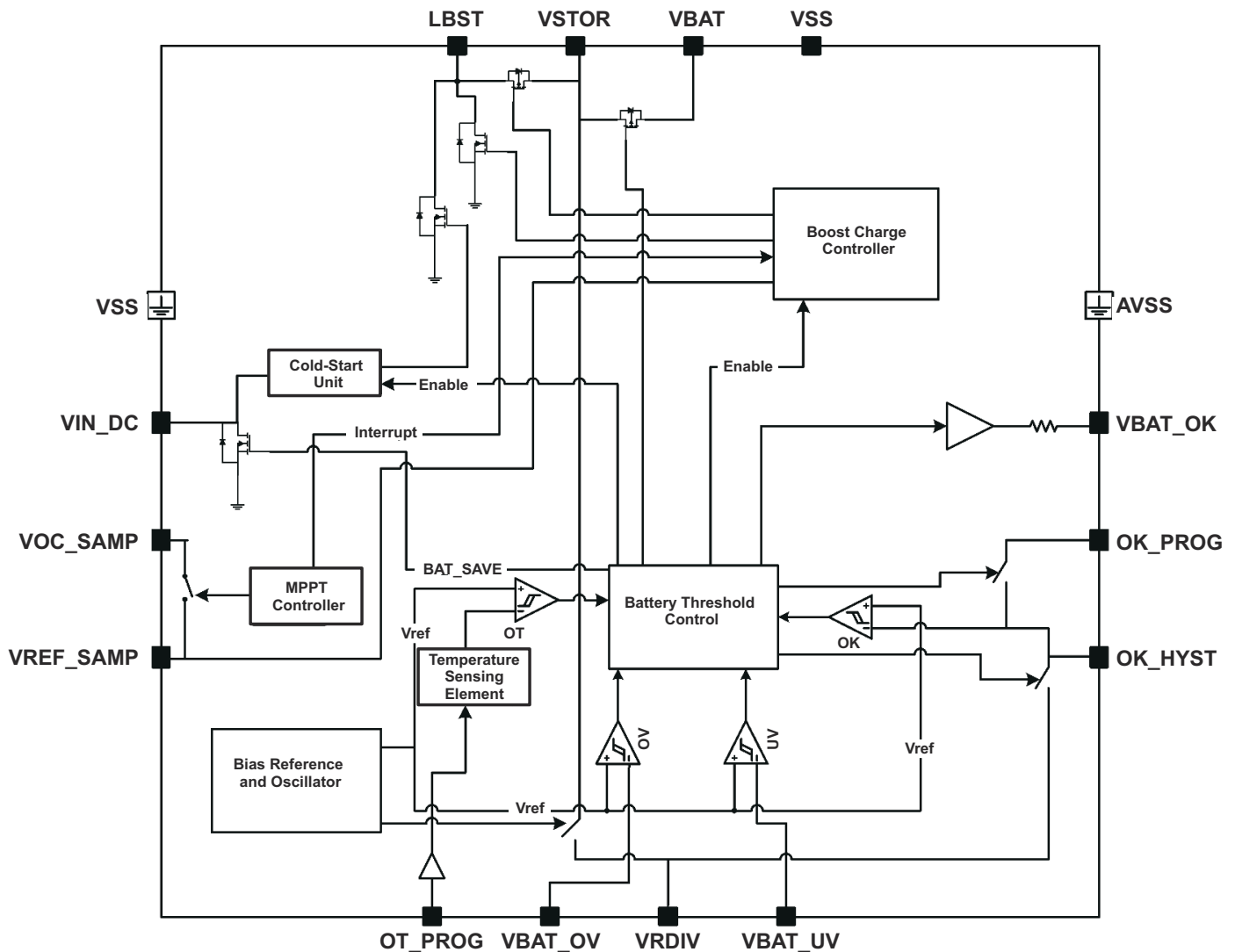
The BQ25504 implements a programmable maximum power point tracking (MPPT) sampling network to optimize the transfer of power into the device. Sampling of the VIN\_DC open circuit voltage is programmed using external resistors, and that sample voltage is held with an external capacitor connected to the VREF\_SAMP pin.

For example solar cells that operate at maximum power point (MPP) of 80% of their open circuit voltage, the resistor divider can be set to 80% of the VIN\_DC voltage and the network will control the VIN\_DC to operate near that sampled reference voltage. Alternatively, an external reference voltage can be applied directly to the VREF\_SAMP pin by a MCU to implement a more complex MPPT algorithm.

The BQ25504 was designed with the flexibility to support a variety of energy storage elements. The availability of the sources from which harvesters extract their energy can often be sporadic or time-varying. Systems will typically need some type of energy storage element, such as a re-chargeable battery, super capacitor, or conventional capacitor. The storage element will make certain constant power is available when needed for the systems. The storage element also allows the system to handle any peak currents that can not directly come from the input source. To prevent damage to the storage element, both maximum and minimum voltages are monitored against the user programmable undervoltage (VBAT\_UV) and overvoltage (VBAT\_OV) levels.

To further assist users in the strict management of their energy budgets, the BQ25504 toggles the battery good flag to signal an attached microprocessor when the voltage on an energy storage battery or capacitor has dropped below a pre-set critical level. This should trigger the shedding of load currents to prevent the system from entering an undervoltage condition. The OV and battery good (VBAT\_OK) thresholds are programmed independently.

## 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Maximum Power Point Tracking

Maximum power point tracking (MPPT) is implemented in order to maximize the power extracted from an energy harvester source. The boost converter indirectly modulates the input impedance of the main boost charger by regulating the charger's input voltage, as sensed by the VIN\_DC pin, to the sampled reference voltage stored on the VREF\_SAMP pin. The MPPT circuit obtains a new reference voltage every 16 s (typical) by periodically disabling the charger for 256 ms (typical) and sampling a fraction of the harvester's open-circuit voltage (VOC). For solar harvesters, the maximum power point is typically 70%-80% of VOC and for thermoelectric harvesters, the MPPT is typically 50%. The exact ratio for MPPT can be optimized to meet the needs of the input source being used by connecting external resistors  $R_{OC1}$  and  $R_{OC2}$  between VIN\_DC and GND with mid-point at VOC\_SAMP.

$$VREF\_SAMP = VIN\_DC(OpenCircuit) \left( \frac{R_{OC1}}{R_{OC1} + R_{OC2}} \right) \quad (1)$$

Spreadsheet [SLUC484](#) provides help on sizing and selecting the resistors.

The internal MPPT circuitry and the periodic sampling of VIN\_DC can be disabled by tying the VOC\_SAMP pin to VSTOR. An external reference voltage can be fed to the VREF\_SAMP pin. The boost converter will then regulate VIN\_DC to the externally provided reference. If input regulation is not desired (i.e. the input source is a low-impedance output battery or power supply instead of a high impedance output energy harvester), VREF\_SAMP can be tied to GND.

### 8.3.2 Battery Undervoltage Protection

To prevent rechargeable batteries from being deeply discharged and damaged, and to prevent completely depleting charge from a capacitive storage element, the undervoltage (VBAT\_UV) threshold must be set using external resistors. The VBAT\_UV threshold voltage when the battery voltage is decreasing is given by 式 2:

$$VBAT\_UV = VBIAS \left( 1 + \frac{R_{UV2}}{R_{UV1}} \right) \quad (2)$$

The sum of the resistors is recommended to be no higher than 10 MΩ that is,  $R_{UV1} + R_{UV2} = 10 \text{ M}\Omega$ . Spreadsheet [SLURAQ1](#) provides help on sizing and selecting the resistors.

The undervoltage threshold when the battery voltage is increasing is VBAT\_UV plus an internal hysteresis voltage denoted by VBAT\_UV\_HYST. For the VBAT\_UV feature to function properly, the load must be connected to the VSTOR pin while the storage element should be connected to the VBAT pin. Once the VSTOR pin voltage goes above VBAT\_UV plus VBAT\_UV\_HYST threshold, the VSTOR pin and the VBAT pins are effectively shorted through an internal PMOS FET. The switch remains closed until the VSTOR pin voltage falls below the VBAT\_UV threshold. The VBAT\_UV threshold should be considered a fail safe to the system. The system load should be removed or reduced based on the VBAT\_OK threshold which should be set above the VBAT\_UV threshold.

### 8.3.3 Battery Overvoltage Protection

To prevent rechargeable batteries from being exposed to excessive charging voltages and to prevent over charging a capacitive storage element, the over-voltage (VBAT\_OV) threshold level must be set using external resistors. This is also the voltage value to which the charger will regulate the VSTOR/VBAT pin when the input has sufficient power. The VBAT\_OV threshold when the battery voltage is rising is given by 式 3:

$$VBAT\_OV = \frac{3}{2} VBIAS \left( 1 + \frac{R_{OV2}}{R_{OV1}} \right) \quad (3)$$

The sum of the resistors is recommended to be no higher 10 MΩ that is,  $R_{OV1} + R_{OV2} = 10 \text{ M}\Omega$ . Spreadsheet [SLURAQ1](#) provides help with sizing and selecting the resistors.

The overvoltage threshold when the battery voltage is decreasing is given by VBAT\_OV - VBAT\_OV\_HYST. Once the voltage at the battery reaches the VBAT\_OV threshold, the boost converter is disabled. The charger will start again once the battery voltage drop by VBAT\_OV\_HYST. When there is excessive input energy, the VBAT pin voltage will ripple between the VBAT\_OV and the VBAT\_OV - VBAT\_OV\_HYST levels.

#### 注意

If VIN\_DC is higher than VSTOR and VSTOR is higher than VBAT\_OV, the input VIN\_DC is pulled to ground through a small resistance to stop further charging of the attached battery or capacitor. It is critical that if this case is expected, the impedance of the source attached to VIN\_DC be higher than 20 Ω and not a low impedance source.

### 8.3.4 Battery Voltage in Operating Range (VBAT\_OK Output)

The IC allows the user to set a programmable voltage independent of the overvoltage and undervoltage settings to indicate whether the VSTOR voltage (and therefore the VBAT voltage when the PFET between the two pins is turned on) is at an acceptable level. When the battery voltage is decreasing the threshold is set by 式 4:

$$VBAT\_OK\_PROG = VBIAS \left( 1 + \frac{R_{OK2}}{R_{OK1}} \right) \quad (4)$$

When the battery voltage is increasing, the threshold is set by 式 5:

$$VBAT\_OK\_HYST = VBIAS \left( 1 + \frac{R_{OK2} + R_{OK3}}{R_{OK1}} \right) \quad (5)$$

The sum of the resistors are recommended to be approximately 10 MΩ i.e.,  $R_{OK1} + R_{OK2} + R_{OK3} = 10 \text{ M}\Omega$ . Spreadsheet [SLURAQ1](#) provides help on sizing and selecting the resistors.

The logic high level of this signal is equal to the VSTOR voltage and the logic low level is ground. The logic high level has ~20 KΩ internally in series to limit the available current to prevent MCU damage until it is fully powered. The VBAT\_OK\_PROG threshold must be greater than or equal to the UV threshold. 图 8-1 shows the relative position of the various threshold voltages.

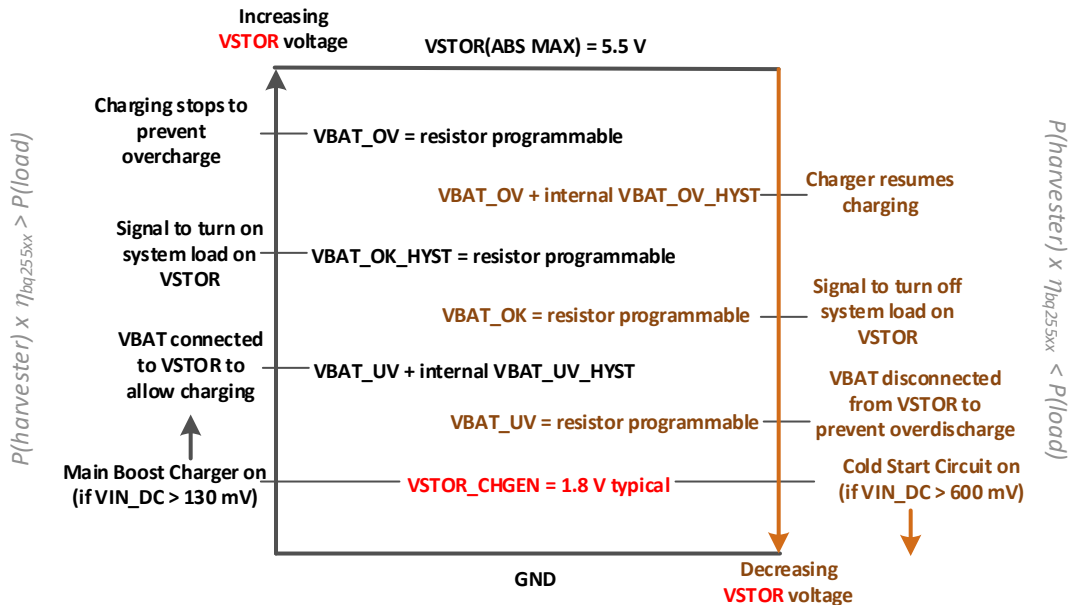


图 8-1. Summary of VSTOR Threshold Voltages

### 8.3.5 Nano-Power Management and Efficiency

The high efficiency of the BQ25504 charger is achieved via the proprietary Nano-Power management circuitry and algorithm. This feature essentially samples and holds the VSTOR voltage in order to reduce the average quiescent current. That is, the internal circuitry is only active for a short period of time and then off for the remaining period of time at the lowest feasible duty cycle. A portion of this feature can be observed in 图 9-6 where the VRDIV node is monitored. Here the VRDIV node provides a connection to the VSTOR voltage (first pulse) and then generates the reference levels for the VBAT\_OV and VBAT\_OK resistor dividers for a short period of time. The divided down values at each pin are compared against VBIAS as part of the hysteric control. Since this biases a resistor string, the current through these resistors is only active when the Nano-Power management circuitry makes the connection—hence reducing the overall quiescent current due to the resistors. This process repeats every 64 ms.

The BQ25504 boost charger efficiency is shown for various input power levels in 图 7-1 through 图 7-7. All data points were captured by averaging the overall input current. This must be done due to the periodic biasing scheme implemented via the Nano-Power management circuitry. In order to properly measure the resulting input current when calculating the output to input efficiency, the input current efficiency data was gathered using

a source meter set to average over at least 50 samples. Quiescent current curves into VSTOR over temperature and voltage is shown at [Figure 7-8](#).

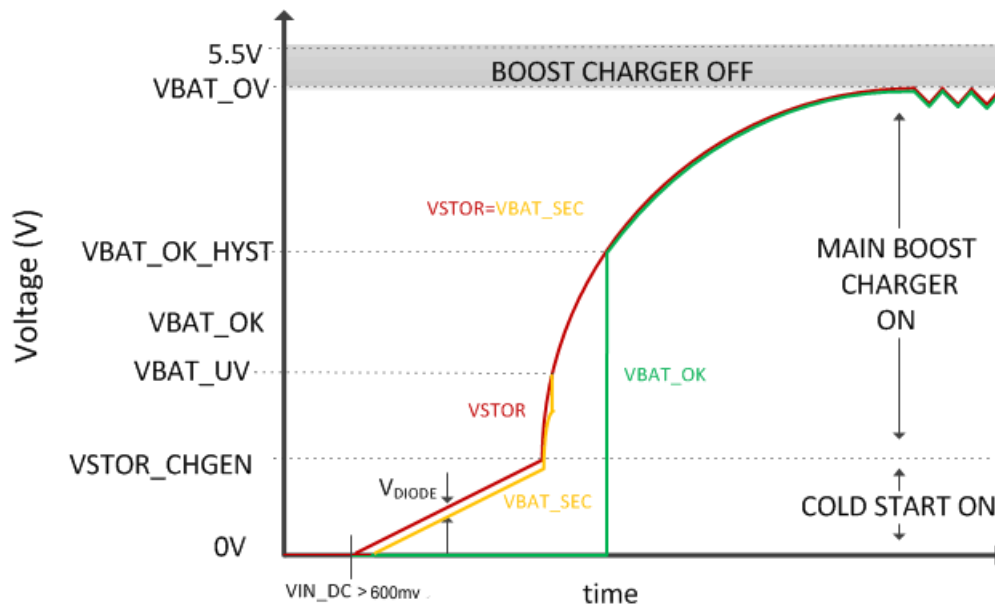
## 8.4 Device Functional Modes

The BQ25504 has three functional modes: cold-start operation, main boost charger enabled and thermal shutdown. The cold start circuitry is powered from VIN\_DC. The main boost charger circuitry is powered from VSTOR while the boost power stage is powered from VIN\_DC. Details of entering and exiting each mode are explained below.

### 8.4.1 Cold-Start Operation (VSTOR < VSTOR\_CHGEN, VIN\_DC > VIN(CS) and PIN > PIN(CS))

Whenever  $V_{STOR} < V_{STOR\_CHGEN}$ ,  $V_{IN\_DC} \geq V_{IN(CS)}$  and  $P_{IN} > P_{IN(CS)}$ , the cold-start circuit is on. This could happen when there is not input power at VIN\_DC to prevent the load from discharging the battery or during a large load transient on VSTOR. During cold start, the voltage at VIN\_DC is clamped to VIN(CS) so the energy harvester's output current is critical to providing sufficient cold start input power,  $P_{IN(CS)} = V_{IN(CS)} \times I_{IN(CS)}$ . The cold-start circuit is essentially an unregulated, hysteretic boost converter with lower efficiency compared to the main boost charger. None of the other features function during cold start operation. The cold start circuit's goal is to charge VSTOR higher than VSTOR\_CHGEN so that the main boost charger can operate. When a depleted storage element is initially attached to VBAT, as shown in [Figure 8-2](#) and the harvester can provide a voltage  $> V_{IN(CS)}$  and total power at least  $> P_{IN(CS)}$ , assuming minimal system load or leakage at VSTOR and VBAT, the cold start circuit can charge VSTOR above VSTOR\_CHGEN. Once the VSTOR voltage reaches the VSTOR\_CHGEN threshold, the IC

1. first performs an initialization pulse on VRDIV to reset the feedback voltages,
2. then disables the charger for 32 ms (typical) to allow the VIN\_DC voltage to rise to the harvester's open-circuit voltage which will be used as the input voltage regulation reference voltage until the next MPPT sampling cycle and
3. lastly performs its first feedback sampling using VRDIV, approximately 64 ms after the initialization pulse.



**Figure 8-2. Charger Operation After a Depleted Storage Element is Attached and Harvester is Available**

The energy harvester must supply sufficient power for the IC to exit cold start. Due to the body diode of the PFET connecting VSTOR and VBAT, the cold start circuit must charge both the capacitor on CSTOR up to the VSTOR\_CHGEN and the storage element connected to VBAT up to VSTOR\_CHGEN less a diode drop. When a rechargeable battery with an open protector is attached, the initial charge time is typically short due to the minimum charge needed to close the battery's protector FETs. When large, discharged super capacitors with high DC leakage currents are attached, the initial charge time can be significant.

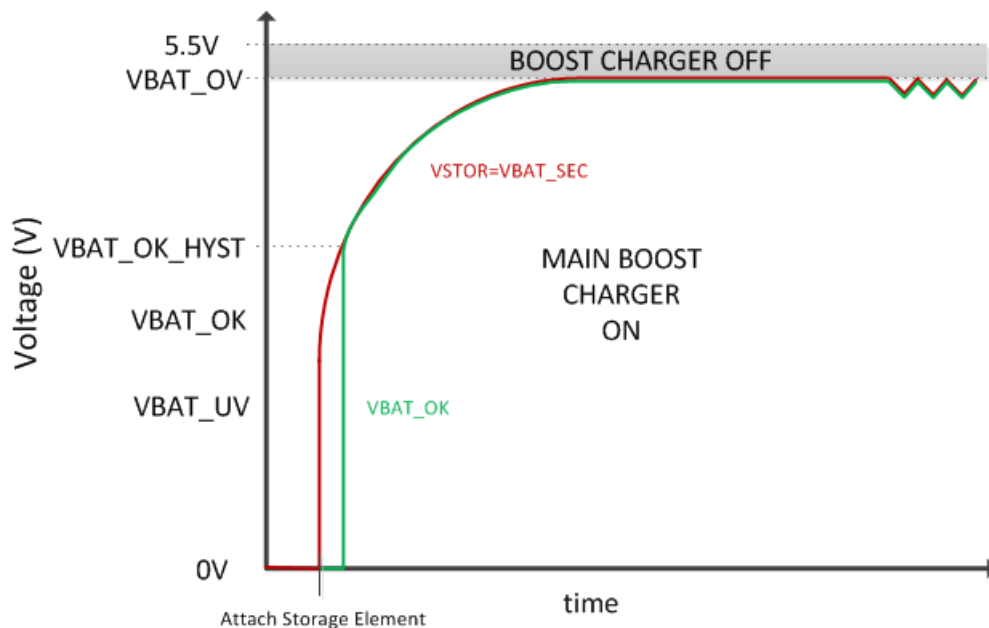


When the VSTOR voltage reaches VSTOR\_CHGEN, the main boost charger starts up. When the VSTOR voltage rises to the VBAT\_UV threshold, the PMOS switch between VSTOR and VBAT turns on, which provides additional loading on VSTOR and could result in the VSTOR voltage dropping below both the VBAT\_UV threshold and the VSTOR\_CHGEN voltage, especially if system loads on VSTOR or VBAT are active during this time. Therefore, it is not uncommon for the VSTOR voltage waveform to have incremental pulses (i.e. stair steps) as the IC cycles between cold-start and main boost charger operation before eventually maintaining VSTOR above VSTOR\_CHGEN.

The cold start circuit initially clamps VIN\_DC to VIN(CS) = 600 mV typical. If sufficient input power (i.e., output current from the harvester clamped to VIN(CS)) is not available, it is possible that the cold start circuit cannot raise the VSTOR voltage above VSTOR\_CHGEN in order for the main boost converter to start up. It is highly recommended to add an external PFET between the system load and VSTOR. An inverted VBAT\_OK signal can be used to drive the gate of this system-isolating, external PFET. See the [セクション 10](#) section for guidance on minimum input power requirements.

#### 8.4.2 Main Boost Charger Enabled (VSTOR > VSTOR\_CHGEN, VIN\_DC > VIN(DC) and $\overline{EN}$ = LOW)

One way to avoid cold start is to attach a partially charged storage element as shown in [図 8-3](#).



**図 8-3. Charger Operation after a Partially Charged Storage Element is Attached and Harvester Power is Available**

When no input source is attached, the VSTOR node should be discharged to ground before attaching a storage element. Hot-plugging a storage element that is charged (e.g., the battery protector PFET is closed) and with the VSTOR node more than 100 mV above ground results in the PFET between VSTOR and VBAT remaining off until an input source is attached.

Assuming the voltages on VSTOR and VBAT are both below 100mV, when a charged storage element is attached (i.e. hot-plugged) to VBAT, the IC.

1. first turns on the internal PFET between the VSTOR and VBAT pins for  $t_{BAT\_HOT\_PLUG}$  (45ms) in order to charge VSTOR to VSTOR\_CHGEN then turns off the PFET to prevent the battery from overdischarge,
2. then performs an initialization pulse on VRDIV to reset the feedback voltages,
3. then disables the charger for 32 ms (typical) to allow the VIN\_DC voltage to rise to the harvester's open-circuit voltage which will be used as the input voltage regulation reference voltage until the next MPPT sampling cycle and
4. lastly performs its first feedback sampling using VRDIV, approximately 64 ms after the initialization pulse.

If the VSTOR pin voltage remains above the internal under voltage threshold (VBAT\_UV) for the additional 64 ms after the VRDIV initialization pulse (following the 45-ms PFET on time), the internal PFET turns back on and the main boost charger begins to charge the storage element assuming there is sufficient power available from the harvester at the VIN\_DC pin. If VSTOR does not reach the VBAT\_UV threshold, then the PFET remains off until the main boost charger can raise the VSTOR voltage to VBAT\_UV. If a system load tied to VSTOR discharges VSTOR below VSTOR\_GEN or below VBAT\_UV during the 32 ms initial MPPT reference voltage measurement or within 110 ms after hot plug, it is recommended to add an external PFET between the system load and VSTOR. An inverted VBAT\_OK signal can be used to drive the gate of this system-isolating, external PFET. Otherwise, the VSTOR voltage waveform will have incremental pulses as the IC turns on and off the internal PFET controlled by VBAT\_UV or cycles between cold-start and main boost charger operation.

Once VSTOR is above VSTOR\_CHGEN, the main boost charger employs pulse frequency modulation (PFM) mode of control to regulate the voltage at VIN\_DC close to the desired reference voltage. The reference voltage is set by the MPPT control scheme as described in the features section. Input voltage regulation is obtained by transferring charge from the input to VSTOR only when the input voltage is higher than the voltage on pin VREF\_SAMP. The current through the inductor is controlled through internal current sense circuitry. The peak current in the inductor is dithered internally to up to three pre-determined levels in order to maintain high efficiency of the charger across a wide input current range. The charger transfers up to a maximum of 100 mA average input current (230mA typical peak inductor current). The boost charger is disabled when the voltage on VSTOR reaches the user set VBAT\_OV threshold to protect the battery connected at VBAT from overcharging. In order for the battery to charge to VBAT\_OV, the input power must exceed the power needed for the load on VSTOR. See the [セグション 10](#) section for guidance on minimum input power requirements.

Steady state operation for the boost charger is shown in [図 9-3](#). These plots highlight the inductor current, the VSTOR voltage ripple, input voltage regulation and the LBOOST switching node. The cycle-by-cycle minor switching frequency is a function of the boost converter's inductor value, peak current limit and voltage levels on each side of each inductor. Once the VSTOR capacitor, CSTOR, droops below a minimum value, the hysteretic switching repeats.

#### 注意

If VIN\_DC is higher than VSTOR and VSTOR is higher than VBAT\_OV, the input VIN\_DC is pulled to ground through a small resistance to stop further charging of the attached battery or capacitor. It is critical that if this case is expected, the impedance of the source attached to VIN\_DC be higher than 20  $\Omega$  and not a low impedance source.

### 8.4.3 Thermal Shutdown

Rechargeable Li-ion batteries need protection from damage due to operation at elevated temperatures. The application should provide this battery protection and ensure that the ambient temperature is never elevated greater than the expected operational range of 85°C.

The BQ25504 uses an integrated temperature sensor to monitor the junction temperature of the device. If the OT\_PROG pin is tied low, then the temperature threshold for thermal protection is set to TSD\_ProgL which is 65°C typically. If the OT\_PROG is tied high, then the temperature is set to TSD\_ProgH which is 120°C typically. Once the temperature threshold is exceeded, the boost converter/charger is disabled and charging ceases. Once the temperature of the device drops below this threshold, the boost converter and or charger can resume operation. To avoid unstable operation near the overtemp threshold, a built-in hysteresis of approximately 5°C has been implemented. Care should be taken to not over discharge the battery in this condition since the boost converter/charger is disabled. However, if the supply voltage drops to the VBAT\_UV setting, then the switch between VBAT and VSTOR will open and protect the battery even if the device is in thermal shutdown.

## 9 Application and Implementation

### 注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

### 9.1 Application Information

#### 9.1.1 Storage Element Selection

In order for the charge management circuitry to protect the storage element from over-charging or discharging, the storage element must be connected to VBAT pin and the system load tied to the VSTOR pin. Many types of elements can be used, such as capacitors, super capacitors or various battery chemistries. A storage element with 100 uF equivalent capacitance is required to filter the pulse currents of the PFM switching charger. The equivalent capacitance of a battery can be computed as computed as:

$$C_{EQ} = 2 \times \text{mAHr}_{\text{BAT(CHRGD)}} \times 3600 \text{ s/Hr} / V_{\text{BAT(CHRGD)}} \quad (6)$$

In order for the storage element to be able to charge VSTOR capacitor (CSTOR) within the  $t_{\text{VB\_HOT\_PLUG}}$  (50 ms typical) window at hot-plug; therefore preventing the IC from entering cold start, the time constant created by the storage element's series resistance (plus the resistance of the internal PFET switch) and equivalent capacitance must be less than  $t_{\text{VB\_HOT\_PLUG}}$ . For example, a battery's resistance can be computed as:

$$R_{\text{BAT}} = V_{\text{BAT}} / I_{\text{BAT(CONTINUOUS)}} \text{ from the battery specifications.} \quad (7)$$

The storage element must be sized large enough to provide all of the system load during periods when the harvester is no longer providing power. The harvester is expected to provide at least enough power to fully charge the storage element while the system is in low power or sleep mode. Assuming no load on VSTOR (i.e., the system is in low power or sleep mode), the following equation estimates charge time from voltage VBAT1 to VBAT2 for given input power is:

Refer to [SLUC462](#) for a design example that sizes the storage element.

$$P_{\text{IN}} \times \eta_{\text{EST}} \times t_{\text{CHRG}} = 1/2 \times C_{\text{EQ}} \times (V_{\text{BAT2}}^2 - V_{\text{BAT1}}^2) \quad (8)$$

Note that if there are large load transients or the storage element has significant impedance then it may be necessary to increase the CSTOR capacitor from the 4.7uF minimum or add additional capacitance to VBAT in order to prevent a droop in the VSTOR voltage. See below for guidance on sizing capacitors.

#### 9.1.2 Inductor Selection

The boost charger needs an appropriately sized inductor for proper operation. The inductor's saturation current should be at least 25% higher than the expected peak inductor currents recommended below if system load transients on VSTOR are expected. Since this device uses hysteretic control, the boost charger is considered naturally stable systems (single order transfer function).

For the boost charger to operate properly, an inductor of appropriate value must be connected between LBOOST, pin 20, and VIN\_DC, pin 2. The boost charger internal control circuitry is designed to control the switching behavior with a nominal inductance of 22  $\mu\text{H} \pm 20\%$ . The inductor must have a peak current capability of > 300 mA with a low series resistance (DCR) to maintain high efficiency.

A list of inductors recommended for this device is shown in [表 9-1](#).

**表 9-1. Recommended Inductors**

INDUCTANCE ( $\mu\text{H}$ )	DIMENSIONS (mm)	PART NUMBER	MANUFACTURER <sup>(1)</sup>
22	4.0x4.0x1.7	LPS4018-223M	Coilcraft
22	3.8x3.8x1.65	744031220	Würth

**表 9-1. Recommended Inductors (continued)**

INDUCTANCE (μH)	DIMENSIONS (mm)	PART NUMBER	MANUFACTURER <sup>(1)</sup>
22	2.8x2.8x2.8	744025220	Würth

(1) See **WHAT?** concerning recommended third-party products.

### 9.1.3 Capacitor Selection

In general, all the capacitors need to be low leakage. Any leakage the capacitors have will reduce efficiency, increase the quiescent current and diminish the effectiveness of the IC for energy harvesting.

#### 9.1.3.1 VREF\_SAMP Capacitance

The MPPT operation depends on the sampled value of the open circuit voltage and the input regulation follows the voltage stored on the CREF capacitor. This capacitor is sensitive to leakage since the holding period is around 16 seconds. As the capacitor voltage drops due to any leakage, the input regulation voltage also drops preventing proper operation from extraction the maximum power from the input source. Therefore, it is recommended that the capacitor be an X7R or COG low leakage capacitor.

#### 9.1.3.2 VIN\_DC Capacitance

Energy from the energy harvester input source is initially stored on a capacitor, CIN, connected to VIN\_DC, pin 2, and VSS, pin 1. For energy harvesters which have a source impedance which is dominated by a capacitive behavior, the value of the harvester capacitor should scaled according to the value of the output capacitance of the energy source, but a minimum value of 4.7 μF is recommended.

#### 9.1.3.3 VSTOR Capacitance

Operation of the BQ25504 requires two capacitors to be connected between VSTOR, pin 15, and VSS, pin 1. A high frequency bypass capacitor of at 0.1 μF should be placed as close as possible between VSTOR and VSS. In addition, a low ESR capacitor of at least 4.7 μF should be connected in parallel.

#### 9.1.3.4 Additional Capacitance on VSTOR or VBAT

If there are large, fast system load transients and/or the storage element has high resistance, then the CSTOR capacitors may momentarily discharge below the VBAT\_UV threshold in response to the transient. This causes the BQ25504 to turn off the PFET switch between VSTOR and VBAT and turn on the boost charger. The CSTOR capacitors may further discharge below the VSTOR\_CHGEN threshold and cause the BQ25504 to enter Cold Start. For instance, some Li-ion batteries or thin-film batteries may not have the current capacity to meet the surge current requirements of an attached low power radio. To prevent VSTOR from drooping, either increasing the CSTOR capacitance or adding additional capacitance in parallel with the storage element is recommended. For example, if boost charger is configured to charge the storage element to 4.2 V and a 500 mA load transient of 50 μs duration infrequently occurs, then, solving  $I = C \times dv/dt$  for CSTOR gives:

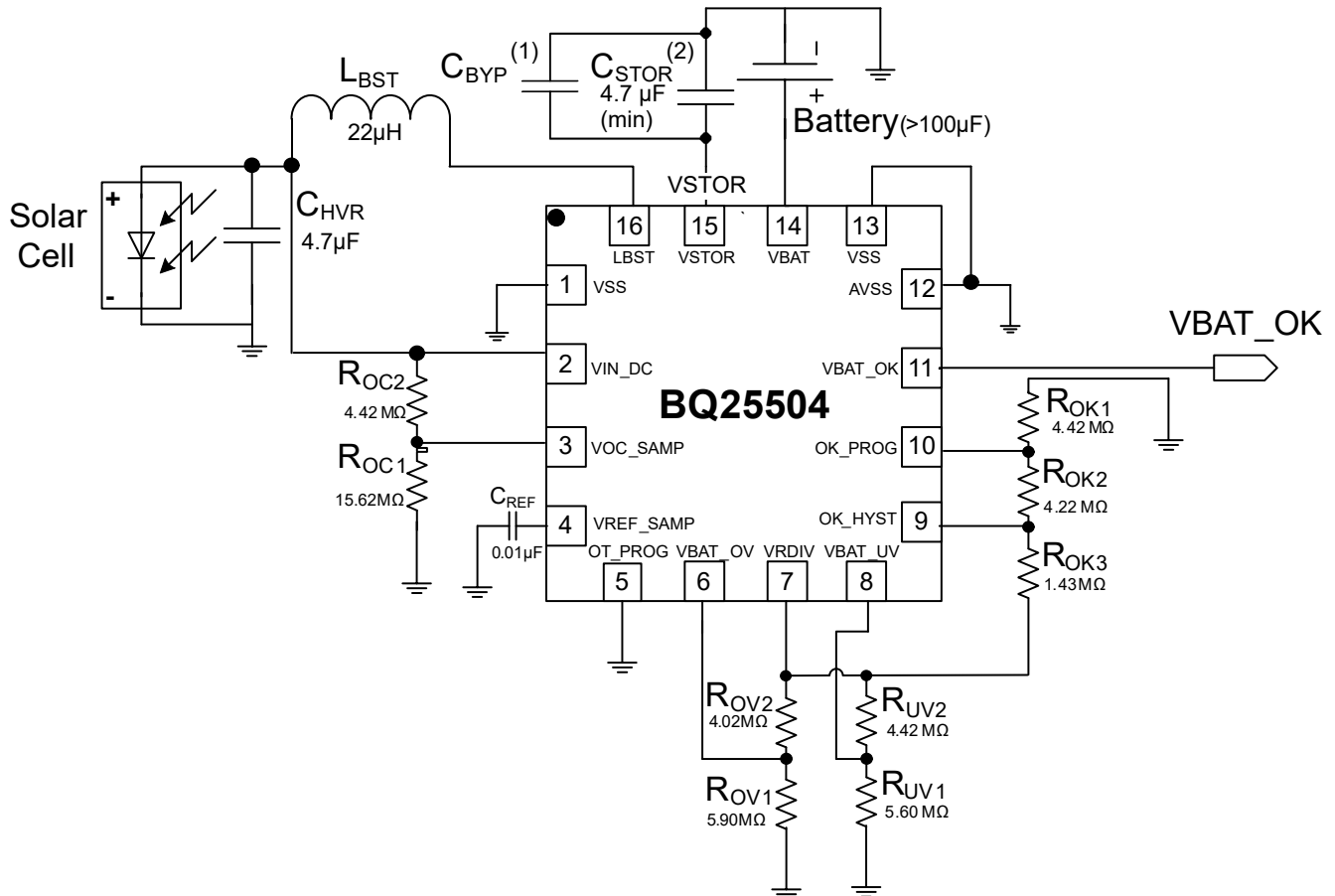
$$CSTOR \geq \frac{500 \text{ mA} \times 50 \text{ } \mu\text{s}}{(4.2 \text{ V} - 1.8 \text{ V})} = 10.5 \text{ } \mu\text{F} \quad (9)$$

Note that increasing CSTOR is the recommended solution but will cause the boost charger to operate in the less efficient cold start mode for a longer period at startup compared to using CSTOR = 4.7 μF. If longer cold start run times are not acceptable, then place the additional capacitance in parallel with the storage element.

For a recommended list of standard components, see the EVM User's Guide ([SLUUA8](#)).

## 9.2 Typical Applications

### 9.2.1 Solar Application Circuit



- Place close as possible to IC pin 15 (VSTOR) and pin 13 (VSS)
- See the Capacitor Selection section for guidance on sizing  $C_{STOR}$

**9-1. Typical Solar Application Circuit**

#### 9.2.1.1 Design Requirements

The desired voltage levels are  $V_{BAT\_OV} = 3.15$  V,  $V_{BAT\_UV} = 2.20$  V,  $V_{BAT\_OK} = 2.44$  V,  $V_{BAT\_OK\_HYST} = 2.80$  V and MPP ( $V_{OC}$ ) = 78% which is typical for solar panels. There are no large load transients expected. The IC must stop charging if its junction temperature is above 65°C. The simulated solar panel open circuit voltage is 1.0 V.

#### 9.2.1.2 Detailed Design Procedure

The recommended  $L_1 = 22$  μH,  $C_{BYP} = 0.01$  μF and low leakage  $C_{REF} = 10$  nF are selected. In order to ensure the fastest recovery of the harvester output voltage to the MPPT level following power extraction, the minimum recommended  $C_{IN} = 4.7$  μF is selected. Because no large system load transients are expected and to ensure fast charge time during cold start, the minimum recommended  $C_{STOR} = 4.7$  μF. To stop charging when the IC junction temperature is above 65°C, the OT\_PROG pin is tied to ground.

- With  $V_{BAT\_UV} < V_{BAT\_OV} \leq 5.5$  V, to size the VBAT\_OV resistors, first choose  $R_{SUM\_OV} = R_{OV1} + R_{OV2} = 10$  MΩ then solve Equation 3 for

$$R_{OV1} = \frac{3}{2} \times \frac{RSUM_{OV} \times VBIAS}{VBAT_{OV}} \times \frac{3}{2} \frac{10 \text{ M}\Omega \times 1.25 \text{ V}}{3.15 \text{ V}} = 5.95 \text{ M}\Omega \rightarrow 5.90 \text{ M}\Omega \text{ closest 1\% value then} \quad (10)$$

- $R_{OV2} = RSUM_{OV} - R_{OV1} = 10 \text{ M}\Omega - 5.95 \text{ M}\Omega = 4.05 \text{ M}\Omega \rightarrow 4.02 \text{ M}\Omega$  resulting in  $VBAT_{OV} = 3.15 \text{ V}$
- To size the  $VBAT_{UV}$  resistors, first choose  $RSUM_{UV} = R_{UV1} + R_{UV2} = 10 \text{ M}\Omega$  then solve 式 2 for

$$R_{UV1} = \frac{RSUM_{UV} \times VBIAS}{VBAT_{UV}} = \frac{10 \text{ M}\Omega \times 1.25 \text{ V}}{2.2 \text{ V}} = 5.68 \text{ M}\Omega \rightarrow 5.60 \text{ M}\Omega \text{ closest 1\% value then} \quad (11)$$

- $R_{UV2} = RSUM_{UV} - R_{UV1} = 10 \text{ M}\Omega - 5.60 \text{ M}\Omega = 4.4 \text{ M}\Omega \rightarrow 4.42 \text{ M}\Omega$  closest 1% resistor resulting in  $VBAT_{UV} = 2.2 \text{ V}$ .
- With  $VBAT_{OV} \geq VBAT_{OK\_HYST} > VBAT_{OK} \geq VBAT_{UV}$ , to size the  $VBAT_{OK}$  and  $VBAT_{OK\_HYST}$  resistors, first choose  $RSUM_{OK} = R_{OK1} + R_{OK2} + R_{OK3} = 10 \text{ M}\Omega$  then solve Equation 4 and Equation 5 for

$$R_{OK1} = \frac{VBIAS \times RSUM_{OK}}{VBAT_{OK\_HYST}} = \left( \frac{1.25 \text{ V}}{2.8 \text{ V}} \right) \times 10 \text{ M}\Omega = 4.46 \text{ M}\Omega \rightarrow 4.42 \text{ M}\Omega \text{ closest 1\% resistor then} \quad (12)$$

$$R_{OK2} = \left( \frac{VBAT_{OK\_PROG}}{VBIAS} - 1 \right) \times R_{OK1} = \left( \frac{2.45 \text{ V}}{1.25 \text{ V}} - 1 \right) \times 4.42 \text{ M}\Omega = 4.07 \text{ M}\Omega, \text{ then} \quad (13)$$

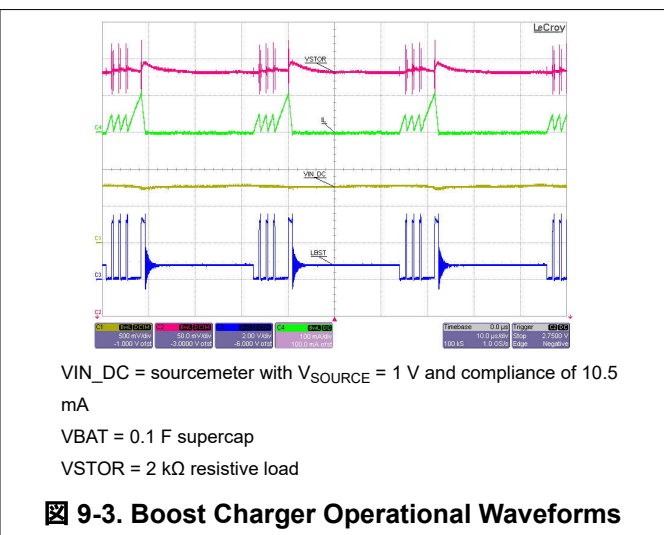
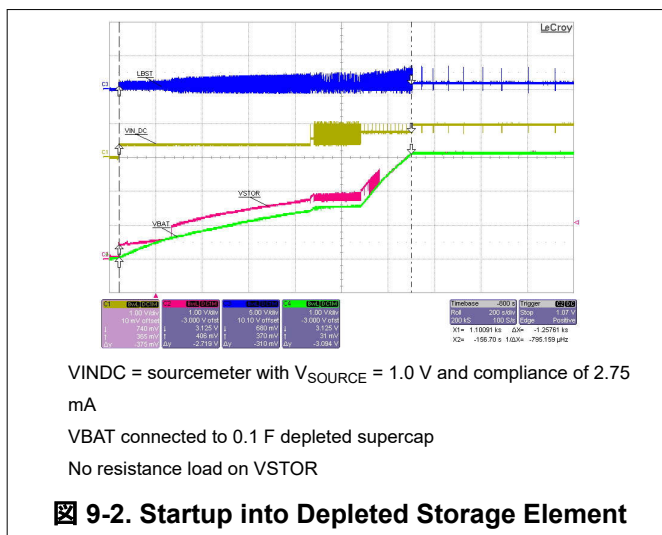
- $R_{OK3} = RSUM_{OK} - R_{OK1} - R_{OK2} = 10 \text{ M}\Omega - 4.42 \text{ M}\Omega - 4.22 \text{ M}\Omega = 1.36 \text{ M}\Omega \rightarrow 1.43 \text{ M}\Omega$  to give  $VBAT_{OK} = 2.44 \text{ V}$  and  $VBAT_{OK\_HYST} = 2.85 \text{ V}$ .
- Keeping in mind that  $VREF\_SAMP$  stores the MPP voltage for the harvester, first choose  $RSUM_{OC} = R_{OC1} + R_{OC2} = 20 \text{ M}\Omega$  then solve Equation 1 for

$$R_{OC1} = \left( \frac{VREF\_SAMP}{VIN\_DC(OC)} \right) \times RSUM_{OC} = 0.78 \times 20 \text{ M}\Omega = 15.6 \text{ M}\Omega, \text{ then} \quad (14)$$

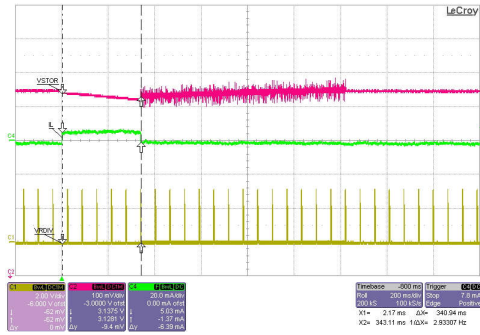
$$R_{OC2} = RSUM_{OC} \times \left( 1 - \frac{VREF\_SAMP}{VIN\_DC(OC)} \right) = 20 \text{ M}\Omega (1 - 0.78) = 4.4 \text{ M}\Omega \text{ closest 1\% resistors} \quad (15)$$

- **SLURAQ1** provides help on sizing and selecting the resistors.

### 9.2.1.3 Application Curves

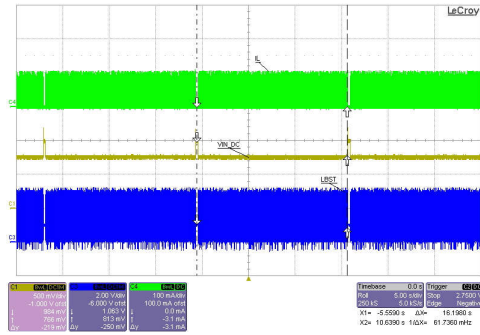






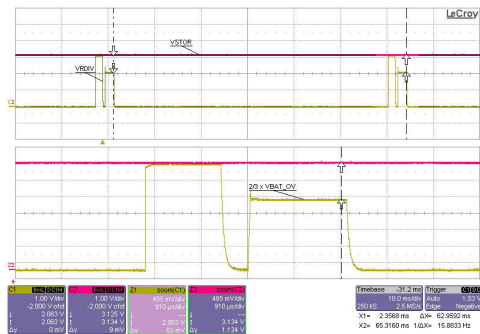
VIN\_DC = sourcemeter with  $V_{SOURCE} = 1\text{ V}$  and compliance of 10.5 mA  
 VBAT = 0.1 F supercap  
 VSTOR = open to 500  $\Omega$  to open resistive load (IL = load current on VSTOR)

**图 9-4. 5 mA Load Transient on VSTOR**



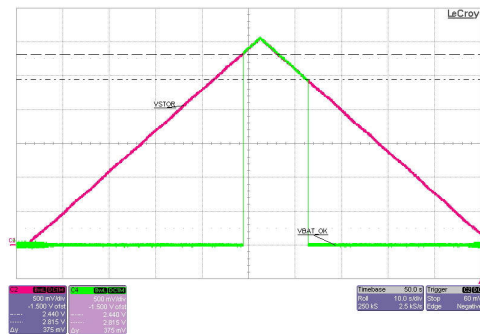
VIN\_DC = sourcemeter with  $V_{SOURCE} = 1\text{ V}$  and compliance of 10.5 mA  
 VBAT = sourcemeter with  $V_{SOURCE} = 2.8\text{ V}$  and compliance of 1A  
 IL = inductor current

**图 9-5. MPPT Operation**



VIN\_DC = sourcemeter with  $V_{SOURCE} = 1\text{ V}$  and compliance of 10.5 mA  
 VBAT = sourcemeter with  $V_{SOURCE} = 2.8\text{ V}$  and compliance of 1A

**图 9-6. VRDIV Operation**

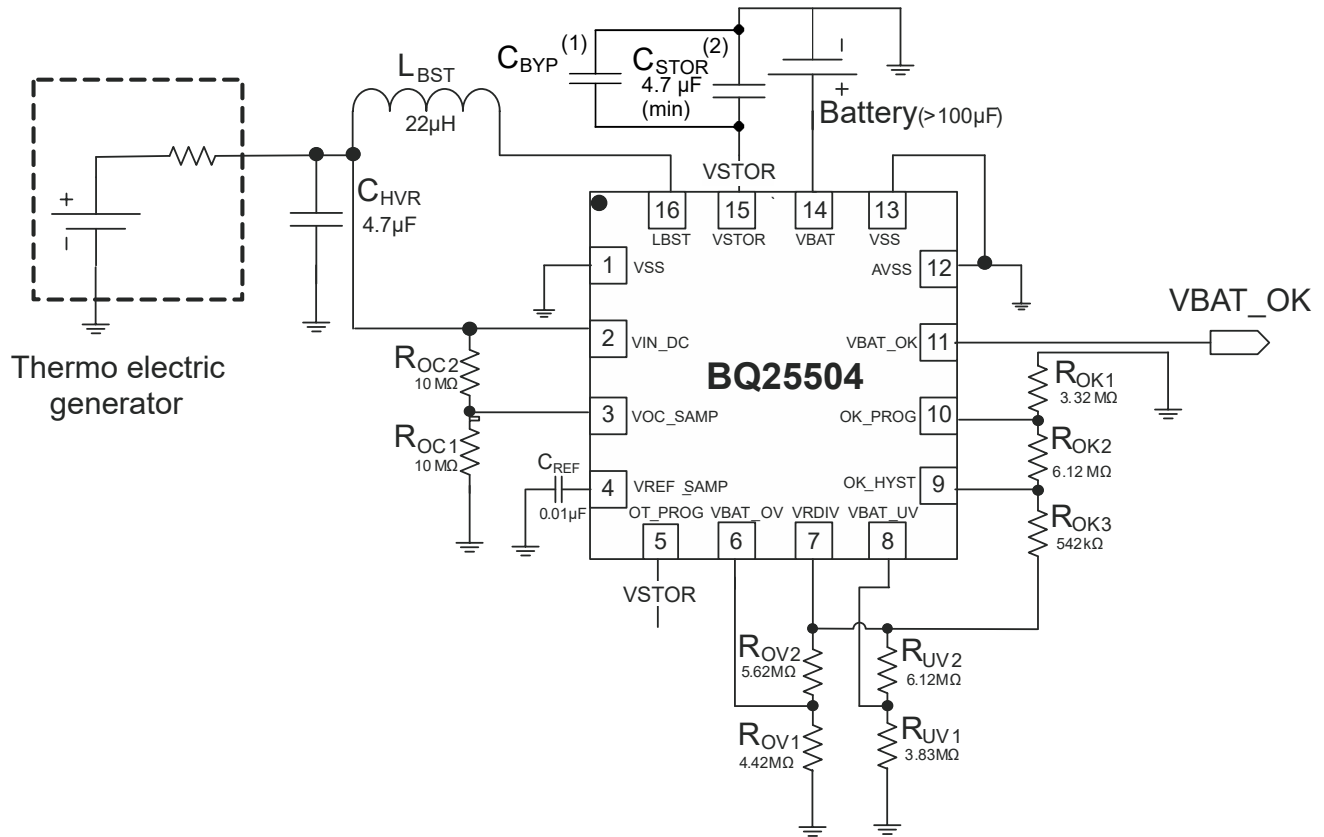


VIN\_DC = sourcemeter with  $V_{SOURCE} = 1\text{ V}$  and compliance of 2.75 mA  
 No storage element on VBAT  
 VSTOR artificially ramped from 0V to 3.15 V to 0 V using a power amp driven by a function generator

**图 9-7. VBAT\_OK Operation**



## 9.2.2 TEG Application Circuit



- Place close as possible to IC pin 15 (VSTOR) and pin 13 (VSS)
- See the Capacitor Selection section for guidance on sizing  $C_{STOR}$

9-8. Typical TEG Application Circuit

### 9.2.2.1 Design Requirements

The desired voltage levels are  $V_{BAT\_OV} = 4.25$  V,  $V_{BAT\_UV} = 3.20$  V,  $V_{BAT\_OK} = 3.55$  V,  $V_{BAT\_OK\_HYST} = 3.76$  V and MPP ( $V_{OC}$ ) = 50% which is typical for TEG harvesters. The IC must stop charging if its junction temperature is above 120°C. The simulated TEG open circuit voltage is 1.0 V.

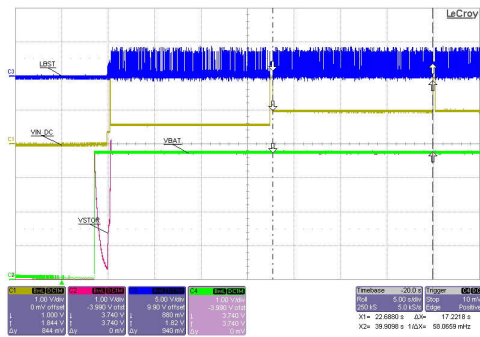
### 9.2.2.2 Detailed Design Procedure

The recommended  $L_1 = 22$   $\mu$ H,  $C_{BYP} = 0.01$   $\mu$ F and low leakage  $C_{REF} = 10$  nF are selected. In order to ensure the fastest recovery of the harvester output voltage to the MPPT level following power extraction, the minimum recommended  $C_{IN} = 4.7$   $\mu$ F is selected. Because no large system load transients are expected and to ensure fast charge time during cold start, the minimum recommended  $C_{STOR} = 4.7$   $\mu$ F. To stop charging when the IC junction temperature is above 120°C, the  $OT\_PROG$  pin is tied to VSTOR.

Referring back to the procedure in [セクション 9.2.1.2](#) or using the spreadsheet calculator at [SLURAQ1](#) gives the following values:

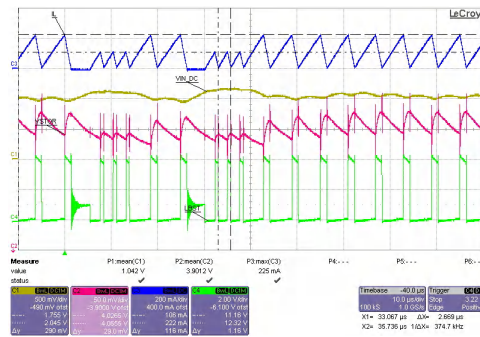
- $R_{OV1} = 4.42$  M $\Omega$ ,  $R_{OV2} = 5.49$  M $\Omega$  resulting in  $V_{BAT\_OV} = 4.26$  V due to rounding to the nearest 1% resistor.
- $R_{UV1} = 3.83$  M $\Omega$ ,  $R_{UV2} = 6.04$  M $\Omega$  resulting in  $V_{BAT\_UV} = 3.22$  V due to rounding to the nearest 1% resistor
- $R_{OK1} = 3.32$  M $\Omega$ ,  $R_{OK2} = 6.04$  M $\Omega$ ,  $R_{OK3} = 0.536$  M $\Omega$  resulting in  $V_{BAT\_OK} = 3.52$  V and  $V_{BAT\_OK\_HYST} = 3.73$  V after rounding.
- $R_{OC1} = 10$  M $\Omega$  and  $R_{OC2} = 10$  M $\Omega$  gives 50% MPP voltage.

### 9.2.2.3 Application Curves



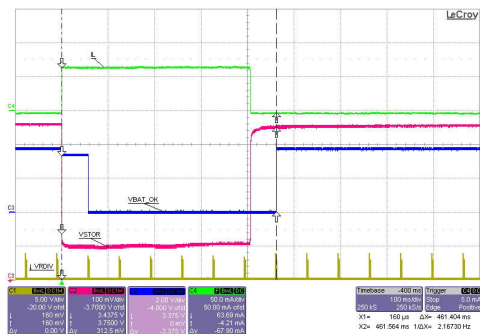
VINDC = sourcemeter with  $V_{SOURCE} = 2.0\text{ V}$  and compliance of 1 mA  
 VBAT connected to Lilon battery  
 VSTOR = 50 kΩ resistor

**9-9. Startup by Attaching Charged Storage Element**



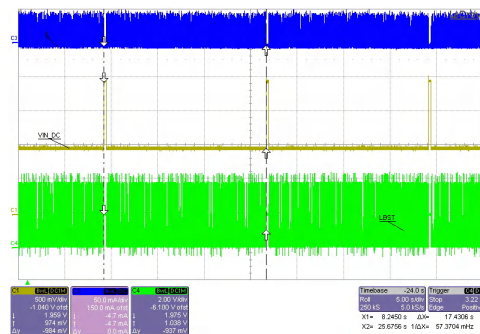
VIN\_DC = sourcemeter with  $V_{SOURCE} = 2.0\text{ V}$  and compliance of 100 mA  
 VBAT connected to Lilon battery  
 VSTOR = 100 kΩ resistive load (IL = inductor current)

**9-10. Boost Charger Operational Waveforms**



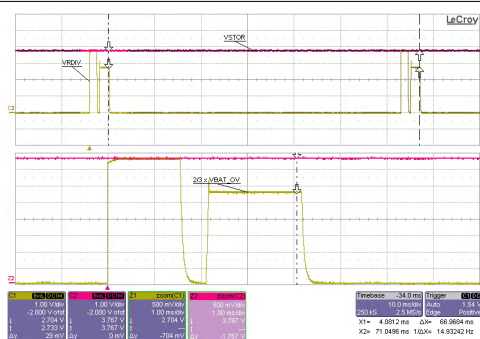
VIN\_DC = sourcemeter with  $V_{SOURCE} = 2.0\text{ V}$  and compliance of 1 mA  
 VBAT connected to Lilon battery  
 VSTOR = open to 50Ω to open resistive load (IL = load current on VSTOR)

**9-11. 50 mA Load Transient on VSTOR**



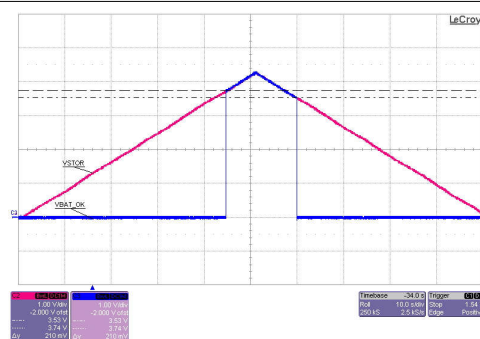
VIN\_DC = sourcemeter with  $V_{SOURCE} = 2.0\text{ V}$  and compliance of 1 mA  
 VBAT connected to Lilon battery  
 IL = inductor current

**9-12. MPPT Operation**



VIN\_DC = sourcemeter with  $V_{SOURCE} = 2.0\text{ V}$  and compliance of 1 mA  
 VBAT connected to Lilon battery

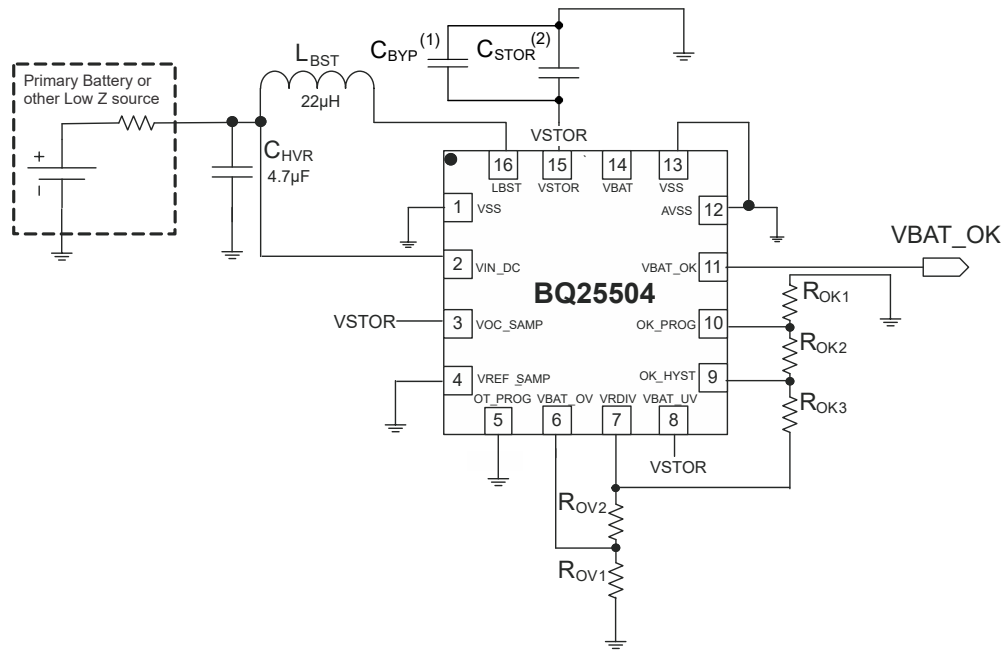
**9-13. VRDIV Operation**



VIN\_DC = sourcemeter with  $V_{SOURCE} = 2.0\text{ V}$  and compliance of 1 mA  
 No storage element on VBAT  
 VSTOR artificially ramped from 0V to 4.25V to 0V using a power amp driven by a function generator

**9-14. VBAT\_OK Operation**

### 9.2.3 MPPT Disabled, Low Impedance Source Application Circuit



- Place close as possible to IC pin 15 (VSTOR) and pin 13 (VSS)
- See the Capacitor Selection section for guidance on sizing  $C_{STOR}$

**图 9-15. Typical MPPT Disabled Application Circuit (Low Iq Boost Converter from Low Impedance Source)**

#### 9.2.3.1 Design Requirements

The input source is a low impedance 1.2 V battery therefore MPPT is not needed. The output will be a low ESR capacitor therefore VSTOR can be tied to VBAT and VBAT\_UV is not needed. The desired voltage levels are VBAT\_OV = 3.30 V, VBAT\_OK = 2.80 V, VBAT\_OK\_HYST = 3.10 V, and MPPT disabled. The IC must stop charging if its junction temperature is above 65°C. Load transients are expected.

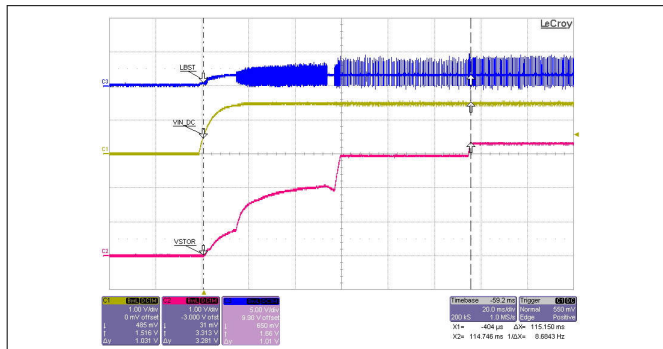
#### 9.2.3.2 Detailed Design Procedure

The recommended  $L_1 = 22 \mu\text{H}$ ,  $C_{BYP} = 0.01 \mu\text{F}$  and low leakage  $C_{REF} = 10 \text{ nF}$  are selected. The minimum recommended  $C_{IN} = 4.7 \mu\text{F}$  is selected. To prevent VSTOR from drooping during system load transients,  $C_{STOR}$  is set to  $100 \mu\text{F}$ . To disable the sampling for MPPT, the VOC\_SAMP pin is tied to VSTOR. To disable the input voltage regulation circuit, the VREF\_SAMP pin is tied to GND. Since the VBAT\_UV function is not needed, the VBAT\_UV can be tied to VSTOR. To stop charging when the IC junction temperature is above 65°C, the OT\_PROG pin is tied to GND.

Referring back to the procedure in [セクション 9.2.1.2](#) or using the spreadsheet calculator at [SLURAQ1](#) gives the following values:

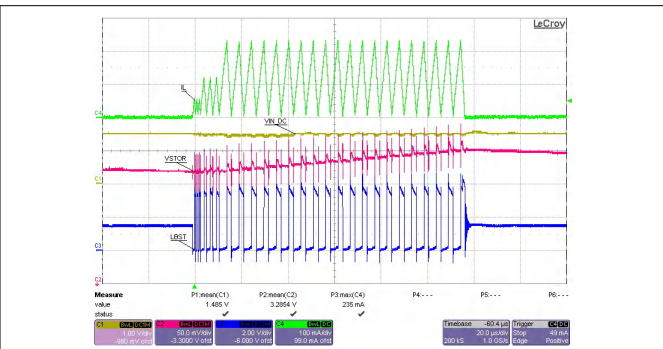
- $R_{OV1} = 5.62 \text{ M}\Omega$ ,  $R_{OV2} = 4.22 \text{ M}\Omega$  resulting in VBAT\_OV = 3.28 V due to rounding to the nearest 1% resistor.
- $R_{OK1} = 4.12 \text{ M}\Omega$ ,  $R_{OK2} = 5.11 \text{ M}\Omega$ ,  $R_{OK3} = 0.976 \text{ M}\Omega$  resulting in VBAT\_OK = 2.80 V and VBAT\_OK\_HYST = 3.10 V after rounding.

### 9.2.3.3 Application Curves



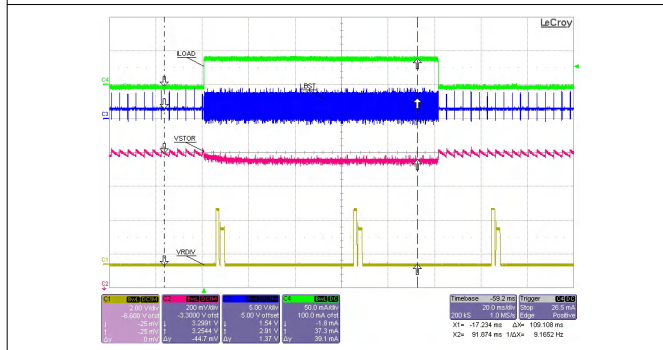
VIN\_DC = low impedance voltage source = 1.5 V  
VBAT = VSTOR = 100  $\mu$ F  
VSTOR = 500  $\Omega$  resistor

**9-16. Startup**



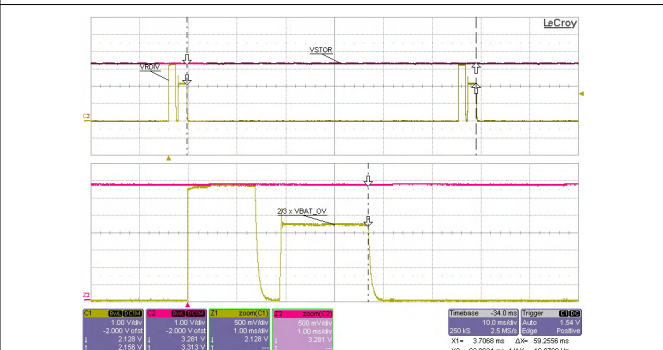
VIN\_DC = low impedance voltage source = 1.5 V  
VBAT = VSTOR = 100  $\mu$ F  
VSTOR = 330  $\Omega$  resistive load (IL = inductor current)

**9-17. Boost Charger Operational Waveforms**



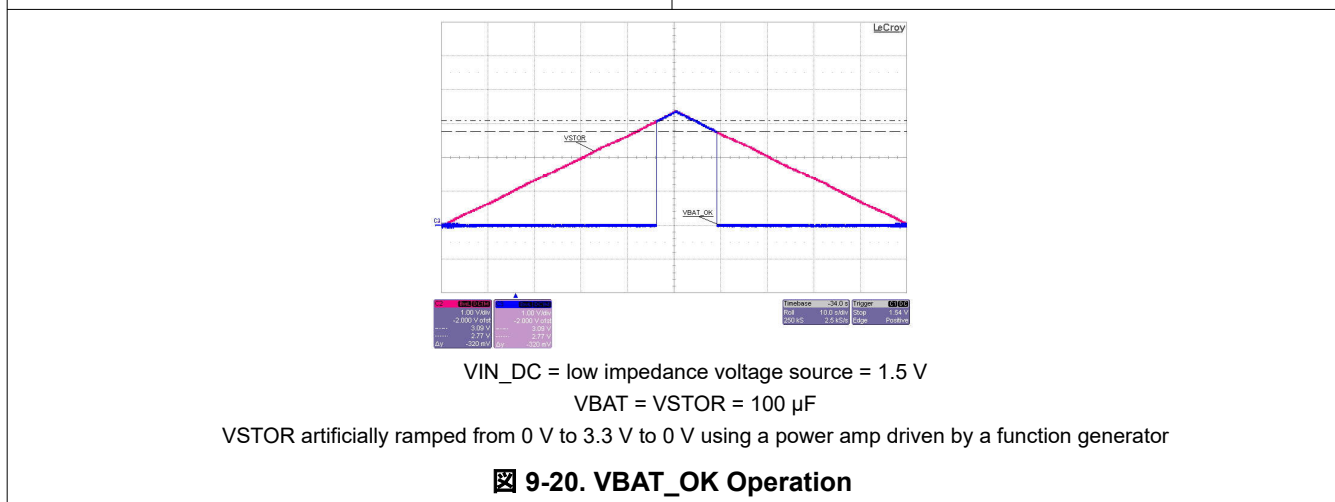
VIN\_DC = low impedance voltage source = 1.5 V )  
VBAT = VSTOR = 100  $\mu$ F  
VSTOR = open to 75  $\Omega$  to open resistive load (IL = load current on VSTOR)

**9-18. 40 mA Load Transient on VSTOR**



VIN\_DC = low impedance voltage source = 1.5 V  
VBAT = VSTOR = 100  $\mu$ F

**9-19. VRDIV Operation**



VIN\_DC = low impedance voltage source = 1.5 V  
VBAT = VSTOR = 100  $\mu$ F  
VSTOR artificially ramped from 0 V to 3.3 V to 0 V using a power amp driven by a function generator

**9-20. VBAT\_OK Operation**

## 10 Power Supply Recommendations

The energy harvesting source (e.g., solar panel, TEG, vibration element) must provide a minimum level of power for the IC to operate as designed. The IC's minimum input power required to exit cold start can be estimated as:

$$P_{IN} > P_{IN}(CS) = V_{IN}(CS) \times I_{IN}(CS) > \frac{(I - STR\_ELM\_LEAK_{@1.8V} \times 1.8V) + \frac{(1.8V)^2}{R_{STOR}(CS)}}{0.05} \quad (16)$$

where  $I - STR\_ELM\_LEAK_{@1.8V}$  is the storage element leakage current at 1.8V and

$R_{STOR}(CS)$  is the equivalent resistive load on  $V_{STOR}$  during cold start and 0.05 is an estimate of the worst case efficiency of the cold start circuit.

Once the IC is out of cold start and the system load has been activated (e.g., using the  $V_{BAT\_OK}$  signal), the energy harvesting element must provide the main boost charger with at least enough power to meet the average system load. Assuming  $R_{STOR}(AVG)$  represents the average resistive load on  $V_{STOR}$ , the simplified **equation below** gives an estimate of the IC's minimum input power needed during system operation:

$$P_{IN} \times \eta_{EST} > P_{LOAD} = \frac{(V_{BAT\_OV})^2}{R_{STOR}(AVG)} + V_{BAT\_OV} \times I - STR\_ELM\_LEAK_{@V_{BAT\_OV}} \quad (17)$$

where  $\eta_{EST}$  can be derived from the datasheet efficiency curves for the given input voltage and current and  $V_{BAT\_OV}$ . The simplified equation above assumes that, while the harvester is still providing power, the system goes into low power or sleep mode long enough to charge the storage element so that it can power the system when the harvester eventually is down. Refer to spreadsheet [SLUC462](#) for a design example that sizes the energy harvester.

## 11 Layout

### 11.1 Layout Guidelines

As for all switching power supplies, the PCB layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the boost charger could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground paths. The input and output capacitors as well as the inductors should be placed as close as possible to the IC. For the boost charger, first priority are the output capacitors, including the 0.1  $\mu\text{F}$  bypass capacitor (CBYP), followed by C<sub>STOR</sub>, which should be placed as close as possible between V<sub>STOR</sub>, pin 15, and V<sub>SS</sub>, pin 1 or 13. Next, the input capacitor, C<sub>IN</sub>, should be placed as close as possible between V<sub>IN\_DC</sub>, pin 2, and V<sub>SS</sub>, pin 1. Last in priority is the boost charger inductor, L<sub>1</sub>, which should be placed close to L<sub>BOOST</sub>, pin 16, and V<sub>IN\_DC</sub>, pin 2 if possible. It is best to use vias and bottom traces for connecting the inductor to its respective pins instead of the capacitors.

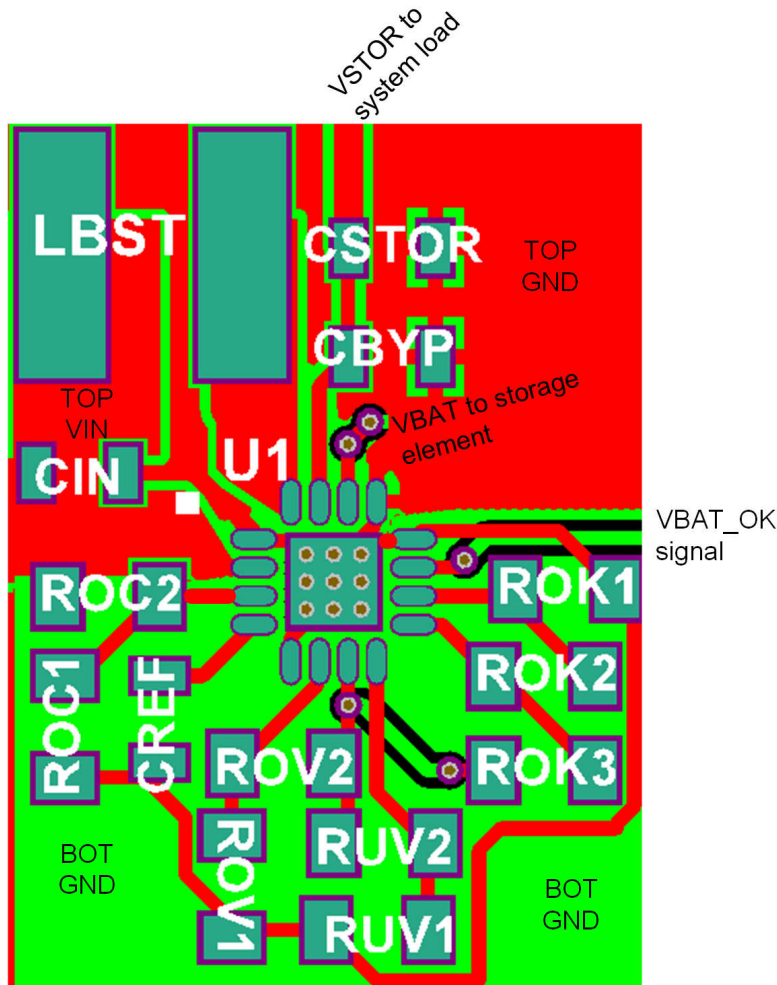
To minimize noise pickup by the high impedance voltage setting nodes (V<sub>BAT\_OV</sub>, V<sub>BAT\_UV</sub>, OK\_PROG, OK\_HYST), the external resistors should be placed so that the traces connecting the midpoints of each divider to their respective pins are as short as possible. When laying out the non-power ground return paths (e.g. from resistors and C<sub>REF</sub>), it is recommended to use short traces as well, separated from the power ground traces and connected to AV<sub>SS</sub> pin 12. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current. The PowerPad should not be used as a power ground return path.

The remaining pins are digital signals with minimal layout restrictions. See [Figure 11-1](#) for an example layout.

In order to maximize efficiency at light load, the use of voltage level setting resistors  $> 1 \text{ M}\Omega$  is recommended. In addition, the sample and hold circuit output capacitor on V<sub>REF\_SAMP</sub> must hold the voltage for 16 s. During board assembly, contaminants such as solder flux and even some board cleaning agents can leave residue that may form parasitic resistors across the physical resistors/capacitors and/or from one end of a resistor/capacitor to ground, especially in humid, fast airflow environments. This can result in the voltage regulation and threshold levels changing significantly from those expected per the installed components. Therefore, it is highly recommended that no ground planes be poured near the voltage setting resistors or the sample and hold capacitor. In addition, the boards must be carefully cleaned, possibly rotated at least once during cleaning, and then rinsed with de-ionized water until the ionic contamination of that water is well above 50 Mohm. If this is not feasible, then it is recommended that the sum of the voltage setting resistors be reduced to at least 5X below the measured ionic contamination.



## 11.2 Layout Example



11-1. Recommended Layout

## 11.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below.

- Improving the power-dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

For more details on how to use the thermal parameters in the Thermal Table, check the Thermal Characteristics Application Note ([SZZA017](#)) and the IC Package Thermal Metrics Application Note ([SPRA953](#)).



## 12 Device and Documentation Support

### 12.1 Device Support

#### 12.1.1 サード・パーティ製品に関する免責事項

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#### 12.1.2 Zip Files

- <http://www.ti.com/lit/zip/SLUC484>
- <http://www.ti.com/lit/zip/SLURAQ1>
- <http://www.ti.com/lit/zip/SLUC462>

### 12.2 Documentation Support

#### 12.2.1 Related Documentation

For related documentation see the following:

- EVM User's Guide, [SLUUAA8](#)
- Thermal Characteristics Application Note, [SZZA017](#)
- IC Package Thermal Metrics Application Note, [SPRA953](#)

### 12.3 ドキュメントの更新通知を受け取る方法

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### 12.7 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ25504RGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B5504	<a href="#">Samples</a>
BQ25504RGTT	ACTIVE	VQFN	RGT	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B5504	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ25504RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ25504RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

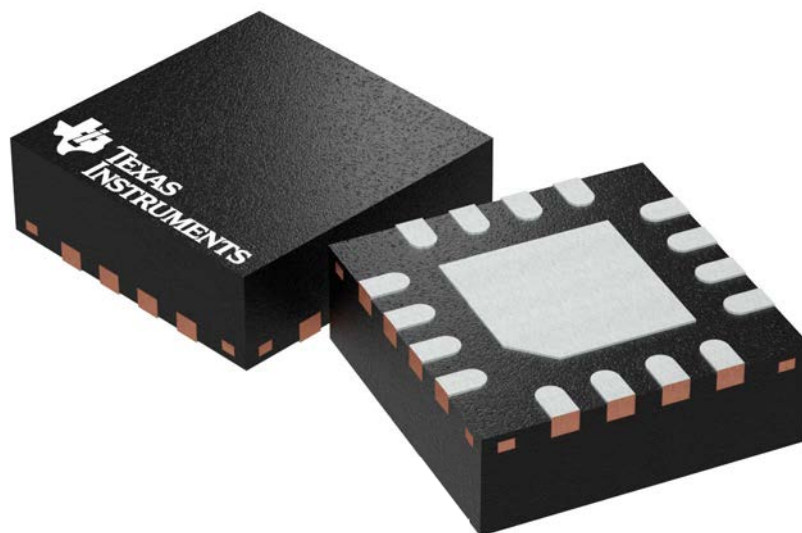
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ25504RGTR	VQFN	RGT	16	3000	346.0	346.0	33.0
BQ25504RGTT	VQFN	RGT	16	250	210.0	185.0	35.0

**RGT 16**

**GENERIC PACKAGE VIEW**

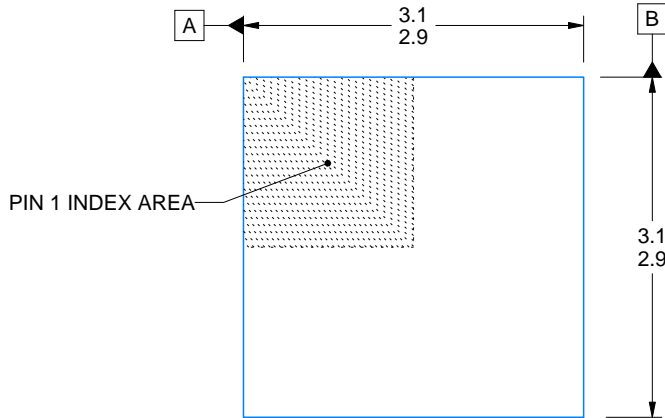
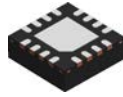
**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD

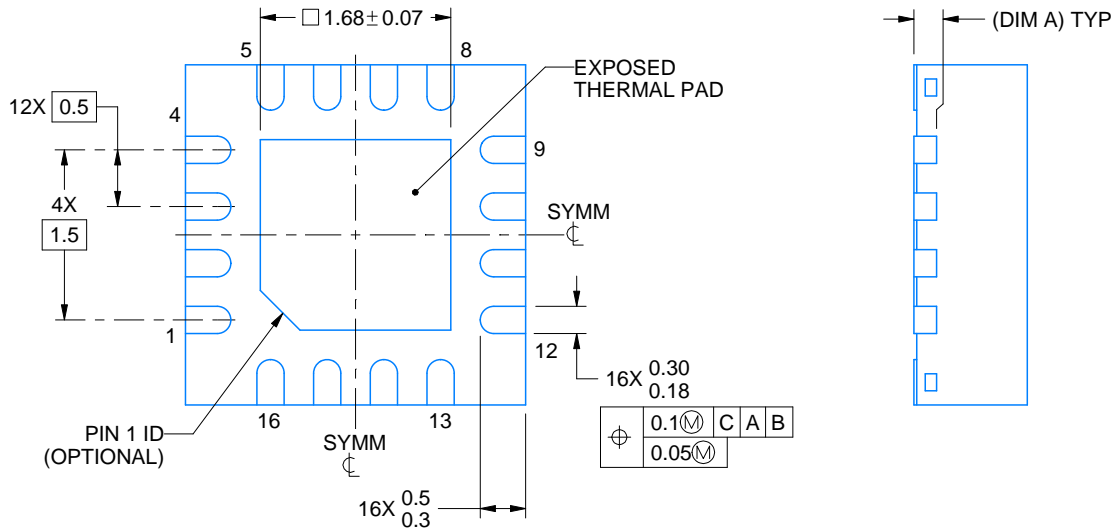
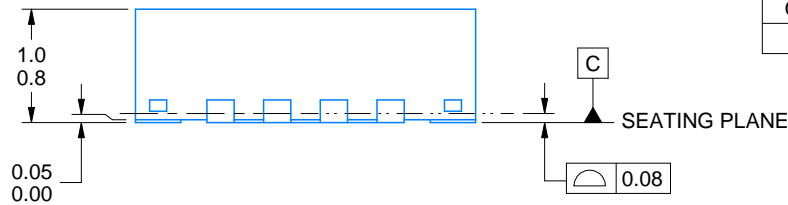


Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4203495/1



SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2



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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



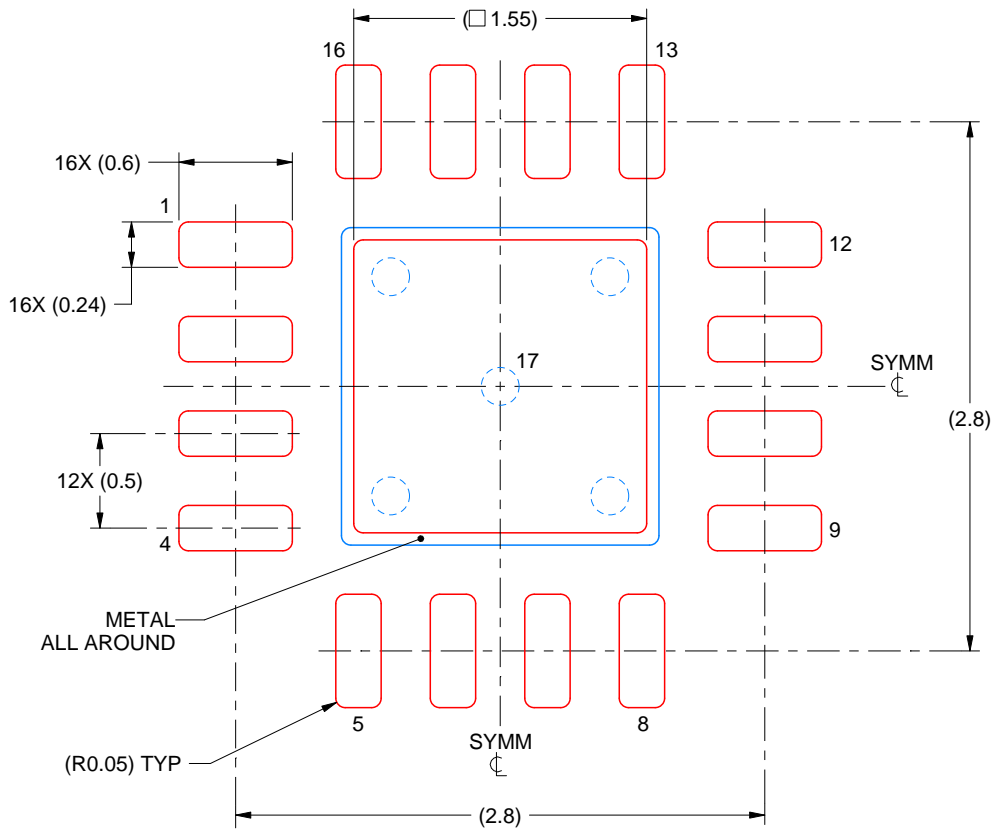


# EXAMPLE STENCIL DESIGN

RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:  
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:25X

4222419/D 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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