TEXAS INSTRUMENTS
BQ29209-Q1
JAJSGH8D – JUNE 2015 – REVISED SEPTEMBER 2020

BQ29209-Q1 2 直列セル・リチウムイオン・バッテリ用電圧保護 IC、自動セル平衡化機能付き

1 特長

- 2 直列セルの 2 次保護
- 外部イネーブル制御でセルの不均衡を自動修正
  - イネーブル ±30mV、ディセーブル 0mV のスレッショルド (標準値)
- 外付けコンデンサで遅延タイマを制御
- 外付け抵抗でセルのバランス電流を制御
- 低消費電力:I_{CC} < 3µA (標準値、V_{CELL}(ALL) < $V_{PROTECT}$)
- 最大 15mA の電流を制御する内部セル平衡化
- 外部セル平衡化モードをサポート
- 高精度の過電圧保護:
  - T_A = 0℃～60℃で ±25mV
- 固定の過電圧保護スレッショルド:
  4.30V
- 小型の 8L DRB パッケージ
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- AEC Q100 グレード 2 で車載用認定済み

2 アプリケーション

- リチウムイオン・バッテリ・パックの 2 次保護
  - 緊急通話 (eCall)
  - ノートブック PC
  - 電動工具
  - 携帯型機器および計測器
  - バッテリ・バックアップ・システム

3 概要

BQ29209-Q1 デバイスは、過電圧を精度よく検出する回路とセルの不均衡を自動修正する機能を備えた 2 直列セル・リチウムイオン・バッテリ・パック用 2 次過電圧保護 IC です。

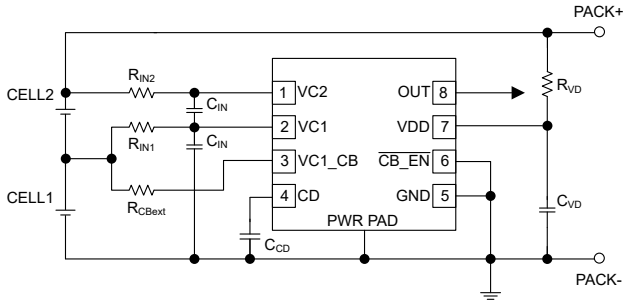
2 直列セルのバッテリ・パック内の各セルの電圧が、出荷時にプログラムされた内部基準電圧と比較されます。いずれかのセルが過電圧条件に達した場合、OUT ピンが LOW 状態から HIGH 状態に変化します。

BQ29209-Q1 は、電圧に基づいてセルの不均衡を自動的に修正できます。平衡化は、セルの電圧差が 30mV (公称値) 以上になると起動し、0mV (公称値) になると停止します。セルの平衡化は、$\overline{\text{CB\_EN}}$ ピンでイネーブル / ディセーブルできます。

製品情報

部品番号(1)	パッケージ	本体サイズ (公称)
BQ29209-Q1	VSON (8)	3.00mm × 3.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図

Table of Contents

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (December 2018) to Revision D (September 2020) — **Page**

- 機能安全対応の情報を追加 ... 1

Changes from Revision B (November 2018) to Revision C (December 2018) — **Page**

- Added a clarification regarding operation if GND is not connected first in sequence ... 8

Changes from Revision A (March 2016) to Revision B (November 2018) — **Page**

- *「概略回路図」の部品名を変更* ... 1
- Changed a component name in *Recommended Operating Conditions* ... 4
- Added the value of internal cell balancing switch resistances to *Electrical Characteristics* ... 4
- Changed resistor names ... 6
- Added 図 8-2 to clarify the cell balancing description; updated the equations ... 9
- Changed values and component names in 図 9-1 ... 12
- Changed component names and values used in the design example ... 12
- Changed external cell balancing figure, equations, and description ... 13

Changes from Revision * (June 2015) to Revision A (March 2016) — **Page**

- *「概略回路図」*の抵抗 R_{VD} の位置を変更、PACK+ と *PACK– を追加* ... 1
- Deleted the Lead Temperature (soldering) from the *セクション 7.1* table ... 3
- Changed resistor R_{VD} location in 図 9-1 ... 12
- Added title to 表 9-1 ... 12
- Changed resistor R_{VD} location, added PACK+ and PACK– in 図 9-3 ... 13

5 Device Options

T_A	PART NUMBER	OVP
–40°C to +105°C	BQ29209-Q1	4.3 V

6 Pin Configuration and Functions

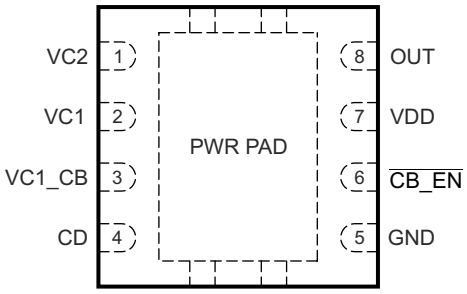


図 6-1. DRB Package 8-Pin VSON Top View

Pin Functions

PIN		DESCRIPTION
NAME	NO.	
$\overline{\text{CB\_EN}}$	6	Cell balance enable
CD	4	Connection to external capacitor for programmable delay time
GND	5	Ground pin
OUT	8	Output
Thermal Pad	PWR PAD	GND pin to be connected to the PWRPAD on the printed circuit board for proper operation
VC1	2	Sense voltage input for bottom cell
VC1_CB	3	Cell balance input for bottom cell
VC2	1	Sense voltage input for top cell
VDD	7	Power supply

7 Specifications

7.1 Absolute Maximum Ratings

Over-operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage range, V_{MAX}	VDD–GND	–0.3	16	V
Input voltage range, V_{IN}	VC2–GND, VC1–GND	–0.3	16	V
	VC2–VC1, CD–GND	–0.3	8	V
	$\overline{\text{CB\_EN}}$–GND	–0.3	16	V
Output voltage range, V_{OUT}	OUT–GND	–0.3	16	V
Continuous total power dissipation, P_{TOT}		See セクション 7.4.		
Storage temperature , T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1]		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins (VC2, CD, OUT, and GND)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, VDD		4		10	V
Input voltage range	VC2–VC1, VC1–GND	0		5	V
Delay time capacitance, $t_{d(CD)}$	C_{CD} (See 図 9-1.)		0.1		µF
Voltage monitor filter resistance	R_{IN} (See 図 9-1.)	100	1K		Ω
Voltage monitor filter capacitance	C_{IN} (See 図 9-1.)	0.01	0.1		µF
Supply voltage filter resistance	R_{VD} (See 図 9-1.)		100	1K	Ω
Supply voltage filter capacitance	C_{VD} (See 図 9-1.)		0.1		µF
Cell balance resistance	R_{CBext} (See 図 9-1 and *セクション 8.3.1*.)	100		4.7K	Ω
Operating ambient temperature range, T_A		–40		105	°C

7.4 Thermal Information

THERMAL METRIC[1]		BQ29209-Q1 DRB 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	50.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	25.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	18.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	5.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

Typical values stated where T_A = 25°C and VDD = 7.2 V. Minimum and maximum values stated where T_A = –40°C to 105°C and VDD = 4 V to 10 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{PROTECT}$	Overvoltage detection voltage			4.3		V
V_{HYS}	Overvoltage detection hysteresis		200	300	400	mV
V_{OA}	Overvoltage detection accuracy	T_A = 25°C	–10		10	mV
V_{OA_DRIFT}	Overvoltage threshold temperature drift	T_A = 0°C to 60°C	–0.4		0.4	mV°/C
		T_A = –40°C to 110°C	–0.6		0.6	

Typical values stated where T_A = 25°C and VDD = 7.2 V. Minimum and maximum values stated where T_A = –40°C to 105°C and VDD = 4 V to 10 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
X_{DELAY}	Overvoltage delay time scale factor	T_A = 0°C to 60°C Note: Does not include external capacitor variation.	6	9	12	s/µF
		T_A = –40°C to 110°C Note: Does not include external capacitor variation.	5.5	9	13.5	
X_{DELAY_CTM} (1)	Overvoltage delay time scale factor in Customer Test Mode			0.08		s/µF
$I_{CD(CHG)}$	Overvoltage detection charging current			150		nA
$I_{CD(DSG)}$	Overvoltage detection discharging current			60		µA
V_{CD}	Overvoltage detection external capacitor comparator threshold			1.2		V
I_{CC}	Supply current	(VC2–VC1) = (VC1–GND) = 3.5 V (See 図 8-5.)		3	6	µA
V_{OUT}	OUT pin drive voltage	(VC2–VC1) or (VC1–GND) > $V_{PROTECT}$, VDD = 10 V, I_{OH} = 0	6	8.25	9.5	V
		(VC2–VC1) or (VC1–GND) = $V_{PROTECT}$, VDD = $V_{PROTECT}$, I_{OH} = –100 µA, T_A = 0°C to 60°C	1.75	2.5		V
		(VC2–VC1) and (VC1–GND) < $V_{PROTECT}$, I_{OL} = 100 µA, T_A = 25°C			200	mV
		(VC2–VC1) and (VC1–GND) < $V_{PROTECT}$, I_{OL} = 0 µA, T_A = 25°C		0	10	mV
		VC2 = VC1 = VDD = 4 V, I_{OL} = 100 µA			200	mV
I_{OH}	High-level output current	OUT = 1.75 V, (VC2–VC1) or (VC1–GND) = $V_{PROTECT}$, VDD = $V_{PROTECT}$ to 10 V, T_A = 0°C to 60°C	–100			µA
I_{OL}	Low-level output current	OUT = 0.05 V, (VC2–VC1) or (VC1–GND) < $V_{PROTECT}$, VDD = $V_{PROTECT}$ to 10 V, T_A = 0°C to 60°C	30		85	µA
I_{OH_ZV}	High-level short-circuit output current	OUT = 0 V, (VC2–VC1) = (VC1–GND) = $V_{PROTECT}$ VDD = 4 to 10 V			–8	mA
I_{IN}	Input current at VCx pins	Measured at VC1, (VC2–VC1) = (VC1–GND) = 3.5 V, T_A = 0°C to 60°C (See 図 8-5.)	–0.2		0.2	µA
		Measured at VC2, (VC2–VC1) = (VC1–GND) = 3.5 V, T_A = 0°C to 60°C (See 図 8-5.)			2.5	µA
$V_{MM\_DET\_ON}$	Cell mismatch detection threshold for turning ON	(VC2–VC1) versus (VC1–GND) and vice-versa when cell balancing is enabled. VC2 = VDD = 7.6 V	17	30	45	mV
$V_{MM\_DET\_OFF}$	Cell mismatch detection threshold for turning OFF	Delta between (VC2–VC1) and (VC1–GND) when cell balancing is disabled. VC2 = VDD = 7.6 V	–9	0	9	mV
$V_{CB\_EN\_ON}$	Cell balance enable ON threshold	Active LOW pin at $\overline{CB\_EN}$			1	V
$V_{CB\_EN\_OFF}$	Cell balance enable OFF threshold	Active HIGH at $\overline{CB\_EN}$	2.2			V
I_{CB_EN}	Cell balance enable ON input current	$\overline{CB\_EN}$ = GND (See 図 8-6.)			0.2	µA
R_{CB1int}	Internal cell balance switch resistance	$\overline{CB\_EN}$ = GND		300		Ω
R_{CB2int}	Internal cell balance switch resistance	$\overline{CB\_EN}$ = GND		235		Ω

(1) Specified by design. Not 100% tested in production.

7.6 Recommended Cell Balancing Configurations

Typical values stated where T_A = 25°C and (VC2–VC1), (VC1–GND) = 3.8 V. Minimum and maximum values stated where T_A = –40°C to 105°C, VDD = 4 V to 10 V, and (VC2–VC1), (VC1–GND) = 3 V to 4.2 V. All values assume recommended supply voltage filter resistance R_{VD} of 100 Ω and 5% accurate or better cell balance resistor R_{CBext}.

			MIN	NOM	MAX	UNIT
I_{CB}	Cell balance input current	R_{CBext} = 4700 Ω	0.5	0.75	1	mA
		R_{CBext} = 2200 Ω	1	1.5	2	
		R_{CBext} = 910 Ω	2	3	4	
		R_{CBext} = 560 Ω	3	4.5	6	
		R_{CBext} = 360 Ω	3.5	6	8.5	
		R_{CBext} = 240 Ω	4	7.5	11	
		R_{CBext} = 120 Ω	5	10	15	

7.7 Typical Characteristics

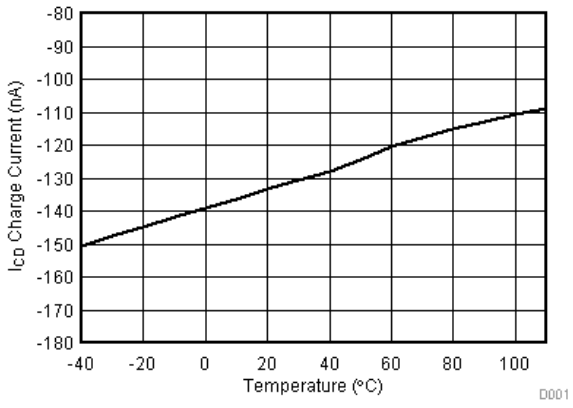


図 7-1. I_{CD} Charge Current

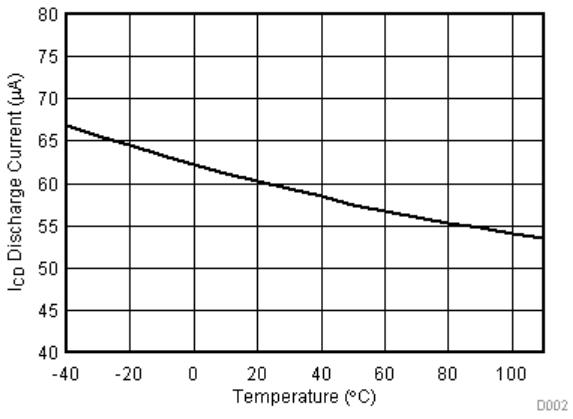


図 7-2. I_{CD} Discharge Current

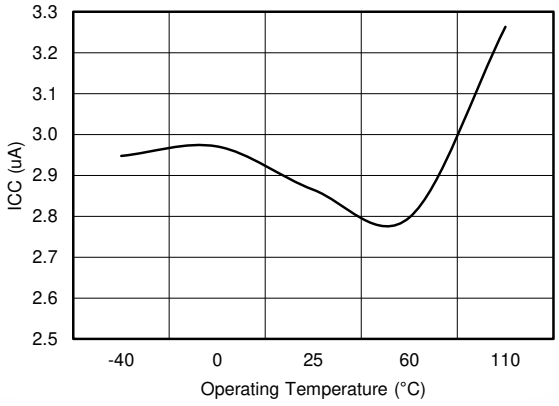


図 7-3. Average ICC During Normal Operation Across Operational Temperature

8 Detailed Description

8.1 Overview

The BQ29209-Q1 provides overvoltage protection and cell balancing for 2-series cell lithium-ion battery packs.

8.1.1 Voltage Protection

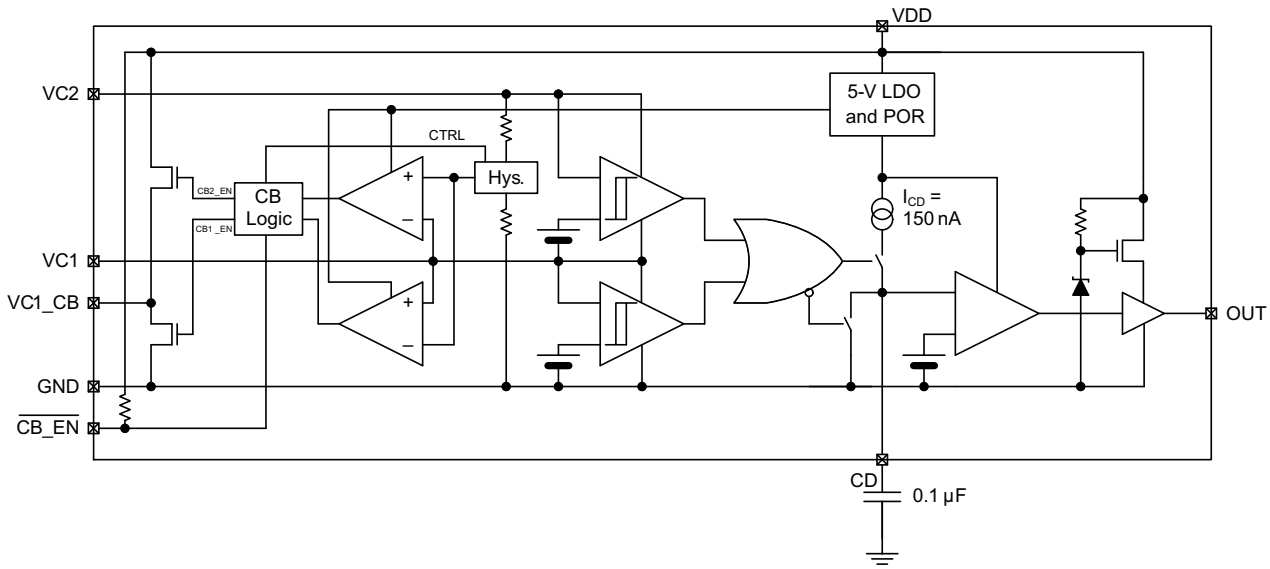
Each cell voltage is continuously compared to a factory configured internal reference threshold. If either cell reaches an overvoltage condition, the BQ29209-Q1 device starts a timer that provides a delay proportional to the capacitance on the CD pin. Upon expiration of the internal timer, the OUT pin changes from a low to high state.

8.1.2 Cell Balancing

If enabled, the BQ29209-Q1 performs automatic cell-balance correction where the two cells are automatically corrected for voltage imbalance by loading the cell with the higher voltage with a small balancing current. When the cells are measured to be equal within nominally 0 mV, the load current is removed. It will be re-applied if the imbalance exceeds nominally 30 mV. The cell mismatch correction circuitry is enabled by pulling the $\overline{\text{CB\_EN}}$ pin low, and disabled when $\overline{\text{CB\_EN}}$ is pulled to greater than 2.2 V, for example, VDD.

If the internal cell balancing current of up to 15 mA is insufficient, the BQ29209-Q1 may be configured via external circuitry to support much higher external cell balancing current.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Protection (OUT) Timing

Sizing the external capacitor is based on the desired delay time as follows:

$$C_{CD} = \frac{t_d}{X_{DELAY}}$$

Where t_d is the desired delay time and X_{DELAY} is the overvoltage delay time scale factor, expressed in seconds per microfarad. X_{DELAY} is nominally 9 s/µF. For example, if a nominal delay of 3 seconds is desired, use a C_{CD} capacitor that is 3 s / 9 s/µF = 0.33 µF.

The delay time is calculated as follows:

$$t_d = C_{CD} \times X_{DELAY}$$

If the cell overvoltage condition is removed before the external capacitor reaches the reference voltage, the internal current source is disabled and an internal discharge block is employed to discharge the external capacitor down to 0 V. In this instance, the OUT pin remains in a low state.

8.3.2 Cell Voltage > $V_{PROTECT}$

When one or both of the cell voltages rises above $V_{PROTECT}$, the internal comparator is tripped, and the delay begins to count to t_d. If the input remains above $V_{PROTECT}$ for the duration of t_d, the BQ29209-Q1 output changes from a low to a high state, by means of an internal pull-up network, to a regulated voltage of no more than 9.5 V when I_{OH} = 0 mA.

The external delay capacitor should charge up to no more than the internal LDO voltage (approximately 5 V typically), and will fully discharge in approximately under 100 ms when the overvoltage condition is removed.

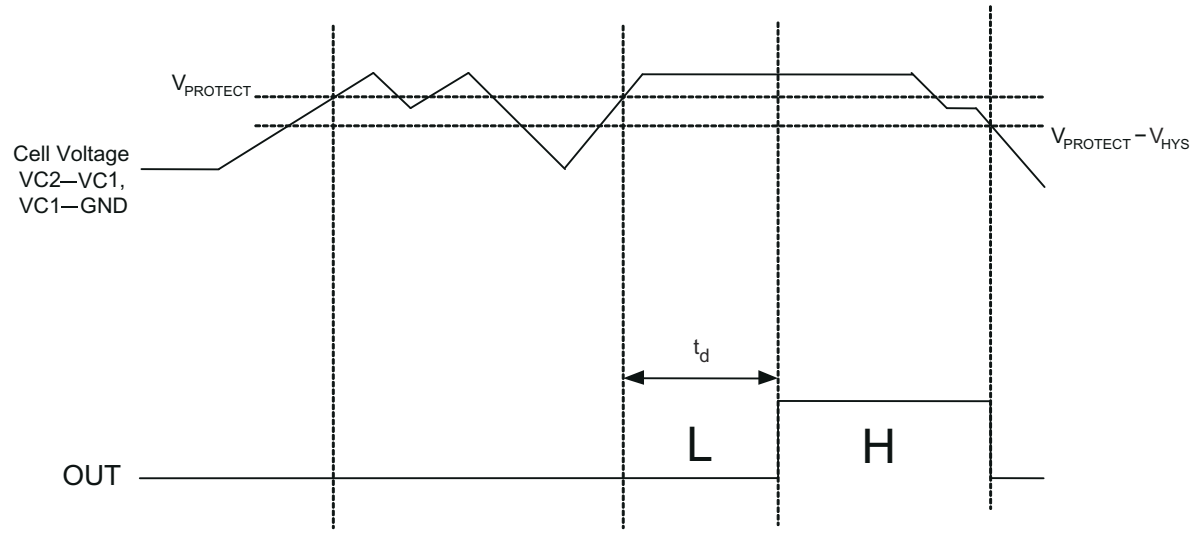


図 8-1. Timing for Overvoltage Sensing

8.3.3 Cell Connection Sequence

Note

Before connecting the cells, populate the overvoltage delay timing capacitor, C_{CD}.

The recommended cell connection sequence begins from the bottom of the stack, as follows:

1. GND
2. VC1
3. VC2

While not advised, connecting the cells in a sequence other than that described above does not result in errant activity on the OUT pin. For example:

1. GND
2. VC2 or VC1
3. Remaining VCx pin

Note

Using any cell connection sequence that does not connect GND first may result in increased leakage current drawn by the VDD pin.

8.3.4 Cell Balance Enable Control

To avoid prematurely discharging the cells, it is recommended to turn off (pull high) the active-low Cell Balance Enable Control pin at lower state-of-charge (SOC) levels.

8.3.5 Cell Balance Configuration

The following cell balancing details relate to 図 8-2.

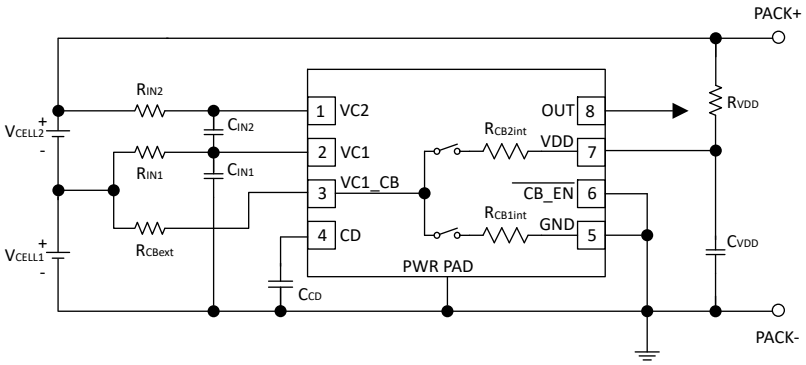


図 8-2. Simplified Schematic for Cell Balancing Description

The cell balancing current may be calculated as follows:

For Cell 1 balancing current, I_{CB1}:

$$I_{CB1} = \frac{V_{CELL1}}{R_{CBext} + R_{CB1int}} \quad (1)$$

For Cell 2 balancing current, I_{CB2}:

$$I_{CB2} = \frac{V_{CELL2}}{R_{CBext} + R_{CB2int} + R_{VDD}} \quad (2)$$

Where:

R_{CBext} = resistor connected between the top of Cell 1 and the VC1_CB pin

R_{IN1} = resistor connected between the top of Cell 1 and the VC1 pin

R_{IN2} = resistor connected between the top of Cell 2 and the VC2 pin

R_{VDD} = resistor connected between the top of Cell 2 and the VDD pin

8.3.6 Cell Imbalance Auto-Detection (Via Cell Voltage)

The $V_{MM\_DET\_ON}$ and $V_{MM\_DET\_OFF}$ specifications are calibrated where VDD = VC2 = 7.6 V and VC1 = 3.8 V. The recommended range of cell balancing is VC2 and VDD between 6.0 V and 8.4 V, and VC1 between 3 V and 4.2 V. Below VDD = 6 V, it is recommended to pull $\overline{CB\_EN}$ high to disable the cell balancing function.

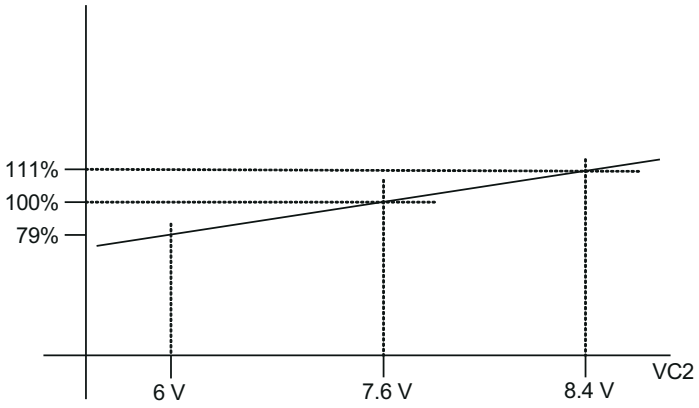


図 8-3. $V_{MM\_DET\_ON}$ and $V_{MM\_DET\_OFF}$ Threshold

8.3.7 Customer Test Mode

Customer Test Mode (CTM) helps to greatly reduce the overvoltage detection delay time and enable quicker customer production testing. This mode is intended for quick-pass board-level verification tests, and, as such, individual cell overvoltage levels may deviate slightly from the specifications ($V_{PROTECT}$, V_{OA}). If accurate overvoltage thresholds are to be tested, use the standard delay settings that are intended for normal use.

To enter CTM, VDD should be set to approximately 9.5 V higher than VC2. When CTM is entered, the device switches from the normal overvoltage delay time scale factor, X_{DELAY}, to a significantly reduced factor of approximately 0.08, thereby reducing the delay time during an overvoltage condition.

CAUTION

Avoid exceeding any Absolute Maximum Voltages on any pins when placing the part into CTM. Also, avoid exceeding absolute maximum voltages for the individual cell voltages (VC1–GND) and (VC2–VC1). Stressing the pins beyond the rated limits may cause permanent damage to the device.

To exit CTM, power off the device and then power it back on.

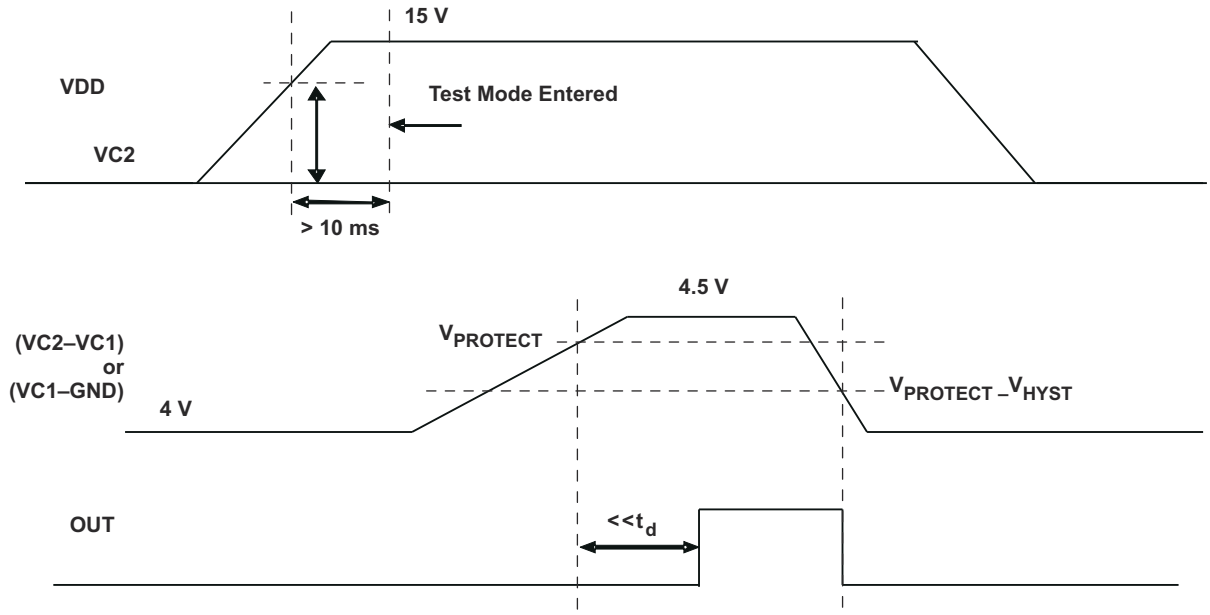


図 8-4. Voltage Test Limits

8.3.8 Test Conditions

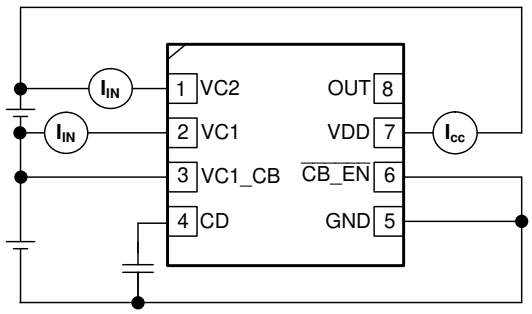


図 8-5. I_{CC}, I_{IN} Measurement

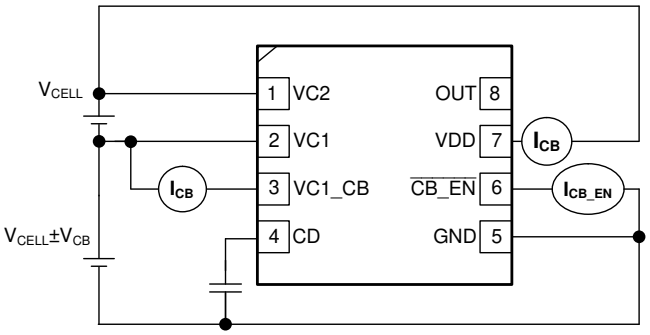


図 8-6. I_{CB} Measurement

8.4 Device Functional Modes

This device monitors the voltage of the cells connected to the VCx pins and depending on these voltages and the overall battery voltage at VDD the device enters different operating modes.

8.4.1 NORMAL Mode

The device is operating in NORMAL mode when the cell voltage range is between the over-charge detection threshold ($V_{PROTECT}$) and the minimum supply voltage.

If this condition is satisfied, the device turns OFF the OUT pin.

8.4.2 PROTECTION Mode

The device is operating in PROTECTION mode when the cell over voltage protection feature has been triggered. See *セクション 8.3.2* for more details on this feature.

If this condition is satisfied, the device turns ON the OUT pin.

9 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The BQ29209-Q1 is designed to be used in 2-series Li-Ion battery packs and with the option to include voltage-based cell balancing. The number of parallel cells or the overall capacity of the battery only affects the cell balancing circuit due to the level of potential imbalance that needs to be corrected.

9.2 Typical Applications

9.2.1 Battery Connection

図 9-1 shows the configuration for the 2-series cell battery connection with cell balancing enabled.

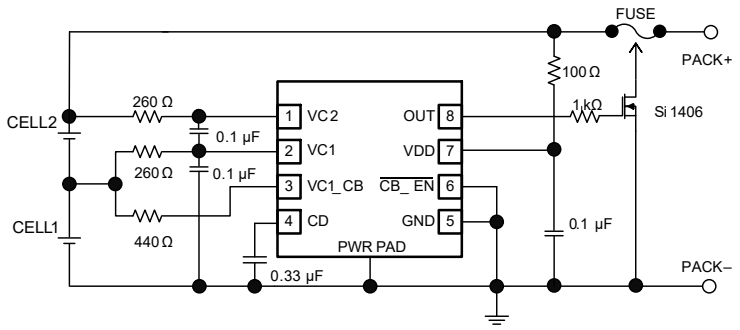


図 9-1. 2-Series Cell Configuration

9.2.1.1 Design Requirements

For this design example, use the parameters listed in 表 9-1.

表 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE at T_A = 25°C
Input voltage range	4 V to 10 V
Overvoltage Protection (OVT)	4.3 V
Overvoltage detection delay time	3 s
Overvoltage detection delay timer capacitor	0.33 µF
Cell Balancing Enabled	Yes
Cell Balancing Current, I_{CB1} and I_{CB2}	5 mA (targeted at a nominal cell voltage of 3.8 V)
Cell Balancing Resistors, R_{CBext}, R_{IN1}, R_{IN2} and R_{VD}	R_{CBext} = 440 Ω, R_{IN1} = 260 Ω, R_{IN2} = 260 Ω, R_{VD} = 100 Ω

9.2.1.2 Detailed Design Procedure

The BQ29209-Q1 has limited features but there are some key calculations to be made when selecting external component values.

- Calculate the required C_{CD} capacitor value for the voltage protection delay time. Care should be taken to evaluate the tolerances of the capacitor and the BQ29209-Q1 to ensure system specifications are met.
- Calculate the cell balancing resistor values to provide a suitable level of balancing current that will, at a minimum, counter act an increase in imbalance during normal operation of the battery. Care should be taken to ensure any connectivity resistance is also considered as this will also reduce the balancing current level.

9.2.1.3 Application Curve

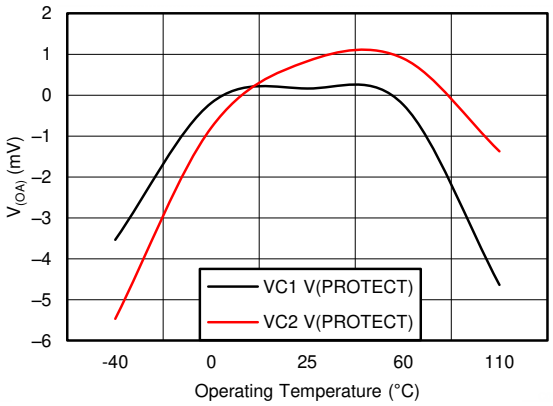


図 9-2. Average $V_{PROTECT}$ Accuracy (V_{OA}) Across Operation Temperature

9.3 System Example

9.3.1 External Cell Balancing

Higher cell balancing currents can be supported by means of a simple external network, as shown in 図 9-3.

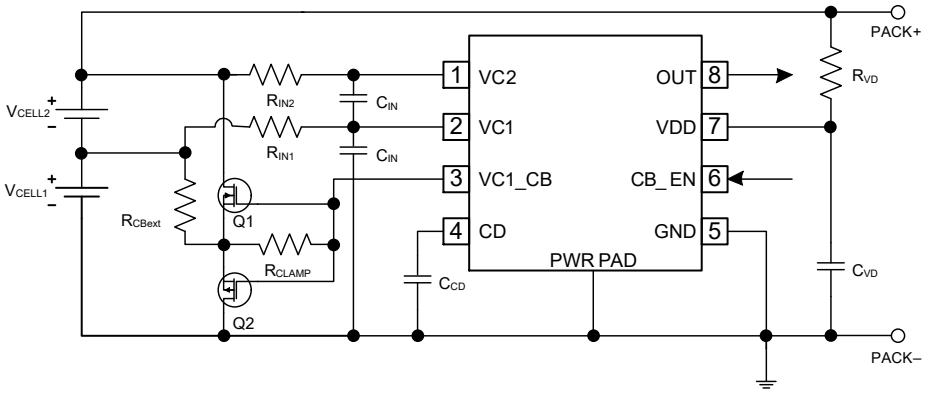


図 9-3. External Cell Balancing Configuration

The VC1_CB pin is tri-stated when cell balancing is disabled, is driven low by the internal logic to enable balancing on CELL1, and is driven high by the internal logic to enable balancing on CELL2. R_{CLAMP} ensures that both Q1 and Q2 remain off when balancing is disabled, and should be sized above 2 kΩ to prevent excessive internal device current when the balancing network is activated. If R_{CLAMP} is too small, then the gate-source voltage required to enable the external FETs cannot be achieved. R_{CBext} determines the value of the balancing current, and is dependent on the voltage of the balanced cell and the specific Q1 and Q2 transistors used in the design (due to the transistors operating in saturation mode during balancing). The balancing currents (assuming the current through R_{CLAMP} is not significant) are given as follows:

$$I_{CB1} = \frac{(V_{CELL1} - V_{SG\_Q2})}{R_{CBext}} \quad (3)$$

$$I_{CB2} = \frac{(V_{CELL2} - V_{GS\_Q1})}{R_{CBext}} \quad (4)$$

10 Power Supply Recommendations

The recommended power supply for this device is a maximum 10-V operation on the VDD input pin.

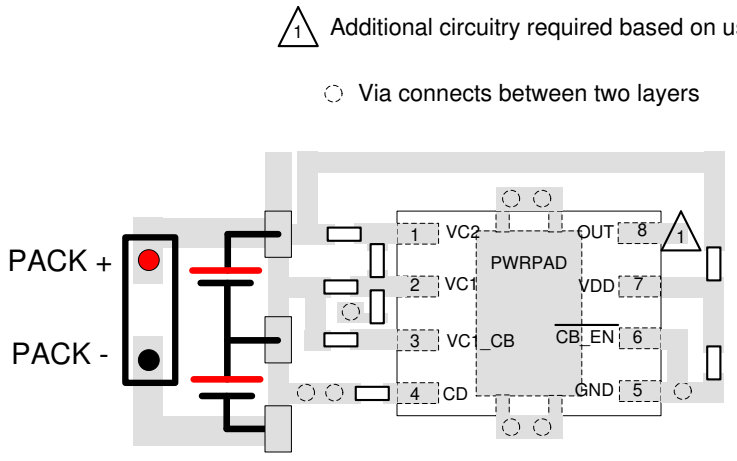
11 Layout

11.1 Layout Guidelines

The following are the recommended layout guidelines:

1. Ensure the input filters to the VC1 and VC2 pins are as close to the IC as possible to improve noise immunity.
2. If the OUT pin is used to control a high current path, for example: to blow a chemical fuse, then care should be taken to ensure the high current path creates minimal interference of the BQ29209-Q1 voltage sense inputs.
3. The input RC filter on the VDD pin should be close to the terminal of the IC.

11.2 Layout Example



12 Device and Documentation Support

12.1 Documentation Support

For additional information, see the following related document:

- *BQ29209-Q1 Functional Safety FIT Rate, FMD, and Pin FMA Application Report*

12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。*「更新の通知を受け取る」をクリック*して登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

12.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい ESD 対策をとらないと、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

12.6 用語集

TI 用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ29209TDRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	209Q1	Samples
BQ29209TDRBTQ1	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	209Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

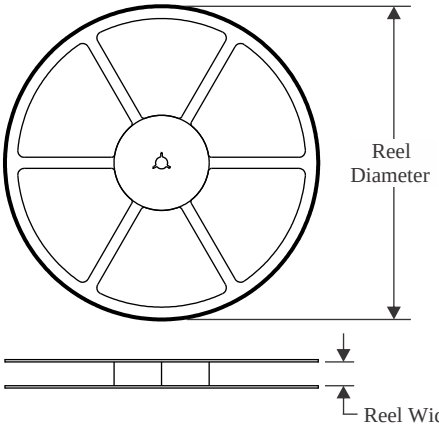
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

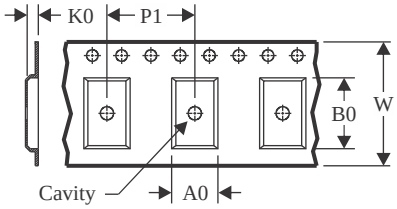
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

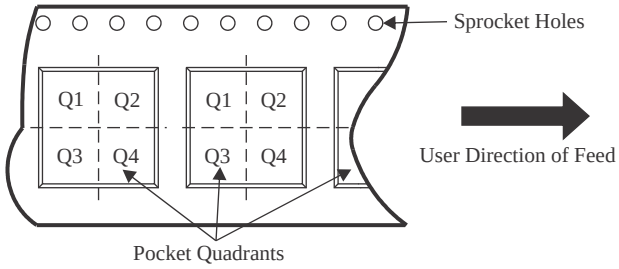


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

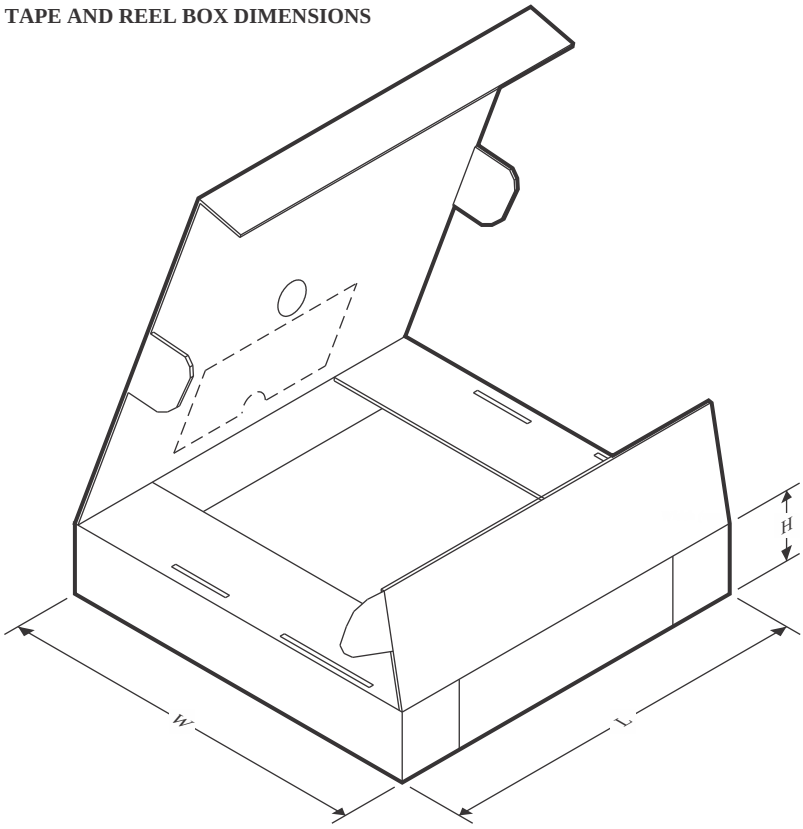
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ29209TDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ29209TDRBTQ1	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ29209TDRBRQ1	SON	DRB	8	3000	346.0	346.0	33.0
BQ29209TDRBTQ1	SON	DRB	8	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

DRB 8

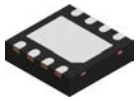
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203482/L

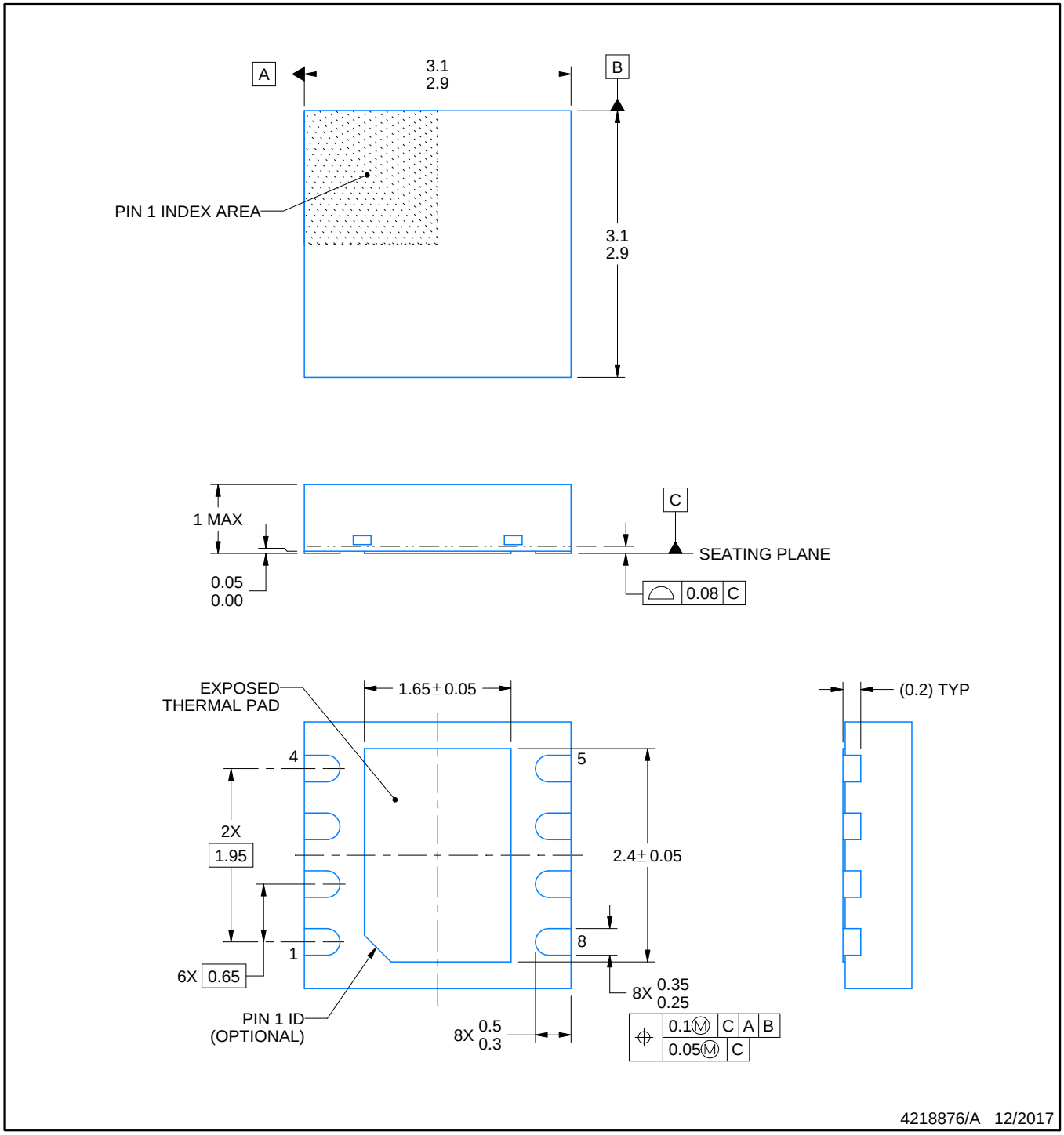
DRB0008B



PACKAGE OUTLINE

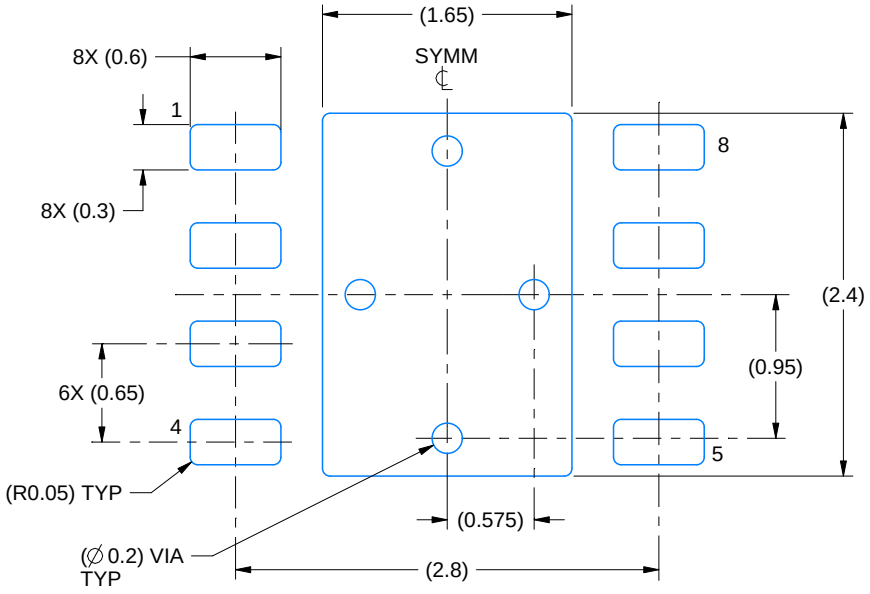
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

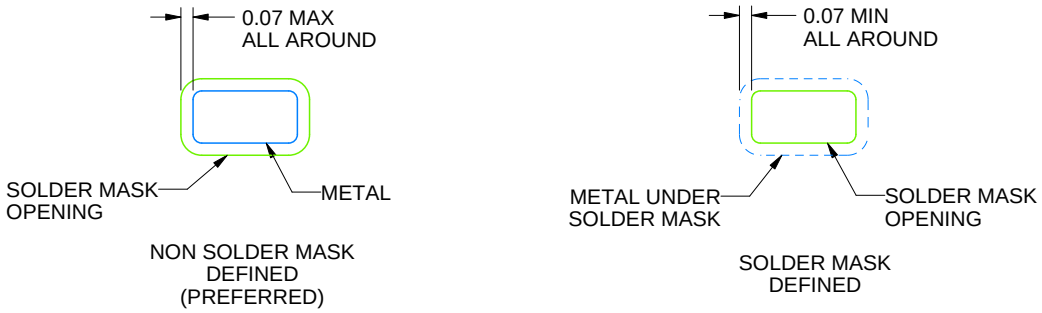


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

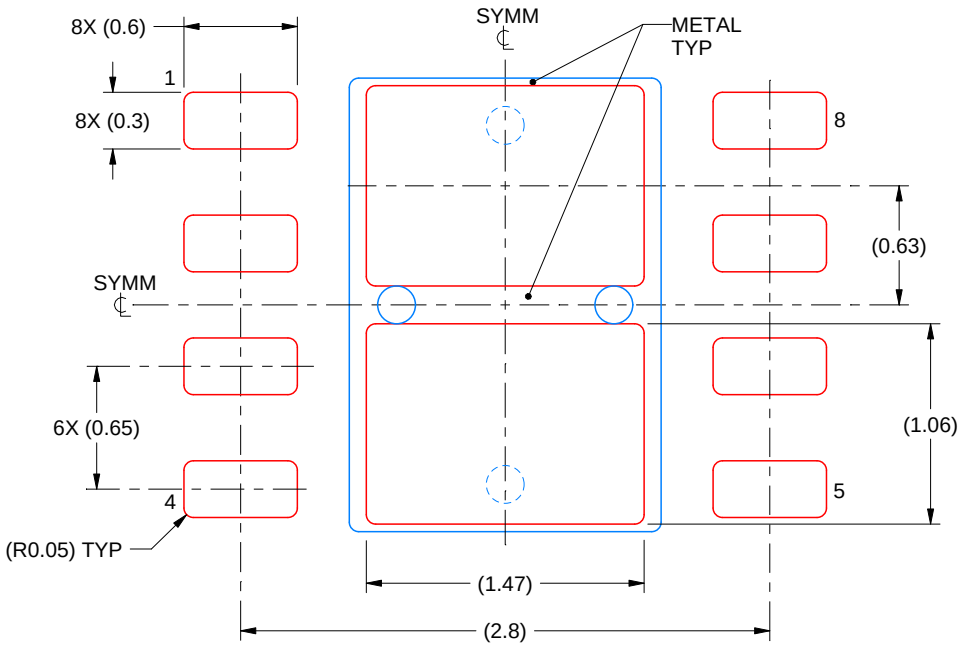


SOLDER MASK DETAILS

4218876/A 12/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218876/A 12/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス· デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265