

BQ34Z100-R2 ワイド・レンジ・バッテリー残量計、Impedance Track™ テクノロジー採用

1 特長

- リチウムイオン、LiFePO₄、PbA、NiMH、NiCd ケミストリをサポート
- 特許取得済みの Impedance Track™ テクノロジーを使った容量推定 (3V～16.7KV のバッテリーに対応)
 - 経時変化補償
 - 自己放電補償
- 標準構成で、最大 7000Ah のバッテリー容量をサポート
- 標準構成で、最大 8160A の充放電電流をサポート
- 外部 NTC サーミスタをサポート
- ホスト・システムとの 2 線式 I²C および HDQ 1 線式通信インターフェイスをサポート
- SHA-1/HMAC 認証機能
- 1 または 4 LED 直接表示制御
- ポート・エクスパンダによる 5 LED 以上の表示
- 低消費電力モード (一般的なバッテリー・パックの動作範囲の条件)
 - 通常動作: < 145μA (平均値)
 - スリープ: < 84μA (平均値)
 - フル・スリープ: < 30μA (平均値)
- パッケージ: 14 ピン TSSOP

2 アプリケーション

- 軽量の電気自動車
- 医療用計測機器
- 移動無線
- 電動工具
- 無停電電源 (UPS)

3 概要

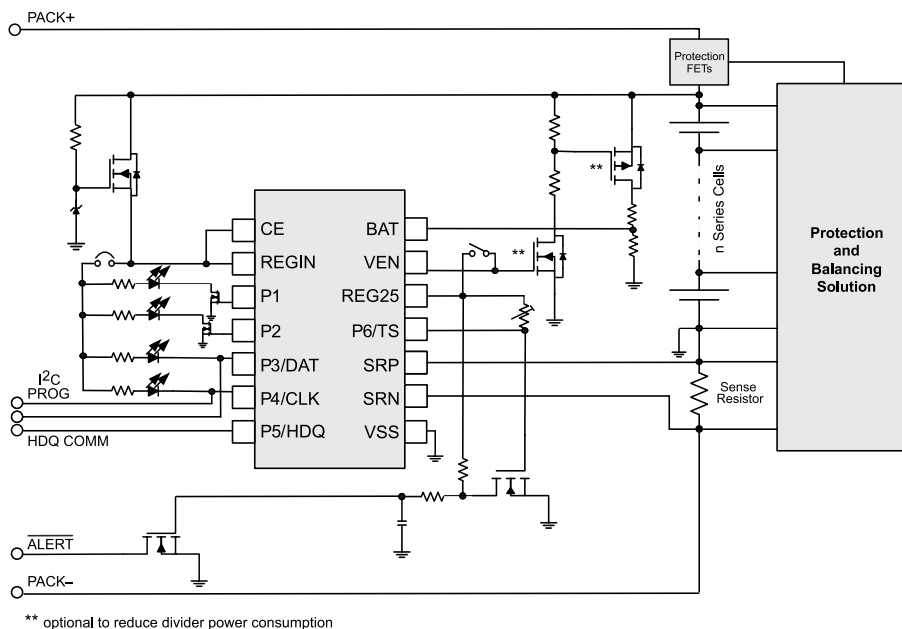
BQ34Z100-R2 デバイスは、リチウムイオン、PbA、NiMH、NiCd バッテリー向けの Impedance Track™ 残量計であり、バッテリーの直列セル構成と無関係に動作します。システムの消費電力を低減するように自動的に制御される外部電圧変換回路を使って、3V～16.7KV のバッテリーを簡単にサポートできます。

BQ34Z100-R2 デバイスは、I²C ペリフェラル、HDQ ペリフェラル、1 つまたは 4 つの直接 LED、ALERT 出力ピンを含む複数のインターフェイスの選択肢を備えています。また、BQ34Z100-R2 は、5 つ以上の LED のための外部ポート・エクスパンダもサポートしています。

製品情報

部品番号 ⁽¹⁾	パッケージ	本体サイズ (公称)
BQ34Z100-R2	TSSOP (14)	5.00mm × 4.40mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



簡略回路図



Table of Contents

1 特長	1	6.12 Electrical Characteristics: Data Flash Memory Characteristics.....	7
2 アプリケーション	1	6.13 Timing Requirements: HDQ Communication.....	7
3 概要	1	6.14 Timing Requirements: I ² C-Compatible Interface.....	8
4 Revision History	2	6.15 Typical Characteristics.....	9
5 Pin Configuration and Functions	3	7 Functional Block Diagram	10
6 Specifications	4	8 Application and Implementation	11
6.1 Absolute Maximum Ratings.....	4	8.1 Application Information.....	11
6.2 ESD Ratings.....	4	8.2 Typical Applications.....	11
6.3 Recommended Operating Conditions.....	4	9 Power Supply Recommendations	17
6.4 Thermal Information.....	5	10 Layout	18
6.5 Electrical Characteristics: Power-On Reset.....	5	10.1 Layout Guidelines.....	18
6.6 Electrical Characteristics: LDO Regulator.....	5	10.2 Layout Example.....	18
6.7 Electrical Characteristics: Internal Temperature Sensor Characteristics.....	5	11 Device and Documentation Support	21
6.8 Electrical Characteristics: Low-Frequency Oscillator.....	6	11.1 Documentation Support.....	21
6.9 Electrical Characteristics: High-Frequency Oscillator.....	6	11.2 ドキュメントの更新通知を受け取る方法.....	21
6.10 Electrical Characteristics: Integrating ADC (Coulomb Counter) Characteristics.....	6	11.3 サポート・リソース.....	21
6.11 Electrical Characteristics: ADC (Temperature and Cell Measurement) Characteristics.....	6	11.4 Trademarks.....	21
		11.5 静電気放電に関する注意事項.....	21
		11.6 用語集.....	21
		12 Mechanical, Packaging, and Orderable Information	21

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
December 2022	*	Initial Release

5 Pin Configuration and Functions

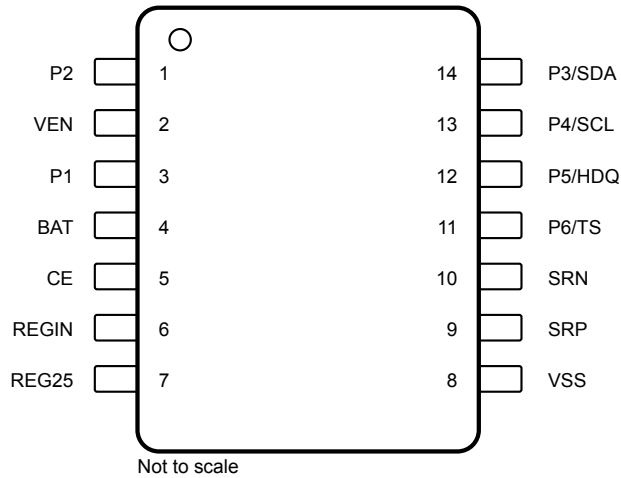


表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
P2	1	O	LED 2 or Not Used (connect to VSS)
VEN	2	O	Active High Voltage Translation Enable. This signal is optionally used to switch the input voltage divider on/off to reduce the power consumption (typ 45 μ A) of the divider network. If not used, then this pin can be left floating or tied to VSS.
P1	3	O	LED 1 or Not Used (connect to VSS). This pin is also used to drive an LED for single-LED mode. Use a small signal N-FET (Q1) in series with the LED as shown on 8-4 .
BAT	4	I	Translated Battery Voltage Input
CE	5	I	Chip Enable. Internal LDO is disconnected from REGIN when driven low.
REGIN	6	P	Internal integrated LDO input. Decouple with a 0.1- μ F ceramic capacitor to VSS.
REG25	7	P	2.5-V output voltage of the internal integrated LDO. Decouple with 1- μ F ceramic capacitor to VSS.
VSS	8	P	Device ground
SRP	9	I	Analog input pin connected to the internal coulomb-counter peripheral for integrating a small voltage between SRP and SRN where SRP is nearest the BAT– connection.
SRN	10	I	Analog input pin connected to the internal coulomb-counter peripheral for integrating a small voltage between SRP and SRN where SRN is nearest the PACK– connection.
P6/TS	11	I	Pack thermistor voltage sense (use a 103AT-type thermistor)
P5/HDQ	12	I/O	Open-drain HDQ Serial communication line (target). If not used, then this pin can be left floating or tied to VSS.
P4/SCL	13	I	Target I ² C serial communication clock input. Use with a 10-k Ω pullup resistor (typical). This pin is also used for LED 4 in the four-LED mode. If not used, then this pin can be left floating or tied to VSS.
P3/SDA	14	I/O	Open-drain target I ² C serial communication data line. Use with a 10-k Ω pullup resistor (typical). This pin is also used for LED 3 in the four-LED mode. If not used, then this pin can be left floating or tied to VSS.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{REGIN}	Regulator Input Range	-0.3	5.5	V
V _{CC}	Supply Voltage Range	-0.3	2.75	V
V _{IOD}	Open-drain I/O pins (SDA, SCL, HDQ, VEN)	-0.3	5.5	V
V _{BAT}	Bat Input pin	-0.3	5.5	V
V _I	Input Voltage range to all other pins (P1, P2, SRP, SRN)	-0.3	V _{CC} + 0.3	V
ESD	Human-body model (HBM), BAT pin		1.5	kV
	Human-body model (HBM), all other pins		2	kV
T _A	Operating free-air temperature range	-40	85	°C
T _F	Functional temperature range	-40	100	°C
T _{STG}	Storage temperature range	-65	150	°C
	Lead temperature (soldering, 10 s)	-40	100	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

T_A = -40°C to 85°C; Typical Values at T_A = 25°C C_{LDO25} = 1.0 µF, and V_{REGIN} = 3.6 V (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V _{REGIN}	Supply Voltage	No operating restrictions	2.7		4.5	V
		No FLASH writes	2.45		2.7	V
C _{REGIN}	External input capacitor for internal LDO between REGIN and VSS	Nominal capacitor values specified. Recommend a 10% ceramic X5R type capacitor located close to the device.		0.1		µF
C _{LDO25}	External output capacitor for internal LDO between VCC and VSS		0.47	1		µF
I _{CC}	NORMAL operating-mode current	Gas Gauge in NORMAL mode, I _{LOAD} > Sleep Current		145		µA
I _{SLP}	SLEEP operating-mode current	Gas Gauge in SLEEP mode, I _{LOAD} < Sleep Current		84		µA
I _{SLP+}	FULLSLEEP operating-mode current	Gas Gauge in FULL SLEEP mode, I _{LOAD} < Sleep Current		30		µA
V _{OL}	Output voltage, low (SCL, SDA, HDQ, VEN)	I _{OL} = 3 mA			0.4	V
V _{OH(PP)}	Output voltage, high	I _{OH} = -1 mA	V _{CC} - 0.5			V
V _{OH(OD)}	Output voltage, high (SDA, SCL, HDQ, VEN)	External pull-up resistor connected to V _{CC}	V _{CC} - 0.5			V
V _{IL}	Input voltage, low		-0.3		0.6	V

6.3 Recommended Operating Conditions (continued)

$T_A = -40^\circ\text{C}$ to 85°C ; Typical Values at $T_A = 25^\circ\text{C}$ $C_{LDO25} = 1.0\ \mu\text{F}$, and $V_{\text{REGIN}} = 3.6\ \text{V}$ (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{\text{IH(OD)}}$	Input voltage, high (SDA, SCL, HDQ)	1.2		6	V
V_{A1}	Input voltage range (TS)	$V_{\text{SS}} - 0.05$		1	V
V_{A2}	Input voltage range (BAT)	$V_{\text{SS}} - 0.125$		5	V
V_{A3}	Input voltage range (SRP, SRN)	$V_{\text{SS}} - 0.125$		0.125	V
I_{LKG}	Input leakage current (I/O pins)			0.3	μA
t_{PUCD}	Power-up communication delay		250		ms

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		BQ34Z100-R2			UNIT
		TSSOP (PW)			
		14 PINS			
$R_{\theta\text{JA, High K}}$	Junction-to-ambient thermal resistance	103.8			°C/W
$R_{\theta\text{JC(top)}}$	Junction-to-case(top) thermal resistance	31.9			
$R_{\theta\text{JB}}$	Junction-to-board thermal resistance	46.6			
ψ_{JT}	Junction-to-top characterization parameter	2.0			
ψ_{JB}	Junction-to-board characterization parameter	45.9			
$R_{\theta\text{JC(bottom)}}$	Junction-to-case(bottom) thermal resistance	N/A			

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics Application Report*, [SPRA953](#).

6.5 Electrical Characteristics: Power-On Reset

$T_A = -40^\circ\text{C}$ to 85°C ; Typical Values at $T_A = 25^\circ\text{C}$ and $V_{\text{REGIN}} = 3.6\ \text{V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{\text{IT+}}$	Positive-going battery voltage input at REG25	2.05	2.20	2.31	V
V_{HYS}	Power-on reset hysteresis	45	115	185	mV

6.6 Electrical Characteristics: LDO Regulator

$T_A = 25^\circ\text{C}$, $C_{\text{LDO25}} = 1.0\ \mu\text{F}$, $V_{\text{REGIN}} = 3.6\ \text{V}$ (unless otherwise noted)⁽¹⁾

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT	
V_{REG25}	Regulator output voltage	$2.7\ \text{V} \leq V_{\text{REGIN}} \leq 4.5\ \text{V}$, $I_{\text{OUT}} \leq 16\ \text{mA}$	$T_A = -40^\circ\text{C}$ to 85°C	2.3	2.5	2.7	V
		$2.45\ \text{V} \leq V_{\text{REGIN}} < 2.7\ \text{V}$ (low battery), $I_{\text{OUT}} \leq 3\ \text{mA}$	$T_A = -40^\circ\text{C}$ to 85°C	2.3			
$I_{\text{SHORT}}^{(2)}$	Short Circuit Current Limit	$V_{\text{REG25}} = 0\ \text{V}$	$T_A = -40^\circ\text{C}$ to 85°C		250	mA	

(1) LDO output current, I_{OUT} , is the sum of internal and external load currents.

(2) Specified by design. Not production tested.

6.7 Electrical Characteristics: Internal Temperature Sensor Characteristics

$T_A = -40^\circ\text{C}$ to 85°C , $2.4\ \text{V} < \text{REG25} < 2.6\ \text{V}$; Typical Values at $T_A = 25^\circ\text{C}$ and $\text{REG25} = 2.5\ \text{V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
G_{TEMP}	Temperature sensor voltage gain		-2		mV/°C

6.8 Electrical Characteristics: Low-Frequency Oscillator

$T_A = -40^\circ\text{C}$ to 85°C , $2.4\text{ V} < \text{REG25} < 2.6\text{ V}$; Typical Values at $T_A = 25^\circ\text{C}$ and $\text{REG25} = 2.5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(\text{LOSC})}$	Operating frequency		32.768		kHz
$f_{(\text{LEIO})}$	Frequency error ^{(1) (2)}	$T_A = 0^\circ\text{C}$ to 60°C	-1.5%	0.25%	1.5%
		$T_A = -20^\circ\text{C}$ to 70°C	-2.5%	0.25%	2.5%
		$T_A = -40^\circ\text{C}$ to 85°C	-4%	0.25%	4%
$t_{(\text{LSXO})}$	Start-up time ⁽³⁾		500		μs

(1) The frequency drift is included and measured from the trimmed frequency at $V_{\text{CC}} = 2.5\text{ V}$, $T_A = 25^\circ\text{C}$.

(2) The frequency error is measured from 32.768 kHz.

(3) The startup time is defined as the time it takes for the oscillator output frequency to be $\pm 3\%$.

6.9 Electrical Characteristics: High-Frequency Oscillator

$T_A = -40^\circ\text{C}$ to 85°C , $2.4\text{ V} < \text{REG25} < 2.6\text{ V}$; Typical Values at $T_A = 25^\circ\text{C}$ and $\text{REG25} = 2.5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(\text{OSC})}$	Operating frequency		8.389		MHz
$f_{(\text{EIO})}$	Frequency error ^{(1) (2)}	$T_A = 0^\circ\text{C}$ to 60°C	-2%	0.38%	2%
		$T_A = -20^\circ\text{C}$ to 70°C	-3%	0.38%	3%
		$T_A = -40^\circ\text{C}$ to 85°C	-4.5%	0.38%	4.5%
$t_{(\text{SXO})}$	Start-up time ⁽²⁾		2.5	5	ms

(1) The frequency error is measured from 2.097 MHz.

(2) The startup time is defined as the time it takes for the oscillator output frequency to be $\pm 3\%$.

6.10 Electrical Characteristics: Integrating ADC (Coulomb Counter) Characteristics

$T_A = -40^\circ\text{C}$ to 85°C , $2.4\text{ V} < \text{REG25} < 2.6\text{ V}$; Typical Values at $T_A = 25^\circ\text{C}$ and $\text{REG25} = 2.5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$V_{(\text{SR})}$	Input voltage range, $V_{(\text{SRN})}$ and $V_{(\text{SRP})}$	$V_{(\text{SR})} = V_{(\text{SRN})} - V_{(\text{SRP})}$		-0.125	0.125	V
$t_{\text{SR_CONV}}$	Conversion time	Single conversion			1	s
	Resolution	14		15	bits	
$V_{\text{OS}(\text{SR})}$	Input offset		10		μV	
I_{NL}	Integral nonlinearity error		$\pm 0.007\%$	$\pm 0.034\%$	FSR ⁽²⁾	
$Z_{\text{IN}(\text{SR})}$	Effective input resistance ⁽¹⁾	2.5			M Ω	
$I_{\text{kg}(\text{SR})}$	Input leakage current ⁽¹⁾			0.3	μA	

(1) Specified by design. Not tested in production.

(2) Full-scale reference

6.11 Electrical Characteristics: ADC (Temperature and Cell Measurement) Characteristics

$T_A = -40^\circ\text{C}$ to 85°C , $2.4\text{ V} < \text{REG25} < 2.6\text{ V}$; Typical Values at $T_A = 25^\circ\text{C}$ and $\text{REG25} = 2.5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{\text{IN}(\text{ADC})}$	Input voltage range	0.05		1	V
$t_{\text{ADC_CONV}}$	Conversion time			125	ms
	Resolution	14		15	bits
$V_{\text{OS}(\text{ADC})}$	Input offset		1		mV
Z_{ADC1}	Effective input resistance (TS) ⁽¹⁾	8			M Ω
Z_{ADC2}	Effective input resistance (BAT) ⁽¹⁾	BQ34Z100-R2 not measuring cell voltage	8		M Ω
		BQ34Z100-R2 measuring cell voltage		100	K Ω

6.11 Electrical Characteristics: ADC (Temperature and Cell Measurement) Characteristics (continued)

$T_A = -40^{\circ}\text{C}$ to 85°C , $2.4\text{ V} < \text{REG25} < 2.6\text{ V}$; Typical Values at $T_A = 25^{\circ}\text{C}$ and $\text{REG25} = 2.5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{\text{kg(ADC)}}$	Input leakage current ⁽¹⁾			0.3	μA

(1) Specified by design. Not tested in production.

6.12 Electrical Characteristics: Data Flash Memory Characteristics

$T_A = -40^{\circ}\text{C}$ to 85°C , $2.4\text{ V} < \text{REG25} < 2.6\text{ V}$; Typical Values at $T_A = 25^{\circ}\text{C}$ and $\text{REG25} = 2.5\text{ V}$ (unless otherwise noted)

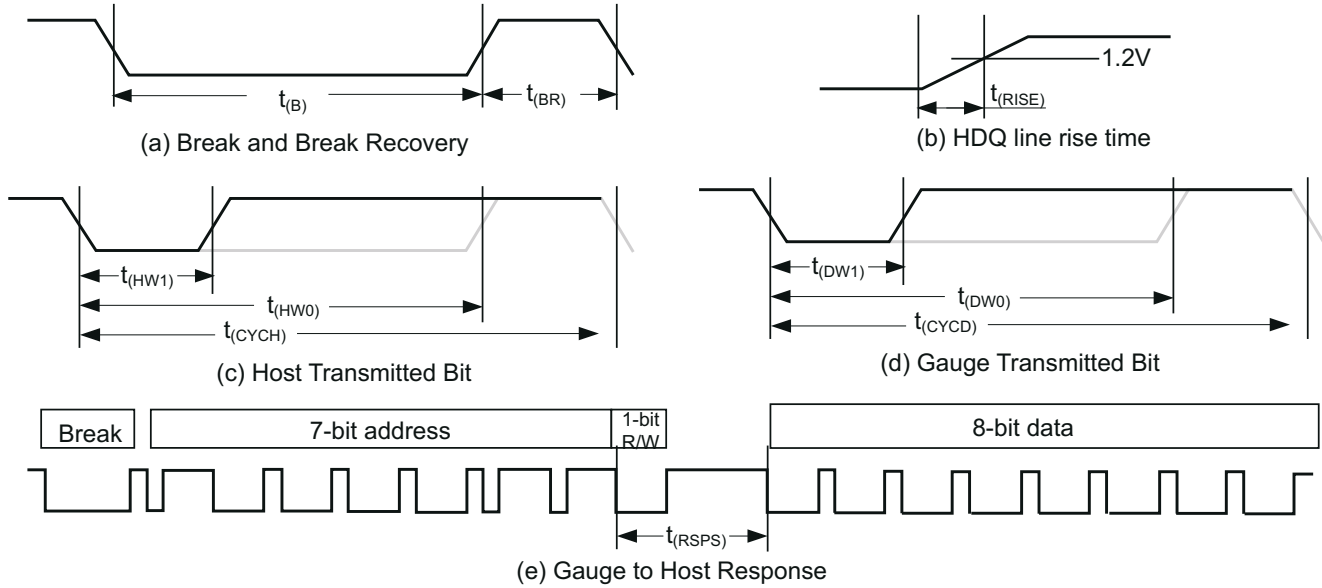
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DR}	Data retention ⁽¹⁾	10			Years
	Flash-programming write cycles ⁽¹⁾	20,000			Cycles
t_{WORDPROG}	Word programming time ⁽¹⁾	2			ms
I_{CCPROG}	Flash-write supply current ⁽¹⁾	5 10			mA

(1) Specified by design. Not tested in production.

6.13 Timing Requirements: HDQ Communication

$T_A = -40^{\circ}\text{C}$ to 85°C , $2.45\text{ V} < V_{\text{REGIN}} = V_{\text{BAT}} < 5.5\text{ V}$; typical values at $T_A = 25^{\circ}\text{C}$ and $V_{\text{REGIN}} = V_{\text{BAT}} = 3.6\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{\text{(CYCH)}}$	Cycle time, host to BQ34Z100-R2	190			μs
$t_{\text{(CYCD)}}$	Cycle time, BQ34Z100-R2 to host	190	205	250	μs
$t_{\text{(HW1)}}$	Host sends 1 to BQ34Z100-R2	0.5			μs
$t_{\text{(DW1)}}$	BQ34Z100-R2 sends 1 to host	32			μs
$t_{\text{(HW0)}}$	Host sends 0 to BQ34Z100-R2	86			μs
$t_{\text{(DW0)}}$	BQ34Z100-R2 sends 0 to host	80			μs
$t_{\text{(RSPS)}}$	Response time, BQ34Z100-R2 to host	190			μs
$t_{\text{(B)}}$	Break time	190			μs
$t_{\text{(BR)}}$	Break recovery time	40			μs
$t_{\text{(RISE)}}$	HDQ line rising time to logic 1 (1.2 V)	950			ns
$t_{\text{(RST)}}$	HDQ Reset	1.8			s

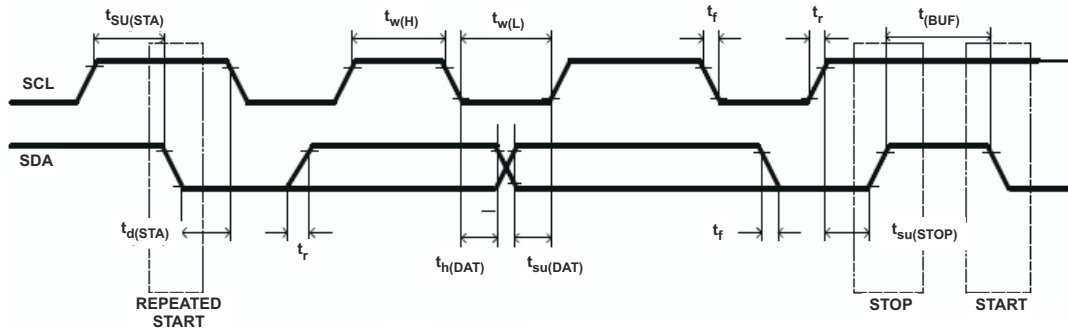


☒ 6-1. Timing Diagrams

6.14 Timing Requirements: I²C-Compatible Interface

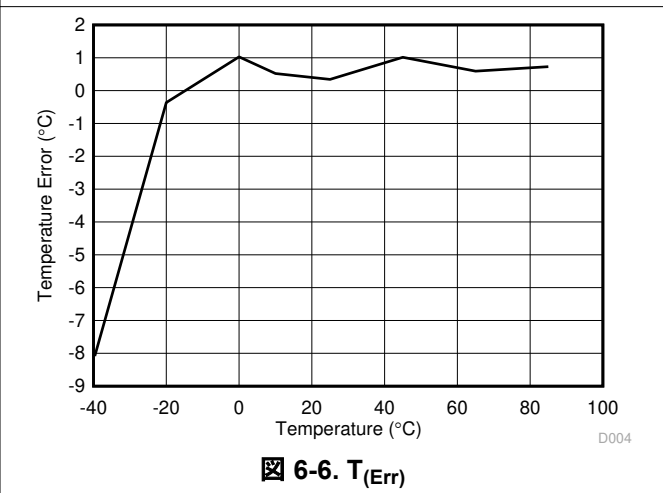
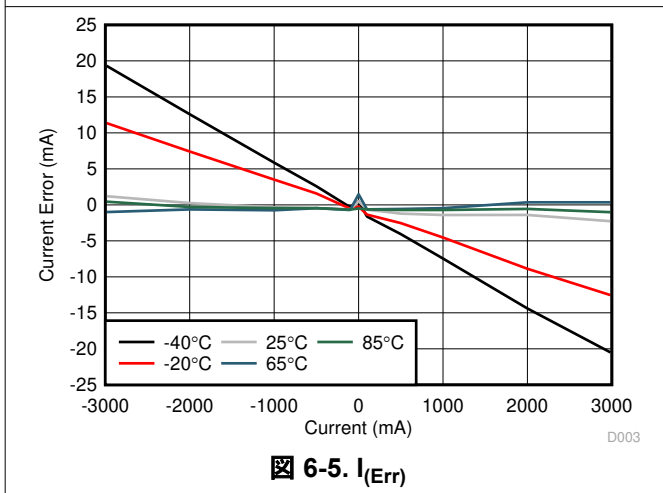
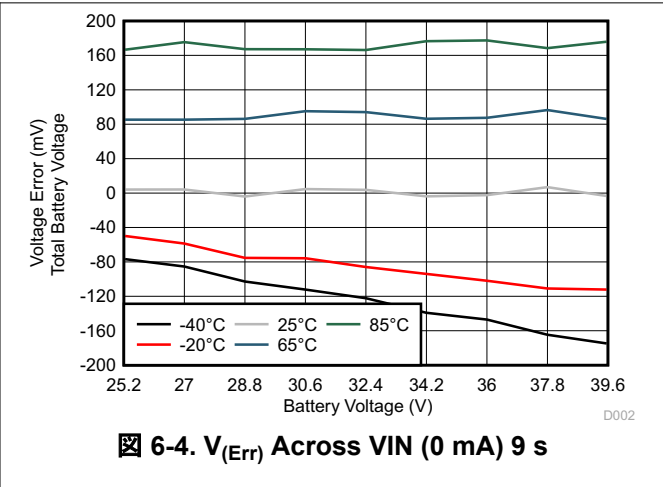
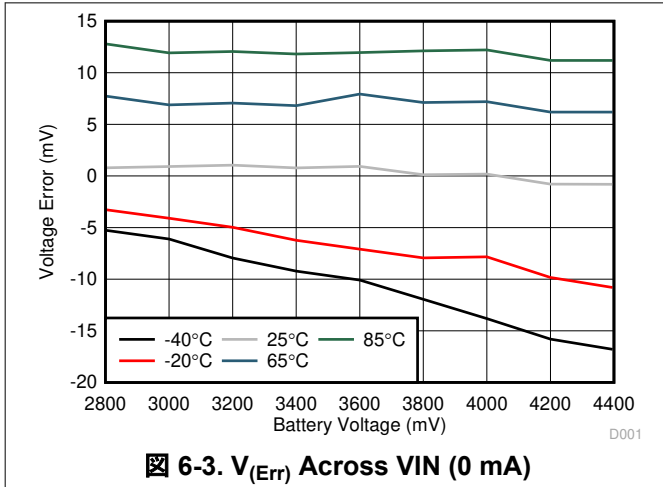
$T_A = -40^\circ\text{C}$ to 85°C , $2.45\text{ V} < V_{\text{REGIN}} = V_{\text{BAT}} < 5.5\text{ V}$; typical values at $T_A = 25^\circ\text{C}$ and $V_{\text{REGIN}} = V_{\text{BAT}} = 3.6\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_r	SCL/SDA rise time				300	ns
t_f	SCL/SDA fall time				300	ns
$t_{w(H)}$	SCL pulse width (high)		600			ns
$t_{w(L)}$	SCL pulse width (low)		1.3			μs
$t_{\text{su(STA)}}$	Setup for repeated start		600			ns
$t_{\text{d(STA)}}$	Start to first falling edge of SCL		600			ns
$t_{\text{su(DAT)}}$	Data setup time		100			ns
$t_{\text{h(DAT)}}$	Data hold time		0			ns
$t_{\text{su(STOP)}}$	Setup time for stop		600			ns
t_{BUF}	Bus free time between stop and start		66			μs
f_{SCL}	Clock frequency				400	kHz

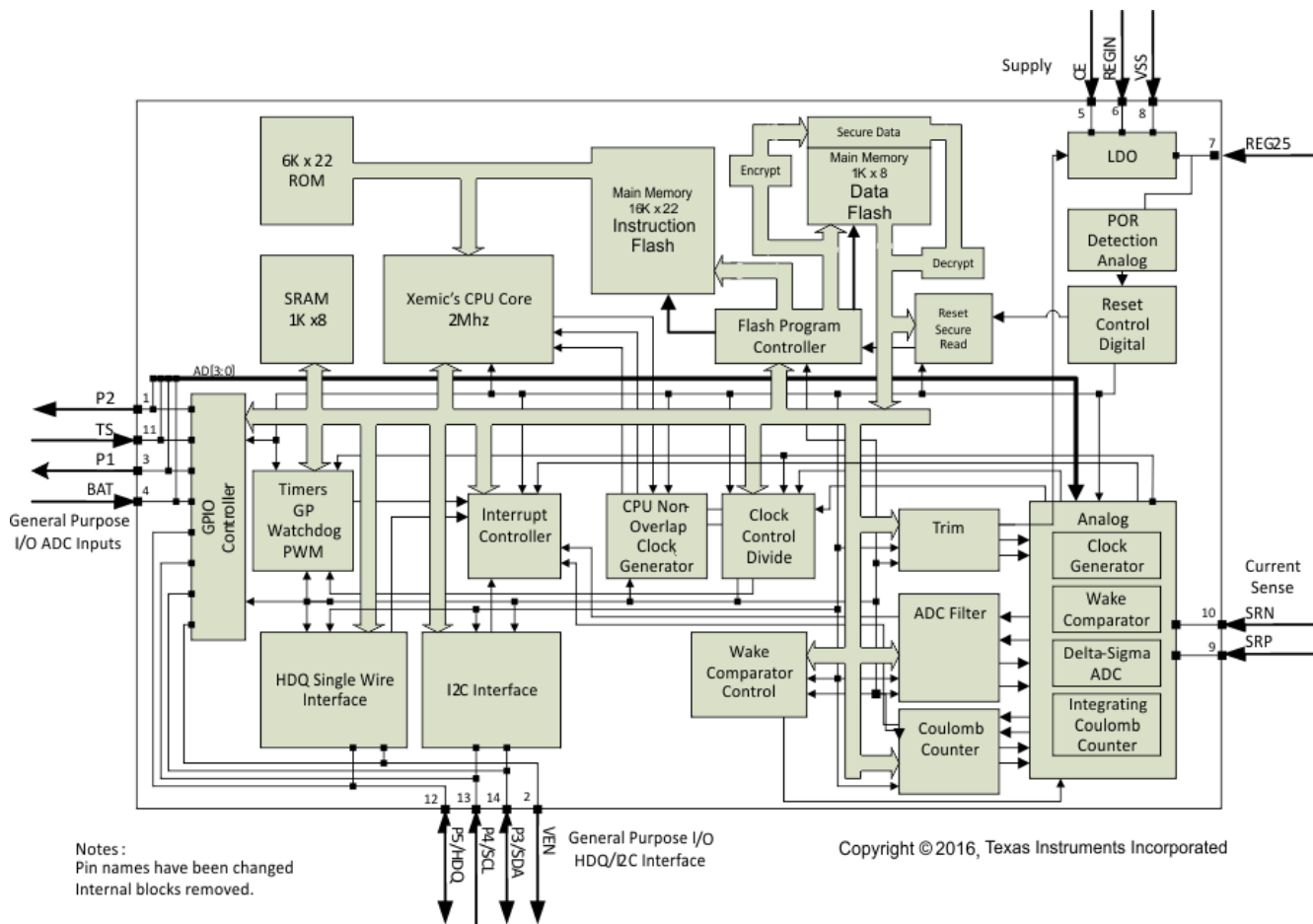


☒ 6-2. I²C-Compatible Interface Timing Diagrams

6.15 Typical Characteristics



7 Functional Block Diagram



8 Application and Implementation

注

以下のアプリケーション情報は、テキサス・インスツルメンツの製品仕様に含まれるものではなく、テキサス・インスツルメンツではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。また、お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The BQ34Z100-R2 is a flexible gas gauge device with many options. The major configuration choices comprise the battery chemistry, digital interface, and display.

8.2 Typical Applications

図 8-1 is a simplified diagram of the main features of the BQ34Z100-R2. Specific implementations detailing the main configuration options are shown later in this section.

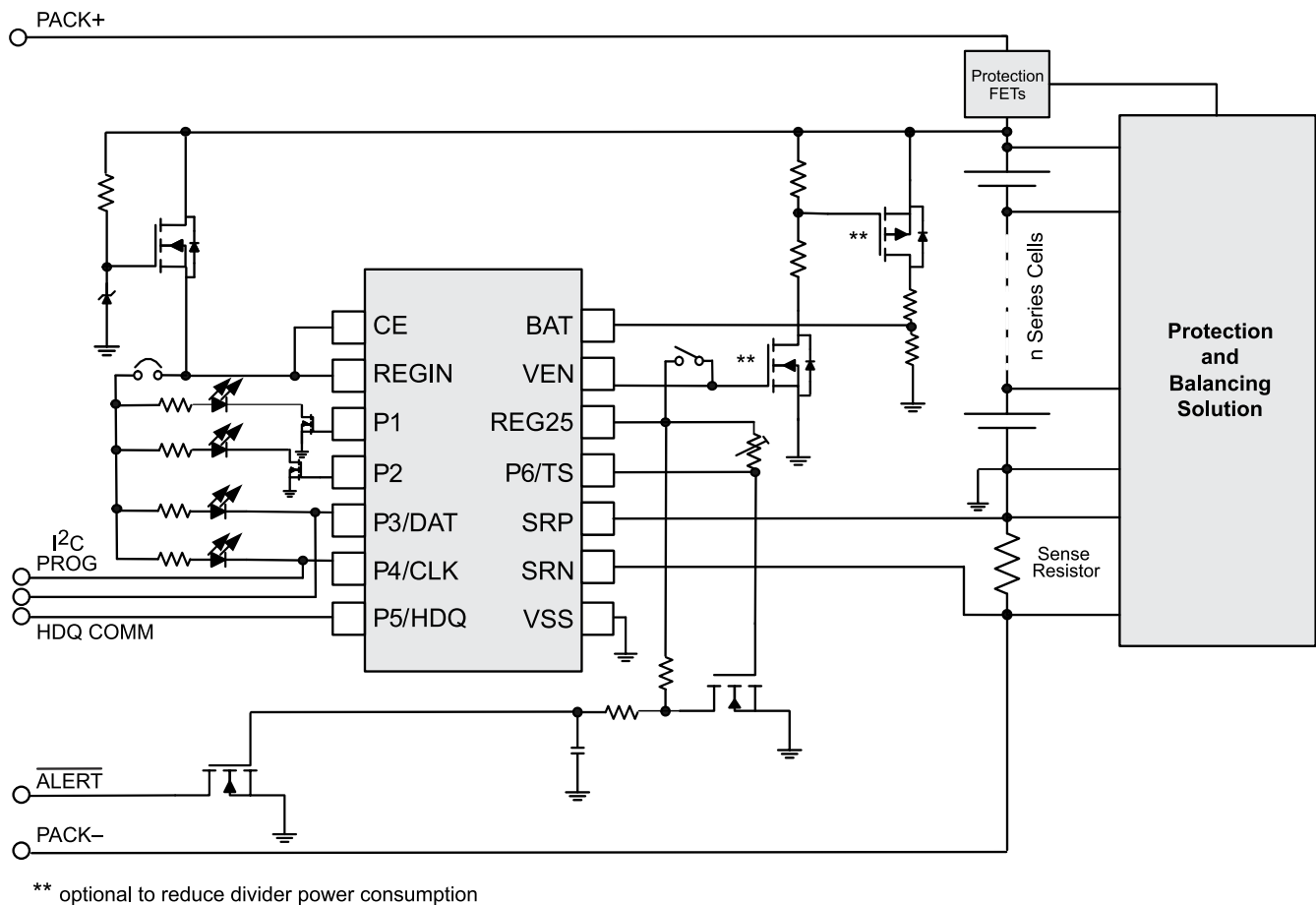
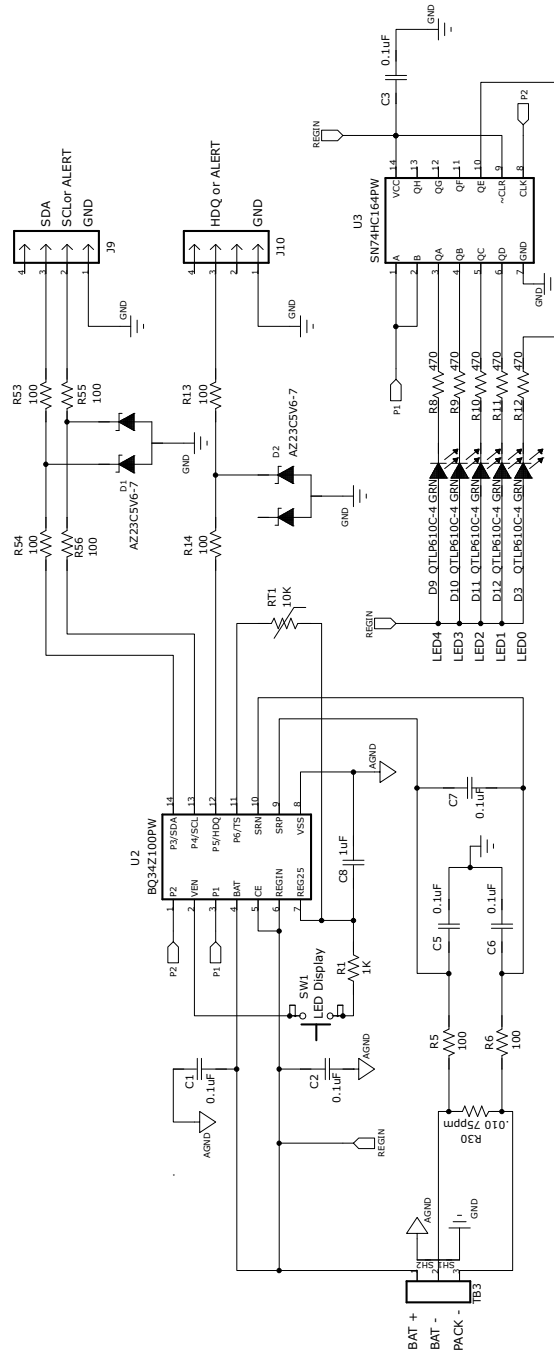


図 8-1. BQ34Z100-R2 Simplified Implementation

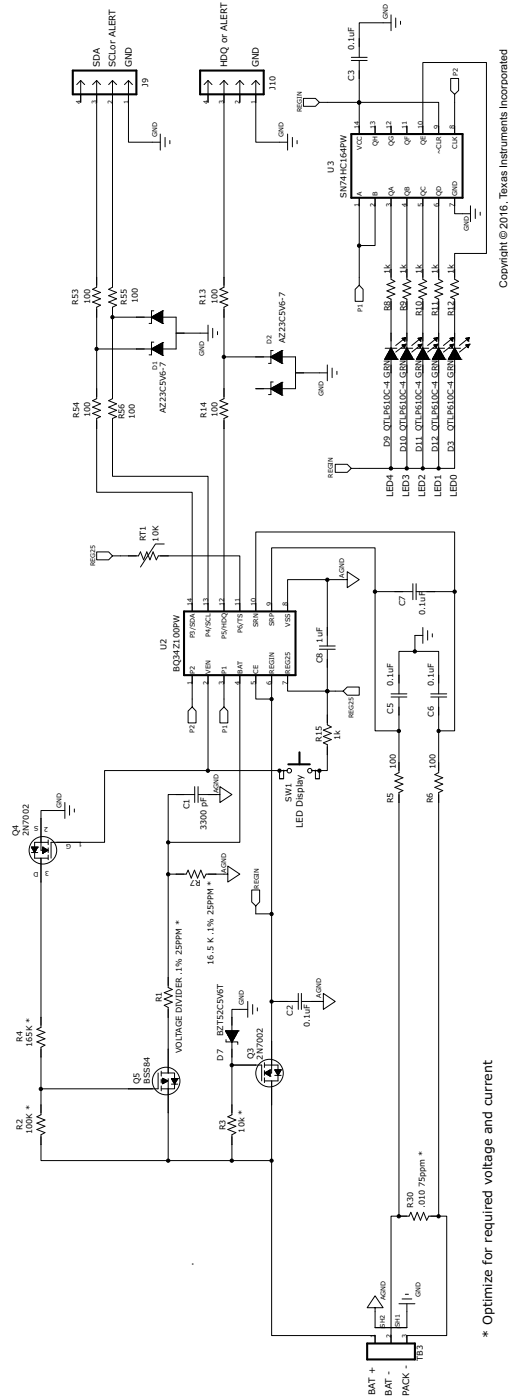
The BQ34Z100-R2 can be used to provide a single Li-ion cell gas gauge with a 5-bar LED display.



Copyright © 2016, Texas Instruments Incorporated

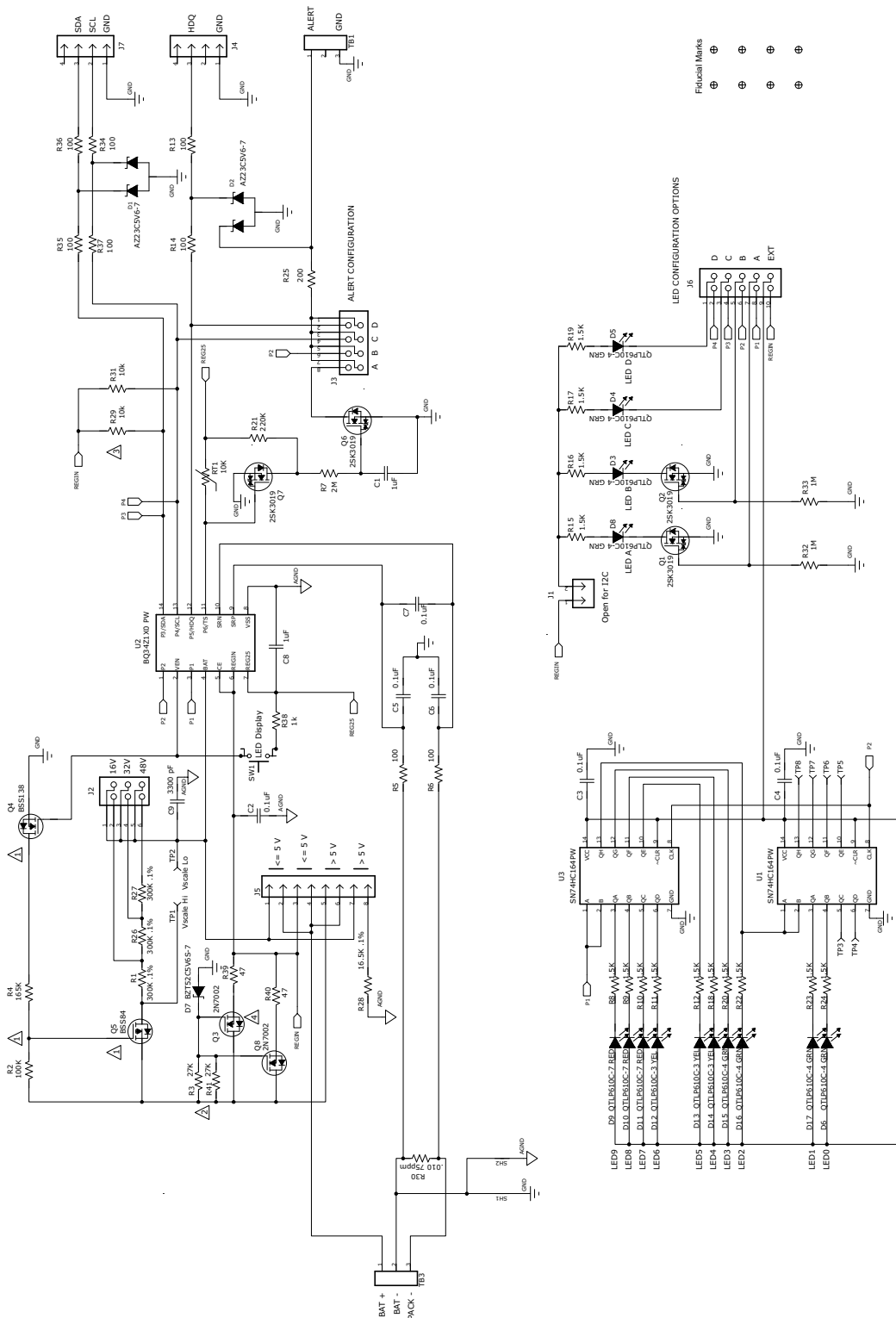
8-2. 1-Cell Li-ion and 5-LED Display

The BQ34Z100-R2 can also be used to provide a gas gauge for a multi-cell Li-ion battery with a 5-bar LED display.



8-3. Multi-Cell and 5-LED Display

☒ 8-4 shows the BQ34Z100-R2 full features enabled.



☒ 8-4. Full-Featured Evaluation Module EVM

8.2.1 Design Requirements

For additional design guidelines, refer to the *BQ34Z100 EVM Wide Range Impedance Track Enabled Battery Fuel Gauge User's Guide (SLUU904)*.

Copyright © 2016, Texas Instruments Incorporated

Optional for additional power saving
 Adjust for minimum current consumption in the application
 I2C pullups normally implemented in the host. Duplicated here since EV2300 does not provide
 Optimize for required LED power dissipation

8.2.2 Detailed Design Procedure

8.2.2.1 Step-by-Step Design Procedure

8.2.2.1.1 STEP 1: Review and Modify the Data Flash Configuration Data.

While many of the default parameters in the data flash are suitable for most applications, the following should first be reviewed and modified to match the intended application.

- **Design Capacity:** Enter the value in mAh divided by *CurrScale()* for the battery, even from the “design energy” point of view.
- **Design Energy:** Enter the value in cWh divided by *EnergyScale()*.
- **Cell Charge Voltage Tx-Ty:** Enter the desired cell charge voltage for each JEITA temperature range.

8.2.2.1.2 STEP 2: Review and Modify the Data Flash Configuration Registers.

- **LED_Comm Configuration:** See in the [BQ34Z100-R2 Technical Reference Manual](#) to aid in selection of an LED mode. Note that the pin used for the optional Alert signal is dependent upon the LED mode selected.
- **Alert Configuration:** See the [BQ34Z100-R2 Technical Reference Manual](#) to aid in selection of which faults trigger the ALERT pin.
- **Number of Series Cells**
- **Pack Configuration:** Ensure that the VOLSEL bit is set for multicell applications and cleared for single-cell applications.

8.2.2.1.3 STEP 3: Design and Configure the Voltage Divider.

If the battery contains more than 1-s cells, a voltage divider network is required. Design the divider network, based on the formula below. The voltage division required is from the highest expected battery voltage, down to approximately 900 mV. For example, using a lower leg resistor of 16.5 K Ω where the highest expected voltage is 32000 mV:

$$R_{\text{series}} = 16.5 \text{ K}\Omega (32000 \text{ mV} - 900 \text{ mV}) / 900 \text{ mV} = 570.2 \text{ K}\Omega$$

Based on price and availability, a 600-K resistor or pair of 300-K resistors could be used in the top leg along with a 16.5-K resistor in the bottom leg.

Set the **Voltage Divider** in the Data Flash Calibration section of the Evaluation Software to 32000 mV with *VoltScale()* = 1.

Use the Evaluation Software to calibrate to the applied nominal voltage; for example, 24000 mV. After calibration, a slightly different value appears in the **Voltage Divider** parameter, which can be used as a default value for the project. For the applications with voltage higher than 65535 mV, please refer to the [BQ34Z100-R2 Technical Reference Manual](#).

Following the successful voltage calibration, calculate and apply the value to **Flash Update OK Cell Volt** as: **Flash Update OK Cell Volt** = 2800 mV \times **Number Of Series Cells** \times 5000 / **Voltage Divider** / *VoltScale()*.

8.2.2.1.4 STEP 4: Determine the Sense Resistor Value.

To ensure accurate current measurement, the input voltage generated across the current sense resistor should not exceed ± 125 mV. For applications with a very high dynamic range, it is allowable to extend this range to absolute maximum of ± 300 mV for overload conditions where a protector device will be taking independent protective action. In such an overloaded state, current reporting and gauging accuracy will not function correctly.

The value of the current sense resistor should be entered into both **CC Gain** and **CC Delta** parameters in the Data Flash Calibration section of the Evaluation Software.

8.2.2.1.5 STEP 5: Review and Modify the Data Flash Gas Gauging Configuration, Data, and State.

- **Load Select:** See *Current Model Used When Load Mode = 0* and *Constant-Power Model Used When Load Mode = 1* in the [BQ34Z100-R2 Technical Reference Manual](#).
- **Load Mode:** See *Current Model Used When Load Mode = 0* and *Constant-Power Model Used When Load Mode =* in the [BQ34Z100-R2 Technical Reference Manual](#).

- **Cell Terminate Voltage:** This is the theoretical voltage where the system begins to fail. It is defined as a zero state-of-charge. Generally, a more conservative level is used to have some reserve capacity. Note the value is for a single cell only.
- **Quit Current:** Generally, this should be set to a value slightly above the expected idle current of the system.
- **Qmax Cell 0:** Start with the C-rate value of your battery.

8.2.2.1.6 STEP 6: Determine and Program the Chemical ID.

Use the BQChem feature in the Evaluation Software to select and program the chemical ID matching your cell. If no match is found, use the procedure defined in TI's ([Mathcad Chemistry Selection Tool \(SLUC138\)](#)).

8.2.2.1.7 STEP 7: Calibrate.

Follow the steps on the **Calibration** screen in the Evaluation Software. Achieving the best possible calibration is important before moving on to Step 8. For mass production, calibration is not required for single-cell applications. For multi-cell applications, only voltage calibration is required. Current and temperature may be calibrated to improve gauging accuracy if needed.

8.2.2.1.8 STEP 8: Run an Optimization Cycle.

Refer to the [Preparing Optimized Default Flash Constants for Specific Battery Types Application Report \(SLUA334B\)](#).

9 Power Supply Recommendations

Power supply requirements for the BQ34Z100-R2 are simplified due to the presence of the internal LDO voltage regulation. The REGIN pin accepts any voltage level between 2.7 V and 4.5 V, which is optimum for a single-cell Li-ion application. For higher battery voltage applications, a simple pre-regulator can be provided to power the bq34Z100-R2 and any optional LEDs. Decoupling the REGIN pin should be done with a 0.1- μ F 10% ceramic X5R capacitor placed close to the device. While the pre-regulator circuit is not critical, special attention should be paid to its quiescent current and power dissipation. The input voltage should handle the maximum battery stack voltage. The output voltage can be centered within the 2.7-V to 4.5-V range as recommended for the REGIN pin.

For high stack count applications, a commercially available LDO is often the best quality solution, but comes with a cost tradeoff. To lower the BOM cost, the following approaches are recommended.

In [Figure 9-1](#), Q1 is used to drop the battery stack voltage to roughly 4 V to power the BQ34Z100-R2 REGIN pin and also to feed the anode of any LEDs used in the application. To avoid unwanted quiescent current consumption, R1 should be set as high as is practical. It is recommended to use a low-current Zener diode.

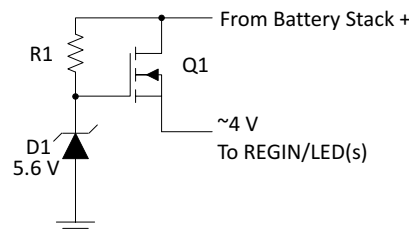


Figure 9-1. Q1 Dropping Battery Stack Voltage to 4 V

Alternatively, if the range of a high-voltage battery stack can be well defined, a simple source follower based on a resistive divider can be used to lower the BOM cost and the quiescent current. For example:

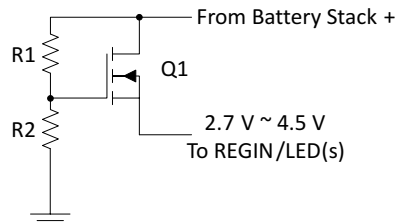


Figure 9-2. Source Follower on a Resistive Divider

Power dissipation of the linear pre-regulator may become an important design decision when multiple LEDs are employed in the application. For example, the BQ34Z100-R2 EVM uses a pair of FETs in parallel to inexpensively dissipate enough power for 10-LED evaluation.

10 Layout

10.1 Layout Guidelines

10.1.1 Introduction

Attention to layout is critical to the success of any battery management circuit board. The mixture of high-current paths with an ultralow-current microcontroller creates the potential for design issues that are not always trivial to solve. Some of the key areas of concern are described in the following sections, and can help to enable success.

10.1.2 Power Supply Decoupling Capacitor

Power supply decoupling from VCC to ground is important for optimal operation of the gas gauge. To keep the loop area small, place this capacitor next to the IC and use the shortest possible traces. A large loop area renders the capacitor useless and forms a small-loop antenna for noise pickup.

Ideally, the traces on each side of the capacitor should be the same length and run in the same direction to avoid differential noise during ESD. If possible, place a via near the VSS pin to a ground plane layer.

10.1.3 Capacitors

Power supply decoupling for the gas gauges requires a pair of 0.1- μ F ceramic capacitors for (BAT) and (VCC) pins. These should be placed reasonably close to the IC without using long traces back to VSS. The LDO voltage regulator, whether external or internal to the main IC, requires a 0.47- μ F ceramic capacitor to be placed fairly close to the regulation output pin. This capacitor is for amplifier loop stabilization and as an energy well for the 2.5-V supply.


10.1.4 Communication Line Protection Components

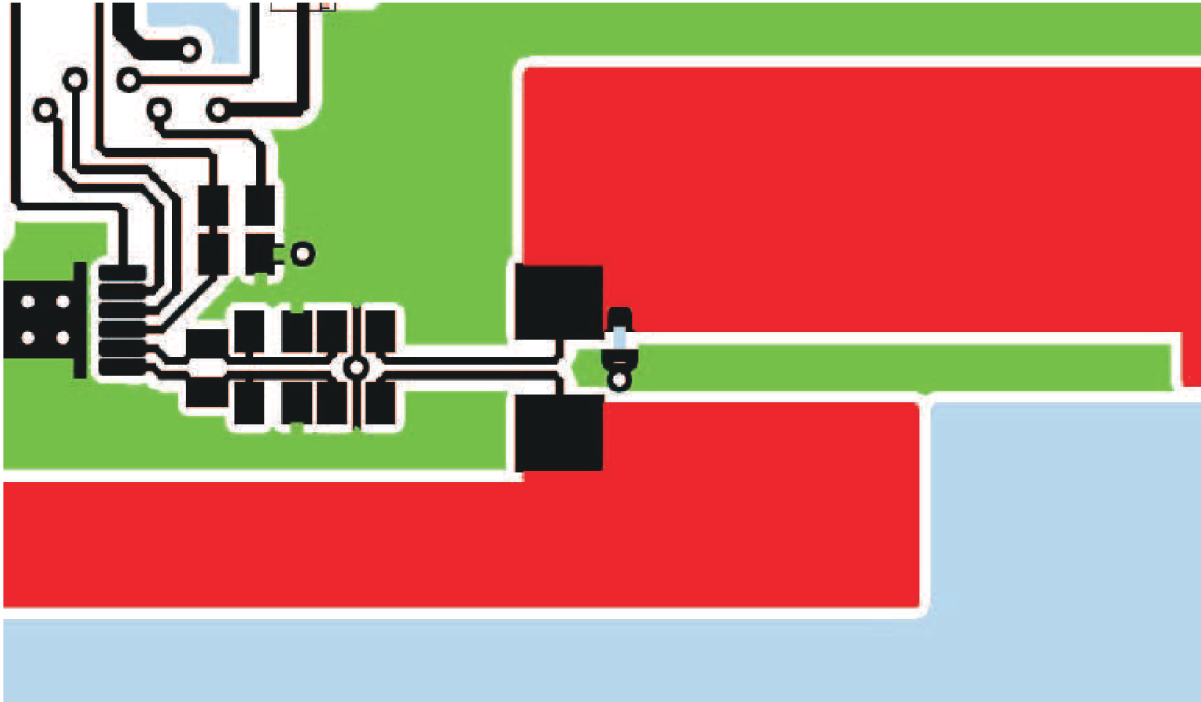
The 5.6-V Zener diodes, used to protect the communication pins of the gas gauge from ESD, should be located as close as possible to the pack connector. The grounded end of these Zener diodes should be returned to the Pack(-) node rather than to the low-current digital ground system. This way, ESD is diverted away from the sensitive electronics as much as possible.

In some applications, it is sometimes necessary to cause transitions on the communication lines to trigger events that manage the gas gauge power modes. An example of one of these transitions is detecting a sustained low logic level on the communication lines to detect that a pack has been removed. Given that most of the gas gauges do not have internal pulldown networks, it is necessary to add a weak pulldown resistor to accomplish this when there's an absence of a strong pullup resistor on the system side. If the weak pulldown resistor is used, it may take less board space to use a small capacitor in parallel instead of the Zener diode to absorb any ESD transients that are received through communication lines.

10.2 Layout Example

10.2.1 Ground System

The gas gauge requires a low-current ground system separate from the high-current PACK(-) path. ESD ground is defined along the high-current path from the PACK(-) terminal to low-side protector FETs (if present) or the sense resistor. It is important that the low-current ground systems only connect to the BAT(-) path at the sense resistor Kelvin pick-off point. It is recommended to use an optional inner layer ground plane for the low-current ground system. In  10-1, the green is an example of using the low-current ground as a shield for the gas gauge circuit. Notice how it is kept separate from the high-current ground, which is shown in red. The high-current path is joined with the low-current path only at one point, shown with the small blue connection between the two planes.



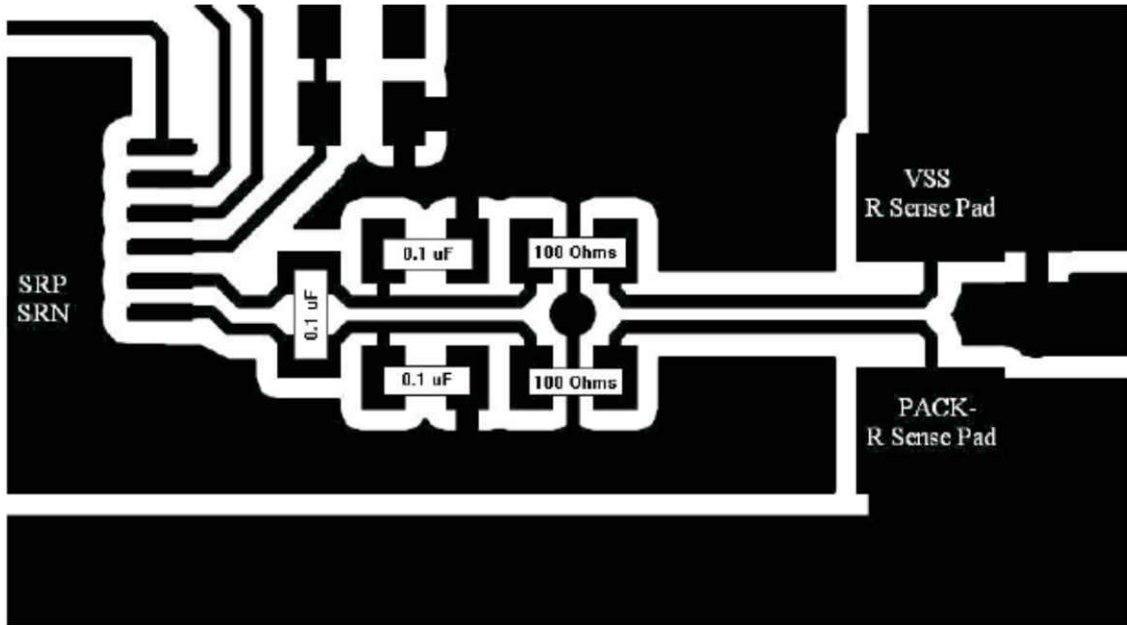
☒ 10-1. Differential Filter Component with Symmetrical Layout

10.2.2 Kelvin Connections

Kelvin voltage sensing is very important to accurately measure current and cell voltage. Notice how the differential connections at the sense resistor do not add any voltage drop across the copper etch that carries the high current path through the sense resistor. See ☒ 10-1 and ☒ 10-2.

10.2.3 Board Offset Considerations

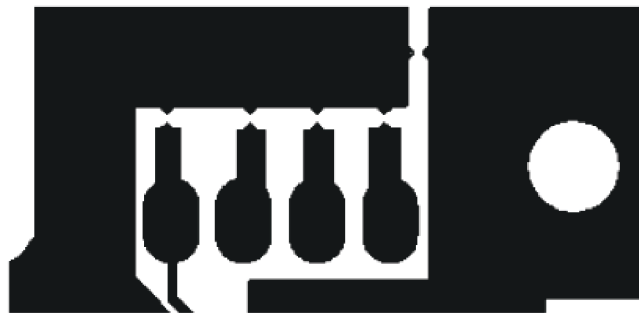
Although the most important component for board offset reduction is the decoupling capacitor for V_{CC} , additional benefit is possible by using this recommended pattern for the coulomb counter differential low-pass filter network. Maintain the symmetrical placement pattern shown for optimum current offset performance. Use symmetrical shielded differential traces, if possible, from the sense resistor to the 100- Ω resistors, as shown in ☒ 10-2.



☒ 10-2. Differential Connection Between SRP and SRN Pins with Sense Resistor

10.2.4 ESD Spark Gap

Protect the communication lines from ESD with a spark gap at the connector. ☒ 10-3 shows the recommended pattern with its 0.2-mm spacing between the points.



☒ 10-3. Recommended Spark-Gap Pattern Helps Protect Communication Lines from ESD

11 Device and Documentation Support

11.1 Documentation Support

For related documentation, see the following:

- [BQ34Z100-R2 Technical Reference Manual](#)
- [BQ34Z100-R2 High Cell Count and High Capacity Applications application report](#)

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](#) のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の [使用条件](#) を参照してください。

11.4 Trademarks

Impedance Track™ is a trademark of Texas Instruments.

TI E2E™ are trademarks of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

11.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ34Z100PWR-R2	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	34Z100	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/G 08/15

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス・デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、または [ti.com](https://www.ti.com) やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所 : Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2023, Texas Instruments Incorporated