TEXAS INSTRUMENTS
BQ77207
JAJSND4A – DECEMBER 2021 – REVISED JUNE 2022

BQ77207 3～7 直列セル・リチウムイオン向け電圧 / 温度保護、内部遅延タイマ付き

1 特長

- 3 直列セルから 7 直列セルまでの保護
- 高精度過電圧保護
  - 25℃で ±10mV
  - 0℃～60℃で ±20mV
- 3.55V～5.1V の過電圧保護オプション
- 1.0V～3.5V の低電圧保護オプション
- 断線検出
- NTC または PTC を使用した過熱保護
- セルをランダムに接続可能
- 機能安全対応
- 固定の内部遅延タイマ
- 固定の検出スレッショルド
- 固定の出力駆動タイプ (COUT と DOUT のそれぞれ)
  - アクティブ HIGH またはアクティブ LOW
  - 6V へのアクティブ HIGH 駆動
  - オープン・ドレイン、外部から VDD にプルアップ可能
- 低消費電力 I_{CC} ≈ 1μA ($V_{CELL(ALL)}$ < V_{OV})
- セル入力あたりのリーク電流:100nA 未満 (断線検出が無効の場合)
- パッケージの占有面積オプション
  - 12 ピン WSON、0.5mm ピン・ピッチ

2 アプリケーション

- 次のものに使用されるリチウムイオン・バッテリ・パックの保護:
  - ハンドヘルド園芸用器具
  - ハンドヘルド電動工具
  - コードレス真空掃除機
  - UPS バッテリ・バックアップ
  - 軽量電動車両 (電動自転車、電動スクーター、ペダル・アシスト自転車)

3 概要

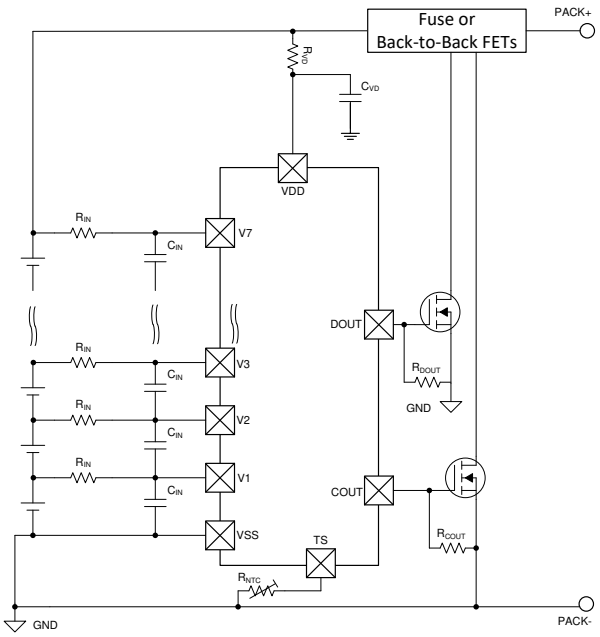
BQ77207 製品ファミリは、過電圧 (OVP)、低電圧 (UVP)、断線 (OW)、および過熱 (OT) 保護など、リチウムイオン・バッテリ・パック・システムのための幅広い電圧および温度監視機能を提供します。各セルの過電圧、低電圧、断線条件を別々に監視できます。外部 NTC または PTC サーミスタを追加すると、本デバイスは過熱条件を検出できます。

BQ77207 デバイスでは、過電圧、低電圧、断線、、過熱のいずれかの条件を検出すると、内部遅延タイマが起動します。遅延タイマが満了すると、各出力はアクティブ状態 (構成により HIGH または LOW) にトリガされます。

「製品情報」の表

部品番号	パッケージ(1)	本体サイズ (公称)
BQ7720700	WSON (12)	3.0mm × 2.0mm

(1) 利用可能なカタログ・パッケージについては、このデータシートの末尾にある注文情報および *Device Comparison Table* を参照してください。



概略回路図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (December 2021) to Revision A (June 2022)	Page
• Added the BQ7720701 and BQ7720702 devices to セクション 6; added the OVP and UVP output delays	3

5 概要 (続き)

フォルトが検出された場合、過電圧であれば COUT ピンがトリガされ、低電圧であれば DOUT ピンがトリガされます。過熱、、または断線フォルトが検出された場合、DOUT と COUT の両方がトリガされます。生産ライン・テストを迅速に行えるよう、BQ77207 デバイスは遅延時間を大幅に短縮したカスタマ・テスト・モード (CTM) を備えています。

6 Device Comparison Table

PART NUMBER(1)	T_A	PACKAGE	PACKAGE DESIGNATOR	OVP (V)	OV HYSTERESIS (V)	OVP OUTPUT DELAY	UVP (V)
BQ7720700	–40°C to 110°C	12-Pin WSON	DSS	4.325	0.100	1 s	2.25
BQ7720701	–40°C to 110°C	12-Pin WSON	DSS	4.275	0.100	1 s	2
BQ7720702	–40°C to 110°C	12-Pin WSON	DSS	4.275	0.100	4 s	2

PART NUMBER (CONT.)(1)	UV HYSTERESIS (V)	UVP OUTPUT DELAY	OT (°C)	OW	LATCH	OUTPUT DRIVE	TAPE AND REEL
BQ7720700	0.100	1 s	70	Enabled	Disabled	Active High 6 V	BQ7720700DSSR
BQ7720701	0.100	1 s	80	Enabled	Disabled	Active High 6 V	BQ7720701DSSR
BQ7720702	0.100	2 s	80	Enabled	Disabled	Active High 6 V	BQ7720702DSSR

(1) For future options, contact TI for more information.

7 Pin Configuration and Functions

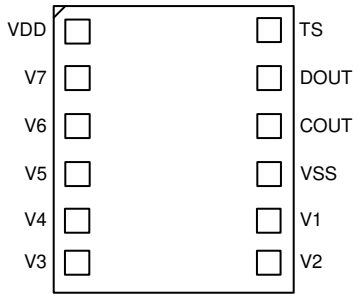


図 7-1. BQ77207 Pin Diagram

12-Pin Functions

NO.	NAME	TYPE(1)	DESCRIPTION
1	VDD	P	Power supply
2	V7	I	Sense input for positive voltage of the seventh cell from the bottom of the stack
3	V6	I	Sense input for positive voltage of the sixth cell from the bottom of the stack
4	V5	I	Sense input for positive voltage of the fifth cell from the bottom of the stack
5	V4	I	Sense input for positive voltage of the fourth cell from the bottom of the stack
6	V3	I	Sense input for positive voltage of the third cell from the bottom of the stack
7	V2	I	Sense input for positive voltage of the second cell from the bottom of the stack
8	V1	I	Sense input for positive voltage of the first cell from the bottom of the stack
9	VSS	P	Electrically connected to IC ground and negative terminal of the lowest cell in the stack
10	COUT	O	Output drive for overvoltage, open wire, and overtemperature. It can be left floating if not used.
11	DOUT	O	Output drive for undervoltage, open wire, and overtemperature. It can be left floating if not used.
12	TS	I	Temperature sensor input. If not used, leave it NC.

(1) I = Input, O = Output, P = Power Connection

8 仕様

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage range	VDD - VSS (2)	–0.3	45	V
Input voltage range	Vn - VSS where n = 1 to 7	–0.3	45	V
	TS	–0.3	1.5	V
Output voltage range	COUT - VSS, DOUT - VSS	–0.3	45	V
Functional temperature,T_{FUNC}		–40	110	°C
Storage temperature, T_{STG}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) DC Voltage applied on this pin should be limited to a maximum of 40 V. Stresses to this pin at voltages beyond this level, up to the 45-V specified maximum level, should be limited to short transients.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage (1)	5		38.5	V
V_{IN}	Input voltage range of Vn - Vn-1 where n = 2 to 7 and V1 - VSS	0		5	V
	TS	0		1.5	V
V_{CTM}	Customer Test Mode Entry V_{DD} > V7 + V_{CTM}	12		13	V
C_{TS}	Total capacitance on the TS Pin			200	pF
T_A	Ambient temperature	–40		85	°C
T_J	Junction temperature	–65		150	°C

(1) V_{DD} is equal to top of stack voltage.

8.4 Thermal Information

THERMAL METRIC(1)		DEVICE DSS 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	67.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	68.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	35.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	35.9	°C/W

8.4 Thermal Information (continued)

THERMAL METRIC[1]		DEVICE DSS 12 PINS	UNIT
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	14	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

8.5 DC Characteristics

Typical values stated where T_A = 25°C and VDD = 25 V, MIN/MAX values stated where T_A = –40°C to 85°C and VDD = 5 V to 38.5 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OVER VOLTAGE PROTECTION (OV)						
V_{OV}	OV Detection Range		3.55		5.1	V
V_{OV_STEP}	OV Detection Steps			25		mV
V_{OV_HYS}	OV Detection Hysteresis	Selected OV Hysteresis depends on part number. See device selection table for details.		V_{OV} – 50		mV
		Selected OV Hysteresis depends on part number. See device selection table for details.		V_{OV} – 100		mV
V_{OV_ACC}	OV Detection Accuracy	T_A = 25°C	–10		10	mV
	OV Detection Accuracy	0°C ≤ T_A ≤ 60°C	–20		20	mV
	OV Detection Accuracy	-40°C ≤ T_A ≤ 110°C	–50		50	mV
UNDER VOLTAGE PROTECTION (UV)						
V_{UV}	UV Detection Range		1.0		3.5	V
V_{UV_STEP}	UV Detection Steps			50		mV
V_{UV_HYS}	UV Detection Hysteresis	Selected OV Hysteresis depends on part number. See device selection table for details.		V_{UV} + 50		mV
		Selected OV Hysteresis depends on part number. See device selection table for details.		V_{UV} + 100		mV
V_{UV_ACC}	UV Detection Accuracy	T_A = 25°C	–30		30	mV
	UV Detection Accuracy	-40 ≤ T_A ≤ 110°C	–50		50	mV
V_{UV_MIN}	UV Detection Disabled Threshold	Vn - Vn-1 where n = 2 to 7 and V1 - VSS	450	500	550	mV
OVER TEMPERATURE PROTECTION (OT)						
T_{OT}	OT Detection Range	Available options: 62°C, 65°C, 70°C, 75°C, 80°C, 83°C	62.0		83.0	°C
$R_{OT\_EXT\_NTC}$	NTC OT Detection External Resistance			2850		Ω
				2570		
				2195		
				1915		
				1651		
				1525		
$R_{OT\_EXT\_PTC}$	PTC OT Detection External Resistance			111100		Ω

8.5 DC Characteristics (continued)

Typical values stated where T_A = 25°C and VDD = 25 V, MIN/MAX values stated where T_A = –40°C to 85°C and VDD = 5 V to 38.5 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{OT_ACC} (1)	OT Detection Accuracy (NTC)		–5		5	°C
T_{OT_HYS} (2)	OT Detection Hysteresis (NTC)			–10		°C
				4186		Ω
				3530		Ω
R_{TC}	Internal Pull Up Resistor	After TI Factory Trim	19.4	20	20.6	kΩ
UNDER TEMPERATURE PROTECTION (UT)						
T_{UT}	UT Detection Threshold		–30.0		0.0	°C
$R_{UT\_EXT\_NTC}$	NTC UT Detection External Resistance			111100		Ω
				68900		
				42200		
				26700		
R_{UT_ACC}	UT Detection External Resistance Accuracy		–2%		2%	
T_{UT_HYS}	UT Detection Hysteresis (NTC)			10		°C
				17800		Ω
T_{UT_ACC} (1)	UT Detection Accuracy (NTC)		–5		5	°C
OPEN WIRE PROTECTION (OW)						
V_{OW}	OW Detection Threshold	Vn < Vn-1 where n = 2 to 7		–200		mV
		V1 - VSS		500		mV
V_{OW_HYS}	OW Detection Hysteresis	Vn < Vn-1 where n = 1 to 7		V_{OW} +100		mV
V_{OW_ACC}	OW Detection Accuracy	-40 °C ≤ T_A ≤ 110°C	–25		25	mV
SUPPLY AND LEAKAGE CURRENT						
I_{CC}	Supply Current	No fault detected.		2	3.5	µA
I_{CC_FAULT}	Supply Current	Fault detected, COUT active High 6V output, DOUT active low. Other faults		20	25	µA
I_{CC_FAULT}	Supply Current	Fault detected, COUT active High 6V output, DOUT active low. UV fault only		3	5	µA
I_{IN} (2)	Input Current at Vx Pins	Vn - Vn-1 and V1 - VSS = 4V, where n = 2 to 7, Open Wire Enabled	–0.3		0.3	µA
		Vn - Vn-1 and V1 - VSS = 4V, where n = 2 to 7, Open Wire Disabled	–0.1		0.1	µA
OUTPUT DRIVE, COUT and DOUT, CMOS ACTIVE HIGH VERSIONS ONLY						
V_{OUT_AH}	Output Drive Voltage for COUT and DOUT, Active High 6V	Vn - Vn-1 or V1 - VSS > V_{OV}, where n = 2 to 7, VDD = 25V, I_{OH} = 100 µA measured out of COUT, DOUT pin.	6			V
	Output Drive Voltage for COUT and DOUT, Active High VDD	VDD - V_{COUT} or V_{DOUT}, Vn - Vn-1 or V1 - VSS > V_{OV}, where n = 2 to 7, I_{OH} = 10 µA measured out of COUT, DOUT pin.	0	1	1.5	V
	Output Drive Voltage for COUT and DOUT, Active High 6V	VDD - V_{COUT} or V_{DOUT}, If 6 of 7 cells are short circuited and only one cell remains powered and > V_{OV}, VDD = Vx (cell voltage), I_{OH} = 100 µA,	0	1	1.5	V
	Output Drive Voltage for COUT and DOUT, Active High 6V and VDD	Vn - Vn-1 and V1 - VSS < V_{OV}, where n = 2 to 7, VDD = 25 V, I_{OH} = 100 µA measured into pin		250	400	mV
R_{OUT_AH}	Internal Pull Up Resistor		80	100	120	kΩ

8.5 DC Characteristics (continued)

Typical values stated where T_A = 25°C and VDD = 25 V, MIN/MAX values stated where T_A = –40°C to 85°C and VDD = 5 V to 38.5 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{OUT\_AH\_H}$	OUT Source Current (during OV)	Vn - Vn-1 or V1 - VSS > V_{OV}, where n = 2 to 7, VDD = 25 V, OUT = 0V. Measured out of COUT, DOUT pin			6.5	mA
$I_{OUT\_AH\_L}$	OUT Sink Current (no OV)	Vn - Vn-1 and V1 - VSS < V_{OV}, where n = 2 to 7, VDD = 25 V, OUT = VDD. Measured into COUT, DOUT pin	0.3		3	mA
OUTPUT DRIVE, COUT and DOUT, NCH OPEN DRAIN ACTIVE LOW VERSIONS ONLY						
V_{OUT_AL}	Output Drive Voltage for COUT and DOUT, Active Low	Vn - Vn-1 or V1 - VSS > V_{OV}, where n = 2 to 7, VDD = 25 V, I_{OH} = 100 µA measured into COUT, DOUT pin.		250	400	mV
$I_{OUT\_AL\_L}$	OUT Source Current (during OV)	Vn - Vn-1 or V1 - VSS > V_{OV}, where n = 2 to 7, VDD = 25 V, OUT = VDD. Measured into COUT, DOUT pin.	0.3		3	mA
$I_{OUT\_AL\_H}$	OUT Sink Current (no OV)	Vn - Vn-1 and V1 - VSS < V_{OV}, where n = 2 to 7, VDD = 25 V, OUT = VDD. Measured out of COUT, DOUT pin.			100	nA

(1) Assured by design. This accuracy assumes the external resistance is within ±2% of the R_OT_EXT values for the corresponding temperature threshold.
(2) Assured by design

8.6 Timing Requirements

Typical values stated where T_A = 25°C and VDD = 25 V, MIN/MAX values stated where T_A = –40°C to 85°C and VDD = 5 V to 38.5 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OV_DELAY}	OV Delay Time			0.25		s
				0.5		s
				1		s
				2		s
				4		s
t_{UV_DELAY}	UV Delay Time			0.25		s
				0.5		s
				1		s
				2		s
t_{OT_DELAY}	OT Delay Time			4		s
t_{OW_DELAY}	OW Delay Time			4		s
t_{DELAY_ACC}	Delay Time Accuracy	For 0.25s, 0.5s delays	–128		128	ms
t_{DELAY_ACC}	Delay Time Accuracy	For 1s delays	–150		150	ms
t_{DELAY_DR}	Delay time drift across operating temp	For all delays other than 0.25s, 0.5s, 1s delays	–10%		10%	
t_{CTM_DELAY}	Fault Detection Delay Time during Customer Test Mode	See Customer Test Mode.		50		ms

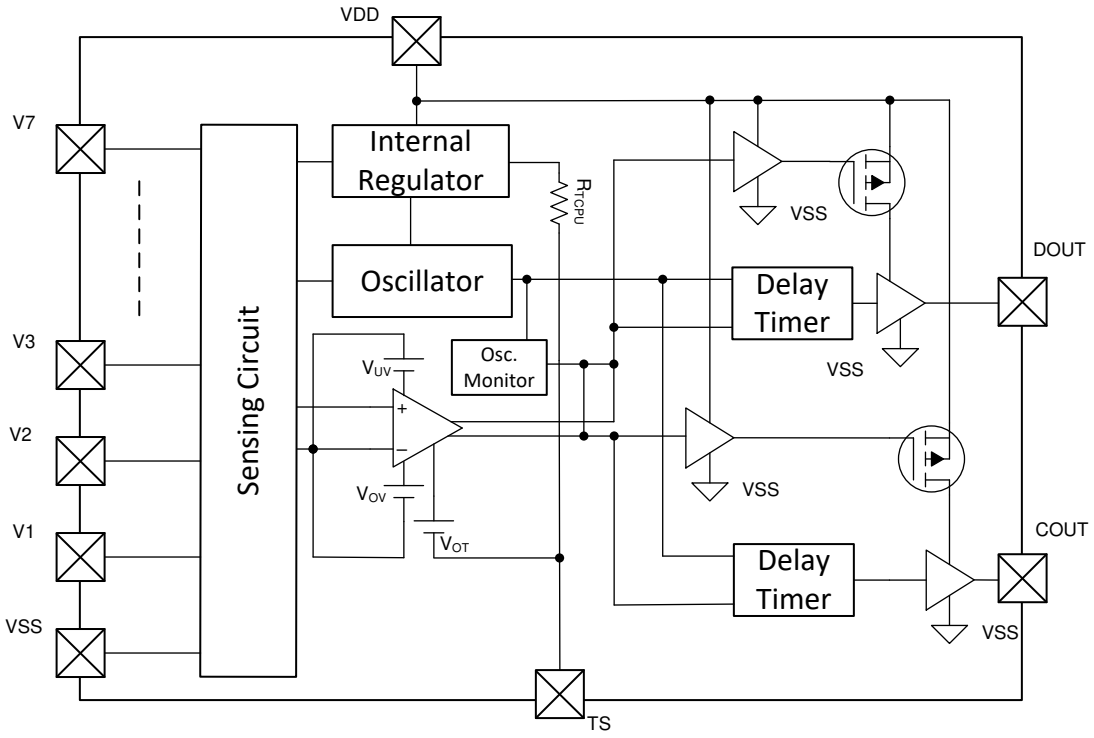
9 Detailed Description

9.1 Overview

The BQ77207 family of devices provides a range of voltage and temperature monitoring including overvoltage (OVP), undervoltage (UVP), open wire (OW), and overtemperature (OT) protection for Li-ion battery pack systems. Each cell is monitored independently for overvoltage, undervoltage, and open-wire conditions. With the addition of an external NTC thermistor, the device can detect overtemperature conditions. An internal delay timer is initiated upon detection of an overvoltage, undervoltage, open-wire, or overtemperature condition. Upon expiration of the delay timer, the respective output is triggered into its active state (either high or low depending on the configuration). The overvoltage triggers the COUT pin if a fault is detected, and undervoltage triggers the DOUT pin if a fault is detected. If an undertemperature, overtemperature, or open-wire fault is detected, then both the DOUT and COUT are triggered.

For quicker production-line testing, the BQ77207 device provides a Customer Test Mode (CTM) with greatly reduced delay time.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Voltage Fault Detection

In the BQ77207 device, each cell is monitored independently. Overvoltage is detected by comparing the actual cell voltage to a protection voltage reference, V_{OV}. If any cell voltage exceeds the programmed OV value, a timer circuit is activated. When the timer expires, the COUT pin goes from inactive to active state. The timer is reset if the cell voltage falls below the recovery threshold ($V_{OV} – V_{OV\_HYS}$). Undervoltage is detected by comparing the actual cell voltage to a protection voltage reference, V_{UV}. If any cell voltage falls below the programmed UV value, a timer circuit is activated. When the timer expires, the DOUT pin goes from inactive to active state. The timer is reset if the cell voltage rises below the recovery threshold ($V_{UV} + V_{UV\_HYS}$).

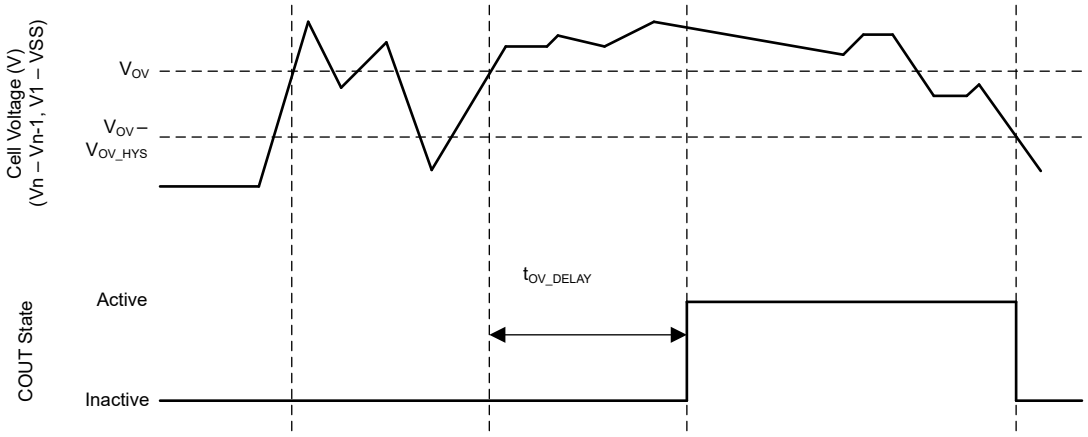


図 9-1. Timing for Overvoltage Sensing

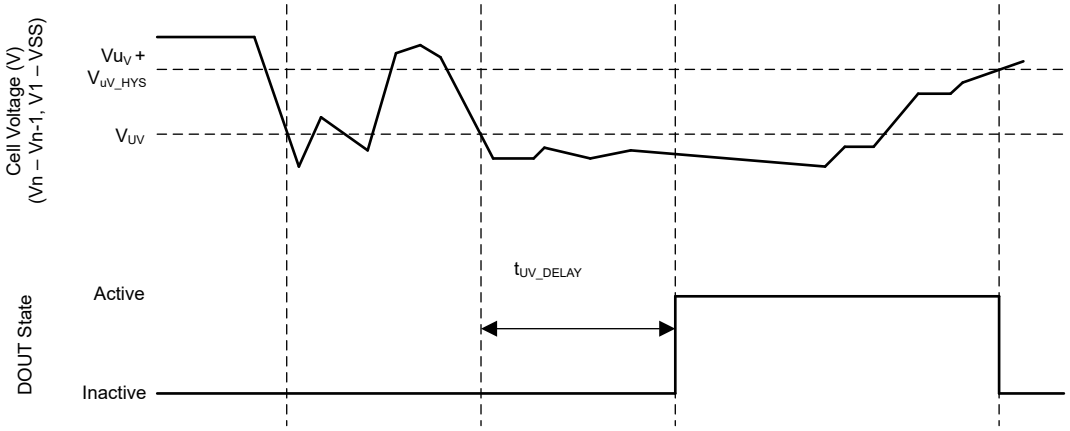


図 9-2. Timing for Undervoltage Sensing

9.3.2 Open Wire Fault Detection

In the BQ77207 device, each cell input is monitored independently to determine if the input is connected to a cell or not by applying a 50-µA pull down current to ground that is activated for 128 µs every 128 ms. If the device detects that Vn < Vn-1 – V_{OW} V, then a timer is activated. When the timer expires, the COUT and DOUT pins go from an inactive to active state. The timer is reset if the cell input rises above the recovery threshold (V_{OW} + V_{OW_HYS}). To recover both the COUT and DOUT output from active to inactive state, the open wire fault must be cleared (such as the broken connection from the device to the battery needs to be restored), and any other remaining faults (such as existing OVP or UVP faults) need to be cleared as well.

9.3.3 Temperature Fault Detection

In the BQ77207 device, the TS pin is ratiometrically monitored with an internal pull up resistance R_{NTC}. Overtemperature is detected by evaluating the TS input voltage to determine the external resistance falls below a protection resistance, R_{OT_EXT}. If the resistance falls below the programmed OT value, a timer circuit is activated. When the timer expires, the COUT and DOUT pins go from inactive to active state. The timer is reset if the resistance rises above the recovery threshold (R_{OT} + R_{OT_HYS}). If external capacitance is added to the TS pin, it needs to be within the spec limit shown in recommended operating conditions.

注

Texas Instruments does not recommend adding an external capacitor to the TS pin. The capacitance on this pin will affect the TS measurement accuracy if greater than C_{TS}.

9.3.4 Oscillator Health Check

The device can detect if the internal oscillator slows down below the f_{OSC_FAULT} threshold. When this occurs then the COUT and DOUT go from inactive to active state. If the oscillator returns to normal then the fault recovers.

9.3.5 Sense Positive Input for Vx

This is an input to sense each single battery cell voltage. A series resistor and a capacitor across the cell for each input is required for noise filtering and stable voltage monitoring.

9.3.6 Output Drive, COUT and DOUT

These pins serve as the fault signal outputs, and may be ordered in either active HIGH with drive to 6V or active LOW options configured through internal OTP.

The COUT and DOUT will respond per the following table when a fault is detected, if the specific fault is enabled.

表 9-1. Fault Detection vs COUT and DOUT Action

FAULT Detected	COUT	DOUT
Overvoltage	Active	Inactive
Undervoltage	Inactive	Active
Open Wire	Active	Active
Over Temperature	Active	Active
Oscillator Health	Active	Active

9.3.7 The LATCH Function

The device can be enabled to latch the fault signal, which effectively disables the recovery functions of all fault detections. The only way to recover from a fault state when the latch is enabled is a POR of the device.

9.3.8 Supply Input, VDD

This pin is the unregulated input power source for the IC. A series resistor is connected to limit the current, and a capacitor is connected to ground for noise filtering.

9.4 Device Functional Modes

9.4.1 NORMAL Mode

When COUT and DOUT are inactive (no fault detected) the device operates in NORMAL mode and device is monitoring for voltage, open wire and temperature faults.

The COUT and DOUT pins are inactive and if configured:

- Active high is low.
- Active low is being externally pulled up and is an open drain.

9.4.2 FAULT Mode

FAULT mode is entered if the COUT or DOUT pins are activated. The OUT pin will either pull high internally, if configured as active high, or will be pulled low internally, if configured as active low. When COUT and DOUT are deactivated the device returns to NORMAL mode.

9.4.3 Customer Test Mode

Customer Test Mode (CTM) helps to reduce test time for checking the delay timer parameter once the circuit is implemented in the battery pack. To enter CTM, VDD should be set to at least V_{CTM} higher than V7 (see 図 9-3). The delay timer is greater than 10 ms, but considerably shorter than the timer delay in normal operation. To exit Customer Test Mode, remove the VDD to a V7 voltage differential of 10 V so that the decrease in this value automatically causes an exit.

注意

Avoid exceeding any Absolute Maximum Voltages on any pins when placing the part into Customer Test Mode. Also avoid exceeding Absolute Maximum Voltages for the individual cell voltages (VCn–VCn-1) and (V1–VSS). Stressing the pins beyond the rated limits may cause permanent damage to the device.

図 9-3 shows the timing for the Customer Test Mode.

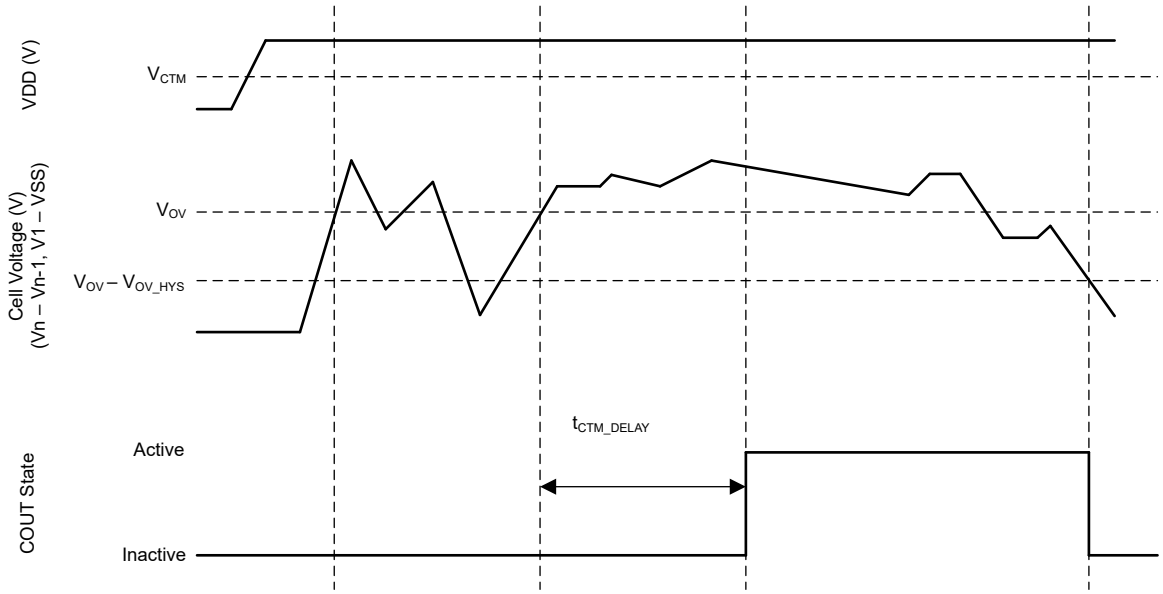


図 9-3. Timing for Customer Test Mode

10 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

Changes to the ranges stated in 表 10-1 will impact the accuracy of the cell measurements.

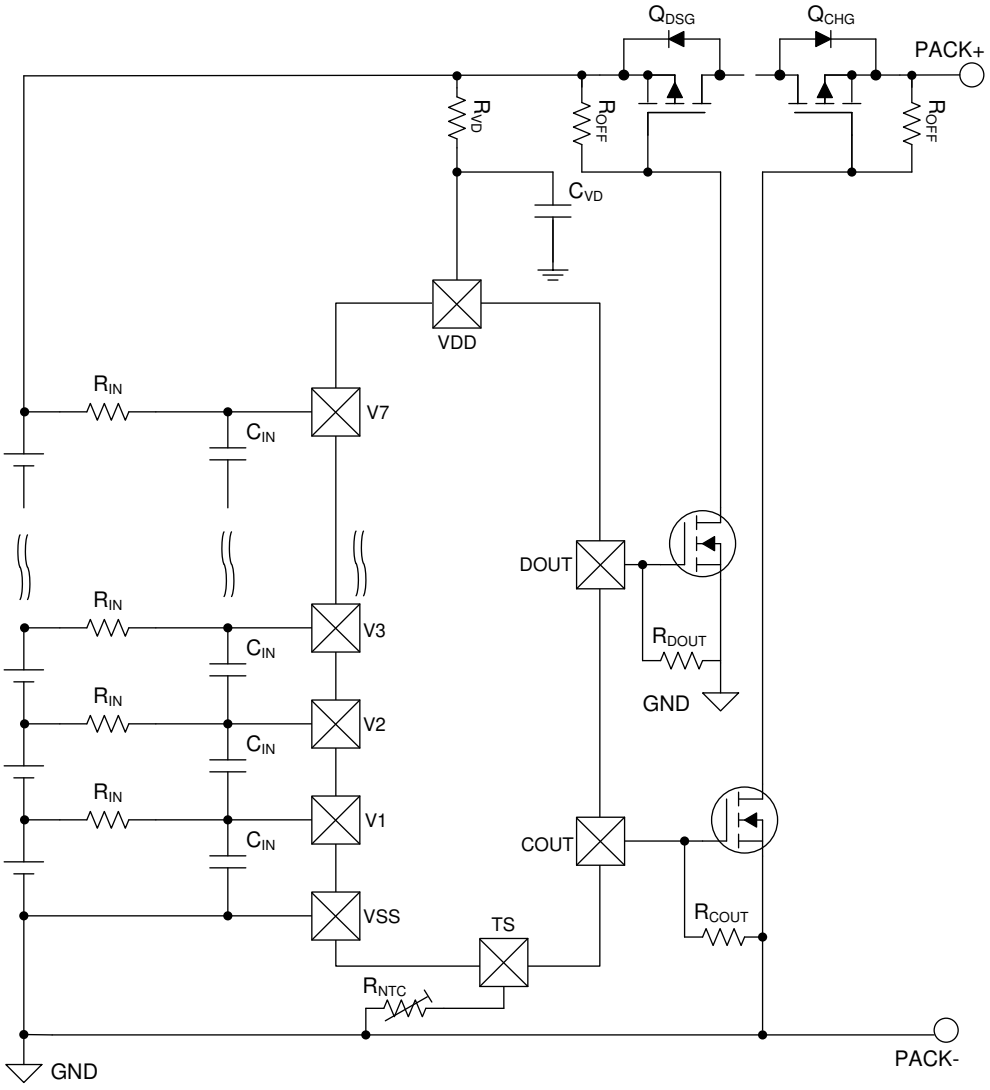


図 10-1. Application Configuration

10.1.1 Design Requirements

Changes to the ranges stated in 表 10-1 will impact the accuracy of the cell measurements. 図 10-1 shows each external component.

表 10-1. Parameters

PARAMETER	EXTERNAL COMPONENT	MIN	NOM	MAX	UNIT
Voltage monitor filter resistance	R_{IN}	900	1000	1100	Ω

表 10-1. Parameters (continued)

PARAMETER	EXTERNAL COMPONENT	MIN	NOM	MAX	UNIT
Voltage monitor filter capacitance	C_{IN}	0.01		0.1	µF
Supply voltage filter resistance	R_{VD}	100	300	1K	Ω
Supply voltage filter capacitance	C_{VD}	0.05	0.1	1	µF

注

The device is calibrated using an R_{IN} value = 1 kΩ. Using a value other than this recommended value changes the accuracy of the cell voltage measurements and V_{OV} trigger level.

10.1.2 Detailed Design Procedure

図 10-2 shows the measurement for current consumption for the product for both VDD and Vx.

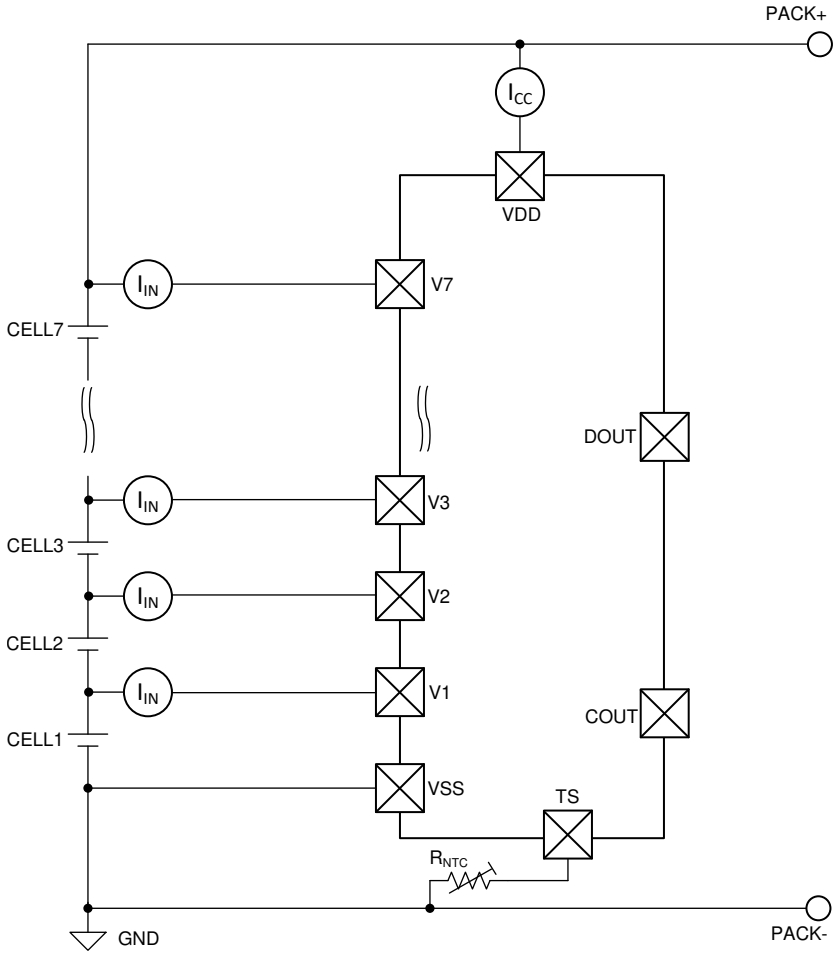


図 10-2. Configuration for IC Current Consumption Test

10.1.2.1 Cell Connection Sequence

The BQ77207 device can be connected to the array of cells in any order without damaging the device.

During cell attachment, the device could detect a fault if the cells are not connected within a fault detection delay period. If this occurs, then COUT and/or DOUT could transition from inactive to active. Both COUT and DOUT can be tied to VSS or VDD to prevent any change in output state during cell attach.

10.2 Systems Example

In this application example, the choice of a FUSE or FETs is required on the COUT and DOUT pins—configured as an active high drive to 6-V outputs.

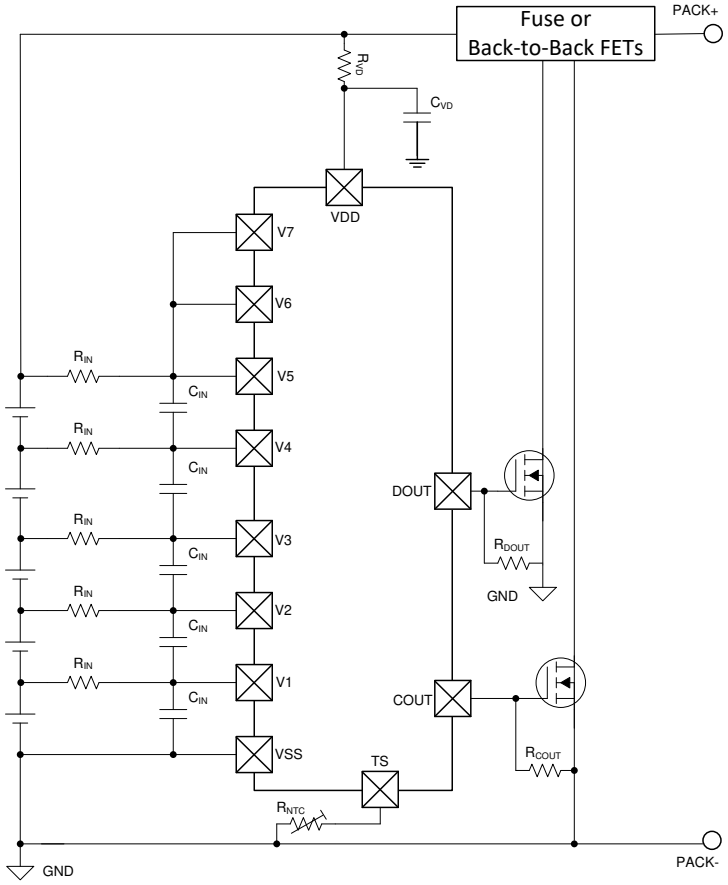


図 10-3. 5-Series Cell Configuration with Active High 6-V Option

When paring with the BQ769x2 or BQ76940 devices, the top cell must be used. For the BQ77207 device to drive the CHG and DSG FETs, the active high 6-V option is preferred. Its COUT and DOUT are controlling two N-CH FETs to jointly control the CHG and DSG FETs with the monitoring device. For such joint architecture, the open-wire feature of the BQ77207 device may be affected if the primary protector or monitor device is actively measuring the cells. Care is needed to ensure the V_{OW} spec of the BQ77207 device is met or to choose a version of the BQ77207 device with open wire disabled. When working with a BQ769x2 device, the LOOPSLOW setting of the BQ769x2 device should be set to 0x11 to ensure the BQ77207 V_{OW} spec is met.

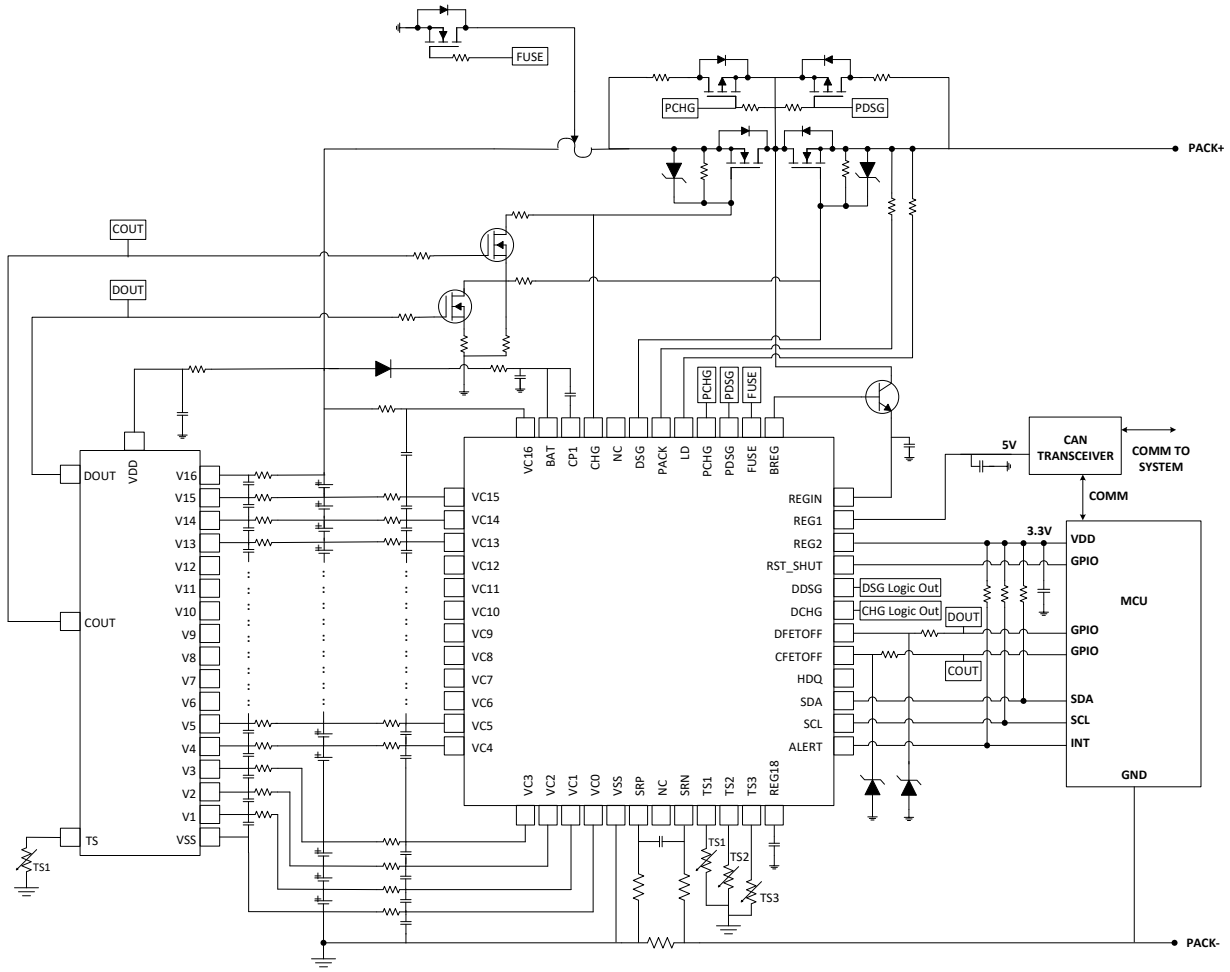


図 10-4. BQ77207 with BQ76952

11 Power Supply Recommendations

The maximum power supply of this device is 38.5 V on VDD.

12 Layout

12.1 Layout Guidelines

- Ensure the RC filters for the Vn and VDD pins are placed as close as possible to the target terminal.
- The VSS pin should be routed to the CELL– terminal.

12.2 Layout Example

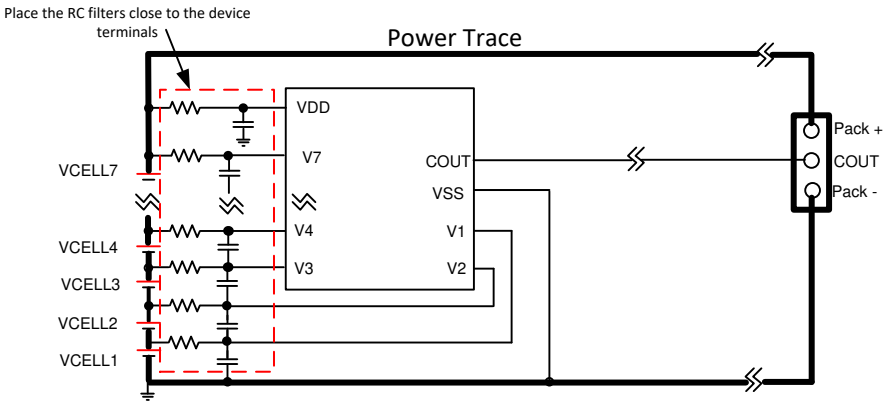


図 12-1. Example Layout

13 Device and Documentation Support

13.1 Third-Party Products Disclaimer

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13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ7720700DSSR	ACTIVE	WSON	DSS	12	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 110	720700	Samples
BQ7720701DSSR	ACTIVE	WSON	DSS	12	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 110	720701	Samples
BQ7720702DSSR	ACTIVE	WSON	DSS	12	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 110	720702	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

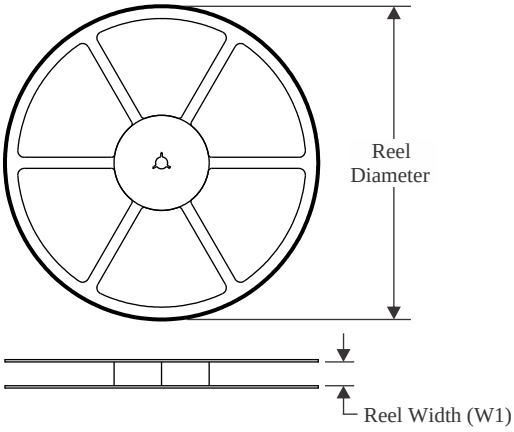
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

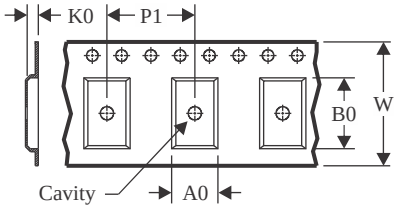
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

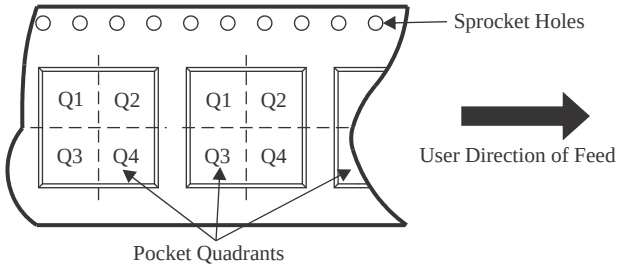


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

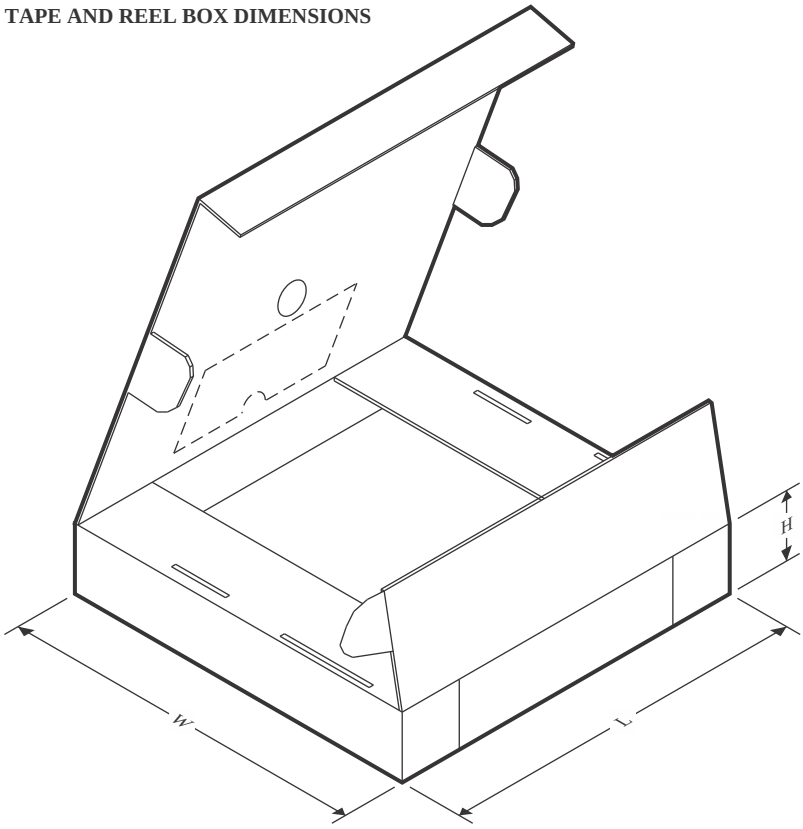
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ7720700DSSR	WSON	DSS	12	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
BQ7720701DSSR	WSON	DSS	12	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
BQ7720702DSSR	WSON	DSS	12	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



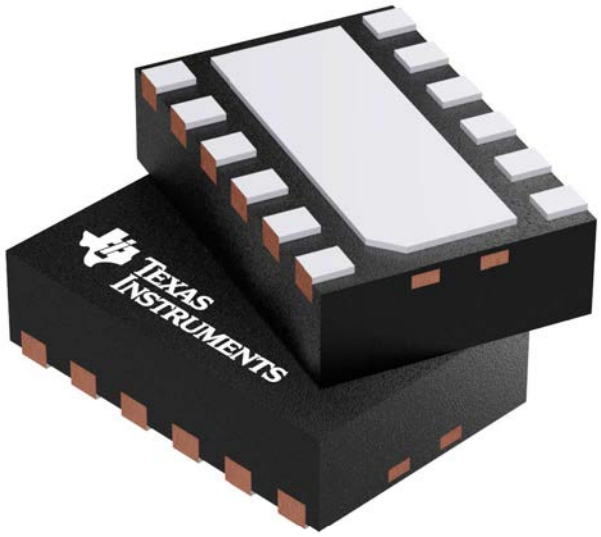
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ7720700DSSR	WSON	DSS	12	3000	210.0	185.0	35.0
BQ7720701DSSR	WSON	DSS	12	3000	210.0	185.0	35.0
BQ7720702DSSR	WSON	DSS	12	3000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

DSS 12 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



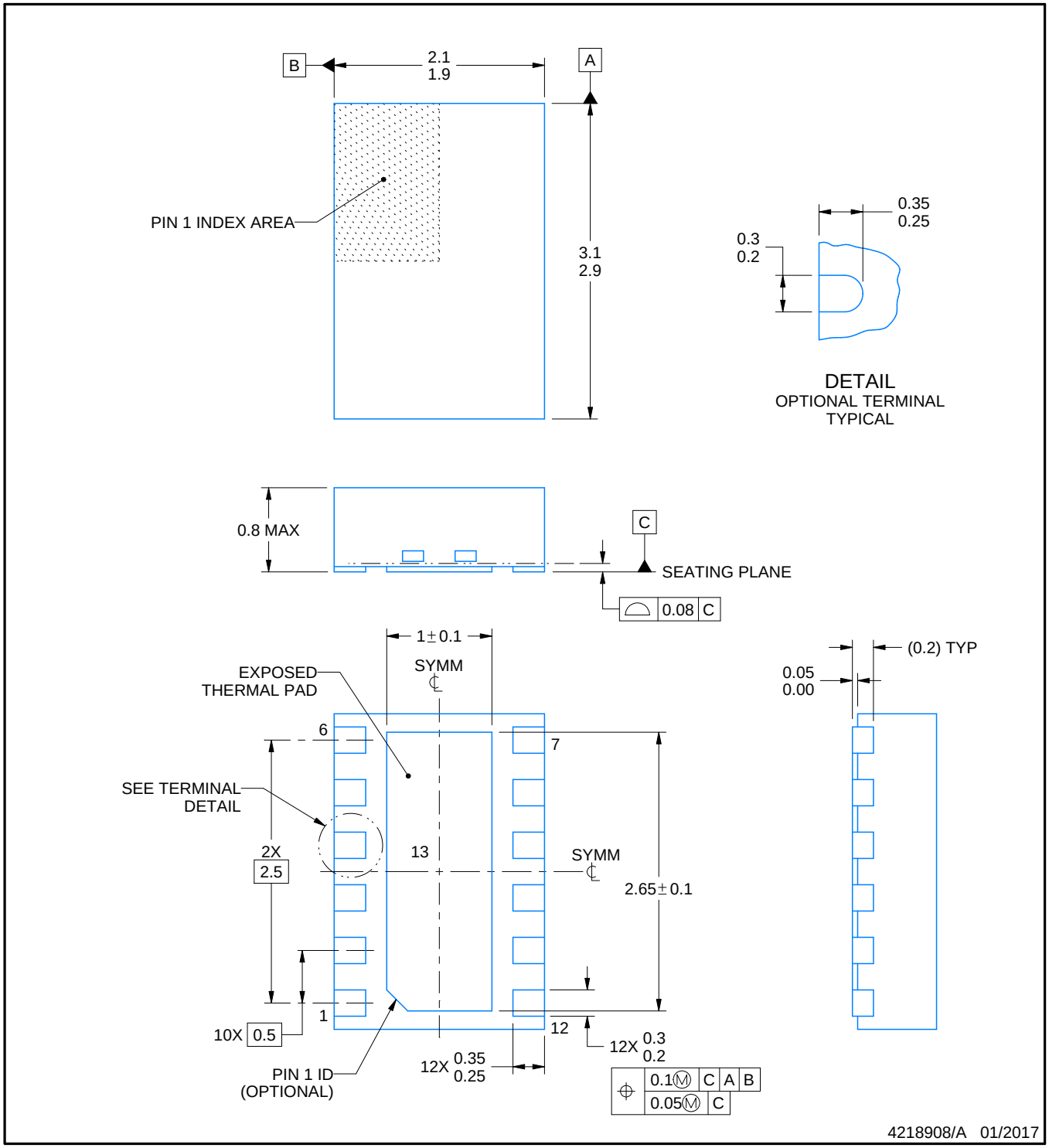
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DSS0012B

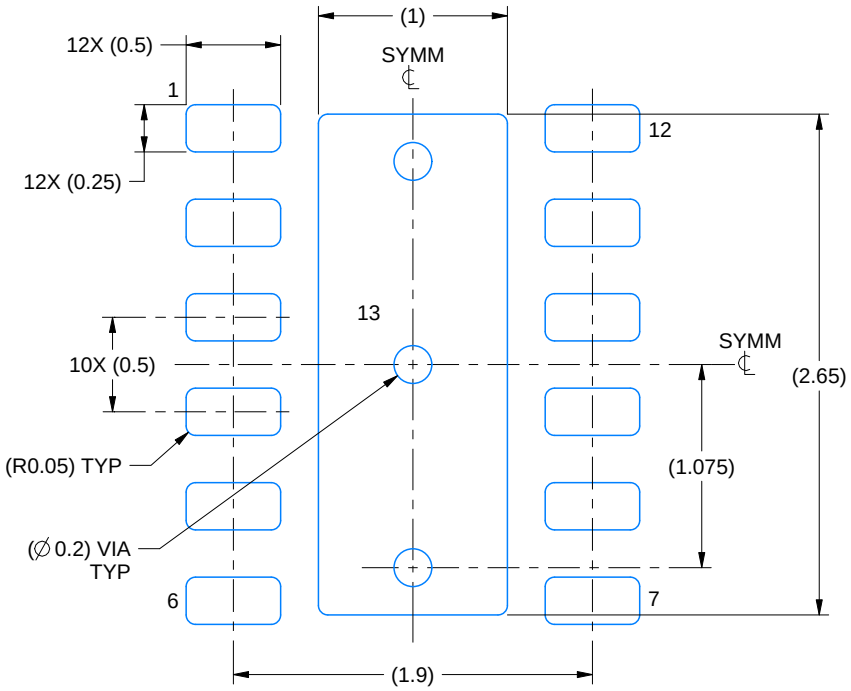
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

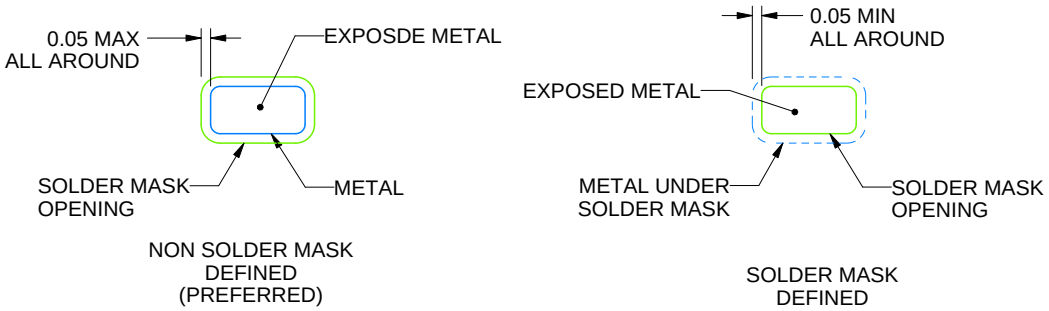


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X



SOLDER MASK DETAILS

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NOTES: (continued)

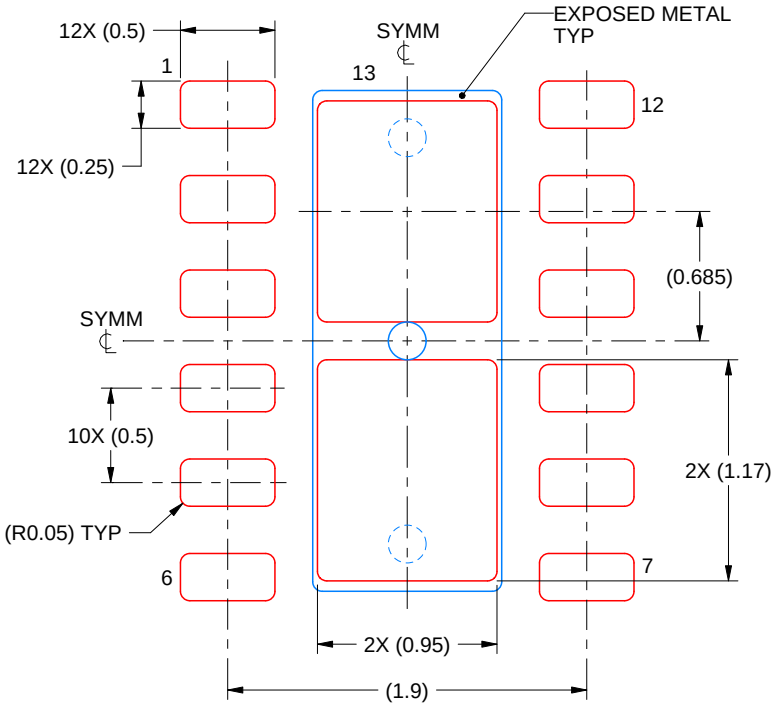
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DSS0012B

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 13:
83% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218908/A 01/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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