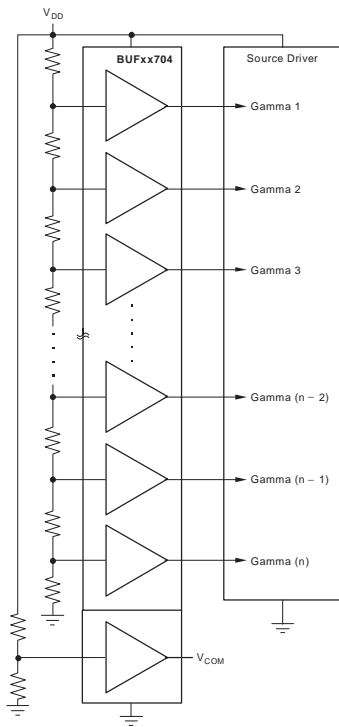# 18-V SUPPLY MULTI-CHANNEL GAMMA CORRECTION BUFFER

FEATURES

- **Wide Supply Range: 4.5 V to 18 V**
- **Gamma Correction Channels: 10, 6, and 4**
- **Integrated V_{COM} Buffer**
- **Excellent Output Current Drive:**
  - **Gamma Channels:**
    > 30 mA at 0.5 V Swing to Rails[1]
  - **V_{COM}:**
    > 100 mA typ at 2 V Swing to Rails[1]
- **Large Capacitive Load Drive Capability**
- **Rail-to-Rail Output**
- **PowerPAD™ Package**
- **Low-Power/Channel: < 500 µA**
- **High ESD Rating: 8 kV HBM, 2 kV CDM, 300 V MM**
- **Specified for –25°C to +85°C**

[1] See Typical Characteristic curves for details.

DESCRIPTION

The BUFxx704 are a series of multi-channel buffers targeted towards gamma correction in high-resolution LCD panels. They are pin-compatible with the existing BUFxx702 and BUFxx703 families and operate at higher supply voltages up to 18 V (19 V absolute max). The higher supply voltage enables faster response times and brighter images in large-screen LCD panels. This is especially important in LCD TV applications.

The number of gamma correction channels required depends on a variety of factors and differs greatly from design to design. Therefore, 10, 6, and 4 channel options are offered. For additional space and cost savings, a V_{COM} channel with > 100mA drive capability is integrated into the BUF11704, BUF07704, and BUF05704.

The BUF11704, BUF07704, BUF06704, and BUF05704 are available in the TSSOP-28, TSSOP-20, TSSOP-16, and TSSOP-14 PowerPAD packages for dramatically increased power dissipation capability. This way, a large number of channels can be handled safely in one package.

A flow-through pinout has been adopted to allow simple PCB routing and maintain the cost-effectiveness of this solution. All inputs and outputs of the BUFxx704 incorporate internal ESD protection circuits that prevent functional failures at voltages up to 8 kV (HBM), 2 kV (CDM), and 300 V (MM).

MODEL	GAMMA CHANNELS	V_{COM} CHANNELS
BUF11704	10	1
BUF07704	6	1
BUF06704	6	0
BUF05704	4	1

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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BUF05704, BUF06704
BUF07704, BUF11704

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ABSOLUTE MAXIMUM RATINGS[1]

Over operating free-air temperature range unless otherwise noted

PARAMETERS	BUFxx704	UNIT
Supply Voltage, V_{DD}[2]	19	V
Input Voltage Range, V_I	$\pm V_{DD}$	
Continuous Total Power Dissipation	See Dissipation Rating Table	
Operating Free-Air Temperature Range, T_A	–25 to 85	°C
Maximum Junction Temperature, T_J	125	°C
Storage Temperature Range, T_{STG}	–65 to 150	°C
Lead Temperature 1.6mm (1/16 inch) from Case for 10s	260	°C
ESD Rating:		
Human Body Model (HBM)	8	kV
Charged-Device Model (CDM)	2	kV
Machine Model (MM)	300	V

[1] Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[2] All voltage values are with respect to GND.

ORDERING INFORMATION[1]

PRODUCT	PACKAGE-LEAD	PACKAGE MARKING
BUF05704	TSSOP-14	BUF05704
BUF06704	TSSOP-16	BUF06704
BUF07704	TSSOP-20	BUF07704
BUF11704	TSSOP-28	BUF11704

[1] For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.
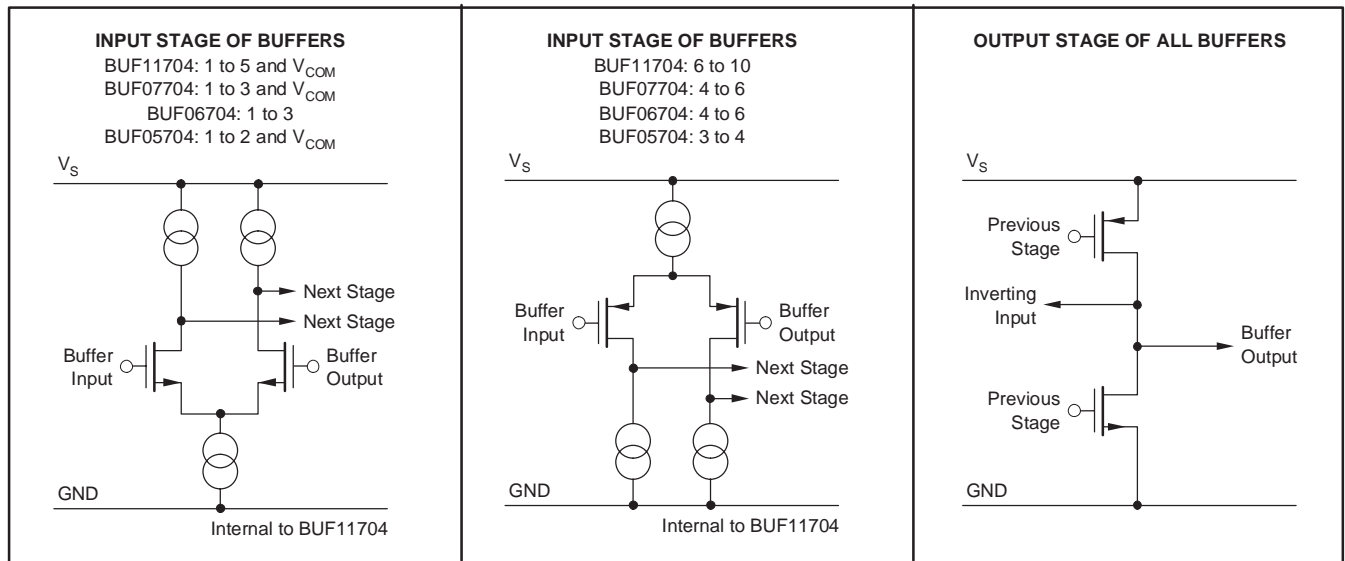
DISSIPATION RATING TABLE

PACKAGE TYPE	PACKAGE DESIGNATOR	θ_{JC}[1] (°C/W)	θ_{JA}[1] (°C/W)	$T_A \leq 25°C$ POWER RATING
TSSOP-28	PWP (28)	0.72	27.9	3.58 W
TSSOP-20	PWP (20)	1.40	32.63	3.06 W
TSSOP-16	PWP (16)	2.07	36.51	2.74
TSSOP-14	PWP (14)	2.07	37.47	2.67

[1] PowerPAD attached to PCB, 0 lfm airflow, and 76mm x 76mm copper area.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage, V_{DD}	7		18	V
Operating Free-Air Temperature, T_A	–25		+85	°C

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BUF05704, BUF06704
BUF07704, BUF11704

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EQUIVALENT SCHEMATICS OF INPUTS AND OUTPUTS

INPUT STAGE OF BUFFERS	INPUT STAGE OF BUFFERS	OUTPUT STAGE OF ALL BUFFERS
BUF11704: 1 to 5 and V_{COM} BUF07704: 1 to 3 and V_{COM} BUF06704: 1 to 3 BUF05704: 1 to 2 and V_{COM}	BUF11704: 6 to 10 BUF07704: 4 to 6 BUF06704: 4 to 6 BUF05704: 3 to 4	

ELECTRICAL CHARACTERISTICS: BUFxx704

Over operating free-air temperature range, V_{DD} = 18 V, T_A = 25°C, unless otherwise noted.

	PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	Gamma buffers	V_I = 9V	25°C		−1	20	mV
				Full range(1)			20	
		V_{COM}		25°C		−1	30	
				Full range(1)			30	
I_{IB}	Input bias current		V_I = V_{DD}/2	25°C		1		pA
				Full range(1)		200		
PSRR	Power-Supply Rejection Ratio		V_{DD} = 4.5 V to 19 V	25°C	62	80		dB
				Full range(1)	60			
	Buffer gain		V_I = 5 V	25°C		0.9995		V/V
BW_3dB	3dB bandwidth	Gamma buffers V_{COM} buffer	C_L = 100 pF, R_L = 2 kΩ	25°C		1 0.6		MHz
SR	Slew rate	Gamma buffers V_{COM} buffer	C_L = 100 pF, R_L = 2 kΩ V_{IN} = 2 V to 16 V	25°C		1.6 4.6		V/µs
	Crosstalk		V_{IP-P} = 6 V, f = 1 kHz	25°C		85		dB

(1) Full range is −25°C to 85°C.

ELECTRICAL CHARACTERISTICS: BUF11704

Over operating free-air temperature range, V_{DD} = 18 V, T_A = 25°C, unless otherwise noted.

PARAMETER			TEST CONDITIONS	T_A[(1)]	MIN	TYP	MAX	UNIT
I_{DD}	Supply current	ALL	V_O = V_{DD}/2 No Load	25°C		5	9.0	mA
				Full range			9.0	
Common-mode input range		Buffers 1-5		25°C	1		V_{DD}	V
		Buffers 6-10			GND		V_{DD} − 1	
		V_{COM} buffer			1		V_{DD}	
	Load regulation	V_{COM} buffer sinking	I_O = 1 mA to 100 mA, V_{IN} = 2 V	25°C		1	5	mV/mA
				Full range			5	
		V_{COM} buffer sourcing	I_O = −1 mA to −100 mA V_{IN} = 16 V	25°C		1	5	
				Full range			5	
		Buffers 1-10 sinking	I_O = 1 mA to 10 mA V_{IN} = 1 V	25°C		1	5	
				Full range			5	
		Buffers 1-10 sourcing	I_O = −1 mA to −10 mA V_{IN} = 17 V	25°C		1	5	
				Full range			5	
V_{OH1-5}	High-level output voltage	Buffers 1-5	V_{IN} = 18 V I_{SOURCE} = 10 mA	25°C	17.85	17.9		V
V_{OH6-10}		Buffers 6-10	V_{IN} = 17 V I_{SINK} = 10 mA	25°C		17	17.15	V
			V_{IN} = 17 V I_{SOURCE} = 10 mA		16.85	17		
V_{OL1-5}	Low-level output voltage	Buffers 1-5	V_{IN} = 1 V I_{SINK} = 10 mA	25°C		1.0	1.15	V
			V_{IN} = 1 V I_{SOURCE} = 10 mA		0.85	1.0		
V_{OL6-10}		Buffers 6-10	V_{IN} = 0 V I_{SINK} = 10 mA	25°C		0	0.15	V
V_{OHCOM}	High-level output voltage	V_{COM} buffer	V_{IN} = 16 V I_{SINK} = 100 mA	25°C		16	16.15	V
			V_{IN} = 16 V I_{SOURCE} = 100 mA		15.85	16		
V_{OLCOM}	Low-level output voltage	V_{COM} buffer	V_{IN} = 2 V I_{SINK} = 100 mA	25°C		2	2.15	V
			V_{IN} = 2 V I_{SOURCE} = 100 mA		1.85	2		

(1) Full range is −25°C to 85°C.

ELECTRICAL CHARACTERISTICS: BUF07704

Over operating free-air temperature range, V_{DD} = 18 V, T_A = 25°C, unless otherwise noted.

PARAMETER			TEST CONDITIONS	T_A[1]	MIN	TYP	MAX	UNIT
I_{DD}	Supply current	ALL	$V_O = V_{DD}/2$ No Load	25°C		5	7.5	mA
				Full range			7.5	
Common-mode input range		Buffers 1-3		25°C	1		V_{DD}	V
		Buffers 4-6			GND		V_{DD} − 1	
		V_{COM} buffer			1		V_{DD}	
Load regulation		V_{COM} buffer sinking	I_O = 1 mA to 100 mA V_{IN} = 2 V	25°C		1	5	mV/mA
				Full range			5	
		V_{COM} buffer sourcing	I_O = −1 mA to −100 mA V_{IN} = 16 V	25°C		1	5	
				Full range			5	
		Buffers 1-6 sinking	I_O = 1 mA to 10 mA V_{IN} = 1 V	25°C		1	5	
				Full range			5	
		Buffers 1-6 sourcing	I_O = −1 mA to −10 mA V_{IN} = 17 V	25°C		1	5	
				Full range			5	
V_{OH1-3}	High-level output voltage	Buffers 1-3	V_{IN} = 18 V I_{SOURCE} = 10 mA	25°C	17.85	17.9		V
V_{OH4-6}		Buffers 4-6	V_{IN} = 17 V I_{SINK} = 10 mA	25°C		17	17.15	V
			V_{IN} = 17 V I_{SOURCE} = 10 mA		16.85	17		
V_{OL1-3}	Low-level output voltage	Buffers 1-3	V_{IN} = 1 V I_{SINK} = 10 mA	25°C		1.0	1.15	V
			V_{IN} = 1 V I_{SOURCE} = 10 mA		0.85	1.0		
V_{OL4-6}		Buffers 4-6	V_{IN} = 0 V I_{SINK} = 10 mA	25°C		0	0.15	V
V_{OHCOM}	High-level output voltage	V_{COM} buffer	V_{IN} = 16 V I_{SINK} = 100 mA	25°C		16	16.15	V
			V_{IN} = 16 V I_{SOURCE} = 100 mA		15.85	16		
V_{OLCOM}	Low-level output voltage	V_{COM} buffer	V_{IN} = 2 V I_{SINK} = 100 mA	25°C		2	2.15	V
			V_{IN} = 2 V I_{SOURCE} = 100 mA		1.85	2		

[1] Full range is −25°C to 85°C.

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BUF07704, BUF11704
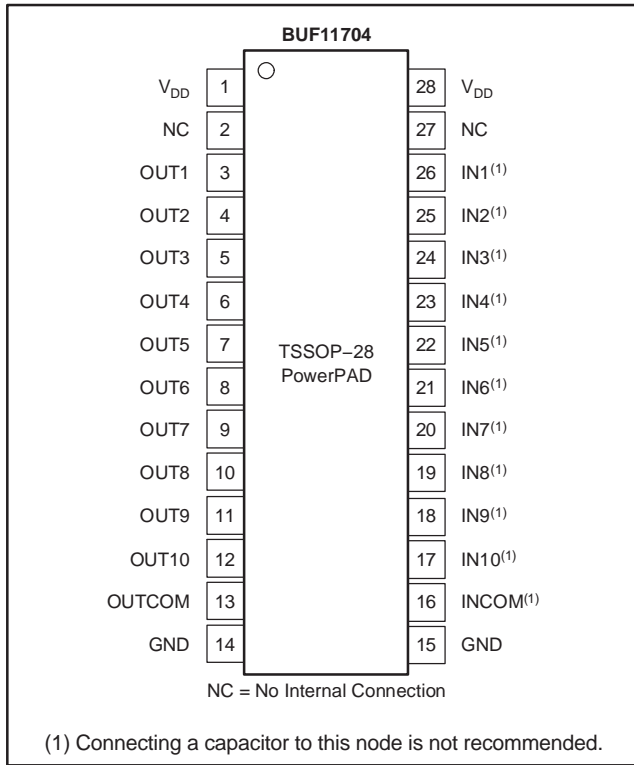
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ELECTRICAL CHARACTERISTICS: BUF06704

Over operating free-air temperature range, V_{DD} = 18 V, T_A = 25°C, unless otherwise noted.

PARAMETER			TEST CONDITIONS	T_A(1)	MIN	TYP	MAX	UNIT
I_{DD}	Supply current	ALL	$V_O = V_{DD}/2$ No Load	25°C		5	7.5	mA
				Full range			7.5	
Common-mode input range		Buffers 1-3		25°C	1		V_{DD}	V
		Buffers 4-6			GND		$V_{DD} - 1$	
Load regulation		Buffers 1-6 sinking	I_O = 1 mA to 10 mA V_{IN} = 1 V	25°C		1	5	mV/mA
				Full range			5	
		Buffers 1-6 sourcing	I_O = −1 mA to −10 mA V_{IN} = 17 V	25°C		1	5	
				Full range			5	
V_{OH1-3}	High-level output voltage	Buffers 1-3	V_{IN} = 18 V I_{SOURCE} = 10 mA	25°C	17.85	17.9		V
V_{OH4-6}		Buffers 4-6	V_{IN} = 17 V I_{SINK} = 10 mA	25°C		17	17.15	V
			V_{IN} = 17 V I_{SOURCE} = 10 mA		16.85	17		
V_{OL1-3}	Low-level output voltage	Buffers 1-3	V_{IN} = 1 V I_{SINK} = 10 mA	25°C		1.0	1.15	V
			V_{IN} = 1 V I_{SOURCE} = 10 mA		0.85	1.0		
V_{OL4-6}		Buffers 4-6	V_{IN} = 0 V I_{SINK} = 10 mA	25°C		0	0.15	V

(1) Full range is −25°C to 85°C.

ELECTRICAL CHARACTERISTICS: BUF05704

Over operating free-air temperature range, V_{DD} = 18 V, T_A = 25°C, unless otherwise noted.

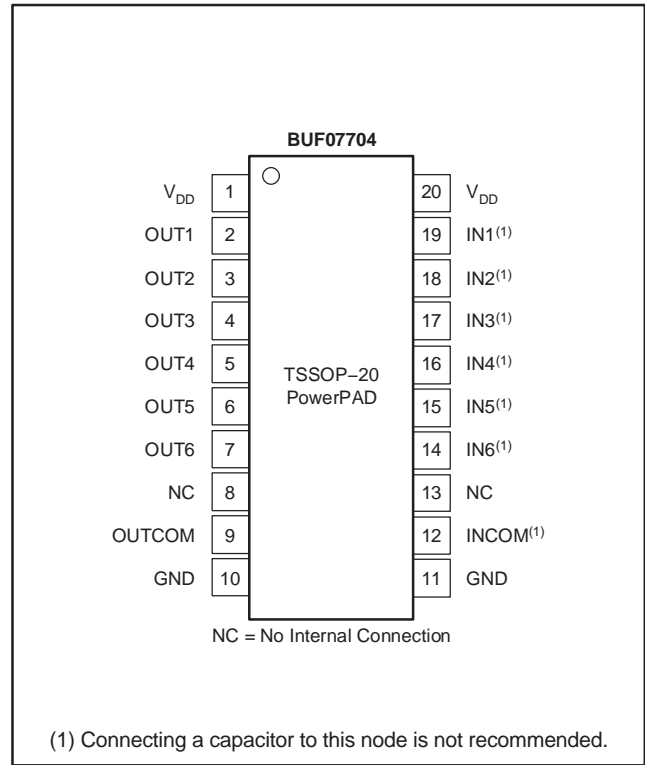| PARAMETER			TEST CONDITIONS	T_A[(1)]	MIN	TYP	MAX	UNIT
I_{DD}	Supply current	ALL	$V_O = V_{DD}/2$ No Load	25°C		5	7.5	mA
				Full range			7.5	
Common-mode input range		Buffers 1-2		25°C	1		V_{DD}	V
		Buffers 3-4			GND		$V_{DD} - 1$	
		V_{COM} buffer			1		V_{DD}	
	Load regulation	V_{COM} buffer sinking	I_O = 1 mA to 100 mA V_{IN} = 2 V	25°C		1	5	mV/mA
				Full range			5	
		V_{COM} buffer sourcing	I_O = −1 mA to −100 mA V_{IN} = 16 V	25°C		1	5	
				Full range			5	
		Buffers 1-4 sinking	I_O = 1 mA to 10 mA V_{IN} = 1 V	25°C		1	5	
				Full range			5	
		Buffers 1-4 sourcing	I_O = −1 mA to −10 mA V_{IN} = 17 V	25°C		1	5	
				Full range			5	
V_{OH1-3}	High-level output voltage	Buffers 1-2	V_{IN} = 18 V I_{SOURCE} = 10 mA	25°C	17.85	17.9		V
V_{OH4-6}		Buffers 3-4	V_{IN} = 17 V I_{SINK} = 10 mA	25°C		17	17.15	V
			V_{IN} = 17 V I_{SOURCE} = 10 mA		16.85	17		
V_{OL1-3}	Low-level output voltage	Buffers 1-2	V_{IN} = 1 V I_{SINK} = 10 mA	25°C		1.0	1.15	V
			V_{IN} = 1 V I_{SOURCE} = 10 mA		0.85	1.0		
V_{OL4-6}		Buffers 3-4	V_{IN} = 0 V I_{SINK} = 10 mA	25°C		0	0.15	V
V_{OHCOM}	High-level output voltage	V_{COM} buffer	V_{IN} = 16 V I_{SINK} = 100 mA	25°C		16	16.15	V
			V_{IN} = 16 V I_{SOURCE} = 100 mA		15.85	16		
V_{OLCOM}	Low-level output voltage	V_{COM} buffer	V_{IN} = 2 V I_{SINK} = 100 mA	25°C		2	2.15	V
			V_{IN} = 2 V I_{SOURCE} = 100 mA		1.85	2		

(1) Full range is −25°C to 85°C.

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BUF11704 Pin Configuration

V_{DD}	1	
NC	2	
OUT1	3	
OUT2	4	
OUT3	5	
OUT4	6	
OUT5	7	
OUT6	8	
OUT7	9	
OUT8	10	
OUT9	11	
OUT10	12	
OUTCOM	13	
GND	14	

BUF11704

TSSOP–28
PowerPAD

28	V_{DD}	
27	NC	
26	IN1[1]	
25	IN2[1]	
24	IN3[1]	
23	IN4[1]	
22	IN5[1]	
21	IN6[1]	
20	IN7[1]	
19	IN8[1]	
18	IN9[1]	
17	IN10[1]	
16	INCOM[1]	
15	GND	

NC = No Internal Connection

(1) Connecting a capacitor to this node is not recommended.

BUF07704 Pin Configuration

BUF07704

V_{DD}	1		20	V_{DD}
OUT1	2		19	IN1[1]
OUT2	3		18	IN2[1]
OUT3	4		17	IN3[1]
OUT4	5	TSSOP–20 PowerPAD	16	IN4[1]
OUT5	6		15	IN5[1]
OUT6	7		14	IN6[1]
NC	8		13	NC
OUTCOM	9		12	INCOM[1]
GND	10		11	GND

NC = No Internal Connection

(1) Connecting a capacitor to this node is not recommended.

BUF06704 Pin Configuration

BUF06704

V_{DD}	1		16	V_{DD}
OUT1	2		15	IN1[1]
OUT2	3		14	IN2[1]
OUT3	4	TSSOP–16 PowerPAD	13	IN3[1]
OUT4	5		12	IN4[1]
OUT5	6		11	IN5[1]
OUT6	7		10	IN6[1]
GND	8		9	GND

(1) Connecting a capacitor to this node is not recommended.

BUF05704 Pin Configuration

BUF05704

V_{DD}	1		14	V_{DD}
OUT1	2		13	IN1[1]
OUT2	3		12	IN2[1]
OUT3	4	TSSOP–14 PowerPAD	11	IN3[1]
OUT4	5		10	IN4[1]
OUTCOM	6		9	INCOM[1]
GND	7		8	GND

(1) Connecting a capacitor to this node is not recommended.

TYPICAL CHARACTERISTICS

DC CURVES

INPUT OFFSET VOLTAGE vs INPUT VOLTAGE

Figure 1

INPUT OFFSET VOLTAGE vs INPUT VOLTAGE

Figure 2

INPUT OFFSET VOLTAGE vs INPUT VOLTAGE

Figure 3

INPUT BIAS CURRENT vs FREE−AIR TEMPERATURE

Figure 4

OUTPUT VOLTAGE vs OUTPUT CURRENT

Figure 5

HIGH−LEVEL OUTPUT VOLTAGE vs
HIGH−LEVEL OUTPUT CURRENT

Figure 6

BUF05704, BUF06704
BUF07704, BUF11704

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TYPICAL CHARACTERISTICS

DC CURVES (continued)

OUTPUT VOLTAGE vs OUTPUT CURRENT

V_{SUPPLY} = 18 V
BUF11704: Channels 6–10
BUF07704: Channels 4–6
BUF06704: Channels 4–6
BUF05704: Channels 3–4

V_O – Output Voltage – V

I_O – Output Current – mA

−10°C
25°C
85°C

Figure 7

LOW–LEVEL OUTPUT VOLTAGE vs
LOW–LEVEL OUTPUT CURRENT (Detailed View)

BUF11704: Channels 6–10
BUF07704: Channels 4–6
BUF06704: Channels 4–6
BUF05704: Channels 3–4

V_{OL} – Low-Level Output Voltage – V

I_{OL} – Low-Level Output Current – mA

85°C
25°C
−10°C

Figure 8

OUTPUT VOLTAGE vs OUTPUT CURRENT

V_{SUPPLY} = 18 V
V_{COM} Buffer

85°C   25°C   −10°C

V_O – Output Voltage – V

I_O – Output Current – mA

Figure 9

SUPPLY CURRENT vs SUPPLY VOLTAGE

Supply Current – mA

Supply Voltage – V

Figure 10

SUPPLY CURRENT vs FREE–AIR TEMPERATURE

V_S = 18 V

I_Q – Supply Current – mA

T_A – Free-Air Temperature – °C

Figure 11

INPUT BIAS CURRENT vs INPUT VOLTAGE

I_B – Input Bias Current – pA

V_{IN} – Input Voltage – V

Figure 12

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TYPICAL CHARACTERISTICS

AC CURVES

POWER–SUPPLY REJECTION RATIO vs FREQUENCY

V_{DD} = 10 V
R_L = 2 k
C_L = 100 pF

Gamma Channels

V_{COM} Buffer

f – Frequency – Hz

PSRR – Power–Supply Rejection Ratio – dB

Figure 13

CROSSTALK vs FREQUENCY

V_{SUPPLY} = 10 V
V_{IN} = 1 V_{PP}

f – Frequency – Hz

CMRR – Common-Mode Rejection Ratio – dB

Figure 14

BUF05704, BUF06704
BUF07704, BUF11704

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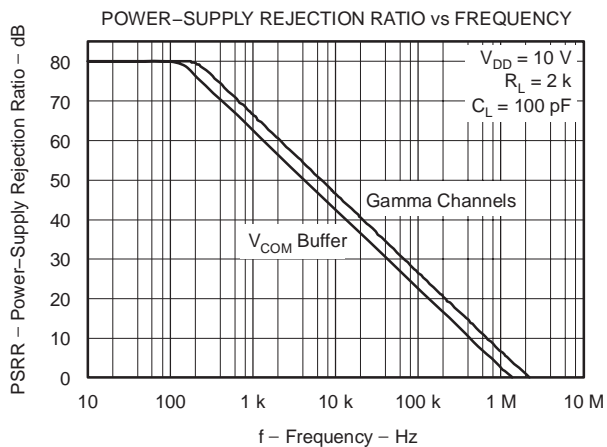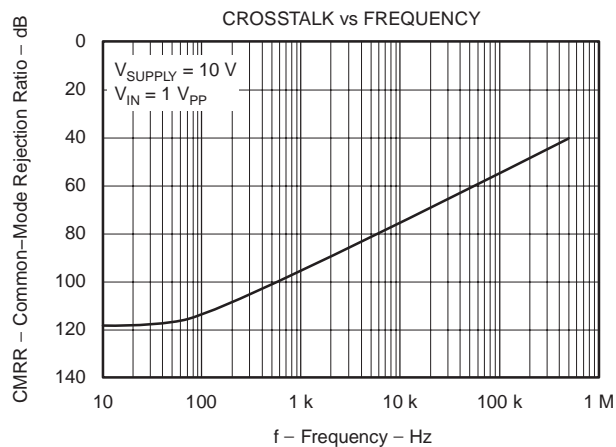
TYPICAL CHARACTERISTICS

SMALL- AND LARGE-SIGNAL WAVEFORM CURVES

SMALL–SIGNAL WAVEFORM

$R_{LOAD} = 2\ k\Omega$
$C_{LOAD} = 100\ pF$
BUF11704: Channels 1–5
BUF07704: Channels 1–3
BUF06704: Channels 1–3
BUF05704: Channels 1–2

50 mV/div

t – Time – 500 ns/div

Figure 15

SMALL–SIGNAL WAVEFORM

$R_{LOAD} = 2\ k\Omega$
$C_{LOAD} = 100\ pF$
BUF11704: Channels 6–10
BUF07704: Channels 4–6
BUF06704: Channels 4–6
BUF05704: Channels 3–4

50 mV/div

t – Time – 500 ns/div

Figure 16

SMALL–SIGNAL WAVEFORM—V_{COM} BUFFER

$R_{LOAD} = 2\ k\Omega$
$C_{LOAD} = 100\ pF$
V_{COM} Buffer

50 mV/div

t – Time – 500 ns/div

Figure 17

LARGE–SIGNAL WAVEFORM

$R_{LOAD} = 2\ k\Omega$
$C_{LOAD} = 100\ pF$
$V_{DD} = 15\ V$

BUF11704: Channels 1–5
BUF07704: Channels 1–3
BUF06704: Channels 1–3
BUF05704: Channels 1–2

3 V/div

t – Time – 4 µs/div

Figure 18

LARGE–SIGNAL WAVEFORM

$R_{LOAD} = 2\ k\Omega$
$C_{LOAD} = 100\ pF$
$V_{DD} = 15\ V$

BUF11704: Channels 6–10
BUF07704: Channels 4–6
BUF06704: Channels 4–6
BUF05704: Channels 3–4

3 V/div

t – Time – 4 µs/div

Figure 19

LARGE–SIGNAL WAVEFORM—V_{COM} BUFFER

$R_{LOAD} = 2\ k\Omega$
$C_{LOAD} = 100\ pF$
V_{COM} Buffer
$V_{DD} = 15\ V$

3 V/div

t – Time – 4 µs/div

Figure 20

APPLICATION INFORMATION

The requirements on the number of gamma correction channels vary greatly from panel to panel. Therefore, the BUFxx704 series of gamma correction buffers offer different channel combinations. The BUF11704 offers 10 gamma channels plus one V_{COM} channel, whereas the BUF07704 provides six gamma channels plus one V_{COM}. The V_{COM} channel on both models can be used to drive the V_{COM} node on the LCD panel.

Gamma correction voltages are often generated using a simple resistor ladder, as shown in Figure 21. The BUFxx704 buffers the various nodes on the gamma correction resistor ladder. The low output impedance of the BUFxx704 forces the external gamma correction voltage on the respective reference node of the LCD source driver. Figure 21 shows an example of the BUFxx704 in a typical block diagram driving an LCD source driver with 10- or 6-channel gamma correction reference inputs.

(1) Optional— Increases stability.
(2) Optional capacitor.
(3) n = max number of gamma channels on respective BUFxx704.
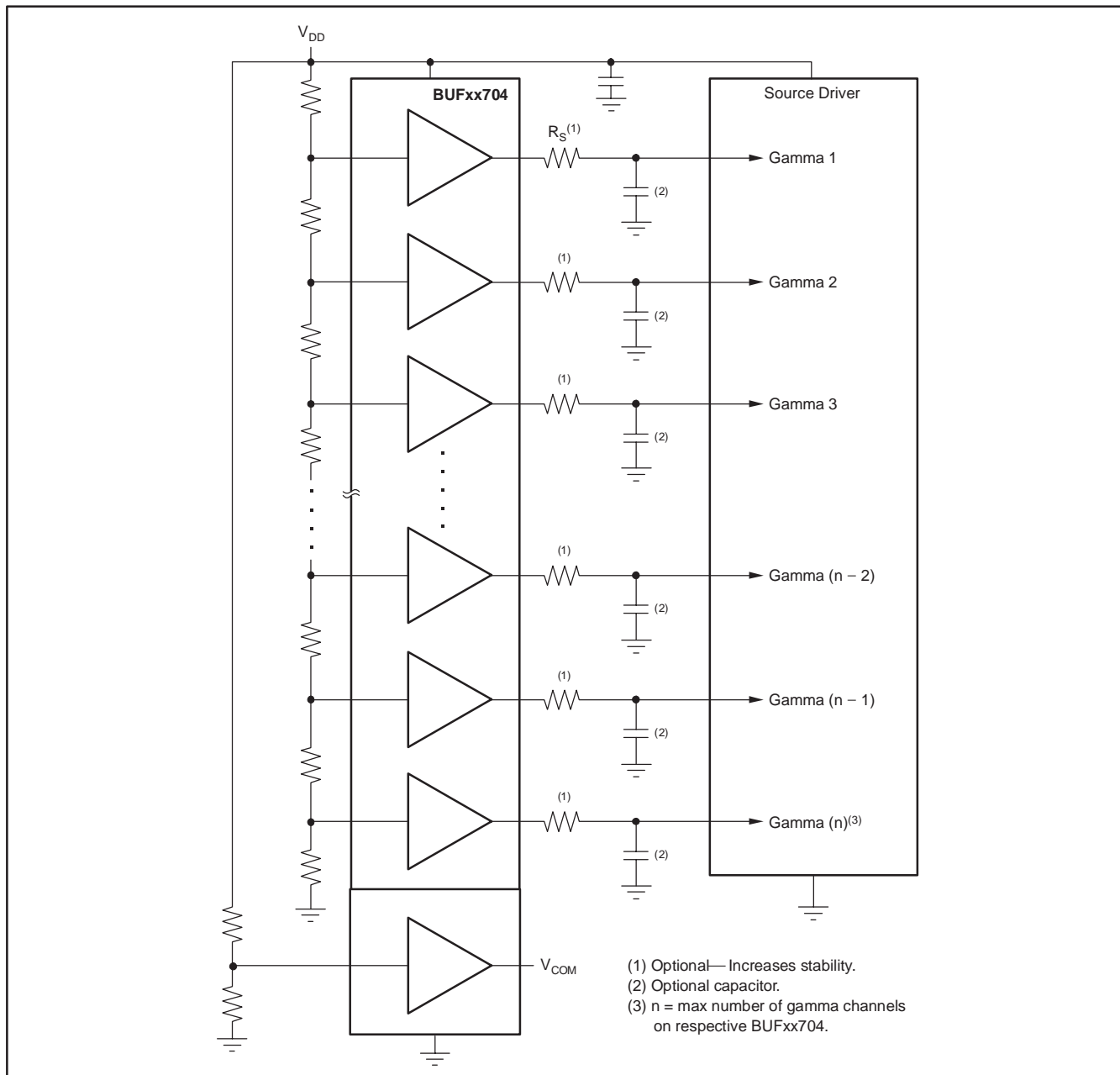
Figure 21. LCD Source Driver Typical Block Diagram

BUF05704, BUF06704
BUF07704, BUF11704

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ESD RATINGS

The BUFxx704 has excellent ESD performance: 8 kV HBM; 2 kV CDM; and 300 V MM. These ESD ratings allow for increased manufacturability, fewer production failures, and higher reliability.

INPUT VOLTAGE RANGE GAMMA BUFFERS

Figure 22 shows a typical gamma correction curve with 10 gamma correction reference points (GMA1 through GMA10). As can be seen from this curve, the voltage requirements for each buffer vary greatly. The swing capability of the input stages of the various buffers is carefully matched to the application. Using the example of the BUF11704 with 10 gamma correction channels, buffers 1 to 5 have input stages that include V_{DD}, but will only swing within 1 V to GND. Buffers 1 through 5 have only a single NMOS input stage. Buffers 6 through 10 have only a single PMOS input stage. The input range of the PMOS input stage includes GND.
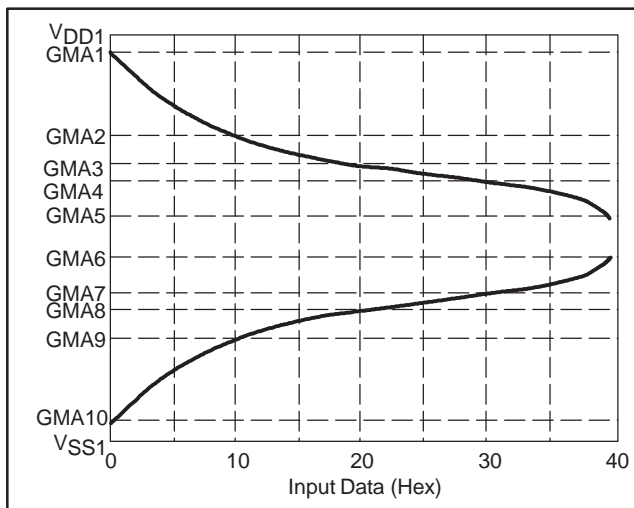
Figure 22. Gamma Correction Curve

OUTPUT VOLTAGE SWING GAMMA BUFFERS

The output stages have been designed to match the characteristic of the input stage. Once again, using the example of the BUF11704, this means that the output stage of buffers 1 to 5 swing very close to V_{DD}, typically V_{CC} – 100 mV at 10 mA; its ability to swing to GND is limited. Buffers 6 through 10 swing closer to GND than V_{DD}. Buffers 6 to 10 are designed to swing very close to GND; typically, GND + 100 mV at a 10 mA load current. See the *Typical Characteristics* for more details. This approach significantly reduces the silicon area and cost of the whole solution. However, due to

this architecture, the correct buffer needs to be connected to the correct gamma correction voltage. Connect buffer 1 to the gamma voltage closest to V_{DD}, and buffers 2 through 5 to the following voltages. Buffer 10 should be connected to the gamma correction voltage closest to GND (or the negative rail), and buffers 9 through 6 to the following higher voltages.

COMMON BUFFER (V_{COM})

The common buffer output of the BUFxx704 has a greater output drive capability than the gamma buffers to meet the heavier current demands of driving the common node of the LCD panel. The common buffer output was also designed to drive heavier capacitive loads. Excellent output swing is possible with high currents (> 100 mA), as shown in Figure 23.
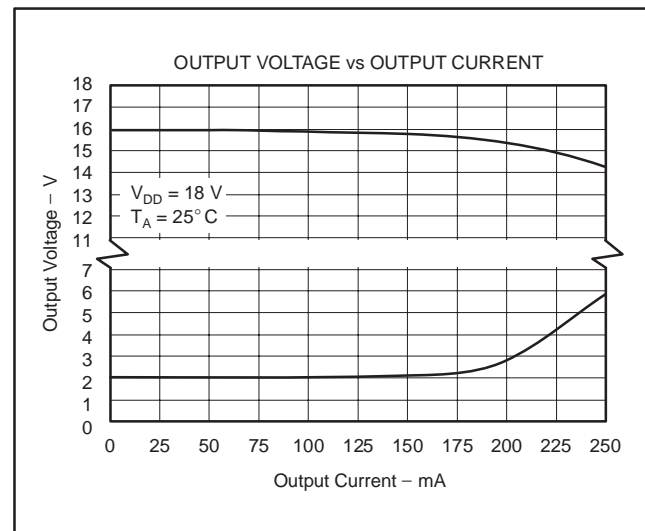
Figure 23. V_{COM} Output Drive Capability

CAPACITIVE LOAD DRIVE

The BUFxx704 has been designed to be able to sink/source large dc currents. Its output stage has been designed to deliver output current transients with little disturbance of the output voltage. However, there are times when very fast current pulses are required. Therefore, in LCD source driver buffer applications, it is quite normal for capacitors to be placed at the outputs of the reference buffers. These capacitors improve the transient load regulation and will typically vary from 100 pF and more. The BUFxx704 gamma buffers were designed to drive capacitances in excess of 100 pF. The output is able to swing within 150 mV of the rails on 10 mA of output current; see Figure 24.
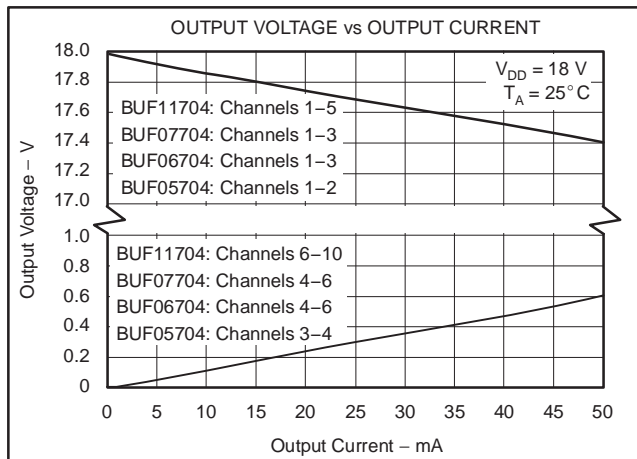
Figure 24. Gamma Buffer Drive Capability

APPLICATIONS WITH >10 GAMMA CHANNELS

When a greater number of gamma correction channels are required, two or more BUFxx704 devices can be used in parallel, as shown in Figure 25. This capability provides a cost-effective way of creating more reference voltages over the use of quad-channel op amps or buffers. The suggested configuration in Figure 25 simplifies layout. The various different channel versions provide a high degree of flexibility and also minimize total cost and space.
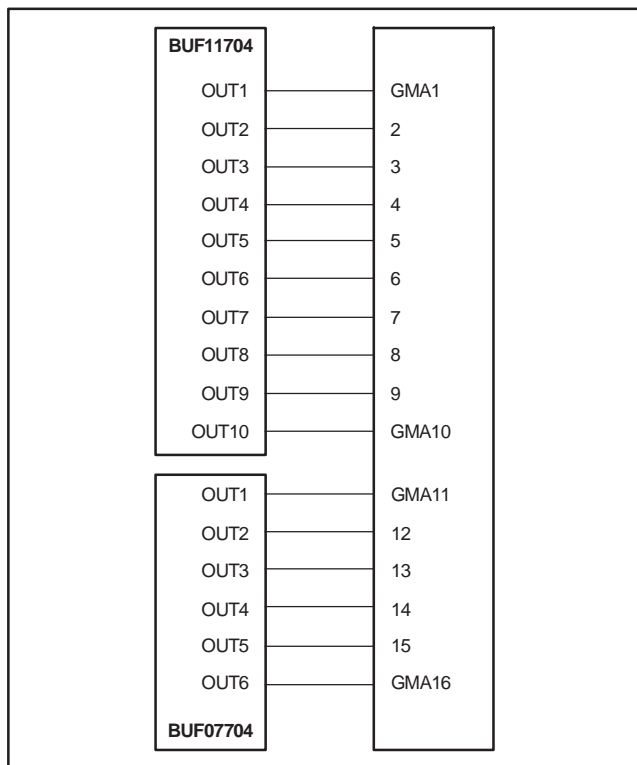
Figure 25. Creating > 10 Gamma Voltage Channels

MULTIPLE V$_{COM}$ CHANNELS

In some LCD panels, more than one V$_{COM}$ driver is required for best panel performance. Figure 26 uses three BUF07704s to create a total of 18 gamma-correction and three V$_{COM}$ channels. This solution saves considerable space and cost over the more conventional approach of using five or six quad-channel buffers or op amps.
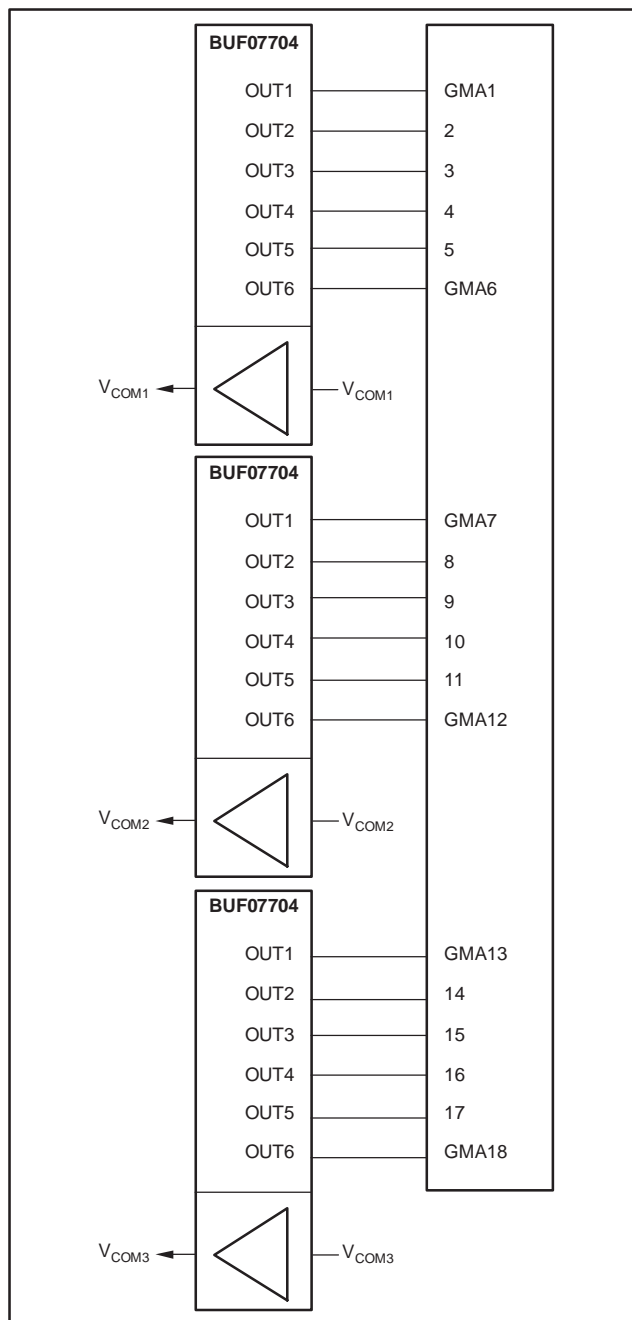

Figure 26. 18-Channel Application with Three Integrated V$_{COM}$ Channels

Table 1. How to Combine for > 10 Channels

	BUF05704	BUF06704	BUF07704	BUF11704
12ch	—	2	—	—
12ch + V_{COM}	—	1	1	—
14ch + V_{COM}	1	—	—	1
16ch + V_{COM}	—	1	—	1
18ch + V_{COM}	—	—	—	2
20ch + V_{COM}	—	—	—	2

COMPLETE LCD SOLUTION FROM TI

In addition to the BUFxx704 line of gamma correction buffers, TI offers a complete set of ICs for the LCD panel market, including source and gate drivers, timing controllers, various power-supply solutions, and audio power solutions. Figure 27 shows the total IC solution from TI.
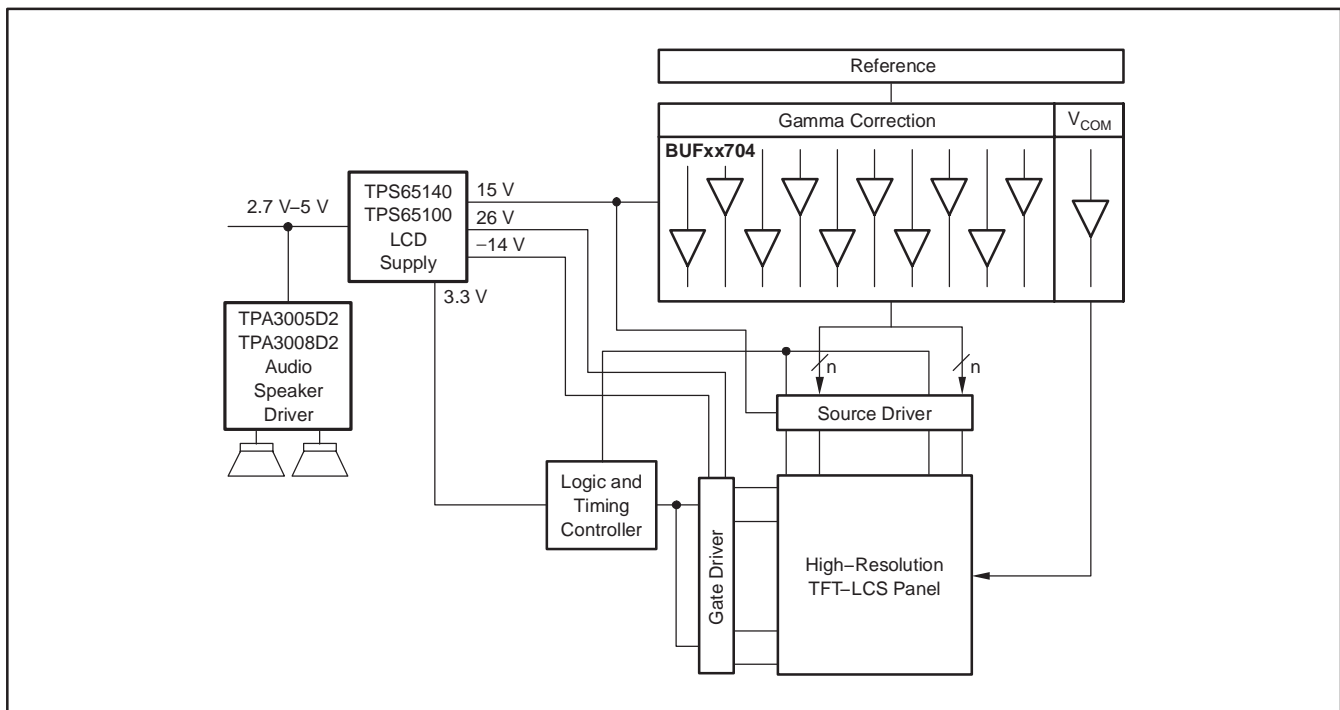
AUDIO POWER AMPLIFIER FOR TV SPEAKERS

The TPA3005D2 is a 6 W (per channel) stereo audio amplifier specifically targeted towards LCD monitors and TVs. It offers highly efficient, filter-free Class-D operation for driving bridge-tied stereo speakers. The TPA3005D2 is designed to drive stereo speakers as low as 8 Ω without an output filter. The high efficiency of the TPA3005D2 eliminates the need for external heatsinks when playing music. The TPA3008D2 is similar to the

TPA3005D2, but is capable of 8 W of output power. Texas Instruments offers a full line of linear and switch-mode audio power amplifiers. For more information, visit www.ti.com. For excellent audio performance, TI recommends the OPA364 (SBOS259) or OPA353 (SBOS103) as headphone drivers.

INTEGRATED DC/DC CONVERTERS FOR LCD PANELS: TPS65100 and TPS65140

The TPS65100 and TPS65140 offer a very compact and small power supply solution to provide all three power-supply voltages required by TFT (thin film transistor) LCD displays. Additionally the devices have an integrated V_{COM} buffer. The auxiliary linear regulator controller can be used to generate the 3.3 V logic power rail for systems powered by a 5 V supply rail only. The main output can power the LCD source drivers as well as the BUFxx704. An integrated adjustable charge pump doubler/tripler provides the positive LCD gate drive voltage. An externally adjustable negative charge pump provides the negative gate drive voltage. The TPS65100 has an integrated V_{COM} buffer to power the LCD backplane. A version of the BUFxx704 without the integrated V_{COM} buffer could be used for minimum redundancy and lowest cost. For LCD panels powered by 5 V only, the TPS65100 has a linear regulator controller that uses an external transistor to provide a regulated 3.3 V output for the digital circuits. Contact the local sales office for more information.

Figure 27. TI LCD Solution

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BUF05704, BUF06704
BUF07704, BUF11704

SBOS277F – JUNE 2004 – REVISED DECEMBER 2007
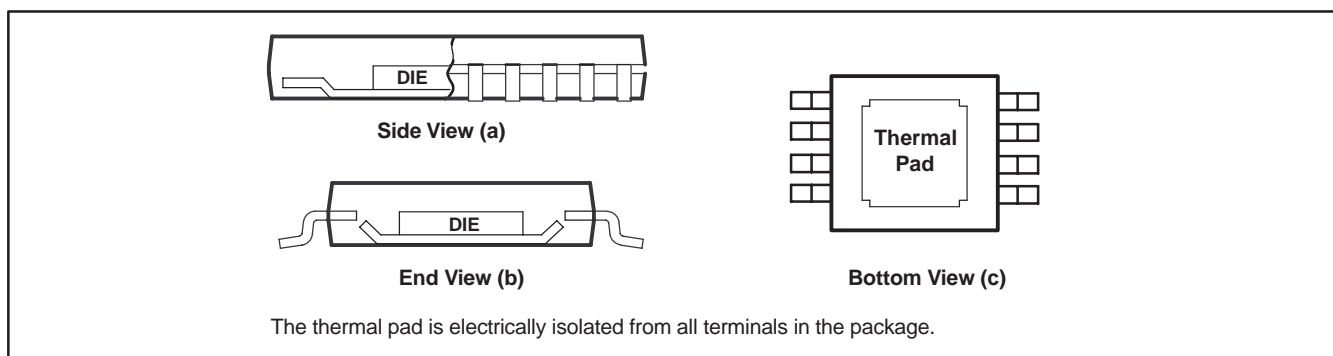
GENERAL PowerPAD DESIGN CONSIDERATIONS

The BUFxx704 is available in the thermally-enhanced PowerPAD family of packages. These packages are constructed using a downset leadframe upon which the die is mounted, as shown in Figure 28(a) and (b). This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package; see Figure 28(c). Due to this thermal pad having direct thermal contact with the die, excellent thermal performance is achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad must be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat-dissipating device. **Soldering the PowerPAD to the PCB is always required, even with applications that have low power dissipation.** This provides the necessary thermal and mechanical connection between the lead frame die pad and the PCB.

The PowerPAD must be connected to the device's most negative supply voltage.

1. Prepare the PCB with a top-side etch pattern. There should be etching for the leads as well as etch for the thermal pad.
2. Place recommended holes in the area of the thermal pad. Ideal thermal land size and thermal via patterns (2x3 for BUF05704 PWP-14 and BUF06704 PWP-16; 2x4 for BUF07704 PWP-20; and 2x5 for BUF11704 PWP-28) can be seen in the technical brief, *PowerPAD Thermally-Enhanced Package* (SLMA002), available for download at www.ti.com. These holes should be 13 mils (0.33 mm) in diameter. Keep them small, so that solder wicking through the holes is not a problem during reflow.

3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the BUFxx704 IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered; thus, wicking is not a problem.
4. Connect all holes to the internal ground plane.
5. When connecting these holes to the ground plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the BUFxx704 PowerPAD package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its six holes (BUF05704 and BUF06704), eight holes (BUF07704) or ten holes (BUF11704) exposed. The bottom-side solder mask should cover the holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, the BUFxx704 IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This preparation results in a properly installed part.

Side View (a)

End View (b)

Bottom View (c)

The thermal pad is electrically isolated from all terminals in the package.

Figure 28. Views of Thermally-Enhanced DGN Package

BUF05704,BUF06704
BUF07704,BUF11704

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For a given θ_{JA}, the maximum power dissipation is shown in Figure 29, and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

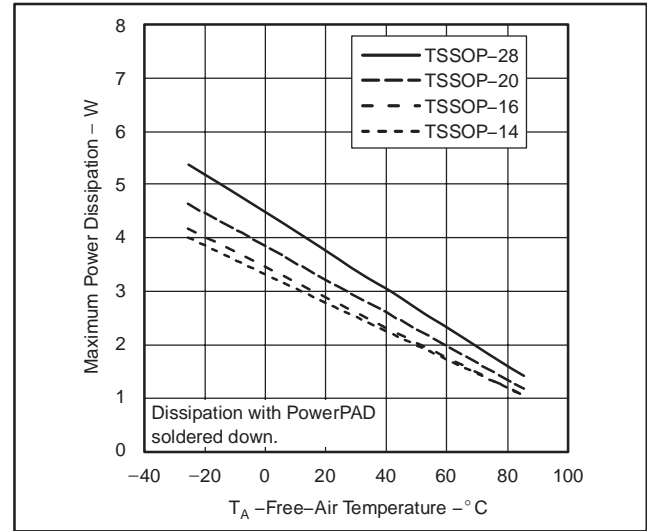P_D = maximum power dissipation (W)
T_{MAX} = absolute maximum junction temperature (125°C)
T_A = free-ambient air temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} = thermal coefficient from junction to case (°C/W)
θ_{CA} = thermal coefficient from case-to-ambient air (°C/W)

Figure 29. Maximum Power Dissipation vs Free-Air Temperature

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BUF05704AIPWPR	NRND	HTSSOP	PWP	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		BUF5704	
BUF07704AIPWPR	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	BUF07704	Samples
BUF11704AIPWP	NRND	HTSSOP	PWP	28	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	BUF11704	
BUF11704AIPWPR	NRND	HTSSOP	PWP	28	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	BUF11704	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BUF05704AIPWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
BUF07704AIPWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
BUF07704AIPWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
BUF11704AIPWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BUF05704AIPWPR	HTSSOP	PWP	14	2000	350.0	350.0	43.0
BUF07704AIPWPR	HTSSOP	PWP	20	2000	356.0	356.0	35.0
BUF07704AIPWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
BUF11704AIPWPR	HTSSOP	PWP	28	2000	350.0	350.0	43.0

TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
BUF11704AIPWP	PWP	HTSSOP	28	50	530	10.2	3600	3.5

PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224765/B

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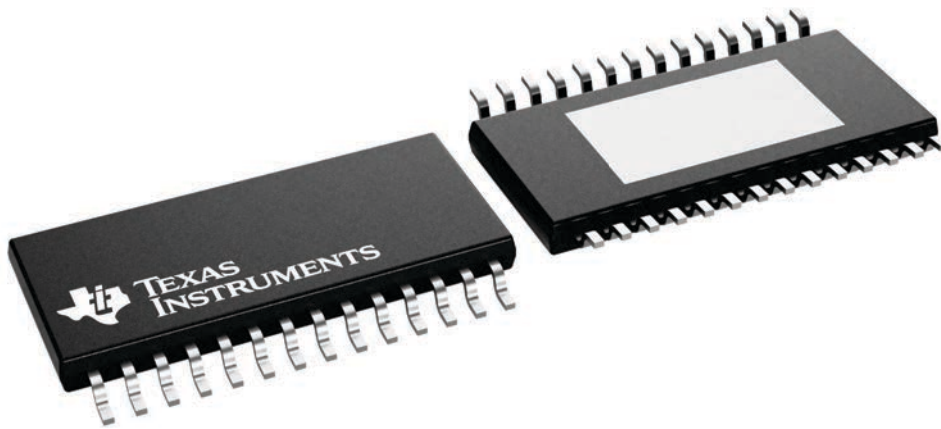
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.
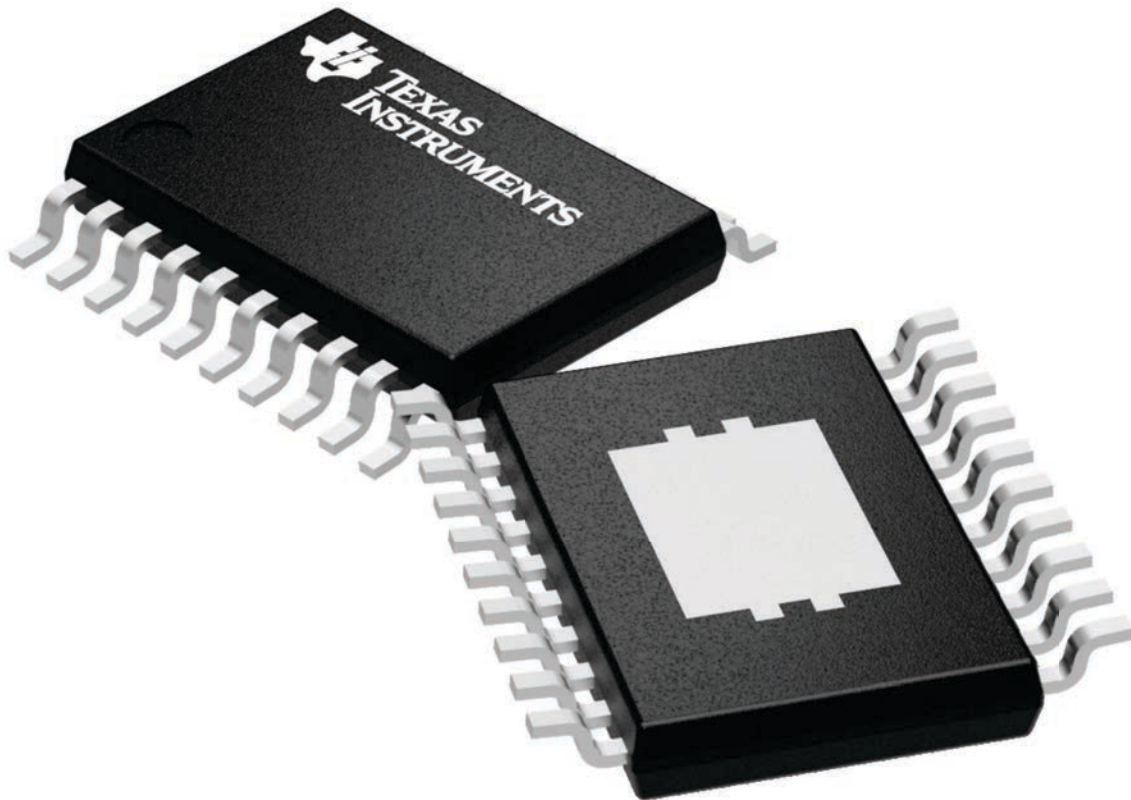
4224669/A

PWP (R−PDSO−G20)   PowerPAD ™ PLASTIC SMALL OUTLINE

4073225−4/I 05/11

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
        D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad
            Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding
            recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
        E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
        E. Falls within JEDEC MO−153

PowerPAD is a trademark of Texas Instruments.

![Texas Instruments logo] **TEXAS INSTRUMENTS**
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PWP (R−PDSO−G20)   PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

20 ... 11

0.30 MAX.

$\frac{2,40}{1,61}$

1.15 MAX. /B\

Exposed Thermal Pad

1 ... 10

$\frac{3,40}{2,61}$

Top View

Exposed Thermal Pad Dimensions

4206332−15/AO 01/16

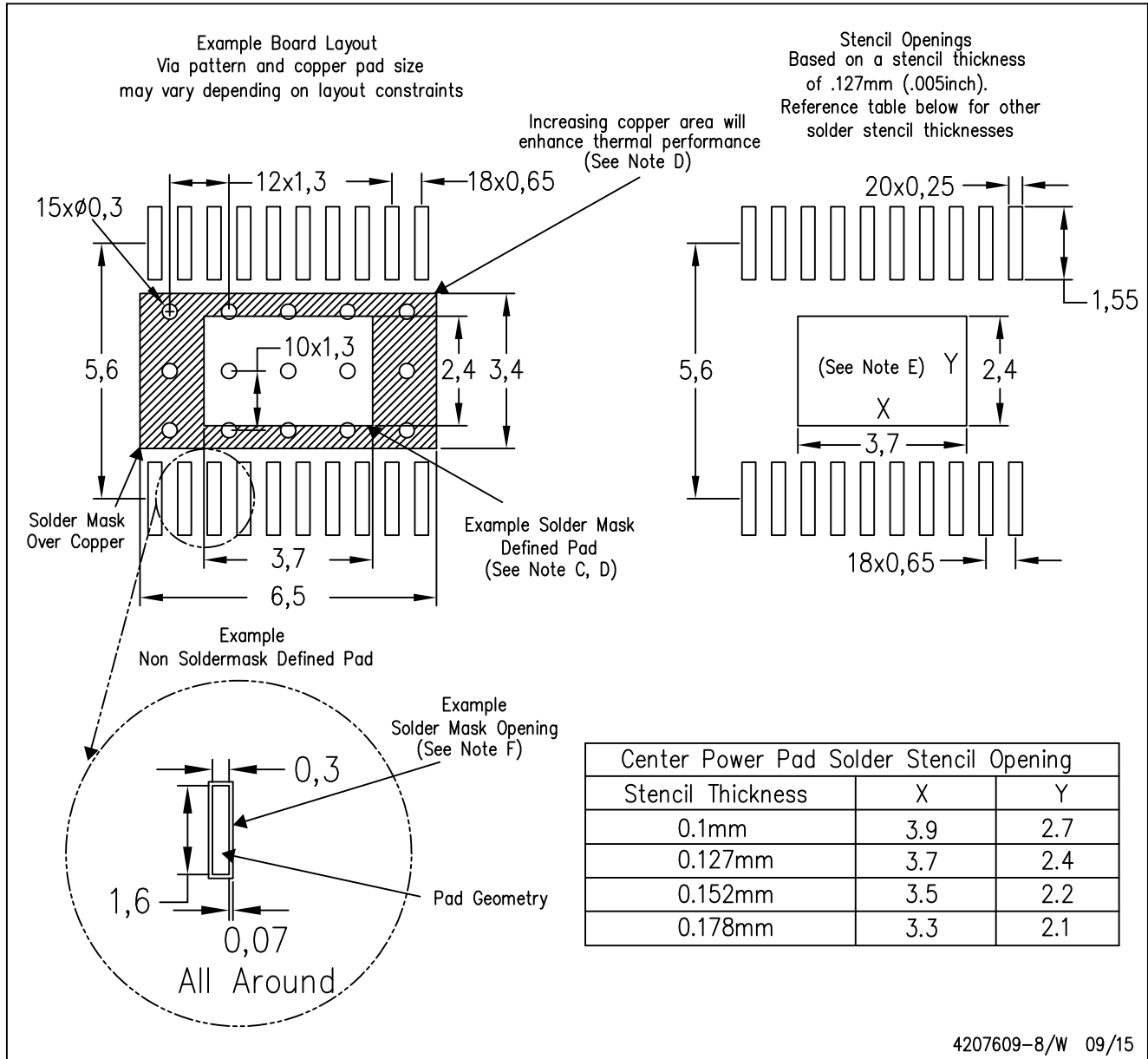NOTE: A. All linear dimensions are in millimeters

/B\ Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

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PWP (R-PDSO-G20)   PowerPAD™ PLASTIC SMALL OUTLINE

Example Board Layout
Via pattern and copper pad size
may vary depending on layout constraints

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).
Reference table below for other
solder stencil thicknesses

Increasing copper area will
enhance thermal performance
(See Note D)

15x⌀0,3

12x1,3   18x0,65

20x0,25

1,55

5,6

10x1,3

2,4 3,4

5,6

(See Note E) Y

2,4

X

3,7

Solder Mask
Over Copper

3,7

6,5

18x0,65

Example Solder Mask
Defined Pad
(See Note C, D)

Example
Non Soldermask Defined Pad

Example
Solder Mask Opening
(See Note F)

0,3

1,6

0,07
All Around

Pad Geometry

Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.9	2.7
0.127mm	3.7	2.4
0.152mm	3.5	2.2
0.178mm	3.3	2.1

4207609-8/W 09/15

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
        D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad
            Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets
            for specific thermal information, via requirements, and recommended board layout. These documents are available at
            www.ti.com <http://www.ti.com>. Publication IPC-7351 is recommended for alternate designs.
        E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric
            metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
        F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
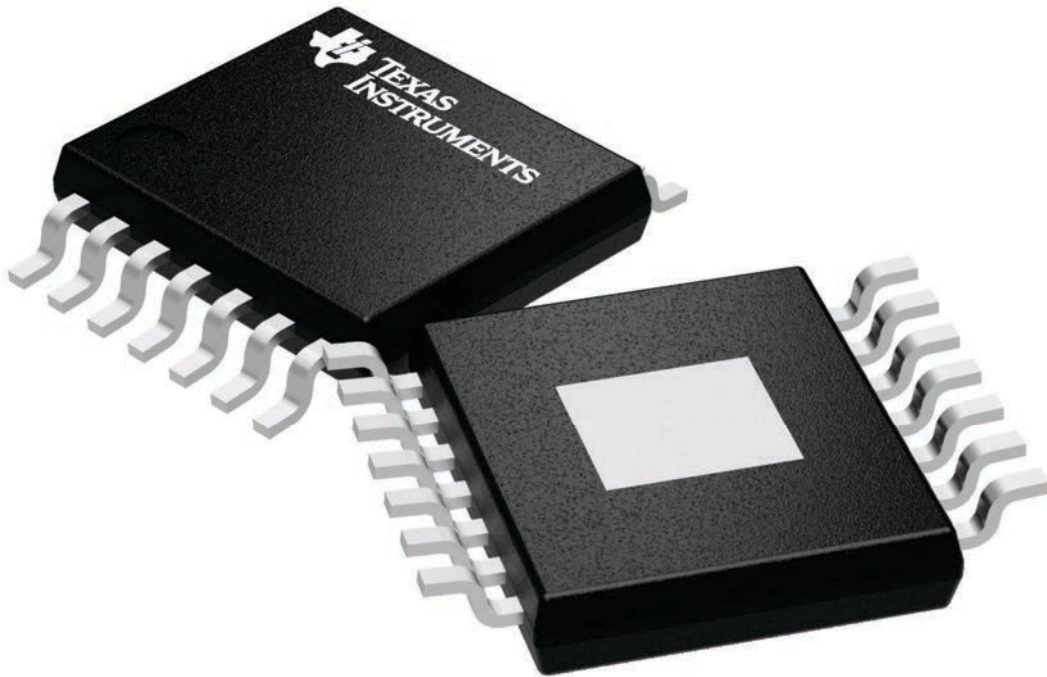
TEXAS
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PWP 14

4.4 x 5.0, 0.65 mm pitch

This image is a representation of the package family, actual package may vary.
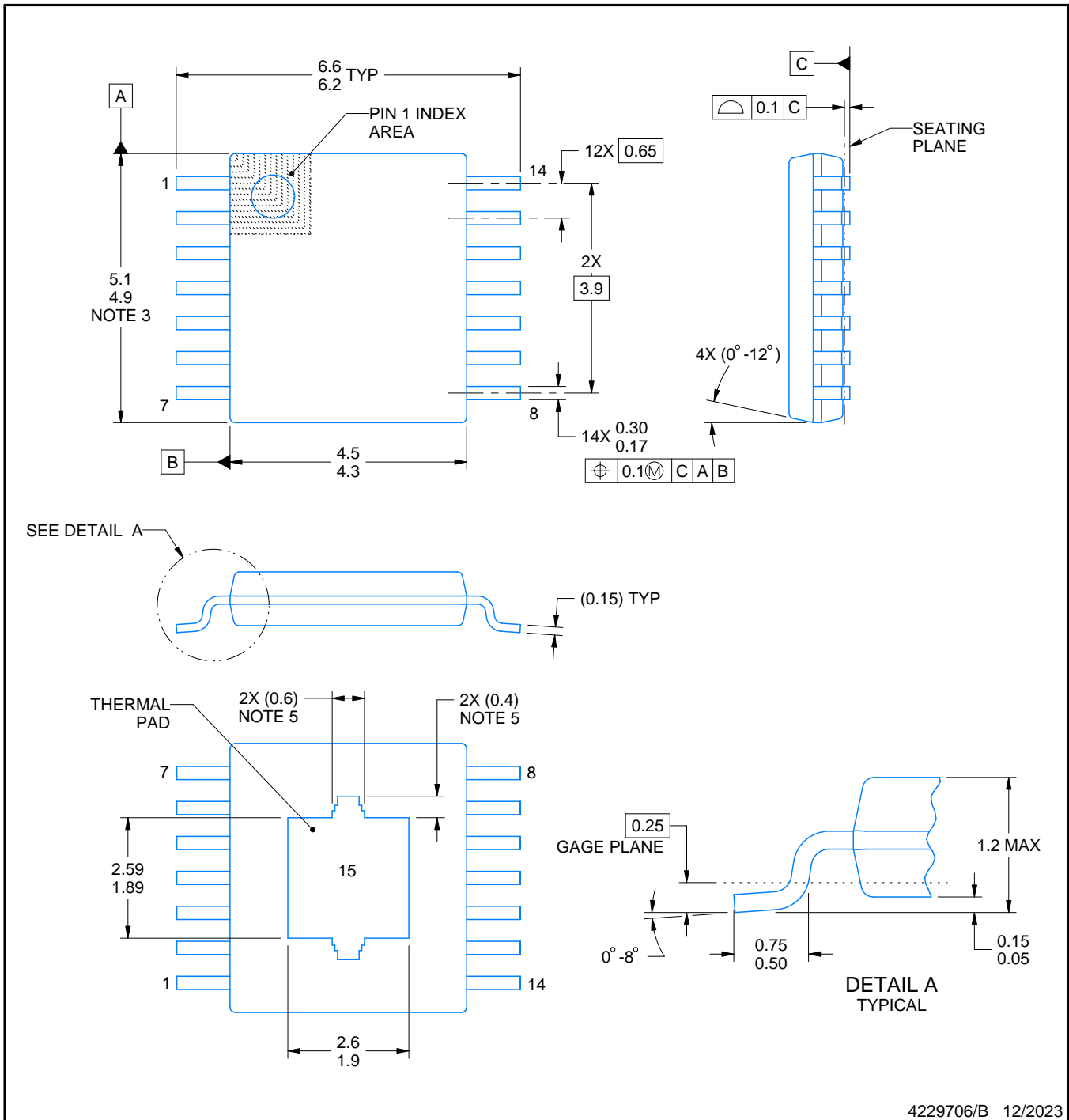Refer to the product data sheet for package details.

4224995/A

6.6 TYP
6.2

A

PIN 1 INDEX
AREA

12X 0.65

14

2X
3.9

5.1
4.9
NOTE 3

1

7

8

B

4.5
4.3

14X 0.30
0.17

⊕ 0.1 Ⓜ C A B

C

⌓ 0.1 C

SEATING
PLANE

4X (0°-12°)

SEE DETAIL A

(0.15) TYP

THERMAL
PAD

2X (0.6)
NOTE 5

2X (0.4)
NOTE 5

7

8

2.59
1.89

15

1

14

2.6
1.9

GAGE PLANE

0.25

0°-8°

0.75
0.50

1.2 MAX

0.15
0.05

DETAIL A
TYPICAL

4229706/B   12/2023

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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

14X (1.5)

14X (0.45) 1

(R0.05) TYP

SYMM ₵

12X (0.65)

7

(∅ 0.2) TYP VIA

SOLDER MASK DEFINED PAD

(3.4)
NOTE 9

(2.6)

SYMM ₵

METAL COVERED BY SOLDER MASK

14

(1.2) TYP

15

(5)
NOTE 9

(0.6)

(2.59)

8

(1.1) TYP

SEE DETAILS

(5.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X

SOLDER MASK OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK DEFINED

METAL UNDER SOLDER MASK

SOLDER MASK OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

PWP0014K

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE
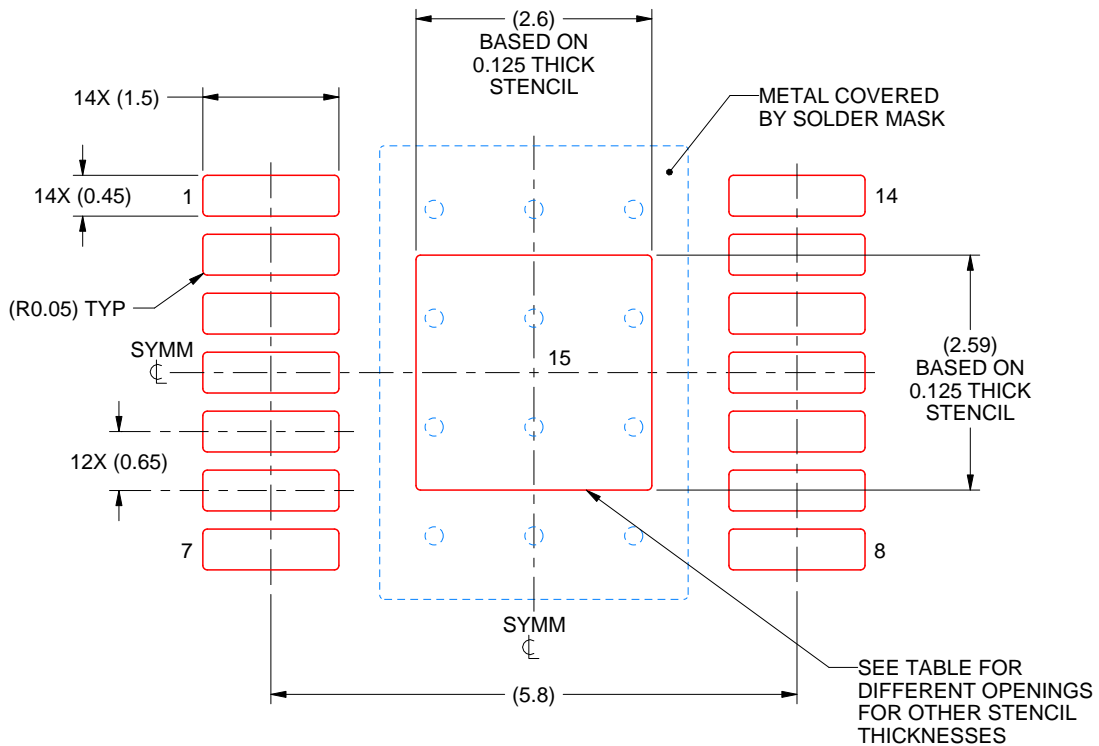
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 12X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 2.90
0.125	2.60 X 2.59 (SHOWN)
0.15	2.37 X 2.36
0.175	2.20 X 2.19

4229706/B   12/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.