TEXAS INSTRUMENTS
CC2640R2F-Q1
JAJSDZ1B – JANUARY 2017 – REVISED OCTOBER 2020

# CC2640R2F-Q1 車載用 SimpleLink™ Bluetooth® Low Energy ワイヤレス MCU

## 1 特長

- 車載アプリケーション認定済み
- 下記内容で AEC-Q100 認定済み:
  - デバイス温度グレード 2:-40℃～+105℃の動作時周囲温度範囲
  - デバイス HBM ESD 分類レベル 2
  - デバイス CDM ESD 分類レベル C3
- マイコン
  - 高性能な Arm® Cortex®-M3
  - EEMBC CoreMark® スコア:142
  - クロック速度:最大 48MHz
  - 275KB の不揮発性メモリ (128KB のイン・システム・プログラマブル・フラッシュを含む)
  - 最大 28KB のシステム SRAM、そのうち 20KB は超低リークの SRAM
  - キャッシュまたはシステム RAM として使用可能な 8KB の SRAM
  - 2 ピン cJTAG および JTAG デバッグ
  - OTA (Over-the-air) アップグレードをサポート
- 超低消費電力センサ・コントローラ
  - システムの他の部分から自律して動作可能
  - 16 ビット・アーキテクチャ
  - 2KB の超低リーク SRAM (コードおよびデータ用)
- 高効率のコード・サイズ・アーキテクチャ:ドライバ、Bluetooth® Low Energy コントローラ、およびブートローダを ROM に格納することで、アプリケーションで利用可能なフラッシュが増加
- RoHS 準拠の車載グレード・パッケージ
  - ウェッタブル・フランクを備えた 7mm×7mm RGZ VQFN48
- ペリフェラル
  - 31 の GPIO、すべてのデジタル・ペリフェラル・ピンを任意の GPIO に配線可能
  - 4 個の汎用タイマ・モジュール (8 個の 16 ビットまたは 4 個の 32 ビット・タイマ、それぞれ PWM)
  - 12 ビット ADC、200k サンプル/秒、8 チャネルのアナログ・セレクタ
  - 連続時間コンパレータ
  - 超低消費電力アナログ・コンパレータ
  - プログラマブルな電流ソース
  - UART
  - SSI×2 (SPI、MICROWIRE、TI)
  - $I^2C$、$I^2S$
  - リアルタイム・クロック (RTC)
  - AES-128 セキュリティ・モジュール
  - TRNG (True Random Number Generator)
  - 8 つの静電容量式センシング・ボタンのサポート
  - 温度センサ内蔵
- 外部システム
  - オンチップの内蔵 DC/DC コンバータ
  - 必要な外部部品はごくわずか
  - SimpleLink™ CC2590 および CC2592 レンジ・エクステンダとのシームレスな統合
- 低消費電力
  - 広い電源電圧範囲:1.8～3.8V
  - アクティブ・モードの RX:6.1mA
  - アクティブ・モードの TX (0dBm):7.0mA
  - アクティブ・モードの TX (+5dBm):9.3mA
  - アクティブ・モードの MCU:61µA/MHz
  - アクティブ・モードの MCU:48.5CoreMark/mA
  - アクティブ・モードのセンサ・コントローラ:0.4mA + 8.2µA/MHz
  - スタンバイ:1.3µA (RTC 動作、RAM/CPU 保持)
  - シャットダウン:150nA (外部イベントによるウェークアップ)
- RF 部:
  - Bluetooth Low Energy (BLE) 4.2 および 5 仕様と互換性のある 2.4GHz RF トランシーバ
  - 優れたレシーバ感度 (Bluetooth Low Energy 1Mbps で -97dBm)、選択性、およびブロッキング性能
  - 最大 +5dBm のプログラム可能な出力電力
  - Bluetooth Low Energy 1Mbps でリンク・バジェット 102dB
  - 国際的な無線周波数規制への準拠を目標としたシステムに最適
    - ETSI EN 300 328 および EN 300 440 (ヨーロッパ)
    - FCC CFR47 Part 15 (米国)
    - ARIB STD-T66 (日本)
- 開発ツールとソフトウェア
  - フル機能の開発キット
  - Sensor Controller Studio
  - SmartRF™ Studio
  - IAR Embedded Workbench®® for Arm®
  - Code Composer Studio™ 統合開発環境 (IDE)
  - Code Composer Studio™ Cloud IDE

## 2 アプリケーション

- 車載用
  - カー・アクセスとセキュリティ・システム
    - パッシブ・エントリ、パッシブ・スタート (PEPS)
    - Phone-as-a-Key (PaaK:電話をキーとして使用)

- リモート・キーレス・エントリ (RKE)
- 産業用
  - ファクトリ・オートメーション
  - アセット・トラッキングおよび管理
  - ヒューマン・マシン・インターフェイス (HMI)
  - アクセス制御

## 3 概要

SimpleLink™ Bluetooth® Low Energy CC2640R2F-Q1 デバイスは、パッシブ・エントリ / パッシブ・スタート (PEPS)、リモート・キーレス・エントリ (RKE)、カー・シェアリング、パイロテッド・パーキング、ケーブル代替、スマートフォン接続といった Bluetooth® 4.2 および Bluetooth® 5 Low Energy 車載アプリケーションを対象とした、AEC-Q100 準拠のワイヤレス・マイクロコントローラ (MCU) です。

CC2640R2F-Q1 デバイス は、テキサス・インスツルメンツ™の SimpleLink™ MCU プラットフォームの一部です。このプラットフォームは、Wi-Fi®、Bluetooth® Low Energy、Sub-1GHz、イーサネット、 Zigbee®、Thread、およびホスト・マイコンで構成されています。これらのデバイスはすべて、中心となる単一のソフトウェア開発キット (SDK) と豊富なツール・セットを持つ、共通の使いやすい開発環境を共有しています。SimpleLink™ プラットフォームは一度で統合を実現でき、製品ラインアップのどのデバイスの組み合わせでも設計に追加できるので、設計要件変更の際もコードの 100% 再利用が可能です。詳細については、http://www.tij.co.jp/wireless-connectivity/simplelink-solutions/overview/overview.html を参照してください。

CC2640R2F-Q1 は、柔軟な低消費電力モードに加えて、アクティブ時の RF および MCU の消費電流が非常に小さいため、優れたバッテリ寿命を実現し、小型のコインセル・バッテリでの長距離動作と、カー・バッテリに接続されたノードでの低消費電力フットプリントを可能にします。優れたレシーバ感度とプログラム可能な出力電力により、要求の厳しい車載用 RF 環境に必要とされる、業界最先端の RF 性能を実現しています。

CC2640R2F-Q1 ワイヤレス MCU には、32 ビットの Arm® Cortex®-M3 プロセッサが搭載されており、メイン・アプリケーション・プロセッサとして 48MHz で動作するほか、Bluetooth® 4.2 Low Energy コントローラとホスト・ライブラリを ROM に格納しています。このアーキテクチャにより、総合的なシステム性能が向上し、消費電力が減少し、アプリケーション用に多くのフラッシュ・メモリを解放できます。

また、このデバイスはグレード 2 温度範囲 (-40℃～＋ 105℃) で AEC-Q100 認定済みであり、ウェッタブル・フランク付きの 7mm×7mm VQFN パッケージで供給されています。ウェッタブル・フランクは、生産ライン・コストの削減と、ハンダ付け箇所の光学検査による信頼性の向上に役立ちます。

Bluetooth Low Energy ソフトウェア・スタックは、TI.com から無償で入手できます。

**製品情報** (1)

| 部品番号 | パッケージ | 本体サイズ (公称) |
|---|---|---|
| CC2640R2FTWRGZQ1 | ウェッタブル・フランク付き VQFN (48) | 7.00mm×7.00mm |

(1) 詳細については、「メカニカル、パッケージ、および注文情報」を参照してください。

# 4 機能ブロック図

図 4-1 に、CC2640R2F-Q1 デバイスの機能ブロック図を示します。

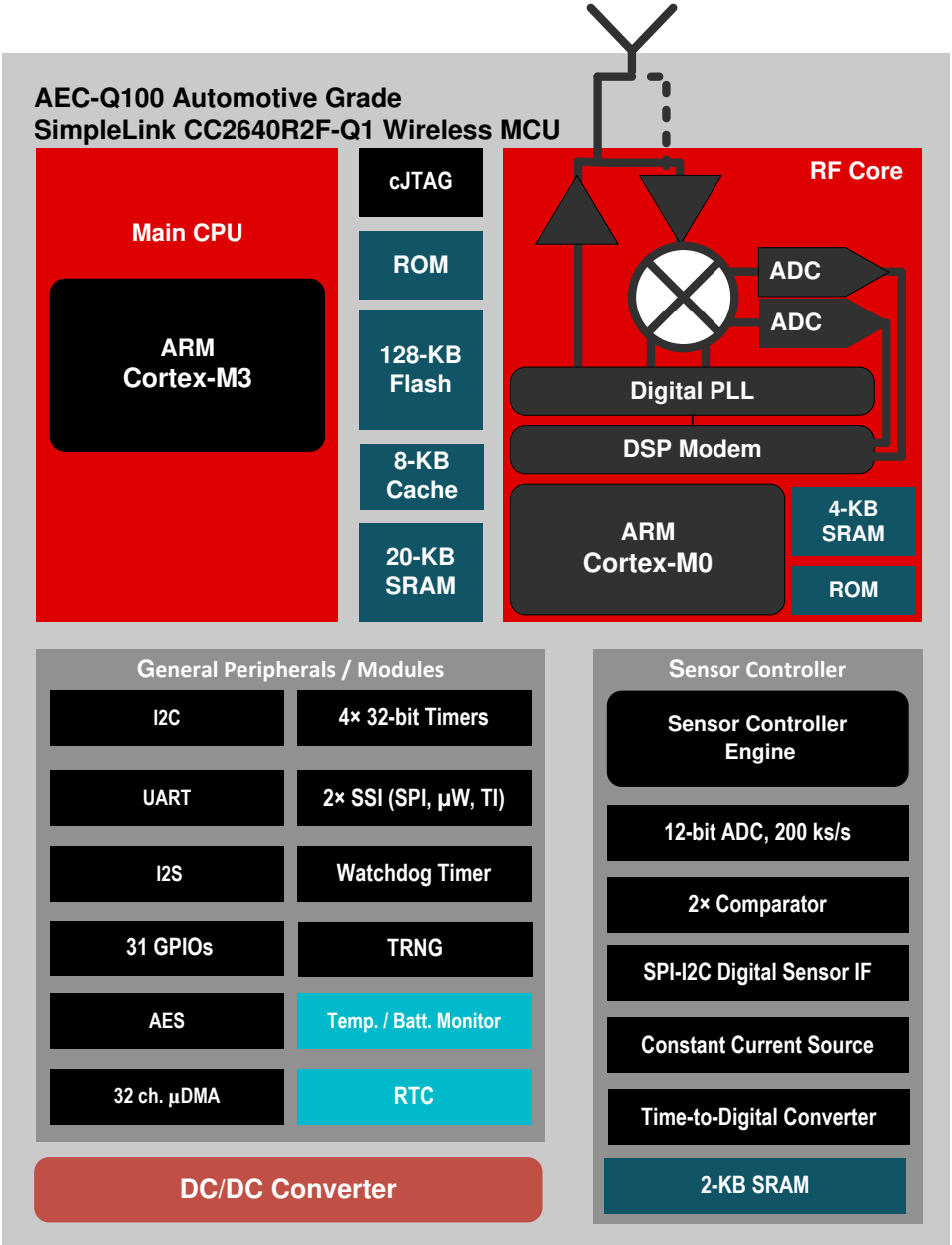


**図 4-1. ブロック図**

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## 5 Revision History

| Changes from Revision A (August 2017) to Revision B (October 2020) | Page |
|---|---|
| • 文書全体にわたってセクション、表、図、相互参照の採番方法を更新 | 1 |
| • セクション 1 の開発ツールとソフトウェアを変更 | 1 |
| • セクション 2 を変更 | 1 |
| • セクション 3 を変更 | 2 |
| • Added note to セクション 8.1 about injection current and associated this note with the "Voltage on any digital pin" specification | 10 |
| • Removed the flash write time specification's association with note 2 in セクション 8.5 | 11 |
| • Added "Zero cycles" as the test condition for flash page/sector erase time in セクション 8.5 | 11 |
| • Added new flash page/sector erase time at 30 000 cycles in セクション 8.5 | 11 |

# 6 Device Comparison

**表 6-1. Device Family Overview**

| DEVICE | PHY SUPPORT | FLASH (KB) | RAM (KB) | GPIO | PACKAGE(1) |
|---|---|---|---|---|---|
| CC2640R2F-Q1(2) | Bluetooth low energy (Normal, High Speed, Long Range, Automotive) | 128 | 20 | 31 | RGZ (Wettable Flanks) |
| CC2640R2Fxxx(2) | Bluetooth low energy (Normal, High Speed, Long Range) | 128 | 20 | 31, 15, 14, 10 | RGZ, RHB, YFV, RSM |
| CC2650F128xxx | Multi-Protocol(3) | 128 | 20 | 31, 15, 10 | RGZ, RHB, RSM |
| CC2640F128xxx | Bluetooth low energy (Normal) | 128 | 20 | 31, 15, 10 | RGZ, RHB, RSM |
| CC2630F128xxx | IEEE 802.15.4 (Zigbee/6LoWPAN) | 128 | 20 | 31, 15, 10 | RGZ, RHB, RSM |
| CC2620F128xxx | IEEE 802.15.4 (RF4CE) | 128 | 20 | 31, 10 | RGZ, RSM |

(1) Package designator replaces the xxx in device name to form a complete device name, RGZ is 7-mm × 7-mm VQFN48, RHB is 5-mm × 5-mm VQFN32, RSM is 4-mm × 4-mm VQFN32, and YFV is 2.7-mm × 2.7-mm DSBGA.
(2) CC2640R2F-xxx devices contain Bluetooth 4.2 Host and Controller libraries in ROM, leaving more of the 128KB of flash available for the customer application when used with supported BLE-Stack software protocol stack releases. Actual use of ROM and flash by the protocol stack may vary depending on device software configuration. See Bluetooth low energy Stack for more details.
(3) The CC2650 device supports all PHYs and can be reflashed to run all the supported standards.

**表 6-2. Typical(1) Flash Memory Available for Customer Applications**

| Device | Simple BLE Peripheral (BT 4.0)(2) | Simple BLE Peripheral (BT 4.2)(2) (3) |
|---|---|---|
| CC2640R2Fxxx, CC2640R2F-Q1(4) | 83 KB | 80 KB |
| CC2640F128xxx, CC2650F128xxx | 41 KB | 31 KB |

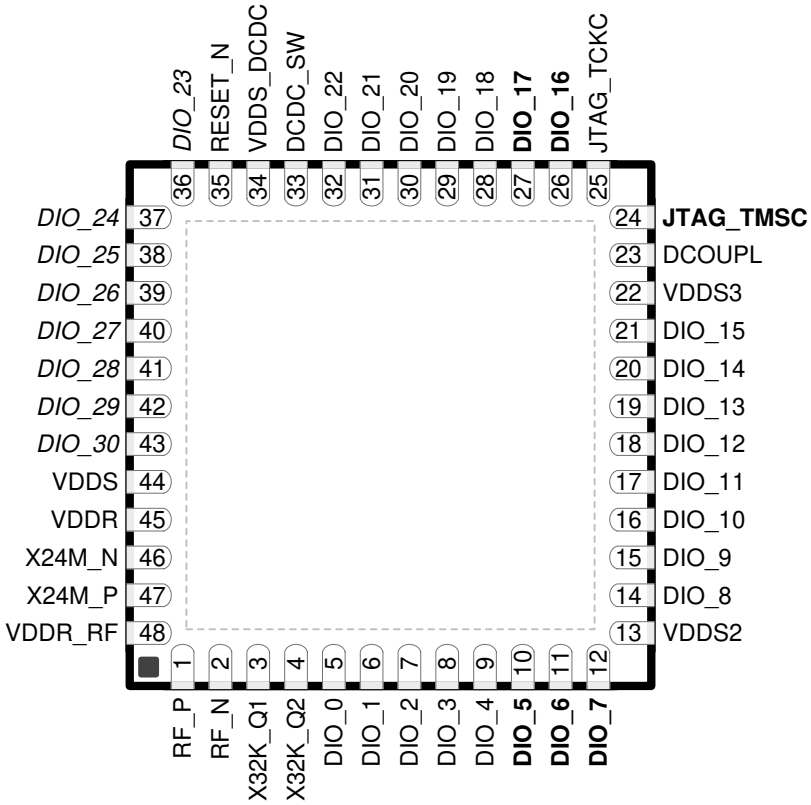
(1) Actual use of ROM and flash by the protocol stack will vary depending on device software configuration. The values in this table are provided as guidance only.
(2) Application example with two services (GAP and Simple Profile). Compiled using IAR.
(3) BT4.2 configuration including Secure Pairing, Privacy 1.2, and Data Length Extension
(4) Bluetooth low energy applications running on the CC2640R2F-Q1 device make use of up to 115 KB of system ROM and up to 32 KB of RF Core ROM in order to minimize the flash usage. The maximum amount of nonvolatile memory available for Bluetooth low energy applications on the CC2640R2F-Q1 device is thus 275 KB (128-KB flash + 147-KB ROM).

## 6.1 Related Products

| | |
|---|---|
| Wireless Connectivity | The wireless connectivity portfolio offers a wide selection of low power RF solutions suitable for a broad range of applications. The offerings range from fully customized solutions to turn key offerings with pre-certified hardware and software (protocol). |
| TI's SimpleLink™ Sub-1 GHz Wireless MCUs | Long-range, low-power wireless connectivity solutions are offered in a wide range of Sub-1 GHz ISM bands. |
| Design & development | Review design and development resources that are available for this product. |
| SimpleLink™ CC2640R2 Wireless MCU LaunchPad™ Development Kit | The CC2640R2 LaunchPad™ development kit brings easy Bluetooth low energy (BLE) connection to the LaunchPad ecosystem with the SimpleLink ultra-low power CC26xx family of devices. Compared to the CC2650 LaunchPad kit, the CC2640R2 LaunchPad kit provides the following:<br>• More free flash memory for the user application in the CC2640R2 wireless MCU<br>• Out-of-the-box support for Bluetooth 4.2 specification<br>• 4× faster over-the-air download speed compared to Bluetooth 4.1 |
| SimpleLink™ Bluetooth low energy/Multistandard SensorTag | The SensorTag IoT kit invites you to realize your cloud-connected product idea. The SensorTag includes 10 low-power MEMS sensors in a tiny red package, and it is expandable with DevPacks to make it easy to add your own sensors or actuators. |
| Reference Designs for CC2640 | TI Reference Design Library is a robust reference design library spanning analog, embedded processor and connectivity. Created by TI experts to help you jump-start your system design, all TI Designs include schematic or block diagrams, BOMs and design files to speed your time to market. Search and download designs at ti.com/tidesigns. |

# 7 Terminal Configuration and Functions

## 7.1 Pin Diagram – RGZ Package




The following I/O pins marked in **bold** have high-drive capabilities:

- Pin 10: DIO_5
- Pin 11: DIO_6
- Pin 12: DIO_7
- Pin 24: JTAG_TMSC
- Pin 26: DIO_16
- Pin 27: DIO_17

The following I/O pins marked in *italics* have analog capabilities:

- Pin 36: DIO_23
- Pin 37: DIO_24
- Pin 38: DIO_25
- Pin 39: DIO_26
- Pin 40: DIO_27
- Pin 41: DIO_28
- Pin 42: DIO_29
- Pin 43: DIO_30

**図 7-1. 48-Pin RGZ Package With Wettable Flanks, 7-mm × 7-mm Pinout, 0.5-mm Pitch (Top View)**

## 7.2 Signal Descriptions – RGZ Package

表 7-1. Signal Descriptions – RGZ Package

| NAME | NO. | TYPE | DESCRIPTION |
|---|---|---|---|
| DCDC_SW | 33 | Power | Output from internal DC/DC(1) |
| DCOUPL | 23 | Power | 1.27-V regulated digital-supply decoupling capacitor(2) |
| DIO_0 | 5 | Digital I/O | GPIO, Sensor Controller |
| DIO_1 | 6 | Digital I/O | GPIO, Sensor Controller |
| DIO_2 | 7 | Digital I/O | GPIO, Sensor Controller |
| DIO_3 | 8 | Digital I/O | GPIO, Sensor Controller |
| DIO_4 | 9 | Digital I/O | GPIO, Sensor Controller |
| DIO_5 | 10 | Digital I/O | GPIO, Sensor Controller, high-drive capability |
| DIO_6 | 11 | Digital I/O | GPIO, Sensor Controller, high-drive capability |
| DIO_7 | 12 | Digital I/O | GPIO, Sensor Controller, high-drive capability |
| DIO_8 | 14 | Digital I/O | GPIO |
| DIO_9 | 15 | Digital I/O | GPIO |
| DIO_10 | 16 | Digital I/O | GPIO |
| DIO_11 | 17 | Digital I/O | GPIO |
| DIO_12 | 18 | Digital I/O | GPIO |
| DIO_13 | 19 | Digital I/O | GPIO |
| DIO_14 | 20 | Digital I/O | GPIO |
| DIO_15 | 21 | Digital I/O | GPIO |
| DIO_16 | 26 | Digital I/O | GPIO, JTAG_TDO, high-drive capability |
| DIO_17 | 27 | Digital I/O | GPIO, JTAG_TDI, high-drive capability |
| DIO_18 | 28 | Digital I/O | GPIO |
| DIO_19 | 29 | Digital I/O | GPIO |
| DIO_20 | 30 | Digital I/O | GPIO |
| DIO_21 | 31 | Digital I/O | GPIO |
| DIO_22 | 32 | Digital I/O | GPIO |
| DIO_23 | 36 | Digital/Analog I/O | GPIO, Sensor Controller, Analog |
| DIO_24 | 37 | Digital/Analog I/O | GPIO, Sensor Controller, Analog |
| DIO_25 | 38 | Digital/Analog I/O | GPIO, Sensor Controller, Analog |
| DIO_26 | 39 | Digital/Analog I/O | GPIO, Sensor Controller, Analog |
| DIO_27 | 40 | Digital/Analog I/O | GPIO, Sensor Controller, Analog |
| DIO_28 | 41 | Digital/Analog I/O | GPIO, Sensor Controller, Analog |
| DIO_29 | 42 | Digital/Analog I/O | GPIO, Sensor Controller, Analog |
| DIO_30 | 43 | Digital/Analog I/O | GPIO, Sensor Controller, Analog |
| JTAG_TMSC | 24 | Digital I/O | JTAG TMSC, high-drive capability |
| JTAG_TCKC | 25 | Digital I/O | JTAG TCKC |
| RESET_N | 35 | Digital input | Reset, active-low. No internal pullup. |
| RF_P | 1 | RF I/O | Positive RF input signal to LNA during RX<br>Positive RF output signal to PA during TX |
| RF_N | 2 | RF I/O | Negative RF input signal to LNA during RX<br>Negative RF output signal to PA during TX |
| VDDR | 45 | Power | Connect to output of internal DC/DC(2) (3) |
| VDDR_RF | 48 | Power | Connect to output of internal DC/DC(2) (4) |

**表 7-1. Signal Descriptions – RGZ Package (continued)**

| NAME | NO. | TYPE | DESCRIPTION |
|---|---|---|---|
| VDDS | 44 | Power | 1.8-V to 3.8-V main chip supply(1) |
| VDDS2 | 13 | Power | 1.8-V to 3.8-V DIO supply(1) |
| VDDS3 | 22 | Power | 1.8-V to 3.8-V DIO supply(1) |
| VDDS_DCDC | 34 | Power | 1.8-V to 3.8-V DC/DC supply |
| X32K_Q1 | 3 | Analog I/O | 32-kHz crystal oscillator pin 1 |
| X32K_Q2 | 4 | Analog I/O | 32-kHz crystal oscillator pin 2 |
| X24M_N | 46 | Analog I/O | 24-MHz crystal oscillator pin 1 |
| X24M_P | 47 | Analog I/O | 24-MHz crystal oscillator pin 2 |
| EGP | | Power | Ground – Exposed Ground Pad |

(1) See the technical reference manual listed in セクション 11.3 for more details.
(2) Do not supply external circuitry from this pin.
(3) If internal DC/DC is not used, this pin is supplied internally from the main LDO.
(4) If internal DC/DC is not used, this pin must be connected to VDDR for supply from the main LDO.

## 7.3 Wettable Flanks

The automotive industry requires original equipment manufacturers (OEMs) to perform 100% automated visual inspection (AVI) post-assembly to ensure that cars meet the current demands for safety and high reliability. Standard quad-flat no-lead (VQFN) packages do not have solderable or exposed pins/terminals that are easily viewed. It is therefore difficult to determine visually whether or not the package is successfully soldered onto the printed circuit board (PCB). To resolve the issue of side-lead wetting of leadless packaging for automotive and commercial component manufacturers, the wettable-flank process was developed. The wettable flanks on the VQFN package provide a visual indicator of solderability and thereby lower the inspection time and manufacturing costs.

The CC2640R2F-Q1 device is assembled using an automotive-grade VQFN package with wettable flanks.

# 8 Specifications

## 8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, VDDS(3) | VDDR supplied by internal DC/DC regulator or internal GLDO. VDDS_DCDC connected to VDDS on PCB. | –0.3 | 4.1 | V |
| Voltage on any digital pin(4) (5) | | –0.3 | VDDS + 0.3, max 4.1 | V |
| Voltage on crystal oscillator pins, X32K_Q1, X32K_Q2, X24M_N and X24M_P | | –0.3 | VDDR + 0.3, max 2.25 | V |
| Voltage on ADC input ($V_{in}$) | Voltage scaling enabled | –0.3 | VDDS | V |
| | Voltage scaling disabled, internal reference | –0.3 | 1.49 | |
| | Voltage scaling disabled, VDDS as reference | –0.3 | VDDS / 2.9 | |
| Input RF level | | | 5 | dBm |
| $T_{stg}$ | Storage temperature | –40 | 150 | °C |

(1) All voltage values are with respect to ground, unless otherwise noted.
(2) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(3) VDDS2 and VDDS3 need to be at the same potential as VDDS.
(4) Including analog-capable DIO.
(5) Injection current is not supported on any GPIO pin.

## 8.2 ESD Ratings

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{ESD}$ | Electrostatic discharge | Human Body Model (HBM), per AEC Q100-002(1) (2) | All pins | ±2000 | V |
| | | Charged Device Model (CDM), per AEC Q100-011(3) | XOCS pins 46, 47 | ±250 | |
| | | | All other pins | ±500 | |

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Ambient temperature | | –40 | 105 | °C |
| Operating supply voltage, VDDS | For operation in battery-powered and 3.3-V systems (internal DC/DC can be used to minimize power consumption) | 1.8 | 3.8 | V |

## 8.4 Power Consumption Summary

Measured on the TI CC2640Q1EM-7ID reference design with $T_c$ = 25°C, $V_{DDS}$ = 3.0 V with internal DC/DC converter, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{core}$ | Core current consumption | Reset. RESET_N pin asserted or VDDS below power-on-reset (POR) threshold | | 100 | | nA |
| | | Shutdown. No clocks running, no retention | | 150 | | |
| | | Standby. With RTC, CPU, RAM and (partial) register retention. RCOSC_LF | | 1.3 | | µA |
| | | Standby. With RTC, CPU, RAM and (partial) register retention. XOSC_LF | | 1.5 | | |
| | | Standby. With Cache, RTC, CPU, RAM and (partial) register retention. RCOSC_LF | | 3.4 | | |
| | | Standby. With Cache, RTC, CPU, RAM and (partial) register retention. XOSC_LF | | 3.6 | | |
| | | Idle. Supply Systems and RAM powered. | | 650 | | |
| | | Active. Core running CoreMark | | 1.45 mA + 31 µA/MHz | | |
| | | Radio RX | | 6.1 | | mA |
| | | Radio TX, 0-dBm output power | | 7.0 | | |
| | | Radio TX, 5-dBm output power | | 9.3 | | |
| **Peripheral Current Consumption (Adds to core current $I_{core}$ for each peripheral unit activated)**(1) | | | | | | |
| $I_{peri}$ | Peripheral power domain | Delta current with domain enabled | | 20 | | µA |
| | Serial power domain | Delta current with domain enabled | | 13 | | µA |
| | RF Core | Delta current with power domain enabled, clock enabled, RF core idle | | 237 | | µA |
| | µDMA | Delta current with clock enabled, module idle | | 130 | | µA |
| | Timers | Delta current with clock enabled, module idle | | 113 | | µA |
| | $I^2C$ | Delta current with clock enabled, module idle | | 12 | | µA |
| | I2S | Delta current with clock enabled, module idle | | 36 | | µA |
| | SSI | Delta current with clock enabled, module idle | | 93 | | µA |
| | UART | Delta current with clock enabled, module idle | | 164 | | µA |

(1) $I_{peri}$ is not supported in Standby or Shutdown.

## 8.5 General Characteristics

$T_c$ = 25°C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **FLASH MEMORY** | | | | | |
| Supported flash erase cycles before failure | | 100 | | | k Cycles |
| Maximum number of write operations per row before erase(1) | | | | 83 | write operations |
| Flash retention | 105°C | 11.4 | | | Years at 105°C |
| Flash page/sector erase current | Average delta current | | 12.6 | | mA |
| Flash page/sector size | | | 4 | | KB |
| Flash page/sector erase time(2) | Zero cycles | | 8 | | ms |
| Flash page/sector erase time (2) | 30 000 cycles | | | 4000 | ms |
| Flash write current | Average delta current, 4 bytes at a time | | 8.15 | | mA |

## 8.5 General Characteristics (continued)

$T_c$ = 25°C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Flash write time | 4 bytes at a time | | 8 | | µs |

(1) Each row is 2048 bits (or 256 bytes) wide.
(2) This number is dependent on Flash aging and will increase over time and erase cycles.

## 8.6 1-Mbps GFSK (Bluetooth low energy Technology) – RX

Measured on the TI CC2640Q1EM-7ID reference design with $T_c$ = 25°C, $V_{DDS}$ = 3.0 V, $f_{RF}$ = 2440 MHz, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Receiver sensitivity | Differential mode. Measured at the CC2640Q1EM-7ID SMA connector, BER = $10^{-3}$ | | –97 | | dBm |
| Receiver saturation | Differential mode. Measured at the CC2640Q1EM-7ID SMA connector, BER = $10^{-3}$ | | 4 | | dBm |
| Frequency error tolerance | Difference between the incoming carrier frequency and the internally generated carrier frequency | –350 | | 350 | kHz |
| Data rate error tolerance | Difference between incoming data rate and the internally generated data rate | –750 | | 750 | ppm |
| Co-channel rejection(3) | Wanted signal at –67 dBm, modulated interferer in channel, BER = $10^{-3}$ | | –6 | | dB |
| Selectivity, ±1 MHz(3) | Wanted signal at –67 dBm, modulated interferer at ±1 MHz, BER = $10^{-3}$ | | 7 / 2(1) | | dB |
| Selectivity, ±2 MHz(3) | Wanted signal at –67 dBm, modulated interferer at ±2 MHz, Image frequency is at –2 MHz, BER = $10^{-3}$ | | 39 / 17(2) (1) | | dB |
| Selectivity, ±3 MHz(3) | Wanted signal at –67 dBm, modulated interferer at ±3 MHz, BER = $10^{-3}$ | | 38 / 30(1) | | dB |
| Selectivity, ±4 MHz(3) | Wanted signal at –67 dBm, modulated interferer at ±4 MHz, BER = $10^{-3}$ | | 42 / 36(1) | | dB |
| Selectivity, ±5 MHz or more(3) | Wanted signal at –67 dBm, modulated interferer at ≥ ±5 MHz, BER = $10^{-3}$ | | 32 | | dB |
| Selectivity, Image frequency(3) | Wanted signal at –67 dBm, modulated interferer at image frequency, BER = $10^{-3}$ | | 17 | | dB |
| Selectivity, Image frequency ±1 MHz(3) | Wanted signal at –67 dBm, modulated interferer at ±1 MHz from image frequency, BER = $10^{-3}$ | | 2 / 30(1) | | dB |
| Out-of-band blocking (4) | 30 MHz to 2000 MHz | | –20 | | dBm |
| Out-of-band blocking | 2003 MHz to 2399 MHz | | –5 | | dBm |
| Out-of-band blocking | 2484 MHz to 2997 MHz | | –8 | | dBm |
| Out-of-band blocking | 3000 MHz to 12.75 GHz | | –8 | | dBm |
| Intermodulation | Wanted signal at 2402 MHz, –64 dBm. Two interferers at 2405 and 2408 MHz respectively, at the given power level | | –34 | | dBm |
| Spurious emissions, 30 MHz to 1000 MHz | Conducted measurement in a 50-Ω single-ended load. Suitable for systems targeting compliance with EN 300 328, EN 300 440, FCC CFR47, Part 15 and ARIB STD-T-66 | | –65 | | dBm |
| Spurious emissions, 1 GHz to 12.75 GHz | Conducted measurement in a 50-Ω single-ended load. Suitable for systems targeting compliance with EN 300 328, EN 300 440, FCC CFR47, Part 15 and ARIB STD-T-66 | | –52 | | dBm |
| RSSI dynamic range | | | 70 | | dB |
| RSSI accuracy | | | ±4 | | dB |

(1) X / Y, where X is +N MHz and Y is –N MHz.
(2) +2MHz selectivity is reduced to 33dB when using radio FW supporting 2Mbps and Coded PHYs
(3) Numbers given as I/C dB.
(4) Excluding one exception at $F_{wanted}$ / 2, per Bluetooth Specification.

## 8.7 1-Mbps GFSK (Bluetooth low energy Technology) – TX

Measured on the TI CC2640Q1EM-7ID reference design with $T_c$ = 25°C, $V_{DDS}$ = 3.0 V, $f_{RF}$ = 2440 MHz, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Output power, highest setting | Differential mode, delivered to a single-ended 50-Ω load through a balun | | 5 | | dBm |
| Output power, lowest setting | Delivered to a single-ended 50-Ω load through a balun | | –21 | | dBm |
| Spurious emission conducted measurement(1) | f < 1 GHz, outside restricted bands | | –44 | | dBm |
| | f < 1 GHz, restricted bands ETSI | | –62 | | dBm |
| | f < 1 GHz, restricted bands FCC | | –62 | | dBm |
| | f > 1 GHz, including harmonics | | –55 | | dBm |

(1) Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan).

## 8.8 24-MHz Crystal Oscillator (XOSC_HF)

$T_c$ = 25°C, $V_{DDS}$ = 3.0 V, unless otherwise noted.(1)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| ESR Equivalent series resistance(2) | 6 pF < $C_L$ ≤ 9 pF | | 20 | 60 | Ω |
| ESR Equivalent series resistance(2) | 5 pF < $C_L$ ≤ 6 pF | | | 80 | Ω |
| $L_M$ Motional inductance(2) | Relates to load capacitance ($C_L$ in Farads) | | < 1.6 × $10^{-24}$ / $C_L$ $^2$ | | H |
| $C_L$ Crystal load capacitance(2) | | 5 | | 9 | pF |
| Crystal frequency(2) (3) | | | 24 | | MHz |
| Crystal frequency tolerance(2) (4) | | –40 | | 40 | ppm |
| Start-up time(3) (5) | | | 150 | | µs |

(1) Probing or otherwise stopping the crystal while the DC/DC converter is enabled may cause permanent damage to the device.
(2) The crystal manufacturer's specification must satisfy this requirement
(3) Measured on the TI CC2640Q1EM-7ID reference design with $T_c$ = 25°C, $V_{DDS}$ = 3.0 V
(4) Includes initial tolerance of the crystal, drift over temperature, ageing and frequency pulling due to incorrect load capacitance, as per Bluetooth specification.
(5) Kick-started based on a temperature and aging compensated RCOSC_HF using precharge injection.

## 8.9 32.768-kHz Crystal Oscillator (XOSC_LF)

$T_c$ = 25°C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Crystal frequency(1) | | | 32.768 | | kHz |
| Crystal frequency tolerance, Bluetooth low-energy applications(1) (2) | | –500 | | 500 | ppm |
| ESR Equivalent series resistance(1) | | | 30 | 100 | kΩ |
| $C_L$ Crystal load capacitance(1) | | 6 | | 12 | pF |

(1) The crystal manufacturer's specification must satisfy this requirement.
(2) Includes initial tolerance of the crystal, drift over temperature, ageing and frequency pulling due to incorrect load capacitance, as per Bluetooth specification.

## 8.10 48-MHz RC Oscillator (RCOSC_HF)

Measured on the TI CC2640Q1EM-7ID reference design with $T_c$ = 25°C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Frequency | | | 48 | | MHz |
| Uncalibrated frequency accuracy | | | ±1% | | |
| Calibrated frequency accuracy(1) | | | ±0.25% | | |
| Start-up time | | | 5 | | µs |

(1) Accuracy relative to the calibration source (XOSC_HF).

## 8.11 32-kHz RC Oscillator (RCOSC_LF)

Measured on the TI CC2640Q1EM-7ID reference design with $T_c$ = 25°C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Calibrated frequency(1) | | | 32.8 | | kHz |
| Temperature coefficient | | | 50 | | ppm/°C |

(1) The frequency accuracy of the real time clock (RTC) is not directly dependent on the frequency accuracy of the 32-kHz RC oscillator. The RTC can be calibrated by measuring the frequency error of RCOSC_LF relative to XOSC_HF and compensating the RTC tick speed.

## 8.12 ADC Characteristics

$T_c$ = 25°C, $V_{DDS}$ = 3.0 V without internal DC/DC converter and with voltage scaling enabled, unless otherwise noted.(1)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| | Input voltage range | | 0 | | VDDS | V |
| | Resolution | | | 12 | | Bits |
| | Sample rate | | | | 200 | ksps |
| | Offset | Internal 4.3-V equivalent reference(2) | | 2 | | LSB |
| | Gain error | Internal 4.3-V equivalent reference(2) | | 2.4 | | LSB |
| DNL(3) | Differential nonlinearity | | | >–1 | | LSB |
| INL(4) | Integral nonlinearity | | | ±3 | | LSB |
| ENOB | Effective number of bits | Internal 4.3-V equivalent reference(2), 200 ksps, 9.6-kHz input tone | | 9.8 | | Bits |
| | | VDDS as reference, 200 ksps, 9.6-kHz input tone | | 10 | | |
| | | Internal 1.44-V reference, voltage scaling disabled, 32 samples average, 200 ksps, 300-Hz input tone | | 11.1 | | |
| THD | Total harmonic distortion | Internal 4.3-V equivalent reference(2), 200 ksps, 9.6-kHz input tone | | –65 | | dB |
| | | VDDS as reference, 200 ksps, 9.6-kHz input tone | | –69 | | |
| | | Internal 1.44-V reference, voltage scaling disabled, 32 samples average, 200 ksps, 300-Hz input tone | | –71 | | |
| SINAD, SNDR | Signal-to-noise and Distortion ratio | Internal 4.3-V equivalent reference(2), 200 ksps, 9.6-kHz input tone | | 60 | | dB |
| | | VDDS as reference, 200 ksps, 9.6-kHz input tone | | 63 | | |
| | | Internal 1.44-V reference, voltage scaling disabled, 32 samples average, 200 ksps, 300-Hz input tone | | 69 | | |
| SFDR | Spurious-free dynamic range | Internal 4.3-V equivalent reference(2), 200 ksps, 9.6-kHz input tone | | 67 | | dB |
| | | VDDS as reference, 200 ksps, 9.6-kHz input tone | | 72 | | |
| | | Internal 1.44-V reference, voltage scaling disabled, 32 samples average, 200 ksps, 300-Hz input tone | | 73 | | |
| | Conversion time | Serial conversion, time-to-output, 24-MHz clock | | 50 | | clock-cycles |

$T_c$ = 25°C, $V_{DDS}$ = 3.0 V without internal DC/DC converter and with voltage scaling enabled, unless otherwise noted.(1)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Current consumption | Internal 4.3-V equivalent reference(2) | | 0.66 | | mA |
| Current consumption | VDDS as reference | | 0.75 | | mA |
| Reference voltage | Equivalent fixed internal reference (input voltage scaling enabled). For best accuracy, the ADC conversion should be initiated through the TI-RTOS API to include the gain/offset compensation factors stored in FCFG1. | | 4.3(2) (5) | | V |
| Reference voltage | Fixed internal reference (input-voltage scaling disabled). For the best accuracy, the ADC conversion should be initiated through the TI-RTOS API to include the gain/offset compensation factors stored in FCFG1. This value is derived from the scaled value (4.3 V) as follows. $V_{ref}$ = 4.3 V × 1408 / 4095 | | 1.48 | | V |
| Reference voltage | VDDS as reference (also known as *RELATIVE*) (input voltage scaling enabled) | | VDDS | | V |
| Reference voltage | VDDS as reference (also known as *RELATIVE*) (input voltage scaling disabled) | | VDDS / 2.82(5) | | V |
| Input Impedance | 200 ksps, voltage scaling enabled. Capacitive input, input impedance depends on sampling frequency and sampling time | | >1 | | MΩ |

(1) Using IEEE Std 1241™-2010 for terminology and test methods.
(2) Input signal scaled down internally before conversion, as if voltage range was 0 to 4.3 V.
(3) No missing codes. Positive DNL typically varies from +0.3 to +3.5, depending on device (see 図 8-21).
(4) For a typical example, see 図 8-22.
(5) Applied voltage must be within absolute maximum ratings at all times (see セクション 8.1).

## 8.13 Temperature Sensor

Measured on the TI CC2640Q1EM-7ID reference design with $T_c$ = 25°C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Resolution | | | 4 | | °C |
| Range | | –40 | | 105 | °C |
| Accuracy | | | ±5 | | °C |
| Supply voltage coefficient(1) | | | 3.2 | | °C/V |

(1) Automatically compensated when using supplied driver libraries.

## 8.14 Battery Monitor

Measured on the TI CC2640Q1EM-7ID reference design with $T_c$ = 25°C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Resolution | | | 50 | | mV |
| Range | | 1.8 | | 3.8 | V |
| Accuracy | | | 13 | | mV |

## 8.15 Continuous Time Comparator

$T_c$ = 25°C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Input voltage range | | 0 | | VDDS | V |
| External reference voltage | | 0 | | VDDS | V |
| Internal reference voltage | DCOUPL as reference | | 1.27 | | V |
| Offset | | | 3 | | mV |
| Hysteresis | | | <2 | | mV |
| Decision time | Step from –10 mV to 10 mV | | 0.72 | | µs |

$T_c$ = 25°C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Current consumption when enabled(1) | | | 8.6 | | µA |

(1) Additionally, the bias module must be enabled when running in standby mode.

## 8.16 Low-Power Clocked Comparator

$T_c$ = 25°C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Input voltage range | | 0 | | VDDS | V |
| Clock frequency | | | 32 | | kHz |
| Internal reference voltage, VDDS / 2 | | | 1.49–1.51 | | V |
| Internal reference voltage, VDDS / 3 | | | 1.01–1.03 | | V |
| Internal reference voltage, VDDS / 4 | | | 0.78–0.79 | | V |
| Internal reference voltage, DCOUPL / 1 | | | 1.25–1.28 | | V |
| Internal reference voltage, DCOUPL / 2 | | | 0.63–0.65 | | V |
| Internal reference voltage, DCOUPL / 3 | | | 0.42–0.44 | | V |
| Internal reference voltage, DCOUPL / 4 | | | 0.33–0.34 | | V |
| Offset | | | <2 | | mV |
| Hysteresis | | | <5 | | mV |
| Decision time | Step from –50 mV to 50 mV | | <1 | | clock-cycle |
| Current consumption when enabled | | | 362 | | nA |

## 8.17 Programmable Current Source

$T_c$ = 25°C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Current source programmable output range | | | 0.25–20 | | µA |
| Resolution | | | 0.25 | | µA |
| Current consumption(1) | Including current source at maximum programmable output | | 23 | | µA |

(1) Additionally, the bias module must be enabled when running in standby mode.

## 8.18 Synchronous Serial Interface (SSI)

$T_c$ = 25°C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| S1(1) $t_{clk\_per}$ (SSIClk period) | Device operating as SLAVE | 12 | | 65024 | system clocks |
| S2(1) $t_{clk\_high}$ (SSIClk high time) | Device operating as SLAVE | | 0.5 | | $t_{clk\_per}$ |
| S3(1) $t_{clk\_low}$ (SSIClk low time) | Device operating as SLAVE | | 0.5 | | $t_{clk\_per}$ |
| S1 (TX only)(1) $t_{clk\_per}$ (SSIClk period) | One-way communication to SLAVE: Device operating as MASTER | 4 | | 65024 | system clocks |
| S1 (TX and RX)(1) $t_{clk\_per}$ (SSIClk period) | Normal duplex operation: Device operating as MASTER | 8 | | 65024 | system clocks |
| S2(1) $t_{clk\_high}$ (SSIClk high time) | Device operating as MASTER | | 0.5 | | $t_{clk\_per}$ |
| S3(1) $t_{clk\_low}$(SSIClk low time) | Device operating as MASTER | | 0.5 | | $t_{clk\_per}$ |

(1) Refer to SSI timing diagrams 図 8-1, 図 8-2, and 図 8-3.

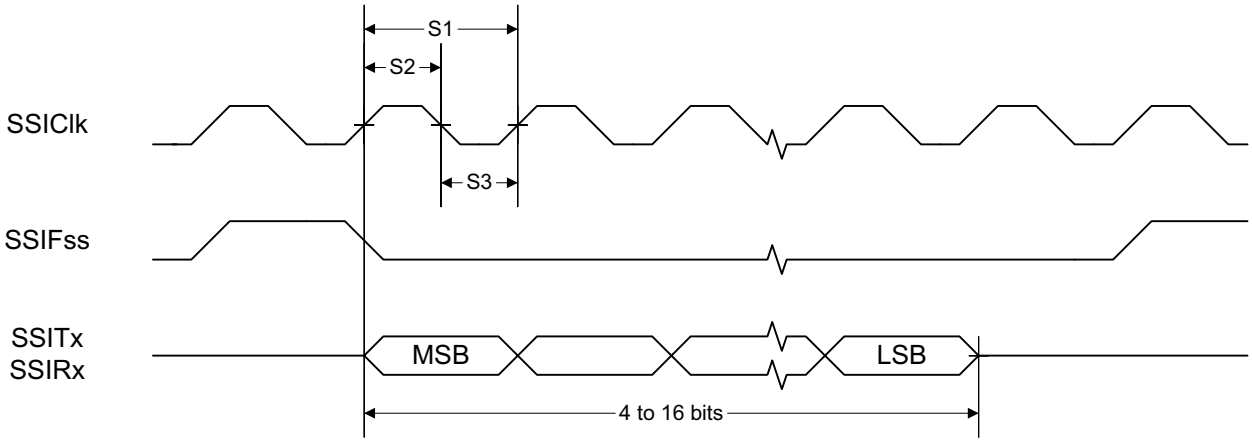



**図 8-1. SSI Timing for TI Frame Format (FRF = 01), Single Transfer Timing Measurement**

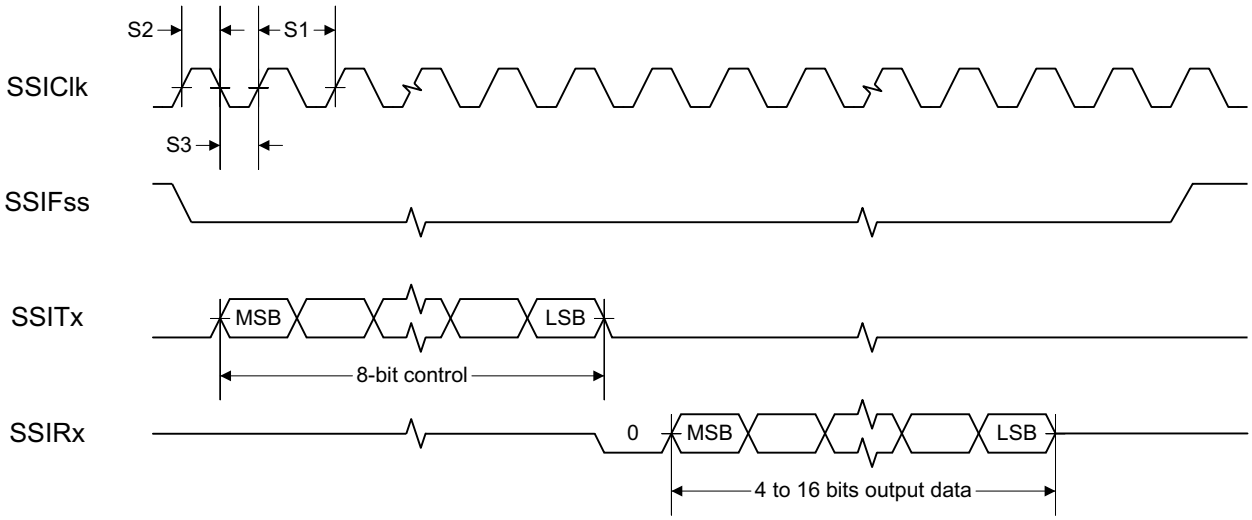



**図 8-2. SSI Timing for MICROWIRE Frame Format (FRF = 10), Single Transfer**

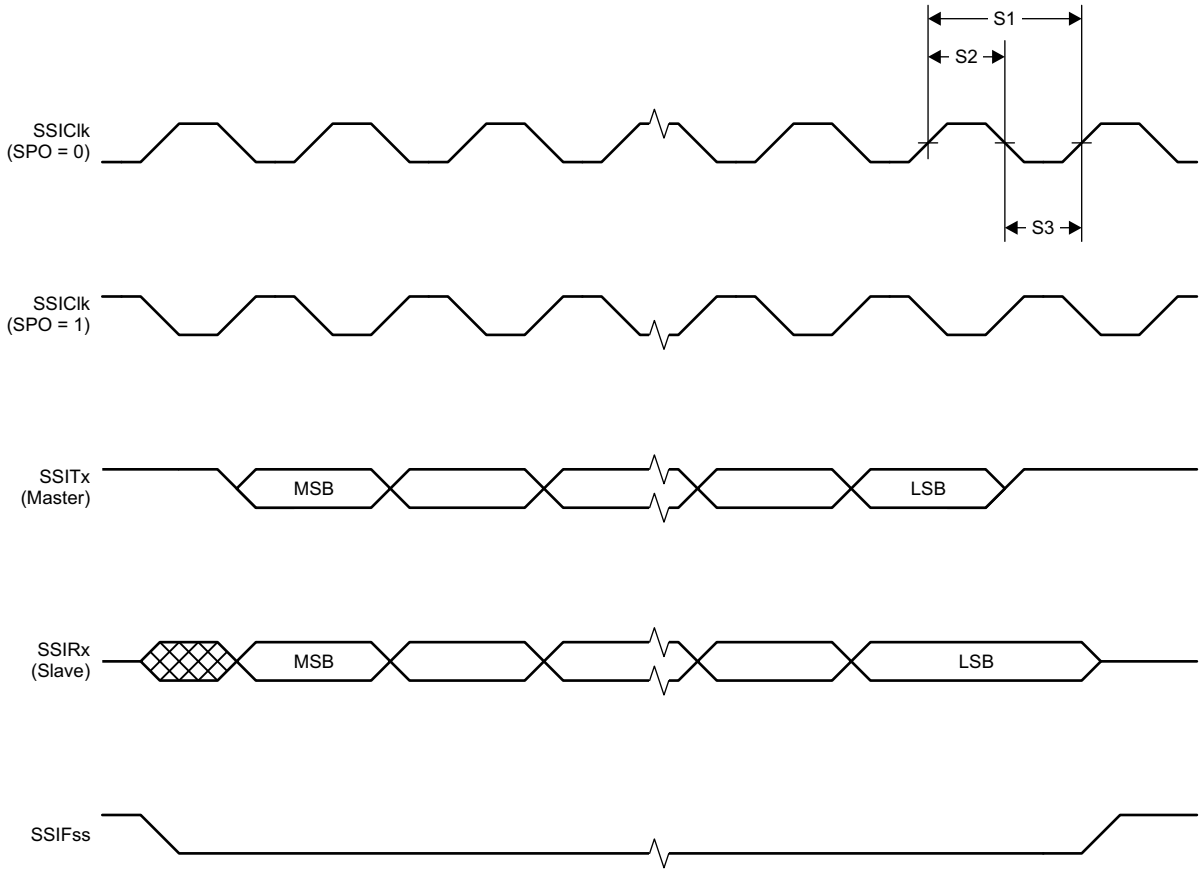



**図 8-3. SSI Timing for SPI Frame Format (FRF = 00), With SPH = 1**

## 8.19 DC Characteristics

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **$T_A$ = 25°C, $V_{DDS}$ = 1.8 V** | | | | | |
| GPIO $V_{OH}$ at 8-mA load | IOCURR = 2, high-drive GPIOs only | 1.32 | 1.54 | | V |
| GPIO $V_{OL}$ at 8-mA load | IOCURR = 2, high-drive GPIOs only | | 0.26 | 0.32 | V |
| GPIO $V_{OH}$ at 4-mA load | IOCURR = 1 | 1.32 | 1.58 | | V |
| GPIO $V_{OL}$ at 4-mA load | IOCURR = 1 | | 0.21 | 0.32 | V |
| GPIO pullup current | Input mode, pullup enabled, $V_{(pad)}$ = 0 V | | 71.7 | | µA |
| GPIO pulldown current | Input mode, pulldown enabled, $V_{(pad)}$ = VDDS | | 21.1 | | µA |
| GPIO high/low input transition, no hysteresis | $I_H$ = 0, transition between reading 0 and reading 1 | | 0.88 | | V |
| GPIO low-to-high input transition, with hysteresis | $I_H$ = 1, transition voltage for input read as 0 → 1 | | 1.07 | | V |
| GPIO high-to-low input transition, with hysteresis | $I_H$ = 1, transition voltage for input read as 1 → 0 | | 0.74 | | V |
| GPIO input hysteresis | $I_H$ = 1, difference between 0 → 1 and 1 → 0 points | | 0.33 | | V |

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **$T_A$ = 25°C, $V_{DDS}$ = 3.0 V** | | | | | |
| GPIO $V_{OH}$ at 8-mA load | IOCURR = 2, high-drive GPIOs only | | 2.68 | | V |
| GPIO $V_{OL}$ at 8-mA load | IOCURR = 2, high-drive GPIOs only | | 0.33 | | V |
| GPIO $V_{OH}$ at 4-mA load | IOCURR = 1 | | 2.72 | | V |
| GPIO $V_{OL}$ at 4-mA load | IOCURR = 1 | | 0.28 | | V |
| **$T_A$ = 25°C, $V_{DDS}$ = 3.8 V** | | | | | |
| GPIO pullup current | Input mode, pullup enabled, $V_{(pad)}$ = 0 V | | 277 | | µA |
| GPIO pulldown current | Input mode, pulldown enabled, $V_{(pad)}$ = VDDS | | 113 | | µA |
| GPIO high/low input transition, no hysteresis | $I_H$ = 0, transition between reading 0 and reading 1 | | 1.67 | | V |
| GPIO low-to-high input transition, with hysteresis | $I_H$ = 1, transition voltage for input read as 0 → 1 | | 1.94 | | V |
| GPIO high-to-low input transition, with hysteresis | $I_H$ = 1, transition voltage for input read as 1 → 0 | | 1.54 | | V |
| GPIO input hysteresis | $I_H$ = 1, difference between 0 → 1 and 1 → 0 points | | 0.4 | | V |
| **$T_A$ = 25°C** | | | | | |
| $V_{(IH)}$ | Lowest GPIO input voltage reliably interpreted as a «High» | | | 0.8 | VDDS(1) |
| $V_{(IL)}$ | Highest GPIO input voltage reliably interpreted as a «Low» | 0.2 | | | VDDS(1) |

(1) Each GPIO is referenced to a specific VDDS pin. See the technical reference manual listed in セクション 11.3 for more details.

## 8.20 Thermal Resistance Characteristics for RGZ Package

over operating free-air temperature range (unless otherwise noted)

| NAME | DESCRIPTION | (°C/W)(1) (2) |
|---|---|---|
| $R\theta_{JA}$ | Junction-to-ambient thermal resistance | 29.6 |
| $R\theta_{JC(top)}$ | Junction-to-case (top) thermal resistance | 15.7 |
| $R\theta_{JB}$ | Junction-to-board thermal resistance | 6.2 |
| $Psi_{JT}$ | Junction-to-top characterization parameter | 0.3 |
| $Psi_{JB}$ | Junction-to-board characterization parameter | 6.2 |
| $R\theta_{JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 1.9 |

(1) °C/W = degrees Celsius per watt.
(2) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see the following EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

Power dissipation of 2 W and an ambient temperature of 70°C is assumed.

## 8.21 Timing Requirements

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Rising supply-voltage slew rate | | 0 | | 100 | mV/µs |
| Falling supply-voltage slew rate | | 0 | | 20 | mV/µs |
| Falling supply-voltage slew rate, with low-power flash settings(1) | | | | 3 | mV/µs |
| Positive temperature gradient in standby(3) | No limitation for negative temperature gradient, or outside standby mode | | | 5 | °C/s |
| **CONTROL INPUT AC CHARACTERISTICS**(2) | | | | | |
| RESET_N low duration | | 1 | | | µs |

(1) For smaller coin cell batteries, with high worst-case end-of-life equivalent source resistance, a 22-µF VDDS input capacitor (see 図 10-1) must be used to ensure compliance with this slew rate.
(2) $T_A$ = –40°C to +105°C, $V_{DDS}$ = 1.8 V to 3.8 V, unless otherwise noted.
(3) Applications using RCOSC_LF as sleep timer must also consider the drift in frequency caused by a change in temperature (see セクション 8.11).

## 8.22 Switching Characteristics

Measured on the TI CC2640Q1EM-7ID reference design with $T_c$ = 25°C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **WAKEUP and TIMING** | | | | | |
| Idle → Active | | | 14 | | µs |
| Standby → Active | | | 151 | | µs |
| Shutdown → Active | | | 1015 | | µs |

## 8.23 Typical Characteristics

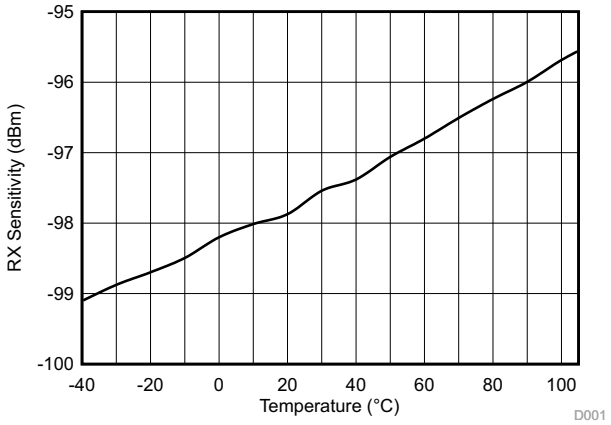



**図 8-4. Bluetooth low energy Sensitivity vs Temperature**

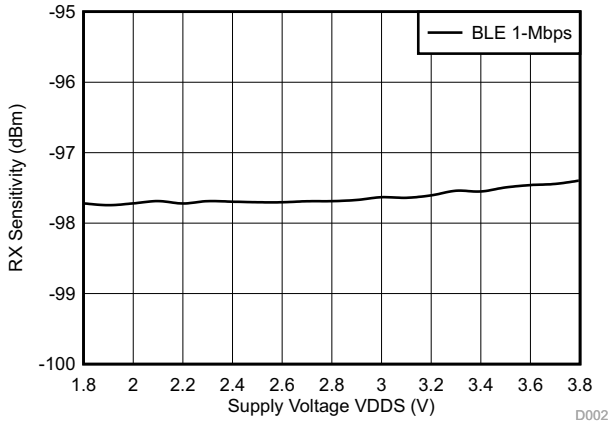



**図 8-5. Bluetooth low energy Sensitivity vs Supply Voltage (VDDS)**

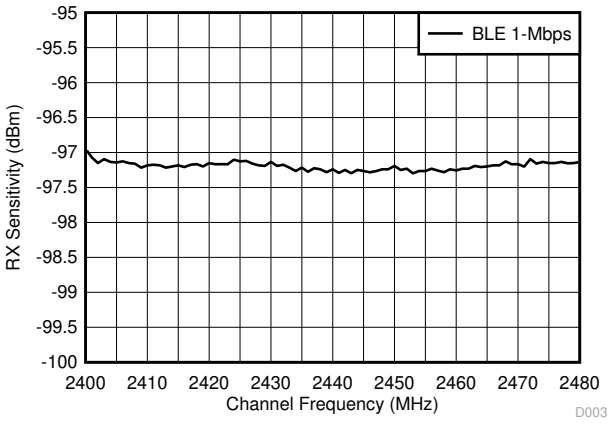



**図 8-6. Bluetooth low energy Sensitivity vs Channel Frequency**

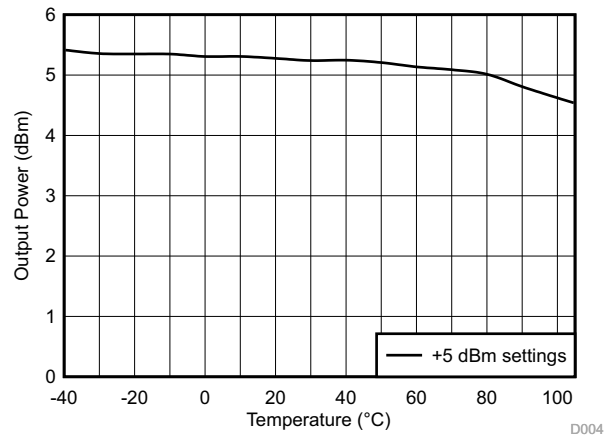



**図 8-7. TX Output Power vs Temperature**

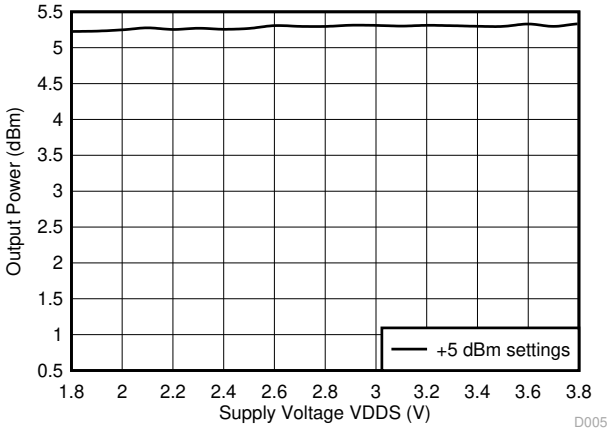



**図 8-8. TX Output Power vs Supply Voltage (VDDS)**

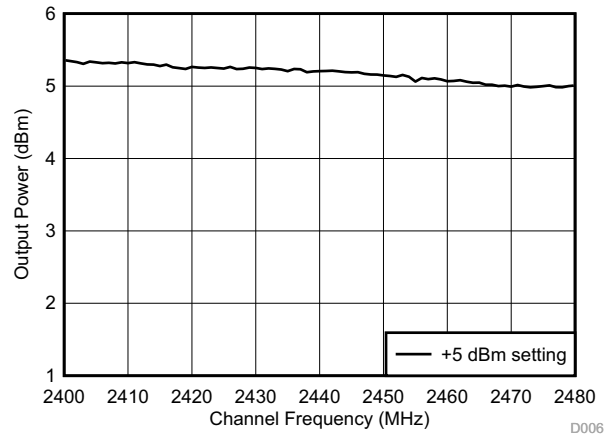



**図 8-9. TX Output Power vs Channel Frequency**

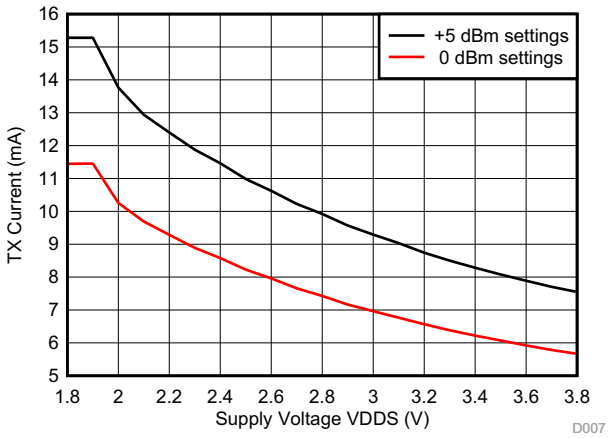



**図 8-10. TX Current Consumption vs Supply Voltage (VDDS)**

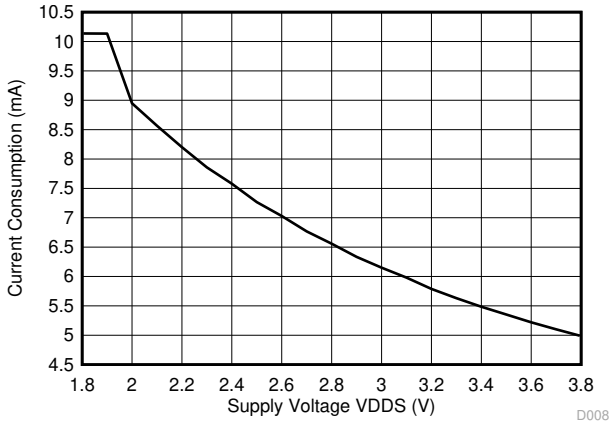



**図 8-11. RX Mode Current vs Supply Voltage (VDDS)**

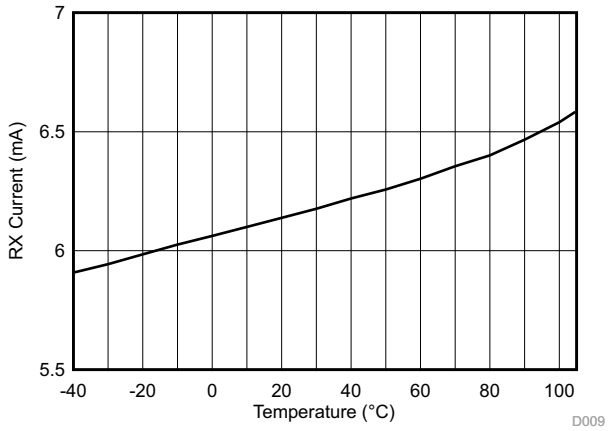



**図 8-12. RX Mode Current Consumption vs Temperature**

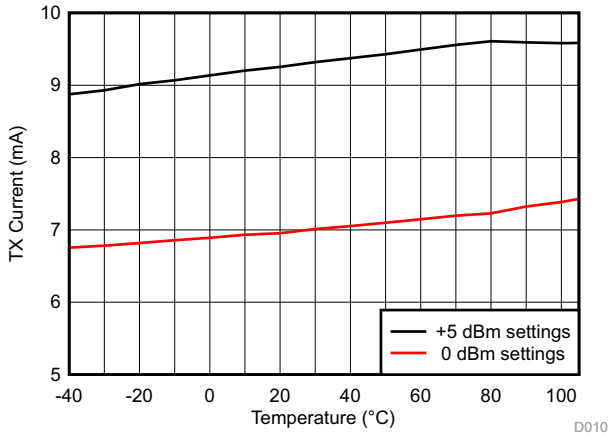



**図 8-13. TX Mode Current Consumption vs Temperature**

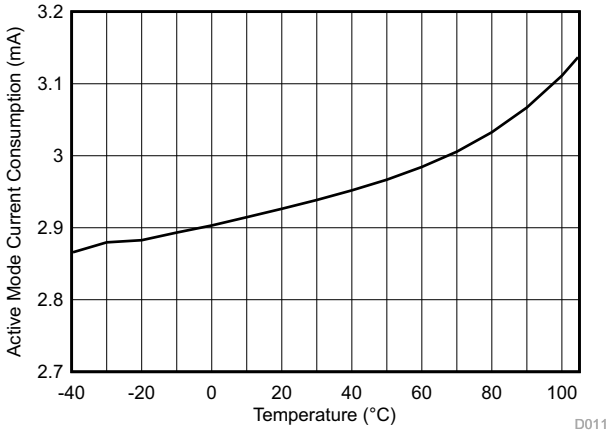



**図 8-14. Active Mode (MCU Running, No Peripherals) Current Consumption vs Temperature**

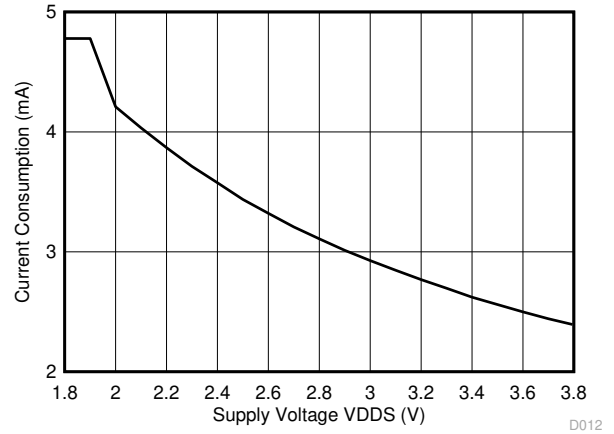



**図 8-15. Active Mode (MCU Running, No Peripherals) Current Consumption vs Supply Voltage (VDDS)**

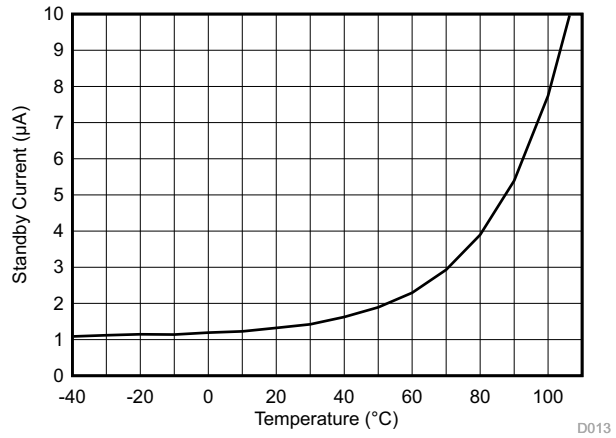



**図 8-16. Standby Mode Current Consumption vs Temperature**

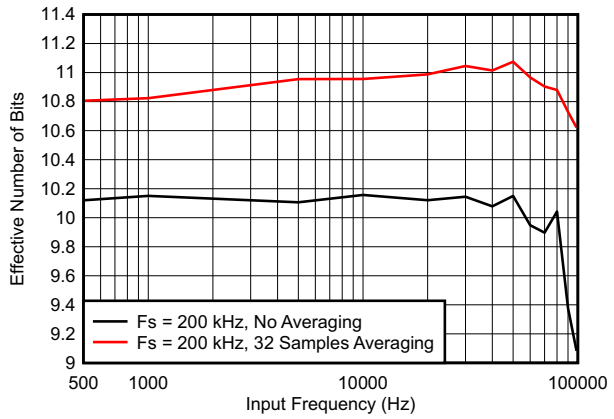



**図 8-17. SoC ADC Effective Number of Bits vs Input Frequency (Internal Reference, No Scaling)**

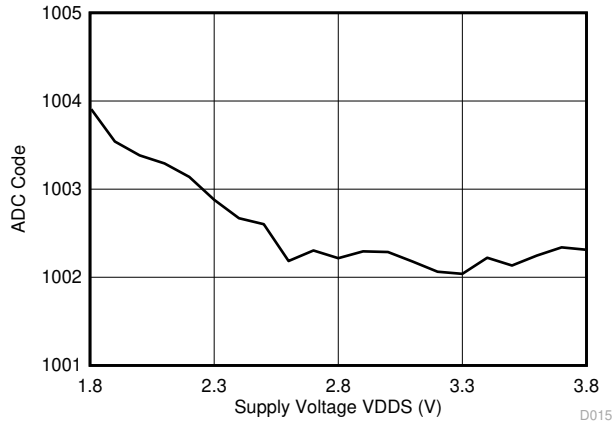



**図 8-18. SoC ADC Output vs Supply Voltage (Fixed Input, Internal Reference, No Scaling)**

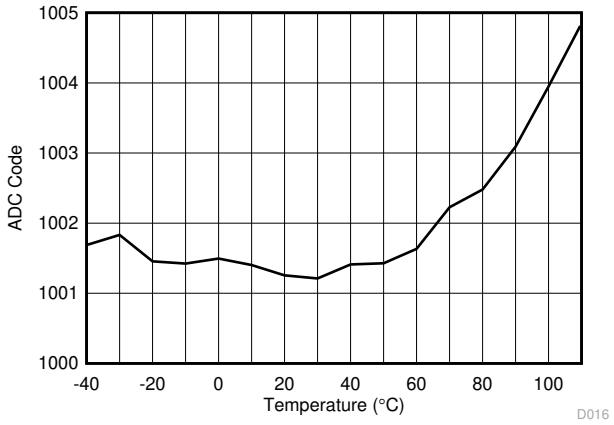



**図 8-19. SoC ADC Output vs Temperature (Fixed Input, Internal Reference, No Scaling)**

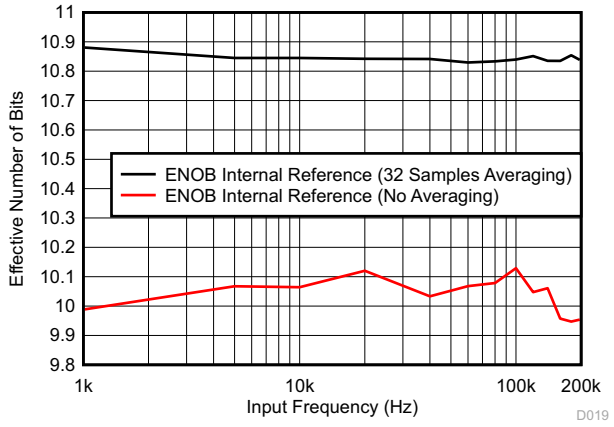



**図 8-20. SoC ADC ENOB vs Sampling Frequency (Input Frequency = FS / 10)**

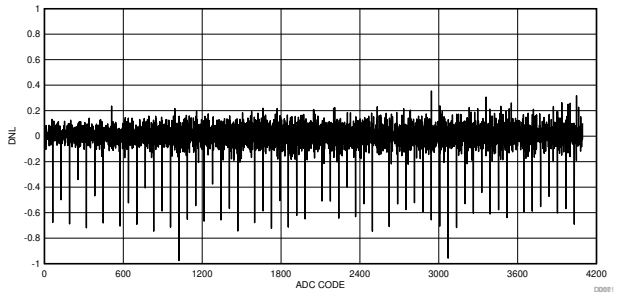



**図 8-21. SoC ADC DNL vs ADC Code (Internal Reference, No Scaling)**

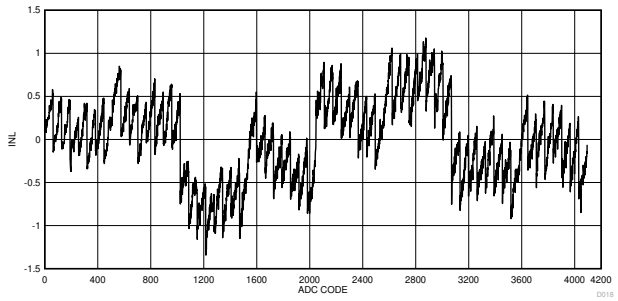



**図 8-22. SoC ADC INL vs ADC Code (Internal Reference, No Scaling)**

# 9 Detailed Description

## 9.1 Overview

セクション 4 shows the core modules of the CC26xx product family.

## 9.2 Main CPU

The automotive grade SimpleLink™ CC2640R2F-Q1 Wireless MCU contains an Arm® Cortex®-M3 (CM3) 32-bit CPU, which runs the application and the higher layers of the protocol stack.

The Cortex®-M3 processor provides a high-performance, low-cost platform that meets the system requirements of minimal memory implementation, and low-power consumption, while delivering outstanding computational performance and exceptional system response to interrupts.

Cortex-M3 features include the following:

- 32-bit Arm® Cortex®-M3 architecture optimized for small-footprint embedded applications
- Outstanding processing performance combined with fast interrupt handling
- Arm Thumb®-2 mixed 16- and 32-bit instruction set delivers the high performance expected of a 32-bit Arm core in a compact memory size usually associated with 8- and 16-bit devices, typically in the range of a few kilobytes of memory for microcontroller-class applications:
  - Single-cycle multiply instruction and hardware divide
  - Atomic bit manipulation (bit-banding), delivering maximum memory use and streamlined peripheral control
  - Unaligned data access, enabling data to be efficiently packed into memory
- Fast code execution permits slower processor clock or increases sleep mode time
- Harvard architecture characterized by separate buses for instruction and data
- Efficient processor core, system, and memories
- Hardware division and fast digital-signal-processing oriented multiply accumulate
- Saturating arithmetic for signal processing
- Deterministic, high-performance interrupt handling for time-critical applications
- Enhanced system debug with extensive breakpoint and trace capabilities
- Serial wire trace reduces the number of pins required for debugging and tracing
- Migration from the ARM7™ processor family for better performance and power efficiency
- Optimized for single-cycle flash memory use
- Ultra-low power consumption with integrated sleep modes
- 1.25 DMIPS per MHz

## 9.3 RF Core

The RF Core contains an Arm Cortex-M0 processor that interfaces the analog RF and base-band circuitries, handles data to and from the system side, and assembles the information bits in a given packet structure. The RF core offers a high level, command-based API to the main CPU.

The RF core is capable of autonomously handling the time-critical aspects of the radio protocols (*Bluetooth* ® low energy) thus offloading the main CPU and leaving more resources for the user application.

The RF core has a dedicated 4-KB SRAM block and runs initially from separate ROM memory. The Arm Cortex-M0 processor is not programmable by customers.

## 9.4 Sensor Controller

The Sensor Controller contains circuitry that can be selectively enabled in standby mode. The peripherals in this domain may be controlled by the Sensor Controller Engine, which is a proprietary power-optimized CPU. This CPU can read and monitor sensors or perform other tasks autonomously, thereby significantly reducing power consumption and offloading the main Cortex-M3 CPU.

The Sensor Controller is set up using a PC-based configuration tool, called Sensor Controller Studio, and potential use cases may be (but are not limited to):

- Analog sensors using integrated ADC
- Digital sensors using GPIOs, bit-banged $I^2C$, and SPI
- UART communication for sensor reading or debugging
- Capacitive sensing
- Waveform generation
- Pulse counting
- Keyboard scan
- Quadrature decoder for polling rotation sensors
- Oscillator calibration

注

Texas Instruments provides application examples for some of these use cases, but not for all of them.

The peripherals in the Sensor Controller include the following:

- The low-power clocked comparator can be used to wake the device from any state in which the comparator is active. A configurable internal reference can be used in conjunction with the comparator. The output of the comparator can also be used to trigger an interrupt or the ADC.
- Capacitive sensing functionality is implemented through the use of a constant current source, a time-to-digital converter, and a comparator. The continuous time comparator in this block can also be used as a higher-accuracy alternative to the low-power clocked comparator. The Sensor Controller will take care of baseline tracking, hysteresis, filtering and other related functions.
- The ADC is a 12-bit, 200-ksamples/s ADC with eight inputs and a built-in voltage reference. The ADC can be triggered by many different sources, including timers, I/O pins, software, the analog comparator, and the RTC.
- The Sensor Controller also includes a SPI–$I^2C$ digital interface.
- The analog modules can be connected to up to eight different GPIOs.

The peripherals in the Sensor Controller can also be controlled from the main application processor.

**表 9-1. GPIOs Connected to the Sensor Controller(1)**

| ANALOG CAPABLE | 7 × 7 RGZ DIO NUMBER |
|---|---|
| Y | 30 |
| Y | 29 |
| Y | 28 |
| Y | 27 |
| Y | 26 |
| Y | 25 |
| Y | 24 |
| Y | 23 |
| N | 7 |
| N | 6 |
| N | 5 |
| N | 4 |
| N | 3 |
| N | 2 |
| N | 1 |
| N | 0 |

(1) Up to 16 pins can be connected to the Sensor Controller. Up to 8 of these pins can be connected to analog modules.

## 9.5 Memory

The flash memory provides nonvolatile storage for code and data. The flash memory is in-system programmable.

The SRAM (static RAM) can be used for both storage of data and execution of code and is split into two 4-KB blocks and two 6-KB blocks. Retention of the RAM contents in standby mode can be enabled or disabled individually for each block to minimize power consumption. In addition, if flash cache is disabled, the 8-KB cache can be used as a general-purpose RAM.

The ROM provides preprogrammed embedded TI-RTOS kernel, Driver Library, and lower layer protocol stack software (*Bluetooth* ® low energy Controller). It also contains a bootloader that can be used to reprogram the device using SPI or UART.

## 9.6 Debug

The on-chip debug support is done through a dedicated cJTAG (IEEE 1149.7) or JTAG (IEEE 1149.1) interface.

## 9.7 Power Management

To minimize power consumption, the CC2640R2F-Q1 device supports a number of power modes and power management features (see 表 9-2).

**表 9-2. Power Modes**

| MODE | SOFTWARE CONFIGURABLE POWER MODES | | | | RESET PIN HELD |
|---|---|---|---|---|---|
| | ACTIVE | IDLE | STANDBY | SHUTDOWN | |
| **CPU** | Active | Off | Off | Off | Off |
| **Flash** | On | Available | Off | Off | Off |
| **SRAM** | On | On | On | Off | Off |
| **Radio** | Available | Available | Off | Off | Off |
| **Supply System** | On | On | Duty Cycled | Off | Off |
| Current | 1.45 mA + 31 µA/MHz | 650 µA | 1.3 µA | 0.15 µA | 0.1 µA |
| Wake-up Time to CPU Active(1) | – | 14 µs | 151 µs | 1015 µs | 1015 µs |
| Register Retention | Full | Full | Partial | No | No |
| SRAM Retention | Full | Full | Full | No | No |
| High-Speed Clock | XOSC_HF or RCOSC_HF | XOSC_HF or RCOSC_HF | Off | Off | Off |
| Low-Speed Clock | XOSC_LF or RCOSC_LF | XOSC_LF or RCOSC_LF | XOSC_LF or RCOSC_LF | Off | Off |
| Peripherals | Available | Available | Off | Off | Off |
| Sensor Controller | Available | Available | Available | Off | Off |
| Wake up on RTC | Available | Available | Available | Off | Off |
| Wake up on Pin Edge | Available | Available | Available | Available | Off |
| Wake up on Reset Pin | Available | Available | Available | Available | Available |
| Brown Out Detector (BOD) | Active | Active | Duty Cycled | Off | N/A |
| Power On Reset (POR) | Active | Active | Active | Active | N/A |

(1) Not including RTOS overhead

In active mode, the application Cortex-M3 CPU is actively executing code. Active mode provides normal operation of the processor and all of the peripherals that are currently enabled. The system clock can be any available clock source (see 表 9-2).

In idle mode, all active peripherals can be clocked, but the Application CPU core and memory are not clocked and no code is executed. Any interrupt event will bring the processor back into active mode.

In standby mode, only the always-on domain (AON) is active. An external wake event, RTC event, or sensor-controller event is required to bring the device back to active mode. MCU peripherals with retention do not need to be reconfigured when waking up again, and the CPU continues execution from where it went into standby mode. All GPIOs are latched in standby mode.

In shutdown mode, the device is turned off entirely, including the AON domain and the Sensor Controller. The I/Os are latched with the value they had before entering shutdown mode. A change of state on any I/O pin defined as a *wake from Shutdown pin* wakes up the device and functions as a reset trigger. The CPU can differentiate between a reset in this way, a reset-by-reset pin, or a power-on-reset by reading the reset status register. The only state retained in this mode is the latched I/O state and the Flash memory contents.

The Sensor Controller is an autonomous processor that can control the peripherals in the Sensor Controller independently of the main CPU, which means that the main CPU does not have to wake up, for example, to execute an ADC sample or poll a digital sensor over SPI. The main CPU saves both current and wake-up time that would otherwise be wasted. The Sensor Controller Studio enables the user to configure the sensor controller and choose which peripherals are controlled and which conditions wake up the main CPU.

## 9.8 Clock Systems

The CC2640R2F-Q1 device supports two external and two internal clock sources.

A 24-MHz crystal is required as the frequency reference for the radio. This signal is doubled internally to create a 48-MHz clock.

The 32-kHz crystal is optional. *Bluetooth* ® low energy requires a slow-speed clock with better than ±500 ppm accuracy if the device is to enter any sleep mode while maintaining a connection. The internal 32-kHz RC oscillator can in some use cases be compensated to meet the requirements. The low-speed crystal oscillator is designed for use with a 32-kHz watch-type crystal.

The internal high-speed oscillator (48-MHz) can be used as a clock source for the CPU subsystem.

The internal low-speed oscillator (32.768-kHz) can be used as a reference if the low-power crystal oscillator is not used.

The 32-kHz clock source can be used as external clocking reference through GPIO.

## 9.9 General Peripherals and Modules

The I/O controller controls the digital I/O pins and contains multiplexer circuitry to allow a set of peripherals to be assigned to I/O pins in a flexible manner. All digital I/Os are interrupt and wake-up capable, have a programmable pullup and pulldown function and can generate an interrupt on a negative or positive edge (configurable). When configured as an output, pins can function as either push-pull or open-drain. Five GPIOs have high drive capabilities (marked in **bold** in セクション 7).

The SSIs are synchronous serial interfaces that are compatible with SPI, MICROWIRE, and synchronous serial interfaces from Texas Instruments™. The SSIs support both SPI master and slave up to 4 MHz.

The UART implements a universal asynchronous receiver/transmitter function. It supports flexible baud-rate generation up to a maximum of 3 Mbps and is compatible with the *Bluetooth* ® HCI specifications.

Timer 0 is a general-purpose timer module (GPTM), which provides two 16-bit timers. The GPTM can be configured to operate as a single 32-bit timer, dual 16-bit timers or as a PWM module.

Timer 1, Timer 2, and Timer 3 are also GPTMs. Each of these timers is functionally equivalent to Timer 0.

In addition to these four timers, the RF core has its own timer to handle timing for RF protocols; the RF timer can be synchronized to the RTC.

The $I^2C$ interface is used to communicate with devices compatible with the $I^2C$ standard. The $I^2C$ interface is capable of 100-kHz and 400-kHz operation, and can serve as both $I^2C$ master and $I^2C$ slave.

The TRNG module provides a true, nondeterministic noise source for the purpose of generating keys, initialization vectors (IVs), and other random number requirements. The TRNG is built on 24 ring oscillators that create unpredictable output to feed a complex nonlinear combinatorial circuit.

The watchdog timer is used to regain control if the system fails due to a software error after an external device fails to respond as expected. The watchdog timer can generate an interrupt or a reset when a predefined time-out value is reached.

The device includes a direct memory access (µDMA) controller. The µDMA controller provides a way to offload data transfer tasks from the Cortex-M3 CPU, allowing for more efficient use of the processor and the available bus bandwidth. The µDMA controller can perform transfer between memory and peripherals. The µDMA controller has dedicated channels for each supported on-chip module and can be programmed to automatically perform transfers between peripherals and memory as the peripheral is ready to transfer more data. Some features of the µDMA controller include the following (this is not an exhaustive list):

- Highly flexible and configurable channel operation of up to 32 channels
- Transfer modes:
  - Memory-to-memory
  - Memory-to-peripheral
  - Peripheral-to-memory
  - Peripheral-to-peripheral
- Data sizes of 8, 16, and 32 bits

The AON domain contains circuitry that is always enabled, except in Shutdown mode (where the digital supply is off). This circuitry includes the following:

- The RTC can be used to wake the device from any state where it is active. The RTC contains three compare and one capture registers. With software support, the RTC can be used for clock and calendar operation. The RTC is clocked from the 32-kHz RC oscillator or crystal. The RTC can also be compensated to tick at the correct frequency even when the internal 32-kHz RC oscillator is used instead of a crystal.
- The battery monitor and temperature sensor are accessible by software and give a battery status indication as well as a coarse temperature measure.

## 9.10 System Architecture

Depending on the product configuration, the CC2640R2F-Q1 device can function either as a wireless network processor (WNP—a device running the wireless protocol stack with the application running on a separate MCU), or as a system-on-chip (SoC), with the application and protocol stack running on the Arm Cortex-M3 core inside the device.

In the first case, the external host MCU communicates with the device using SPI or UART. In the second case, the application must be written according to the application framework supplied with the wireless protocol stack.

# 10 Application, Implementation, and Layout

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

## 10.1 Application Information

Very few external components are required for the operation of the CC2640R2F-Q1 device. This section provides general information about the differential configuration when using the CC2640R2F-Q1 device in an application, and an example application circuit with schematics and layout is shown in 図 10-1, 図 10-2, 図 10-3, and 図 10-4. This is only a small selection of the many application circuit examples available as complete reference designs from the product folder on www.ti.com.

図 10-1 shows the differential RF front-end configuration option with internal biasing. See the CC2640Q1EM-7ID reference design for this option.

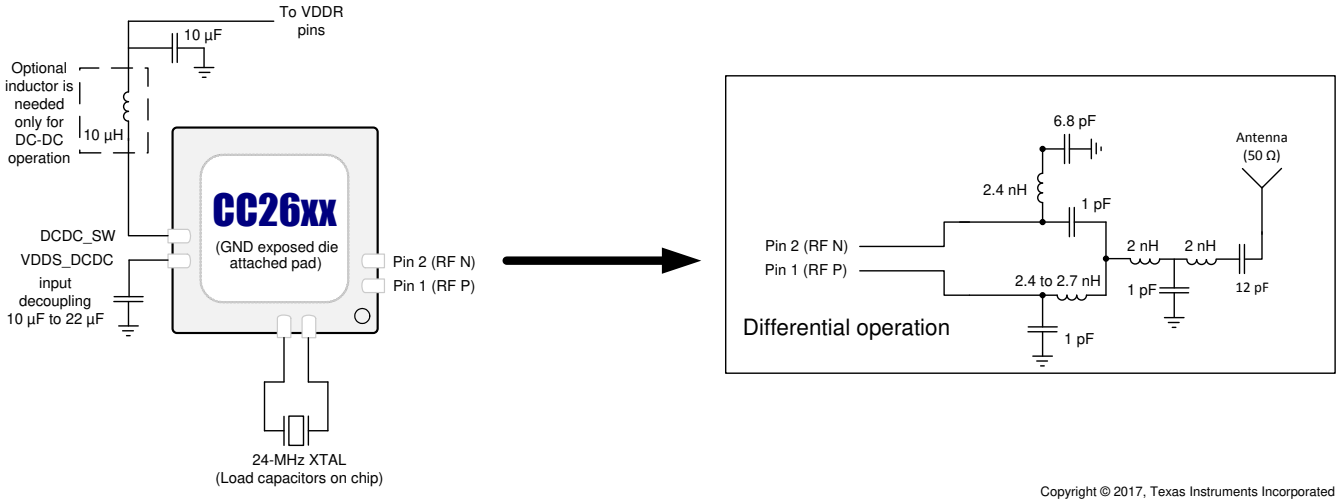



**図 10-1. CC2640R2F-Q1 Application Circuit**

図 10-2 shows the various supply voltage configuration options for the CC2640R2F-Q1 device. Not all power supply decoupling capacitors or digital I/Os are shown. For a detailed overview of power supply decoupling and wiring, see the TI reference designs and the *CC13x0, CC26x0 SimpleLink Wireless MCU Technical Reference Manual*.

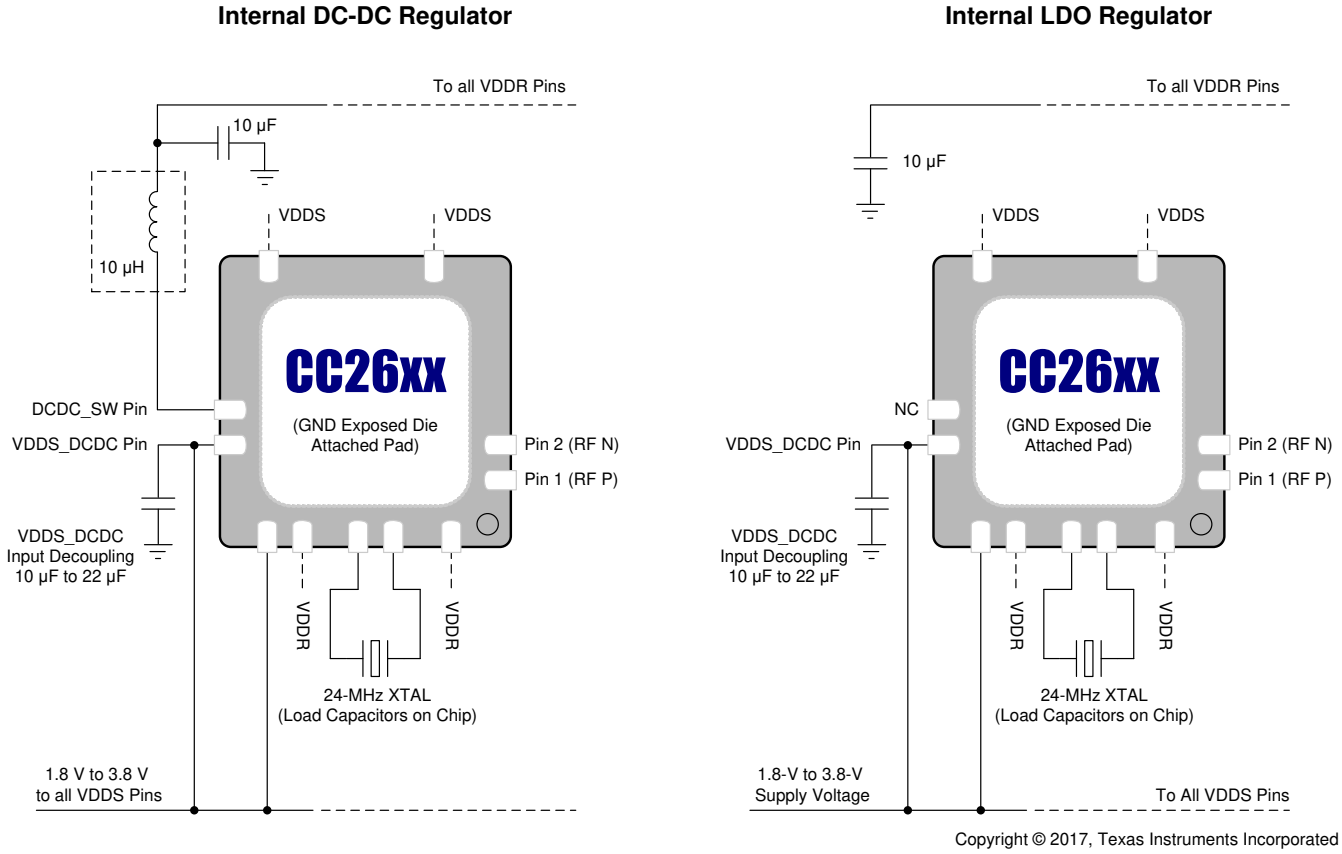



**図 10-2. Supply Voltage Configurations**

## 10.2 7 × 7 Internal Differential (7ID) Application Circuit

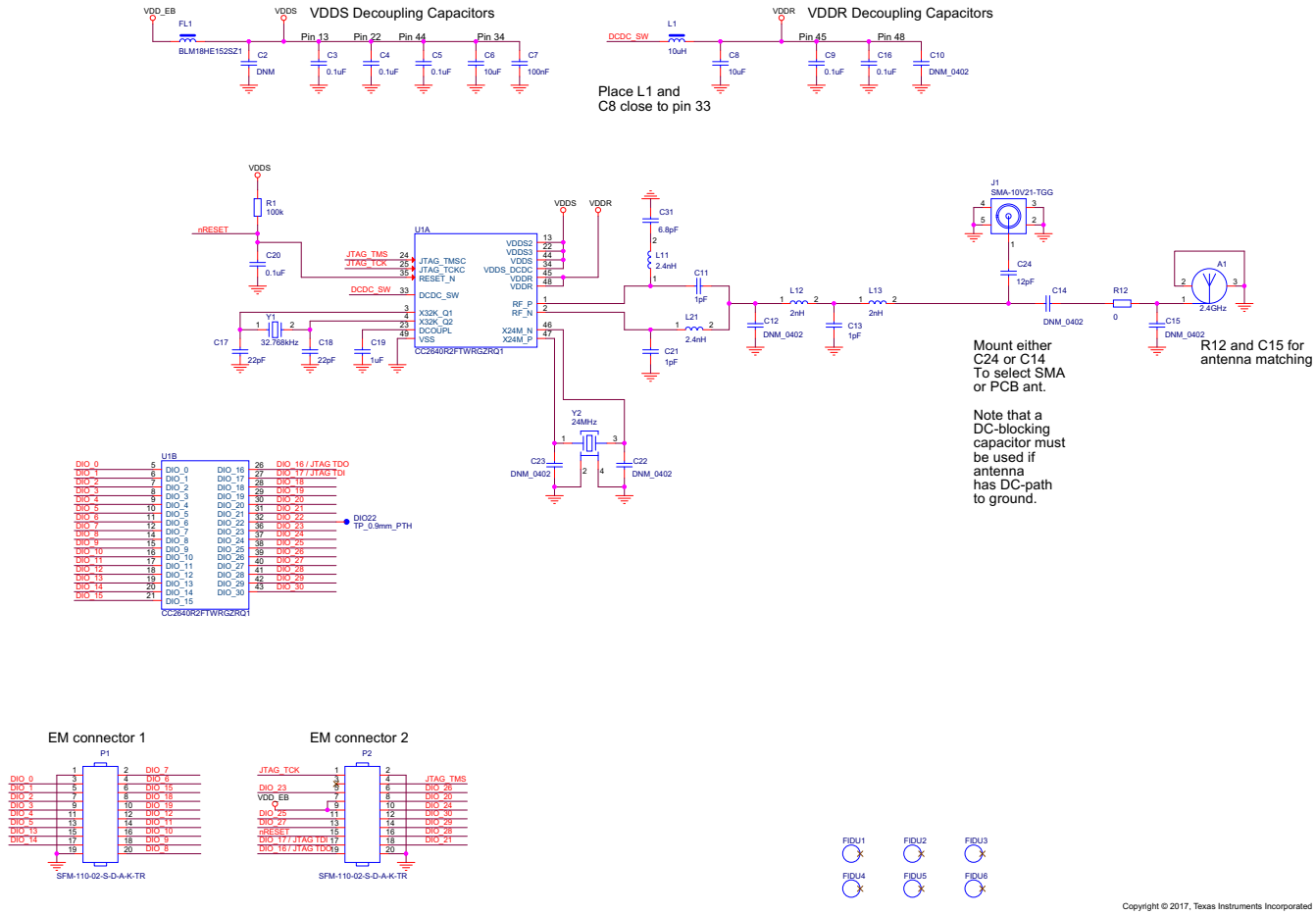



**図 10-3. 7 × 7 Internal Differential (7ID) Application Circuit**

### 10.2.1 Layout

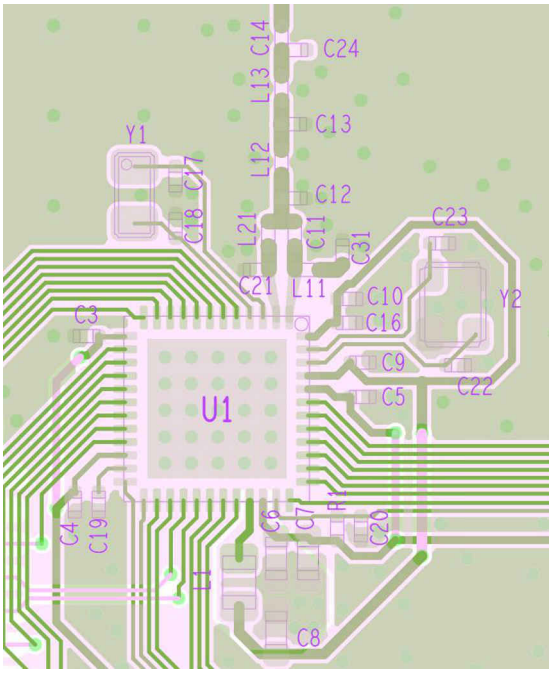



**図 10-4. Layout**

# 11 Device and Documentation Support

## 11.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to all part numbers and date-code. Each device has one of three prefixes/identifications: X, P, or null (no prefix) (for example, CC2640R2F-Q1 is in production; therefore, no prefix/identification is assigned).

Device development evolutionary flow:

**X** Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

**P** Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

**null** Production version of the silicon die that is fully qualified.

Production devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, *RGZ*).

For orderable part numbers of the *CC2640R2F-Q1* device package types, see the Package Option Addendum of this document, the TI website (www.ti.com), or contact your TI sales representative.

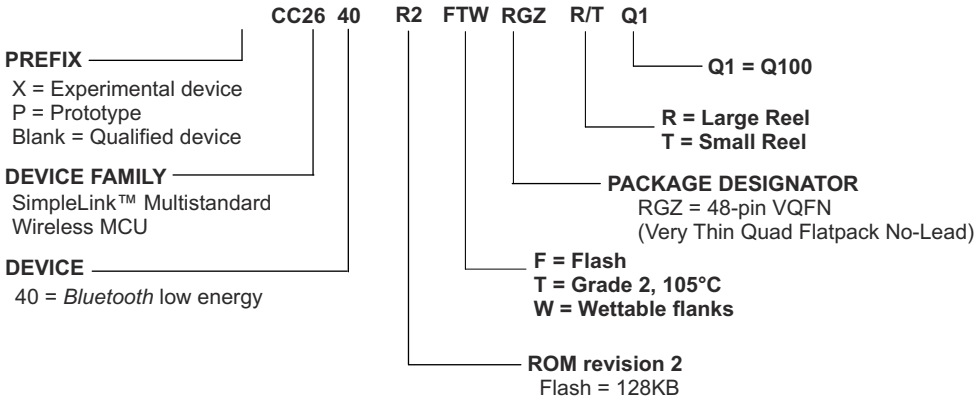



**図 11-1. Device Nomenclature**

## 11.2 Tools and Software

TI offers an extensive line of development tools, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules.

The following products support development of the CC2640R2F-Q1 device applications:

**Software Tools:**

SmartRF Studio 7 is a PC application that helps designers of radio systems to easily evaluate the RF-IC at an early stage in the design process.

- Test functions for sending and receiving radio packets, continuous wave transmit and receive
- Evaluate RF performance on custom boards by wiring it to a supported evaluation board or debugger
- Can also be used without any hardware, but then only to generate, edit and export radio configuration settings
- Can be used in combination with several development kits for TI's CCxxxx RF-ICs

Sensor Controller Studio provides a development environment for the CC26xx Sensor Controller. The Sensor Controller is a proprietary, power-optimized CPU in the CC26xx, which can perform simple background tasks autonomously and independent of the System CPU state.

- Allows for Sensor Controller task algorithms to be implemented using a C-like programming language
- Outputs a Sensor Controller Interface driver, which incorporates the generated Sensor Controller machine code and associated definitions
- Allows for rapid development by using the integrated Sensor Controller task testing and debugging functionality. This allows for live visualization of sensor data and algorithm verification.

**IDEs and Compilers:**

Code Composer Studio™ Integrated Development Environment (IDE):

- Integrated development environment with project management tools and editor
- Code Composer Studio (CCS) 6.1 and later has built-in support for the CC26xx device family
- Best support for XDS debuggers; XDS100v3, XDS110 and XDS200
- High integration with TI-RTOS with support for TI-RTOS Object View

IAR Embedded Workbench® for Arm®:

- Integrated development environment with project management tools and editor
- IAR EWARM 7.30.3 and later has built-in support for the CC26xx device family
- Broad debugger support, supporting XDS100v3, XDS200, IAR I-Jet and Segger J-Link
- Integrated development environment with project management tools and editor
- RTOS plugin available for TI-RTOS

For a complete listing of development-support tools for theCC2640R2F-Q1 platform, visit the Texas Instruments website at www.ti.com. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

## 11.3 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com (CC2640R2F-Q1). In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the CC2640R2F-Q1 devices, related peripherals, and other technical collateral is listed in the following.

**Technical Reference Manual**

*CC13x0, CC26x0 SimpleLink™ Wireless MCU Technical Reference Manual*

**Errata**

*CC2640R2M-Q1 SimpleLink™ Wireless MCU Errata*

## 11.4 Texas Instruments Low-Power RF Website

Texas Instruments' Low-Power RF website has all the latest products, application and design notes, FAQ section, news and events updates. Go to www.ti.com/lprf.

## 11.5 サポート・リソース

TI E2E™ サポート・フォーラムは、検証済みの迅速な回答と設計支援をエンジニアがエキスパートから直接得るための頼れる情報源です。既存の回答を検索し、または新たに質問することで、必要とする設計支援を迅速に得ることができます。

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## 11.6 Trademarks

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## 11.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.8 Export Control Notice

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## 11.9 用語集

TI 用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

# 12 Mechanical, Packaging, and Orderable Information

## 12.1 Packaging Information

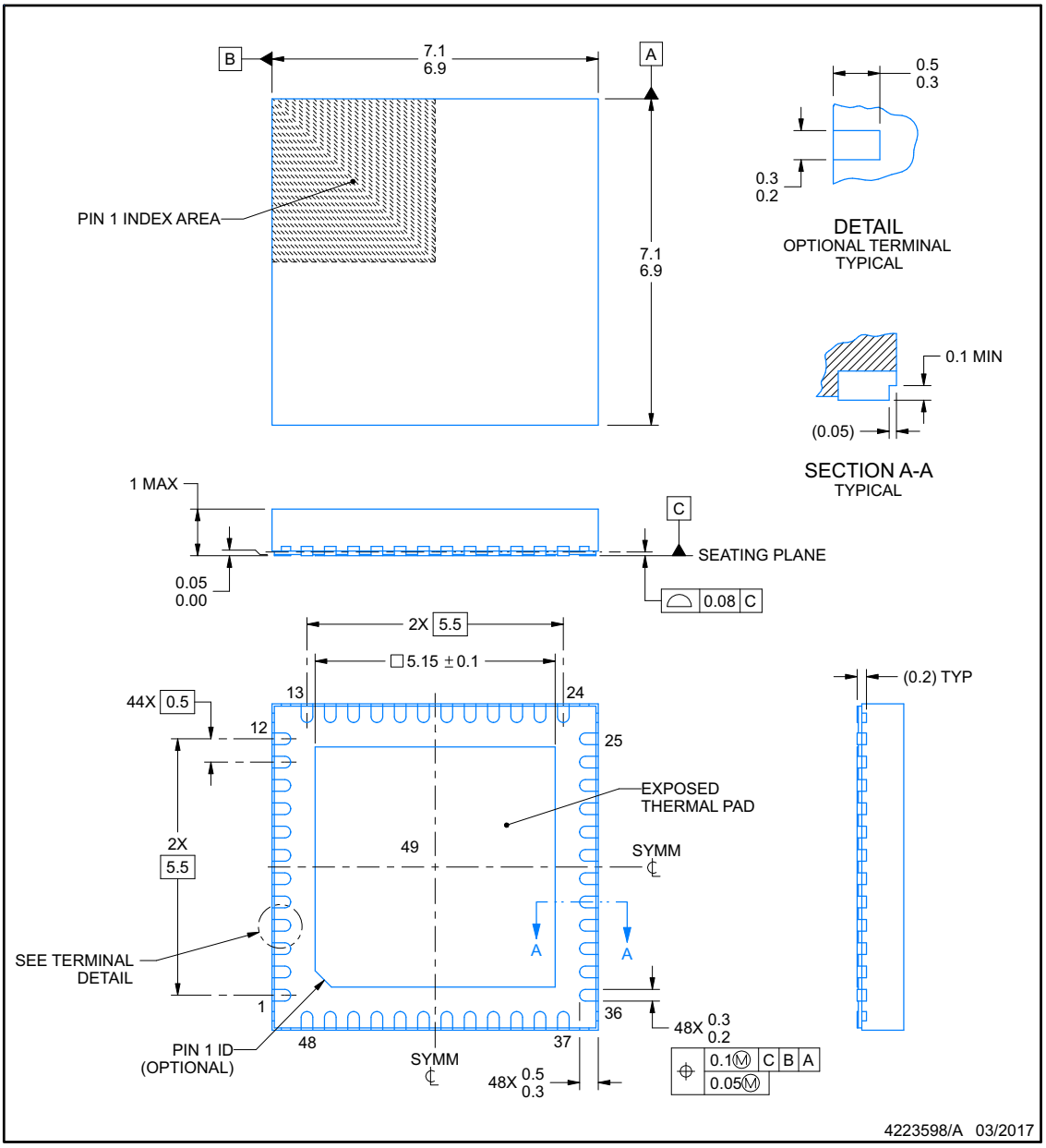
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

# PACKAGE OUTLINE

## RGZ0048N

### VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD




NOTES:

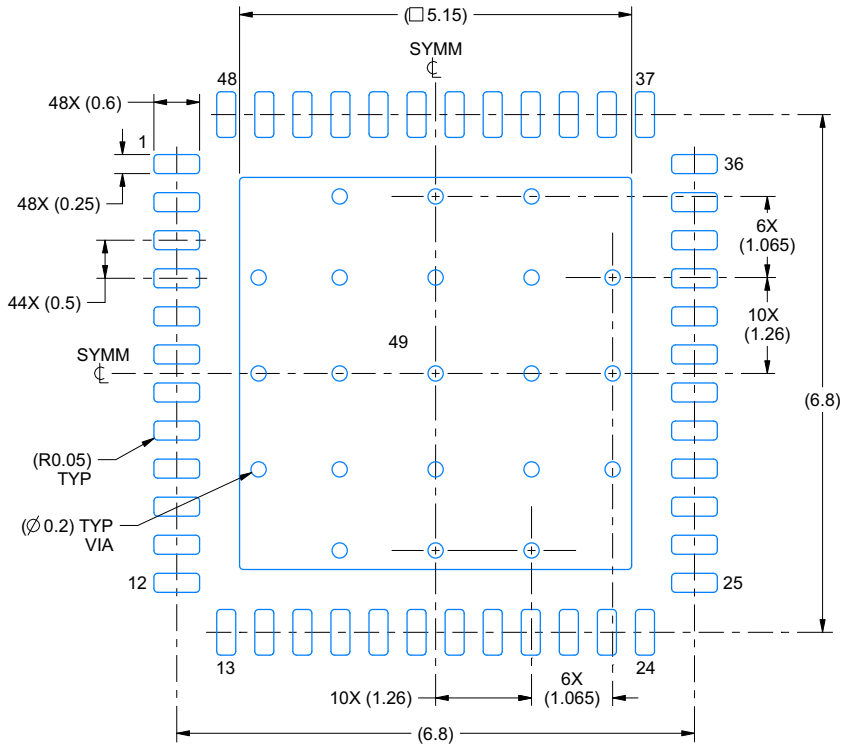
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

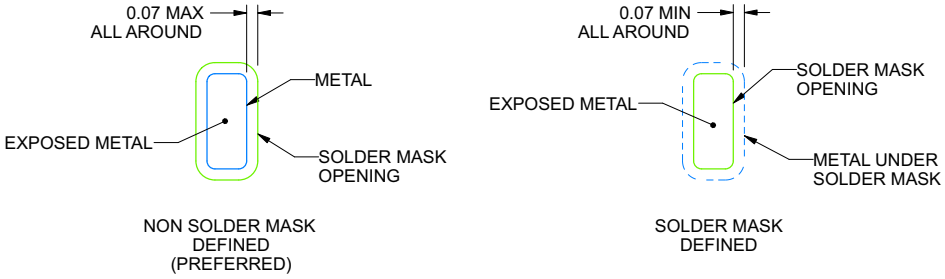
## RGZ0048N

### VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X




SOLDER MASK DETAILS

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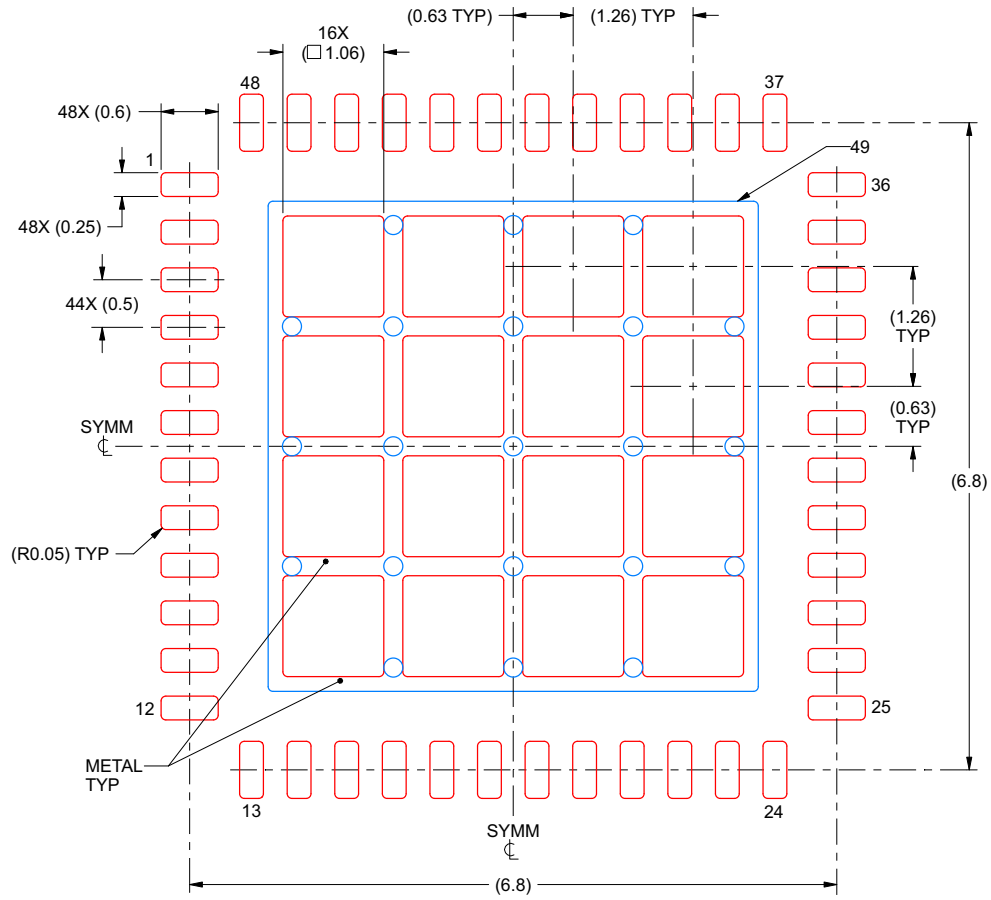
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

## EXAMPLE STENCIL DESIGN

**RGZ0048N** — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
68% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CC2640R2FTWRGZRQ1 | ACTIVE | VQFN | RGZ | 48 | 2500 | RoHS & Green | Call TI \| SN | Level-3-260C-168 HR | -40 to 105 | CC2640Q1 R2F | Samples |
| CC2640R2FTWRGZTQ1 | ACTIVE | VQFN | RGZ | 48 | 250 | RoHS & Green | Call TI \| SN | Level-3-260C-168 HR | -40 to 105 | CC2640Q1 R2F | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**OTHER QUALIFIED VERSIONS OF CC2640R2F-Q1 :**

- Catalog : CC2640R2F

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

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