

# CD405xB-Q1 8 チャンネルを 1 セット備えた、車載用 CMOS アナログ・マルチプレクサ / デマルチプレクサ、ロジック・レベル変換付き

## 1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
  - 温度グレード 1:  $-45^{\circ}\text{C} \sim +125^{\circ}\text{C}$ ,  $T_A$
- 幅広いデジタルおよびアナログ信号レベル:
  - デジタル:  $3\text{V} \sim 20\text{V}$
  - アナログ:  $20\text{V}_{\text{P-P}}$  以下
- 低いオン抵抗、 $15\text{V}_{\text{P-P}}$  信号入力範囲で、 $V_{\text{DD}} - V_{\text{EE}} = 18\text{V}$  において  $125\Omega$  (代表値)
- 高いオフ抵抗、 $V_{\text{DD}} - V_{\text{EE}} = 18\text{V}$  でチャンネル・リーク  $\pm 100\text{pA}$  (代表値)
- $3\text{V} \sim 20\text{V}$  のデジタル・アドレッシング信号 ( $V_{\text{DD}} - V_{\text{SS}} = 3\text{V} \sim 20\text{V}$ ) のロジック・レベル変換により、 $20\text{V}_{\text{P-P}}$  ( $V_{\text{DD}} - V_{\text{EE}} = 20\text{V}$ ) に一致するスイッチ特性にアナログ信号をスイッチング、 $r_{\text{ON}} 5\Omega$  (代表値、 $V_{\text{DD}} - V_{\text{EE}} = 15\text{V}$  の場合) ですべてのデジタル制御入力および電源条件において非常に低い静止電力、 $V_{\text{DD}} - V_{\text{SS}} = V_{\text{DD}} - V_{\text{EE}} = 10\text{V}$  において  $0.2\mu\text{W}$  (代表値)
- オンチップでバイナリ・アドレスをデコード
- 5V、10V、15V のパラメータ定格
- 20V で静止電流を 100% テスト済み
- パッケージの温度範囲全体にわたって 18V 時に最大入力電流  $1\mu\text{A}$ 、 $25^{\circ}\text{C}$  では 18V 時に  $100\text{nA}$
- Break-Before-Make スwitchングにより、チャンネルのオーバーラップを排除

## 2 アプリケーション

- アナログおよびデジタルの多重化 / 多重分離
- アナログ・デジタルおよびデジタル・アナログ変換
- 信号ゲーティング
- ファクトリ・オートメーション
- テレビ
- 電化製品
- 民生用オーディオ
- プログラム可能な論理回路
- センサ

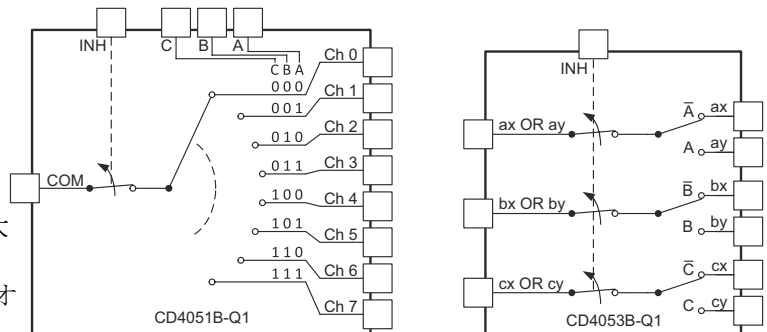
## 3 概要

CD405xB-Q1 アナログ・マルチプレクサ / デマルチプレクサは、オン状態のインピーダンスが低くオフ状態のリーク電流が非常に小さいデジタル制御のアナログ・スイッチです。これらのマルチプレクサ回路は、制御信号の論理状態にかかわらず、 $V_{\text{DD}} - V_{\text{SS}}$  および  $V_{\text{DD}} - V_{\text{EE}}$  の電源電圧範囲全体にわたって非常に小さな静止電力しか消費しません。

### パッケージ情報<sup>(1)</sup>

部品番号	パッケージ	本体サイズ (公称)
CD405xB-Q1	D (SOIC, 16)	9.90mm × 3.91mm
	PW (TSSOP, 16)	5.00mm × 4.40mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



CD405xB-Q1 の機能ブロック図



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## 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (April 2019) to Revision C (March 2023)	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新.....	1
• データシート全体にわたって CD4051-Q1 の仕様を更新.....	1

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Changes from Revision A (January 2008) to Revision B (April 2019)	Page
• 「ピン構成および機能」セクション、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加.....	1
• データシートから部品番号 CD4052B-Q1 を削除.....	1

## 5 Pin Configuration and Functions

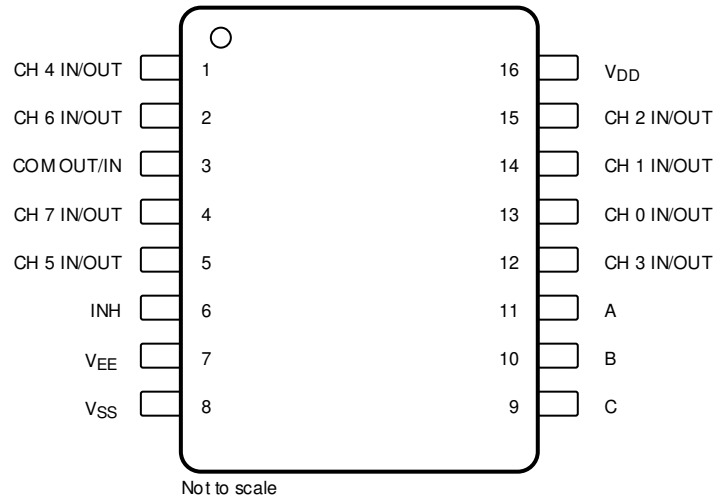


图 5-1. CD4051B-Q1 D or PW Package, (Top View)

表 5-1. Pin Functions CD4051B-Q1

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NO.	NAME		
1	CH 4 IN/OUT	I/O	Channel 4 in/out
2	CH 6 IN/OUT	I/O	Channel 6 in/out
3	COM OUT/IN	I/O	Common out/in
4	CH 7 IN/OUT	I/O	Channel 7 in/out
5	CH 5 IN/OUT	I/O	Channel 5 in/out
6	INH	I	Disables all channels. See 表 8-1.
7	VEE	—	Negative power input
8	VSS	—	Ground
9	C	I	Channel select C. See 表 8-1.
10	B	I	Channel select B. See 表 8-1.
11	A	I	Channel select A. See 表 8-1.
12	CH 3 IN/OUT	I/O	Channel 3 in/out
13	CH 0 IN/OUT	I/O	Channel 0 in/out
14	CH 1 IN/OUT	I/O	Channel 1 in/out
15	CH 2 IN/OUT	I/O	Channel 2 in/out
16	VDD	—	Positive power input

(1) I = input, O = output

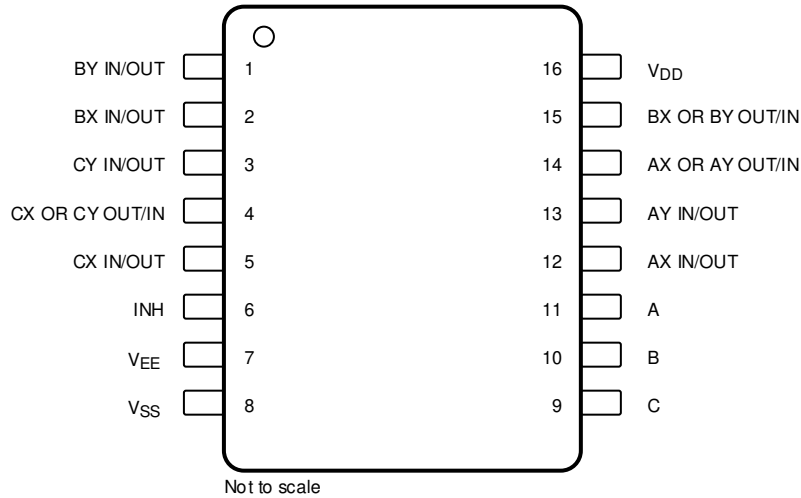


图 5-2. CD4053B-Q1 D or PW Package, (Top View)

表 5-2. Pin Functions CD4053B-Q1

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NO.	NAME		
1	BY IN/OUT	I/O	B channel Y in/out
2	BX IN/OUT	I/O	B channel X in/out
3	CY IN/OUT	I/O	C channel Y in/out
4	CX OR CY OUT/IN	I/O	C common out/in
5	CX IN/OUT	I/O	C channel X in/out
6	INH	I	Disables all channels. See 表 8-1.
7	V <sub>EE</sub>	—	Negative power input
8	V <sub>SS</sub>	—	Ground
9	C	I	Channel select C. See 表 8-1.
10	B	I	Channel select B. See 表 8-1.
11	A	I	Channel select A. See 表 8-1.
12	AX IN/OUT	I/O	A channel X in/out
13	AY IN/OUT	I/O	A channel Y in/out
14	AX OR AY OUT/IN	I/O	A common out/in
15	BX OR BY OUT/IN	I/O	B common out/in
16	V <sub>DD</sub>	—	Positive power input

(1) I = input, O = output

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

		MIN	MAX	UNIT
	Supply Voltage	V+ to V-, Voltages Referenced to V <sub>SS</sub> Terminal		V
	DC Input Voltage	-0.5	V <sub>DD</sub> +0.5	V
	DC Input Current	Any One Input		mA
T <sub>JMAX1</sub>	Maximum junction temperature, ceramic package			175 °C
T <sub>JMAX2</sub>	Maximum junction temperature, plastic package			150 °C
T <sub>stg</sub>	Storage temperature			-65 150 °C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground, unless otherwise specified.

### 6.2 ESD Ratings

			VALUE	UNIT
CD4051B-Q1				
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins <sup>(1)</sup>	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±750	
CD4053B-Q1				
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins <sup>(1)</sup>	±2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Temperature Range	-55		125	°C

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		CD405xB-Q1		UNIT
		D (SOIC)	PW (TSSOP)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86.7	116.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.3	47.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45.3	63.0	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	12.1	6.4	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	44.9	62.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics - CD4051B-Q1

Over operating free-air temperature range,  $V_{SUPPLY} = \pm 5\text{ V}$ , and  $R_L = 100\ \Omega$ , (unless otherwise noted)<sup>(1)</sup>

PARAMETER	TEST CONDITIONS					MIN	TYP	MAX	UNIT
	$V_{IS}$ (V)	$V_{EE}$ (V)	$V_{SS}$ (V)	$V_{DD}$ (V)	TEMP				
<b>SIGNAL INPUTS (<math>V_{IS}</math>) AND OUTPUTS (<math>V_{OS}</math>) - CD4051B-Q1</b>									
Quiescent Device Current, $I_{DD}$ (Max)	0 V	0 V	0 V	5 V	-55°C			60	$\mu\text{A}$
					-40°C			60	
					25°C		17	60	
					85°C			150	
					125°C			150	
	0 V	0 V	0 V	10 V	-55°C			60	
					-40°C			60	
					25°C		18	60	
					85°C			300	
					125°C			300	
	0 V	0 V	0 V	15 V	-55°C			60	
					-40°C			60	
					25°C		18	60	
					85°C			600	
					125°C			600	
	0 V	0 V	0 V	20 V	-55°C			100	
					-40°C			100	
					25°C		18	100	
					85°C			3000	
					125°C			3000	
Drain to Source ON Resistance $r_{ON}$ (Max) $0 \leq V_{IS} \leq V_{DD}$	0 V	0 V	5 V	-55°C			800	$\Omega$	
				-40°C			850		
				25°C		470	1050		
				85°C			1200		
				125°C			1300		
	0 V	0 V	10 V	-55°C			310		
				-40°C			300		
				25°C		180	400		
				85°C			520		
				125°C			550		
	0 V	0	15 V	-55°C			200		
				-40°C			210		
				25°C		125	240		
				85°C			300		
				125°C			300		
Change in ON Resistance (Between Any Two Channels), $\Delta R_{ON}$	0 V	0 V	5 V	25°C			15	$\Omega$	
			10 V				10		
			15 V				5		

### 6.5 Electrical Characteristics - CD4051B-Q1 (continued)

Over operating free-air temperature range,  $V_{SUPPLY} = \pm 5\text{ V}$ , and  $R_L = 100\ \Omega$ , (unless otherwise noted)<sup>(1)</sup>

PARAMETER		TEST CONDITIONS				MIN	TYP	MAX	UNIT
		$V_{IS}$ (V)	$V_{EE}$ (V)	$V_{SS}$ (V)	$V_{DD}$ (V)	TEMP			
OFF Channel Leakage Current: Any Channel OFF (Max) or ALL Channels OFF (COMMON OUT/IN) (Max)						-55°C	± 100		nA
						-40°C			
			0 V	0 V	18 V	25°C	± 0.3	± 100 <sup>(2)</sup>	
						85°C	± 1000 <sup>(2)</sup>		
						125°C			
ON Channel Leakage Current: Any Channel ON (Max) or ALL Channels ON (COMMON OUT/IN) (Max)		5 or 0	-5 V	0 V	10.5 V	85°C	± 800		nA
		5	0 V	0 V	18 V	85°C	± 800		
Capacitance	Input, $C_{IS}$						5		pF
	Output, $C_{OS}$	CD4051-Q1	0 V	0 V	10 V	25°C	30		
	Feed-through, $C_{IOS}$						0.2		
Prop Delay		$V_{DD}$	$R_L = 200\text{ k}\Omega$		5 V	25°C	30	60	ns
			$C_L = 50\text{ pF}$		10 V		15	30	
			$t_r, t_f = 20\text{ ns}$		15 V		10	20	



## 6.5 Electrical Characteristics - CD4051B-Q1 (continued)

Over operating free-air temperature range,  $V_{SUPPLY} = \pm 5\text{ V}$ , and  $R_L = 100\ \Omega$ , (unless otherwise noted)<sup>(1)</sup>

PARAMETER		TEST CONDITIONS					MIN	TYP	MAX	UNIT
		$V_{IS}$ (V)	$V_{EE}$ (V)	$V_{SS}$ (V)	$V_{DD}$ (V)	TEMP				
<b>CONTROL (ADDRESS OR INHIBIT), <math>V_C</math> - CD4051B-Q1</b>										
Input Low Voltage, $V_{IL}$ , (Max)					5 V	-55°C	0.8		V	
						-40°C	0.8			
						25°C	0.8			
						85°C	0.8			
						125°C	0.8			
					10 V	-55°C	0.8			
						-40°C	0.8			
						25°C	0.8			
						85°C	0.8			
						125°C	0.8			
					15 V	-55°C	0.8			
						-40°C	0.8			
						25°C	0.8			
						85°C	0.8			
						125°C	0.8			
Input High Voltage, $V_{IH}$ , (Min)					5 V	-55°C	3.5		V	
						-40°C	3.5			
						25°C	3.5			
						85°C	3.5			
						125°C	3.5			
					10 V	-55°C	7			
						-40°C	7			
						25°C	7			
						85°C	7			
						125°C	7			
					15 V	-55°C	11			
						-40°C	11			
						25°C	11			
						85°C	11			
						125°C	11			
Input current, $I_{IN}$ (Max)					18 V	-55°C	$\pm 1$		$\mu\text{A}$	
						-40°C	$\pm 1$			
						25°C	$\pm 0.6$			
						85°C	$\pm 1$			
						125°C	$\pm 1$			
Propagation Delay Time	Address-to-Signal OUT (Channels ON or OFF) (See Figure 7-2 Figure 7-3, and Figure 7-8)	$t_r, t_f = 20\text{ns}$ , $C_L = 50\text{ pF}$ , $R_L = 10\text{ k}\Omega$	0 V	0 V	5 V		450	720	ns	
			0 V	0 V	10 V		160	320		
			0 V	0 V	15 V		120	240		
			-5 V	0 V	5 V		225	450		

## 6.5 Electrical Characteristics - CD4051B-Q1 (continued)

Over operating free-air temperature range,  $V_{\text{SUPPLY}} = \pm 5 \text{ V}$ , and  $R_L = 100 \ \Omega$ , (unless otherwise noted)<sup>(1)</sup>

PARAMETER		TEST CONDITIONS					MIN	TYP	MAX	UNIT
		$V_{\text{IS}}$ (V)	$V_{\text{EE}}$ (V)	$V_{\text{SS}}$ (V)	$V_{\text{DD}}$ (V)	TEMP				
Propagation Delay Time	Inhibit-to-Signal OUT (Channel Turning ON) (See Figure 7-3)	$t_r, t_f = 20 \text{ ns}$ , $C_L = 50 \text{ pF}$ , $R_L = 1 \text{ k}\Omega$	0 V	0 V	5 V		400	720	ns	
			0 V	0 V	10 V		160	320		
			0 V	0 V	15 V		120	240		
			-10 V	0 V	5 V		200	400		
Propagation Delay Time	Inhibit-to-Signal OUT (Channel Turning OFF) (See Figure 7-10)	$t_r, t_f = 20 \text{ ns}$ , $C_L = 50 \text{ pF}$ , $R_L = 10 \text{ k}\Omega$	0 V	0 V	5 V		200	450	ns	
			0 V	0 V	10 V		90	210		
			0 V	0 V	15 V		70	160		
			-10 V	0 V	5 V		130	300		
Input Capacitance, $C_{\text{IN}}$ (Any Address or Inhibit Input)			-5 V	0 V	5 V	25°C	5	7.5	pF	

(1) Peak-to-Peak voltage symmetrical about  $(V_{\text{DD}} - V_{\text{EE}}) / 2$ .

(2) Determined by minimum feasible leakage measurement for automatic testing.

## 6.6 AC Performance Characteristics - CD4051B-Q1

$V_{DD} = +15\text{ V}$ ,  $V_{SS} = V_{EE} = 0\text{ V}$ ,  
 $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS				TYP	UNIT	
	$V_{IS}$ (V)	$V_{DD}$ (V)	$R_L$ (k $\Omega$ )				
Cutoff (–3 dB) Frequency Channel ON (Sine Wave Input)	5 <sup>(1)</sup>	10	1	$V_{OS}$ at Common OUT/IN	CD4051-Q1	20	MHz
	$V_{EE} = V_{SS}$ , $20\text{Log}(V_{OS}/V_{IS}) = -3\text{ dB}$			$V_{OS}$ at Any Channel		60	
Total Harmonic Distortion, THD	2 <sup>(1)</sup>	5	10			0.3%	%
	3 <sup>(1)</sup>	10	10			0.2%	
	5 <sup>(1)</sup>	15	10			0.12%	
	$V_{EE} = V_{SS}$ , $f_{IS} = 1\text{ kHz}$ Sine Wave						
–40 dB Feed-through Frequency (All Channels OFF)	5 <sup>(1)</sup>	10	1	$V_{OS}$ at Common OUT/IN	CD4051-Q1	12	MHz
	$V_{EE} = V_{SS}$ , $20\text{Log}(V_{OS}/V_{IS}) = -40\text{ dB}$			$V_{OS}$ at Any Channel		8	MHz
–40 dB Signal Crosstalk Frequency	5 <sup>(1)</sup>	10	1			3	MHz
Address-or-Inhibit-to- Signal Crosstalk		10	10 <sup>(2)</sup>			65	mV <sub>PEAK</sub>
	$V_{EE} = 0$ , $V_{SS} = 0$ , $t_r$ , $t_f = 20\text{ ns}$ , mV <sub>PEAK</sub> $V_{CC} = V_{DD} - V_{SS}$ (Square Wave)						65

- (1) Peak-to-Peak voltage symmetrical about  $(V_{DD} - V_{EE}) / 2$ .  
(2) Both ends of channel.

### 6.7 Electrical Characteristics - CD4053B-Q1

Over operating free-air temperature range,  $V_{SUPPLY} = \pm 5\text{ V}$ , and  $R_L = 100\ \Omega$ , (unless otherwise noted)<sup>(1)</sup>

PARAMETER	TEST CONDITIONS					MIN	TYP	MAX	UNIT
	$V_{IS}$ (V)	$V_{EE}$ (V)	$V_{SS}$ (V)	$V_{DD}$ (V)	TEMP				
<b>SIGNAL INPUTS (<math>V_{IS}</math>) AND OUTPUTS (<math>V_{OS}</math>) - CDIP, PDIP, SOIC and SOP Packages</b>									
Quiescent Device Current, $I_{DD}$ (Max)	0 V	0 V	0 V	5 V	-55°C			5	$\mu\text{A}$
					-40°C			5	
					25°C	0.04		5	
					85°C			150	
					125°C			150	
	0 V	0 V	0 V	10 V	-55°C			10	
					-40°C			10	
					25°C	0.04		10	
					85°C			300	
					125°C			300	
	0 V	0 V	0 V	15 V	-55°C			20	
					-40°C			20	
					25°C	0.04		20	
					85°C			600	
					125°C			600	
	0 V	0 V	0 V	20 V	-55°C			100	
					-40°C			100	
					25°C	18		100	
					85°C			3000	
					125°C			3000	
Drain to Source ON Resistance $r_{ON}$ (Max) $0 \leq V_{IS} \leq V_{DD}$	0 V	0 V	5 V	-55°C			800	$\Omega$	
				-40°C			850		
				25°C	470		1050		
				85°C			1200		
				125°C			1300		
	0 V	0 V	0 V	10 V	-55°C				310
					-40°C				300
					25°C	180			400
					85°C				520
					125°C				550
	0 V	0	0	15 V	-55°C				200
					-40°C				210
25°C					125		240		
85°C							300		
125°C							300		
Change in ON Resistance (Between Any Two Channels), $\Delta R_{ON}$	0 V	0 V	5 V	25°C			15	$\Omega$	
			10 V				10		
			15 V				5		

## 6.7 Electrical Characteristics - CD4053B-Q1 (continued)

Over operating free-air temperature range,  $V_{\text{SUPPLY}} = \pm 5 \text{ V}$ , and  $R_L = 100 \Omega$ , (unless otherwise noted)<sup>(1)</sup>

PARAMETER		TEST CONDITIONS					MIN	TYP	MAX	UNIT
		$V_{\text{IS}}$ (V)	$V_{\text{EE}}$ (V)	$V_{\text{SS}}$ (V)	$V_{\text{DD}}$ (V)	TEMP				
OFF Channel Leakage Current: Any Channel OFF (Max) or ALL Channels OFF (COMMON OUT/IN) (Max)			0 V	0 V	18 V	-55°C		± 100	nA	
						-40°C				
						25°C		± 0.01 ± 100 <sup>(2)</sup>		
						85°C		± 1000 <sup>(2)</sup>		
						125°C				
ON Channel Leakage Current: Any Channel ON (Max) or ALL Channels ON (COMMON OUT/IN) (Max)		5 or 0	-5 V	0 V	10.5 V	85°C		± 300	nA	
							5	0 V		0 V
Capacitance	Input, $C_{\text{IS}}$		0 V	0 V	10 V	25°C		5	pF	
	Output, $C_{\text{OS}}$						CD4053-Q1			9
	Feed-through, $C_{\text{IOS}}$									0.2
Prop Delay		$V_{\text{DD}}$	$R_L = 200 \text{ k}\Omega$		5 V	25°C		30 60	ns	
			$C_L = 50 \text{ pF}$		10 V			15 30		
			$t_r, t_f = 20 \text{ ns}$		15 V			10 20		

### 6.7 Electrical Characteristics - CD4053B-Q1 (continued)

Over operating free-air temperature range,  $V_{SUPPLY} = \pm 5\text{ V}$ , and  $R_L = 100\ \Omega$ , (unless otherwise noted)<sup>(1)</sup>

PARAMETER		TEST CONDITIONS					MIN	TYP	MAX	UNIT
		$V_{IS}$ (V)	$V_{EE}$ (V)	$V_{SS}$ (V)	$V_{DD}$ (V)	TEMP				
<b>CONTROL (ADDRESS OR INHIBIT), <math>V_C</math> - CDIP, PDIP, SOIC and SOP Packages</b>										
Input Low Voltage, $V_{IL}$ , (Max)						5 V	-55°C	1.5		V
							-40°C	1.5		
							25°C	1.5		
							85°C	1.5		
							125°C	1.5		
						10 V	-55°C	3		
							-40°C	3		
							25°C	3		
							85°C	3		
							125°C	3		
						15 V	-55°C	4		
							-40°C	4		
							25°C	4		
							85°C	4		
							125°C	4		
Input High Voltage, $V_{IH}$ , (Min)						5 V	-55°C	3.5		V
							-40°C	3.5		
							25°C	3.5		
							85°C	3.5		
							125°C	3.5		
						10 V	-55°C	7		
							-40°C	7		
							25°C	7		
							85°C	7		
							125°C	7		
						15 V	-55°C	11		
							-40°C	11		
							25°C	11		
							85°C	11		
							125°C	11		
Input current, $I_{IN}$ (Max)						18 V	-55°C	$\pm 0.1$		$\mu\text{A}$
							-40°C	$\pm 0.1$		
							25°C	$\pm 10^{-5} \pm 0.1$		
							85°C	$\pm 1$		
							125°C	$\pm 1$		
Propagation Delay Time	Address-to-Signal OUT (Channels ON or OFF) (See Figure 7-2 Figure 7-3, and Figure 7-8)	$t_r, t_f = 20\text{ns}$ , $C_L = 50\text{ pF}$ , $R_L = 10\text{ k}\Omega$	0 V	0 V	5 V	450	720	ns		
			0 V	0 V	10 V	160	320			
			0 V	0 V	15 V	120	240			
			-5 V	0 V	5 V	225	450			

## 6.7 Electrical Characteristics - CD4053B-Q1 (continued)

Over operating free-air temperature range,  $V_{\text{SUPPLY}} = \pm 5 \text{ V}$ , and  $R_L = 100 \Omega$ , (unless otherwise noted)<sup>(1)</sup>

PARAMETER		TEST CONDITIONS					MIN	TYP	MAX	UNIT
		$V_{\text{IS}}$ (V)	$V_{\text{EE}}$ (V)	$V_{\text{SS}}$ (V)	$V_{\text{DD}}$ (V)	TEMP				
Propagation Delay Time	Inhibit-to-Signal OUT (Channel Turning ON) (See Figure 7-3)	$t_r, t_f = 20 \text{ ns}$ , $C_L = 50 \text{ pF}$ , $R_L = 1 \text{ k}\Omega$	0 V	0 V	5 V		400	720	ns	
			0 V	0 V	10 V		160	320		
			0 V	0 V	15 V		120	240		
			-10 V	0 V	5 V		200	400		
Propagation Delay Time	Inhibit-to-Signal OUT (Channel Turning OFF) (See Figure 7-10)	$t_r, t_f = 20 \text{ ns}$ , $C_L = 50 \text{ pF}$ , $R_L = 10 \text{ k}\Omega$	0 V	0 V	5 V		200	450	ns	
			0 V	0 V	10 V		90	210		
			0 V	0 V	15 V		90	160		
			-10 V	0 V	5 V		130	300		
Input Capacitance, $C_{\text{IN}}$ (Any Address or Inhibit Input)			-5 V	0 V	5 V	25°C	5	7.5	pF	

- (1) Peak-to-Peak voltage symmetrical about  $(V_{\text{DD}} - V_{\text{EE}}) / 2$ .  
(2) Determined by minimum feasible leakage measurement for automatic testing.

### 6.8 AC Performance Characteristics - CD4053B-Q1

$V_{DD} = +15\text{ V}$ ,  $V_{SS} = V_{EE} = 0\text{ V}$ ,

$T_A = 25^\circ\text{C}$  (unless otherwise noted)

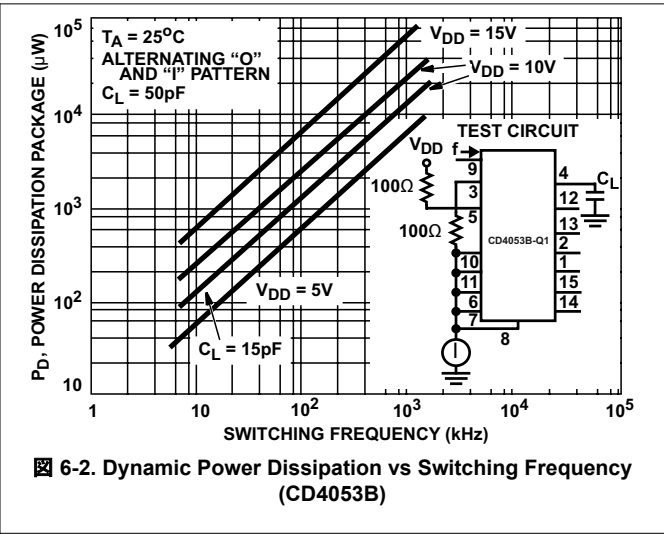
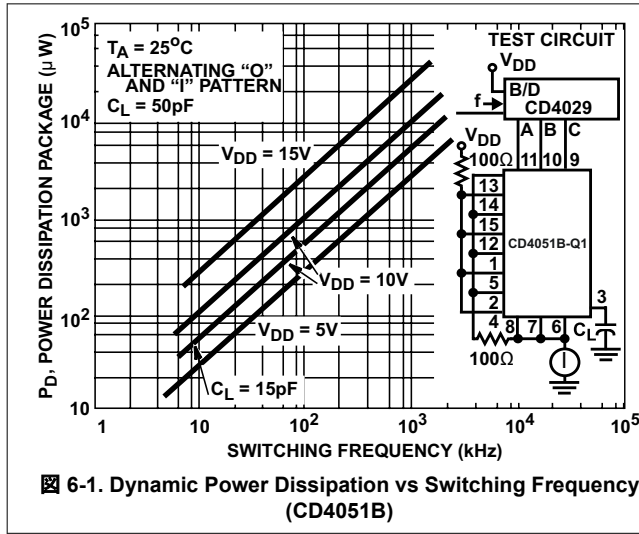
PARAMETER	TEST CONDITIONS				TYP	UNIT		
	$V_{IS}$ (V)	$V_{DD}$ (V)	$R_L$ (k $\Omega$ )					
Cutoff (–3 dB) Frequency Channel ON (Sine Wave Input)	5 <sup>(1)</sup>	10	1	$V_{OS}$ at Common OUT/IN	CD4053-Q1	30	MHz	
	$V_{EE} = V_{SS}$ , $20\text{Log}(V_{OS}/V_{IS}) = -3\text{ dB}$			$V_{OS}$ at Any Channel		60		
Total Harmonic Distortion, THD	2 <sup>(1)</sup>	5	10			0.3%	%	
	3 <sup>(1)</sup>	10	10			0.2%		
	5 <sup>(1)</sup>	15	10			0.12%		
	$V_{EE} = V_{SS}$ , $f_{IS} = 1\text{ kHz}$ Sine Wave							
–40 dB Feed-through Frequency (All Channels OFF)	5 <sup>(1)</sup>	10	1	$V_{OS}$ at Common OUT/IN	CD4053-Q1	8	MHz	
	$V_{EE} = V_{SS}$ , $20\text{Log}(V_{OS}/V_{IS}) = -40\text{ dB}$			$V_{OS}$ at Any Channel		8	MHz	
–40 dB Signal Crosstalk Frequency	5 <sup>(1)</sup>	10	1	Between Any Two Sections, CD4053-Q1 Only		3	MHz	
	$V_{EE} = V_{SS}$ , $20\text{Log}(V_{OS}/V_{IS}) = -3\text{ dB}$					In Pin 2, Out Pin 14	2.5	MHz
						In Pin 15, Out Pin 14	6	MHz
Address-or-Inhibit-to- Signal Crosstalk		10	10 <sup>(2)</sup>			65	mV <sub>PEAK</sub>	
	$V_{EE} = 0$ , $V_{SS} = 0$ , $t_r$ , $t_f = 20\text{ ns}$ , mV <sub>PEAK</sub> $V_{CC} = V_{DD} - V_{SS}$ (Square Wave)					65	mV <sub>PEAK</sub>	

(1) Peak-to-Peak voltage symmetrical about  $(V_{DD} - V_{EE}) / 2$ .

(2) Both ends of channel.



## 6.9 Typical Characteristics



## 7 Parameter Measurement Information

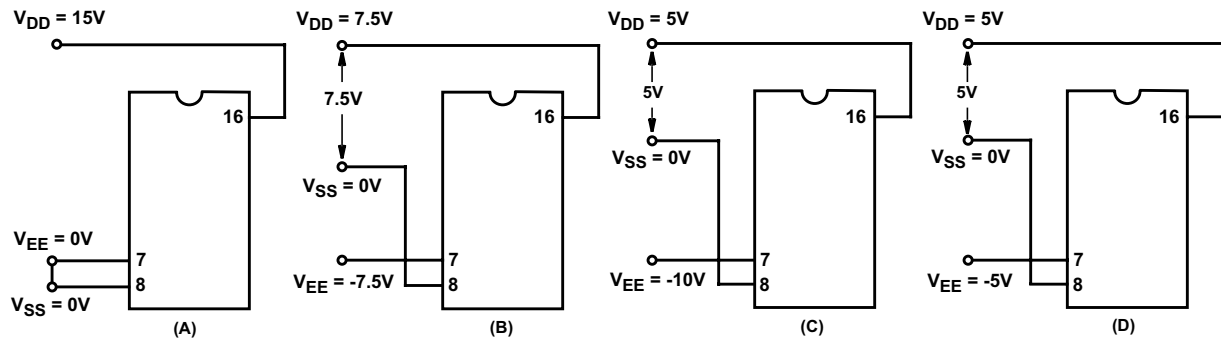


图 7-1. Typical Bias Voltages

注

The ADDRESS (digital-control inputs) and INHIBIT logic levels are: 0 =  $V_{SS}$  and 1 =  $V_{DD}$ . The analog signal (through the TG) may swing from  $V_{EE}$  to  $V_{DD}$ .

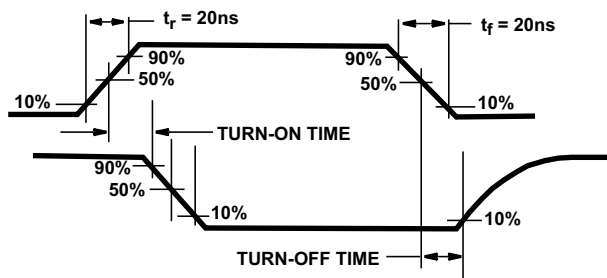


图 7-2. Waveforms, Channel Being Turned ON ( $R_L = 1\text{ k}\Omega$ )

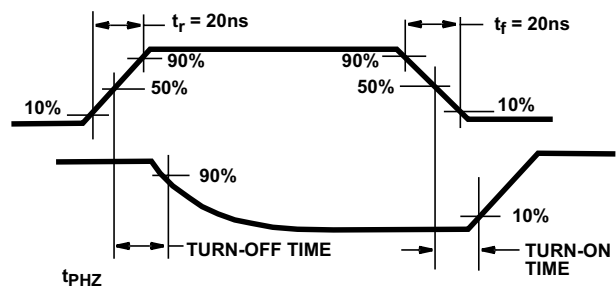


图 7-3. Waveforms, Channel Being Turned OFF ( $R_L = 1\text{ k}\Omega$ )

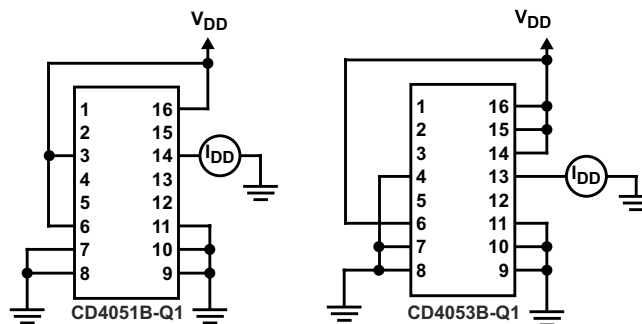
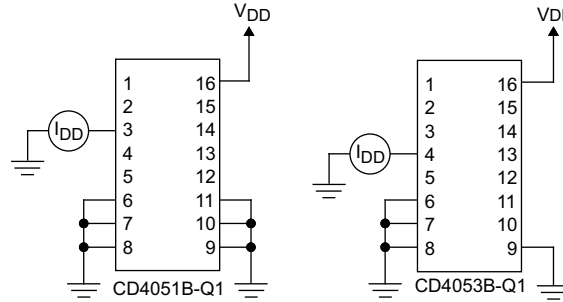
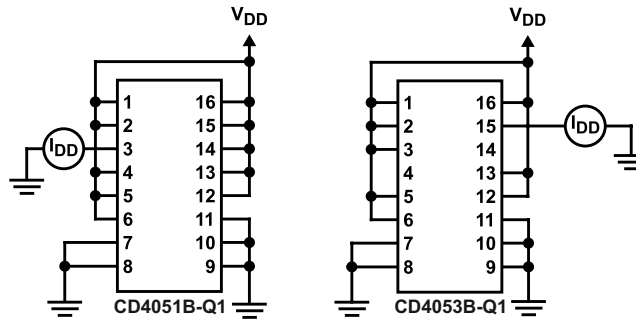


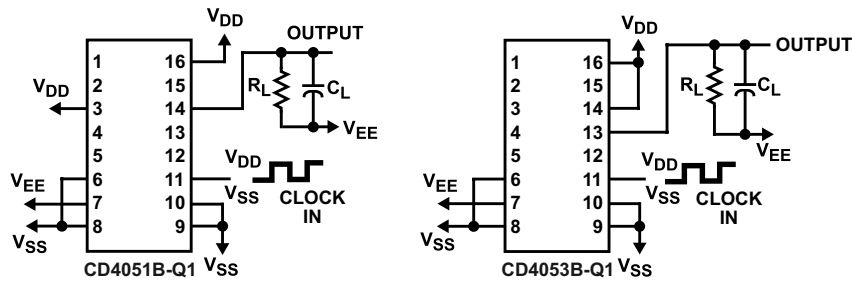
图 7-4. OFF Channel Leakage Current – Any Channel OFF



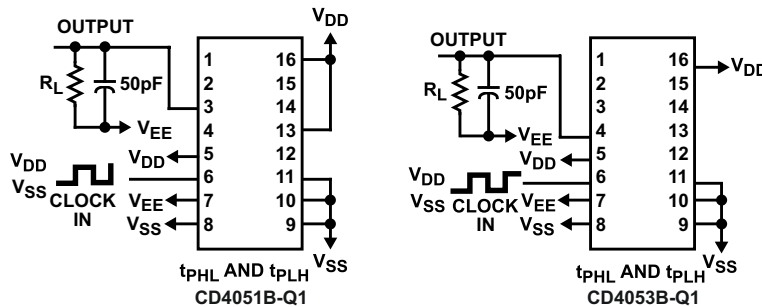
7-5. On Channel Leakage Current – Any Channel On



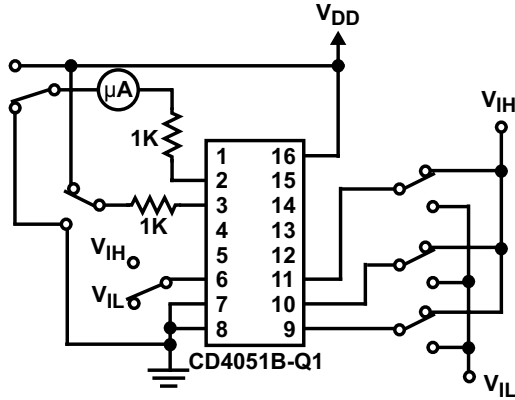
7-6. OFF Channel Leakage Current – All Channels OFF



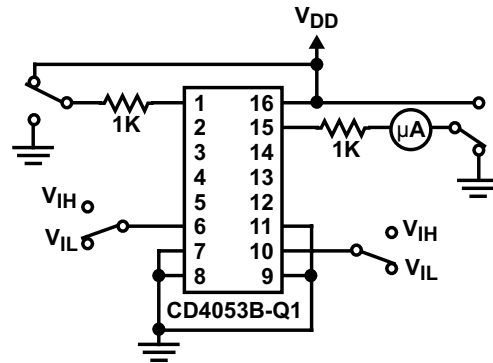
7-7. Propagation Delay – Address Input to Signal Output



7-8. Propagation Delay – Inhibit Input to Signal Output



MEASURE  $< 2\mu\text{A}$  ON ALL "OFF" CHANNELS (e.g., CHANNEL 6)



MEASURE  $< 2\mu\text{A}$  ON ALL "OFF" CHANNELS (e.g., CHANNEL 6)

图 7-9. Input Voltage Test Circuits (Noise Immunity)

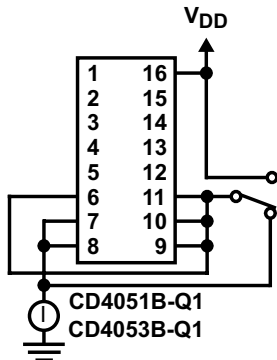


图 7-10. Quiescent Device Current

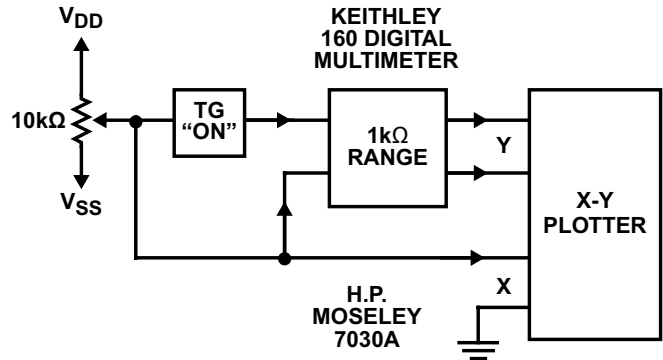
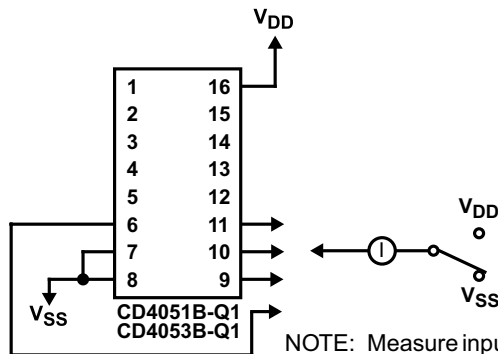


图 7-11. Channel ON Resistance Measurement Circuit



NOTE: Measure inputs sequentially, to both  $V_{DD}$  and  $V_{SS}$  connect all unused inputs to either  $V_{DD}$  or  $V_{SS}$ .

图 7-12. Input Current

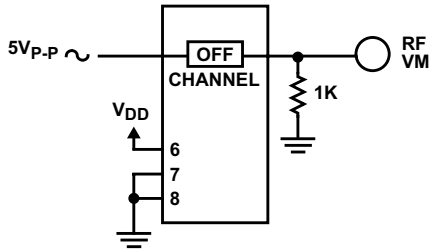


图 7-13. Feed-Through (All Types)

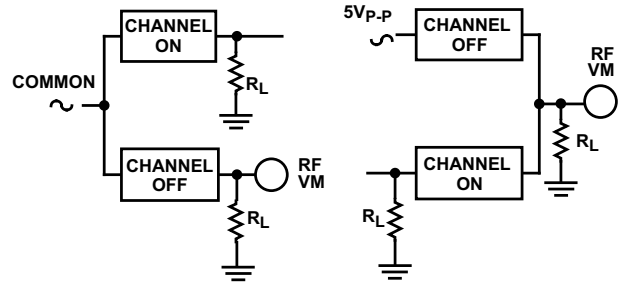


图 7-14. Crosstalk Between Any Two Channels (All Types)

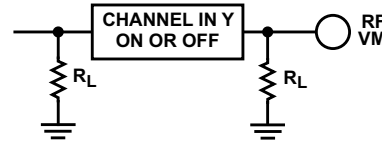
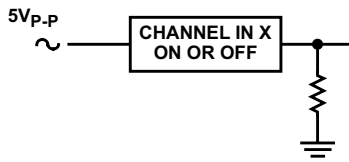


图 7-15. Crosstalk Between Duals or Triplets (CD4053B-Q1)

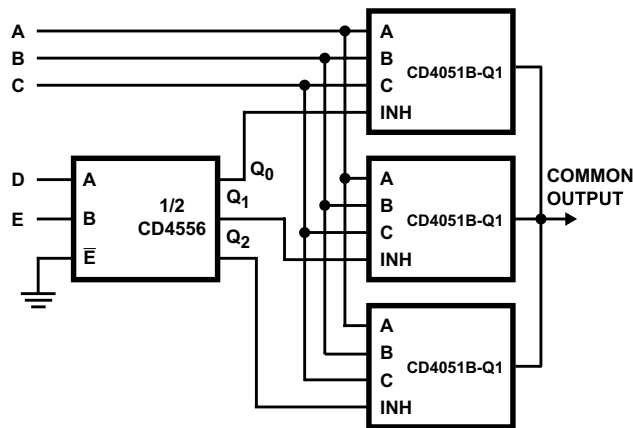


图 7-16. 24-to-1 MUX Addressing

## 8 Detailed Description

### 8.1 Overview

The CD4051B-Q1 and CD4053B-Q1 analog multiplexers are digitally-controlled analog switches having low ON impedance and very low OFF leakage current. Control of analog signals up to 20 V<sub>P-P</sub> can be achieved by digital signal amplitudes of 4.5 V to 20 V (if  $V_{DD} - V_{SS} = 3$  V, a  $V_{DD} - V_{EE}$  of up to 13 V can be controlled; for  $V_{DD} - V_{EE}$  level differences above 13 V, a  $V_{DD} - V_{SS}$  of at least 4.5 V is required). For example, if  $V_{DD} = +4.5$  V,  $V_{SS} = 0$  V, and  $V_{EE} = -13.5$  V, analog signals from  $-13.5$  V to  $+4.5$  V can be controlled by digital inputs of 0 V to 5 V. These multiplexer circuits dissipate extremely low quiescent power over the full  $V_{DD} - V_{SS}$  and  $V_{DD} - V_{EE}$  supply-voltage ranges, independent of the logic state of the control signals. When a logic 1 is present at the inhibit input terminal, all channels are off.

The CD4051B-Q1 device is a single 8-channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned on, and connect one of the 8 inputs to the output.

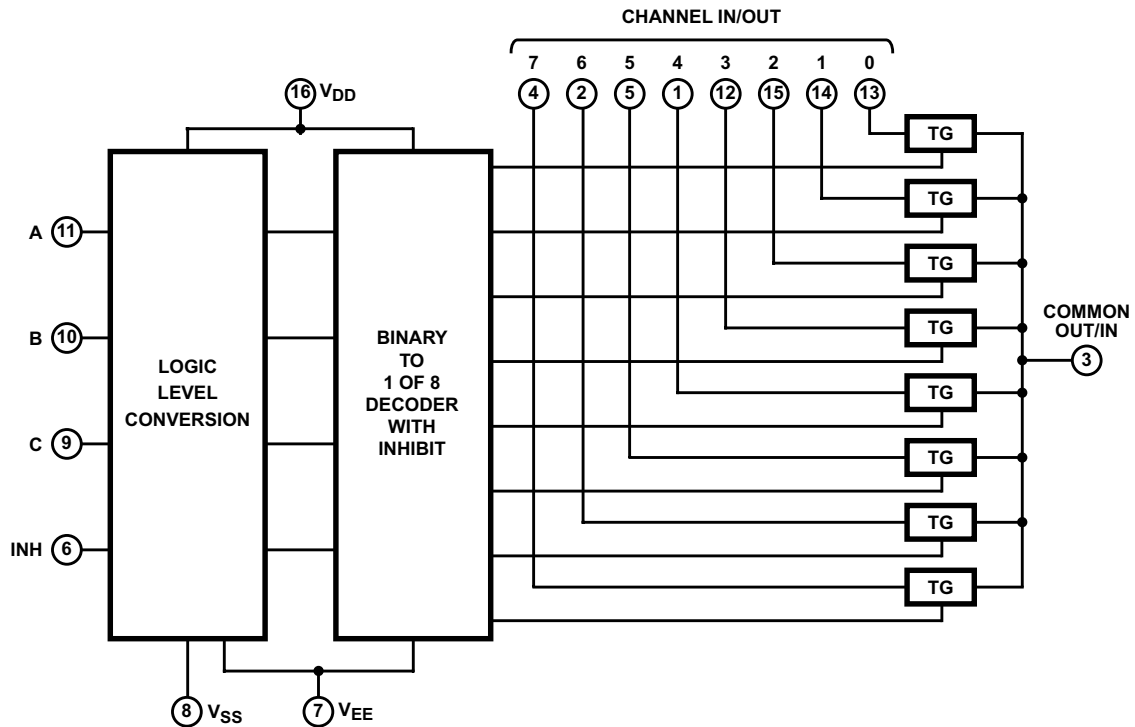
The CD4053B-Q1 device is a triple 2-channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole, double-throw configuration.

**CD4051B-Q1, CD4053B-Q1**

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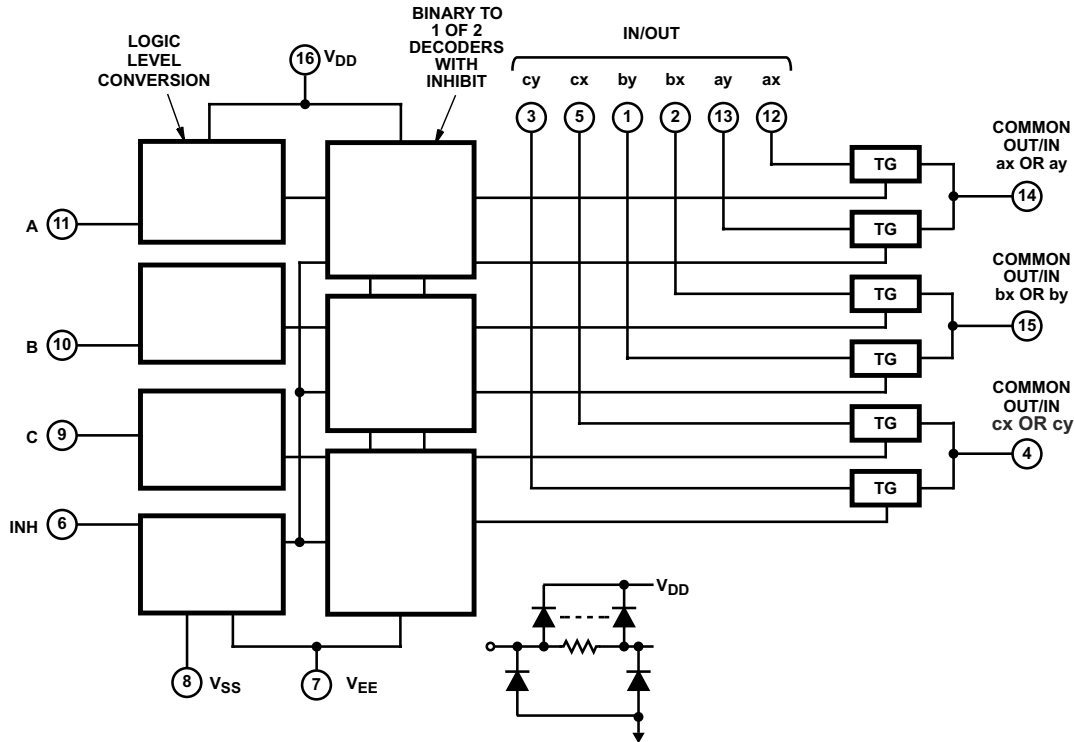
When these devices are used as demultiplexers, the CHANNEL IN/OUT terminals are the outputs and the COMMON OUT/IN terminals are the inputs.

**8.2 Functional Block Diagrams**



All inputs are protected by standard CMOS protection network.

**8-1. Functional Block Diagram, CD4051B-Q1**



All inputs are protected by standard CMOS protection network.

**8-2. Functional Block Diagram, CD4053B-Q1**

### 8.3 Feature Description

The CD405xB-Q1 line of multiplexers and demultiplexers can accept a wide range of digital and analog signal levels. Digital signals range from 3 V to 20 V, and analog signals are accepted at levels  $\leq 20$  V. The devices have low ON resistance, typically  $125 \Omega$  over  $15 V_{P-P}$  signal input range for  $V_{DD} - V_{EE} = 18$  V. This feature allows for very little signal loss through the switch. Matched switch characteristics are typically  $r_{ON} = 5 \Omega$  for  $V_{DD} - V_{EE} = 15$  V.

The CD405xB-Q1 devices also have high OFF resistance, which keeps from wasting power when the switch is in the OFF position, with typical channel leakage of  $\pm 100$  pA at  $V_{DD} - V_{EE} = 18$  V. Very low quiescent power dissipation under all digital-control input and supply conditions, typically  $0.2 \mu W$  at  $V_{DD} - V_{SS} = V_{DD} - V_{EE} = 10$  V keeps power consumption total very low. All devices have been 100% tested for quiescent current at 20 V with maximum input current of  $1 \mu A$  at 18 V over the full package temperature range, and only 100 nA at 18 V and  $25^\circ C$ .

Logic-level conversion for digital addressing signals of 3 V to 20 V ( $V_{DD} - V_{SS} = 3$  V to 20 V) to switch analog signals to  $20 V_{P-P}$  ( $V_{DD} - V_{EE} = 20$  V). Binary address decoding on chip makes channel selection easy. When channels are changed, a break-before-make system eliminates channel overlap.

## 8.4 Device Functional Modes

表 8-1. Truth Table<sup>(1)</sup>

INPUT STATES				ON CHANNEL(S)
INHIBIT	C	B	A	
<b>CD4051B-Q1</b>				
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	X	X	X	None
<b>CD4053B-Q1</b>				
L	L	L	L	ay or by or cy
L	H	H	H	ay or by or cy
H	X	X	X	None

(1) X = Do not care



## 9 Application and Implementation

### 注

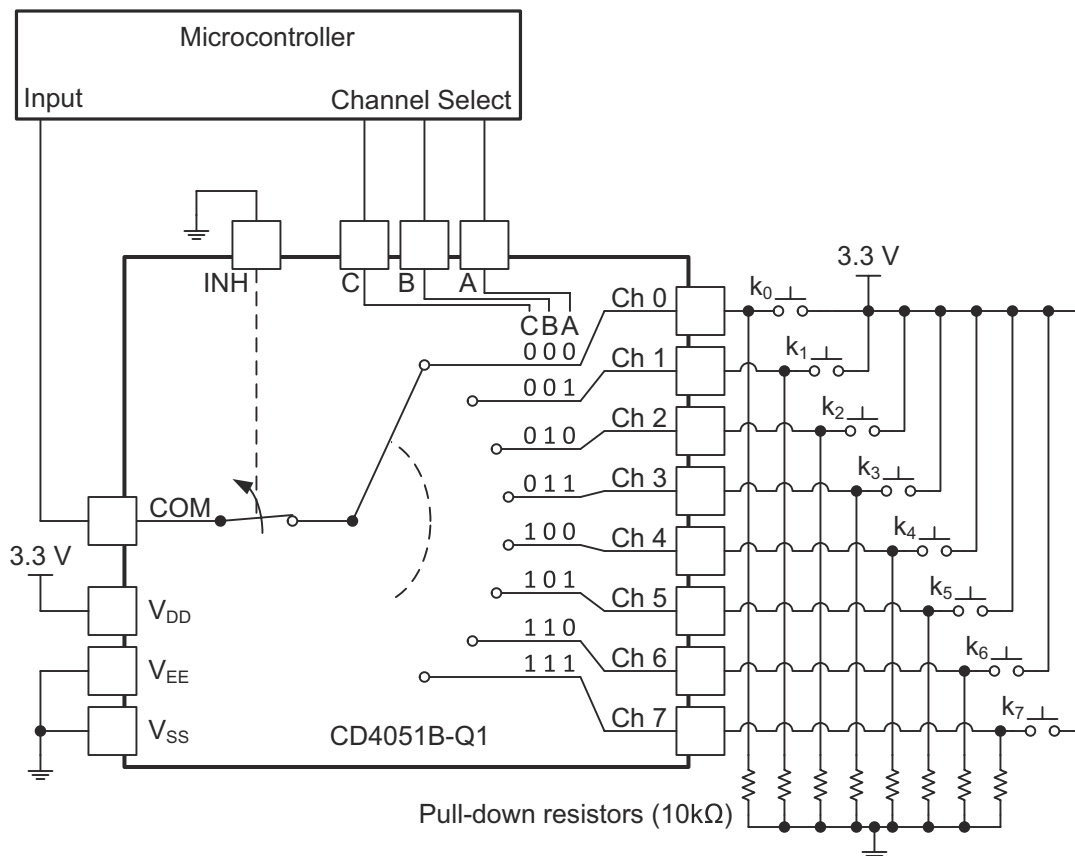
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### 9.1 Application Information

The CD405xB-Q1 multiplexers and demultiplexers can be used for a wide variety of applications.

### 9.2 Typical Application

One application of the CD4051B-Q1 is to use it in conjunction with a microcontroller to poll a keypad. [図 9-1](#) shows the basic schematic for such a polling system. The microcontroller uses the channel select pins to cycle through the different channels while reading the input to see if a user is pressing any of the keys. This application is a very robust setup, allowing for multiple simultaneous key-presses with very little power consumption. This setup also uses very few pins on the microcontroller. The down side of polling is that the microcontroller must continually scan the keys for a press and can do little else during this process.



**図 9-1. The CD4051B-Q1 Being Used to Help Read Button Presses on a Keypad**

#### 9.2.1 Design Requirements

These devices use CMOS technology and have balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

## 9.2.2 Detailed Design Procedure

- Recommended Input Conditions:
  - For switch time specifications, see propagation delay times in [Electrical Characteristics](#).
  - Inputs should not be pushed more than 0.5 V above  $V_{DD}$  or below  $V_{EE}$ .
  - For input voltage level specifications for control inputs, see  $V_{IH}$  and  $V_{IL}$  in [Electrical Characteristics](#).
- Recommended Output Conditions:
  - Outputs should not be pulled above  $V_{DD}$  or below  $V_{EE}$ .
- Input or output current consideration:
  - The CD405xB-Q1 series of parts do not have internal current drive circuitry and thus cannot sink or source current. Any current will be passed through the device.

## 9.2.3 Application Curve

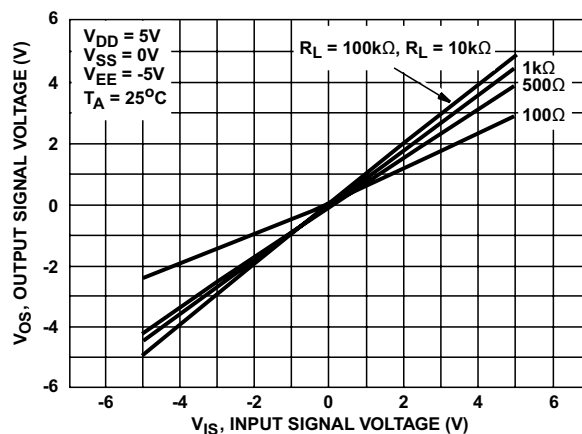


FIG 9-2. ON Characteristics for 1 of 8 Channels (CD4051B-Q1)

## 9.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Electrical Characteristics](#).

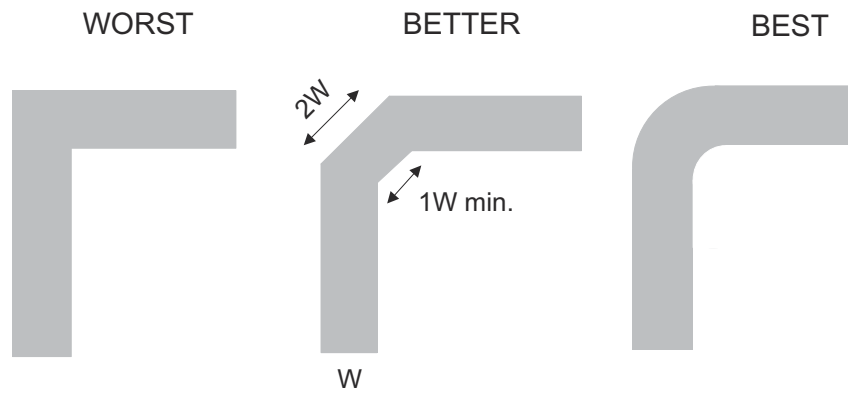
Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- $\mu F$  bypass capacitor is recommended. If there are multiple pins labeled  $V_{CC}$ , then a 0.01- $\mu F$  or 0.022- $\mu F$  capacitor is recommended for each  $V_{CC}$  because the  $V_{CC}$  pins will be tied together internally. For devices with dual supply pins operating at different voltages, for example  $V_{CC}$  and  $V_{DD}$ , a 0.1- $\mu F$  bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1- $\mu F$  and 1- $\mu F$  capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 9.4 Layout

### 9.4.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This reflection is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self-inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and so they will have to turn corners. FIG 9-3 shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

### 9.4.2 Layout Example



9-3. Trace Example

## 10 Device and Documentation Support

### 10.1 Documentation Support

#### 10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Implications of Slow or Floating CMOS Inputs](#)

### 10.2 ドキュメントの更新通知を受け取る方法

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### 10.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 10.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD4051BQPWRG4Q1	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-40 to 125	CM051BQ	
CD4051BQPWRQ1	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CM051BQ	Samples
CD4053BQM96G4Q1	NRND	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CD4053Q	
CD4053BQM96Q1	NRND	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CD4053Q	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD4051B-Q1, CD4053B-Q1 :**

- Catalog : [CD4051B](#), [CD4053B](#)
- Military : [CD4051B-MIL](#), [CD4053B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4051BQPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4051BQPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4051BQPWRQ1	TSSOP	PW	16	2000	367.0	367.0	35.0
CD4051BQPWRQ1	TSSOP	PW	16	2000	367.0	367.0	35.0



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.



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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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