

## CDx4HCT86 クワッド 2 入力 XOR ゲート

### 1 特長

- LSTTL 入力ロジック互換
  - $V_{IL(max)} = 0.8V$ ,  $V_{IH(min)} = 2V$
- CMOS 入力ロジック互換
  - $I_I \leq 1\mu A$  ( $V_{OL}$ ,  $V_{OH}$ )
- バッファ付き入力
- 4.5V~5.5V で動作
- 広い動作温度範囲: -55°C~+125°C
- 最大 10 個の LSTTL 負荷ファンアウトに対応
- LSTTL ロジック IC に比べて消費電力を大幅削減

### 2 アプリケーション

- 複数の入力信号の位相差を検出
- 選択可能なインバータ / バッファの作成

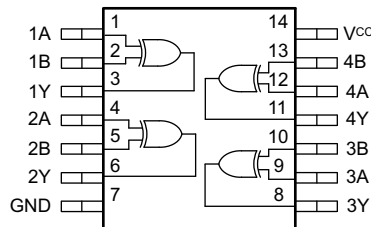
### 3 概要

このデバイスには、4 つの独立した 2 入力 XOR ゲートが内蔵されています。各ゲートはブール関数  $Y = A \oplus B$  を正論理で実行します。

#### 製品情報

部品番号	パッケージ <sup>(1)</sup>	パッケージ サイズ <sup>(2)</sup>	本体サイズ <sup>(3)</sup>
CDx4HCT86	D (SOIC, 14)	8.65mm × 6mm	8.65mm × 3.9mm
	N (PDIP, 14)	19.30mm × 9.4mm	19.30mm × 6.35mm
	J (CDIP, 14)	19.56mm × 6.7mm	19.56mm × 4.57mm

- (1) 詳細については、「[メカニカル](#)、[パッケージ](#)、および[注文情報](#)」を参照してください。
- (2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。
- (3) 本体サイズ (長さ × 幅) は公称値であり、ピンは含まれません。



機能的なピン配置

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## 4 Pin Configuration and Functions

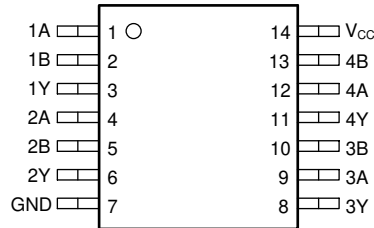


图 4-1. D, N, or J Package 14-Pin SOIC, PDIP, or CDIP Top View

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
1A	1	Input	Channel 1, Input A
1B	2	Input	Channel 1, Input B
1Y	3	Output	Channel 1, Output Y
2A	4	Input	Channel 2, Input A
2B	5	Input	Channel 2, Input B
2Y	6	Output	Channel 2, Output Y
GND	7	—	Ground
3Y	8	Output	Channel 3, Output Y
3A	9	Input	Channel 3, Input A
3B	10	Input	Channel 3, Input B
4Y	11	Output	Channel 4, Output Y
4A	12	Input	Channel 4, Input A
4B	13	Input	Channel 4, Input B
V <sub>CC</sub>	14	—	Positive Supply

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	-0.5	7	V
I <sub>IK</sub>	Input clamp current <sup>(2)</sup>	V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V		±20 mA
I <sub>OK</sub>	Output clamp current <sup>(2)</sup>	V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V		±20 mA
I <sub>O</sub>	Continuous output current	V <sub>O</sub> > -0.5 V or V <sub>O</sub> < V <sub>CC</sub> + 0.5 V		±25 mA
Continuous current through V <sub>CC</sub> or GND				±50 mA
T <sub>J</sub>	Junction temperature <sup>(3)</sup>			150 °C
Lead temperature (soldering 10s)		SOIC - lead tips only		300 °C
T <sub>stg</sub>	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) Guaranteed by design.

### 5.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/ JEDEC JS-001 <sup>(1)</sup>	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	4.5		5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V			V
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V		0.8	V
V <sub>I</sub>	Input voltage	0		V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0		V <sub>CC</sub>	V
t <sub>t</sub>	Input transition time	V <sub>CC</sub> = 4.5 V		500	ns
		V <sub>CC</sub> = 5.5 V		400	
T <sub>A</sub>	Operating free-air temperature	-55		125	°C

### 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	CD74HCT86		UNIT	
	N (PDIP)	D (SOIC)		
	14 PINS	14 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	103.8	138.7	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	91.6	93.8	°C/W

THERMAL METRIC <sup>(1)</sup>		CD74HCT86		UNIT
		N (PDIP)	D (SOIC)	
		14 PINS	14 PINS	
R <sub>θJB</sub>	Junction-to-board thermal resistance	83.5	94.7	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	71.1	49.1	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	83.4	94.3	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 5.5 Electrical Characteristics

over operating free-air temperature range; typical values measured at T<sub>A</sub> = 25°C (unless otherwise noted).

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	Operating free-air temperature (T <sub>A</sub> )									UNIT			
			25°C			–40°C to 85°C			–55°C to 125°C						
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX				
V <sub>OH</sub>	High-level output voltage V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	4.5 V	I <sub>OH</sub> = –20 μA			4.4			4.4			4.4			V
			I <sub>OH</sub> = –4 mA			3.98			3.84			3.7			
V <sub>OL</sub>	Low-level output voltage V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	4.5 V	I <sub>OL</sub> = 20 μA			0.1			0.1			0.1			V
			I <sub>OL</sub> = 4 mA			0.26			0.33			0.4			
I <sub>I</sub>	Input leakage current V <sub>I</sub> = V <sub>CC</sub> and GND	I <sub>O</sub> = 0	5.5 V			±0.1			±1			±1			μA
I <sub>CC</sub>	Supply current V <sub>I</sub> = V <sub>CC</sub> or GND	I <sub>O</sub> = 0	5.5 V			2			20			40			μA
ΔI <sub>CC</sub> <sup>(1)</sup>	Additional Quiescent Device Current Per Input Pin. V <sub>I</sub> = V <sub>CC</sub> – 2.1		4.5 V to 5.5 V			100 360			450			490			μA
C <sub>i</sub>	Input capacitance		5 V			10			10			10			pF

(1) For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4 V, V<sub>CC</sub> = 5.5 V) specification is 1.8 mA.

## 5.6 Switching Characteristics

over operating free-air temperature range; typical values measured at T<sub>A</sub> = 25°C (unless otherwise noted).

PARAMETER	FROM	TO	TEST CONDITIONS	V <sub>CC</sub>	Operating free-air temperature (T <sub>A</sub> )									UNIT
					25°C			–40°C to 85°C			–55°C to 125°C			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t <sub>pd</sub>	A or B	Y	C <sub>L</sub> = 50 pF	4.5 V	32			40			48			ns
	A or B	Y	C <sub>L</sub> = 15 pF	5 V	13									
t <sub>t</sub>		Y	C <sub>L</sub> = 50 pF	4.5 V	15			19			22			ns

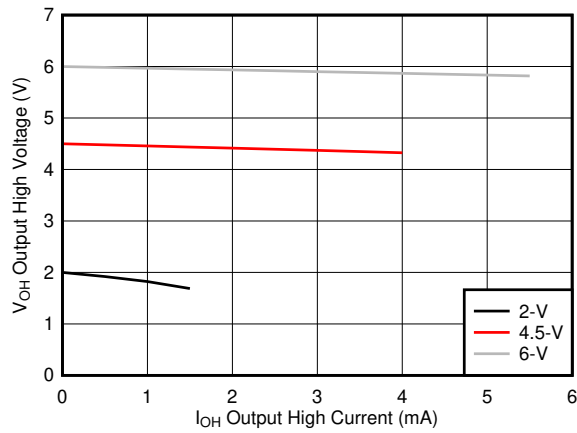
## 5.7 Operating Characteristics

over operating free-air temperature range; typical values measured at T<sub>A</sub> = 25°C (unless otherwise noted).

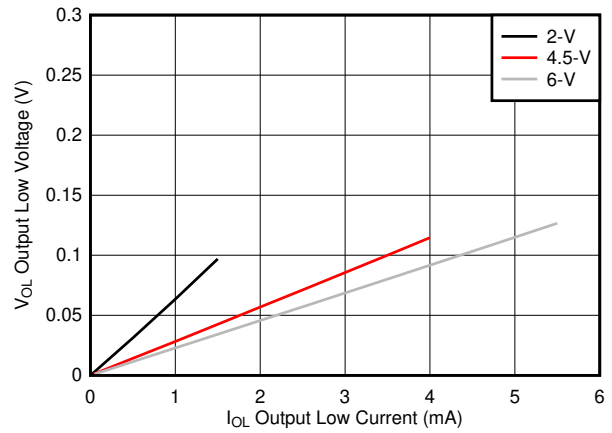
PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
C <sub>pd</sub>	Power dissipation capacitance per gate No load	5 V		27		pF

## 5.8 Typical Characteristics

$T_A = 25^\circ\text{C}$



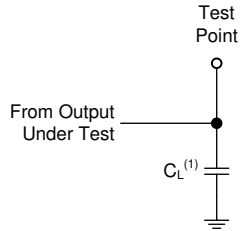
**5-1. Typical output voltage in the high state ( $V_{OH}$ )**



**5-2. Typical output voltage in the low state ( $V_{OL}$ )**

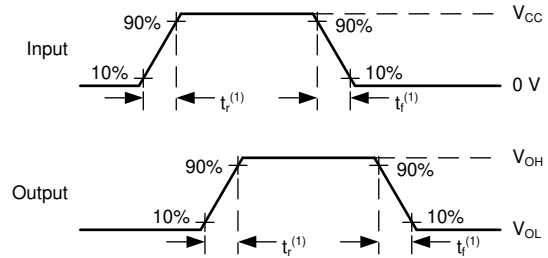
## 6 Parameter Measurement Information

- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_t < 6 \text{ ns}$ .
- The outputs are measured one at a time, with one input transition per measurement.



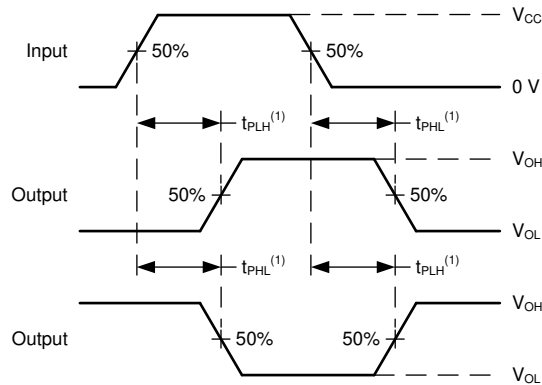
A.  $C_L = 50 \text{ pF}$  and includes probe and jig capacitance.

图 6-1. Load Circuit



A.  $t_t$  is the greater of  $t_r$  and  $t_f$ .

图 6-2. Voltage Waveforms Transition Times



A. The maximum between  $t_{PLH}$  and  $t_{PLH}$  is used for  $t_{pd}$ .

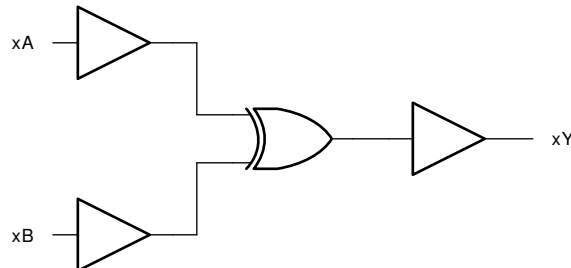
图 6-3. Voltage Waveforms Propagation Delays

## 7 Detailed Description

### 7.1 Overview

This device contains four independent 2-input XOR gates. Each gate performs the Boolean function  $Y = A \oplus B$  in positive logic.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

#### 7.3.1 Balanced CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to over-current. The electrical and thermal limits defined in the [セクション 5.1](#) must be followed at all times.

The CD74HCT86 can drive a load with a total capacitance less than or equal to the maximum load listed in the [セクション 5.6](#) connected to a high-impedance CMOS input while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed the provided load value. If larger capacitive loads are required, it is recommended to add a series resistor between the output and the capacitor to limit output current to the values given in the [セクション 5.1](#).

#### 7.3.2 TTL-Compatible CMOS Inputs

TTL-Compatible CMOS inputs are high impedance and are typically modeled as a resistor from the input to ground in parallel with the input capacitance given in the [セクション 5.5](#). The worst case resistance is calculated with the maximum input voltage, given in the [セクション 5.1](#), and the maximum input leakage current, given in the [セクション 5.5](#), using ohm's law ( $R = V \div I$ ).

Signals applied to the inputs need to have fast edge rates, as defined by  $\Delta t/\Delta v$  in the [セクション 5.3](#) to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the TTL-compatible CMOS input.

TTL-Compatible CMOS inputs have a lower threshold voltage than standard CMOS inputs to allow for compatibility with older bipolar logic devices. See the [セクション 5.3](#) for the valid input voltages for the CD74HCT86.



### 7.3.3 Clamp Diode Structure

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in 図 7-1.

注意

Voltages beyond the values specified in the セクション 5.1 table can cause damage to the device. The recommended input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

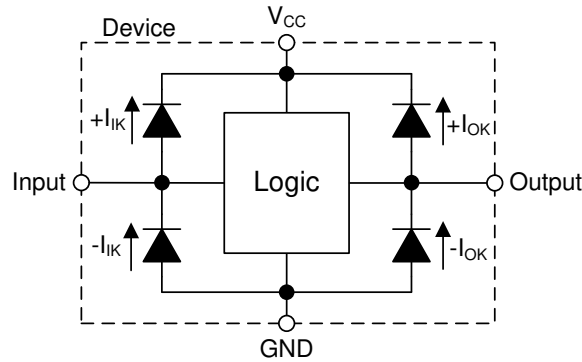


図 7-1. Electrical Placement of Clamping Diodes for Each Input and Output

### 7.4 Device Functional Modes

表 7-1. Function Table

INPUTS <sup>(1)</sup>		OUTPUT <sup>(2)</sup>
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

- (1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care  
 (2) H = Driving High, L = Driving Low, Z = High Impedance State

## 8 Application and Implementation

### 注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

### 8.1 Application Information

In this application, a 2-input XOR gate is used as a phase difference detector as shown in [図 8-1](#) . The remaining three gates can be used for other applications in the system, or the inputs can be grounded and the channels left unused.

The device is used to identify phase difference between a reference clock and another input clock. Whenever the clock states are different, the XOR output will pulse HIGH until the clocks return to the same state. The output is fed into a low-pass filter to obtain a DC representation of the phase difference.

### 8.2 Typical Application

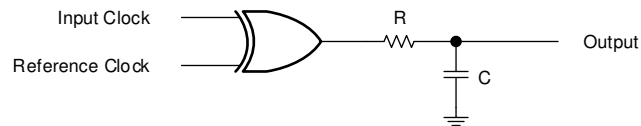


図 8-1. Typical application schematic

#### 8.2.1 Design Requirements

##### 8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the [セクション 5.3](#) . The supply voltage sets the device's electrical characteristics as described in the [セクション 5.5](#) .

The supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the CD74HCT86 plus the maximum supply current,  $I_{CC}$ , listed in the [セクション 5.5](#) . The logic device can only source or sink as much current as it is provided at the supply and ground pins, respectively. Be sure not to exceed the maximum total current through GND or  $V_{CC}$  listed in the [セクション 5.1](#) .

Total power consumption can be calculated using the information provided in [CMOS Power Consumption and  \$C\_{pd}\$  Calculation](#).

Thermal increase can be calculated using the information provided in [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#).

### 注意

The maximum junction temperature,  $T_J(\text{max})$  listed in the [セクション 5.1](#) , is an *additional limitation* to prevent damage to the device. Do not violate any values listed in the [セクション 5.1](#) . These limits are provided to prevent damage to the device.

##### 8.2.1.2 Input Considerations

Unused inputs must be terminated to either  $V_{CC}$  or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the CD74HCT86, as specified in the [セクション 5.5](#) , and the desired input transition rate. A 10-k $\Omega$  resistor value is often used due to these factors.

Refer to the [セクション 7.3](#) for additional information regarding the inputs for this device.

### 8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the  $V_{OH}$  specification in the [セクション 5.5](#). Similarly, the ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the  $V_{OL}$  specification in the [セクション 5.5](#).

Unused outputs can be left floating. Do not connect outputs directly to  $V_{CC}$  or ground.

Refer to [セクション 7.3](#) for additional information regarding the outputs for this device.

### 8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from  $V_{CC}$  to GND. The capacitor needs to be placed physically close to the device and electrically close to both the  $V_{CC}$  and GND pins. An example layout is shown in the [セクション 8.4](#).
2. Ensure the capacitive load at the output is  $\leq 70$  pF. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the CD74HCT86 to the receiving device.
3. Ensure the resistive load at the output is larger than  $(V_{CC} / I_{O(max)}) \Omega$ . This will ensure that the maximum output current from the [セクション 5.1](#) is not violated. Most CMOS inputs have a resistive load measured in megaohms; much larger than the minimum calculated above.
4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#)

### 8.2.3 Application Curves

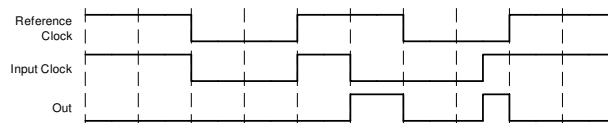


図 8-2. Typical application timing diagram

## 8.3 Power Supply Recommendations

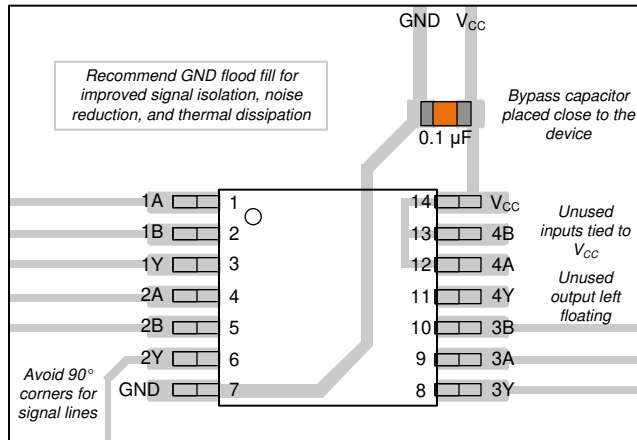
The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [セクション 5.3](#). Each  $V_{CC}$  terminal should have a bypass capacitor to prevent power disturbance. A 0.1- $\mu$ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- $\mu$ F and 1- $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in [図 8-3](#).

## 8.4 Layout

### 8.4.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

### 8.4.2 Layout Example



8-3. Example layout for the CD74HCT86

## 9 Device and Documentation Support

### 9.1 Documentation Support

#### 9.1.1 Related Documentation

For related documentation see the following:

- [HCMOS Design Considerations](#)
- [CMOS Power Consumption and CPD Calculation](#)
- [Designing with Logic](#)

### 9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[www.tij.co.jp](http://www.tij.co.jp) のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

### 9.3 サポート・リソース

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### 9.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 9.6 用語集

[テキサス・インスツルメンツ用語集](#)

この用語集には、用語や略語の一覧および定義が記載されています。

## 10 Revision History

Changes from Revision * (June 2020) to Revision A (August 2024)	Page
• 最新のデータシート規格を反映するように、文書全体の採番、書式設定、表、図、相互参照を更新.....	1
• 「製品情報」の表にパッケージ サイズを追加.....	1
• Updated RθJA values: D = 95.0 to 138.7, N = 62.3 to 103.8; Updated D and N packages for RθJC(top), RθJB, ΨJT, ΨJB, and RθJC(bot), all values in °C/W.....	4

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8984401CA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8984401CA CD54HCT86F3A	<a href="#">Samples</a>
CD54HCT86F	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54HCT86F	<a href="#">Samples</a>
CD54HCT86F3A	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8984401CA CD54HCT86F3A	<a href="#">Samples</a>
CD74HCT86E	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT86E	<a href="#">Samples</a>
CD74HCT86EE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT86E	<a href="#">Samples</a>
CD74HCT86M	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-55 to 125	HCT86M	
CD74HCT86M96	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-55 to 125	HCT86M	<a href="#">Samples</a>
CD74HCT86MT	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-55 to 125	HCT86M	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF CD54HCT86, CD74HCT86 :**

- Catalog : [CD74HCT86](#)
- Military : [CD54HCT86](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HCT86M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HCT86M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HCT86M96	SOIC	D	14	2500	356.0	356.0	35.0
CD74HCT86M96	SOIC	D	14	2500	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74HCT86E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT86E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT86EE4	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT86EE4	N	PDIP	14	25	506	13.97	11230	4.32

D0014A



# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

J 14

**GENERIC PACKAGE VIEW**  
**CDIP - 5.08 mm max height**  
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

# J0014A



## PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

### NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.



# EXAMPLE BOARD LAYOUT

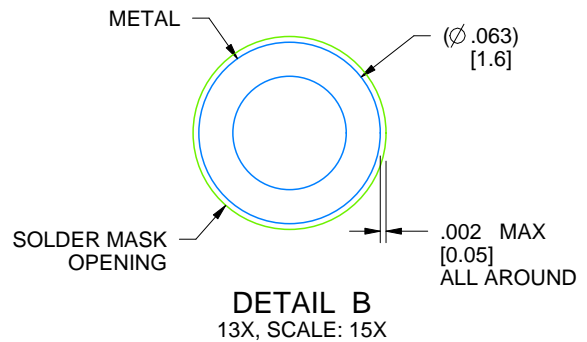
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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