CD74AC174 クリア搭載、ヘキサ D タイプ・フリップ・フロップ

1 特長

- AC タイプは 1.5V～5.5V で動作し、バランスのとれたノイズ耐性を電源電圧の 30% で実現
- シングル レール出力を備えた 6 つのフリップ フロップを内蔵
- バッファ付き入力
- バイポーラ F、AS、S の速度と消費電力の大幅な低減
- 伝搬遅延時間の平衡化
- ±24mA 出力駆動電流
  - 15 F デバイスへのファンアウト
- SCR ラッチアップ耐性の高い CMOS プロセスと回路設計

2 アプリケーション

- バッファ / ストレージ・レジスタ
- シフト・レジスタ

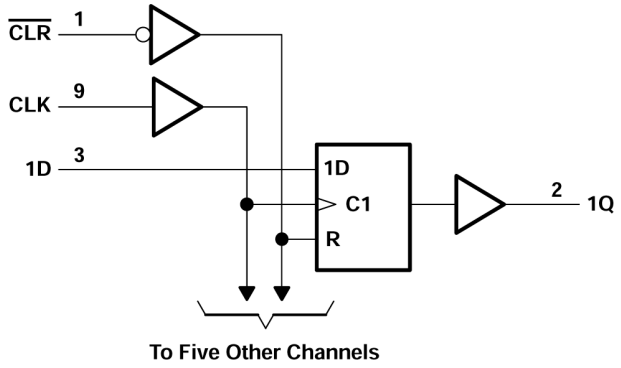
3 概要

CD74AC174 は、ダイレクト クリア ($\overline{CLR}$) 入力を備えたポジティブ エッジ トリガ D タイプ フリップ フロップで、1.5V～5.5V の V_{CC} で動作するよう設計されています。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)	本体サイズ (3)
CD74AC174	N (PDIP、16)	19.3mm × 9.4mm	19.3mm × 6.35mm
	D (SOIC、16)	9.9mm × 6mm	9.9mm × 3.9mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。
(3) 本体サイズ (長さ×幅) は公称値であり、ピンは含まれません。



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4 Pin Configuration and Functions

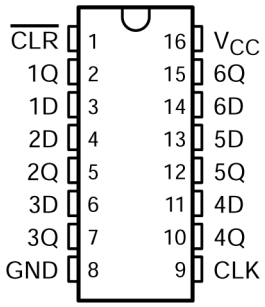


図 4-1. D or N Package (Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
$\overline{CLR}$	1	I	Clear Pin
1Q	2	O	1Q Output
1D	3	I	1D Input
2D	4	I	2D Input
2Q	5	O	2Q Output
3D	6	I	3D Input
3Q	7	O	3Q Output
GND	8	—	Ground Pin
CLK	9	I	Clock Pin
4Q	10	O	4Q Output
4D	11	I	4D Input
5Q	12	O	5Q Output
5D	13	I	5D Input
6D	14	I	6D Input
6Q	15	O	6Q Output
V_{CC}	16	P	Power Pin

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	6	V
I_{IK}	Input clamp current	(V_I < 0 V or V_I > V_{CC})(2)		±20	mA
I_{OK}	Output clamp current	(V_O < 0 V or V_O > V_{CC})(2)		±50	mA
I_O	Continuous output current	(V_O> 0 V or V_O < V_{CC})		±50	mA
	Continuous current through V_{CC} or GND			±150	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)(1)

			T_A = 25°C		–55°C to 125°C		–40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		1.5	5.5	1.5	5.5	1.5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 1.5 V	1.2		1.2		1.2		V
		V_{CC} = 3 V	2.1		2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 1.5 V		0.3		0.3		0.3	V
		V_{CC} = 3 V		0.9		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65		1.65	
V_I	Input voltage		0	V_{CC}	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 4.5 V to 5.5 V		-24		-24		-24	mA
I_{OL}	Low-level output current	V_{CC} = 4.5 V to 5.5 V		24		24		24	mA
Δt/Δv	Input transition rise or fall rate	V_{CC} = 1.5 V to 3 V		50		50		50	ns/V
		V_{CC} = 1.6 V to 5.5 V		20		20		20	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

5.4 Thermal Information

THERMAL METRIC(1)		CD74AC174		UNIT
		D (SOIC)	N (PDIP)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	106.6	67	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25 °C		–55°C to 125°C		–40°C to 85°C		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = -50 µA	1.5 V	1.4		1.4		1.4		V
			3 V	2.9		2.9		2.9		
			4.5 V	4.4		4.4		4.4		
		I_{OH} = -4 mA	3 V	2.58		2.4		2.48		
		I_{OH} = -24 mA	4.5 V	3.94		3.7		3.8		
		I_{OH} = -50 mA(1)	5.5 V			3.85				
		I_{OH} = -75 mA(1)	5.5 V					3.85		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 50 µA	1.5 V		0.1		0.1		0.1	V
			3 V		0.1		0.1		0.1	
			4.5 V		0.1		0.1		0.1	
		I_{OL} = 12 mA	3 V		0.36		0.5		0.44	
		I_{OL} = 24 mA	4.5 V		0.36		0.5		0.44	
		I_{OL} = 50 mA(1)	5.5 V				1.65			
		I_{OL} = 75 mA(1)	5.5 V						1.65	
I_I	V_I = V_{CC} or GND		5.5 V		±0.1		±1		±1	µA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	5.5 V		8		160		80	µA
C_i					10		10		10	pF

(1) Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.

5.6 Timing Requirements, V_{CC} = 1.5 V

over recommended operating free-air temperature range, V_{CC} = 1.5 V (unless otherwise noted)

			–55°C to 125°C		–40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			8		9	MHz
t_w	Pulse duration	$\overline{CLR}$ low	50		44		ns
		CLK high or low	65		57		
T_{su}	Setup time before CLK ↑	Data	2		2		ns
t_h	Hold time, data after CLK ↑		38		33		ns
t_{rec}	Recovery time, before CLK ↑	$\overline{CLR}$ ↑	1.5		1.5		ns

5.7 Timing Requirements, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

			–55°C to 125°C		–40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			68		77	MHz
t_w	Pulse duration	$\overline{CLR}$ low	5.6		4.9		ns
		CLK high or low	7.3		6.4		
T_{su}	Setup time before CLK ↑	Data	2		2		ns
t_h	Hold time, data after CLK ↑		4.2		3.7		ns
t_{rec}	Recovery time, before CLK ↑	$\overline{CLR}$ ↑	1.5		1.5		ns

5.8 Timing Requirements, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted)

			–55°C to 125°C		–40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			95		108	MHz
t_w	Pulse duration	$\overline{CLR}$ low	4		3.5		ns
		CLK high or low	5.2		4.6		
t_{su}	Setup time before CLK ↑	Data	2		2		ns
t_h	Hold time, data after CLK ↑		3		2.6		ns
t_{rec}	Recovery time, before CLK ↑	$\overline{CLR}$ ↑	1.5		1.5		ns

5.9 Switching Characteristics, V_{CC} = 1.5 V

over recommended operating free-air temperature range, V_{CC} = 1.5 V, C_L = 50 pF (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–55°C to 125°C		–40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
f_{max}			8		9		MHz
t_{PLH}	CLK	Any Q		169		154	ns
t_{PHL}				169		154	
t_{PLH}	$\overline{CLR}$	Any Q		181		165	ns
t_{PHL}				181		165	

5.10 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V, C_L = 50 pF (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–55°C to 125°C		–40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
f_{max}			68		77		MHz
t_{PLH}	CLK	Any Q	4.7	18.9	4.9	17.2	ns
t_{PHL}			4.7	18.9	4.9	17.2	
t_{PLH}	$\overline{CLR}$	Any Q	5.1	20.3	5.2	18.5	ns
t_{PHL}			5.1	20.3	5.2	18.5	

5.11 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V, C_L = 50 pF (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

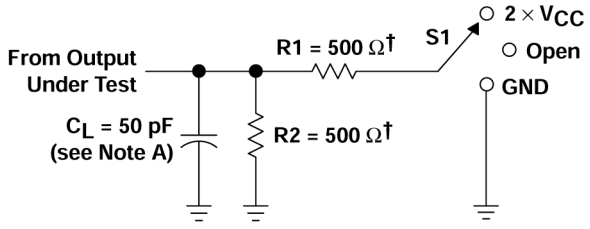
PARAMETER	FROM (INPUT)	TO (OUTPUT)	–55°C to 125°C		–40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
f_{max}			95		108		MHz
t_{PLH}	CLK	Any Q	3.4	13.5	3.5	12.3	ns
t_{PHL}			3.4	13.5	3.5	12.3	
t_{PLH}	$\overline{CLR}$	Any Q	3.6	14.5	3.7	13.2	ns
t_{PHL}			3.6	14.5	3.7	13.2	

5.12 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

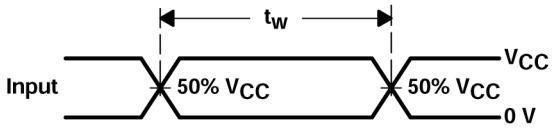
PARAMETER		TYP	UNIT
C_{pd}	Power dissipation capacitance	37	pF

6 Parameter Measurement Information

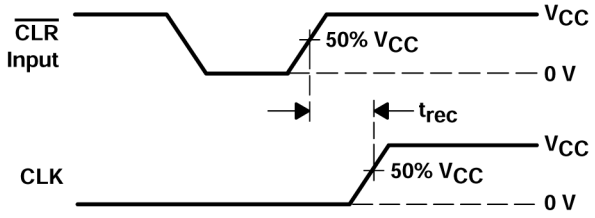


† When V_{CC} = 1.5 V, R1 = R2 = 1 kΩ

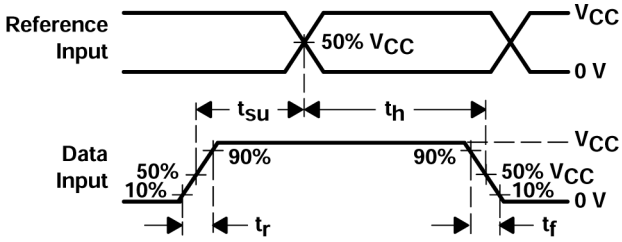
LOAD CIRCUIT



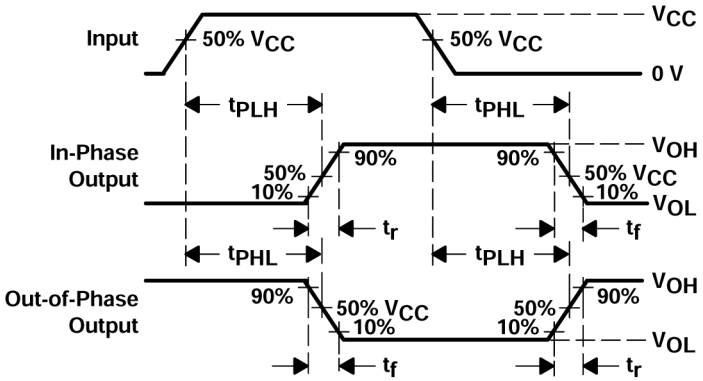
VOLTAGE WAVEFORMS
PULSE DURATION



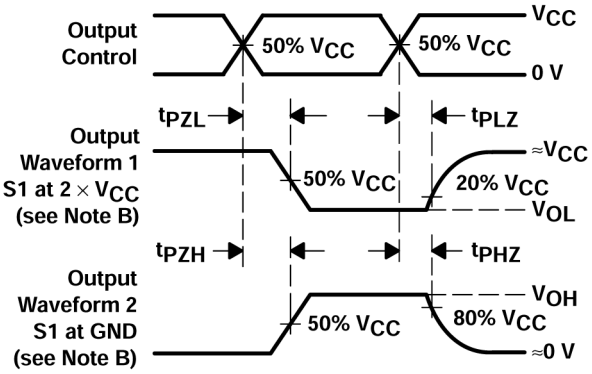
VOLTAGE WAVEFORMS
RECOVERY TIME



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
OUTPUT ENABLE AND DISABLE TIMES

図 6-1. Load Circuit and Voltage Waveforms

A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns. Phase relationships between waveforms are arbitrary.
D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
E. The outputs are measured one at a time with one input transition per measurement.
F. t_{PLH} and t_{PHL} are the same as t_{pd}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.
H. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
I. All parameters and waveforms are not applicable to all devices.

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

7 Detailed Description

7.1 Overview

Information at the data (D) inputs that meets the setup time requirements is transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going edge of CLK. When CLK is at either the high or low level, the D input has no effect at the output.

7.2 Functional Block Diagram

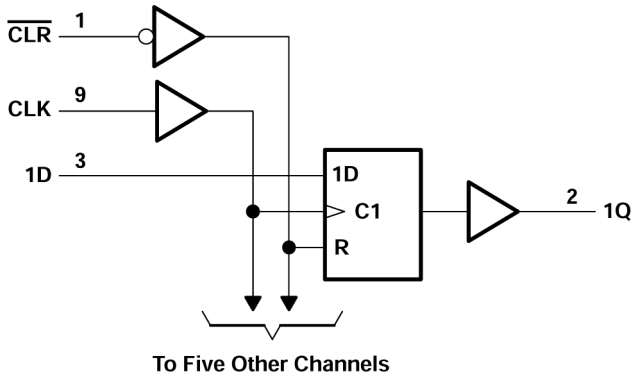


図 7-1. Logic Diagram (Positive Logic)

7.3 Device Functional Modes

表 7-1. Function Table (Each Flip-flop)

INPUTS			OUTPUT
$\overline{CLR}$	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in *セクション 5.3*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends 0.1 µF and if there are multiple V_{CC} terminals, then TI recommends .01 µF or .022 µF for each power terminal. It is okay to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

8.2 Layout

8.2.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient. It is generally okay to float outputs unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This does not disable the input section of the IOs so they cannot float when disabled.

9 Device and Documentation Support

9.1 Documentation Support (Analog)

9.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 9-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
CD74AC174	Click here	Click here	Click here	Click here	Click here

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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9.4 Trademarks

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9.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (November 2023) to Revision B (April 2024)	Page
• Updated thermal values for D package from RθJA = 73 to 106.6, all values in °C/W	4

Changes from Revision * (April 2003) to Revision A (November 2023)	Page
• 「パッケージ情報」表、「ピンの機能」表、「ESD 定格」表、「熱に関する情報」表、「デバイスの機能モード」、「アプリケーションと実装」セクション、「デバイスおよびドキュメントのサポート」セクション、および「メカニカル、パッケージ、および注文情報」セクションを追加	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74AC174E	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74AC174E	Samples
CD74AC174M96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC174M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

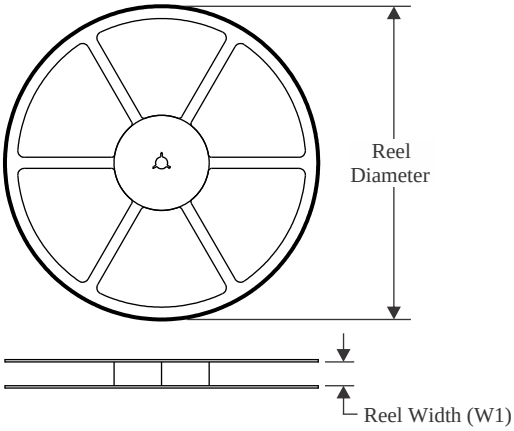
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

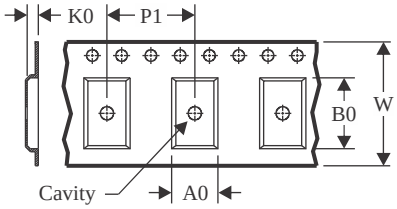
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

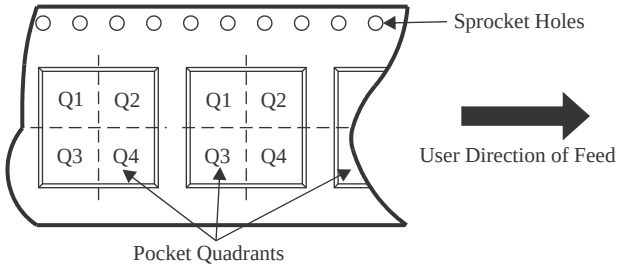


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

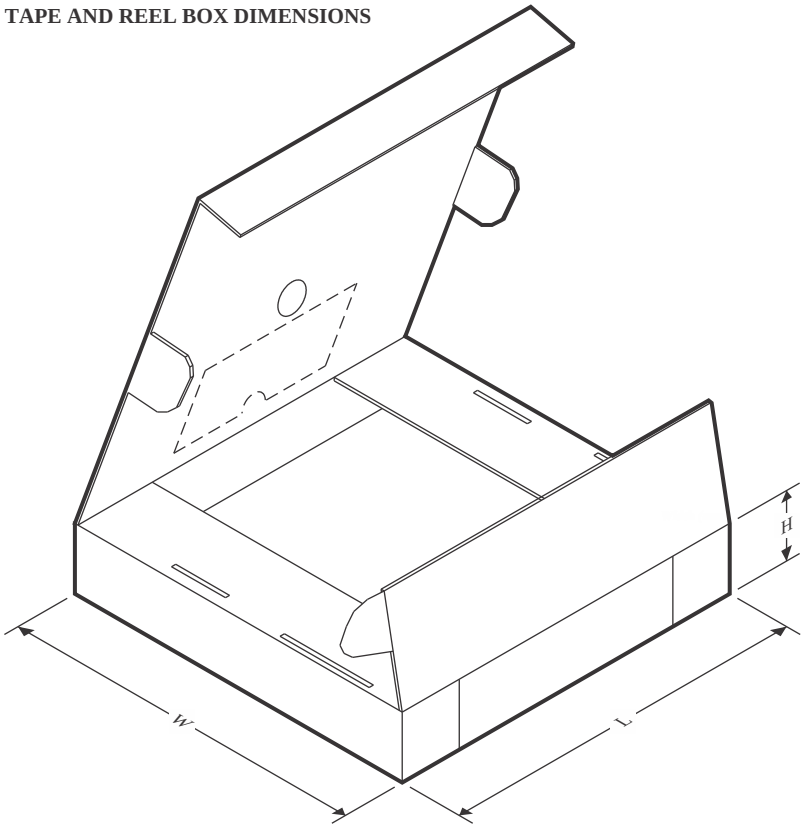
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74AC174M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

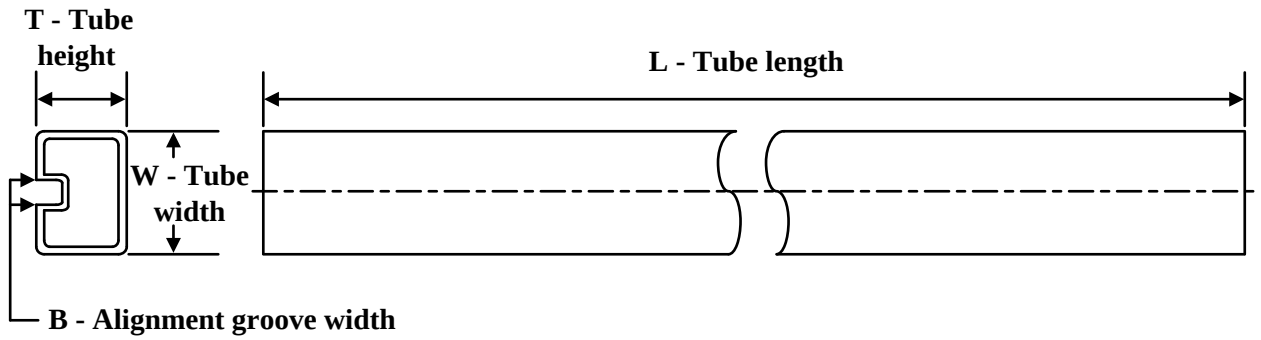
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74AC174M96	SOIC	D	16	2500	340.5	336.1	32.0

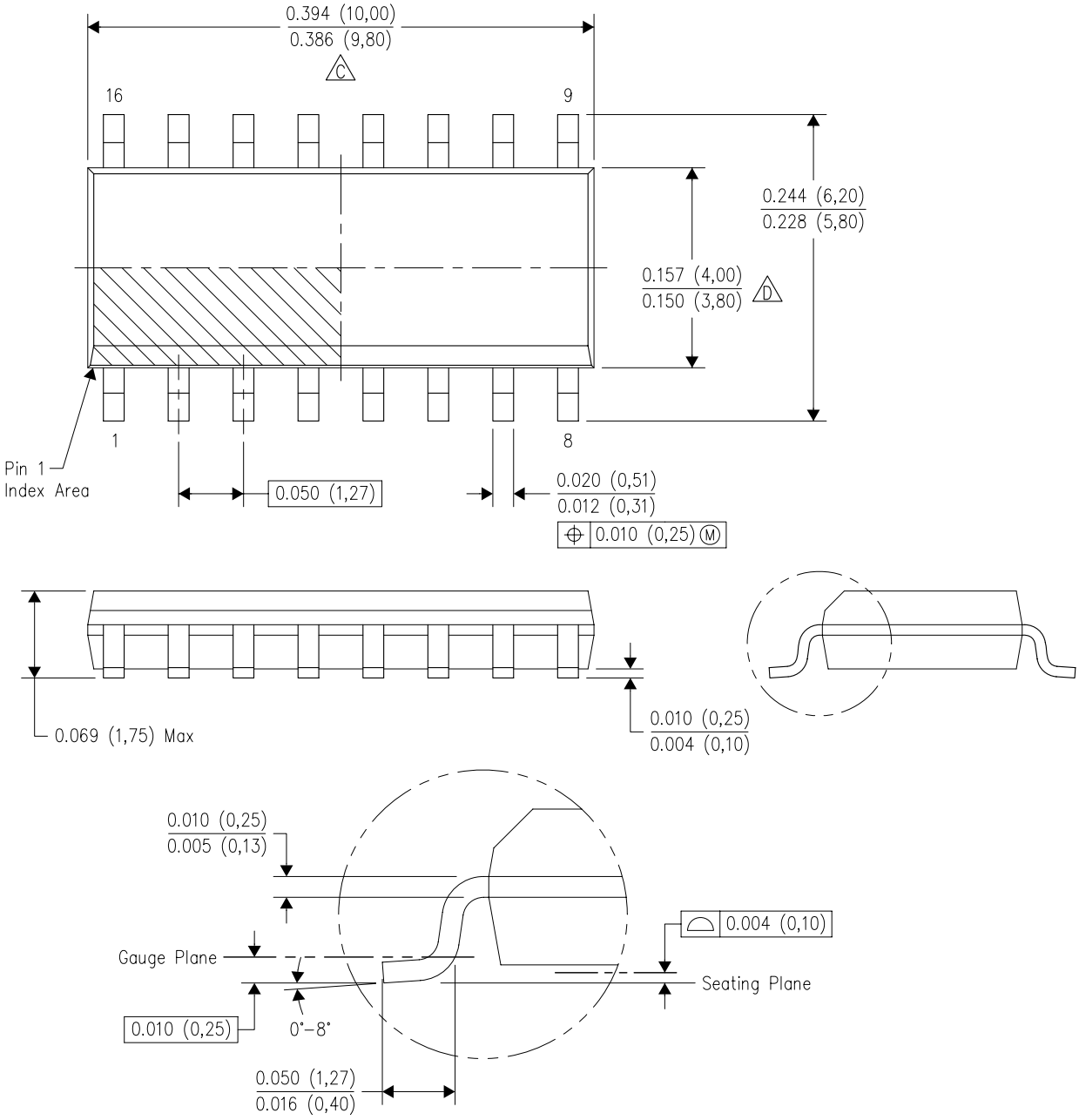
TUBE



*All dimensions are nominal

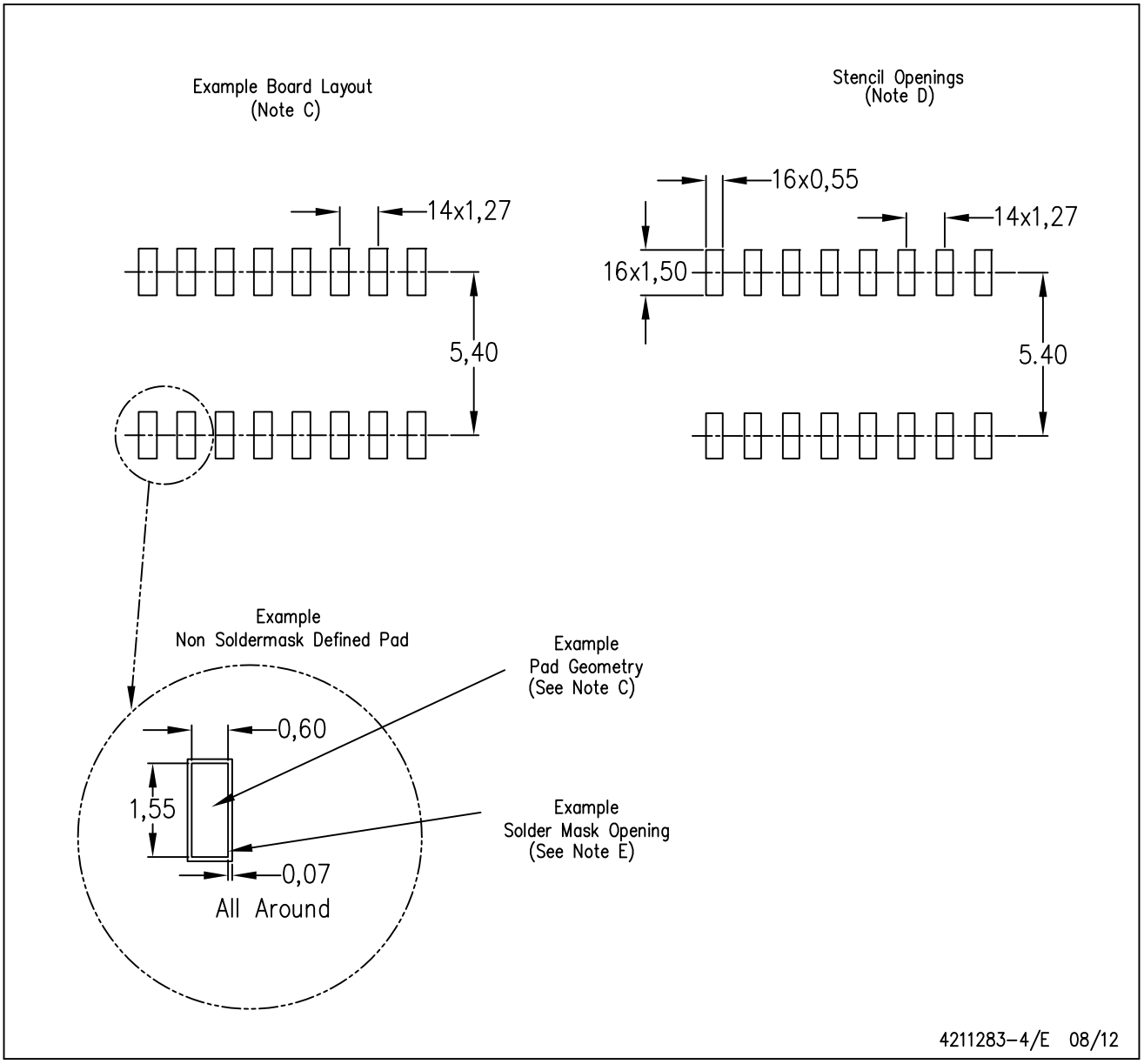
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74AC174E	N	PDIP	16	25	506	13.97	11230	4.32
CD74AC174E	N	PDIP	16	25	506	13.97	11230	4.32

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

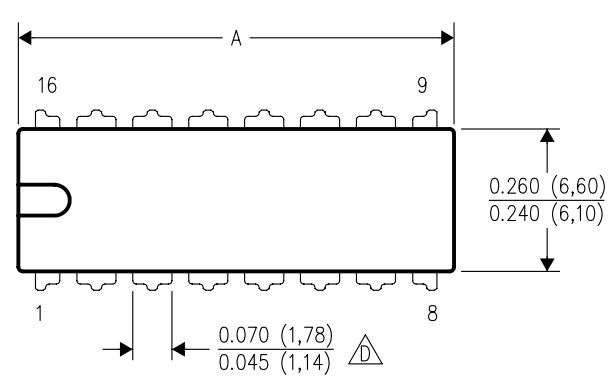


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

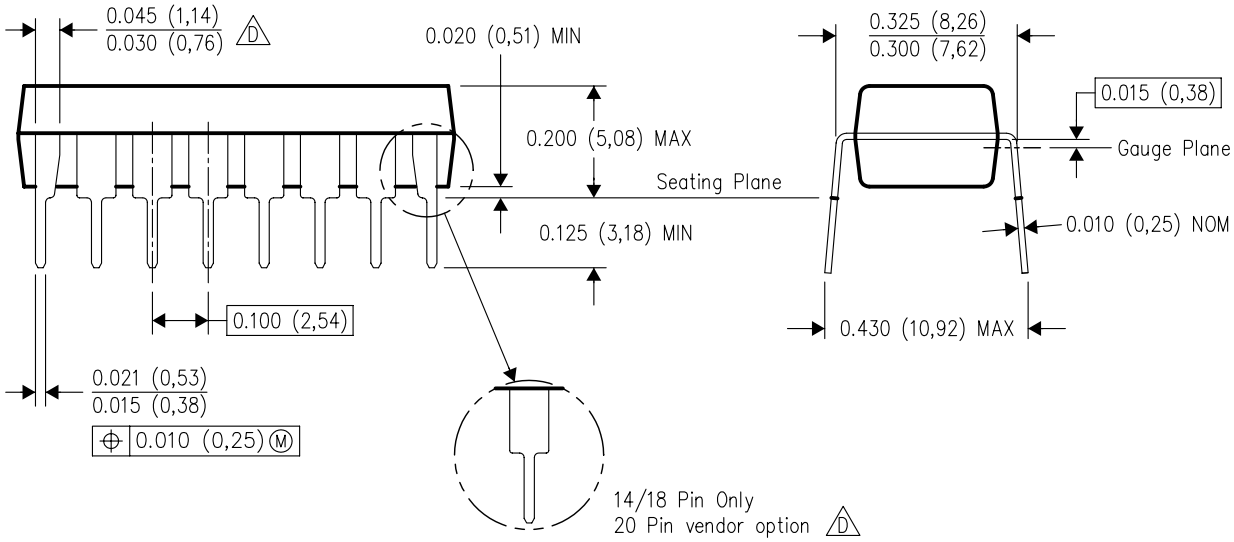
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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