TEXAS INSTRUMENTS
CD54HC283, CD74HC283, CD54HCT283, CD74HCT283
JAJSOX9E – NOVEMBER 1997 – REVISED JULY 2022

ハイスピード CMOS ロジック、高速桁上がり機能搭載、4 ビット、2 進全加算器

1 特長

- 2 つの 2 進数を加算
- 完全内部ルックアヘッド
- 高速リップル・キャリーによる経済的な拡張
- 正ロジックと負ロジックの両方で動作
- ファンアウト (全温度範囲にわたって)
  - 標準出力は 10 個の LSTTL 負荷を駆動可能
  - バス・ドライバ出力は 15 個の LSTTL 負荷を駆動可能
- 広い動作温度範囲:–55℃～125℃
- 平衡な伝搬遅延と遷移時間
- LSTTL ロジック IC に比べて消費電力を大幅削減
- HC タイプ
  - 2V～6V で動作
  - 優れたノイズ耐性:V_{CC} に対して N_{IL} = 30%、N_{IH} = 30% (V_{CC} = 5V 時)
- HCT タイプ
  - 4.5V～5.5V で動作
  - LSTTL 入力ロジックと直接互換、V_{IL} = 0.8V (最大値)、V_{IH} = 2V (最小値)
  - CMOS 入力互換、V_{OL}、V_{OH} で $I_I \leq 1\mu A$

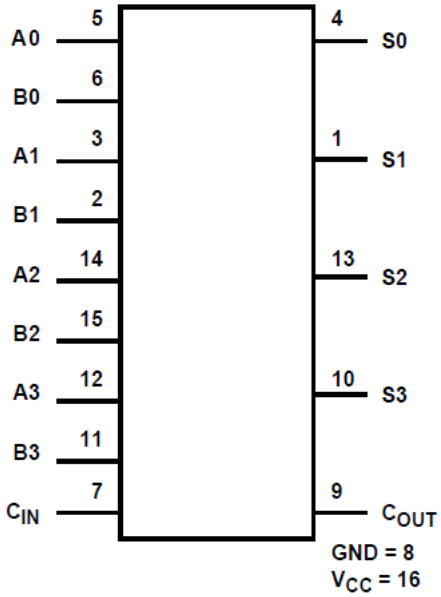
2 概要

CDx4HC283 および CDx4HCT283 は、4 ビットのバイナリ加算器を内蔵しています。CDx4HCT283 は TTL 電圧互換入力を備えています。

製品情報

部品番号	パッケージ (1)	本体サイズ (公称)
CD54HC283	J (CDIP) (16)	24.38mm × 6.92mm
CD74HC283CD74HC283	D (SOIC) (16)	9.90mm × 3.90mm
	N (PDIP) (16)	19.31mm × 6.35mm
CD74HCT283CD74HCT283	D (SOIC) (16)	9.90mm × 3.90mm
	N (PDIP) (16)	19.31mm × 6.35mm

(1) すべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



機能ダイアグラム

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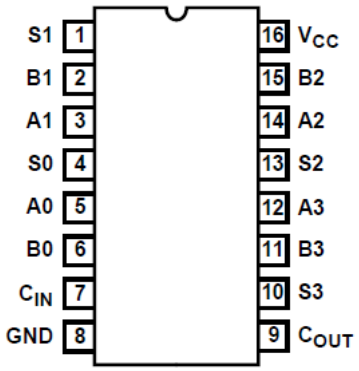
3 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (October 2003) to Revision E (July 2022)	Page
• 最新のデータシート規格を反映するように、文書全体の採番、書式設定、表、図、相互参照を更新	1

4 Pin Configuration and Functions



J, N, or D package
16-Pin CDIP, PDIP, or SOIC
Top View

5 Specifications

5.1 Absolute Maximum Ratings[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		– 0.5	7	V
I_{IK}	Input diode current	For $V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V		±20	mA
I_{OK}	Output diode current	For $V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V		±20	mA
I_O	Drain current, per output	For $–0.5 \text{ V} < V_O < V_{CC} + 0.5$ V		±25	mA
I_O	Output source or sink current per output pin	For $V_O > –0.5$ V or $V_O < V_{CC} + 0.5$ V		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature range		– 65	150	°C
	Lead temperature (Soldering 10s)(SOIC - lead tips only)			300	°C

(1) Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

5.2 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage range	HC types	2	6	V
V_I, V_O	DC input or output voltage		0	V_{CC}	V
	Input rise and fall time	2 V		1000	ns
		4.5 V		500	
		6 V		400	
T_A	Temperature range		–55	125	V

5.3 Thermal Information

THERMAL METRIC		D (SOIC) 16 PINS	N (PDIP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance[1]	73	67	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.4 Electrical Characteristics

PARAMETER		TEST CONDITIONS[2]	V_{CC} (V)	25℃			–40℃ to 85℃		–55℃ to 125℃		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
V_{IH}	High level input voltage		2	1.5			1.5		1.5		V
			4.5	3.15			3.15		3.15		
			6	4.2			4.2		4.2		
V_{IL}	Low level input voltage		2			0.5		0.5		0.5	V
			4.5			1.35		1.35		1.35	
			6			1.8		1.8		1.8	
V_{OH}	High level output voltage	I_{OH} = –20 μA	2	1.9			1.9		1.9		V
		I_{OH} = –20 μA	4.5	4.4			4.4		4.4		
		I_{OH} = –20 μA	6	5.9			5.9		5.9		
		I_{OH} = –4 mA	4.5	3.98			3.84		3.7		V
		I_{OH} = –5.2 mA	6	6			5.34		5.2		
V_{OL}	Low level output voltage	I_{OL} = 20 μA	2			0.1		0.1		0.1	V
		I_{OL} = 20 μA	4.5			0.1		0.1		0.1	
		I_{OL} = 20 μA	6			0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5			0.26		0.33		0.4	V
		I_{OL} = 5.2 mA	6			0.26		0.33		0.4	
I_I	Input leakage current	V_{CC} or GND	6			±0.1		±1		±1	μA
I_{CC}	Supply current	V_{CC} or GND	6			8		80		160	μA
HCT Types											
V_{IH}	High level input voltage		4.5 to 5.5	2			2		2		V
V_{IL}	Low level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V_{OH}	High level output voltage	I_{OH} = – 20 μA	4.5	4.4			4.4		4.4		V
V_{OH}		I_{OH} = – 4 mA	4.5	3.98			3.84		3.7		V
V_{OL}	Low level output voltage	I_{OL} = 20 μA	4.5			0.1		0.1		0.1	V
V_{OL}		I_{OL} = 4 mA	4.5			0.26		0.33		0.4	V
I_I	Input leakage current	V_{CC} to GND	5.5			±0.1		±1		±1	μA
I_{CC}	Supply current	V_{CC} or GND	5.5			8		80		160	μA
ΔI_{CC} [1]	Additional supply current per input pin	C_{IN} input held at V_{CC} – 2.1	4.5 to 5.5		100	540		675		735	μA
		B1, A1, A0 inputs held at V_{CC} – 2.1	4.5 to 5.5		100	360		450		490	μA
		B0 input held at V_{CC} – 2.1	4.5 to 5.5		100	144		180		196	μA
		B3, A3, A2, B2 inputs held at V_{CC} – 2.1	4.5 to 5.5		100	180		225		245	μA

(1) For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.
(2) $V_I = V_{IH}$ or V_{IL}, unless otherwise noted.

5.5 Switching Characteristics

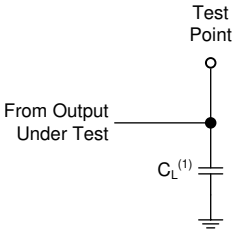
PARAMETER		TEST CONDITIONS	V_{CC} (V)	25℃			–40 to 85℃		–55℃ to 125℃		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
t_{PLH}, t_{PHL}	Propagation delay C_{IN} to S0	C_L = 50 pF	2			160		200		240	ns
			4.5			32		40		45	
		C_L = 15 pF	5		13						
		C_L = 50 pF	6			27		34		41	
t_{PLH}, t_{PHL}	C_{IN} to S1	C_L = 50 pF	2			180		225		270	ns
			4.5			36		45		54	
		C_L = 15 pF	5		15						
		C_L = 50 pF	6			31		38		46	
t_{PLH}, t_{PHL}	C_{IN} to S2, C_{IN} to C_{OUT}	C_L = 50 pF	2			195		245		295	ns
			4.5			39		49		59	
		C_L = 15 pF	5		16						
		C_L = 50 pF	6			33		42		50	
t_{PLH}, t_{PHL}	C_{IN} to S3	C_L = 50 pF	2			230		290		345	ns
			4.5			46		58		69	
		C_L = 15 pF	5		19						
		C_L = 50 pF	6			39		49		59	
t_{PLH}, t_{PHL}	An, Bn to C_{OUT}	C_L = 50 pF	2			195		245		295	ns
			4.5			39		49		59	
		C_L = 15 pF	5		16						
		C_L = 50 pF	6			33		42		50	
t_{PLH}, t_{PHL}	An, Bn to Sn	C_L = 5 0pF	2			210		265		315	ns
			4.5			42		53		63	
		C_L = 15 pF	5		18						
		C_L = 50 pF	6			36		45		54	
t_{TLH}, t_{THL}	Output transition time	C_L = 50 pF	2			75		95		110	ns
			4.5			15		19		22	
			6			13		16		19	
C_{IN}	Input capacitance	C_L = 50 pF	-			10		10		10	pF
C_{PD}	Power dissipation capacitance(1) (2)		5		70						pF
HCT TYPES											
t_{PLH}, t_{PHL}	Propagation delay C_{IN} to S0	C_L = 15 pF	5		13						ns
		C_L = 50 pF	4.5			31		39		47	
t_{PLH}, t_{PHL}	C_{IN} to S1	C_L = 15 pF	5		18						ns
		C_L = 50 pF	4.5			43		54		65	
t_{PLH}, t_{PHL}	C_{IN} to S2, C_{IN} to C_{OUT}	C_L = 15 pF	5		19						ns
		C_L = 50 pF	4.5			46		58		69	
t_{PLH}, t_{PHL}	C_{IN} to S3	C_L = 15 pF	5		22						ns
		C_L = 50 pF	4.5			53		66		80	
t_{PLH}, t_{PHL}	An, Bn to C_{OUT}	C_L = 15 pF	5		20						ns
		C_L = 50 pF	4.5			48		60		72	
t_{PLH}, t_{PHL}	An, Bn to Sn	C_L = 15 pF	5		21						ns
		C_L = 50 pF	4.5			49		61		74	

5.5 Switching Characteristics (continued)

PARAMETER		TEST CONDITIONS	V_{CC} (V)	25℃			–40 to 85℃		–55℃ to 125℃		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{TLH}, t_{THL}	Output transition time	C_L = 50 pF	4.5			15		19		22	ns
C_{IN}	Input capacitance					10		10		10	pF
C_{PD}	Power dissipation capacitance(1) (2)		5		82						pF

(1) C_{PD} is used to determine the dynamic power consumption, per package.
(2) $P_D = V_{CC}{}^2 f_i (C_{PD} + C_L)$ where: f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

6 Parameter Measurement Information



1. Includes probe and test-fixture capacitance.

図 6-1. Load Circuit for Push-Pull Output

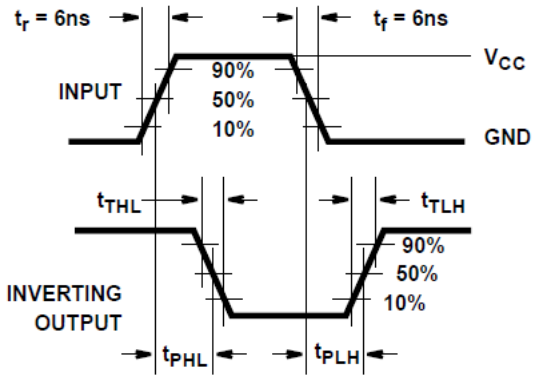


図 6-2. HC and HCT Transition Times and Propagation Delay Times, Combination Logic

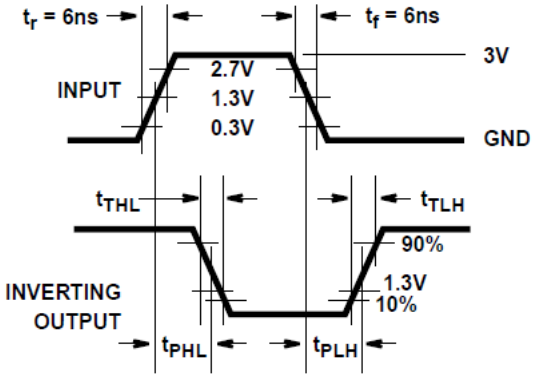


図 6-3. HCT Transition Times and Propagation Delay Times, Combination Logic

1. The greater between t_r and t_f is the same as t_t.
2. The greater between t_{plh} and t_{phl} is the same as t_{pd}.

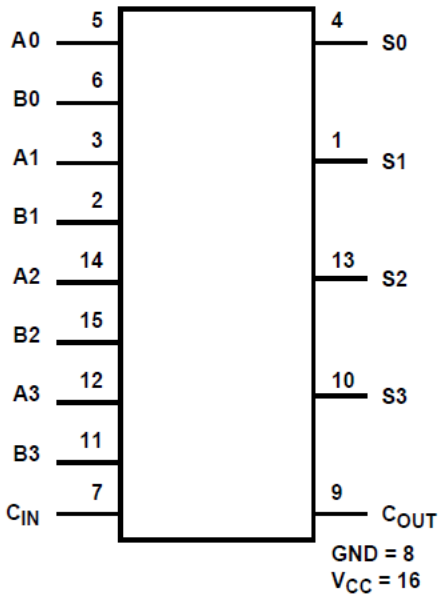
7 Detailed Description

7.1 Overview

The ’HC283 and ’HCT283 binary full adders add two 4-bit binary numbers and generate a carry-out bit if the sum exceeds 15.

Because of the symmetry of the add function, this device can be used with either all active-high operands (positive logic) or with all active-low operands (negative logic). When using positive logic the carry-in input must be tied low if there is no carry-in.

7.2 Functional Block Diagram



7.3 Feature Description

- Balanced CMOS Push-Pull Outputs
- Clamp Diode Structure

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8976501EA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8976501EA CD54HC283F3A	Samples
CD54HC283F3A	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8976501EA CD54HC283F3A	Samples
CD54HCT283F3A	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54HCT283F3A	Samples
CD74HC283E	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC283E	Samples
CD74HC283M96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	HC283M	Samples
CD74HCT283E	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT283E	Samples
CD74HCT283M	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-55 to 125	HCT283M	
CD74HCT283M96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	HCT283M	Samples
CD74HCT283MT	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-55 to 125	HCT283M	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF CD54HC283, CD54HCT283, CD74HC283, CD74HCT283 :

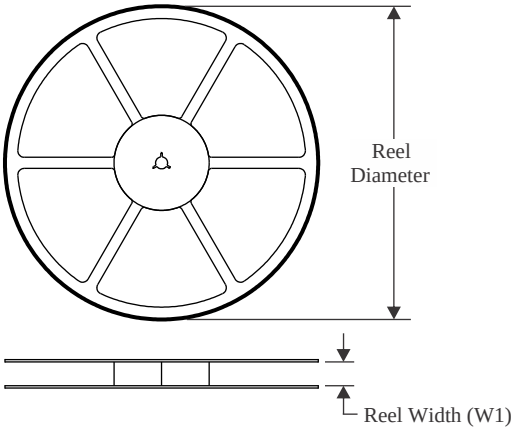
- Catalog : CD74HC283, CD74HCT283
- Military : CD54HC283, CD54HCT283

NOTE: Qualified Version Definitions:

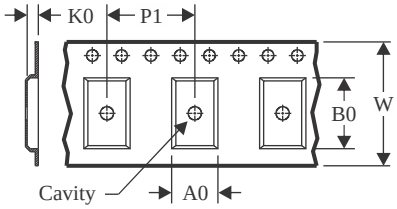
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

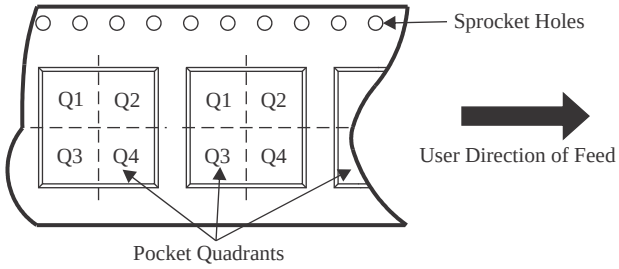


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

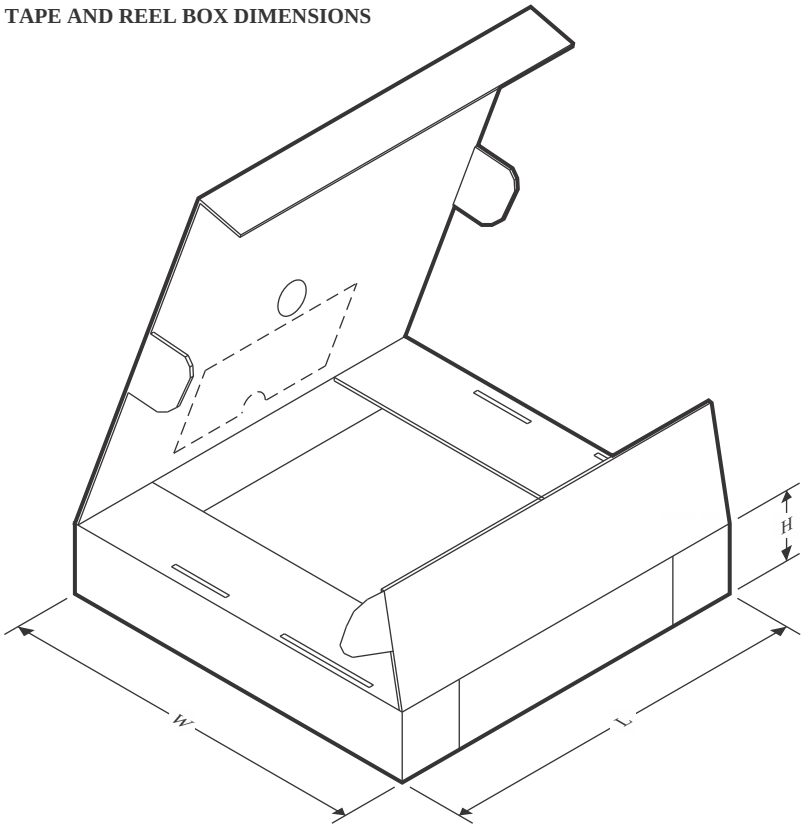
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC283M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT283M96	SOIC	D	16	2500	330.0	16.4	6.6	9.3	2.1	8.0	16.0	Q1
CD74HCT283M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

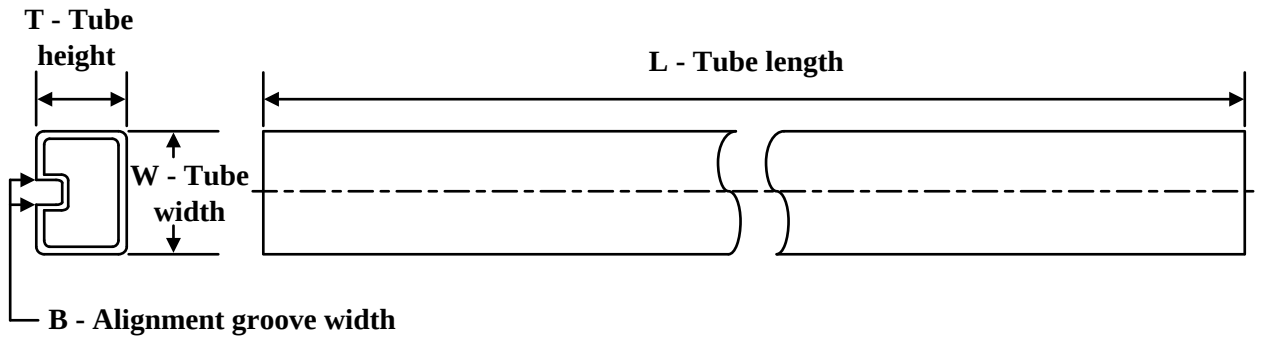
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC283M96	SOIC	D	16	2500	356.0	356.0	35.0
CD74HCT283M96	SOIC	D	16	2500	366.0	364.0	50.0
CD74HCT283M96	SOIC	D	16	2500	356.0	356.0	35.0

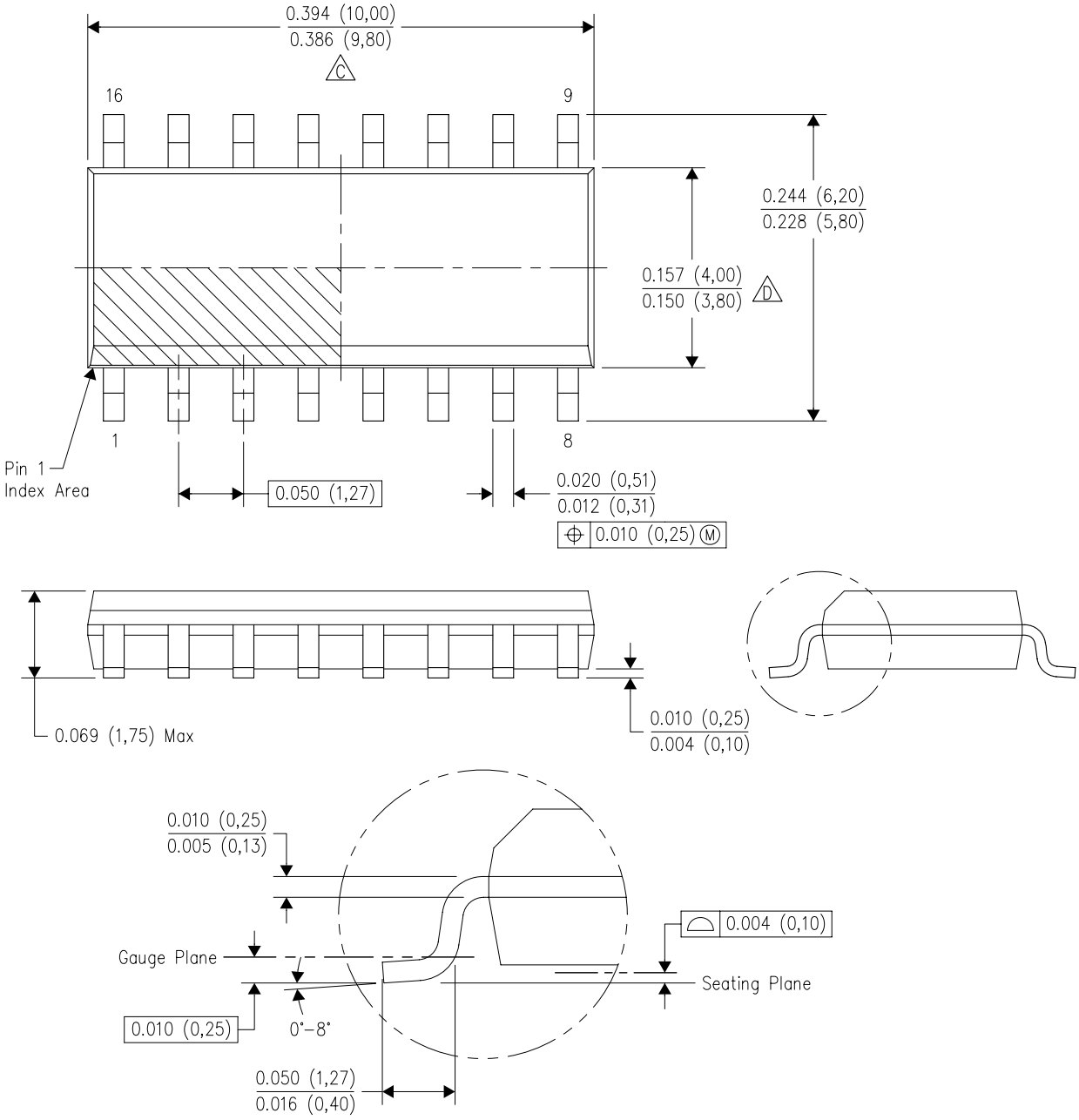
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74HC283E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC283E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT283E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT283E	N	PDIP	16	25	506	13.97	11230	4.32

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

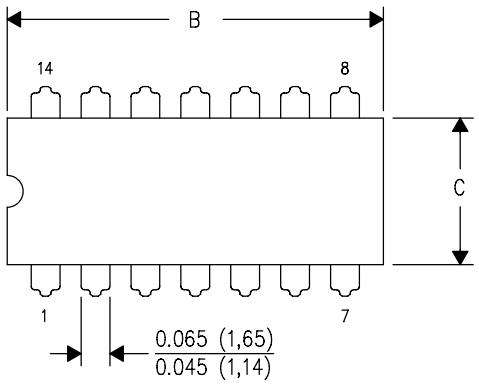


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

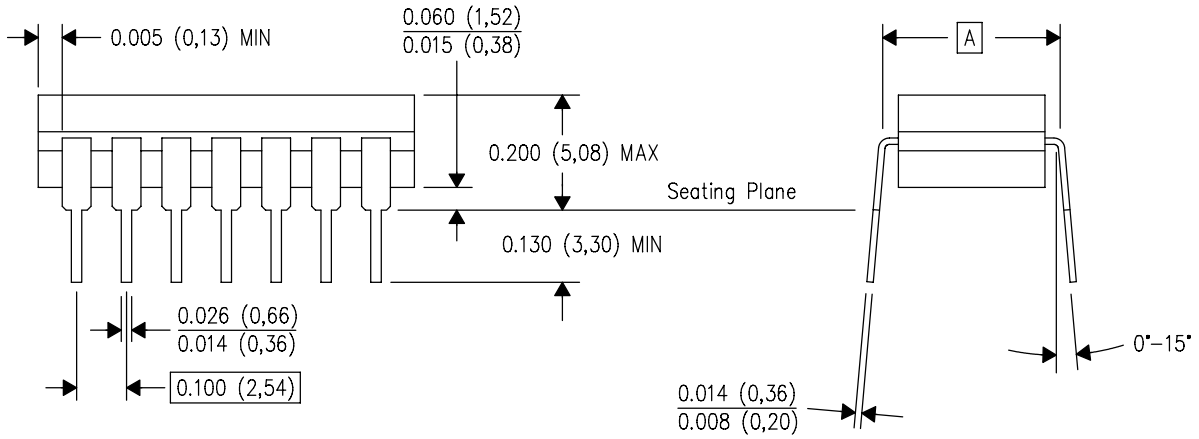
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



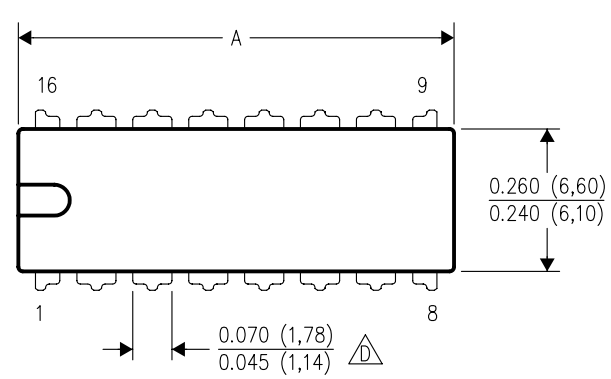
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

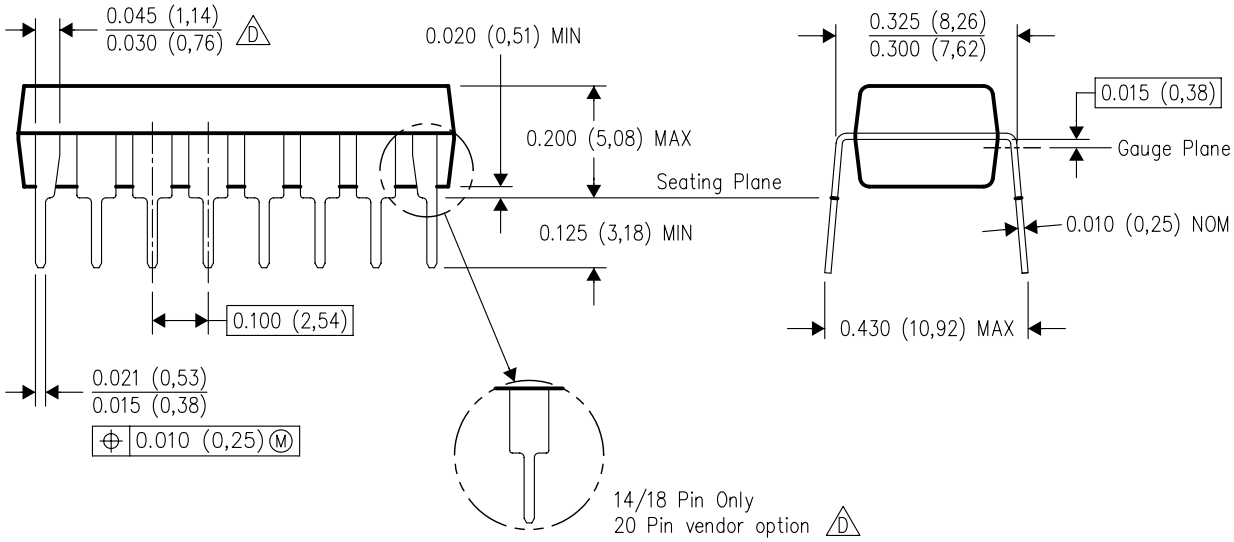
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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