

CD74HC93、CD74HCT93 ハイスピード CMOS ロジック、4 ビット・バイナリ・リップル・カウンタ

1 特長

- 2 分周、8 分周、16 分周の構成が可能
- 非同期リセット
- ファンアウト (全温度範囲にわたって)
 - 標準出力: 10 個の LSTTL 負荷
 - バス・ドライバ出力: 15 個の LSTTL 負荷
- 広い動作温度範囲: $-55^{\circ}\text{C} \sim 125^{\circ}\text{C}$
- 平衡な伝搬遅延と遷移時間
- LSTTL ロジック IC に比べて消費電力を大幅削減
- HC タイプ
 - 2V~6V で動作
 - 優れたノイズ耐性: $N_{IL} = V_{CC}$ の 30%, $N_{IH} = V_{CC}$ の 30%
- HCT タイプ
 - 4.5V~5.5V で動作
 - LSTTL 入力ロジックと直接互換、 $V_{IL} = 0.8\text{V}$ (最大値)、 $V_{IH} = 2\text{V}$ (最小値)
 - CMOS 入力互換、 V_{OL} 、 V_{OH} で $I_L \leq 1\mu\text{A}$

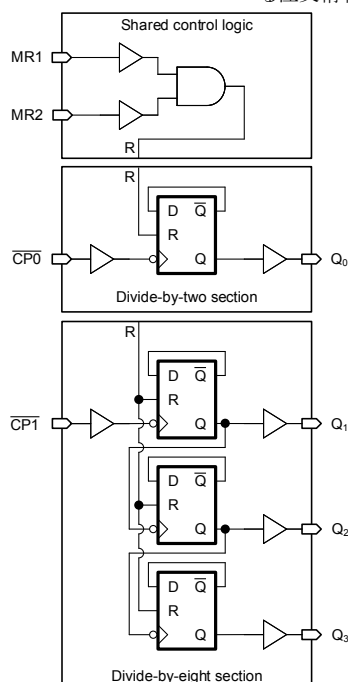
2 概要

CD74HC93 および CD74HCT93 は高速シリコン・ゲート CMOS デバイスで、低消費電力のショットキー TTL (LSTTL) とピン互換です。これらの 4 ビット・バイナリ・リップル・カウンタは、内部的に接続された 4 つのフリップ・フロップで構成されており、2 分周セクションと 8 分周セクションがあります。各セクションには個別のクロック入力 ($\overline{\text{CP0}}$ と $\overline{\text{CP1}}$) があり、High から Low へのクロックの遷移でカウンタの状態変化が開始されます。内部リップル遅延のため、 Q_n 出力の状態変化は同時に発生しません。このため、デコードされた出力信号にはデコーディング・スパイクが発生するため、クロックやストロブには使用しないでください。

デバイス情報

部品番号	パッケージ ⁽¹⁾	本体サイズ (公称)
CD74HC93M	SOIC (14)	8.65mm × 3.90mm
CD74HC93E	PDIP (14)	19.31mm × 6.35mm
CD74HCT93E	PDIP (14)	19.31mm × 6.35mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



機能ブロック図



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3 Revision History

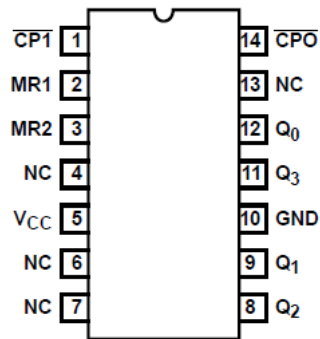
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (September 2003) to Revision D (March 2022)

Page

- 最新のデータシート規格を反映するように、文書全体の表、図、相互参照の採番と書式設定を更新..... 1

4 Pin Configuration and Functions



**N or D package
14-Pin PDIP or SOIC
Top View**

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	7	V
I _{IK}	Input diode current ⁽²⁾	(V _I < -0.5 V or V _I > V _{CC} + 0.5 V)	±20	mA
I _{OK}	Output diode current ⁽²⁾	(V _O < -0.5 V or V _O > V _{CC} + 0.5 V)	±20	mA
I _O	Output source or sink current per output pin	(V _O > -0.5 V or V _O < V _{CC} + 0.5 V)	±25	mA
	Continuous current through V _{CC} or GND		±50	mA
T _J	Junction temperature		150	°C
T _{stg}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	HC types		6	V
		HCT types	4.5	5.5	
V _I	Input voltage	0		V _{CC}	V
V _O	Output voltage	0		V _{CC}	V
t _t	Input transition rise/fall time	2 V		1000	ns
		4.5 V		500	
		6 V		400	
T _A	Operating free-air temperature	-55		125	°C

5.3 Thermal Information

THERMAL METRIC		D (SOIC)	N (PDIP)	UNIT
		14 PINS	14 PINS	
R _{θJA}	Junction-to-ambient thermal resistance ⁽¹⁾	86	80	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

5.4 Electrical Characteristics

PARAMETER		TEST CONDITIONS ⁽¹⁾	V _{CC} (V)	T _A = 25°C			– 40°C to 85°C		– 55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
V _{IH}	High level input voltage		2	1.5			1.5		1.5		V
			4.5	3.15			3.15		3.15		V
			6	4.2			4.2		4.2		V
V _{IL}	Low level input voltage		2	0.5			0.5		0.5		V
			4.5	1.35			1.35		1.35		V
			6	1.8			1.8		1.8		V
V _{OH}	High-level output voltage	I _{OH} = – 20 μA	2	1.9			1.9		1.9		V
		I _{OH} = – 20 μA	4.5	4.4			4.4		4.4		V
		I _{OH} = – 20 μA	6	5.9			5.9		5.9		V
		I _{OH} = – 4 mA	4.5	3.98			3.84		3.7		V
		I _{OH} = – 5.2 mA	6	5.48			5.34		5.2		V
V _{OL}	Low-level output voltage	I _{OL} = 20 μA	2	0.1			0.1		0.1		V
		I _{OL} = 20 μA	4.5	0.1			10.1		0.1		V
		I _{OL} = 20 μA	6	0.1			0.1		0.1		V
		I _{OL} = 4 mA	4.5	0.26			0.33		0.4		V
		I _{OL} = 5.2 mA	6	0.26			0.33		0.4		V
I _I	Input leakage current	V _{CC} or GND	6	±0.1			±1		±1		nA
I _{CC}	Supply current	V _{CC} or GND	6	8			80		160		μA
I _{CC}	Supply-current change	One input at 0.5 V or 2.4 V, Other inputs at 0 or V _{CC}	5.5	1.4 2.4			2.9				mA
C _i	Input capacitance		4.5 to 5.5	3 10			10				pF
HCT TYPES											
V _{IH}	High level input voltage		4.5 to 5.5	2			2		2		V
V _{IL}	Low level input voltage		4.5 to 5.5	0.8			0.8		0.8		V
V _{OH}	High level Output Voltage	I _{OH} = – 20 μA	4.5	4.4			4.4		4.4		V
		I _{OH} = – 4 mA	4.5	3.98			3.84		3.7		V
V _{OL}	Low level output voltage	I _{OH} = 20 μA	4.5	0.1			0.1		0.1		V
		I _{OH} = 4 mA	4.5	0.26			0.33		0.4		V
I _I	Input leakage current	V _{CC} or GND	5.5	±0.1			±1		±1		μA
I _{CC}	Supply current	V _{CC} or GND	5.5	8			80		160		μA
ΔI _{CC} ⁽²⁾ ⁽³⁾	Additional supply current per input pin	$\overline{CP0}, \overline{CP1}$	4.5 to 5.5	100 216			270		294		μA
		CLR1, CLR2	4.5 to 5.5	100 144			180		196		μA

(1) V_I = V_{IH} or V_{IL}, unless otherwise noted.

(2) For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specifications is 1.8 mA.

(3) Inputs held at V_{CC} – 2.1.

5.5 Prerequisite for Switching Characteristics

PARAMETER		V _{CC} (V)	25°C		– 40°C to 85°C		– 55°C to 125°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
HC TYPES									
f _{MAX}	Maximum clock frequency	2	6		5		4		MHz
		4.5	30		24		20		MHz
		6	35		28		24		MHz
t _W	Clock pulse width $\overline{CP0}$, $\overline{CP1}$	2	80		100		120		ns
		4.5	16		20		24		ns
		6	14		17		20		ns
t _W	Reset pulse width	2	80		100		120		ns
		4.5	16		20		24		ns
		6	14		17		20		ns
t _{REM}	Reset removal time	2	50		65		75		ns
		4.5	10		13		15		ns
		6	9		11		13		ns
HCT TYPES									
f _{MAX}	Maximum clock frequency	4.5	30		24		20		MHz
t _W	Clock pulse width $\overline{CP0}$, $\overline{CP1}$	4.5	16		20		24		ns
t _W	Reset pulse width	4.5	16		20		24		ns
t _{REM}	Reset removal time	4.5	10		13		15		ns

5.6 Switching Characteristics

Input t_r, t_f = 6ns. C_L = 50pF unless otherwise noted

PARAMETER		V _{CC} (V)	25°C			– 40°C to 85°C		– 55°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES										
t _{PLH} , t _{PHL}	$\overline{CP0}$ to Q0	2		125		155		190		ns
		4.5		10 ⁽¹⁾	25		31		38	ns
		6			21		26		32	ns
t _{PLH} , t _{PHL}	$\overline{CP1}$ to Q1	2		135		170		205		ns
		4.5			27		34		41	ns
		6			23		29		35	ns
t _{PLH} , t _{PHL}	$\overline{CP1}$ to Q2	2		185		230		280		ns
		4.5			37		46		56	ns
		6			31		39		48	ns
t _{PLH} , t _{PHL}	$\overline{CP1}$ to Q3	2		245		305		370		ns
		4.5		21 ⁽¹⁾	49		61		74	ns
		6			42		52		63	ns
t _{PLH} , t _{PHL}	MR1, MR2 to Qn	2		155		195		235		ns
		4.5		13 ⁽¹⁾	31		39		47	ns
		6			26		33		40	ns
t _{TLH} , t _{THL}	Output transition time	2		75		95		110		ns
		4.5			15		19		22	ns
		6			13		16		19	ns
C _{IN}	Input capacitance			10		10		10		pF

5.6 Switching Characteristics (continued)

Input t_r , t_f = 6ns. C_L = 50pF unless otherwise noted

PARAMETER		V_{CC} (V)	25°C			– 40°C to 85°C		– 55°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
C_{PD}	Power dissipation capacitance			25			10		19	pF
HCT TYPES										
t_{PLH} , t_{PHL}	$\overline{CP0}$ to Q0	4.5		14 ⁽¹⁾	34		43		51	ns
t_{PLH} , t_{PHL}	$\overline{CP1}$ to Q1	4.5			34		43		51	ns
t_{PLH} , t_{PHL}	$\overline{CP1}$ to Q2	4.5			46		58		69	ns
t_{PLH} , t_{PHL}	$\overline{CP1}$ to Q3	4.5		24 ⁽¹⁾	58		73		87	ns
t_{PLH} , t_{PHL}	MR1, MR2 to Qn	4.5		13 ⁽¹⁾	33		41		50	ns
t_{TLH} , t_{THL}	Output Transition time	4.5			15		19		22	ns
C_{IN}	Input Capacitance				10		10		10	pF
C_{PD}	Power dissipation capacitance			25						pF

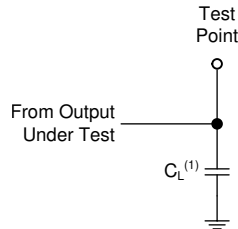
(1) C_L = 15pF. V_{CC} = 5.

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_t < 6 \text{ ns}$.

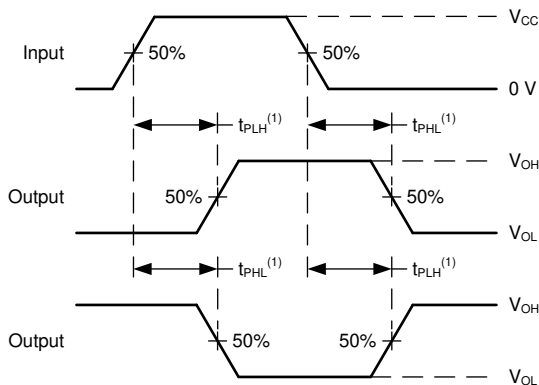
For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



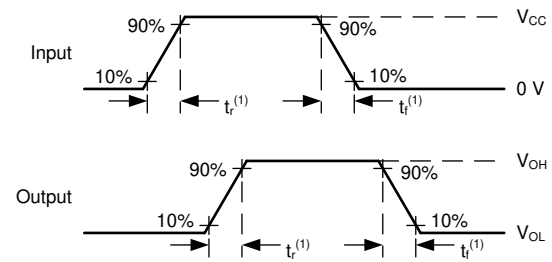
(1) C_L includes probe and test-fixture capacitance.

6-1. Load Circuit for Push-Pull Outputs



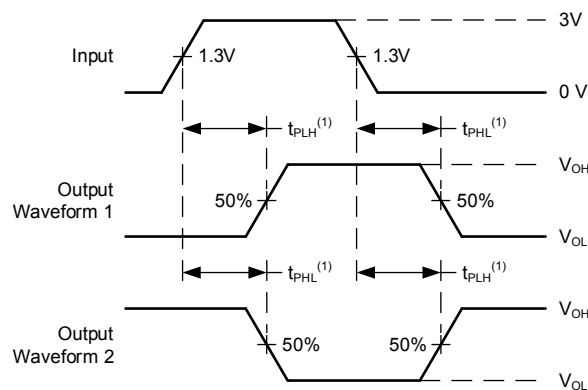
(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd} .

6-2. Voltage Waveforms, Propagation Delays for Standard CMOS Inputs



(1) The greater between t_r and t_f is the same as t_t .

6-3. Voltage Waveforms, Input and Output Transition Times for Standard CMOS Inputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd} .

6-4. Voltage Waveforms, Propagation Delays for TTL-Compatible Inputs

7 Detailed Description

7.1 Overview

The CD74HC93 and CD74HCT93 are high-speed silicon-gate CMOS devices and are pin-compatible with low power Schottky TTL (LSTTL). These 4-bit binary ripple counters consist of four flip-flops internally connected to provide a divide-by-two section and a divide-by-eight section. Each section has a separate clock input ($\overline{CP0}$ and $\overline{CP1}$) to initiate state changes of the counter on the HIGH to LOW clock transition. State changes of the Q_n outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

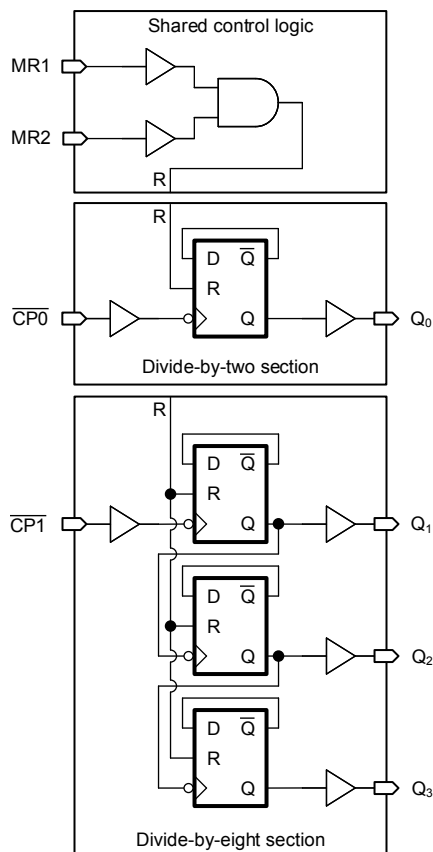
A gated AND asynchronous reset (MR1 and MR2) is provided which overrides both clocks and resets (clears) all flip-flops.

Because the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes.

In a 4-bit ripple counter the output Q_0 must be connected externally to input $\overline{CP1}$. The input count pulses are applied to clock input $\overline{CP0}$. Simultaneous frequency divisions of 2, 4, 8, and 16 are performed at the Q_0 , Q_1 , Q_2 , and Q_3 outputs as shown in the function table. As a 3-bit ripple counter the input count pulses are applied to input $\overline{CP1}$.

Simultaneous frequency divisions of 2, 4, and 8 are available at the Q_1 , Q_2 , Q_3 outputs. Independent use of the first flipflop is available if the reset function coincides with the reset of the 3-bit ripple-through counter.

7.2 Functional Block Diagram



7-1. Functional Block Diagram

7.3 Device Functional Modes

Truth Table

COUNT	OUTPUTS ⁽¹⁾			
	Q ₀	Q ₁	Q ₂	Q ₃
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

(1) H = High voltage level, L = Low voltage level.

表 7-1. Mode Selection

RESET OUTPUTS		OUTPUTS ⁽¹⁾			
MR1	MR2	Q ₀	Q ₁	Q ₂	Q ₃
H	H	L	L	L	L
L	H	Count	Count	Count	Count
H	L				
L	L				

(1) H = High voltage level, L = Low voltage level.

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μF and 1- μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 サポート・リソース

[TI E2E™ サポート・フォーラム](#)は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HC93E	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC93E	Samples
CD74HC93EE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC93E	Samples
CD74HC93M	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-55 to 125	HC93M	
CD74HC93M96	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-55 to 125	HC93M	Samples
CD74HC93MT	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-55 to 125	HC93M	
CD74HCT93E	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT93E	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC93M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HC93M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC93M96	SOIC	D	14	2500	356.0	356.0	35.0
CD74HC93M96	SOIC	D	14	2500	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74HC93E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC93E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC93EE4	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC93EE4	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT93E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT93E	N	PDIP	14	25	506	13.97	11230	4.32

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.



D0014A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



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NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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