

2.5V および 3.3V 出力付き、 CDCE813-Q1 プログラマブル 1-PLL クロック シンセサイザおよびジッタ クリ ーナ

1 特長

- 車載アプリケーション認定済み
- 以下の結果で AEC-Q100 認定済み:
 - デバイス温度グレード 2:動作時周囲温度範囲 $-40^{\circ}\text{C}\sim 105^{\circ}\text{C}$
 - デバイス HBM ESD 分類レベル H2
 - デバイス CDM ESD 分類レベル C6
- システム内プログラミングおよび EEPROM
 - シリアル プログラム可能な揮発性レジスタ
 - 不揮発性 EEPROM に顧客設定を保存
- 柔軟な入力クロック設定の概念
 - 外部水晶振動子: $8\text{MHz}\sim 32\text{MHz}$
 - シングルエンドの LVCMOS: 最高 160MHz
- 出力周波数を最高 230MHz まで自由に選択可能
- 低ノイズの PLL コア
 - PLL ループ フィルタ コンポーネントを内蔵
 - 短いジッタ時間 (標準値 50ps)
- 1.8V デバイス電源 (コア電圧)
- 独立した出力供給ピン: 3.3V および 2.5V
- 柔軟なクロックドライバ
 - 3 つのユーザ定義可能な制御入力 [S0, S1, S2] を、SSC 選択、周波数切り替え、出力イネーブル、電源オフなどに使用可能
 - ビデオ、オーディオ、USB、IEEE1394、RFID、Bluetooth®, WLAN、イーサネット、GPS に高精度のクロックを生成
 - TI-DaVinci™、OMAP™、DSP を使用して共通クロックの周波数を生成
 - SSC 変調をプログラム可能
 - 0PPM クロック生成が可能
- TSSOP パッケージ
- 開発およびプログラミング キットにより PLL の設計とプログラムが容易 (TI ClockPro™ プログラミング ソフトウェア)

2 アプリケーション

- クラスタ
- ヘッドユニット
- ナビゲーションシステム
- 先進運転支援システム (ADAS)

3 概要

CDCE813-Q1 デバイスは、位相ロック ループ(PLL)をベースとし、低コスト、高性能でプログラマブルな、モジュール式のクロック シンセサイザです。単一の入力周波数から最大 3 つの出力クロックを生成できます。それぞれの出力は、内蔵の構成可能 PLL を使用して、 230MHz までの任意のクロック周波数にシステム内でプログラム可能です。

CDCE813-Q1 には独立した出力電源ピン V_{DDOUT} があり、 $2.5\text{V}\sim 3.3\text{V}$ を供給します。

入力には外付けの水晶振動子、または LVCMOS クロック信号を接続できます。選択可能なオンチップ VCXO により、出力周波数を外部の制御信号に同期できます。

PLL は SSC (スペクトラム拡散クロッキング) をサポートしているため、電磁気干渉(EMI)性能に優れています。

このデバイスは不揮発性 EEPROM のプログラミングをサポートしているため、アプリケーションに応じて簡単にカスタマイズ可能です。すべてのデバイス設定は、2 線式シリアル インターフェイスの I²C バスでプログラムできます。

CDCE813-Q1 は 1.8V のコア環境で動作し、独立した水晶発振器を追加する必要がないため、部品数と基板サイズを削減できます。このデバイスは、 $-40^{\circ}\text{C}\sim 105^{\circ}\text{C}$ の温度範囲で動作します。

パッケージ情報

部品番号	パッケージ ⁽¹⁾	パッケージ サイズ ⁽²⁾
CDCE813-Q1	PW (TSSOP, 14)	5mm × 6.4mm

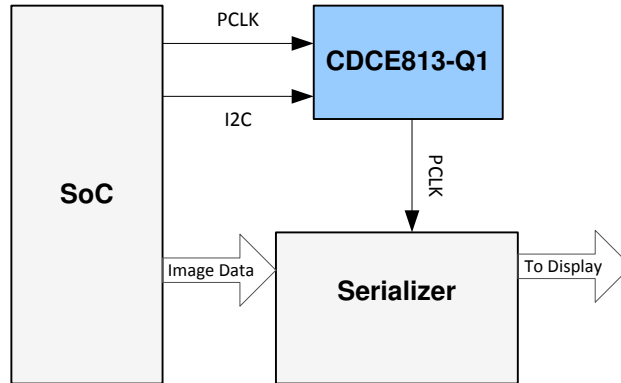
- (1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
- (2) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。

デバイスの比較

注文可能製品	S0 制御ピンのデフォルト機能
CDCE813R02-Q1	Y1 出力イネーブル (アクティブ HIGH)
CDCE813-Q1	未使用 ⁽¹⁾

- (1) 出力は I²C 制御によりイネーブルにする必要があります。





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代表的なアプリケーション回路図

Table of Contents

1 特長	1	8 Application and Implementation	19
2 アプリケーション	1	8.1 Application Information.....	19
3 概要	1	8.2 Typical Application.....	19
4 Pin Configuration and Functions	4	8.3 Power Supply Recommendations.....	23
5 Specifications	5	8.4 Layout.....	23
5.1 Absolute Maximum Ratings.....	5	9 Register Maps	25
5.2 ESD Ratings.....	5	9.1 I ² C Configuration Registers.....	25
5.3 Recommended Operating Conditions.....	5	10 デバイスおよびドキュメントのサポート	29
5.4 Thermal Information.....	6	10.1 ドキュメントのサポート.....	29
5.5 Electrical Characteristics.....	6	10.2 ドキュメントの更新通知を受け取る方法.....	29
5.6 Timing Requirements.....	8	10.3 サポート・リソース.....	29
5.7 Typical Characteristics.....	10	10.4 商標.....	29
6 Parameter Measurement Information	11	10.5 静電気放電に関する注意事項.....	29
7 Detailed Description	12	10.6 用語集.....	29
7.1 Overview.....	12	11 Revision History	30
7.2 Functional Block Diagram.....	12	12 Mechanical, Packaging, and Orderable Information	31
7.3 Feature Description.....	13		
7.4 Device Functional Modes.....	16		
7.5 Programming.....	16		

4 Pin Configuration and Functions

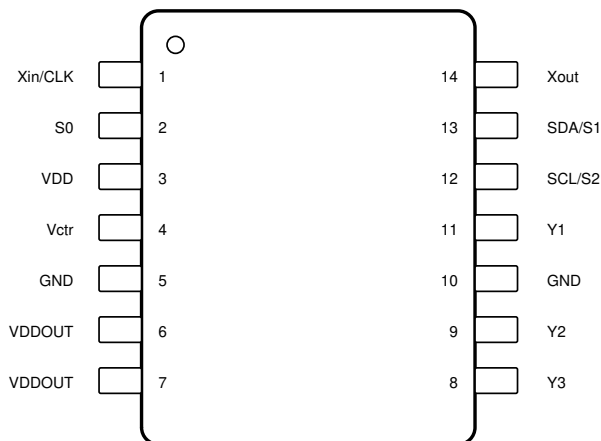


図 4-1. PW Package 14-Pin TSSOP Top View

表 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
GND	5, 10	G	Ground
SCL/S2	12	I	SCL: serial clock input LVCMOS (default configuration), 500-kΩ internal pullup; or S2: user-programmable control input, LVCMOS input, 500-kΩ internal pullup
SDA/S1	13	I/O or I	SDA: bidirectional serial data input or output (default configuration), LVCMOS internal pullup; or S1: user-programmable control input, LVCMOS input, 500-kΩ internal pullup
S0	2	I	User-programmable control input S0, LVCMOS input, 500-kΩ internal pullup CDCE813-Q1 default: S0 = 1: Y1 is 3-state, S0 = 0: Y1 is 3-state CDCE813R02-Q1 default: S0 = 1: Y1 is enabled, S0 = 0: Y1 is 3-state
V _{ctr}	4	I	VCXO control voltage (leave open or pull up when not used)
V _{DD}	3	P	1.8-V power supply for the device
V _{DDOUT}	6, 7	P	3.3-V or 2.5-V supply for all outputs
Xin/CLK	1	I	Crystal oscillator input or LVCMOS clock input (selectable through the I ² C bus)
Xout	14	O	Crystal oscillator output (leave open or pull up when not used)
Y1	11	O	LVCMOS output
Y2	9	O	LVCMOS output
Y3	8	O	LVCMOS output

(1) G = Ground, I = Input, O = Output, P = Power

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{DD}	Supply voltage		-0.5	2.5	V
V _{DDOUT}	Output clocks supply voltage	CDCE813-Q1	-0.5	3.6 + 0.5	V
V _I	Input voltage ^{(2) (3)}		-0.5	V _{DD} + 0.5	V
V _O	Output voltage ⁽²⁾		-0.5	V _{DDOUT} + 0.5	V
I _I	Input current (V _I < 0, V _I > V _{DD})			20	mA
I _O	Continuous output current			50	mA
T _J	Maximum junction temperature			125	°C
T _{stg}	Storage temperature		-65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) SDA and SCL can go up to 3.6 V as stated in the *Recommended Operating Conditions* table.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1500	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V _{DD}	Device supply voltage		1.7	1.8	1.9	V
V _O	Output Yx supply voltage, V _{DDOUT}	CDCE813-Q1	2.3		3.6	V
V _{IL}	Low-level input voltage, LVCMOS				0.3 × V _{DD}	V
V _{IH}	High-level input voltage, LVCMOS		0.7 × V _{DD}			V
V _{I(thresh)}	Input voltage threshold, LVCMOS			0.5 × V _{DD}		V
V _{I(S)}	Input voltage range, S0		0		1.9	V
	Input voltage range S1, S2, SDA, SCL (V _{I(thresh)} = 0.5 V _{DD})		0		3.6	
V _{I(CLK)}	Input voltage range CLK		0		1.9	V
I _{OH} , I _{OL}	Output current	V _{DDOUT} = 3.3 V			±12	mA
		V _{DDOUT} = 2.5 V			±10	
C _L	Output load, LVCMOS				15	pF
T _A	Operating ambient temperature		-40		105	°C

		MIN	NOM	MAX	UNIT
CRYSTAL AND VCXO SPECIFICATIONS ⁽¹⁾					
f_{Xtal}	Crystal input frequency range (fundamental mode)	8	27	32	MHz
ESR	Effective series resistance			100	Ω
f_{PR}	Pulling range ($0\text{ V} \leq V_{ctr} \leq 1.8\text{ V}$) ⁽²⁾	± 120	± 150		ppm
V_{ctr}	Frequency control voltage	0		V_{DD}	V
C_0 / C_1	Pullability ratio			220	
C_L	On-chip load capacitance at Xin and Xout	0		20	pF

(1) For more information about VCXO configuration, and crystal recommendation, see application report [VCXO Application Guideline for CDCE\(L\)9xx Family](#) (SCAA085).

(2) Pulling range depends on crystal type, on-chip crystal load capacitance, and PCB stray capacitance; pulling range of minimum ± 120 ppm applies for crystal listed in the application report [VCXO Application Guideline for CDCE\(L\)9xx Family](#) (SCAA085).

5.4 Thermal Information

THERMAL METRIC ^{(1) (2)}		CDCE813-Q1		UNIT
		PW (TSSOP)		
		14 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110.6		$^{\circ}\text{C}/\text{W}$
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	35.4		$^{\circ}\text{C}/\text{W}$
$R_{\theta JB}$	Junction-to-board thermal resistance	53.6		$^{\circ}\text{C}/\text{W}$
Ψ_{JT}	Junction-to-top characterization parameter	2.1		$^{\circ}\text{C}/\text{W}$
Ψ_{JB}	Junction-to-board characterization parameter	52.8		$^{\circ}\text{C}/\text{W}$
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—		$^{\circ}\text{C}/\text{W}$

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report (SPRA953).

(2) The package thermal impedance is calculated in accordance with JESD 51 and JEDEC2S2P (high-K board).

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
OVERALL PARAMETER							
I_{DD}	Supply current (see 5-1)	All outputs off, $f_{CLK} = 27\text{ MHz}$, $f_{VCO} = 135\text{ MHz}$, $f_{OUT} = 27\text{ MHz}$	All PLLS on		11		mA
			Per PLL		9		
$I_{DD(OUT)}$	Supply current (see 5-2)	No load, all outputs on, $f_{OUT} = 27\text{ MHz}$	$V_{DDOUT} = 3.3\text{ V}$		1.3		mA
$I_{DD(PD)}$	Power-down current. Every circuit powered down except I ² C	$f_{IN} = 0\text{ MHz}$, $V_{DD} = 1.9\text{ V}$			30		μA
$V_{(PUC)}$	Supply voltage V_{DD} threshold for power-up control circuit			0.85		1.45	V
f_{VCO}	VCO frequency range of PLL			70		230	MHz
f_{OUT}	LVC MOS output frequency	$V_{DDOUT} = 3.3\text{ V}$				230	MHz

over recommended operating free-air temperature range (unless otherwise noted)

		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
LVC MOS PARAMETER						
V _{IK}	LVC MOS input voltage	V _{DD} = 1.7 V, I _I = -18 mA			-1.2	V
I _I	LVC MOS input current	V _I = 0 V or V _{DD} , V _{DD} = 1.9 V			±5	μA
I _{IH}	LVC MOS input current for S0, S1, and S2	V _I = V _{DD} , V _{DD} = 1.9 V			5	μA
I _{IL}	LVC MOS input current for S0, S1, and S2	V _I = 0 V, V _{DD} = 1.9 V			-4	μA
C _I	Input capacitance at Xin/CLK	V _{IClk} = 0 V or V _{DD}		6		pF
	Input capacitance at Xout	V _{IXout} = 0 V or V _{DD}		2		
	Input capacitance at S0, S1, and S2	V _{IS} = 0 V or V _{DD}		3		
CDCE813-Q1, LVC MOS PARAMETER FOR V_{DDOUT} = 3.3-V MODE						
V _{OH}	LVC MOS high-level output voltage	V _{DDOUT} = 3 V, I _{OH} = -0.1 mA	2.9			V
		V _{DDOUT} = 3 V, I _{OH} = -8 mA	2.4			
		V _{DDOUT} = 3 V, I _{OH} = -12 mA	2.2			
V _{OL}	LVC MOS low-level output voltage	V _{DDOUT} = 3 V, I _{OL} = 0.1 mA			0.1	V
		V _{DDOUT} = 3 V, I _{OL} = 8 mA			0.5	
		V _{DDOUT} = 3 V, I _{OL} = 12 mA			0.8	
t _{PLH} , t _{PHL}	Propagation delay	PLL bypass		3.2		ns
		PLL enabled (f _{CLK} = f _{VCO}), 70 MHz ≤ f _{VCO} ≤ 85 MHz	1.6		4.3	
t _r , t _f	Rise and fall time	V _{DDOUT} = 3.3 V (20%–80%)		0.6		ns
t _{jit(cc)}	Cycle-to-cycle jitter ⁽²⁾	1 PLL switching, Y2-to-Y3, 10,000 cycles		50	200	ps
t _{jit(per)}	Peak-to-peak period jitter ⁽²⁾	1 PLL switching, Y2-to-Y3		60	200	ps
t _{sk(o)}	Output skew (see 表 7-2) ⁽³⁾	f _{OUT} = 50 MHz, Y1-to-Y3			440	ps
odc	Output duty cycle ⁽⁴⁾	f _{VCO} = 100 MHz, Pdiv = 1	45%		55%	
CDCE813-Q1, LVC MOS PARAMETER FOR V_{DDOUT} = 2.5-V MODE						
V _{OH}	LVC MOS high-level output voltage	V _{DDOUT} = 2.3 V, I _{OH} = -0.1 mA	2.2			V
		V _{DDOUT} = 2.3 V, I _{OH} = -6 mA	1.7			
		V _{DDOUT} = 2.3 V, I _{OH} = -10 mA	1.6			
V _{OL}	LVC MOS low-level output voltage	V _{DDOUT} = 2.3 V, I _{OL} = 0.1 mA			0.1	V
		V _{DDOUT} = 2.3 V, I _{OL} = 6 mA			0.5	
		V _{DDOUT} = 2.3 V, I _{OL} = 10 mA			0.7	
t _{PLH} , t _{PHL}	Propagation delay	PLL bypass		3.6		ns
t _r , t _f	Rise and fall time	V _{DDOUT} = 2.5 V (20%–80%)		0.8		ns
t _{jit(cc)}	Cycle-to-cycle jitter ⁽²⁾	1 PLL switching, Y2-to-Y3, 10,000 cycles		50	200	ps
t _{jit(per)}	Peak-to-peak period jitter ⁽²⁾	1 PLL switching, Y2-to-Y3		60	200	ps
t _{sk(o)}	Output skew (see 表 7-2) ⁽³⁾	f _{OUT} = 50 MHz, Y1-to-Y3			440	ps
odc	Output duty cycle ⁽⁴⁾	f _{VCO} = 100 MHz, Pdiv = 1	45%		55%	

over recommended operating free-air temperature range (unless otherwise noted)

		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
I²C PARAMETER						
V _{IK}	SCL and SDA input clamp voltage	V _{DD} = 1.7 V, I _I = -18 mA			-1.2	V
I _{IH}	SCL and SDA input current	V _I = V _{DD} , V _{DD} = 1.9 V			±10	μA
V _{IH}	I ² C input high voltage ⁽⁵⁾		0.7 × V _{DD}			V
V _{IL}	I ² C input low voltage ⁽⁵⁾				0.3 × V _{DD}	V
V _{OL}	SDA low-level output voltage	I _{OL} = 3 mA, V _{DD} = 1.7 V			0.2 × V _{DD}	V
C _I	SCL-SDA input capacitance	V _I = 0 V or V _{DD}		3	10	pF
EEPROM SPECIFICATION						
EEcyc	Programming cycles of EEPROM		100	1000		cycles
EEret	Data retention		10			years

(1) All typical values are at respective nominal V_{DD}.

(2) Jitter depends on configuration. Jitter data is for input frequency = 27 MHz, f_{VCO} = 108 MHz, f_{OUT} = 27 MHz (measured at Y2).

(3) The tsk(o) specification is only valid for equal loading of each bank of outputs, and the outputs are generated from the same divider.

(4) odc depends on the output rise and fall time (t_r and t_f); data sampled on the rising edge (t_r)

(5) SDA and SCL pins are 3.3-V tolerant.

5.6 Timing Requirements

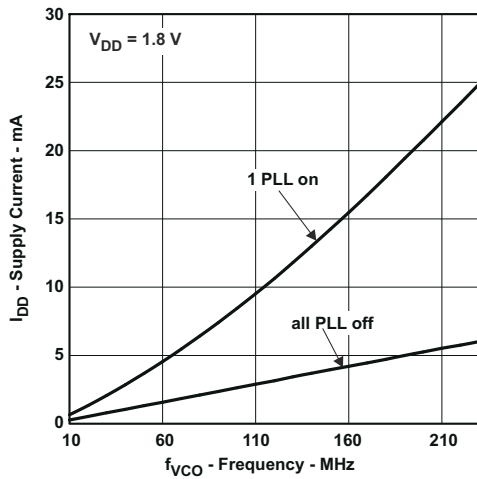
over recommended ranges of supply voltage, load, and operating free-air temperature

		MIN	NOM	MAX	UNIT
CLK_IN					
f _{CLK}	LVCMOS clock input frequency	PLL bypass mode	0	160	MHz
		PLL mode	8	160	
t _r and t _f	Rise and fall time, CLK signal (20% to 80%)			3	ns
	Duty cycle of CLK at V _{DD} / 2	40%		60%	
I²C (SEE 7-9)					
f _{SCL}	SCL clock frequency	Standard mode	0	100	kHz
		Fast mode	0	400	
t _{su} (START)	START setup time (SCL high before SDA low)	Standard mode	4.7		μs
		Fast mode	0.6		
t _h (START)	START hold time (SCL low after SDA low)	Standard mode	4		μs
		Fast mode	0.6		
t _w (SCLL)	SCL low-pulse duration	Standard mode	4.7		μs
		Fast mode	1.3		
t _w (SCLH)	SCL high-pulse duration	Standard mode	4		μs
		Fast mode	0.6		
t _h (SDA)	SDA hold time (SDA valid after SCL low)	Standard mode	0	3.45	μs
		Fast mode	0	0.9	
t _{su} (SDA)	SDA setup time	Standard mode	250		ns
		Fast mode	100		
t _r	SCL-SDA input rise time	Standard mode		1000	ns
		Fast mode		300	
t _f	SCL-SDA input fall time			300	ns
t _{su} (STOP)	STOP setup time	Standard mode	4		μs
		Fast mode	0.6		

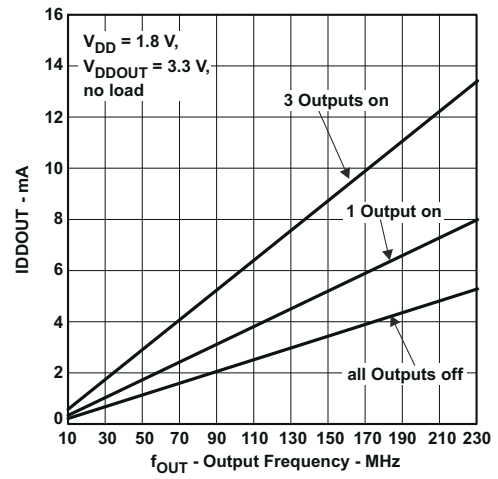
over recommended ranges of supply voltage, load, and operating free-air temperature

		MIN	NOM	MAX	UNIT
t _{BUS}	Bus free time between a STOP and START condition	Standard mode	4.7		μs
		Fast mode	1.3		

5.7 Typical Characteristics

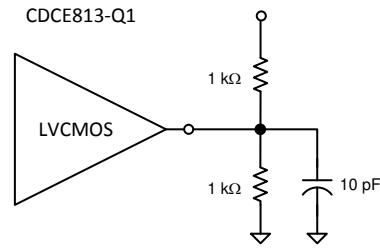


5-1. CDCE813-Q1 Supply Current vs PLL Frequency



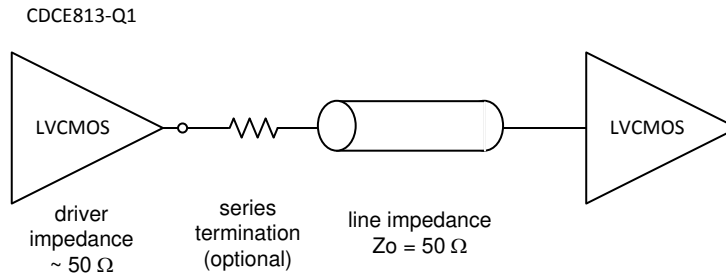
5-2. CDCE813-Q1 Output Current vs Output Frequency

6 Parameter Measurement Information



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6-1. Test Load



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6-2. Test Load for 50-Ω Board Environment

7 Detailed Description

7.1 Overview

The CDCExxx-Q1 devices are modular PLL-based, low-cost, high-performance, programmable clock synthesizers, multipliers, and dividers. They generate up to three output clocks from a single input frequency. Each output can be programmed in-system for any clock frequency up to 230 MHz, using the integrated configurable PLL.

The CDCExxx-Q1 devices have separate output supply pins, V_{DDOUT} , with output of 2.5 V to 3.3 V.

The input accepts an external crystal or LVCMOS clock signal. If an external crystal is used, an on-chip load capacitor is adequate for most applications. The value of the load capacitor is programmable from 0 pF to 20 pF. Additionally, a selectable on-chip VCXO allows synchronization of the output frequency to an external control signal, that is, the PWM signal.

The deep M / N divider ratio allows the generation of zero-ppm audio-video, networking (WLAN, Bluetooth, Ethernet, GPS) or interface (USB, IEEE1394, memory stick) clocks from, for example, a 27-MHz reference input frequency.

The PLL supports spread-spectrum clocking (SSC). SSC can be center-spread or down-spread clocking, which is a common technique to reduce electromagnetic interference (EMI).

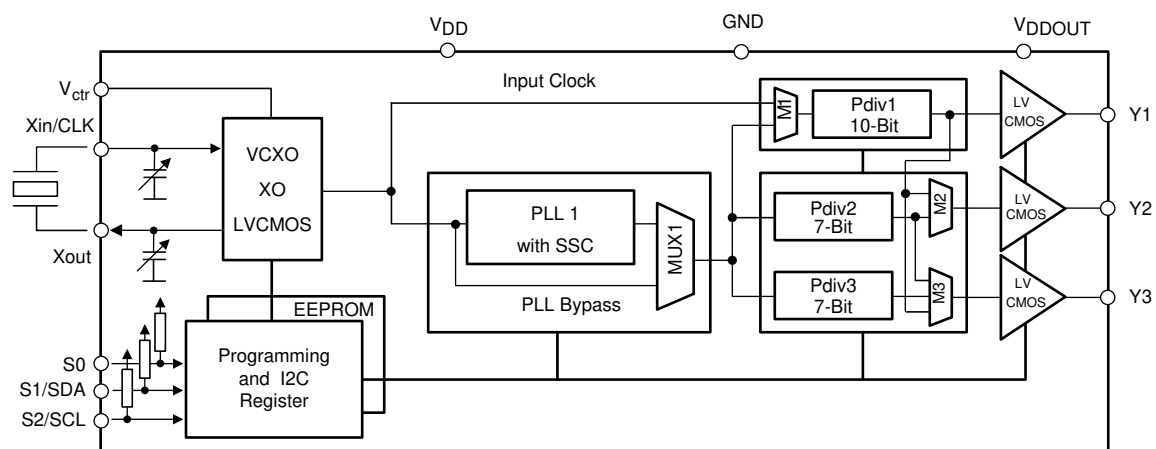
Based on the PLL frequency and the divider settings, the internal loop filter components are automatically adjusted to achieve high stability and optimized jitter transfer characteristics.

The device supports nonvolatile EEPROM programming for easy customization of the device to the application. The device is preset to a factory default configuration (see [Default Device Configuration](#)) that can be reprogrammed to a different application configuration before PCB assembly, or reprogrammed by in-system programming. All device settings are programmable through the SDA-SCL bus, a 2-wire serial interface.

Three programmable control inputs, S0, S1, and S2, can be used to select different frequencies, change SSC setting for lowering EMI, or control other features like outputs disable to low, outputs in Hi-Z state, power down, PLL bypass, and so forth). For CDCE813-Q1, the S0 pin is unused by default. For the CDCE813R02-Q1, the S0 control input pin provides output enable (OE) control for output Y1 only.

The CDCE813-Q1 core operates in a 1.8-V environment. It operates in a temperature range of -40°C to 105°C .

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Control Terminal Configuration

The CDCE813-Q1 device has three user-definable control terminals (S0, S1, and S2), which allow external control of device settings. They can be programmed to any of the following functions:

- Spread-spectrum clocking selection → spread type and spread amount selection
- Frequency selection → switching between any of two user-defined frequencies
- Output state selection → output configuration and power-down control

The user can predefine up to eight different control settings. 表 7-1 and 表 7-2 explain these settings.

表 7-1. Control Terminal Definition

EXTERNAL CONTROL BITS	PLL1 SETTING			Y1 SETTING
Control function	PLL frequency selection	SSC selection	Output Y2 and Y3 selection	Output Y1 and power-down selection

表 7-2. PLL1 Setting (1)

SSCx [3 BITS]			CENTER	DOWN
SSC SELECTION (CENTER AND DOWN)				
0	0	0	0% (off)	0% (off)
0	0	1	±0.25%	-0.25%
0	1	0	±0.5%	-0.5%
0	1	1	±0.75%	-0.75%
1	0	0	±1.0%	-1.0%
1	0	1	±1.25%	-1.25%
1	1	0	±1.5%	-1.5%
1	1	1	±2.0%	-2.0%

- (1) Center and down-spread, Frequency0, Frequency1, State0, and State1 are user-definable in PLL1 configuration register.

表 7-3. PLL1 Setting, Frequency Selection (1)

FSx	FUNCTION
0	Frequency 0
1	Frequency 1

- (1) Frequency0 and Frequency1 can be any frequency within the specified f_{VCO} range.

表 7-4. PLL1 Setting, Output Selection (Y2, Y3) (1)

Y2, Y3	FUNCTION
0	State 0
1	State 1

- (1) State0 or State1 selection is valid for both outputs of the corresponding PLL module and can be power down, Hi-Z state, low, or active.

表 7-5. Y1 Setting (1)

Y1	FUNCTION
0	State 0
1	State 1

- (1) State0 and State1 are user definable in the generic configuration register and can be power down, Hi-Z state, low, or active.

The S1/SDA and S2/SCL pins of the CDCE813-Q1 device are dual-function pins. In the default configuration, they are defined as SDA and SCL for the serial programming interface. They can be programmed as control pins (S1 and S2) by setting the appropriate bits in the EEPROM.

注

Changes to the control register (Bit [6] of byte 02h) have no effect until they are written into the EEPROM.

After the S1/SDA and S2/SCL pins are set as control pins, the serial programming interface is no longer available. However, if V_{DDOUT} is forced to GND, the two control pins, S1 and S2, temporarily act as serial programming pins (SDA and SCL).

S0 is *not* a multi-use pin. S0 is a control pin only.

7.3.2 Default Device Configuration

The internal EEPROM of the CDCE813-Q1 device is pre-configured with a factory default configuration as shown in 図 7-1 (the input frequency is routed through PLL1 to the outputs as a default). This mode can be used to clean the jitter of an incoming clock signal. For the CDCE813-Q1, the outputs are disabled by default and must be turned on through I²C. For the CDCE813R02-Q1, output Y1 is enabled through the S0 control pin (active high), while outputs Y2 and Y3 are either in a tri-state condition or disabled by the register default. Y1 is enabled when S0 is floating because S0 has an internal pullup.

The default setting appears either after power is supplied or after a power-down – power-up sequence until it is reprogrammed by the user to a different application configuration. A new register setting is programmed through the serial I²C interface.

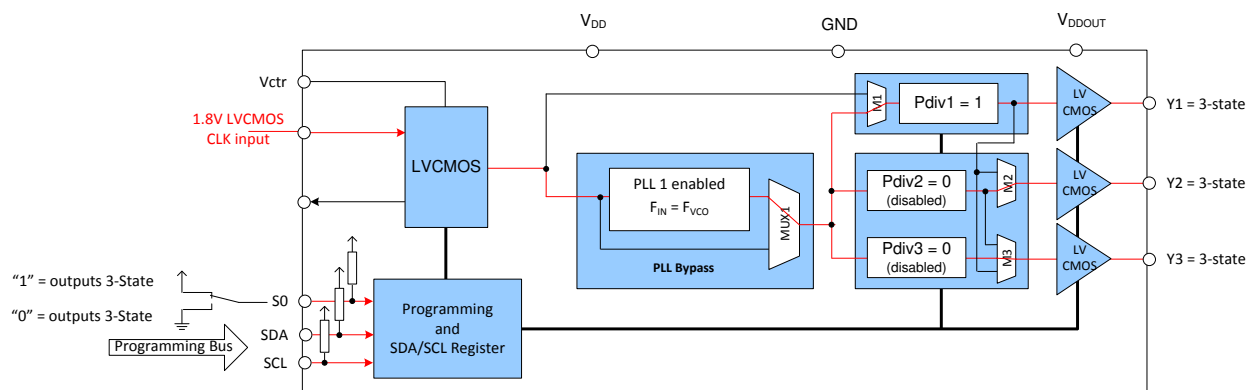


図 7-1. CDCE813-Q1 Default Configuration

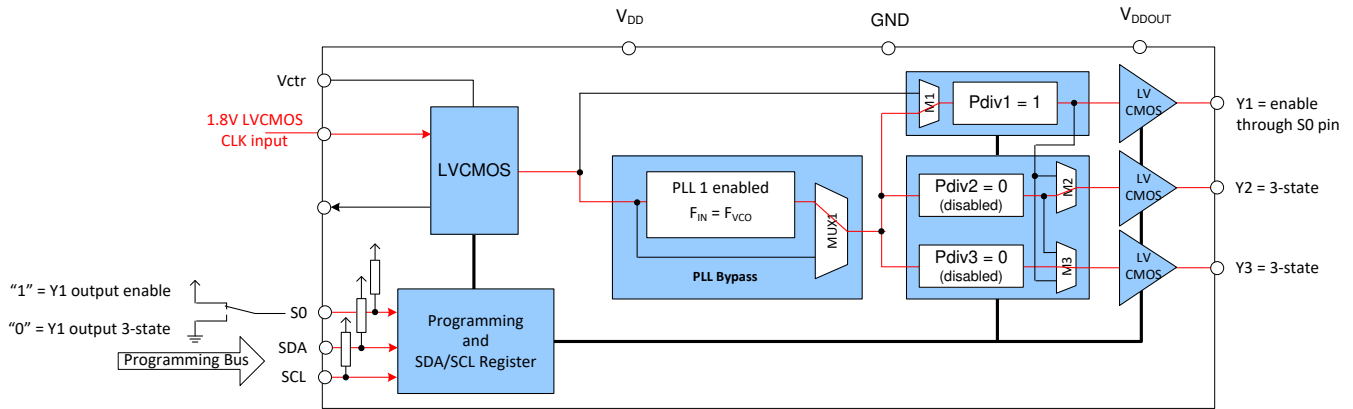


図 7-2. CDCE813R02-Q1 Default Configuration

表 7-6 shows the factory default setting for the Control Terminal Register.

注

Even though eight different register settings are possible, in the default configuration, only the first two settings (0 and 1) can be selected with S0, as S1 and S2 are configured as programming pins in default mode.

表 7-6. Factory Default Setting for Control Terminal Register (1)

GPN	EXTERNAL CONTROL PINS			Y1	PLL1 SETTINGS		
				OUTPUT SELECTION	FREQUENCY SELECTION	SSC SELECTION	OUTPUT SELECTION
	S2	S1	S0	Y1	FS1	SSC1	Y2Y3
CDCE813-Q1	SCL (I ² C)	SDA (I ² C)	0	3-state	f _{VCO1_0}	Off	3-state
	SCL (I ² C)	SDA (I ² C)	1	3-state	f _{VCO1_0}	Off	3-state
CDCE813R02-Q1	SCL (I ² C)	SDA (I ² C)	0	3-state	f _{VCO1_0}	Off	3-state
	SCL (I ² C)	SDA (I ² C)	1	Enabled	f _{VCO1_0}	Off	3-state

(1) In default mode or when programmed respectively, S1 and S2 act as serial programming interface, I²C. They do not have any control-pin function but they are internally interpreted as if S1 = 0 and S2 = 0. For the CDCE813-Q1, S0 is an unused control pin by default. For the CDCE813R02-Q1, S0 provides output enable (OE) control output Y1 only.

7.3.3 I²C Serial Interface

The CDCE813-Q1 device operates as a target device on the 2-wire serial I²C bus compatible with the popular SMBus or I²C specification. The device operates in the standard-mode transfer (up to 100 kbps) and fast-mode transfer (up to 400 kbps) and supports 7-bit addressing.

The S1/SDA and S2/SCL pins of the CDCE813-Q1 device are dual-function pins. In the default configuration, the pins are used as the I²C serial programming interface. The pins can be reprogrammed as general-purpose control pins, S1 and S2, by changing the corresponding EEPROM setting, byte 02h, bit [6].

7.3.4 Data Protocol

The device supports *Byte Write and Byte Read* and *Block Write and Block Read* operations.

For *Byte Write/Read* operations, the system controller can individually access addressed bytes.

For *Block Write/Read* operations, the bytes are accessed in sequential order from lowest to highest byte (with most-significant bit first) with the ability to stop after any complete byte has been transferred. The numbers of bytes read out are defined by Byte Count in the generic configuration register. At the *Block Read* instruction, all bytes defined in Byte Count must be read out to finish the read cycle correctly.

After a byte has been sent, the byte is written into the internal register and is effective immediately. This applies to each transferred byte, regardless of whether this is a *Byte Write* or a *Block Write* sequence.

If the EEPROM write cycle is initiated, the internal registers are written into the EEPROM. Data can be read out during the programming sequence (*Byte Read* or *Block Read*). The programming status can be monitored by *EEPIP*, byte 01h–bit 6. Before beginning EEPROM programming, pull CLKIN LOW. CLKIN must be held LOW for the duration of EEPROM programming. After initiating EEPROM programming with *EEWRITE*, byte 06h-bit 0, do not write to the device registers until *EEPIP* is read back as a 0.

The offset of the indexed byte is encoded in the command code, as described in 表 7-8.

表 7-7. Target Receiver Address (7 Bits)

DEVICE	A6	A5	A4	A3	A2	A1 ⁽¹⁾	A0 ⁽¹⁾	R/ W
CDCE813-Q1	1	1	0	0	1	0	1	1/0
CDCEx925	1	1	0	0	1	0	0	1/0
CDCEx937	1	1	0	1	1	0	1	1/0
CDCEx949	1	1	0	1	1	0	0	1/0

(1) Address bits A0 and A1 are programmable through the I²C bus (byte 01, bits [1:0]). This allows addressing up to 4 devices connected to the same I²C bus. The least-significant bit of the address byte designates a write or read operation.

7.4 Device Functional Modes

7.4.1 SDA and SCL Hardware Interface

图 7-3 shows how the CDCE813-Q1 clock synthesizer is connected to the I²C serial interface bus. Multiple devices can be connected to the bus, but it may be necessary to reduce the speed (400 kHz is the maximum) if many devices are connected.

Note that the pullup resistors (R_P) depend on the supply voltage, bus capacitance, and number of connected devices. The recommended pullup value is 4.7 k Ω . The resistor must meet the minimum sink current of 3 mA at $V_{OLmax} = 0.4$ V for the output stages (for more details see the SMBus or I²C Bus specifications in the [Timing Requirements](#) table).

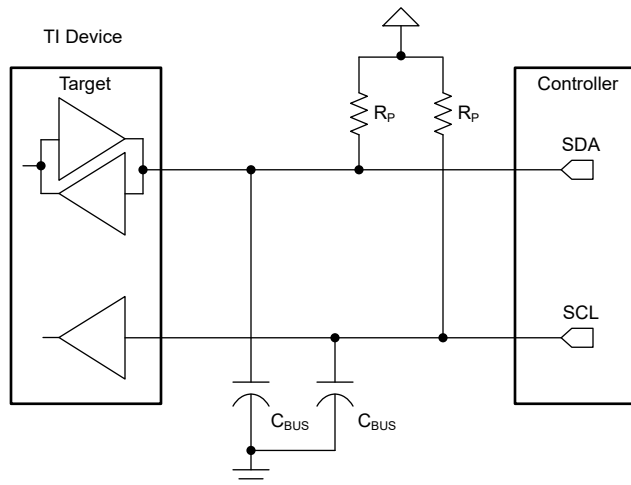


图 7-3. I²C Hardware Interface

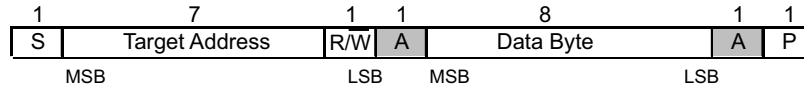
7.5 Programming

表 7-8. Command Code Definition

BIT	DESCRIPTION
7	0 = <i>Block Read</i> or <i>Block Write</i> operation 1 = <i>Byte Read</i> or <i>Byte Write</i> operation

表 7-8. Command Code Definition (続き)

BIT	DESCRIPTION
(6:0)	Byte offset for <i>Byte Read</i> , <i>Block Read</i> , <i>Byte Write</i> , and <i>Block Write</i> operations



- S** Start Condition
- Sr** Repeated Start Condition
- R/W** 1 = Read (Rd) From CDCE9xx Device; 0 = Write (Wr) to CDCE9xxx
- A** Acknowledge (ACK = 0 and NACK =1)
- P** Stop Condition
- Controller-to-Target Transmission
- Target-to-Controller Transmission

図 7-4. Generic Programming Sequence

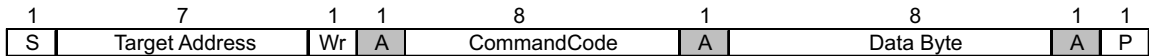


図 7-5. Byte Write Protocol

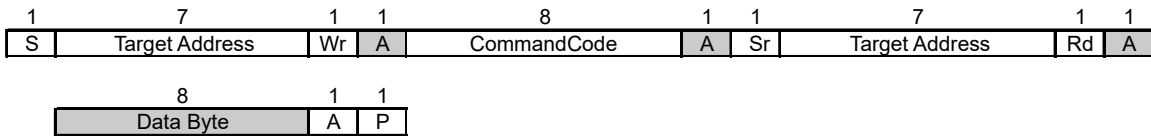
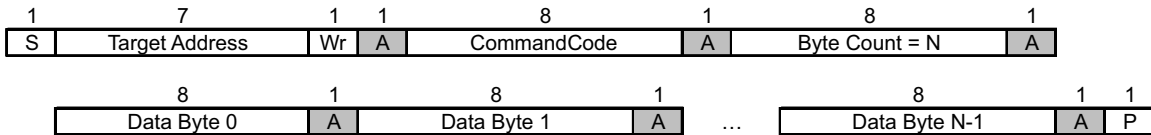


図 7-6. Byte Read Protocol



A. Data byte 0 bits [7:0] is reserved for Revision Code and Vendor Identification. Also, it is used for internal test purpose and should not be overwritten.

図 7-7. Block Write Protocol

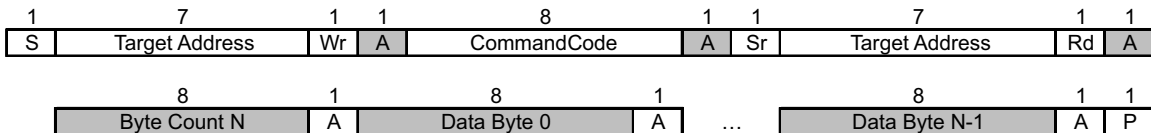


図 7-8. Block Read Protocol

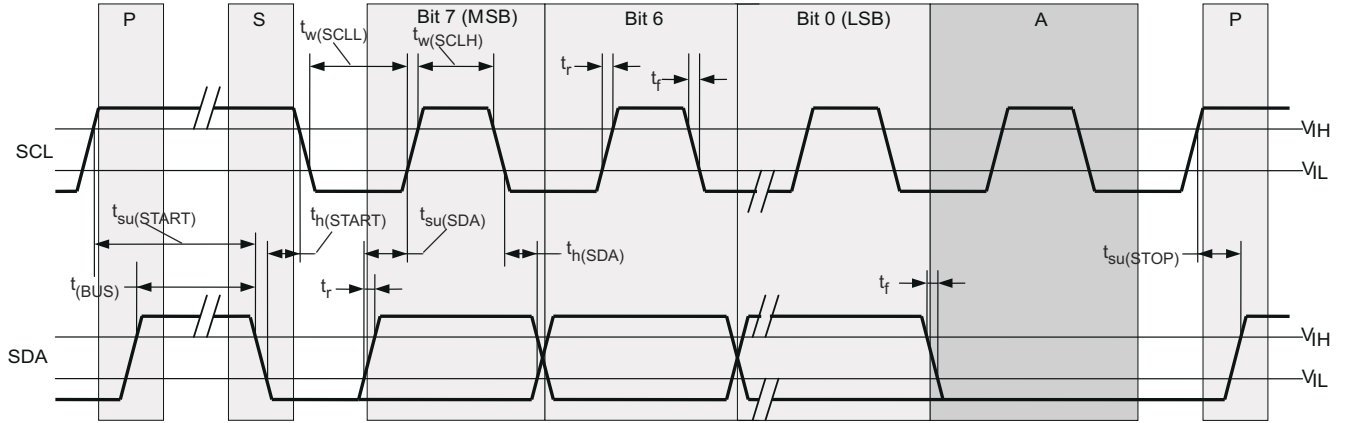


图 7-9. Timing Diagram for I²C Serial Control Interface

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The CDCE813-Q1 device is an easy-to-use, high-performance, programmable CMOS clock synthesizer which can be used as a crystal buffer, clock synthesizer with separate output supply pin. The CDCE813-Q1 device features an on-chip loop filter and spread-spectrum modulation. Programming can be done through the I²C interface, or previously saved settings can be loaded from on-chip EEPROM. The pins S0, S1, and S2 can be programmed as control pins to select various output settings. This section shows some examples of the CDCE813-Q1 in various applications.

8.2 Typical Application

図 8-1 shows the application example of CDCE813-Q1 in combination with an SoC processor and an FPD-Link3 serializer, serving as a PCLK jitter cleaner.

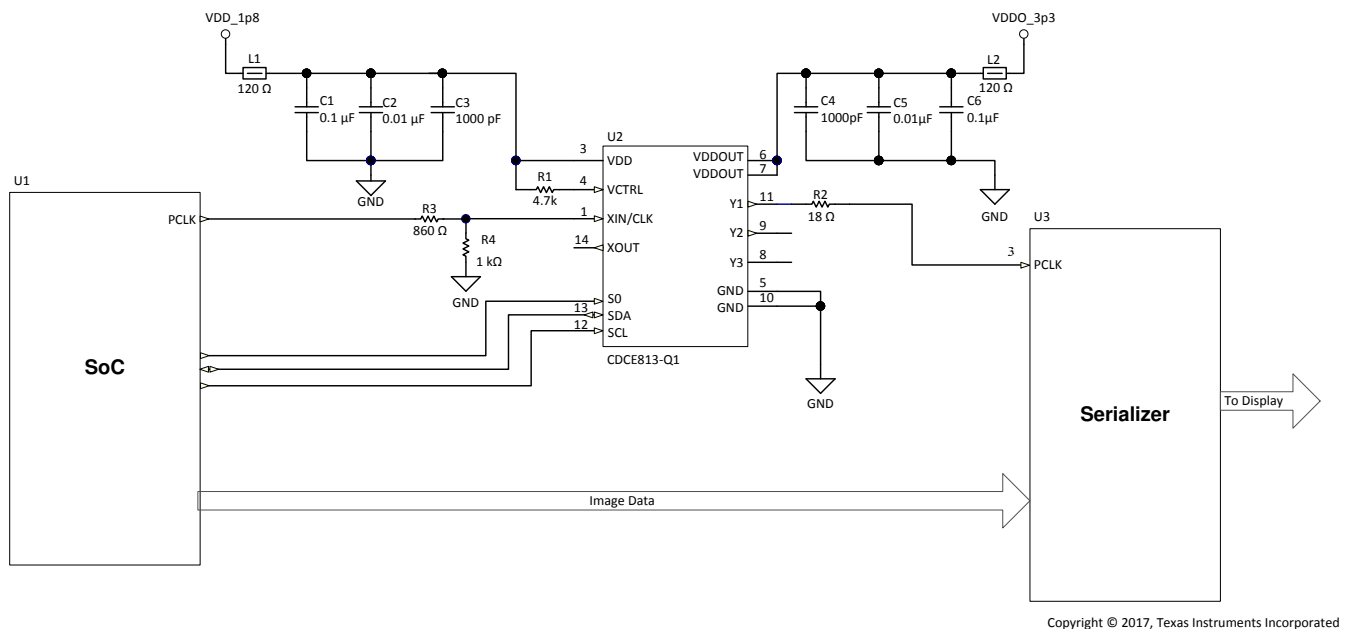


図 8-1. PCLK Jitter Cleaner Reference Design

8.2.1 Design Requirements

The CDCE813-Q1 device supports spread-spectrum clocking (SSC) with multiple control parameters:

- Modulation amount (%)
- Modulation frequency (>20 kHz)
- Center spread or down spread (\pm or $-$)

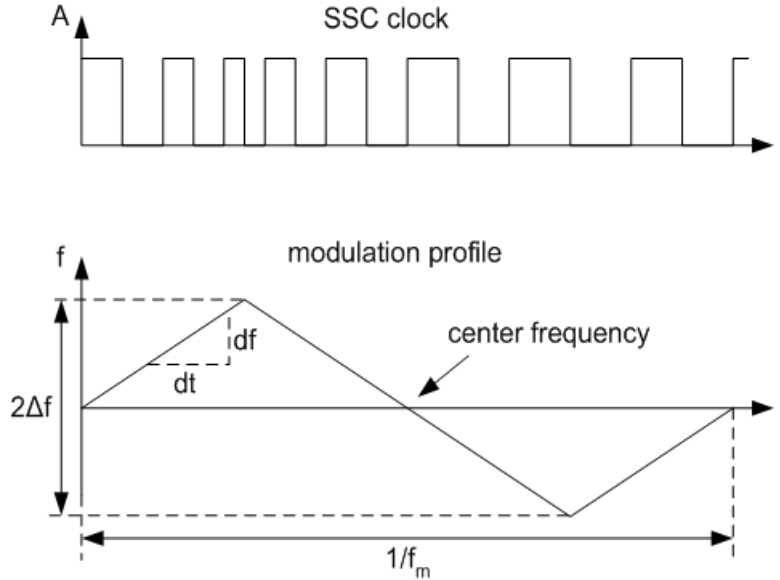
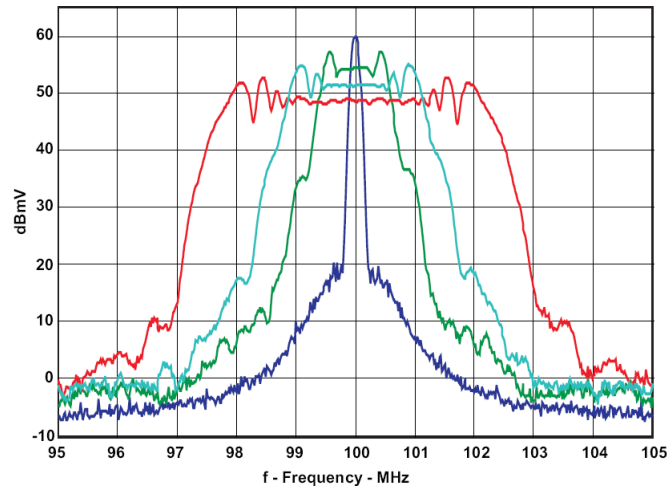


図 8-2. Modulation Frequency (f_m) and Modulation Amount

8.2.2 Detailed Design Procedure

8.2.2.1 Spread-Spectrum Clock (SSC)

Spread-spectrum modulation is a method to spread emitted energy over a larger bandwidth. In clocking, spread spectrum can reduce electromagnetic interference (EMI) by reducing the level of emission from clock distribution network.



CDCS502 with a 25-MHz Crystal, FS = 1, f_{OUT} = 100 MHz, and 0%, ± 0.5 , $\pm 1\%$, and $\pm 2\%$ SSC

図 8-3. Comparison Between Typical Clock Power Spectrum and Spread-Spectrum Clock

Spread spectrum clocking can be used to help reduce EMI to meet design specifications. For example, a specified EMI threshold of 55 dB/mV would require $\pm 1\%$ spread-spectrum clocking to meet this requirement.

8.2.2.2 PLL Frequency Planning

At a given input frequency (f_{IN}), use 式 1 to calculate the output frequency (f_{OUT}) of the CDCE813-Q1 device.

$$f_{OUT} = \frac{f_{IN}}{P_{div}} \times \frac{N}{M} \quad (1)$$

- M (1 to 511) and N (1 to 4095) are the multiplier or divider values of the PLL
- Pdiv (1 to 127) is the output divider

Use 式 2 to calculate the target VCO frequency (f_{VCO}) of each PLL.

$$f_{VCO} = f_{IN} \times \frac{N}{M} \quad (2)$$

The PLL internally operates as fractional divider and requires the following multiplier or divider settings:

- N
- $P = 4 - \text{int}(\log_2 N / M)$; if $P < 0$ then $P = 0$
- $Q = \text{int}(N' / M)$
- $R = N' - M \times Q$

where

- $\text{int}(X)$ = integer portion of X
- $N' = N \times 2^P$
- $N \geq M$

$$80 \text{ MHz} \leq f_{VCO} \leq 230 \text{ MHz}$$

$$16 \leq Q \leq 63$$

$$0 \leq P \leq 4$$

$$0 \leq R \leq 51$$

Example:

for $f_{IN} = 27 \text{ MHz}$; $M = 1$; $N = 4$; $P_{div} = 2$

- $f_{OUT} = 54 \text{ MHz}$
- $f_{VCO} = 108 \text{ MHz}$
- $P = 4 - \text{int}(\log_2 4) = 4 - 2 = 2$
- $N' = 4 \times 2^2 = 16$
- $Q = \text{int}(16) = 16$
- $R = 16 - 16 = 0$

for $f_{IN} = 27 \text{ MHz}$; $M = 2$; $N = 11$; $P_{div} = 2$

- $f_{OUT} = 74.25 \text{ MHz}$
- $f_{VCO} = 148.50 \text{ MHz}$
- $P = 4 - \text{int}(\log_2 5.5) = 4 - 2 = 2$
- $N' = 11 \times 2^2 = 44$
- $Q = \text{int}(22) = 22$
- $R = 44 - 44 = 0$

The values for P, Q, R, and N' are automatically calculated when using TI Pro-Clock™ software.

8.2.2.3 Crystal Oscillator Start-Up


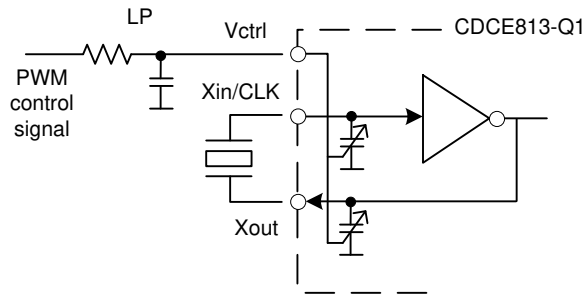
When the CDCE813-Q1 device can be used as a crystal buffer, the crystal oscillator start-up dominates the start-up time compared to the internal PLL lock time.  8-4 shows the oscillator start-up sequence for a 27-MHz crystal input with an 8-pF load. The start-up time for the crystal is on the order of approximately 250 μs compared to approximately 10 μs of lock time. In general, lock time is an order of magnitude less compared to the crystal start-up time.



図 8-4. Crystal Oscillator Start-Up vs PLL Lock Time

8.2.2.4 Frequency Adjustment With Crystal Oscillator Pulling

The frequency for the CDCE813-Q1 device is adjusted for media and other applications with the VCXO control input V_{ctr} . If a PWM-modulated signal is used as a control signal for the VCXO, an external filter is needed.



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図 8-5. Frequency Adjustment Using PWM Input to the VCXO Control

8.2.2.5 Unused Inputs and Outputs

If VCXO-pulling functionality is not required, V_{ctr} should be left floating. All other unused inputs should be set to GND. Unused outputs should be left floating.

If one output block is not used, TI recommends disabling it. However, TI recommends providing a supply for all output blocks, even if they are disabled.

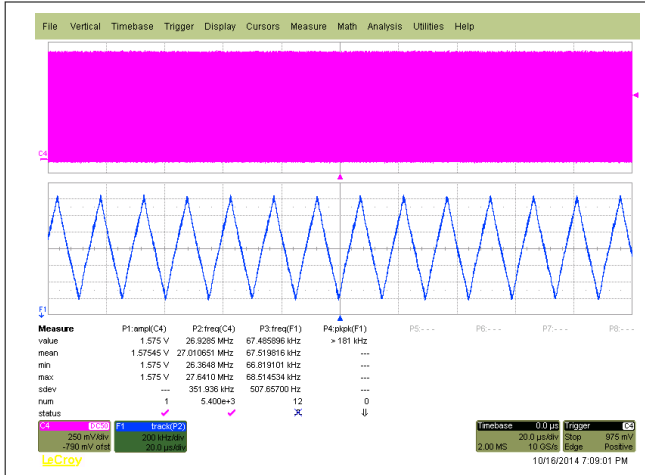
8.2.2.6 Switching Between XO and VCXO Mode

When the CDCE813-Q1 device is in the crystal-oscillator or VCXO configuration, the internal capacitors require different internal capacitance. The following steps are recommended to switch to VCXO mode when the configuration for the on-chip capacitor is still set for XO mode. To center the output frequency to 0 ppm:

1. While in XO mode, put $V_{ctr} = V_{DD} / 2$
2. Switch from XO mode to VCXO mode
3. Program the internal capacitors to obtain 0 ppm at the output.

8.2.3 Application Curves

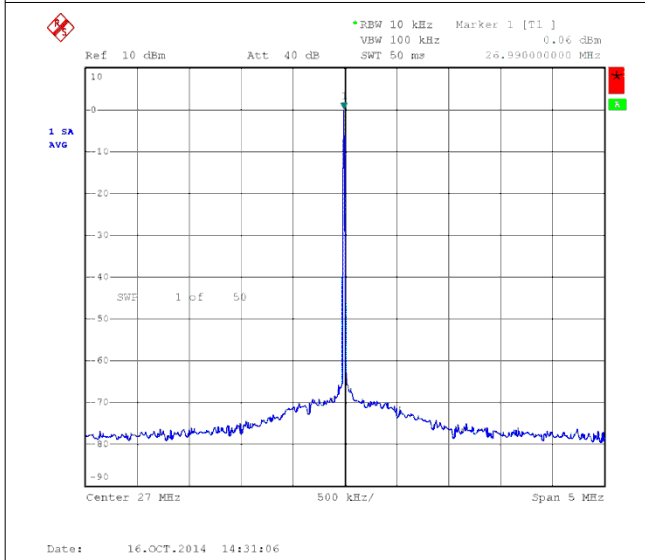
図 8-6, 図 8-7, 図 8-8, and 図 8-9 show CDCE813-Q1 measurements with the SSC feature enabled. Device configuration: 27-MHz input, 27-MHz output.



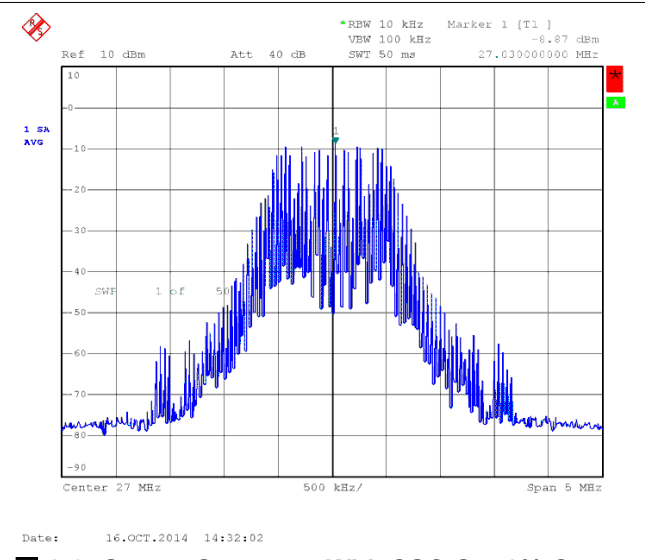
8-6. $f_{OUT} = 27$ MHz, VCO frequency < 125 MHz, SSC (2% Center)



8-7. $f_{OUT} = 27$ MHz, VCO frequency > 175 MHz, SSC (1%, Center)



8-8. Output Spectrum With SSC Off



8-9. Output Spectrum With SSC On, 2% Center

8.3 Power Supply Recommendations

There is no restriction on the power-up sequence. In case V_{DDOUT} is applied first, TI recommends grounding the V_{DD} . In case V_{DDOUT} is powered while V_{DD} is floating, there is a risk of high current flowing on the V_{DDOUT} pins.

The device has a power-up control that is connected to the 1.8-V supply. This keeps the whole device disabled until the 1.8-V supply reaches a sufficient voltage level. Then the device switches on all internal components, including the outputs. If a 3.3-V V_{DDOUT} is available before the 1.8-V, the outputs stay disabled until the 1.8-V supply has reached a certain level.

8.4 Layout

8.4.1 Layout Guidelines

When the CDCE813-Q1 device is used as a crystal buffer, any parasitic across the crystal affect the pulling range of the VCXO. Therefore, take care in placing the crystal units on the board. Crystals must be placed as close to the device as possible, ensuring that the routing lines from the crystal terminals to Xin and Xout have the same length.

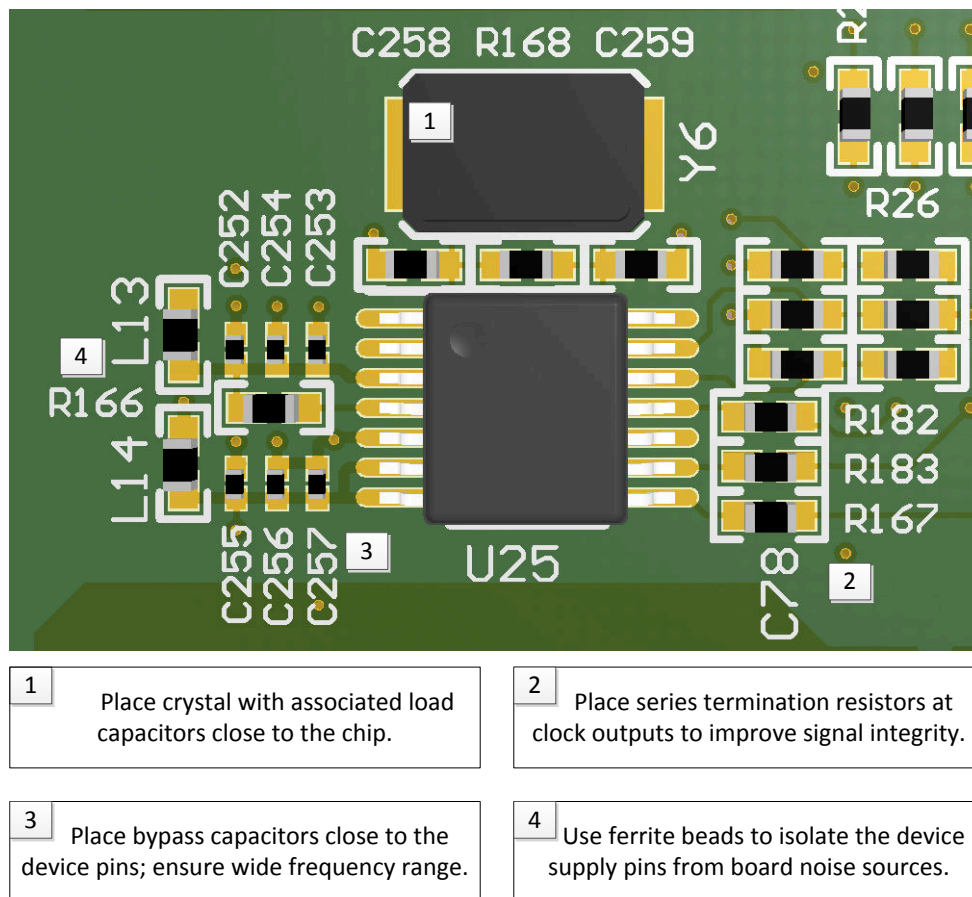
If possible, cut out both ground plane and power plane under the area where the crystal and the routing to the device are placed. In this area, always avoid routing any other signal line, as it could be a source of noise coupling.

Additional discrete capacitors can be required to meet the load capacitance specification of certain crystals. For example, a 10.7-pF load capacitor is not fully programmable on the chip, because the internal capacitor can range from 0 pF to 20 pF with steps of 1 pF. The 0.7-pF capacitor therefore can be discretely added on top of an internal 10-pF capacitor.

To minimize the inductive influence of the trace, TI recommends placing this small capacitor as close to the device as possible and symmetrically with respect to Xin and Xout.

☒ 8-10 shows a conceptual layout detailing recommended placement of power-supply bypass capacitors. For component-side mounting, use 0402 body-size capacitors to facilitate signal routing. Keep the connections between the bypass capacitors and the power supply on the device as short as possible. Ground the other side of the capacitor using a low-impedance connection to the ground plane.

8.4.2 Layout Example



☒ 8-10. Annotated Layout

表 9-3. Generic Configuration Register (続き)

OFFSET ⁽¹⁾	BIT ⁽²⁾	ACRONYM	DEFAULT ⁽³⁾	DESCRIPTION	
02h	7	M1	1b	Clock source selection for output Y1:	0 – Input clock 1 – PLL1 clock
	6	SPICON	0b	Operation mode selection for pins 12 and 13 ⁽⁶⁾ 0 – Serial programming interface SDA (pin 13) and SCL (pin 12) 1 – Control pins S1 (pin 13) and S2 (pin 12)	
	5:4	Y1_ST1	CDCE813-Q1: 01b CDCE813R02-Q1: 11b	Y1-State0/1 definition	
	3:2	Y1_ST0	01b	00 – Device power down (all PLLs in power down and all outputs in Hi-Z state) 01 – Y1 disabled to Hi-Z state	10 – Y1 disabled to low 11 – Y1 enabled
	1:0	Pdiv1 [9:8]	001h	10-bit Y1-output-divider Pdiv1:	
03h	7:0	Pdiv1 [7:0]		0 – Divider reset and stand-by 1 to 1023 – Divider value	
04h	7	Y1_7	0b	Y1_x State selection ⁽⁷⁾ 0 – State0 (predefined by Y1_ST0) 1 – State1 (predefined by Y1_ST1)	
	6	Y1_6	0b		
	5	Y1_5	0b		
	4	Y1_4	0b		
	3	Y1_3	0b		
	2	Y1_2	0b		
	1	Y1_1	CDCE813-Q1: 0b CDCE813R02-Q1: 1b		
05h	7:3	XCSEL	00h	Crystal load capacitor selection ⁽⁸⁾	00h – 0 pF 01h – 1 pF 02h – 2 pF :14h to 1Fh – 20 pF
	2:0		0b	Reserved – do not write other than 0	
06h	7:1	BCOUNT	00h	7-bit byte count (defines the number of bytes which will be sent from this device at the next <i>Block Read</i> transfer); all bytes must be read out to finish the read cycle correctly.	
	0	EEWRITE	0b	Initiate EEPROM write cycle ⁽⁴⁾ ⁽⁹⁾ 0 – No EEPROM write cycle 1 – Start EEPROM write cycle (internal registers are saved to the EEPROM)	
07h-0Fh		—	0h	Unused address range	

- (1) Writing data beyond 20h may affect device function.
- (2) All data transferred with the MSB first
- (3) Unless customer-specific setting
- (4) During EEPROM programming, no data is allowed to be sent to the device through the I²C bus until the programming sequence is completed. Data, however, can be read out during the programming sequence (*Byte Read* or *Block Read*).
- (5) If this bit is set to high in the EEPROM, the actual data in the EEPROM is permanently locked. No further programming is possible. Data, however can still be written through the I²C bus to the internal register to change device function on the fly, but new data can no longer be saved to the EEPROM. EELOCK is effective only if written into the EEPROM.
- (6) Selection of *control pins* is effective only if written into the EEPROM. After the pins are written into the EEPROM, the serial programming pins are no longer available. However, if V_{DDOUT} is forced to GND, the two control pins, S1 and S2, temporarily act as serial programming pins (SDA-SCL), and the two target receiver address bits are reset to A0 = 0 and A1 = 0.
- (7) These are the bits of the control terminal register (see 表 9-2). The user can predefine up to eight different control settings. These settings then can be selected by the external control pins, S0, S1, and S2.
- (8) The internal load capacitor (C₁, C₂) must be used to achieve the best clock performance. External capacitors should be used only to finely adjust C_L by a few picofarads. The value of C_L can be programmed with a resolution of 1 pF for a crystal load range of 0 pF to 20 pF. For C_L > 20 pF, use additional external capacitors. The device input capacitance value must be considered, which always adds 1.5 pF (6 pF//2 pF) to the selected C_L. For more about VCXO configuring and crystal recommendation, see application report [VCXO Application Guideline for CDCE\(L\)9xx Family](#) (SCAA085).
- (9) The EEPROM WRITE bit must be sent last. This ensures that the content of all internal registers are stored in the EEPROM. The EEWRITE cycle is initiated with the rising edge of the EEWRITE bit. A static level-high does not trigger an EEPROM WRITE cycle. The EEWRITE bit must be reset to low after the programming is completed. The programming status can be monitored by reading out EEPIP. If EELOCK is set to high, no EEPROM programming is possible.

表 9-4. PLL1 Configuration Register

OFFSET ⁽¹⁾	BIT ⁽²⁾	ACRONYM	DEFAULT ⁽³⁾	DESCRIPTION																			
10h	7:5	SSC1_7 [2:0]	000b	SSC1: PLL1 SSC selection (modulation amount). ⁽⁴⁾ <table border="0"> <tr> <td>Down</td> <td>Center</td> </tr> <tr> <td>000 (off)</td> <td>000 (off)</td> </tr> <tr> <td>001 – 0.25%</td> <td>001 ± 0.25%</td> </tr> <tr> <td>010 – 0.5%</td> <td>010 ± 0.5%</td> </tr> <tr> <td>011 – 0.75%</td> <td>011 ± 0.75%</td> </tr> <tr> <td>100 – 1.0%</td> <td>100 ± 1.0%</td> </tr> <tr> <td>101 – 1.25%</td> <td>101 ± 1.25%</td> </tr> <tr> <td>110 – 1.5%</td> <td>110 ± 1.5%</td> </tr> <tr> <td>111 – 2.0%</td> <td>111 ± 2.0%</td> </tr> </table>		Down	Center	000 (off)	000 (off)	001 – 0.25%	001 ± 0.25%	010 – 0.5%	010 ± 0.5%	011 – 0.75%	011 ± 0.75%	100 – 1.0%	100 ± 1.0%	101 – 1.25%	101 ± 1.25%	110 – 1.5%	110 ± 1.5%	111 – 2.0%	111 ± 2.0%
	Down	Center																					
	000 (off)	000 (off)																					
001 – 0.25%	001 ± 0.25%																						
010 – 0.5%	010 ± 0.5%																						
011 – 0.75%	011 ± 0.75%																						
100 – 1.0%	100 ± 1.0%																						
101 – 1.25%	101 ± 1.25%																						
110 – 1.5%	110 ± 1.5%																						
111 – 2.0%	111 ± 2.0%																						
4:2	SSC1_6 [2:0]	000b																					
1:0	SSC1_5 [2:1]	000b																					
11h	7	SSC1_5 [0]	000b																				
	6:4	SSC1_4 [2:0]	000b																				
	3:1	SSC1_3 [2:0]	000b																				
	0	SSC1_2 [2]	000b																				
12h	7:6	SSC1_2 [1:0]	000b																				
	5:3	SSC1_1 [2:0]	000b																				
	2:0	SSC1_0 [2:0]	000b																				
13h	7	FS1_7	0b	FS1_x: PLL1 frequency selection ⁽⁴⁾ 0 – f_{VCO1_0} (predefined by PLL1_0 – multiplier/divider value) 1 – f_{VCO1_1} (predefined by PLL1_1 – multiplier/divider value)																			
	6	FS1_6	0b																				
	5	FS1_5	0b																				
	4	FS1_4	0b																				
	3	FS1_3	0b																				
	2	FS1_2	0b																				
	1	FS1_1	0b																				
	0	FS1_0	0b																				
14h	7	MUX1	0b	PLL1 multiplexer:	0 – PLL1 1 – PLL1 bypass (PLL1 is in power down)																		
	6	M2	1b	Output Y2 multiplexer:	0 – Pdiv1 1 – Pdiv2																		
	5:4	M3	10b	Output Y3 Multiplexer:	00 – Pdiv1-divider 01 – Pdiv2-divider 10 – Pdiv3-divider 11 – Reserved																		
	3:2	Y2Y3_ST1	00b	Y2, Y3- State0/1definition:	00 – Y2 and Y3 disabled to Hi-Z state (PLL1 is in power down) 01 – Y2 and Y3 disabled to Hi-Z state 10 – Y2 and Y3 disabled to low 11 – Y2 and Y3 enabled																		
	1:0	Y2Y3_ST0	01b																				
15h	7	Y2Y3_7	0b	Y2Y3_x output state selection. ⁽⁴⁾ 0 – State0 (predefined by Y2Y3_ST0) 1 – State1 (predefined by Y2Y3_ST1)																			
	6	Y2Y3_6	0b																				
	5	Y2Y3_5	0b																				
	4	Y2Y3_4	0b																				
	3	Y2Y3_3	0b																				
	2	Y2Y3_2	0b																				
	1	Y2Y3_1	0b																				
	0	Y2Y3_0	0b																				
16h	7	SSC1DC	0b	PLL1 SSC down or center selection:	0 – Down 1 – Center																		
	6:0	Pdiv2	00h	7-bit Y2-output-divider Pdiv2:	0 – Reset and standby 1 to 127 – Divider value																		
17h	7	—	0b	Reserved – do not write other than 0																			
	6:0	Pdiv3	00h	7-bit Y3-output-divider Pdiv3:	0 – Reset and standby 1 to 127 – Divider value																		

表 9-4. PLL1 Configuration Register (続き)

OFFSET ⁽¹⁾	BIT ⁽²⁾	ACRONYM	DEFAULT ⁽³⁾	DESCRIPTION			
18h	7:0	PLL1_0N [11:4]	1FFh	PLL1_0 ⁽⁵⁾ : 30-bit multiplier or divider value for frequency f_{VCO1_0} (for more information, see PLL Frequency Planning).			
19h	7:4	PLL1_0N [3:0]					
	3:0	PLL1_0R [8:5]	000h				
1Ah	7:3	PLL1_0R[4:0]					
	2:0	PLL1_0Q [5:3]	10h				
1Bh	7:5	PLL1_0Q [2:0]					
	4:2	PLL1_0P [2:0]	100b				
	1:0	VCO1_0_RANGE	00b			f_{VCO1_0} range selection:	00 – $f_{VCO1_0} < 125$ MHz 01 – $125 \text{ MHz} \leq f_{VCO1_0} < 150$ MHz 10 – $150 \text{ MHz} \leq f_{VCO1_0} < 175$ MHz 11 – $f_{VCO1_0} \geq 175$ MHz
1Ch	7:0	PLL1_1N [11:4]	1FFh			PLL1_1 ⁽⁵⁾ : 30-bit multiplier or divider value for frequency f_{VCO1_1} (for more information, see PLL Frequency Planning).	
1Dh	7:4	PLL1_1N [3:0]					
	3:0	PLL1_1R [8:5]	000h				
1Eh	7:3	PLL1_1R[4:0]					
	2:0	PLL1_1Q [5:3]	10h				
1Fh	7:5	PLL1_1Q [2:0]					
	4:2	PLL1_1P [2:0]	100b				
	1:0	VCO1_1_RANGE	00b	f_{VCO1_1} range selection:	00 – $f_{VCO1_1} < 125$ MHz 01 – $125 \text{ MHz} \leq f_{VCO1_1} < 150$ MHz 10 – $150 \text{ MHz} \leq f_{VCO1_1} < 175$ MHz 11 – $f_{VCO1_1} \geq 175$ MHz		

- (1) Writing data beyond 20h may adversely affect device function.
- (2) All data is transferred MSB-first.
- (3) Unless a custom setting is used
- (4) The user can predefine up to eight different control settings. In normal device operation, these settings can be selected by the external control pins, S0, S1, and S2.
- (5) PLL settings limits: $16 \leq q \leq 63$, $0 \leq p \leq 7$, $0 \leq r \leq 511$, $0 < N < 4096$

10 デバイスおよびドキュメントのサポート

10.1 ドキュメントのサポート

10.1.1 関連資料

関連資料については、以下を参照してください。

- テキサス・インスツルメンツ、『[CDCE\(L\)9xx ファミリの VCO アプリケーション ガイドライン](#)』アプリケーションノート
- テキサス・インスツルメンツ、『[CDCE\(L\)9xx ファミリの水晶振動子選択に関する実践的な考慮事項](#)』アプリケーションノート
- テキサス・インスツルメンツ、『[CDCE\(L\)9xx ファミリの一般的な I²C/EEPROM の使用法](#)』アプリケーションノート
- テキサス・インスツルメンツ、『[水晶発振子または発振器とシリコン デバイスの置き換え](#)』アプリケーションノート
- テキサス・インスツルメンツ、『[CDCE\(L\)949, CDCE\(L\)937, CDCE\(L\)925, CDCE\(L\)813 向け I²C の使用方法](#)』アプリケーションノート
- テキサス・インスツルメンツ、『[低周波数ワード クロックからのオーディオ データ コンバータ用低位相ノイズ クロックの生成](#)』アプリケーションノート

10.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

10.3 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.6 用語集

[テキサス・インスツルメンツ用語集](#)

この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (April 2019) to Revision D (February 2024)	Page
ドキュメント全体にわたって表、図、相互参照の採番方法を更新.....	1
I ² C に言及している場合、すべての旧式の用語をコントローラおよびターゲットに変更.....	1
製品情報表を「パッケージ情報」に変更	1
Added information on allowable data inputs during the EEPROM write cycle in <i>Data Protocol</i>	15

Changes from Revision B (May 2018) to Revision C (April 2019)	Page
データシートに CDCE813R02-Q1 の発注情報を追加.....	1
デバイス比較表を追加	1
Added default configuration information to the S0 pin description.....	4
Removed 'CDCE813-Q1' text from the V _{DDOUT} pin description. The information applies to both CDCE813-Q1 and CDCE813R02-Q1 orderables.....	4
Added S0 pin information in the <i>Overview</i> section.....	12
Added S0 pin information to the <i>Default Device Configuration</i> section.....	14
Added <i>CDCE813R02-Q1 Default Configuration</i> graphic.....	14
Changed S0 pin information in the <i>Factory Default Setting for Control Terminal Register</i> table.....	14
Added Y1_ST1 default settings for the CDCE813-Q1 and CDCE813R02-Q1 orderables.....	25
Added Y1_1 default settings for the CDCE813-Q1 and CDCE813R02-Q1 orderables.....	25

Changes from Revision A (May 2018) to Revision B (May 2018)	Page
Changed the text in the <i>Default Device Configuration</i> section from: However the outputs are disabled by default and need to be turned on through I ² C or with the S0 pin to: However the outputs are disabled by default and need to be turned on through I ² C.....	14
Changed the <i>Factory Default Setting</i> table and <i>Default Configuration</i> graphic text to show that the Y1 outputs as 3-state when S0 = 1 or S0 = 0.....	14
Changed the default value of the TARGET 1:0 bits from: 00b to: 01b in the <i>Generic Configuration Register</i> table.....	25
Changed the default value of the Y1_ST0 3:2 bits from: 11b to: 01b in the <i>Generic Configuration Register</i> table.....	25
Changed the default value of the BCOUNT 7:1 bits from: 20h to: 00h in the <i>Generic Configuration Register</i> table.....	25
Changed the default value of the Y2Y3_1 bit from: 1b to: 0b in the <i>PLL1 Configuration Register</i> table.....	25

Changes from Revision * (January 2017) to Revision A (May 2018)	Page
Changed the <i>Factory Default Setting</i> table and <i>Default Configuration</i> graphic text to show that S0 = 1 means Y1 outputs 3-state and S0 = 0 means Y1 is enabled.....	14

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCE813QPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	CE813Q	Samples
CDCE813R02TPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	E813Q02	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCE813QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CDCE813R02TPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCE813QPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0
CDCE813R02TPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0

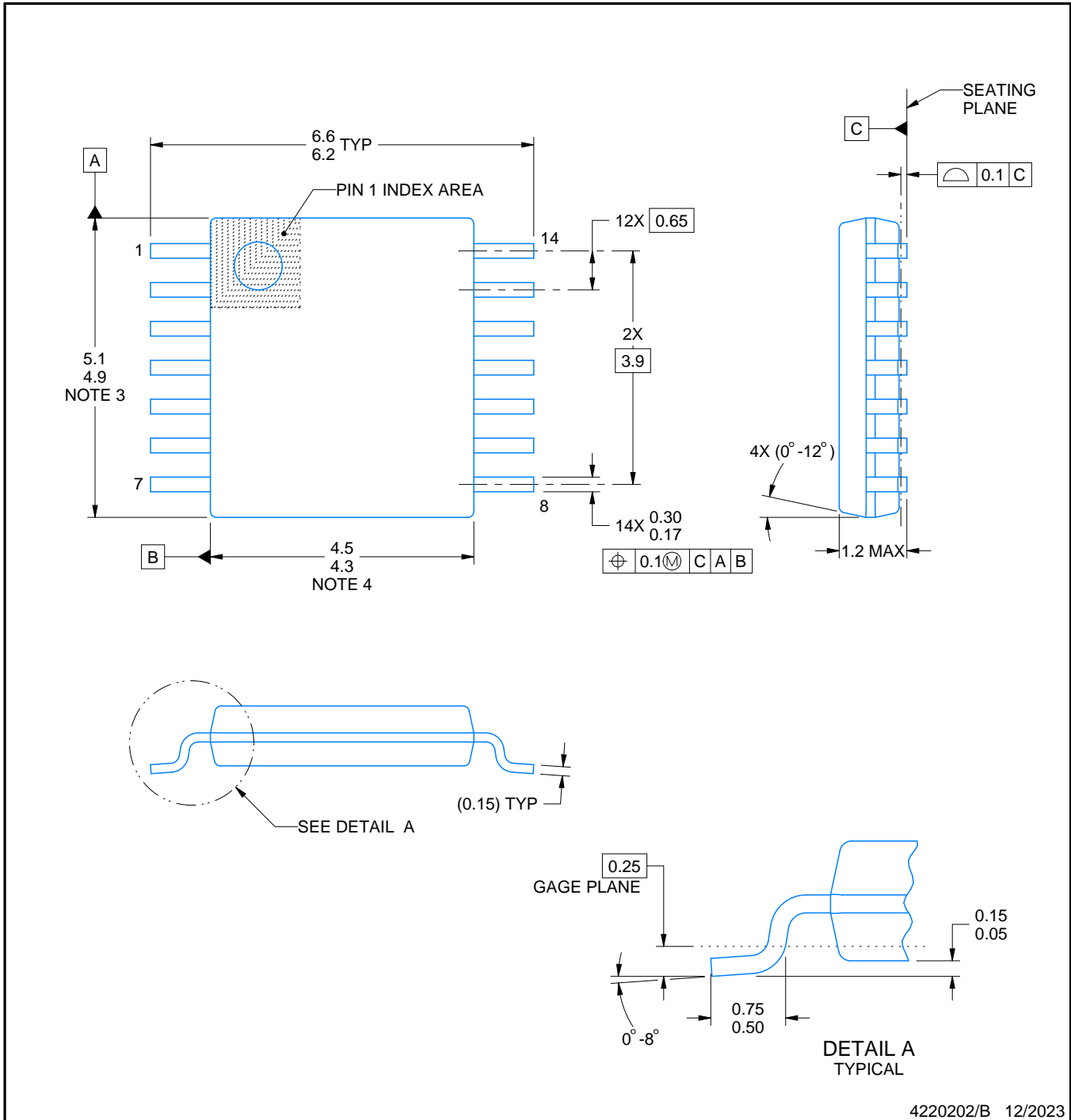
PW0014A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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