CSD16321Q5 25V、N チャネル NexFET™ パワー MOSFET

1 特長

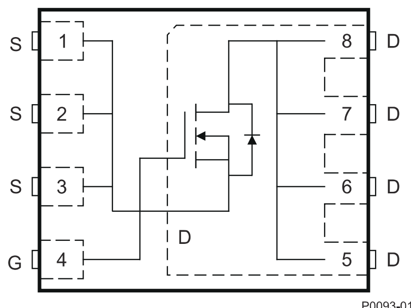
- 5V ゲートの駆動に最適化
- 非常に低い Q_g および Q_{gd}
- 低い熱抵抗
- アバランシェ定格
- 鉛フリーの端子メッキ処理
- RoHS 準拠
- SON 5mm × 6mm プラスチック・パッケージ

2 アプリケーション

- ネットワーク、テレコム、コンピューティング・システム・アプリケーション用のポイント・オブ・ロード(POL)同期整流降圧型コンバータ
- 同期 FET アプリケーション用に最適化

3 概要

この 25V、1.9mΩ、5mm × 6mm の SON NexFET™ パワー MOSFET は、電力変換アプリケーションでの損失を最小限に抑えるように設計されています。



上面図

製品概要

T_A = 25℃		標準値		単位
V_{DS}	ドレイン - ソース間電圧	25		V
Q_g	ゲートの合計電荷 (4.5V)	14		nC
Q_{gd}	ゲート-ドレイン間ゲート電荷	2.5		nC
$R_{DS(on)}$	ドレイン - ソース間オン抵抗	V_{GS} = 3V	2.8	mΩ
		V_{GS} = 4.5V	2.1	
		V_{GS} = 8V	1.9	
$V_{GS(th)}$	スレッショルド電圧	1.1		V

製品情報 (1)

デバイス	メディア	数量	パッケージ	出荷形態
CSD16321Q5	13 インチ・リール	2500	SON 5.00mm × 6.00mm プラスチック パッケージ	テープおよびリール
CSD16321Q5T	7 インチ・リール	250		

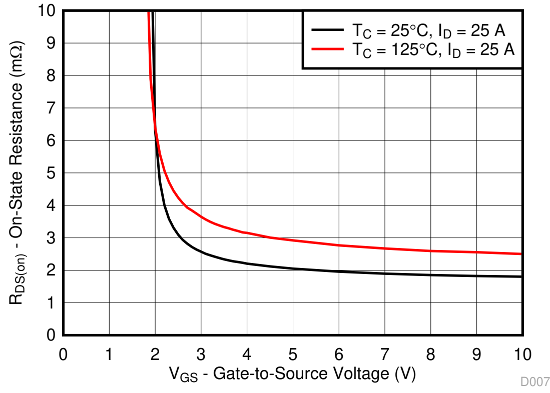
(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。

絶対最大定格

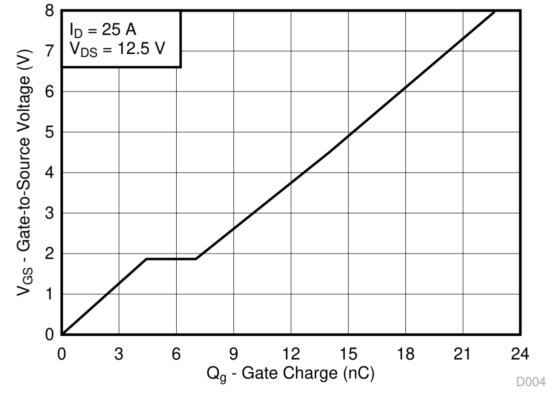
T_A = 25℃		値	単位
V_{DS}	ドレイン - ソース間電圧	25	V
V_{GS}	ゲート - ソース間電圧	+10 / –8	V
I_D	連続ドレイン電流 (パッケージ制限)	100	A
	連続ドレイン電流 (シリコン制限)、T_C = 25℃	177	
	連続ドレイン電流(1)	29	
I_{DM}	パルス・ドレイン電流(2)	400	A
P_D	消費電力(1)	3.1	W
	消費電力、T_C = 25℃	113	
T_J、T_{stg}	動作時の接合部温度、保存温度	–55～150	℃
E_{AS}	アバランシェ エネルギー、単一パルス I_D = 66A、L = 0.1mH、R_G = 25Ω	218	mJ

(1) 厚さ 0.06in の FR4 PCB 上に構築された面積 $1in^2$、2 オンスの Cu パッド上で、標準値 $R_{θJA}$ = 40°C/W
(2) 最大 $R_{θJC}$ = 1.1°C/W、パルス期間 ≤ 100μs、デューティ・サイクル ≤ 1%

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。



$R_{DS(on)}$ と V_{GS} との関係



ゲート電荷

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4 Specifications

4.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_D = 250 μA	25			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = 20 V			1	μA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = +10 / –8 V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_D = 250 μA	0.9	1.1	1.4	V
$R_{DS(on)}$	Drain-to-source on resistance	V_{GS} = 3 V, I_D = 25 A		2.8	3.8	mΩ
		V_{GS} = 4.5 V, I_D = 25 A		2.1	2.6	
		V_{GS} = 8 V, I_D = 25 A		1.9	2.4	
g_{fs}	Transconductance	V_{DS} = 12.5 V, I_D = 25 A		150		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 12.5 V, f = 1 MHz		2360	3100	pF
C_{oss}	Output capacitance			1700	2200	pF
C_{rss}	Reverse transfer capacitance			115	150	pF
R_G	Series gate resistance			1.5	3	Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 12.5 V, I_D = 25 A		14	19	nC
Q_{gd}	Gate charge gate-to-drain			2.5		nC
Q_{gs}	Gate charge gate-to-source			4		nC
$Q_{g(th)}$	Gate charge at V_{th}			2.1		nC
Q_{oss}	Output charge	V_{DS} = 15 V, V_{GS} = 0 V		36		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = 12.5 V, V_{GS} = 4.5 V, I_D = 25 A, R_G = 2 Ω		9		ns
t_r	Rise time			15		ns
$t_{d(off)}$	Turnoff delay time			27		ns
t_f	Fall time			17		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 25 A, V_{GS} = 0 V		0.8	1	V
Q_{rr}	Reverse recovery charge	V_{DD} = 13 V, I_F = 25 A, di/dt = 300 A/μs		33		nC
t_{rr}	Reverse recovery time	V_{DD} = 13 V, I_F = 25 A, di/dt = 300 A/μs		32		ns

4.2 Thermal Information

T_A = 25°C (unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance(1)			1.1	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1) (2)			50	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-in^2, 2-oz Cu pad on a 1.5-in × 1.5-in, 0.06-in thick FR4 board. $R_{\theta JC}$ is specified by design while $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 Material with 1 in^2 of 2-oz Cu.

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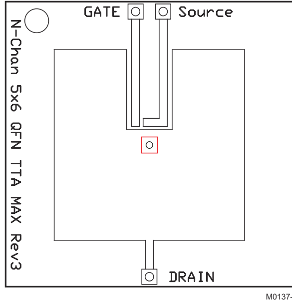
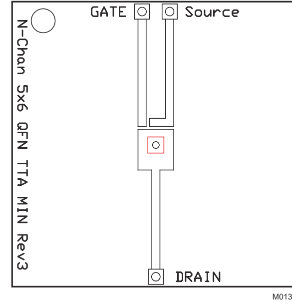


Max $R_{\theta JA}$ = 50°C/W when mounted on 1 in^2 of 2-oz Cu.



Max $R_{\theta JA}$ = 125°C/W when mounted on minimum pad area of 2-oz Cu.

4.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

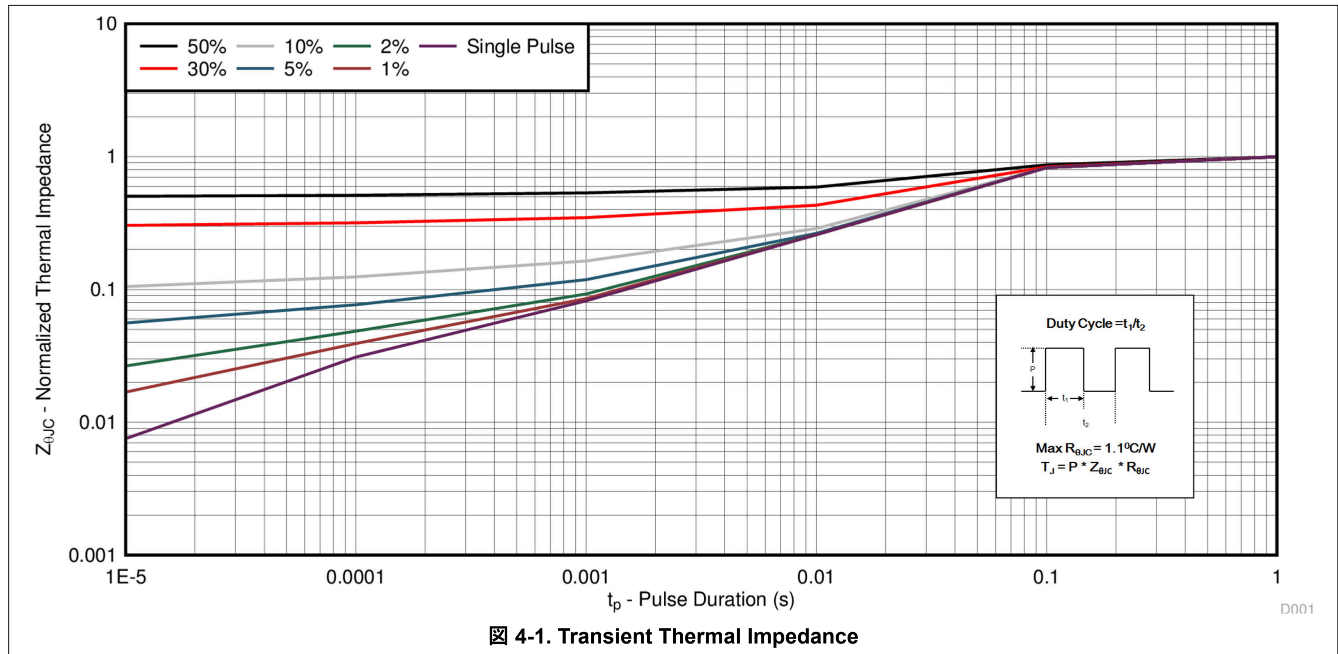


図 4-1. Transient Thermal Impedance

4.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

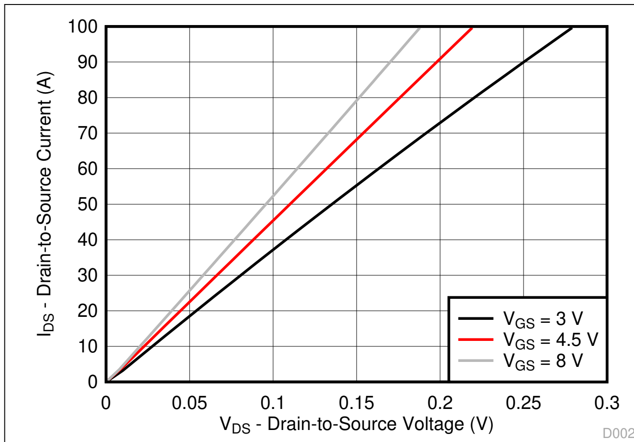
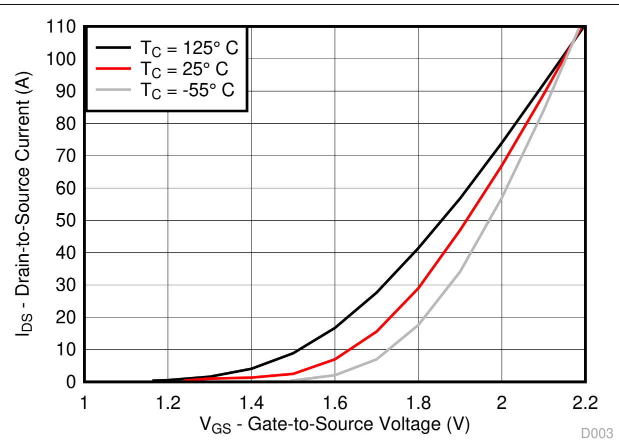
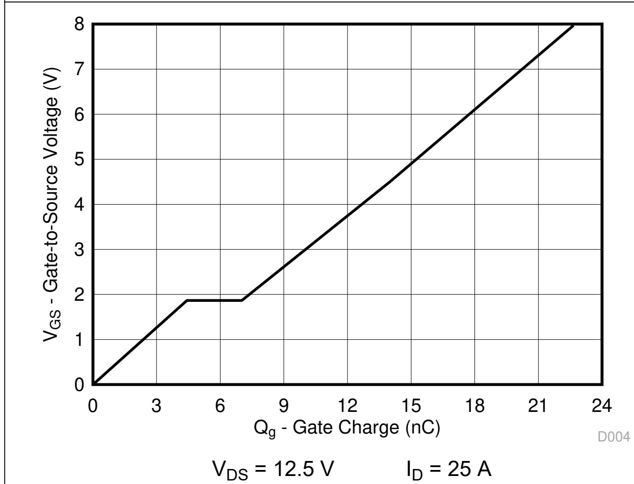


図 4-2. Saturation Characteristics



V_{DS} = 5 V

図 4-3. Transfer Characteristics



V_{DS} = 12.5 V I_D = 25 A

図 4-4. Gate Charge

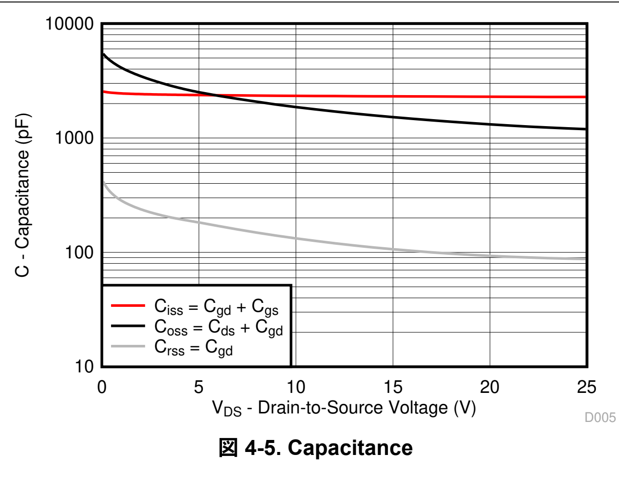
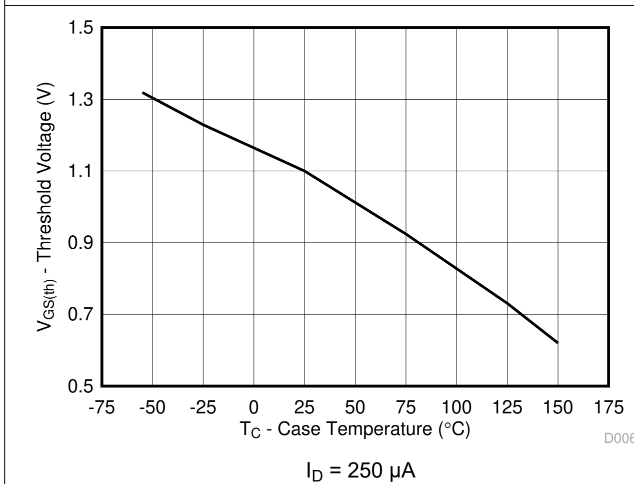


図 4-5. Capacitance



I_D = 250 µA

図 4-6. Threshold Voltage vs Temperature

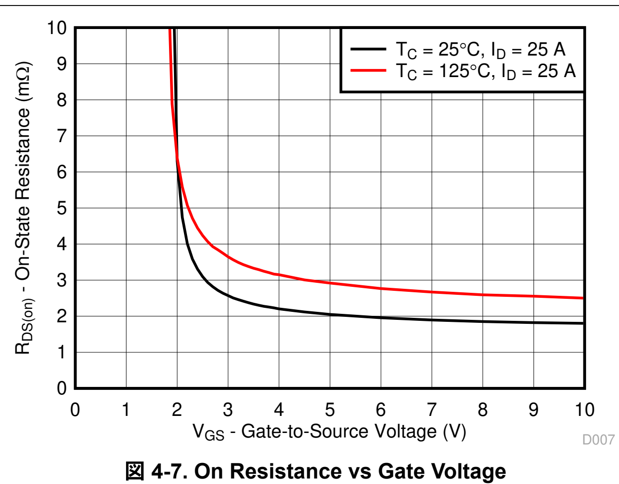


図 4-7. On Resistance vs Gate Voltage

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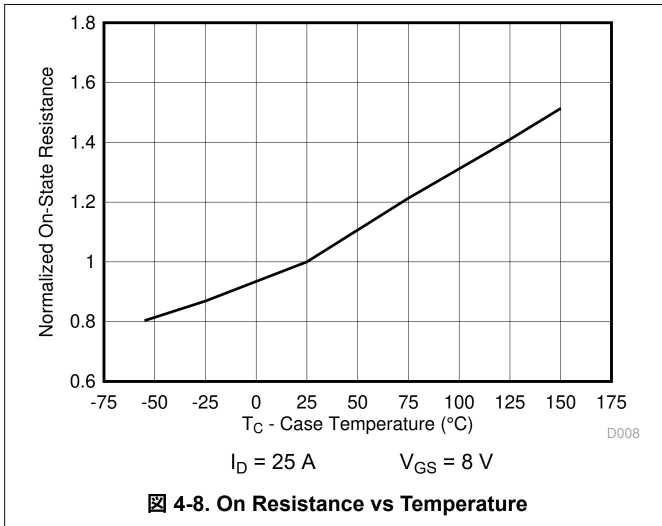
4.3 Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)



I_D = 25 A V_{GS} = 8 V

図 4-8. On Resistance vs Temperature

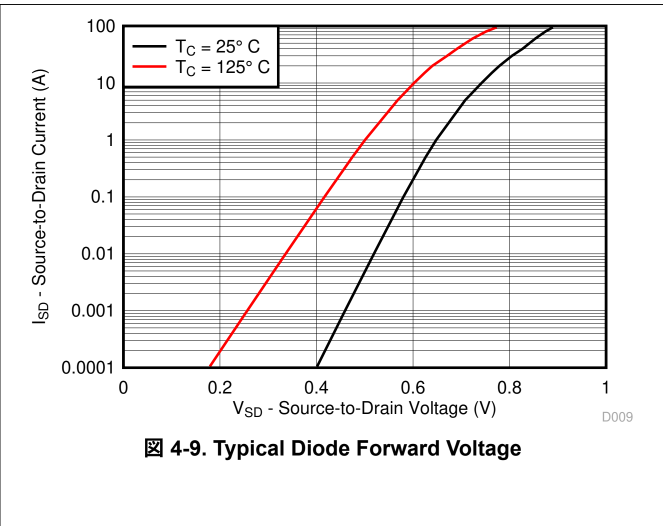
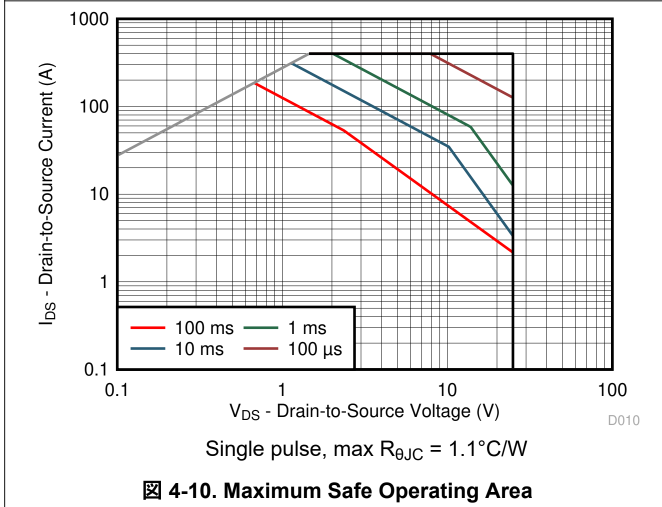


図 4-9. Typical Diode Forward Voltage



Single pulse, max $R_{\theta JC}$ = 1.1°C/W

図 4-10. Maximum Safe Operating Area

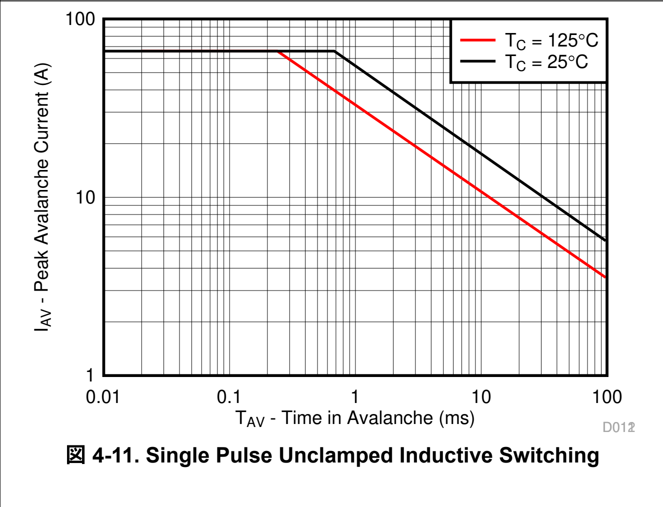


図 4-11. Single Pulse Unclamped Inductive Switching

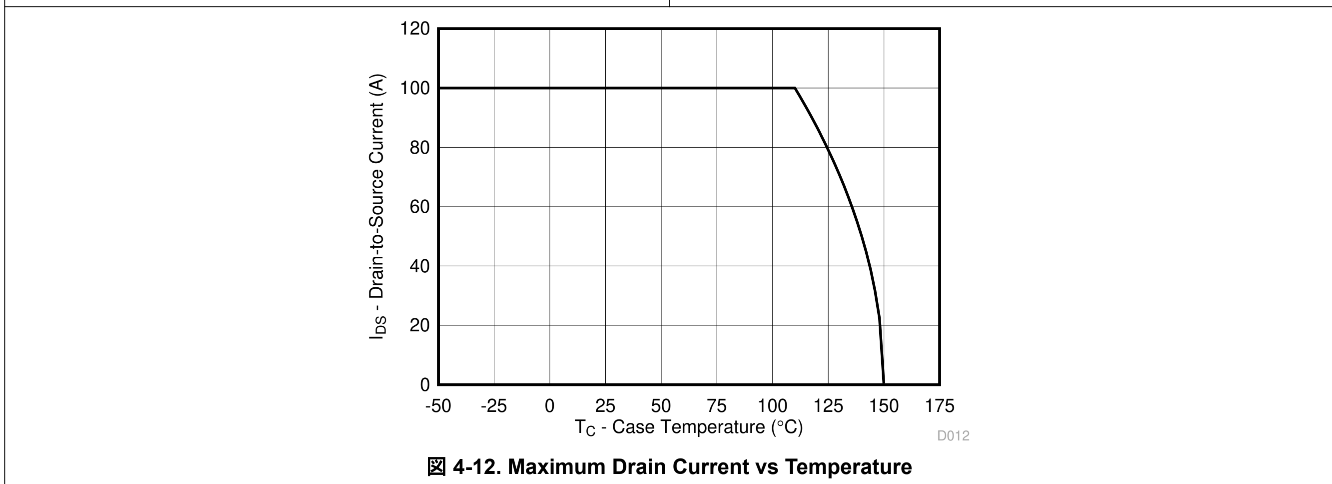


図 4-12. Maximum Drain Current vs Temperature

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5 Device and Documentation Support

5.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

5.2 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

5.5 用語集

テキサス・インスツルメンツ用語集	この用語集には、用語や略語の一覧および定義が記載されています。

6 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (May 2017) to Revision E (December 2023) — **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新 1

Changes from Revision C (December 2016) to Revision D (May 2017) — **Page**

- 3V、4.5V、8V での $R_{DS(ON)}$ の値と説明を「電気的特性」の表の値と一致するように変更 1

Changes from Revision B (May 2010) to Revision C (December 2016) — **Page**

- 「概要」の記述を変更 1
- 「絶対最大定格」の表にシリコン制限連続ドレイン電流を追加 1
- 「絶対最大定格」の表に T_C = 25℃での最大消費電力を追加 1
- 「絶対最大定格」の表の注 2 を変更 1
- Changed $R_{θJA}$ max from 48°C/W : to 50°C/W 4
- Changed the SOA in 図 4-10 to reflect measured data 5
- Changed *MECHANICAL DATA* section to *Mechanical, Packaging, and Orderable Information* section 10

Changes from Revision A (January 2010) to Revision B (May 2010) — **Page**

- Changed $R_{DS(on)}$ - V_{GS} = 3 V, I_D = 25 A MAX value From: 3.5 To: 3.8 4

Changes from Revision * (August 2009) to Revision A (January 2010) — **Page**

- 上面図のピン配置図のラベルを変更 1

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- 絶対最大定格 の注 1 を $R_{θJA}$ = 39℃/W から $R_{θJA}$ = 39℃/W (標準値) に変更 1
- Changed 図 4-1 text From: $R_{θJA}$ = 92°C/W To: Typical $R_{θJA}$ = 93°C/W 5
- Changed 図 4-10 text From: $R_{θJA}$ = 92°C/W To: Typical $R_{θJA}$ = 93°C/W 5
- Changed 図 4-11 X-axis values 5

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7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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7.1 Package Option Addendum

Packaging Information

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan(2)	Lead/Ball Finish(6)	MSL Peak Temp(3)	Op Temp (°C)	Device Marking(4) (5)
CSD16321Q5	ACTIVE (1)	VSON-CLIP	DQH	8	2500	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD16321
CSD16321Q5T	ACTIVE	VSON-CLIP	DQH	8	250	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD16321

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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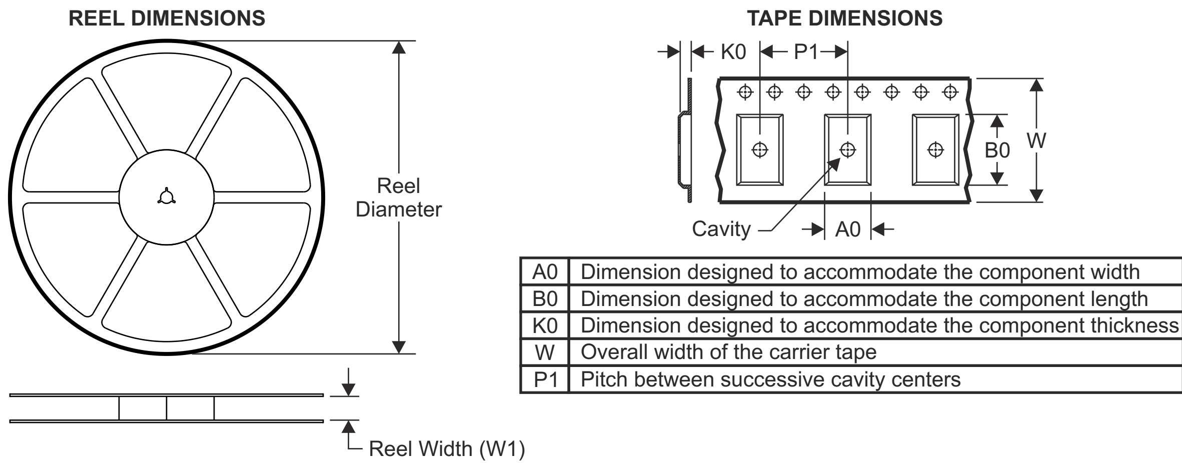
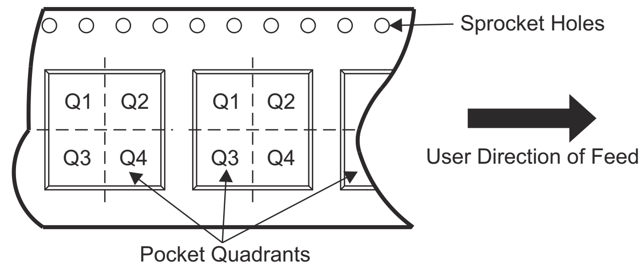
7.2 Tape and Reel Information





Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD16321Q5T	VSON-CLIP	DQH	8	250	178.0	12.4	6.3	5.3	1.2	8.0	12.0	Q1

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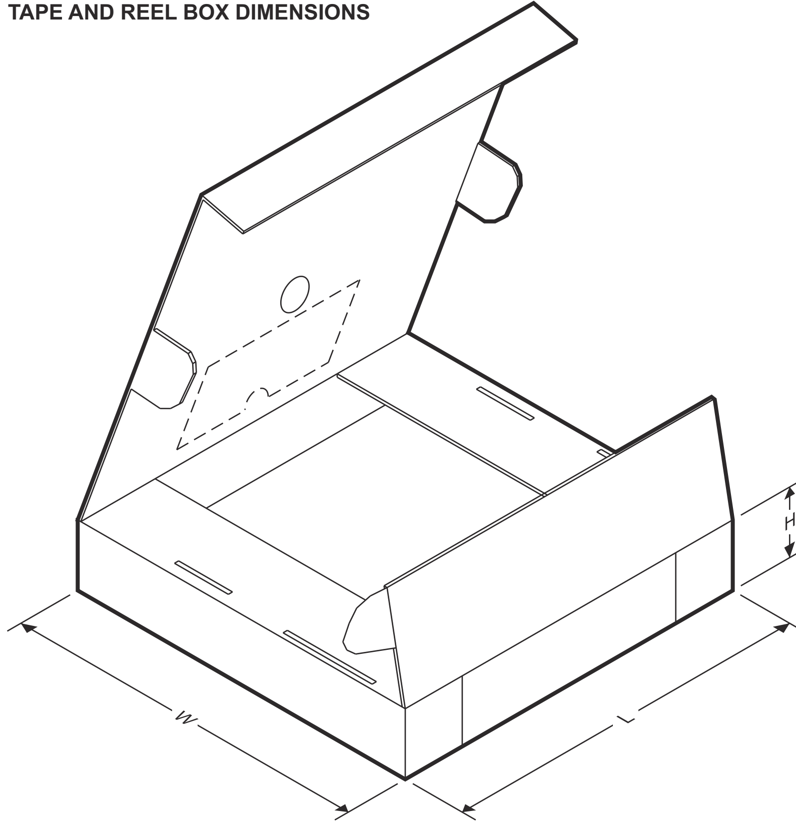
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD16321Q5T	VSON-CLIP	DQH	8	250	180.0	180.0	79.0

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PACKAGE OUTLINE

DQH0008A

VSON-CLIP - 1.05 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

B
6.1
5.9
A
PIN 1 INDEX AREA
5.1
4.9
C
1.05 MAX
SEATING PLANE
0.05
0.00
0.08 C
4.018 ±0.1
2.39 ±0.05
(0.2) TYP
EXPOSED
THERMAL PAD
4
5
2X
3.81
SYMM
9
4.42 ±0.1
6X 1.27
8
1
4X 0.71
0.51
PKG
4X 0.71
0.51
8X 0.46
0.36
0.1Ⓜ C A B
0.05Ⓜ C
PIN 1 ID
(OPTIONAL)

4223292/A 10/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

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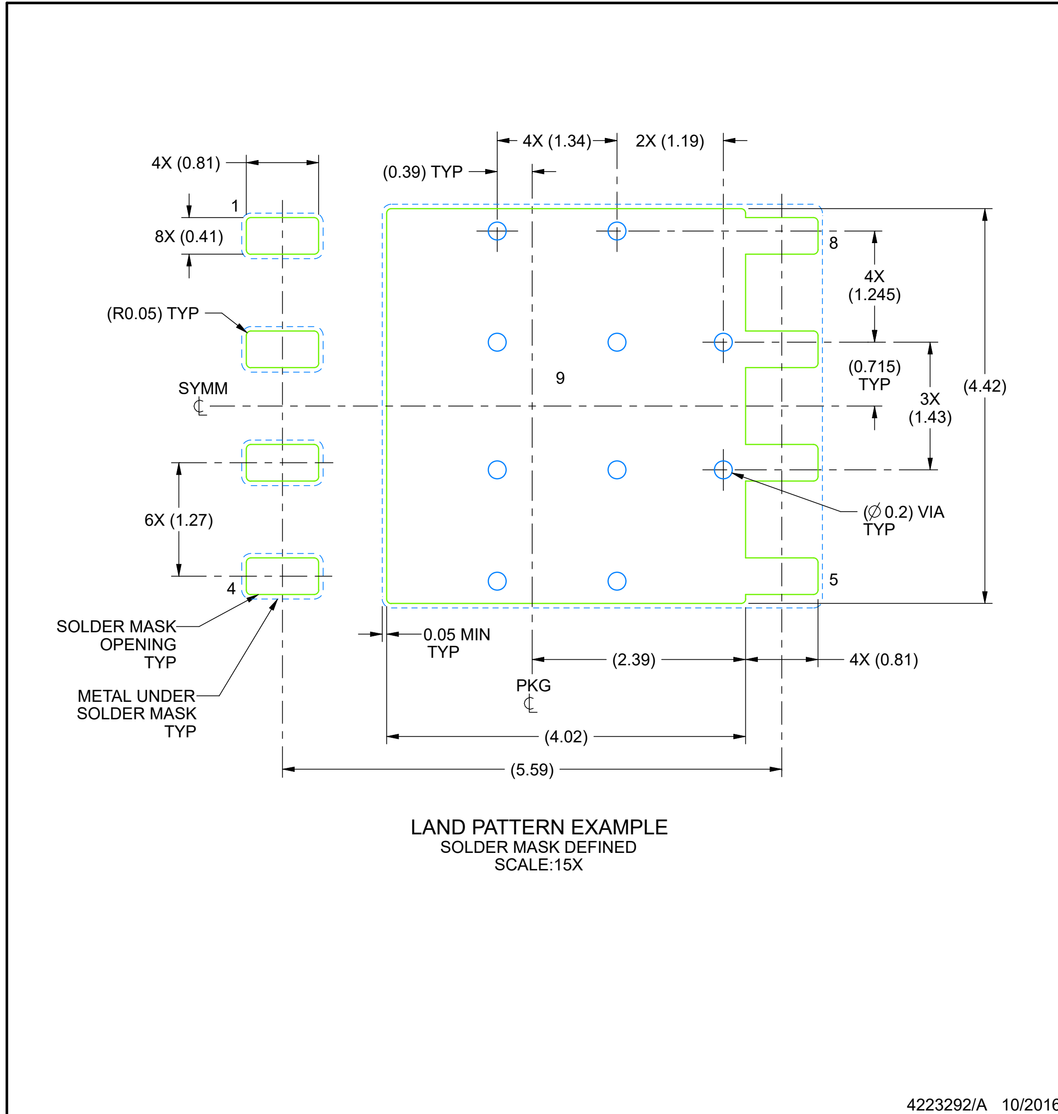
EXAMPLE BOARD LAYOUT

DQH0008A VSON-CLIP - 1.05 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:15X

4223292/A 10/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

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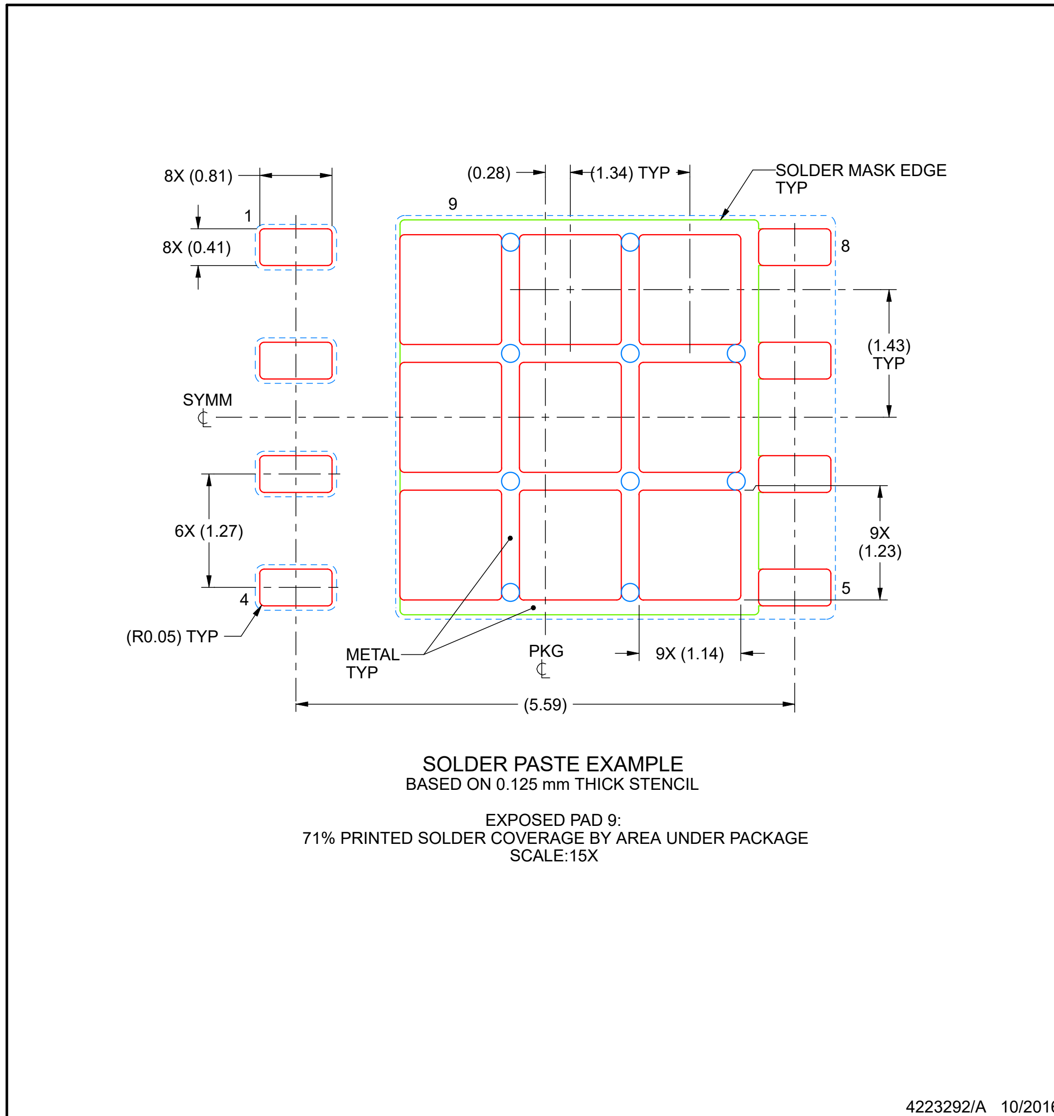
EXAMPLE STENCIL DESIGN

DQH0008A

VSON-CLIP - 1.05 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

4223292/A 10/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD16321Q5	ACTIVE	VSON-CLIP	DQH	8	2500	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD16321	Samples
CSD16321Q5T	ACTIVE	VSON-CLIP	DQH	8	250	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD16321	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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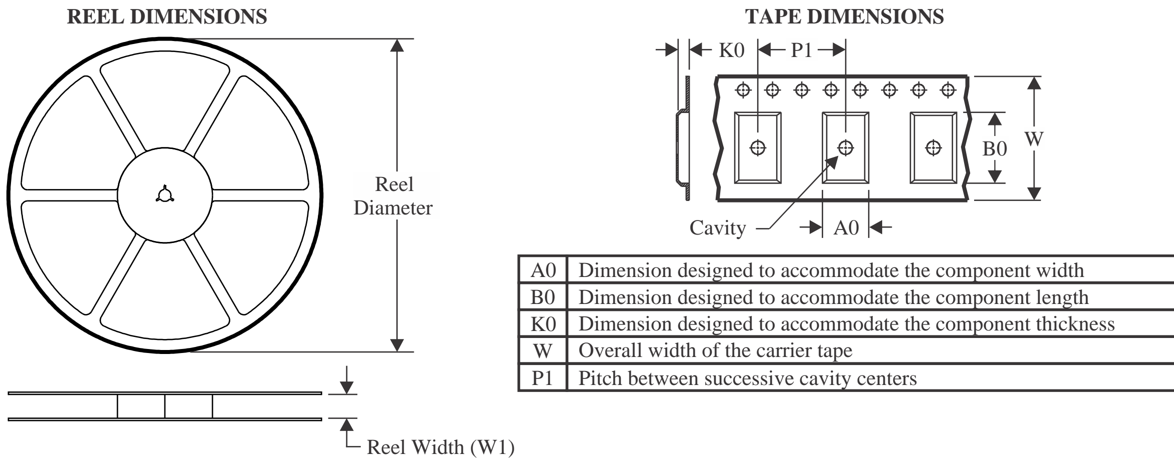
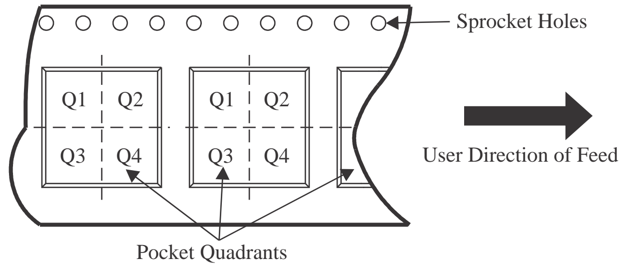
TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

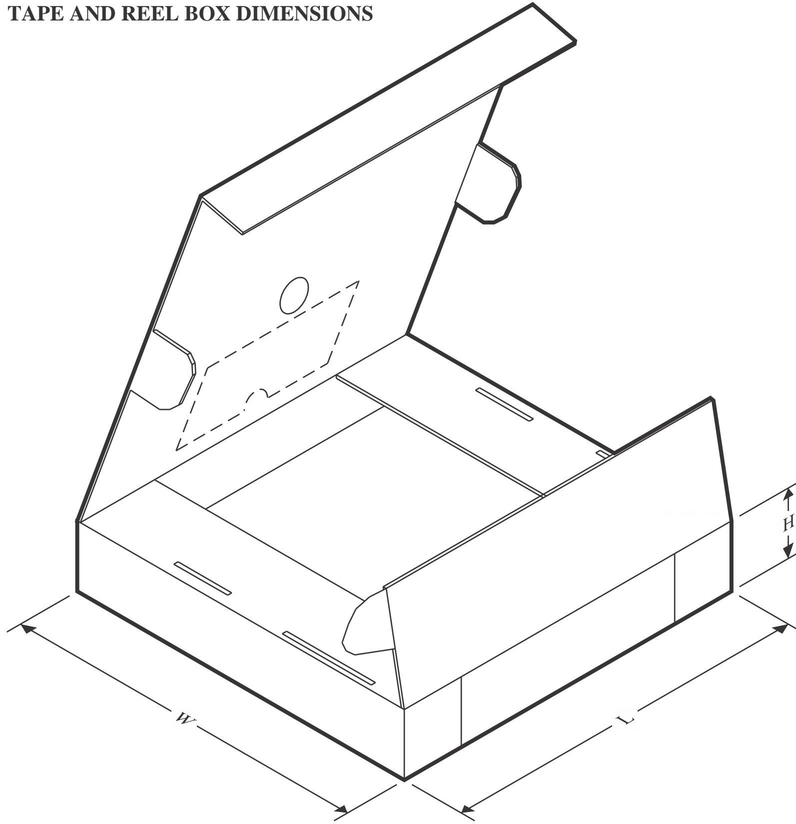
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD16321Q5T	VSON-CLIP	DQH	8	250	178.0	12.4	6.3	5.3	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD16321Q5T	VSON-CLIP	DQH	8	250	180.0	180.0	79.0

PACKAGE OUTLINE

VSON-CLIP - 1.05 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

4223292/A 10/2016

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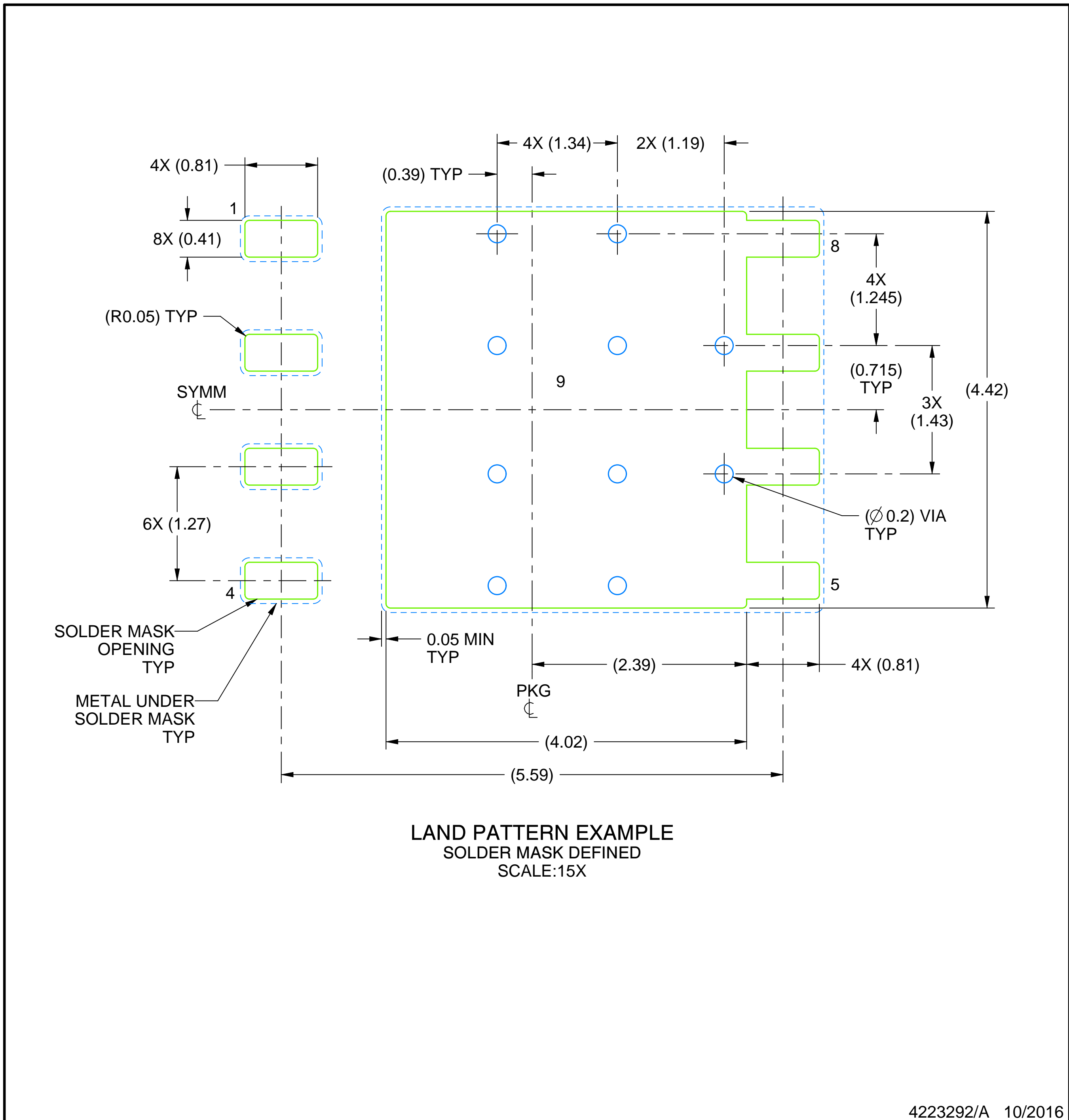

LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:15X

4223292/A 10/2016

NOTES: (continued)

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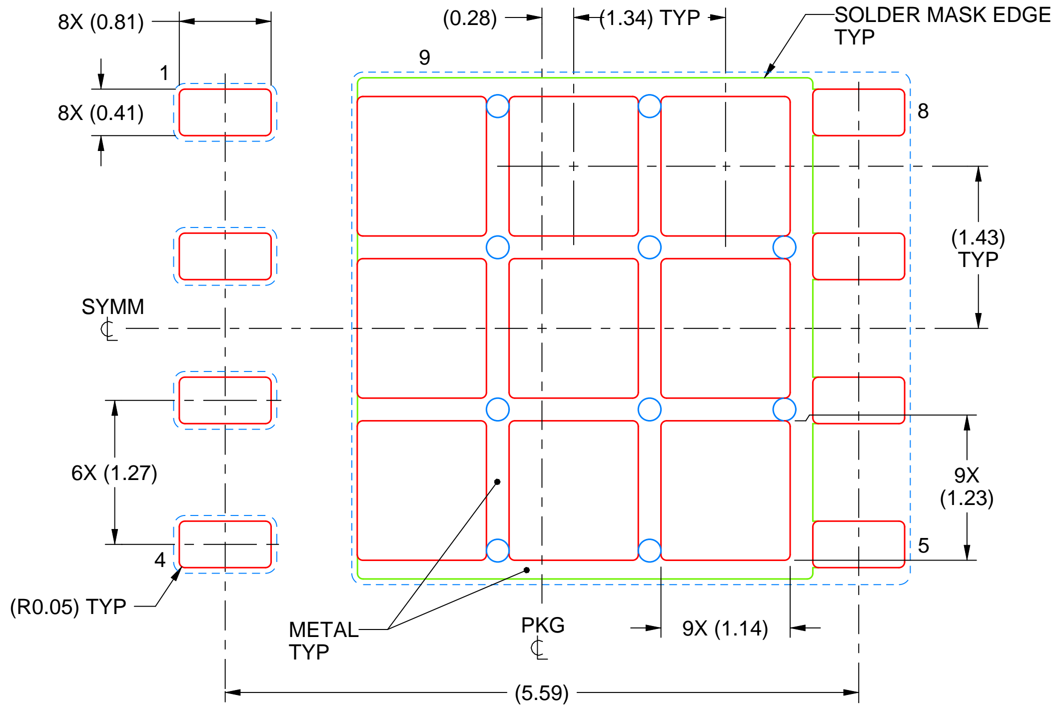

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

4223292/A 10/2016

NOTES: (continued)

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