TEXAS INSTRUMENTS
CSD17483F4
JAJSFA6F – JULY 2013 – REVISED FEBRUARY 2022

# CSD17483F4 30V N チャネル FemtoFET™ MOSFET

## 1 特長

- 低オン抵抗
- 低い $Q_g$ および $Q_{gd}$
- 低いスレッショルド電圧
- 非常に小さな外形 (0402 ケース・サイズ)
  - 1.0mm × 0.6mm
- 超薄型プロファイル
  - 高さ 0.36mm
- ESD 保護ダイオード搭載
  - HBM 定格 4kV 超
  - CDM 定格 2kV 超
- 鉛およびハロゲン不使用
- RoHS 準拠

## 2 アプリケーション

- ロード・スイッチ・アプリケーションに最適
- 汎用スイッチング・アプリケーションに最適
- 単一セル・バッテリのアプリケーション
- ハンドヘルドおよびモバイル・アプリケーション

## 3 概要

この 200mΩ、30V N チャネル FemtoFET™ MOSFET テクノロジは、さまざまなハンドヘルドおよびモバイル・アプリケーション向けに、フットプリントを最小化するよう設計され、最適化されています。標準の小信号 MOSFET をこのテクノロジに置き換えて、占有面積を 60% 以上減らすことができます。

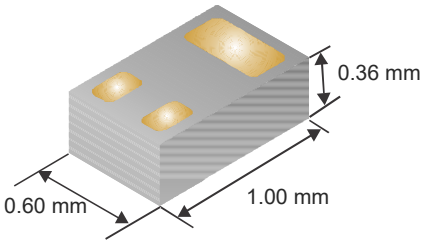


**図 3-1. 標準的な部品寸法**

**製品概要**

| $T_A$ = 25℃ | | 標準値 | | 単位 |
|---|---|---|---|---|
| $V_{DS}$ | ドレイン - ソース間電圧 | 30 | | V |
| $Q_g$ | ゲートの合計電荷 (4.5V) | 1010 | | pC |
| $Q_{gd}$ | ゲート電荷、ゲート - ドレイン間 | 130 | | pC |
| $R_{DS(on)}$ | ドレイン - ソース間オン抵抗 | $V_{GS}$ = 1.8V | 370 | mΩ |
| | | $V_{GS}$ = 2.5V | 240 | |
| | | $V_{GS}$ = 4.5V | 200 | |
| $V_{GS(th)}$ | スレッショルド電圧 | 0.85 | | V |

**製品情報**

| デバイス(1) | 数量 | メディア | パッケージ | 出荷形態 |
|---|---|---|---|---|
| CSD17483F4 | 3000 | 7 インチ・リール | Femto (0402) 1.00mm × 0.60mm SMD リード・レス | テープ・アンド・リール |
| CSD17483F4T | 250 | | | |

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。

**絶対最大定格**

| $T_A$ = 25℃ (特に記述のない限り) | | 値 | 単位 |
|---|---|---|---|
| $V_{DS}$ | ドレイン - ソース間電圧 | 30 | V |
| $V_{GS}$ | ゲート - ソース間電圧 | 12 | V |
| $I_D$ | 連続ドレイン電流、$T_A$ = 25℃(1) | 1.5 | A |
| $I_{DM}$ | パルス・ドレイン電流、$T_A$ = 25℃(2) | 5 | A |
| $I_G$ | 連続ゲート・クランプ電流 | 35 | mA |
| | パルス・ゲート・クランプ電流(2) | 350 | |
| $P_D$ | 消費電力(1) | 500 | mW |
| $V_{(ESD)}$ | 人体モデル (HBM) | 4 | kV |
| | デバイス帯電モデル (CDM) | 2 | |
| $T_J$、$T_{stg}$ | 動作時の接合部温度、保存温度 | –55～150 | ℃ |
| $E_{AS}$ | アバランシェ・エネルギー、単一パルス $I_D$ = 7.4A、L = 0.1mH、$R_G$ = 25Ω | 2.7 | mJ |

(1) $R_{\theta JA}$ = 90℃/W (標準値、厚さ 0.06 インチ (1.52mm) の FR4 PCB 上の面積 1 平方インチ (6.45cm$^2$)、厚さ 2oz (0.071mm) の Cu パッドに実装した場合)
(2) パルス幅 ≤ 300µs、デューティ・サイクル ≤ 2%

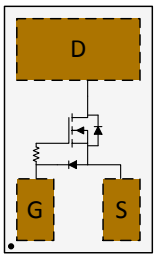


**図 3-2. 上面図**

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## 4 Revision History

**Changes from Revision E (April 2018) to Revision F (February 2022)** **Page**

- 超薄型プロファイルの箇条書き項目を、高さ 0.35mm から 0.36mm に変更。 ..... 1
- 超薄型プロファイルの画像の高さを 0.35mm から 0.36mm に更新。 ..... 1
- Changed ultra-low profile image height from 0.35 mm to 0.36 mm ..... 8
- Added FemtoFET Surface Mount Guide note ..... 9

**Changes from Revision D (Decermber 2016) to Revision E (April 2018)** **Page**

- Raised $I_{DSS}$ Test Condition Voltage ..... 3
- Raised $I_{GSS}$ Test Condition Voltage ..... 3

# 5 Specifications

## 5.1 Electrical Characteristics

$T_A$ = 25°C (unless otherwise stated)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **STATIC CHARACTERISTICS** | | | | | | |
| $BV_{DSS}$ | Drain-to-source voltage | $V_{GS}$ = 0 V, $I_{DS}$ = 250 µA | 30 | | | V |
| $I_{DSS}$ | Drain-to-source leakage current | $V_{GS}$ = 0 V, $V_{DS}$ = 24 V | | | 100 | nA |
| $I_{GSS}$ | Gate-to-source leakage current | $V_{DS}$ = 0 V, $V_{GS}$ = 10 V | | | 50 | nA |
| $V_{GS(th)}$ | Gate-to-source threshold voltage | $V_{DS}$ = $V_{GS}$, $I_{DS}$ = 250 µA | 0.65 | 0.85 | 1.10 | V |
| $R_{DS(on)}$ | Drain-to-source on-resistance | $V_{GS}$ = 1.8 V, $I_{DS}$ =0.5 A | | 370 | 550 | mΩ |
| | | $V_{GS}$ = 2.5 V, $I_{DS}$ =0.5 A | | 240 | 310 | |
| | | $V_{GS}$ = 4.5 V, $I_{DS}$ = 0.5 A | | 200 | 260 | |
| | | $V_{GS}$ = 8 V, $I_{DS}$ = 0.5 A | | 185 | 240 | |
| $g_{fs}$ | Transconductance | $V_{DS}$ = 15 V, $I_{DS}$ = 0.5 A | | 2.4 | | S |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| $C_{iss}$ | Input capacitance | $V_{GS}$ = 0 V, $V_{DS}$ = 15 V, $f$ = 1 MHz | | 145 | 190 | pF |
| $C_{oss}$ | Output capacitance | | | 42 | 55 | pF |
| $C_{rss}$ | Reverse transfer capacitance | | | 2 | 3 | pF |
| $R_G$ | Series gate resistance | | | 23 | | Ω |
| $Q_g$ | Gate charge total (4.5 V) | $V_{DS}$ = 15 V, $I_{DS}$ = 0.5 A | | 1010 | 1300 | pC |
| $Q_{gd}$ | Gate charge gate-to-drain | | | 130 | | pC |
| $Q_{gs}$ | Gate charge gate-to-source | | | 220 | | pC |
| $Q_{g(th)}$ | Gate charge at $V_{th}$ | | | 145 | | pC |
| $Q_{oss}$ | Output charge | $V_{DS}$ = 15 V, $V_{GS}$ = 0 V | | 1095 | | pC |
| $t_{d(on)}$ | Turnon delay time | $V_{DS}$ = 15 V, $V_{GS}$ = 4.5 V, $I_{DS}$ = 0.5 A,$R_G$ = 2 Ω | | 3.3 | | ns |
| $t_r$ | Rise time | | | 1.3 | | ns |
| $t_{d(off)}$ | Turnoff delay time | | | 10.6 | | ns |
| $t_f$ | Fall time | | | 3.4 | | ns |
| **DIODE CHARACTERISTICS** | | | | | | |
| $V_{SD}$ | Diode forward voltage | $I_{SD}$ = 0.5 A, $V_{GS}$ = 0 V | | 0.73 | 0.9 | V |
| $Q_{rr}$ | Reverse recovery charge | $V_{DS}$= 15 V, $I_F$ = 0.5 A, di/dt = 300 A/µs | | 1475 | | pC |
| $t_{rr}$ | Reverse recovery time | | | 5.5 | | ns |

## 5.2 Thermal Information

$T_A$ = 25°C (unless otherwise stated)

| THERMAL METRIC | | TYPICAL VALUES | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance(1) | 90 | °C/W |
| | Junction-to-ambient thermal resistance(2) | 250 | |

(1) Device mounted on FR4 material with 1-in$^2$ (6.45-cm$^2$), 2-oz (0.071-mm) thick Cu.
(2) Device mounted on FR4 material with minimum Cu mounting area.

## 5.3 Typical MOSFET Characteristics

$T_A$ = 25°C (unless otherwise stated)

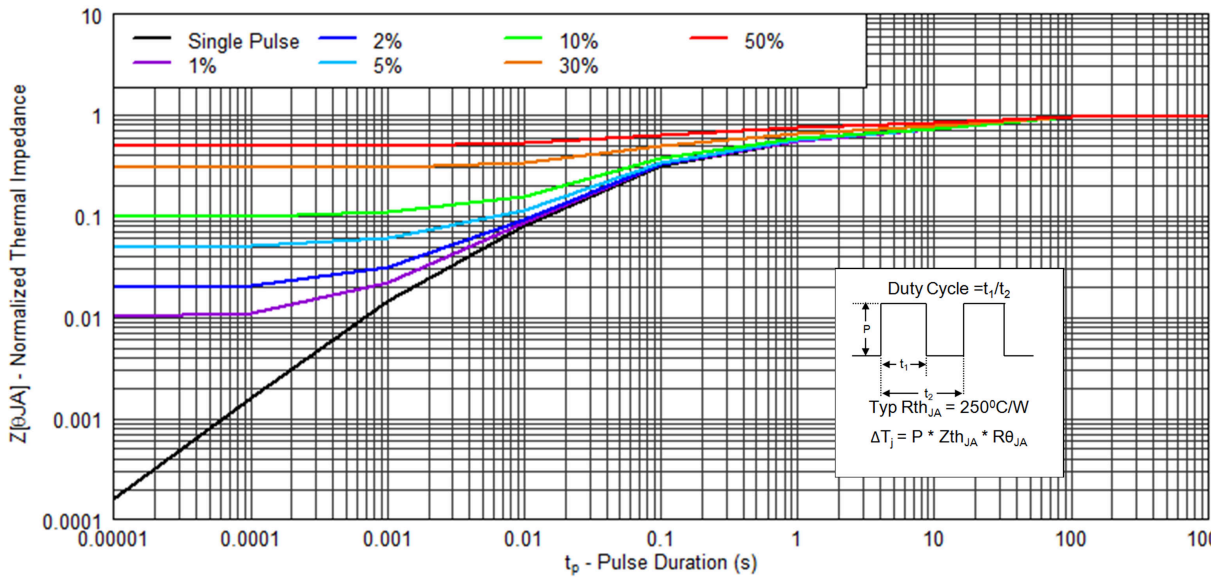



**図 5-1. Transient Thermal Impedance**

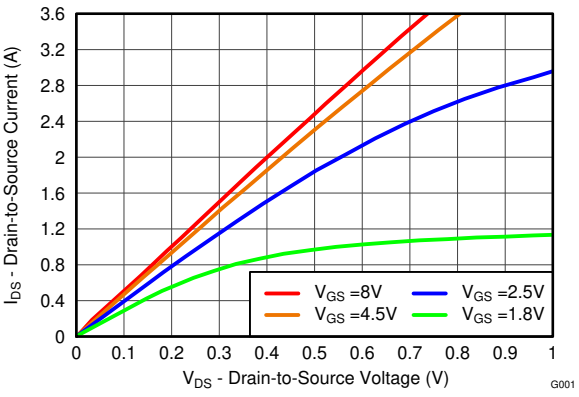



**図 5-2. Saturation Characteristics**

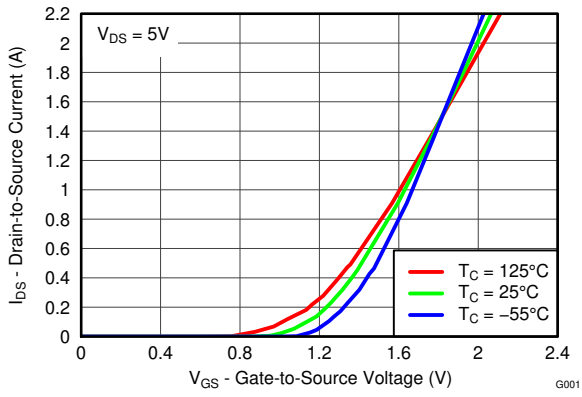



**図 5-3. Transfer Characteristics**

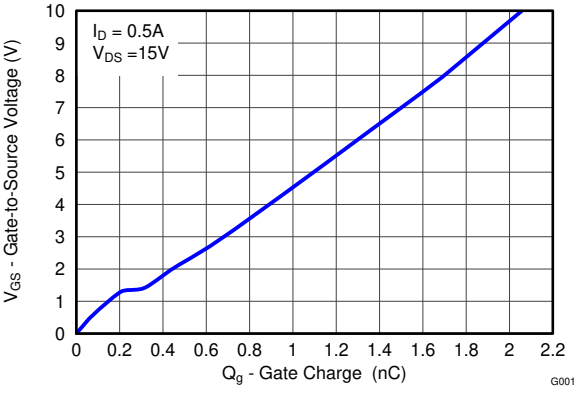



**図 5-4. Gate Charge**

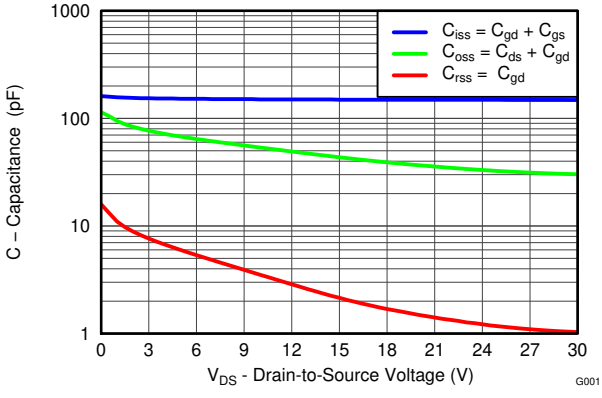



**図 5-5. Capacitance**

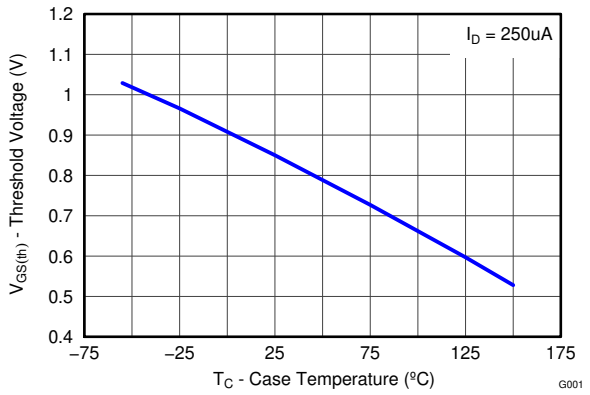



**図 5-6. Threshold Voltage vs Temperature**

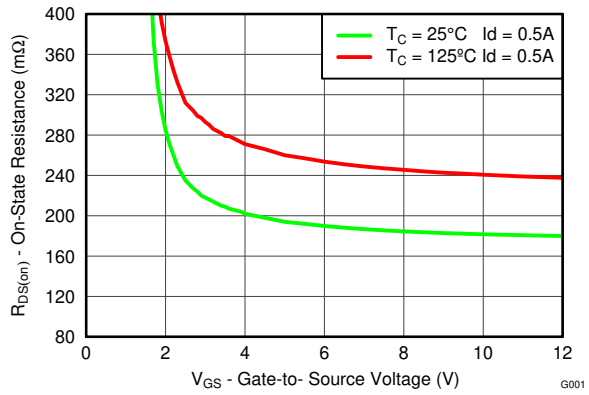



**図 5-7. On-State Resistance vs Gate-to-Source Voltage**

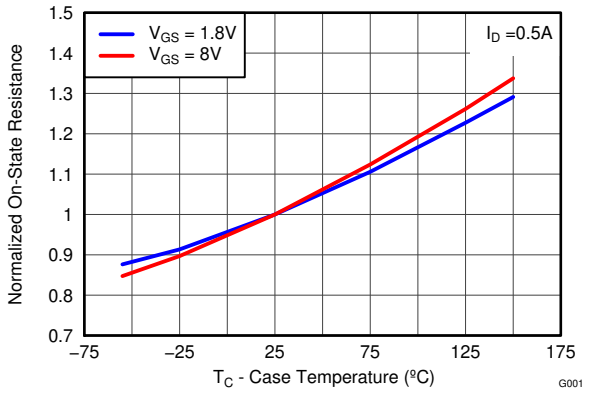



**図 5-8. Normalized On-State Resistance vs Temperature**

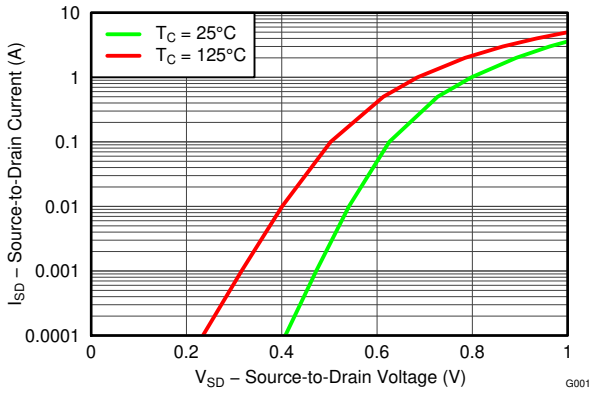



**図 5-9. Typical Diode Forward Voltage**

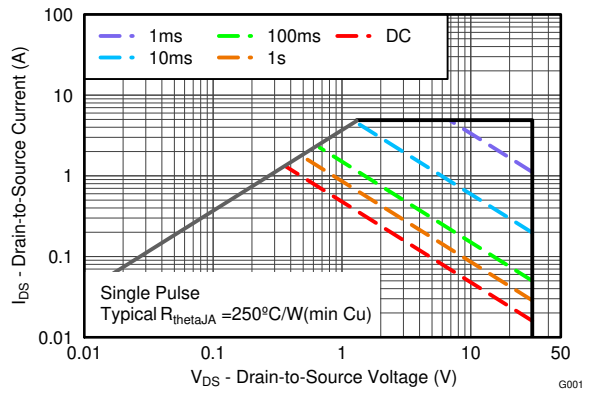



**図 5-10. Maximum Safe Operating Area**

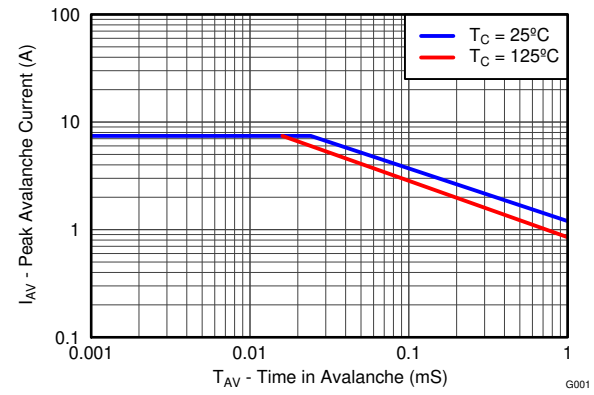



**図 5-11. Single Pulse Unclamped Inductive Switching**

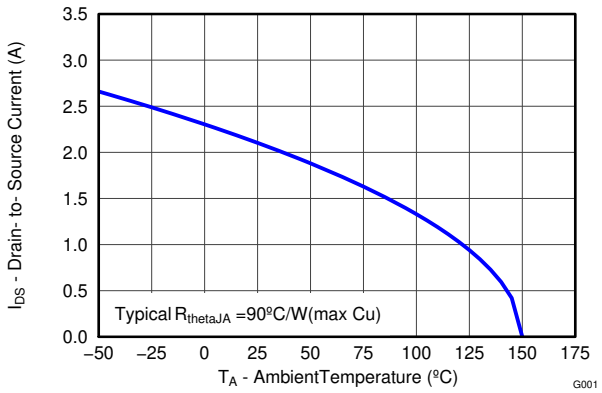



**図 5-12. Maximum Drain Current vs Temperature**

# 6 Device and Documentation Support

## 6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 6.2 Trademarks

FemtoFET™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

## 6.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

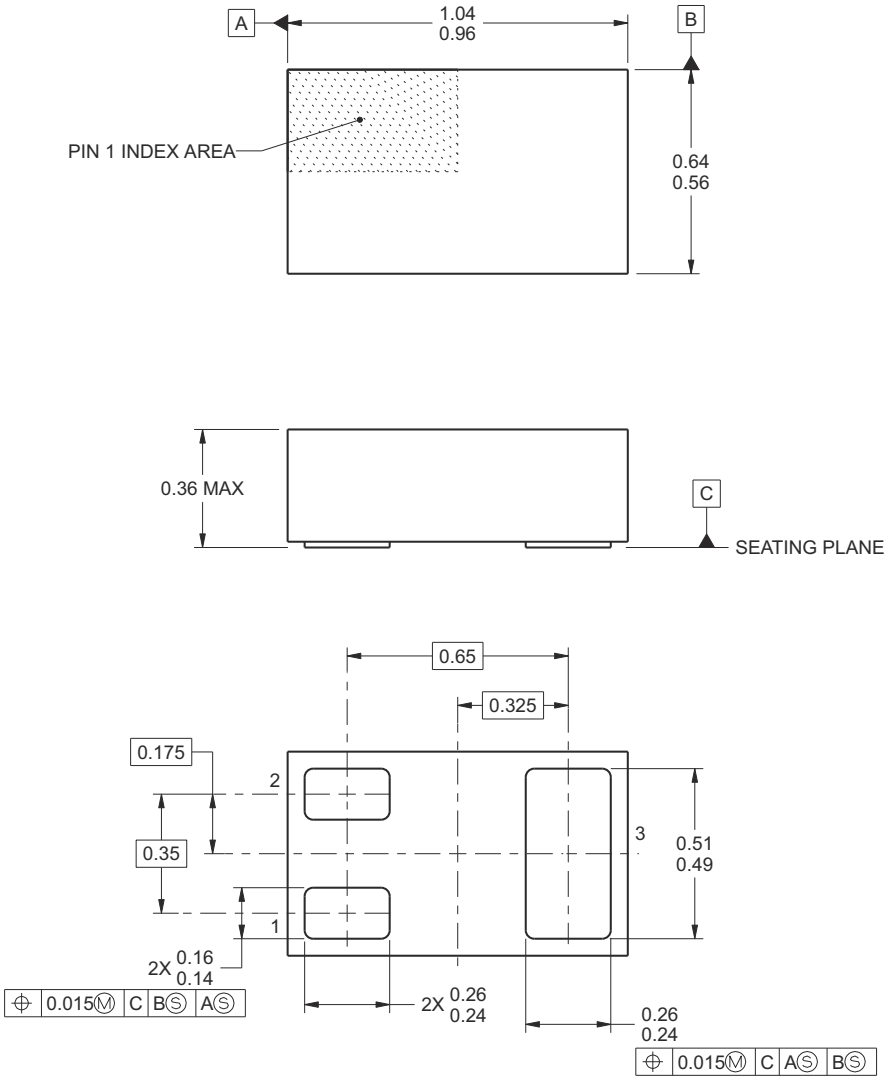
## 6.4 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## 7.1 Mechanical Dimensions

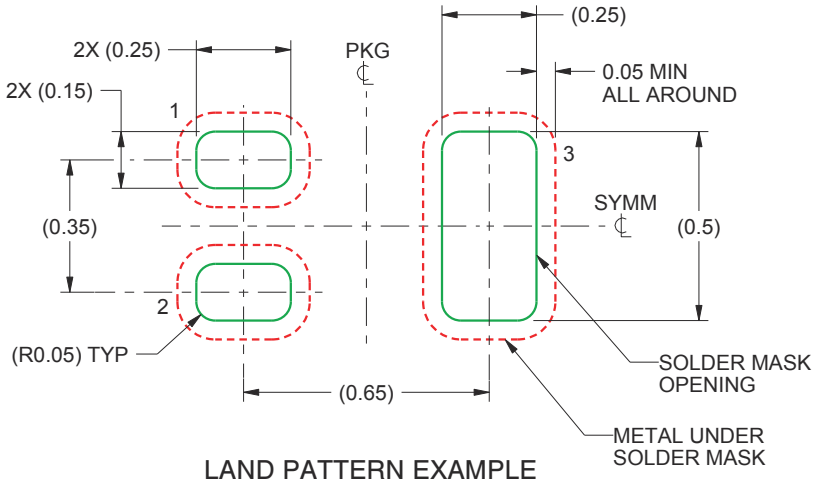



A. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

B. This drawing is subject to change without notice.

C. This package is a Pb-free bump design. Bump finish may vary. To determine the exact finish, refer to the device data sheet or contact a local TI representative.

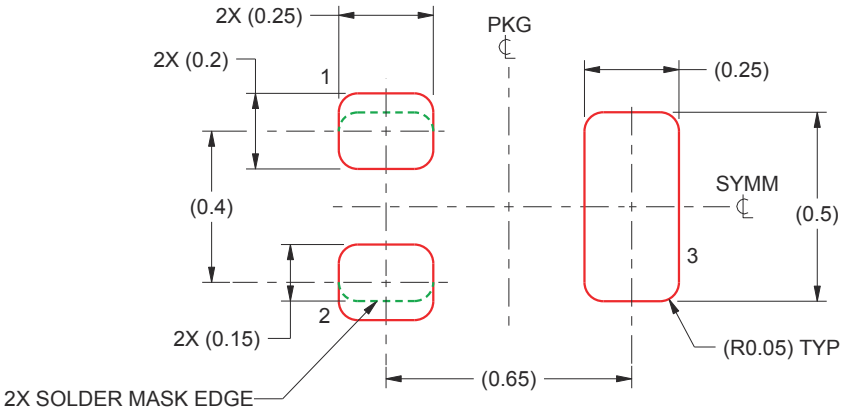
## 7.2 Recommended Minimum PCB Layout




LAND PATTERN EXAMPLE
SOLDER MASK DEFINED

A. All dimensions are in millimeters.
B. For more information, see *FemtoFET Surface Mount Guide* (SLRA003D).

## 7.3 Recommended Stencil Pattern




SOLDER PASTE EXAMPLE

A. All dimensions are in millimeters.
B. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CSD17483F4 | ACTIVE | PICOSTAR | YJC | 3 | 3000 | RoHS & Green | NIAU | Level-1-260C-UNLIM | -55 to 150 | DP | Samples |
| CSD17483F4T | ACTIVE | PICOSTAR | YJC | 3 | 250 | RoHS & Green | NIAU | Level-1-260C-UNLIM | -55 to 150 | DP | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

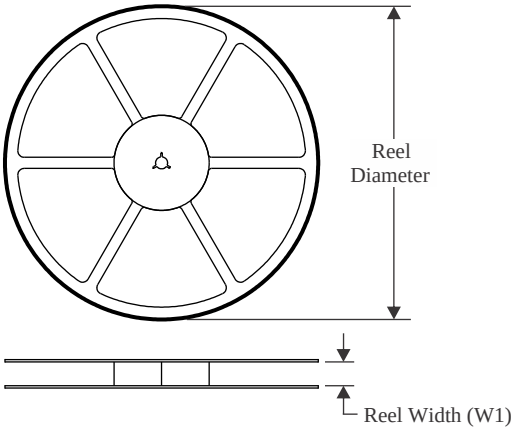
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

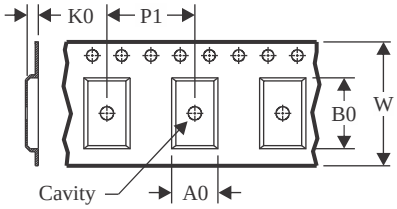
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

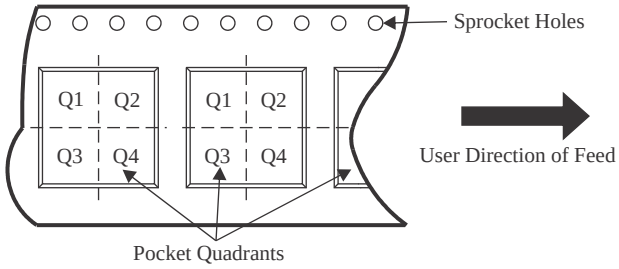



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

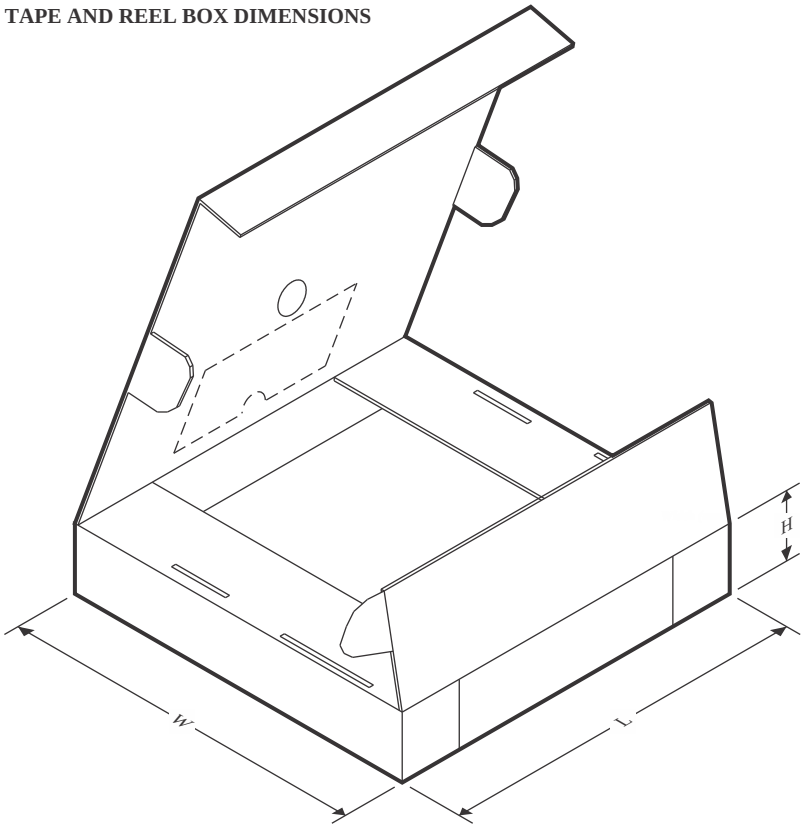
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CSD17483F4 | PICOSTAR | YJC | 3 | 3000 | 180.0 | 8.4 | 0.7 | 1.1 | 0.46 | 4.0 | 8.0 | Q2 |
| CSD17483F4T | PICOSTAR | YJC | 3 | 250 | 180.0 | 8.4 | 0.7 | 1.1 | 0.46 | 4.0 | 8.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

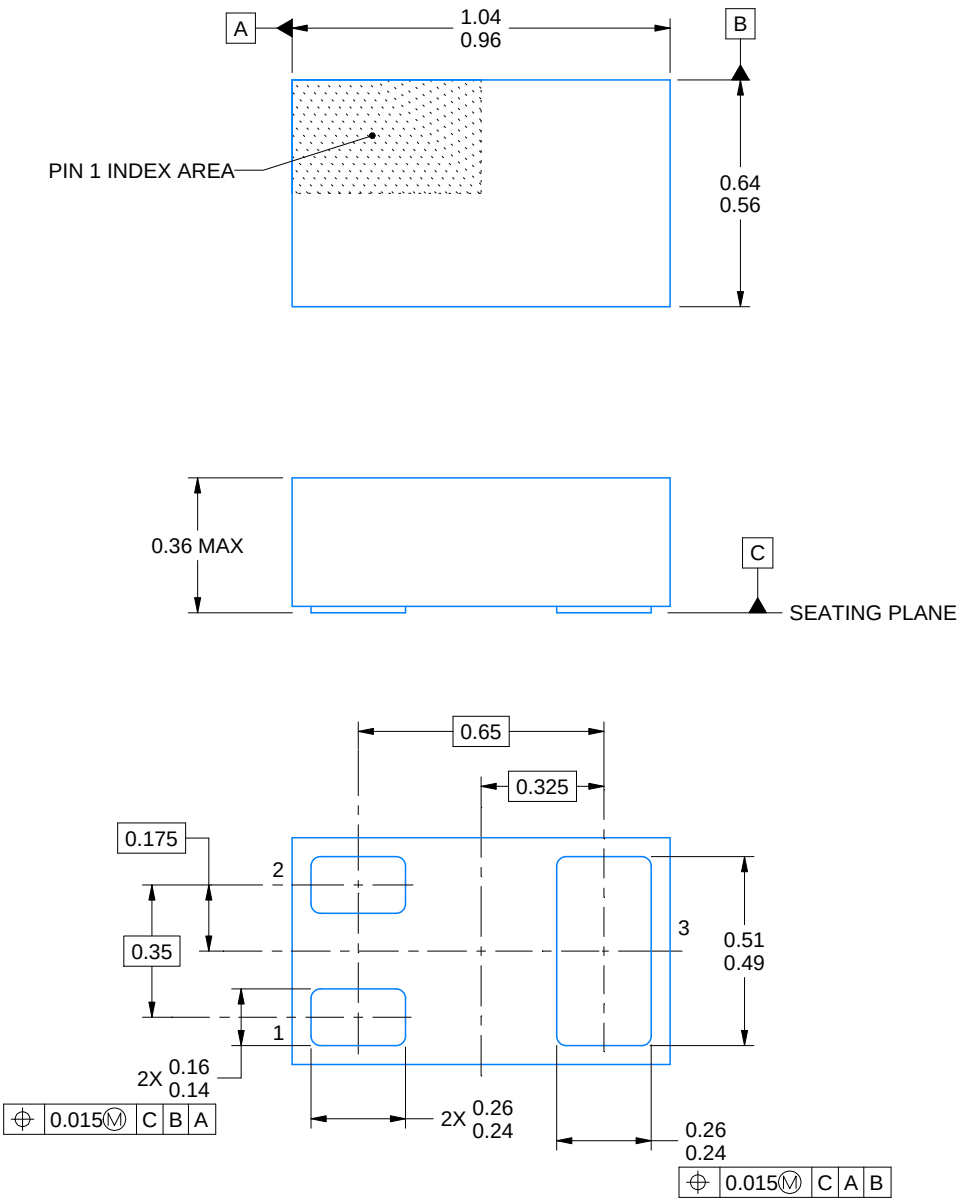
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CSD17483F4 | PICOSTAR | YJC | 3 | 3000 | 182.0 | 182.0 | 20.0 |
| CSD17483F4T | PICOSTAR | YJC | 3 | 250 | 182.0 | 182.0 | 20.0 |

# PACKAGE OUTLINE

## YJC0003A

## PicoStar™ - 0.36 mm max height

PicoStar™

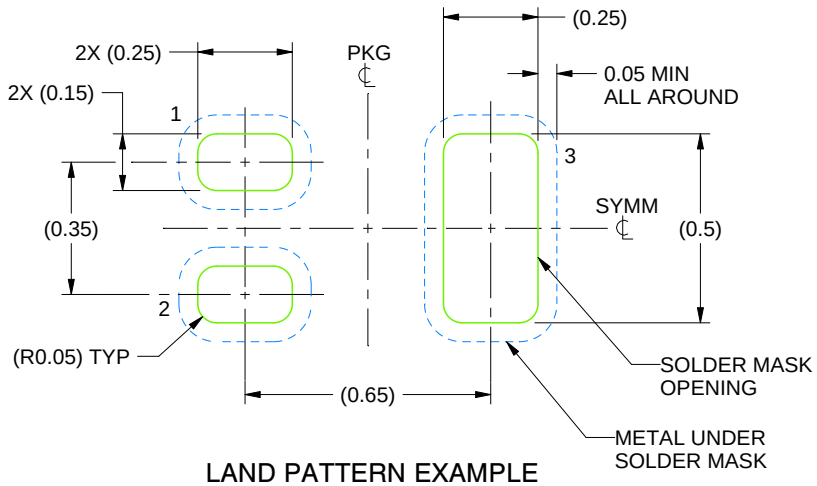



4220651/C 03/2022

PicoStar is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.
3. This package is a Pb-free bump design. Bump finish may vary. To determine the exact finish, refer to the device datasheet or contact a local TI representative.

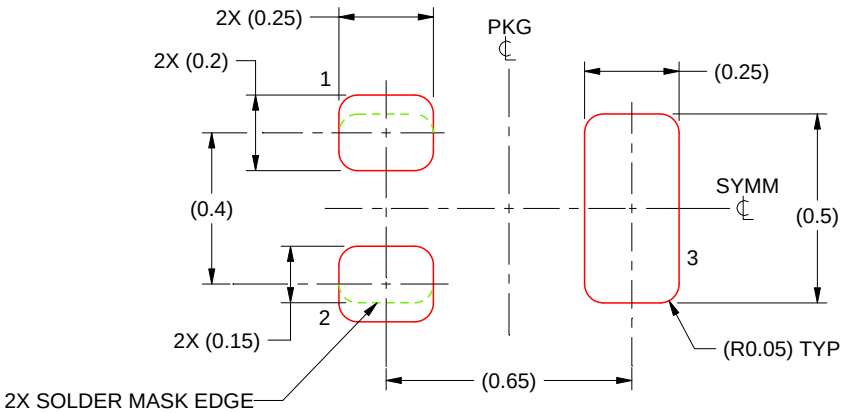



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:50X

4220651/C 03/2022

NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).




SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:50X

4220651/C 03/2022

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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