

CSD22205L -8V P チャネル NexFET™ パワー MOSFET

1 特長

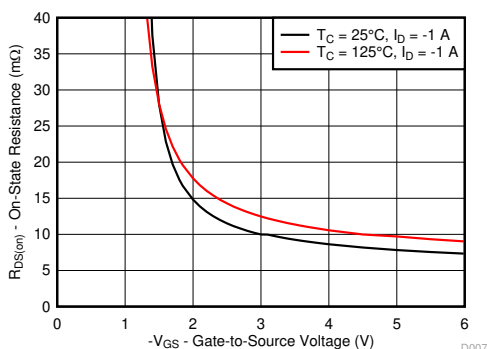
- 低い抵抗
- 1.2mm × 1.2mm の小さな占有面積
- 薄型、高さ 0.36mm
- 鉛不使用
- ゲート・ソース電圧クランプ
- ゲート ESD 保護
- RoHS に準拠
- ハロゲン不使用

2 アプリケーション

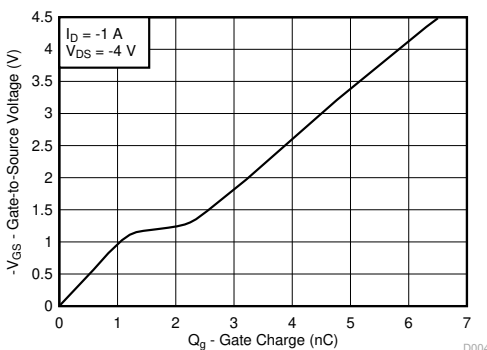
- バッテリ管理
- ロード・スイッチ
- バッテリ保護

3 概要

この -8V、8.2mΩ、1.2mm × 1.2mm LGA (Land Grid Array) の NexFET™ デバイスは、可能な限り小さな外形で、最低のオン抵抗とゲート電荷を実現し、非常に低いプロファイルで優れた熱特性を持つよう設計されています。ランド・グリッド・アレイ (LGA) パッケージはシリコン・チップ・スケール・パッケージで、ハンダ・ボールの代わりに金属のパッドを使用しています。



$R_{DS(on)}$ と V_{GS} との関係



$R_{DS(on)}$ と V_{GS} との関係

製品概要

$T_A = 25^\circ\text{C}$		値	単位
V_{DS}	ドレイン - ソース間電圧	-8	V
Q_g	ゲートの合計電荷 (-4.5V)	6.5	nC
Q_{gd}	ゲート電荷、ゲート - ドレイン間	1.0	nC
$R_{DS(on)}$	ドレイン - ソース間オン抵抗	$V_{GS} = -1.5\text{V}$	30
		$V_{GS} = -1.8\text{V}$	20
		$V_{GS} = -2.5\text{V}$	11.5
		$V_{GS} = -4.5\text{V}$	8.2
$V_{GS(th)}$	スレッシュホールド電圧	-0.7	V

製品情報(1)

デバイス	数量	メディア	パッケージ	出荷形態
CSD22205L	3000	7 インチ・リール	1.20mm × 1.20mm ランド・グリッド・アレイ パッケージ	テープ・アンド・リール
CSD22205LT	250			

- (1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。

絶対最大定格

$T_A = 25^\circ\text{C}$		値	単位
V_{DS}	ドレイン - ソース間電圧	-8	V
V_{GS}	ゲート - ソース間電圧	-6	V
I_D	連続ドレイン電流 ⁽¹⁾	-7.4	A
I_{DM}	パルス・ドレイン電流 ⁽²⁾	-71	A
P_D	消費電力 ⁽¹⁾	0.6	W
T_J , T_{stg}	動作時の接合部温度、 保存温度	-55~150	°C

- (1) 最小 Cu、 $R_{\theta JA} = 225^\circ\text{C/W}$
 (2) パルス幅 $\leq 100\mu\text{s}$ 、デューティ・サイクル $\leq 1\%$

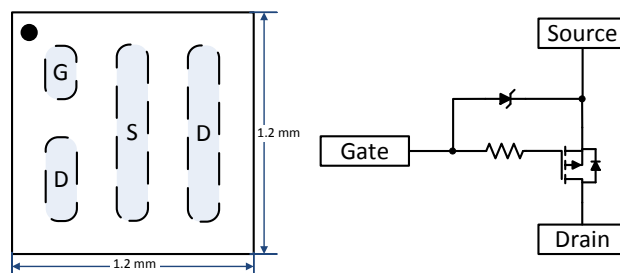


図 3-1. 上面図と回路の構成



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4 Revision History

Changes from Revision A (August 2017) to Revision B (February 2022)	Page
• 超薄型の簡条書き項目を、高さ 0.35mm から 0.36mm に変更。.....	1
• Changed CSD22205L Package Dimensions image height from 0.35 mm to 0.36 mm.....	8

Changes from Revision * (May 2017) to Revision A (August 2017)	Page
• Changed the units for timing parameters from μ s : to ns (nanoseconds) in the セクション 5.1 table.....	3

5 Specifications

5.1 Electrical Characteristics

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

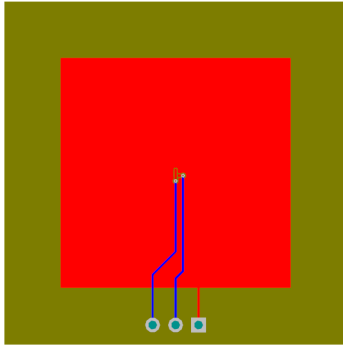
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
$B_{V_{DSS}}$	Drain-to-source voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-8			V
I_{DSS}	Drain-to-source leakage current	$V_{GS} = 0\text{ V}, V_{DS} = -6.4\text{ V}$			-100	nA
I_{GSS}	Gate-to-source leakage current	$V_{DS} = 0\text{ V}, V_{GS} = -6\text{ V}$			-100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-0.4	-0.7	-1.05	V
$R_{DS(on)}$	Drain-to-source on-resistance	$V_{GS} = -1.5\text{ V}, I_D = -0.2\text{ A}$		30		m Ω
		$V_{GS} = -1.8\text{ V}, I_D = -1\text{ A}$		20	40	
		$V_{GS} = -2.5\text{ V}, I_D = -1\text{ A}$		11.5	15.0	
		$V_{GS} = -4.5\text{ V}, I_D = -1\text{ A}$		8.2	9.9	
g_{fs}	Transconductance	$V_{DS} = -0.8\text{ V}, I_D = -1\text{ A}$		10.4		S
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input capacitance	$V_{GS} = 0\text{ V}, V_{DS} = -4\text{ V}, f = 1\text{ MHz}$		1070	1390	pF
C_{OSS}	Output capacitance			560	730	pF
C_{RSS}	Reverse transfer capacitance			190	250	pF
R_G	Series gate resistance			30		Ω
Q_g	Gate charge total (-4.5 V)	$V_{DS} = -4\text{ V}, I_D = -1\text{ A}$		6.5	8.5	nC
Q_{gd}	Gate charge gate-to-drain			1.0		nC
Q_{gs}	Gate charge gate-to-source			1.2		nC
$Q_{g(th)}$	Gate charge at V_{th}			0.7		nC
Q_{OSS}	Output charge	$V_{DS} = -4\text{ V}, V_{GS} = 0\text{ V}$		4.1		nC
$t_{d(on)}$	Turnon delay time	$V_{DS} = -4\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -1\text{ A}, R_G = 0\ \Omega$		30		ns
t_r	Rise time			14		ns
$t_{d(off)}$	Turnoff delay time			70		ns
t_f	Fall time			32		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	$I_S = -1\text{ A}, V_{GS} = 0\text{ V}$		-0.68	-1.0	V
Q_{rr}	Reverse recovery charge	$V_{DS} = -4\text{ V}, I_F = -1\text{ A}, di/dt = 200\text{ A}/\mu\text{s}$		16		nC
t_{rr}	Reverse recovery time			38		ns

5.2 Thermal Information

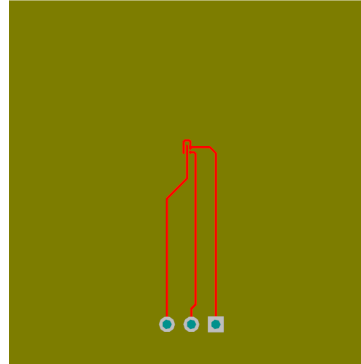
$T_A = 25^\circ\text{C}$ (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance ⁽²⁾		75		$^\circ\text{C}/\text{W}$
	Junction-to-ambient thermal resistance ⁽¹⁾		225		

- (1) Device mounted on FR4 material with minimum Cu mounting area.
- (2) Device mounted on FR4 material with 1-in² (6.45-cm²), 2-oz (0.071-mm) thick Cu.



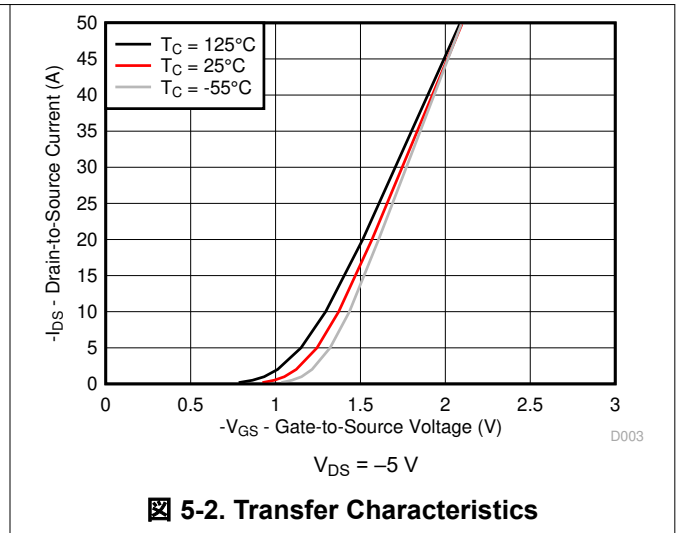
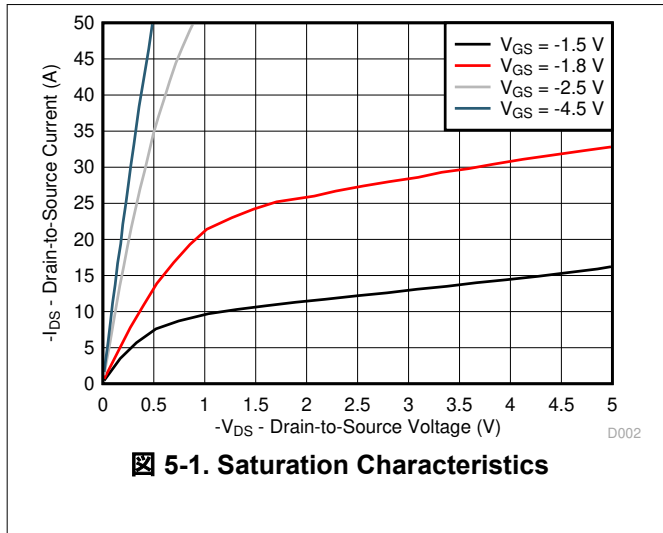
Typ $R_{\theta JA} = 75^\circ\text{C}/\text{W}$ when mounted on 1 in² of 2-oz Cu.

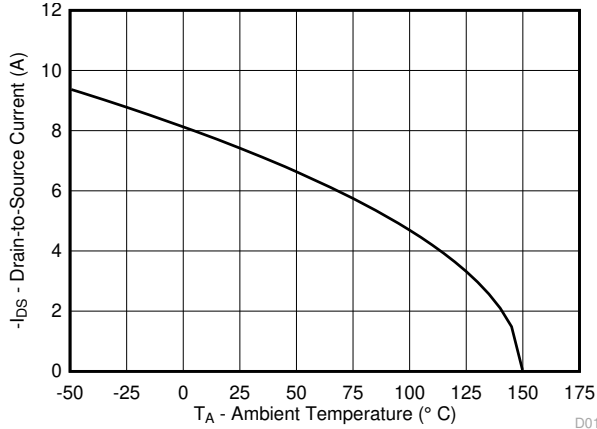


Typ $R_{\theta JA} = 225^\circ\text{C}/\text{W}$ when mounted on minimum pad area of 2-oz Cu.

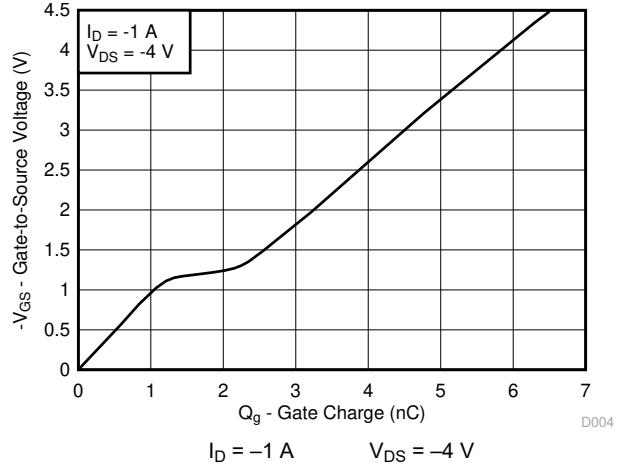
5.3 Typical MOSFET Characteristics

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

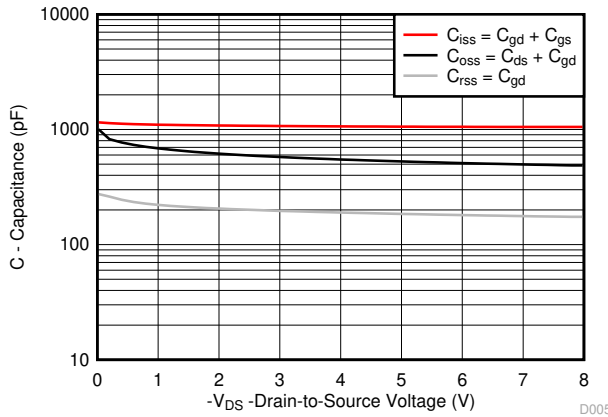




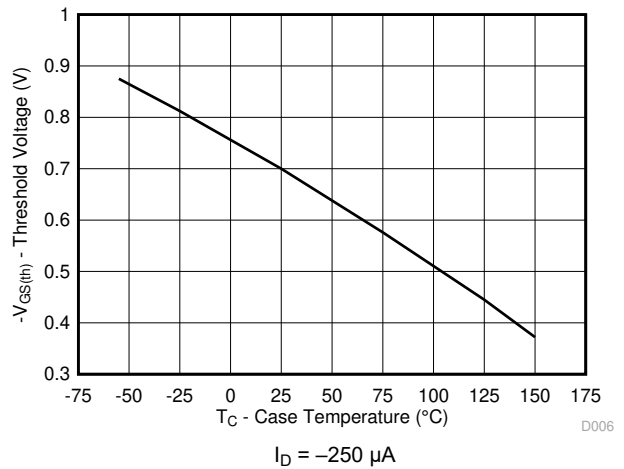
5-3. Maximum Drain Current vs Temperature



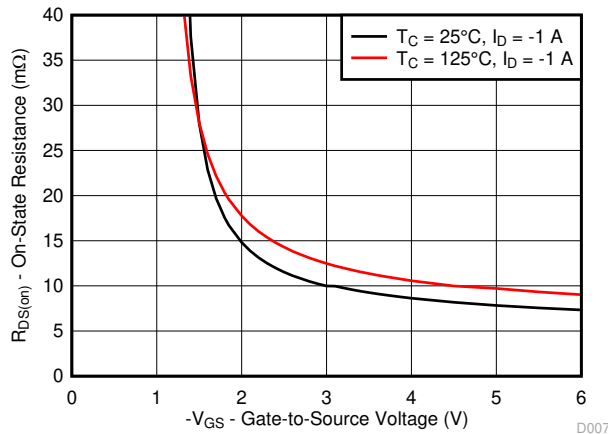
5-4. Gate Charge



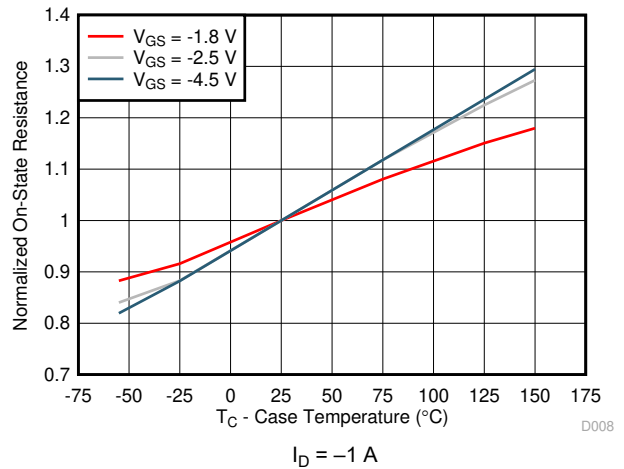
5-5. Capacitance



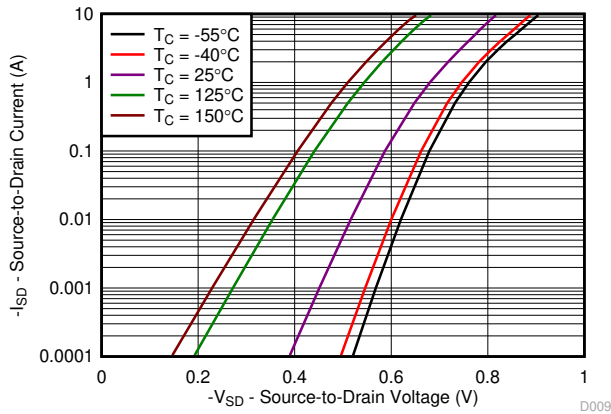
5-6. Threshold Voltage vs Temperature



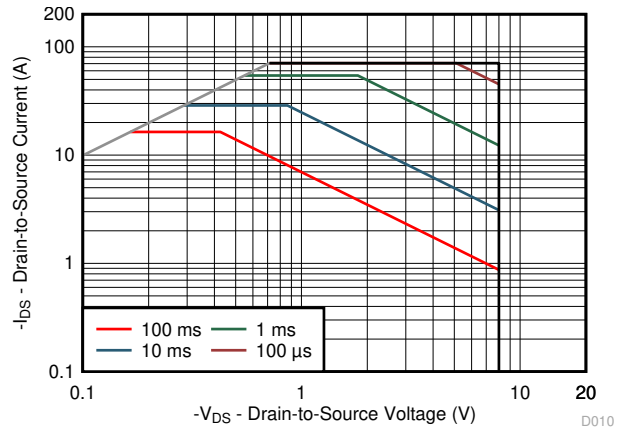
5-7. On-State Resistance vs Gate-to-Source Voltage



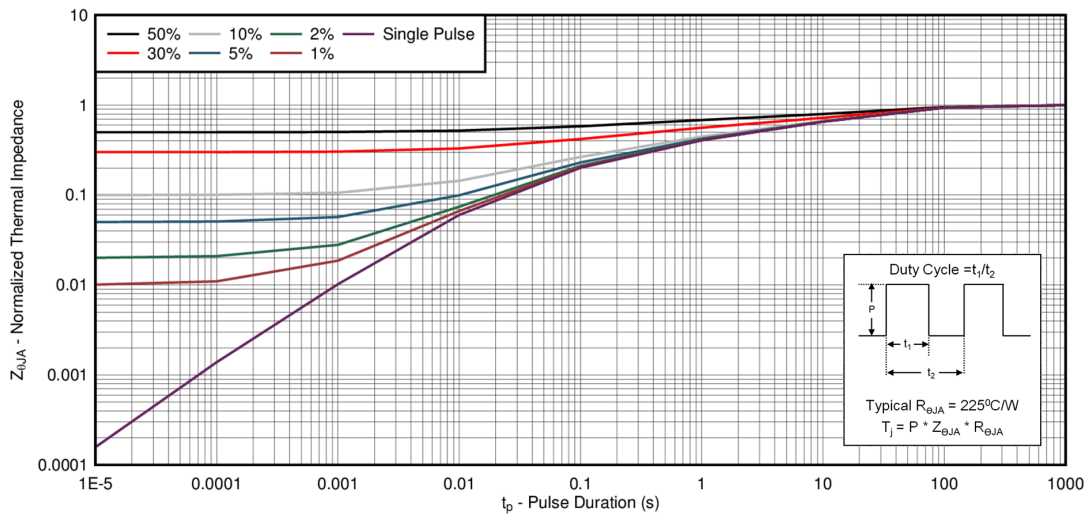
5-8. Normalized On-State Resistance vs Temperature



5-9. Typical Diode Forward Voltage



5-10. Maximum Safe Operating Area



5-11. Transient Thermal Impedance

6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Trademarks

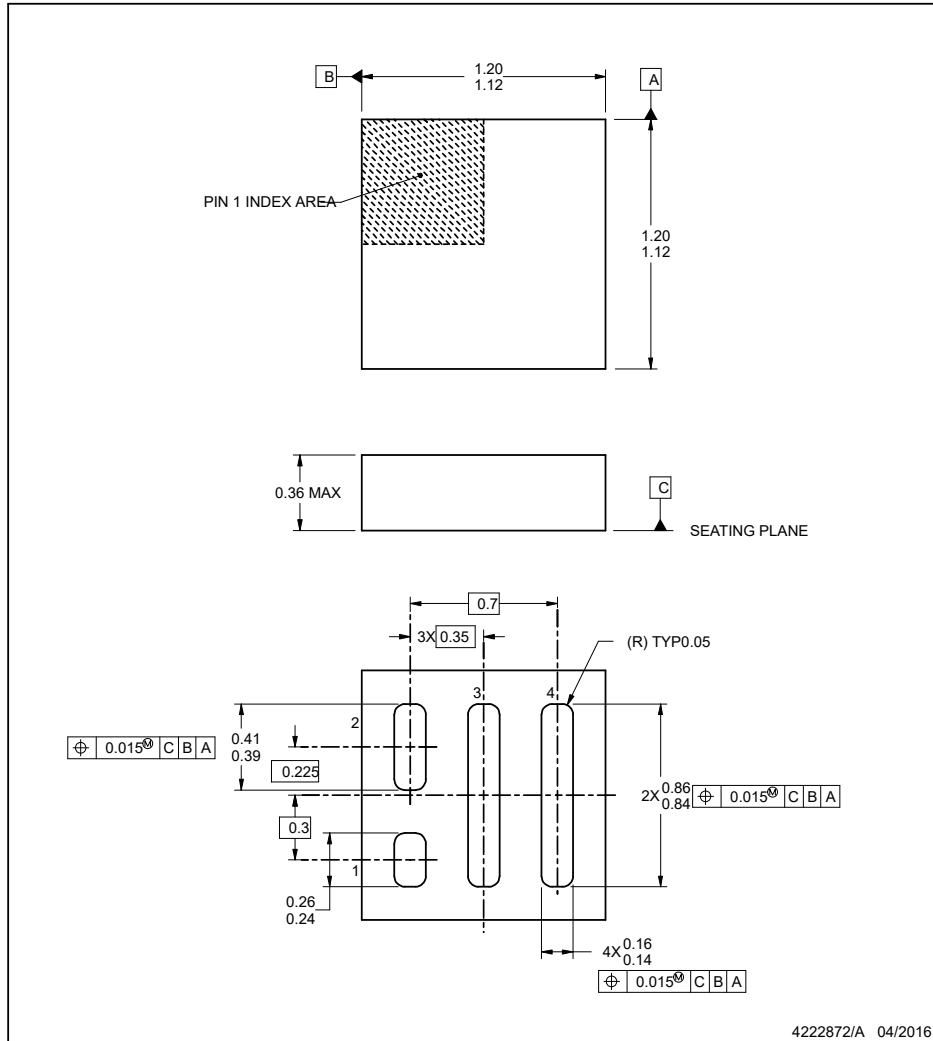
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7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 CSD22205L Package Dimensions

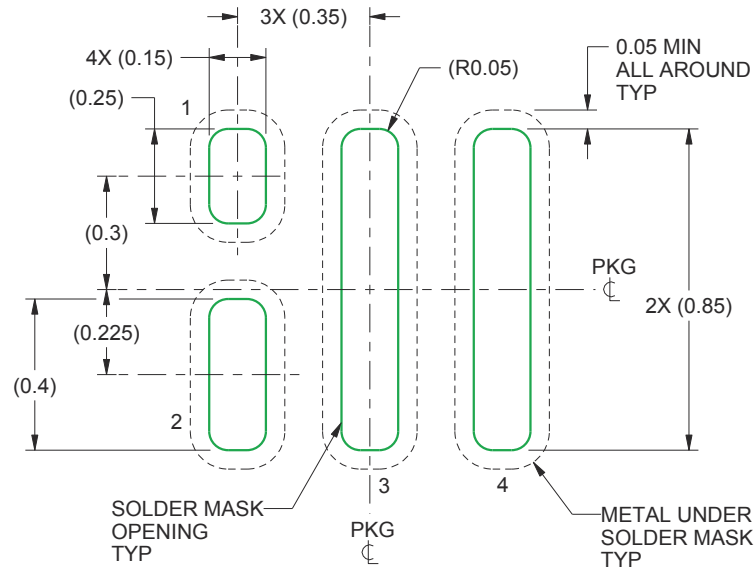


1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is a lead-free bump design. Bump finish may vary. To determine the exact finish, refer to the device data sheet or contact a local TI representative.

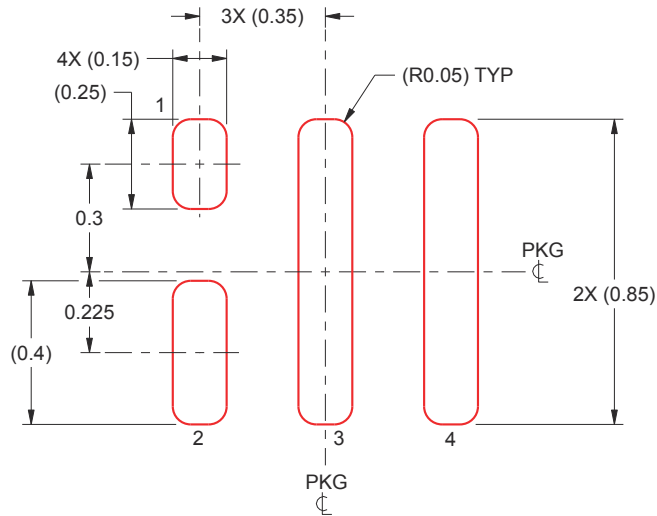
表 7-1. Pin Configuration Table

POSITION	DESIGNATION
1	Gate
2	Drain
3	Source
4	Drain

7.2 Land Pattern Recommendation



7.3 Stencil Recommendation



- A. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD22205L	ACTIVE	PICOSTAR	YMG	4	3000	RoHS & Green	NIAU	Level-1-260C-UNLIM	-55 to 150	205	Samples
CSD22205LT	ACTIVE	PICOSTAR	YMG	4	250	RoHS & Green	NIAU	Level-1-260C-UNLIM	-55 to 150	205	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD22205L	PICOSTAR	YMG	4	3000	180.0	8.4	1.26	1.26	0.42	4.0	8.0	Q1
CSD22205LT	PICOSTAR	YMG	4	250	180.0	8.4	1.26	1.26	0.42	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD22205L	PICOSTAR	YMG	4	3000	182.0	182.0	20.0
CSD22205LT	PICOSTAR	YMG	4	250	182.0	182.0	20.0

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