DAC5652A デュアル、10ビット、275MSPSのデジタル/アナログ・コンバータ

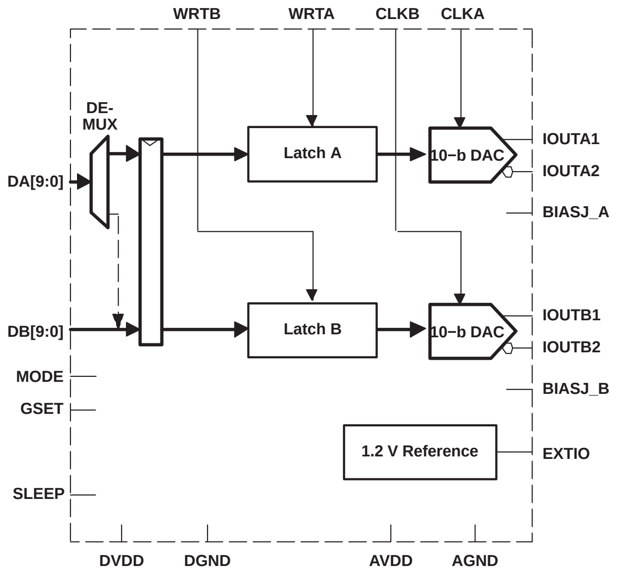
1 特長

- 10ビットのデュアル伝送DAC
- 更新速度: 275MSPS
- 単一電源: 3.0V～3.6V
- 高SFDR (スプリアス・フリー・ダイナミック・レンジ): 5MHz時80dBc
- 高IMD3 (3次相互変調歪): 15.1MHzおよび16.1MHz時78dBc
- 独立または単一抵抗によるゲイン制御
- デュアル・データまたはインターリーブ・データ
- 1.2Vのリファレンスを内蔵
- 低消費電力: 290mW
- パワーダウン・モード: 9mW
- パッケージ
  - 48ピンTQFP (Thin-Quad Flat Pack)
  - 48ピンVQFN (Very-Thin-Quad Flat Pack)

2 アプリケーション

- 携帯電話基地局通信チャネル
  - CDMA: W-CDMA、CDMA2000、IS-95
  - TDMA: GSM、IS-136、EDGE/UWC-136
- 医療/テスト用計測機器
- 任意波形発生器(ARB)
- ダイレクト・デジタル・シンセシス(DDS)
- ケーブル・モデム終端システム(CMTS)

機能ブロック図



3 概要

DAC5652Aは、オンチップの電圧リファレンスを内蔵したモノリシック、デュアル・チャネルの10ビット高速デジタル/アナログ・コンバータ(DAC)です。

最高275MSPSの更新速度で動作し、抜群の動的性能、正確なゲイン、オフセット整合といった特性から、I/Qベースバンドまたは直接IF通信アプリケーションに最適です。

各DACには、シングルエンドまたは差動アナログ出力構成に適した高インピーダンスの差動電流出力が備えられています。外部抵抗を使用して、各DACのフルスケール出力電流を別々に、または同時にスケーリングできます(一般的には2mA～20mA)。高精度の内蔵電圧リファレンスは温度補償機能を備え、安定した1.2Vのリファレンス電圧を提供します。外部リファレンスも使用できます。

DAC5652Aには、クロックとデータ・ラッチが異なる10ビットのパラレル入力ポートが2つあります。柔軟性を高めるため、インターリーブ・モードで動作する際には1ポートで各DACへの多重化データもサポートされます。

DAC5652Aは、50Ωの二重終端負荷を接続した変圧器結合の差動出力用に設計されています。20mAのフルスケール出力電流の場合、インピーダンス比4:1 (結果として出力4dBm)とインピーダンス比1:1の変圧器(出力-2dBm)の両方がサポートされています。

DAC5652Aは、48ピンTQFPおよび48ピンVQFNパッケージで供給されます。TQFPパッケージはファミリのメンバ間でピン互換性があり、10ビット(DAC5652A)、12ビット(DAC5662)、14ビット(DAC5672)の分解能を選択できます。また、TQFPパッケージはDAC2900およびAD9763デュアルDACともピン互換です。このデバイスは、-40℃～+85℃の工業用温度範囲で動作が規定されています。

製品情報[1]

型番	パッケージ	本体サイズ(公称)
DAC5652A	TQFP (48)	7mm×7mm
	VQFN (48)	6mm×6mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。

目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision E (May 2018) から Revision F に変更 **Page**

- 「*概要*」セクションのテキストにVQFNパッケージを 追加 1
- 「*概要*」セクションのテキストを、TQFPパッケージのみがピン互換であることを明確にするよう 変更 1

Revision D (August 2012) から Revision E に変更 **Page**

- 既存のコンテンツを新しいセクションに移動、「*製品情報*」表、「*ESD定格*」表、「*推奨動作条件*」表、および「*詳細説明*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを 追加 1
- 新しいVQFN-48パッケージと関連コンテンツを 追加 1

Revision C (June 2011) から Revision D に変更 **Page**

- Deleted the V_{IH} MAX value of 3.3 V 9
- Deleted the V_{IL} MIN value of 0 V 9

Revision B (December 2010) から Revision C に変更 **Page**

- Added *Thermal Information* table 6

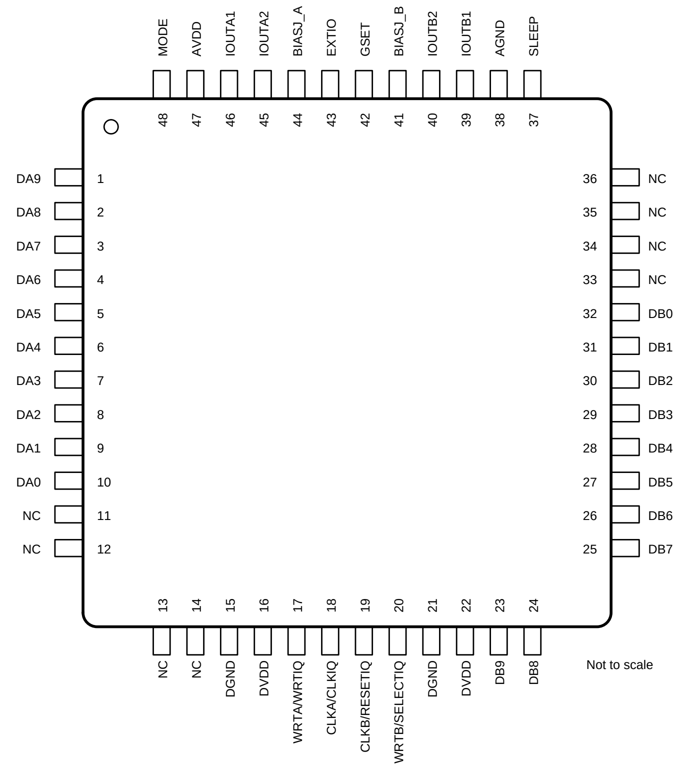
Revision A (May 2009) から Revision B に変更 **Page**

- Changed the non-printing µ symbols in the *Digital Input* section of the *Electrical Characteristics* table (units column) to the correct µ symbols recognized by the PDF processor 9

2007年9月発行のものから更新	**Page**
• Added internal pulldown to DA and DB pin descriptions	5
• Added GSET to *Absolute Maximum Ratings* table	6
• Added "The pullup and pulldown circuitry is approximately equivalent to 100 kΩ" to *Digital Inputs* section	13
• Added resistor values to Figure 13	13
• Added resistor values to Figure 14	13

5 Pin Configuration and Functions

**PFB Package
48-Pin TQFP
Top View**



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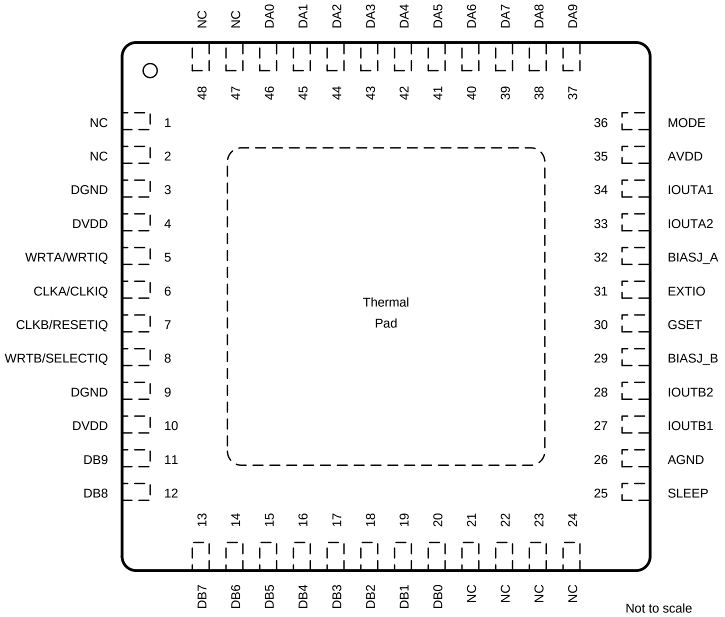
**RSL Package
48-Pin VQFN
Top View**



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Pin Functions

PIN			I/O	DESCRIPTION
NAME	TQFP	VQFN		
AGND	38	26	I	Analog ground
AVDD	47	35	I	Analog supply voltage
BIASJ_A	44	32	O	Full-scale output current bias for DACA
BIASJ_B	41	29	O	Full-scale output current bias for DACB
CLKA/CLKIQ	18	6	I	Clock input for DACA, CLKIQ in interleaved mode
CLKB/RESETIQ	19	7	I	Clock input for DACB, RESETIQ in interleaved mode
DA0	10	46	I	Data port A0 (LSB). Internal pulldown.
DA1	9	45	I	Data port A1. Internal pulldown.
DA2	8	44	I	Data port A2. Internal pulldown.
DA3	7	43	I	Data port A3. Internal pulldown.
DA4	6	42	I	Data port A4. Internal pulldown.
DA5	5	41	I	Data port A5. Internal pulldown.
DA6	4	40	I	Data port A6. Internal pulldown.
DA7	3	39	I	Data port A7. Internal pulldown.
DA8	2	38	I	Data port A8. Internal pulldown.
DA9	1	37	i	Data port A9 (MSB). Internal pulldown.
DB0	32	20	I	Data port B0 (LSB). Internal pulldown.
DB1	31	19	I	Data port B1. Internal pulldown.
DB2	30	18	I	Data port B2. Internal pulldown.
DB3	29	17	I	Data port B3. Internal pulldown.
DB4	28	16	I	Data port B4. Internal pulldown.
DB5	27	15	I	Data port B5. Internal pulldown.
DB6	26	14	I	Data port B6. Internal pulldown.
DB7	25	13	I	Data port B7. Internal pulldown.
DB8	24	12	I	Data port B8. Internal pulldown.
DB9	23	11	I	Data port B9 (MSB). Internal pulldown.
DGND	15, 21	3, 9	I	Digital ground
DVDD	16, 22	4, 10	I	Digital supply voltage
EXTIO	43	31	I/O	Internal reference output (bypass with 0.1 μF to AGND) or external reference input
GSET	42	30	I	Gain-setting mode: H – 1 resistor, L – 2 resistors. Internal pullup.
IOUTA1	46	34	O	DACA current output. Full-scale with all bits of DA high.
IOUTA2	45	33	O	DACA complementary current output. Full-scale with all bits of DA low.
IOUTB1	39	27	O	DACB current output. Full-scale with all bits of DB high.
IOUTB2	40	28	O	DACB complementary current output. Full-scale with all bits of DB low.
MODE	48	36	I	Mode Select: H – Dual Bus, L – Interleaved. Internal pullup.
NC	11-14, 33-36	1,2, 21-24, 47, 48	—	Factory use only. Pins must be connected to DGND or left unconnected.
SLEEP	37	25	I	Sleep function control input: H – DAC in power-down mode, L – DAC in operating mode. Internal pulldown.
WRTA/WRTIQ	17	5	I	Input write signal for PORT A (WRTIQ in interleaving mode)
WRTB/SELECTIQ	20	8	I	Input write signal for PORT B (SELECTIQ in interleaving mode)

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	AVDD (measured with respect to AGND)	–0.5	4	V
	DVDD (measured with respect to DGND)	–0.5	4	
	Between AGND and DGND	–0.5	0.5	
	Between AVDD and DVDD	–4	4	
	DA[9:0] and DB[9:0]	–0.5	DVDD + 0.5	
	MODE, SLEEP, CLKA, CLKB, WRTA, WRTB	–0.5	DVDD + 0.5	
	IOUTA1, IOUTA2, IOUTB1, IOUTB2	–1	AVDD + 0.5	
	EXTIO, BIASJ_A, BIASJ_B, GSET	–0.5	AVDD + 0.5	
Current	Peak input current (any input)		20	mA
	Peak total input current (all inputs)		–30	
Temperature	Operating free-air, T_A	–40	85	°C
	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
AVDD	Analog supply voltage	3	3.3	3.6	V
DVDD	Digital supply voltage	3	3.3	3.6	V
	Output voltage compliance range(1)	–1		1.25	V
	Clock input frequency			275	MHz
T_A	Operating free-air temperature	–40		85	°C

(1) The lower limit of the output compliance is determined by the CMOS process. Exceeding this limit may result in transistor breakdown, resulting in reduced reliability of the DAC5652A device. The upper limit of the output compliance is determined by the load resistors and full-scale output current. Exceeding the upper limit adversely affects distortion performance and integral nonlinearity.

6.4 Thermal Information

THERMAL METRIC(1)		DAC5652A		UNIT
		PFB (TQFP)	RSL (VQFN)	
		48 PINS	48 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	65.3	27.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	16.4	17.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	28.6	9.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	28.4	9.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	2.2	°C/W

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics: DC

dc specifications over T_A, AVDD = DVDD = 3.3 V, $I_{(OUTFS)}$ = 20 mA, and independent gain set mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RESOLUTION						
	Resolution		10			Bits
DC ACCURACY(1)						
INL	Integral nonlinearity	1 LSB = $I_{(OUTFS)}/2^{10}$, T_{MIN} to T_{MAX}	–1	±0.25	1	LSB
DNL	Differential nonlinearity		–0.5	±0.16	0.5	LSB
ANALOG OUTPUT						
	Offset error	Midscale value (internal reference)		±0.05		%FSR
	Offset mismatch	Midscale value (internal reference)		±0.03		%FSR
	Gain error	With internal reference		±0.75		%FSR
	Minimum full-scale output current(2)			2		mA
	Maximum full-scale output current(2)			20		mA
	Gain mismatch	With internal reference	–2	0.2	2	%FSR
	Output voltage compliance range(3)		–1		1.25	V
R_O	Output resistance			300		kΩ
C_O	Output capacitance			5		pF
REFERENCE OUTPUT						
	Reference voltage		1.14	1.2	1.26	V
	Reference output current(4)			100		nA
REFERENCE INPUT						
$V_{(EXTIO)}$	Input voltage		0.1		1.25	V
R_I	Input resistance			1		MΩ
	Small signal bandwidth			300		kHz
C_I	Input capacitance			100		pF
TEMPERATURE COEFFICIENTS						
	Offset drift			2		ppm of FSR/°C
	Gain drift	With external reference		±20		ppm of FSR/°C
		With internal reference		±40		
	Reference voltage drift			±20		ppm/°C

(1) Measured differentially through 50 Ω to AGND.
(2) Nominal full-scale current, $I_{(OUTFS)}$, equals 32x the $I_{(BIAS)}$ current.
(3) The lower limit of the output compliance is determined by the CMOS process. Exceeding this limit may result in transistor breakdown, resulting in reduced reliability of the DAC5652A device. The upper limit of the output compliance is determined by the load resistors and full-scale output current. Exceeding the upper limit adversely affects distortion performance and integral nonlinearity.
(4) Use an external buffer amplifier with high-impedance input to drive any external load.

6.6 Electrical Characteristics: AC

ac specifications over T_A, AVDD = DVDD = 3.3 V, $I_{(OUTFS)}$ = 20 mA, independent gain set mode, differential 1:1 impedance ratio transformer coupled output, and 50-Ω doubly terminated load (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG OUTPUT						
f_{clk}	Maximum output update rate(1)		275			MSPS
t_s	Output settling time to 0.1% (DAC)	Midscale transition		20		ns
t_r	Output rise time 10% to 90% (OUT)			1.4		ns
t_f	Output fall time 90% to 10% (OUT)			1.5		ns
	Output noise	$I_{(OUTFS)}$ = 20 mA		55		pA/√Hz
		$I_{(OUTFS)}$ = 2 mA		30		
AC LINEARITY						
SFDR	Spurious-free dynamic range	1st Nyquist zone, T_A = 25°C, f_{DATA} = 50 MSPS, f_{OUT} = 1 MHz, $I_{(OUTFS)}$ = 0 dB		79		dBc
		1st Nyquist zone, T_A = 25°C, f_{DATA} = 50 MSPS, f_{OUT} = 1 MHz, $I_{(OUTFS)}$ = –6 dB		78		
		1st Nyquist zone, T_A = 25°C, f_{DATA} = 50 MSPS, f_{OUT} = 1 MHz, $I_{(OUTFS)}$ = –12 dB		73		
		1st Nyquist zone, T_A = 25°C, f_{DATA} = 100 MSPS, f_{OUT} = 5 MHz, $I_{(OUTFS)}$ = 0 dB		80		
		1st Nyquist zone, T_A = 25°C, f_{DATA} = 100 MSPS, f_{OUT} = 20 MHz, $I_{(OUTFS)}$ = 0 dB		76		
		1st Nyquist zone, T_{MIN} to T_{MAX}, f_{DATA} = 200 MSPS, f_{OUT} = 20 MHz, $I_{(OUTFS)}$ = 0 dB	61	70		
		1st Nyquist zone, T_A = 25°C, f_{DATA} = 200 MSPS, f_{OUT} = 41 MHz, $I_{(OUTFS)}$ = 0 dB		67		
		1st Nyquist zone, T_A = 25°C, f_{DATA} = 275 MSPS, f_{OUT} = 20 MHz		70		
SNR	Signal-to-noise ratio	1st Nyquist zone, T_A = 25°C, f_{DATA} = 100 MSPS, f_{OUT} = 5 MHz, $I_{(OUTFS)}$ = 0 dB		63		dB
		1st Nyquist zone, T_A = 25°C, f_{DATA} = 160 MSPS, f_{OUT} = 20 MHz, $I_{(OUTFS)}$ = 0 dB		62		dB
IMD3	Third-order two-tone intermodulation	Each tone at –6 dBFS, T_A = 25°C, f_{DATA} = 200 MSPS, f_{OUT} = 45.4 MHz and 46.4 MHz		61		dBc
		Each tone at –6 dBFS, T_A = 25°C, f_{DATA} = 100 MSPS, f_{OUT} = 15.1 MHz and 16.1 MHz		78		
IMD	Four-tone intermodulation	Each tone at –12 dBFS, T_A = 25°C f_{DATA} = 100 MSPS, f_{OUT} = 15.6, 15.8, 16.2, and 16.4 MHz		76		dBc
		Each tone at –12 dBFS, T_A = 25°C f_{DATA} = 165 MSPS, f_{OUT} = 19.0, 19.1, 19.3, and 19.4 MHz		55		
		Each tone at –12 dBFS, T_A = 25°C f_{DATA} = 165 MSPS, f_{OUT} = 68.8, 69.6, 71.2, and 72.0 MHz		70		
	Channel isolation	T_A = 25°C, f_{DATA} = 165 MSPS f_{OUT} (CH1) = 20 MHz, f_{OUT} (CH2) = 21 MHz		90		dBc

(1) Specified by design and bench characterization. Not production tested.

6.7 Electrical Characteristics: Digital Input

digital specifications over T_A, AVDD = DVDD = 3.3 V, and $I_{(OUTFS)}$ = 20 mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{IH}	High-level input current			±50		µA
I_{IL}	Low-level input current			±10		µA
$I_{IH(GSET)}$	High-level input current, GSET pin			7		µA
$I_{IL(GSET)}$	Low-level input current, GSET pin			–80		µA
$I_{IH(MODE)}$	High-level input current, MODE pin			–30		µA
$I_{IL(MODE)}$	Low-level input current, MODE pin			–80		µA
C_I	Input capacitance			5		pF

6.8 Electrical Characteristics: Power Supply

power supply specifications over T_A, AVDD = DVDD = 3.3 V, $I_{(OUTFS)}$ = 20 mA, f_{DATA} = 200 MSPS, f_{OUT} = 1 MHz, and independent gain set mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(AVDD)}$	Supply current, analog	Including output current through load resistor		75	90	mA
		Sleep mode with clock		2.5		
		Sleep mode without clock		2.5		
$I_{(DVDD)}$	Supply current, digital			12	20	mA
		Sleep mode with clock		11.3	18	
		Sleep mode without clock		0.6		
	Power dissipation			290	360	mW
		Sleep mode with clock		45.5		
		Sleep mode without clock		9.2		
		f_{DATA} = 275 MSPS, f_{OUT} = 20 MHz		310		
APSRR	Analog power supply rejection ratio		–0.2	–0.01	0.2	%FSR/V
DPSRR	Digital power supply rejection ratio		–0.2	0	0.2	%FSR/V

6.9 Switching Characteristics

digital specifications over T_A, AVDD = DVDD = 3.3 V, and $I_{(OUTFS)}$ = 20 mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TIMING - DUAL BUS MODE						
t_{su}	Input setup time		1			ns
t_h	Input hold time		1			ns
t_{LPH}	Input clock pulse high time			1		ns
t_{LAT}	Clock latency (WRTA/B to outputs)		4		4	clk
t_{PD}	Propagation delay time			1.5		ns
TIMING - SINGLE BUS INTERLEAVED MODE						
t_{su}	Input setup time			0.5		ns
t_h	Input hold time			0.5		ns
t_{LAT}	Clock latency (WRTA/B to outputs)		4		4	clk
t_{PD}	Propagation delay time			1.5		ns

6.10 Typical Characteristics

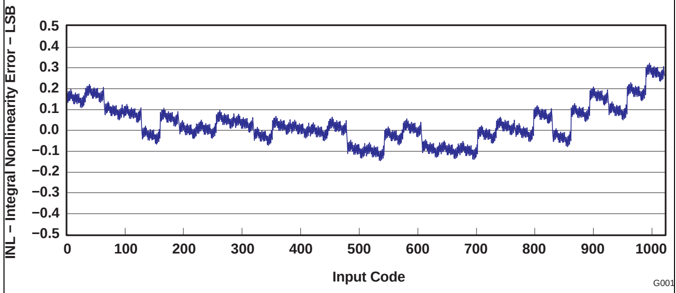


Figure 1. Integral Nonlinearity vs Input Code

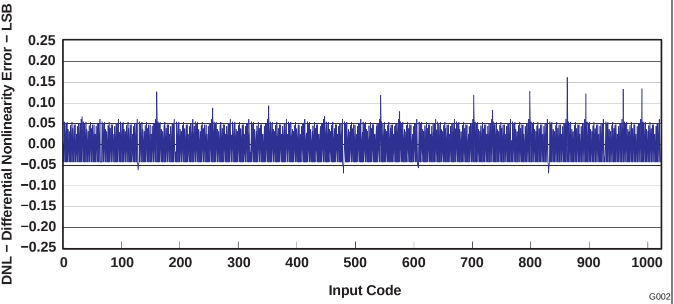


Figure 2. Differential Nonlinearity vs Input Code

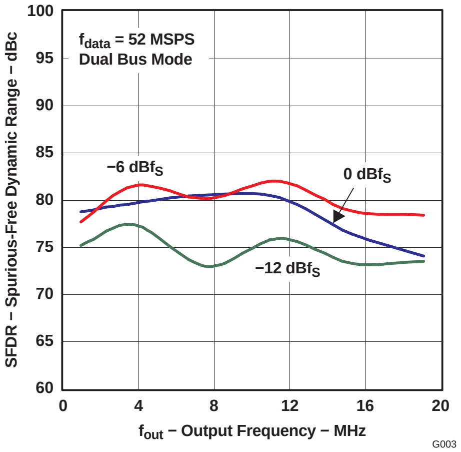


Figure 3. Spurious-Free Dynamic Range vs Output Frequency

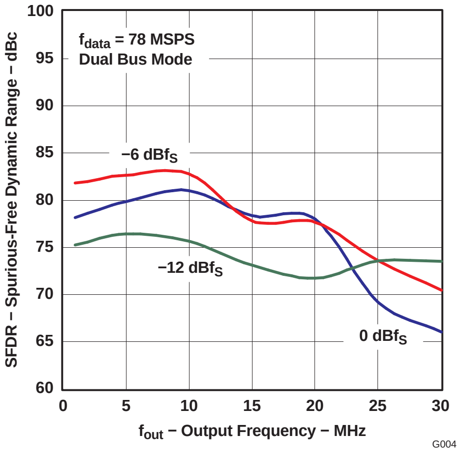


Figure 4. Spurious-Free Dynamic Range vs Output Frequency

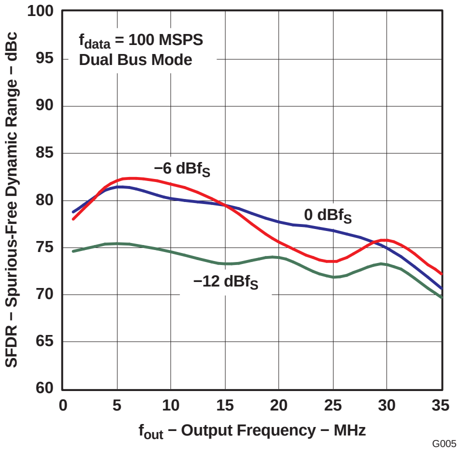


Figure 5. Spurious-Free Dynamic Range vs Output Frequency

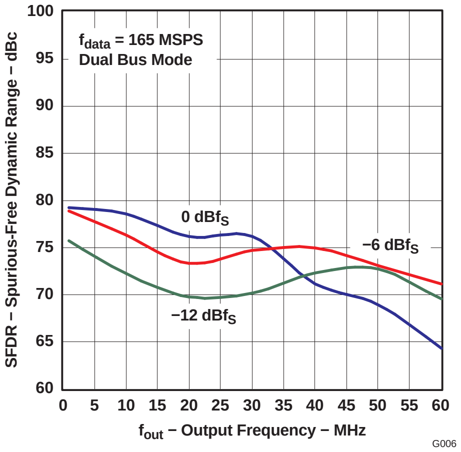


Figure 6. Spurious-Free Dynamic Range vs Output Frequency

Typical Characteristics (continued)

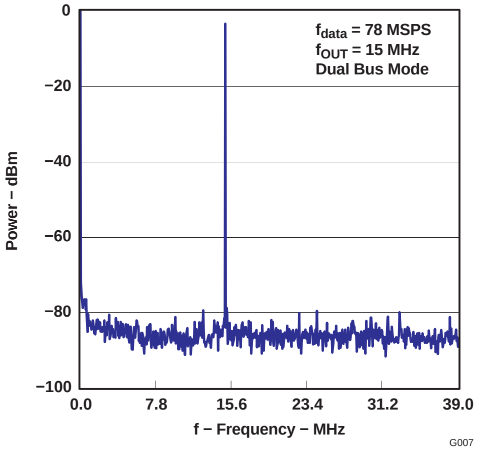


Figure 7. Single-Tone Spectrum

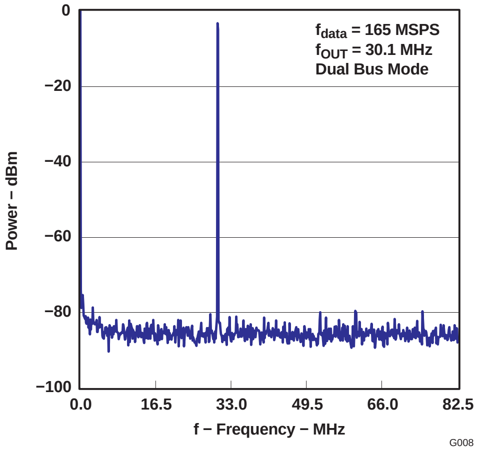


Figure 8. Single-Tone Spectrum

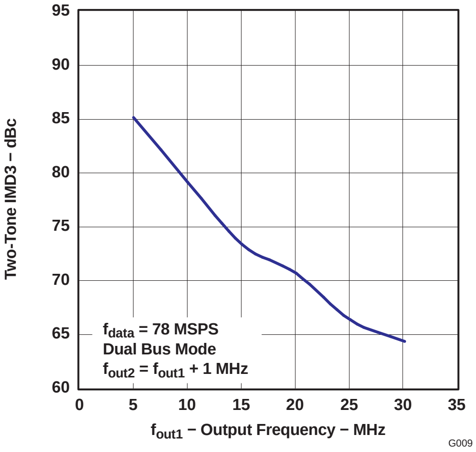


Figure 9. Two-Tone IMD3 vs Output Frequency

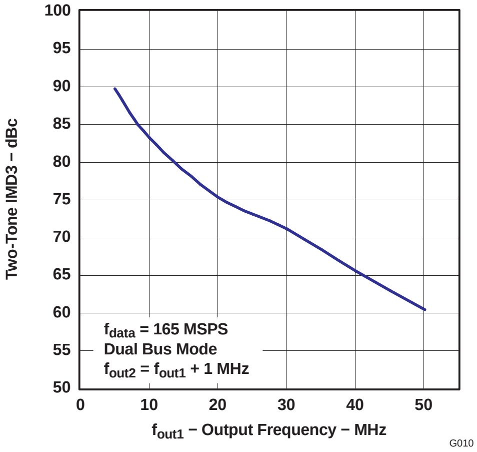


Figure 10. Two-Tone IMD3 vs Output Frequency

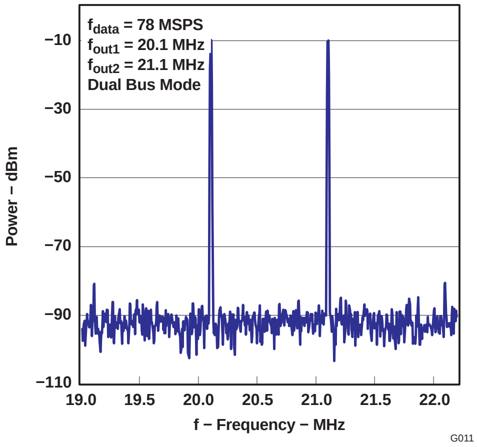


Figure 11. Two-Tone Spectrum

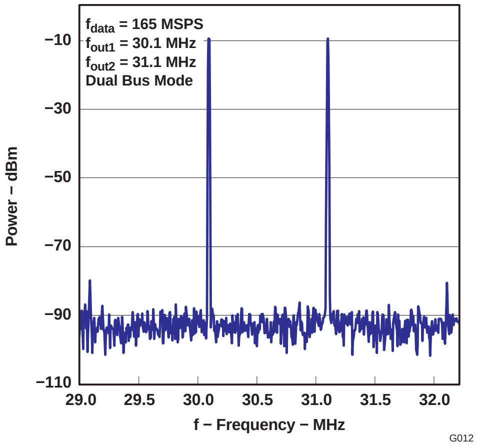


Figure 12. Two-Tone Spectrum

7 Detailed Description

7.1 Overview

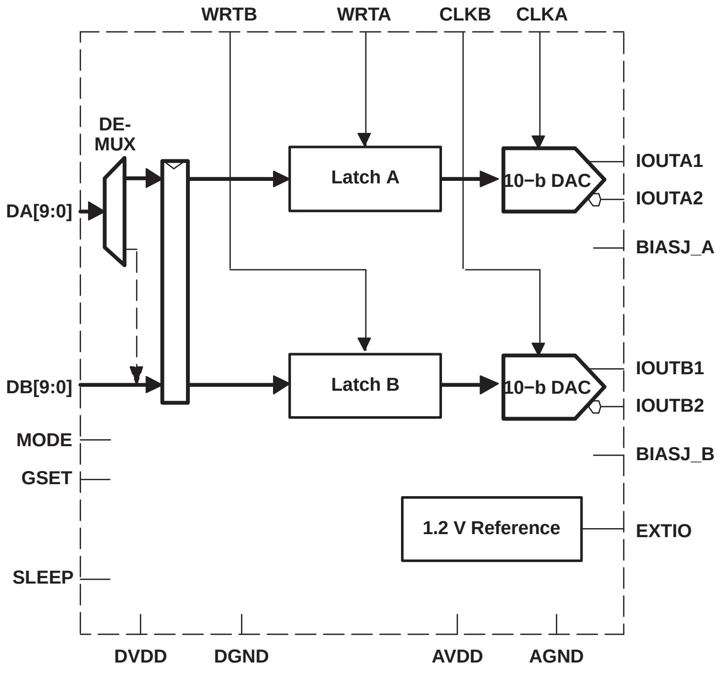
The architecture of the DAC5652A uses a current steering technique to enable fast switching and a high update rate. The core element within the monolithic DAC is an array of segmented current sources that are designed to deliver a full-scale output current of up to 20 mA. An internal decoder addresses the differential current switches each time the DAC is updated, and a corresponding output current is formed by steering all currents to either output summing node, IOUT1 or IOUT2. The complementary outputs deliver a differential output signal, which improves the dynamic performance through reduction of even-order harmonics, common-mode signals (noise), and doubles the peak-to-peak output signal swing by a factor of two, as compared to single-ended operation.

The segmented architecture results in a significant reduction of the glitch energy and improves the dynamic performance (SFDR) and DNL. The current outputs maintain a very high output impedance of greater than 300 kΩ.

When pin 42 (GSET) is high (simultaneous gain set mode), the full-scale output current for DACs is determined by the ratio of the internal reference voltage (1.2 V) and an external resistor (R_{SET}) connected to BIASJ_A. When GSET is low (independent gain set mode), the full-scale output current for each DAC is determined by the ratio of the internal reference voltage (1.2 V) and separate external resistors (R_{SET}) connected to BIASJ_A and BIASJ_B. The resulting I_{REF} is internally multiplied by a factor of 32 to produce an effective DAC output current that can range from 2 mA to 20 mA, depending on the value of R_{SET}.

The DAC5652A is split into a digital and an analog portion, each of which is powered through its own supply pin. The digital section includes edge-triggered input latches and the decoder logic, while the analog section comprises both the current source array with its associated switches, and the reference circuitry.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Digital Inputs

The data input ports of the DAC5652A accept a standard positive coding with data bits DA9 and DB9 being the most significant bits (MSB). The converter outputs support a clock rate of up to 275 MSPS. The best performance is typically achieved with a symmetric duty cycle for write and clock; however, the duty cycle may vary as long as the timing specifications are met. Similarly, the setup and hold times may be chosen within their specified limits.

All digital inputs of the DAC5652A are CMOS compatible. Figure 13 and Figure 14 show schematics of the equivalent CMOS digital inputs of the DAC5652A. The pullup and pulldown circuitry is approximately equivalent to 100 kΩ. The 10-bit digital data input follows the offset positive binary coding scheme. The DAC5652A is designed to operate with a digital supply (DVDD) of 3 V to 3.6 V.

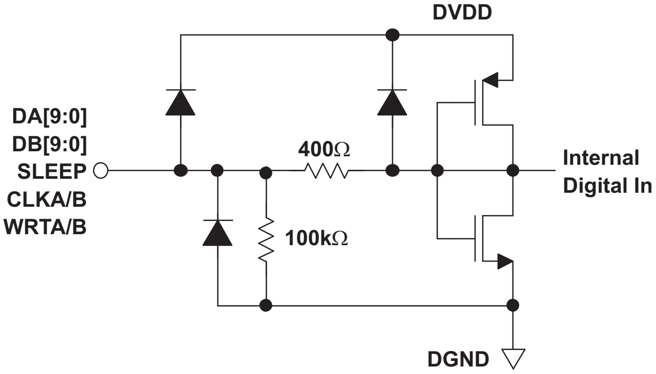


Figure 13. CMOS/TTL Digital Equivalent Input With Internal Pulldown Resistor

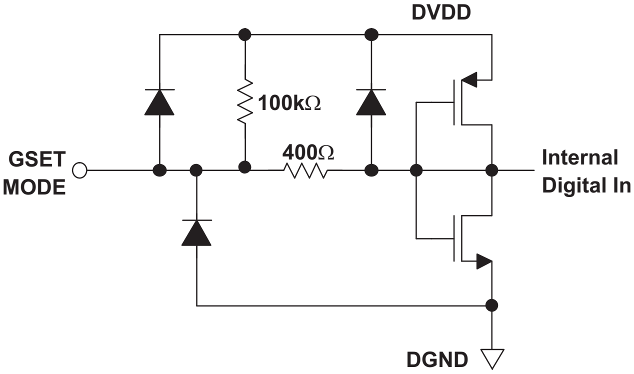


Figure 14. CMOS/TTL Digital Equivalent Input With Internal Pullup Resistor

Feature Description (continued)

7.3.2 References

7.3.2.1 Internal Reference

The DAC5652A has an on-chip reference circuit which comprises a 1.2-V bandgap reference and two control amplifiers, one for each DAC. The full-scale output current, $I_{(OUTFS)}$, of the DAC5652A is determined by the reference voltage, V_{REF}, and the value of resistor R_{SET}. $I_{(OUTFS)}$ is calculated by:

$$I_{OUTFS} = 32 \times I_{REF} = 32 \times \frac{V_{REF}}{R_{SET}} \qquad (1)$$

The reference control amplifier operates as a V-to-I converter producing a reference current, I_{REF}, which is determined by the ratio of V_{REF} and R_{SET} (see Equation 9). The full-scale output current, $I_{(OUTFS)}$, results from multiplying I_{REF} by a fixed factor of 32.

Using the internal reference, a 2-kΩ resistor value results in a full-scale output of approximately 20 mA. Resistors with a tolerance of 1% or better should be considered. Selecting higher values, the output current can be adjusted from 20 mA down to 2 mA. Operating the DAC5652A at lower than 20-mA output currents may be desirable for reasons of reducing the total power consumption, improving the distortion performance, or observing the output compliance voltage limitations for a given load condition.

It is recommended to bypass the EXTIO pin with a ceramic chip capacitor of 0.1 µF or more. The control amplifier is internally compensated and its small signal bandwidth is approximately 300 kHz.

7.3.2.2 External Reference

The internal reference can be disabled by simply applying an external reference voltage into the EXTIO pin, which in this case functions as an input. The use of an external reference may be considered for applications that require higher accuracy and drift performance or to add the ability of dynamic gain control.

While a 0.1-µF capacitor is recommended to be used with the internal reference, it is optional for the external reference operation. The reference input, EXTIO, has a high input impedance (1 MΩ) and can be driven by various sources. Note that the voltage range of the external reference must stay within the compliance range of the reference input.

7.4 Device Functional Modes

7.4.1 Input Interfaces

The DAC5652A features two operating modes selected by the MODE pin, as shown in Table 1.

- For dual-bus input mode, the device essentially consists of two separate DACs. Each DAC has its own separate data input bus, clock input, and data write signal (data latch-in).
- In single-bus interleaved mode, the data must be presented interleaved at the A-channel input bus. The B-channel input bus is not used in this mode. The clock and write input are now shared by both DACs.

Table 1. Operating Modes

MODE PIN	MODE PIN CONNECTED TO DGND	MODE PIN CONNECTED TO DVDD
Bus input	Single-bus interleaved mode, clock and write input equal for both DACs	Dual-bus mode, DACs operate independently

7.4.1.1 Dual-Bus Data Interface and Timing

In dual-bus mode, the MODE pin is connected to DVDD. The two converter channels within the DAC5652A consist of two independent, 10-bit, parallel data ports. Each DAC channel is controlled by its own set of write (WRTA, WRTB) and clock (CLKA, CLKB) lines. The WRTA/B lines control the channel input latches and the CLKA/B lines control the DAC latches. The data is first loaded into the input latch by a rising edge of the WRTA/B line.

The internal data transfer requires a correct sequence of write and clock inputs, since essentially two clock domains having equal periods (but possibly different phases) are input to the DAC5652A. This is defined by a minimum requirement of the time between the rising edge of the clock and the rising edge of the write inputs. This essentially implies that the rising edge of CLKA/B must occur at the same time or before the rising edge of the WRTA/B signal. A minimum delay of 2 ns must be maintained if the rising edge of the clock occurs after the rising edge of the write. Note that these conditions are satisfied when the clock and write inputs are connected externally. Note that all specifications were measured with the WRTA/B and CLKA/B lines connected together.

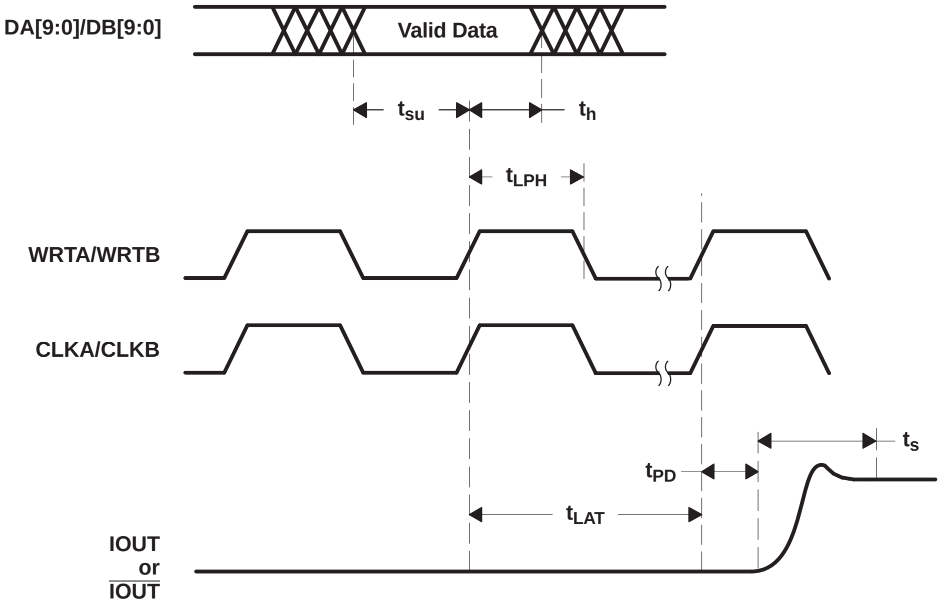


Figure 15. Dual-Bus Mode Operation

7.4.1.2 Single-Bus Interleaved Data Interface and Timing

In single-bus interleaved mode, the MODE pin is connected to DGND. Figure 16 shows the timing diagram. In interleaved mode, the A- and B-channels share the write input (WRTIQ) and update clock (CLKIQ and internal CLKDACIQ). Multiplexing logic directs the input word at the A-channel input bus to either the A-channel input latch (SELECTIQ is high) or to the B-channel input latch (SELECTIQ is low). When SELECTIQ is high, the data value in the B-channel latch is retained by presenting the latch output data to its input again. When SELECTIQ is low, the data value in the A-channel latch is retained by presenting the latch output data to its input.

In interleaved mode, the A-channel input data rate is twice the update rate of the DAC core. As in dual-bus mode, it is important to maintain a correct sequence of write and clock inputs. The edge-triggered flip-flops latch the A- and B-channel input words on the rising edge of the write input (WRTIQ). This data is presented to the A- and B-DAC latches on the following falling edge of the write inputs. The DAC5652A clock input is divided by a factor of two before it is presented to the DAC latches.

Correct pairing of the A- and B-channel data is done by RESETIQ. In interleaved mode, the clock input CLKIQ is divided by two, which would translate to a non-deterministic relation between the rising edges of the CLKIQ and CLKDACIQ. RESETIQ ensures, however, that the correct position of the rising edge of CLKDACIQ with respect to the data at the input of the DAC latch is determined. CLKDACIQ is disabled (low) when RESETIQ is high.

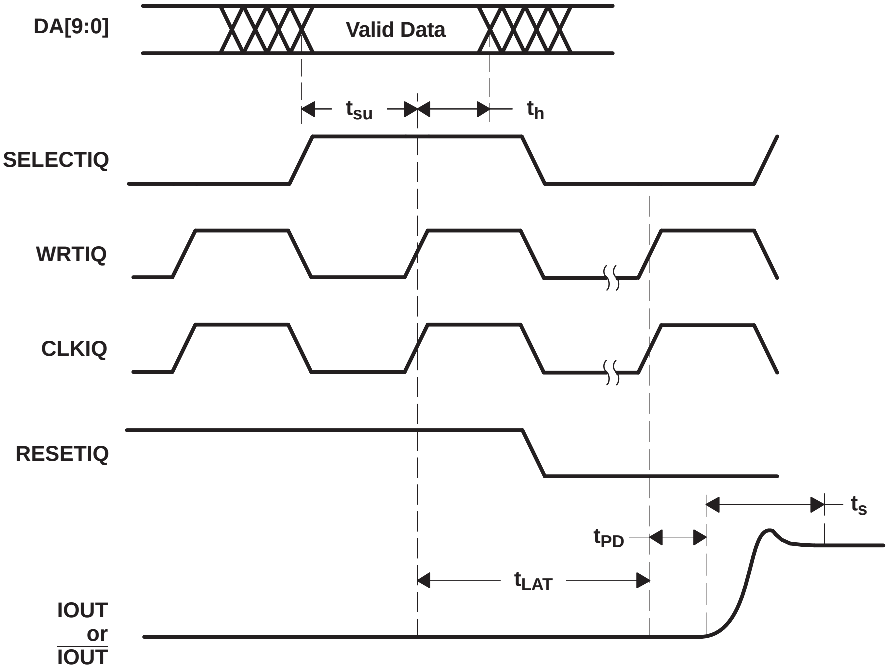


Figure 16. Single-Bus Interleaved Mode Operation

7.4.2 Gain Setting Option

The full-scale output current on the DAC5652A can be set two ways: either for each of the two DAC channels independently or for both channels simultaneously. For the independent gain set mode, the GSET pin (pin 42) must be low (that is, connected to AGND). In this mode, two external resistors are required — one R_{SET} connected to the BIASJ_A pin (pin 44) and the other to the BIASJ_B pin (pin 41). In this configuration, the user has the flexibility to set and adjust the full-scale output current for each DAC independently, allowing for the compensation of possible gain mismatches elsewhere within the transmit signal path.

Alternatively, bringing the GSET pin high (that is, connected to AVDD), the DAC5652A switches into the simultaneous gain set mode. Now the full-scale output current of both DAC channels is determined by only one external R_{SET} resistor connected to the BIASJ_A pin. The resistor at the BIASJ_B pin may be removed; however, this is not required since this pin is not functional in this mode and the resistor has no effect on the gain equation.

7.4.3 Sleep Mode

The DAC5652A features a power-down function that can reduce the total supply current to approximately 3.1 mA over the specified supply range if no clock is present. Applying a logic high to the SLEEP pin initiates power-down mode, whereas a logic low enables normal operation. When left unconnected, an internal active pulldown circuit enables the normal operation of the converter.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DAC5652A is a 10-bit dual DAC with max update rate of 275 MSPS. The DAC supports two different modes of operation: dual bus and single bus. In dual-bus mode, the DAC provides two independent transmit paths that can be programmed for two different update rates. In single-bus mode, the interleaved data for both channels are applied at the A-channel input bus. The B-channel input bus is not used in this mode. The clock and write input are now shared by both DACs. Thus, two different input signals can be transmitted from the two channels, but the update rate for both channels is the same.

8.1.1 DAC Transfer Function

Each of the DACs in the DAC5652A has a set of complementary current outputs, IOUT1 and IOUT2. The full-scale output current, I_{OUTFS}, is the summation of the two complementary output currents:

$$I_{OUTFS} = I_{OUT1} + I_{OUT2} \tag{2}$$

The individual output currents depend on the DAC code and can be expressed as:

$$I_{OUT1} = I_{OUTFS} \times \left(\frac{Code}{1024}\right) \tag{3}$$

$$I_{OUT2} = I_{OUTFS} \times \left(\frac{1023 - Code}{1024}\right) \tag{4}$$

where Code is the decimal representation of the DAC data input word. Additionally, I_{OUTFS} is a function of the reference current I_{REF}, which is determined by the reference voltage and the external setting resistor (R_{SET}).

$$I_{OUTFS} = 32 \times I_{REF} = 32 \times \frac{V_{REF}}{R_{SET}} \tag{5}$$

In most cases, the complementary outputs drive resistive loads or a terminated transformer. A signal voltage develops at each output according to:

$$V_{OUT1} = I_{OUT1} \times R_{LOAD} \tag{6}$$

$$V_{OUT2} = I_{OUT2} \times R_{LOAD} \tag{7}$$

The value of the load resistance is limited by the output compliance specification of the DAC5652A. To maintain specified linearity performance, the voltage for IOUT1 and IOUT2 must not exceed the maximum allowable compliance range.

The total differential output voltage is:

$$V_{OUTDIFF} = V_{OUT1} - V_{OUT2} \tag{8}$$

$$V_{OUTDIFF} = \frac{(2 \times Code - 1023)}{1024} \times I_{OUTFS} \times R_{LOAD} \tag{9}$$

Application Information (continued)

8.1.1.1 Analog Outputs

The DAC5652A provides two complementary current outputs, IOUT1 and IOUT2. The simplified circuit of the analog output stage representing the differential topology is shown in Figure 17. The output impedance of IOUT1 and IOUT2 results from the parallel combination of the differential switches, along with the current sources and associated parasitic capacitances.

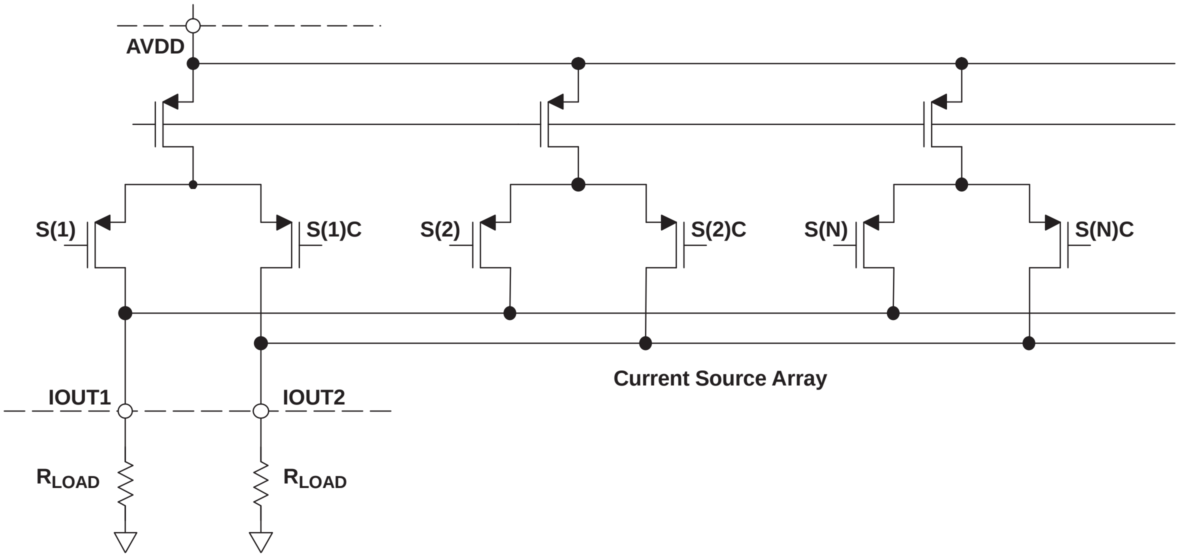


Figure 17. Analog Outputs

The signal voltage swing that may develop at the two outputs, IOUT1 and IOUT2, is limited by a negative and positive compliance. The negative limit of –1 V is given by the breakdown voltage of the CMOS process and exceeding it compromises the reliability of the DAC5652A (or even causes permanent damage). With the full-scale output set to 20 mA, the positive compliance equals 1.2 V. Note that the compliance range decreases to about 1 V for a selected output current of $I_{(OUTFS)}$ = 2 mA. Care must be taken that the configuration of DAC5652A does not exceed the compliance range to avoid degradation of the distortion performance and integral linearity.

Best distortion performance is typically achieved with the maximum full-scale output signal limited to approximately 0.5 V_{PP}. This is the case for a 50-Ω doubly-terminated load and a 20-mA full-scale output current. A variety of loads can be adapted to the output of the DAC5652A by selecting a suitable transformer while maintaining optimum voltage levels at IOUT1 and IOUT2. Furthermore, using the differential output configuration in combination with a transformer is instrumental for achieving excellent distortion performance. Common-mode errors, such as even-order harmonics or noise, can be substantially reduced. This is particularly the case with high output frequencies.

For those applications requiring the optimum distortion and noise performance, it is recommended to select a full-scale output of 20 mA. A lower full-scale range of 2 mA may be considered for applications that require low power consumption, but can tolerate a slight reduction in performance level.

8.1.2 Output Configurations

The current outputs of the DAC5652A allow for a variety of configurations. As mentioned previously, utilizing the converter's differential outputs yield the best dynamic performance. Such a differential output circuit may consist of an RF transformer or a differential amplifier configuration. The transformer configuration is ideal for most applications with ac coupling, while op amps are suitable for a dc-coupled configuration.

The single-ended configuration may be considered for applications requiring a unipolar output voltage. Connecting a resistor from either one of the outputs to ground converts the output current into a ground-referenced voltage signal. To improve on the dc linearity by maintaining a virtual ground, an I-to-V or op-amp configuration may be considered.

Application Information (continued)

8.1.3 Differential With Transformer

Using an RF transformer provides a convenient way of converting the differential output signal into a single-ended signal while achieving excellent dynamic performance. The appropriate transformer must be carefully selected based on the output frequency spectrum and impedance requirements.

The differential transformer configuration has the benefit of significantly reducing common-mode signals, thus improving the dynamic performance over a wide range of frequencies. Furthermore, by selecting a suitable impedance ratio (winding ratio) the transformer can provide optimum impedance matching while controlling the compliance voltage for the converter outputs.

Figure 18 and Figure 19 show 50-Ω doubly-terminated transformer configurations with 1:1 and 4:1 impedance ratios, respectively. Note that the center tap of the primary input of the transformer has to be grounded to enable a dc-current flow. Applying a 20-mA full-scale output current would lead to a 0.5-V_{PP} output for a 1:1 transformer and a 1-V_{PP} output for a 4:1 transformer. In general, the 1:1 transformer configuration has a better output distortion, but the 4:1 transformer has 6 dB higher output power.

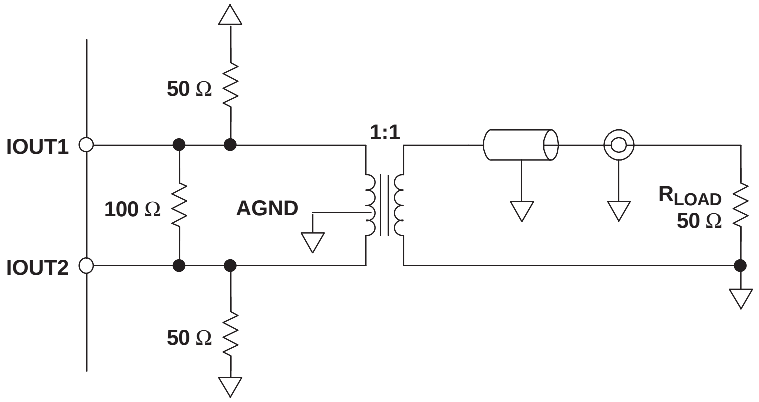


Figure 18. Driving a Doubly-Terminated 50-Ω Cable Using a 1:1 Impedance Ratio Transformer

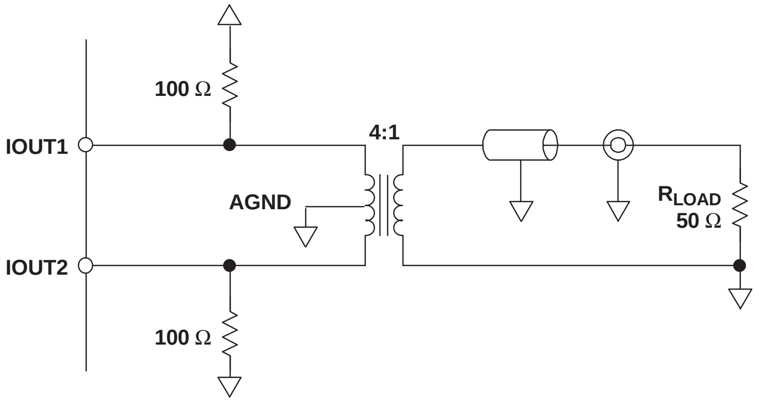


Figure 19. Driving a Doubly-Terminated 50-Ω Cable Using a 4:1 Impedance Ratio Transformer

Application Information (continued)

8.1.4 Single-Ended Configuration

Figure 20 shows the single-ended output configuration, where the output current IOUT1 flows into an equivalent load resistance of 25 Ω. Node IOUT2 must be connected to AGND or terminated with a resistor of 25 Ω to AGND. The nominal resistor load of 25 Ω gives a differential output swing of 1 V_{PP} when applying a 20-mA full-scale output current.

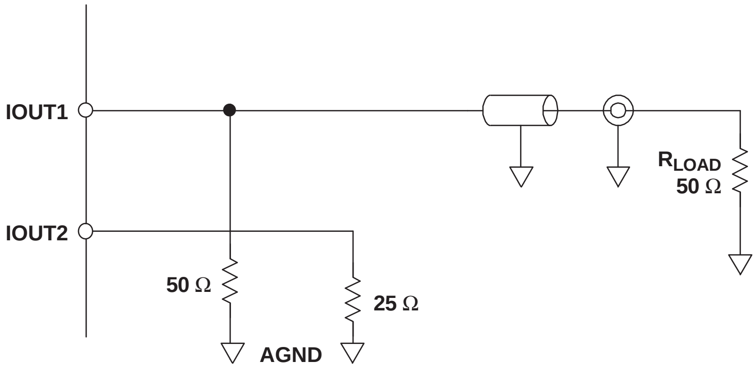


Figure 20. Driving a Doubly-Terminated 50-Ω Cable Using a Single-Ended Output

8.2 Typical Application

A typical application for the DAC5652A is a dual- or single-carrier transmitter. The DAC is provided with some input digital baseband signal, and outputs an analog carrier. A design example for a single-carrier transmitter is described in this section.

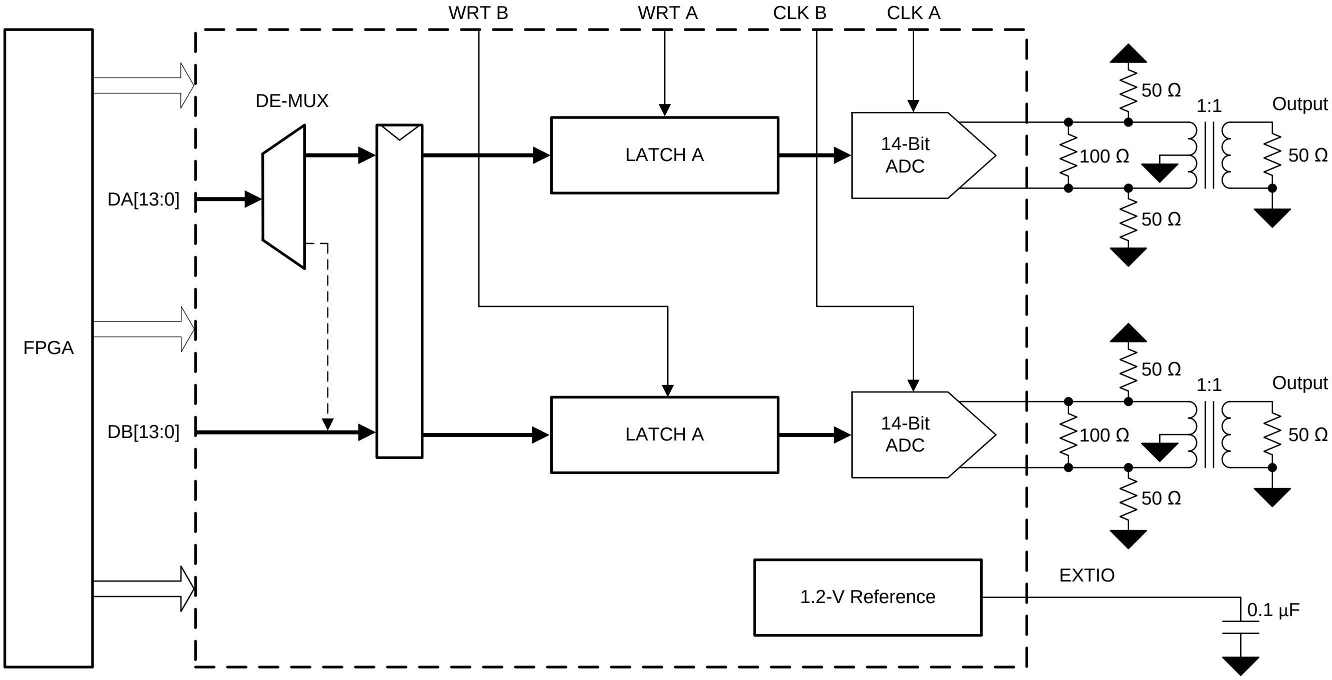


Figure 21. Single-Carrier Transmitter

8.2.1 Design Requirements

The requirements for this design are to generate a single WCDMA signal at an intermediate frequency of 30.72 MHz. The ACLR needs to be better than 72 dBc.

Table 2. Design Parameters

FEATURE	SPECIFICATION
Number of carriers	1
AVDD and DVDD	3.3 V
Clock rate	122.88 MSPS
Input data	WCDMA with IF at 30.72 MHz
ACPR	> 72 dB

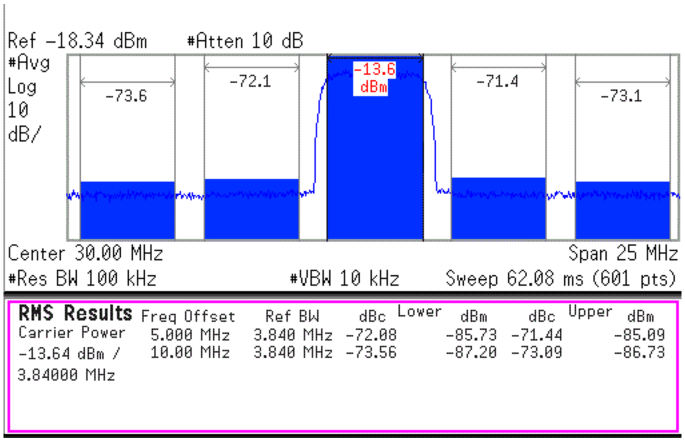
8.2.2 Detailed Design Procedure

The single WCDMA carrier signal with an intermediate frequency (IF) of 30.72 MHz must be created in the digital processor at a sample rate of 122.88 MSPS for the DAC. These 10-bit samples are placed on the 10-bit CMOS input port of the DAC.

A CMOS DAC clock must be generated from a clock source at 122.88 MHz. This clock must be provided to the CLK pin of the DAC. The IOUTA and IOUTB differential connections must be connected to a transformer in order to provide a single-ended output. A typical 1:1 impedance transformer is used on the device EVM. The DAC5672A evaluation module (EVM) provides a good reference for this design example.

8.2.3 Application Curve

Figure 22 presents a spectrum analyzer plot shows the adjacent channel power ratio (ACPR) for the transformer-output, single-carrier signal with an intermediate frequency of 30.72 MHz. The results meet the system requirements for a minimum of 72-dBc ACPR.



Ref -18.34 dBm #Atten 10 dB
#Avg
Log
10
dB/
Center 30.00 MHz Span 25 MHz
#Res BW 100 kHz #VBW 10 kHz Sweep 62.08 ms (601 pts)

RMS Results	Freq Offset	Ref BW	Lower		Upper	
			dBc	dBm	dBc	dBm
Carrier Power -13.64 dBm / 3.84000 MHz	5.000 MHz	3.840 MHz	-72.08	-85.73	-71.44	-85.09
	10.00 MHz	3.840 MHz	-73.56	-87.20	-73.09	-86.73

Figure 22. ACPR Performance

9 Power Supply Recommendations

Power the device with the nominal supply voltages as indicated in the *Recommended Operating Conditions*.

In most instances, the best performance is achieved with LDO supplies. However, the supplies may be driven with direct outputs from a DC/DC switcher, as long as the noise performance of the switcher is acceptable.

For best performance:

- Use at least two power layers.
- Avoid placing digital supplies and clean supplies on adjacent board layers.
- Use a ground layer between noisy and clean supplies, if possible.
- Decouple all supply pins as close to the pins as possible, using small-value capacitors, with larger, bulk capacitors placed further away.

10 Layout

10.1 Layout Guidelines

Use the DAC5652AEVM layout as a reference to obtain the best performance. A sample layout is shown in Figure 23 through Figure 26. Some important layout recommendations are:

1. Use a single ground plane. Keep the digital and analog signals on distinct separate sections of the board. This may be virtually divided down the middle of the device package when doing placement and layout.
2. Keep the analog outputs as far away from the switching clocks and digital signals as possible. This keeps coupling from the digital circuits to the analog outputs to a minimum.
3. Keep decoupling capacitors close to the power pins of the device.

10.2 Layout Examples

Figure 23 through Figure 26 show the layout examples.

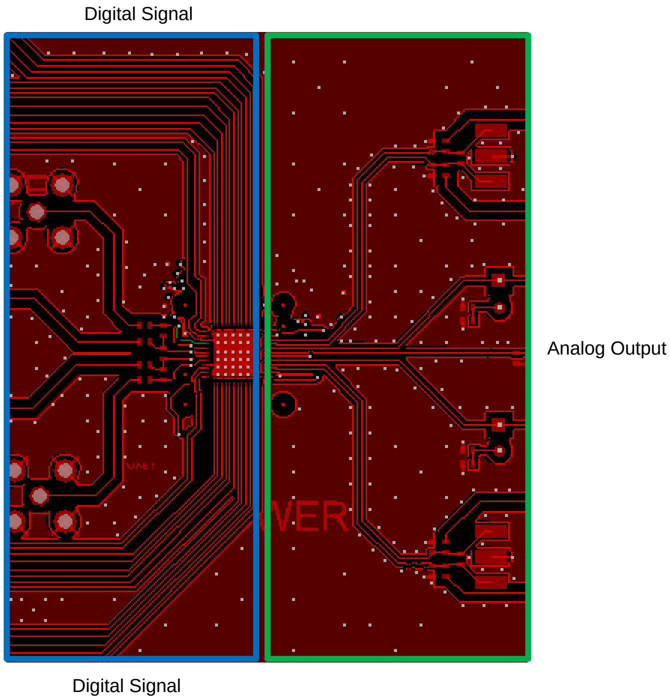


Figure 23. Layout Example: Top Layer (Layer 1)

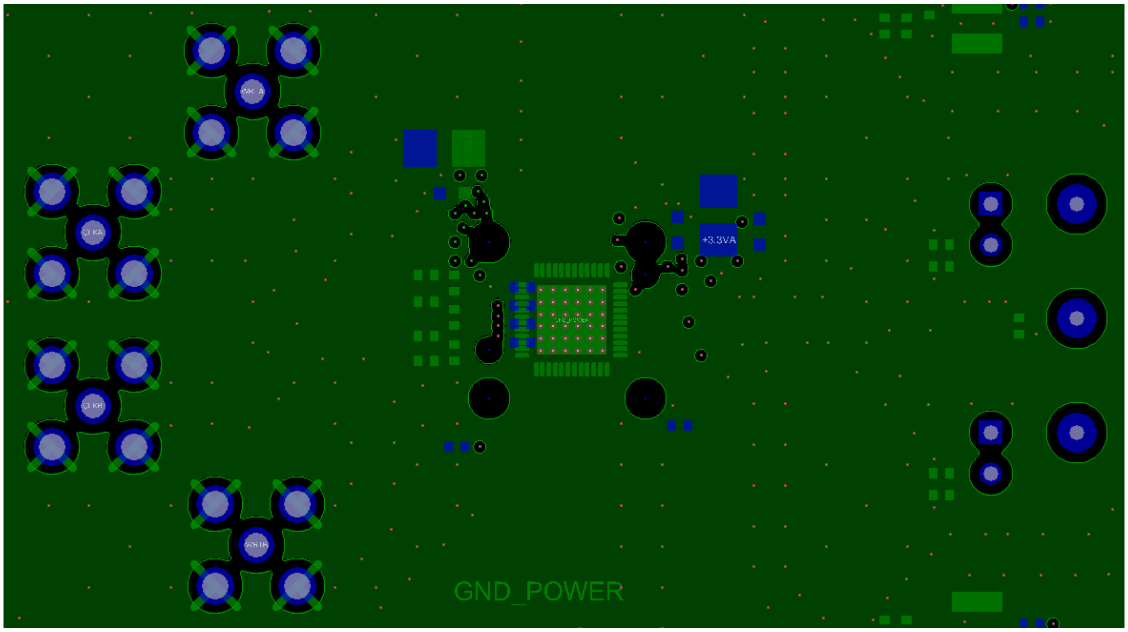


Figure 24. Layout Example: Single Ground Plane (Layer 2)

Layout Examples (continued)

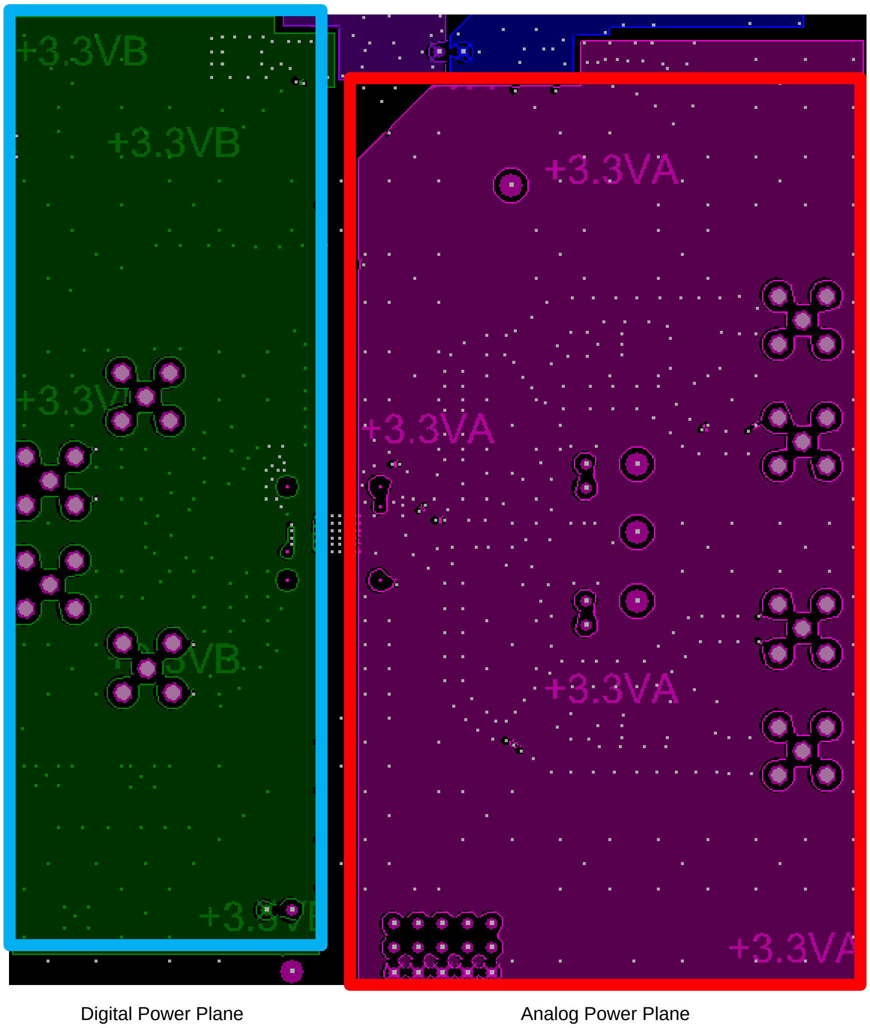


Figure 25. Layout Example: Power Plane (Layer 3)

Layout Examples (continued)

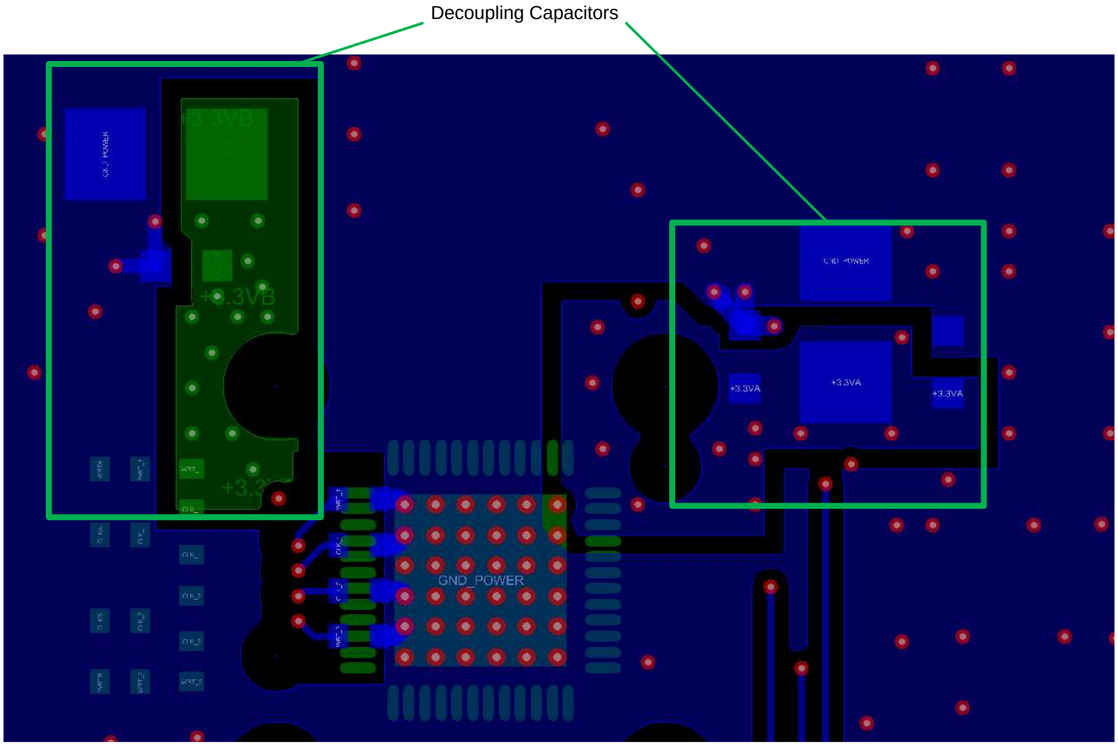


Figure 26. Layout Example: Bottom Layer (Layer 4)

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントのサポート

11.1.1 関連資料

関連資料については、以下を参照してください。

- *『DAC5652AEVMユーザー・ガイド』*

11.2 ドキュメントの更新通知を受け取る方法

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11.3 コミュニティ・リソース

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静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC5652AIPFB	ACTIVE	TQFP	PFB	48	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC5652AI	Samples
DAC5652AIPFBR	ACTIVE	TQFP	PFB	48	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC5652AI	Samples
DAC5652AIRSLR	ACTIVE	VQFN	RSL	48	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DA5652A	Samples
DAC5652AIRSLT	ACTIVE	VQFN	RSL	48	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DA5652A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

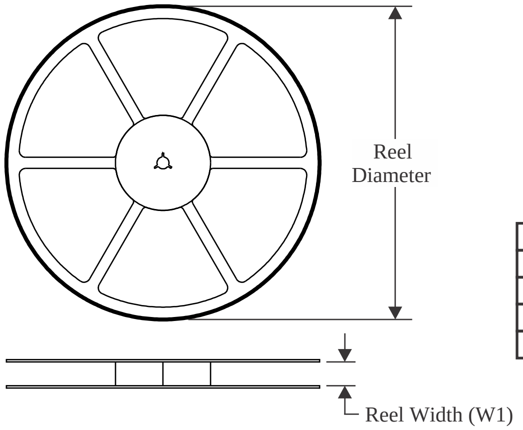
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

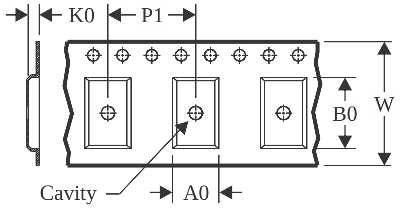
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

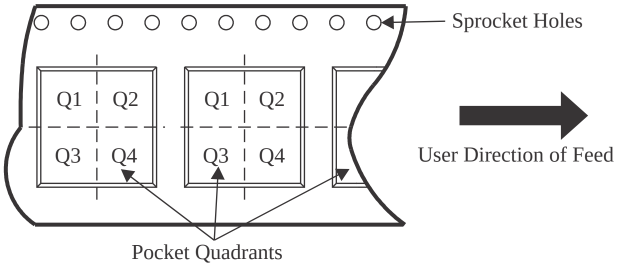


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

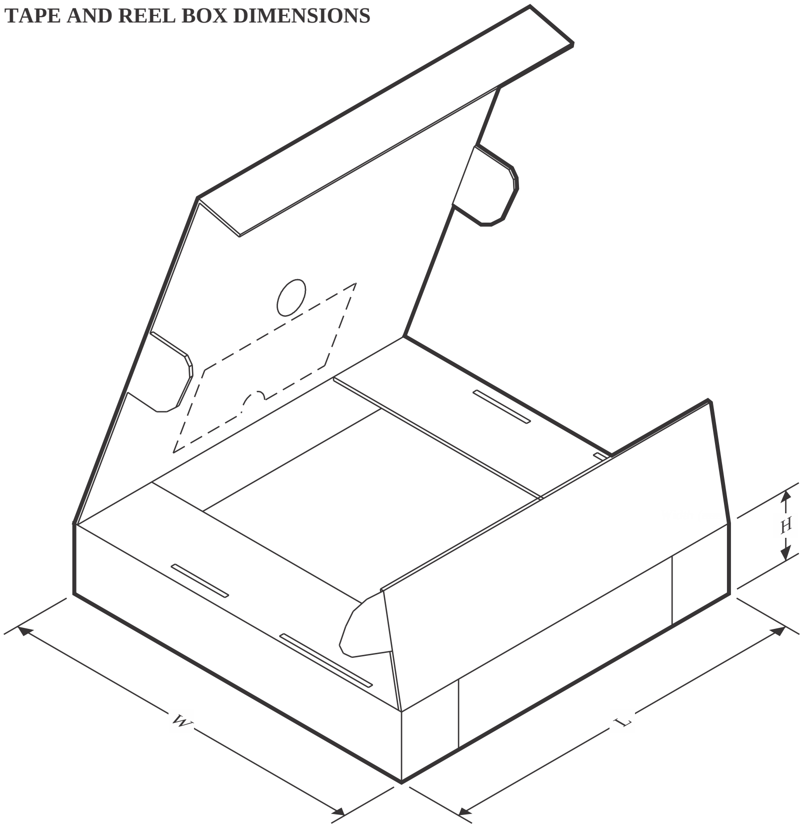
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC5652AIPFBR	TQFP	PFB	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
DAC5652AIRSLR	VQFN	RSL	48	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
DAC5652AIRSLT	VQFN	RSL	48	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

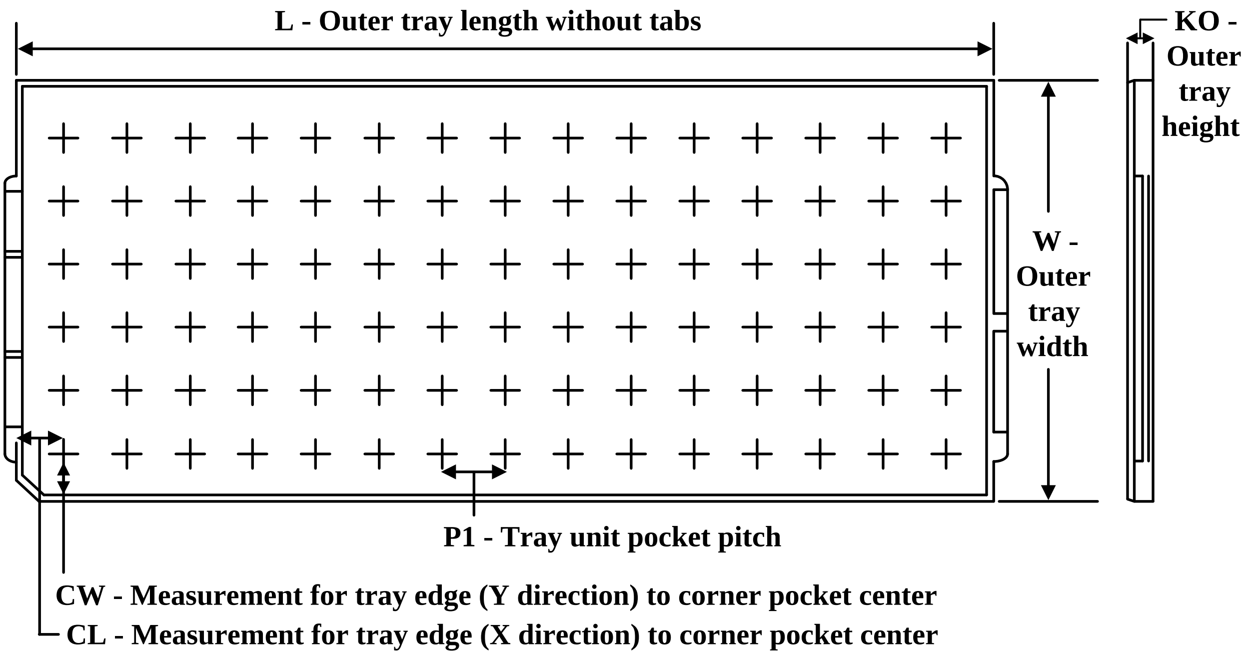
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC5652AIPFBR	TQFP	PFB	48	1000	367.0	367.0	38.0
DAC5652AIRSLR	VQFN	RSL	48	2500	367.0	367.0	35.0
DAC5652AIRSLT	VQFN	RSL	48	250	210.0	185.0	35.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

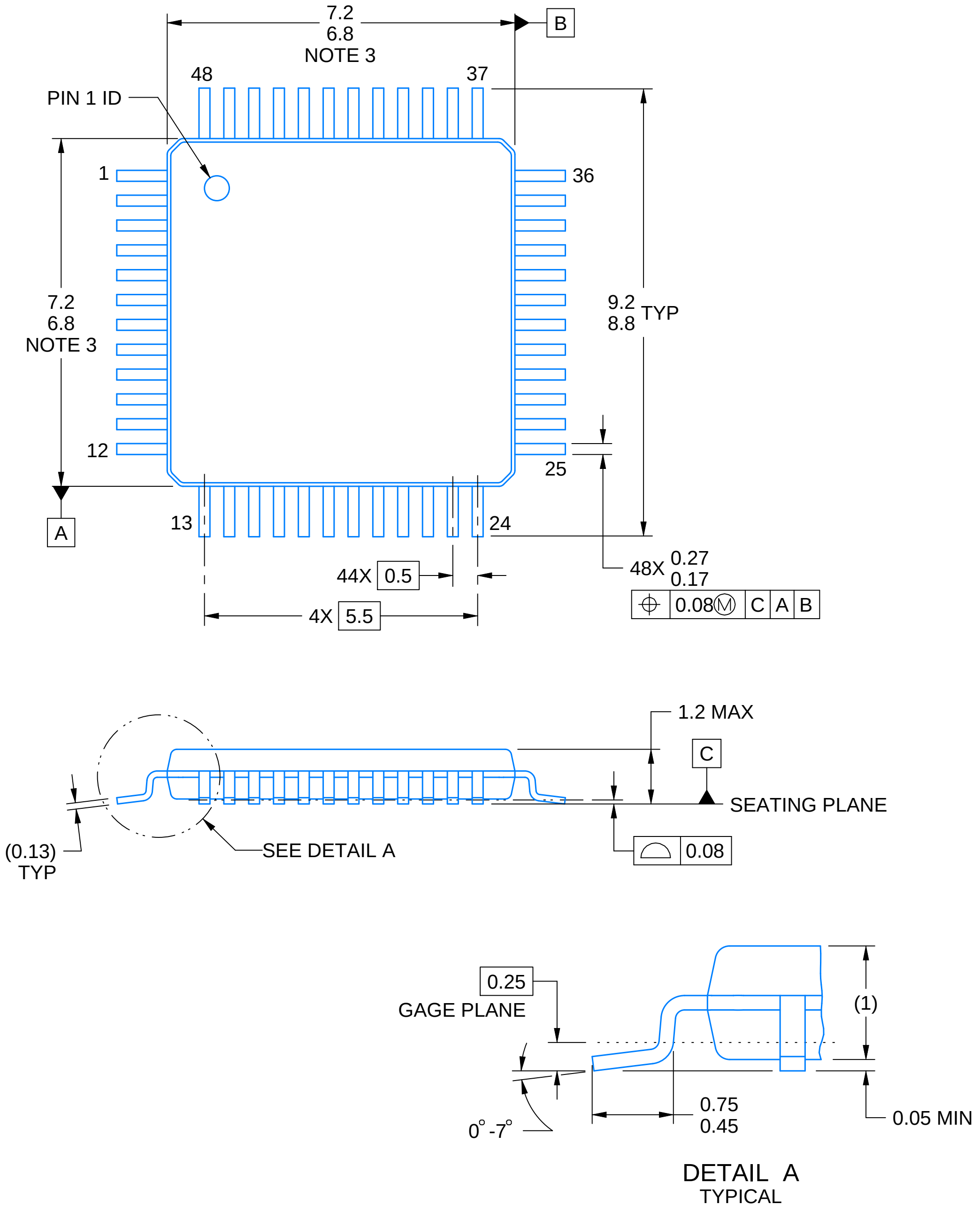
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
DAC5652AIPFB	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.5	11.25

PACKAGE OUTLINE

TQFP - 1.2 mm max height

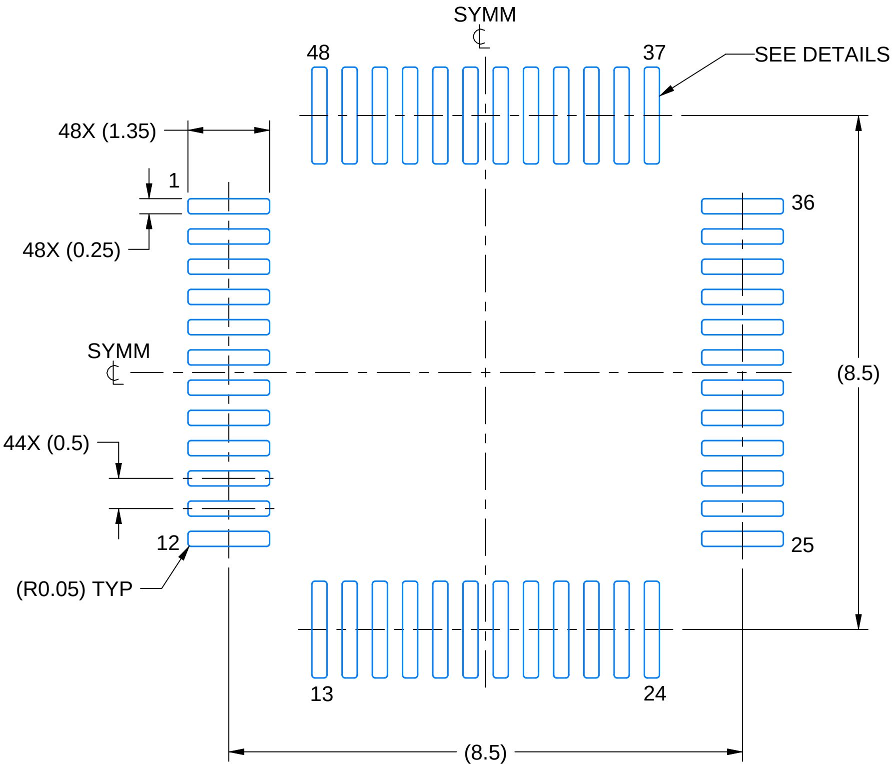
PLASTIC QUAD FLATPACK



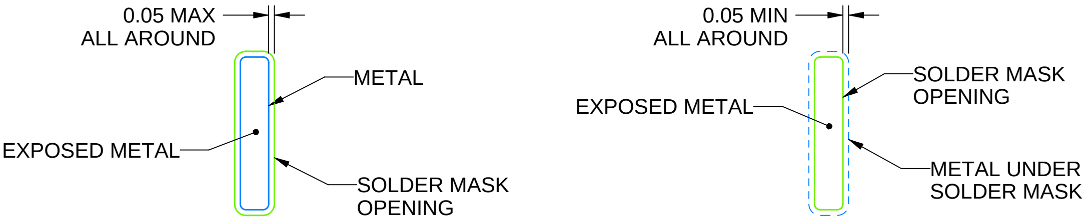
4215157/A 03/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK
DEFINED

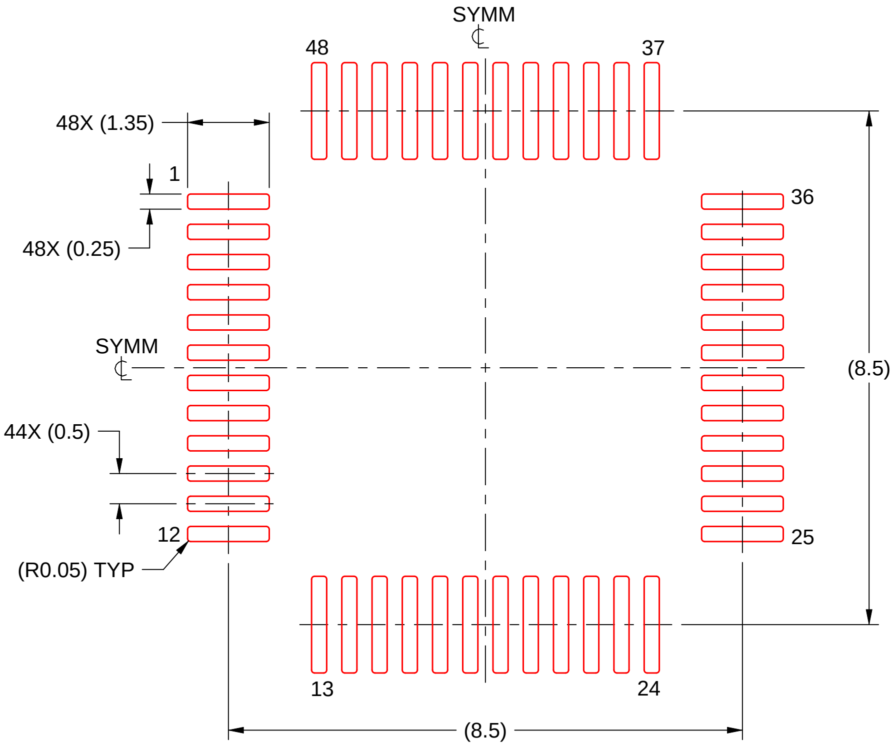
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4215157/A 03/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



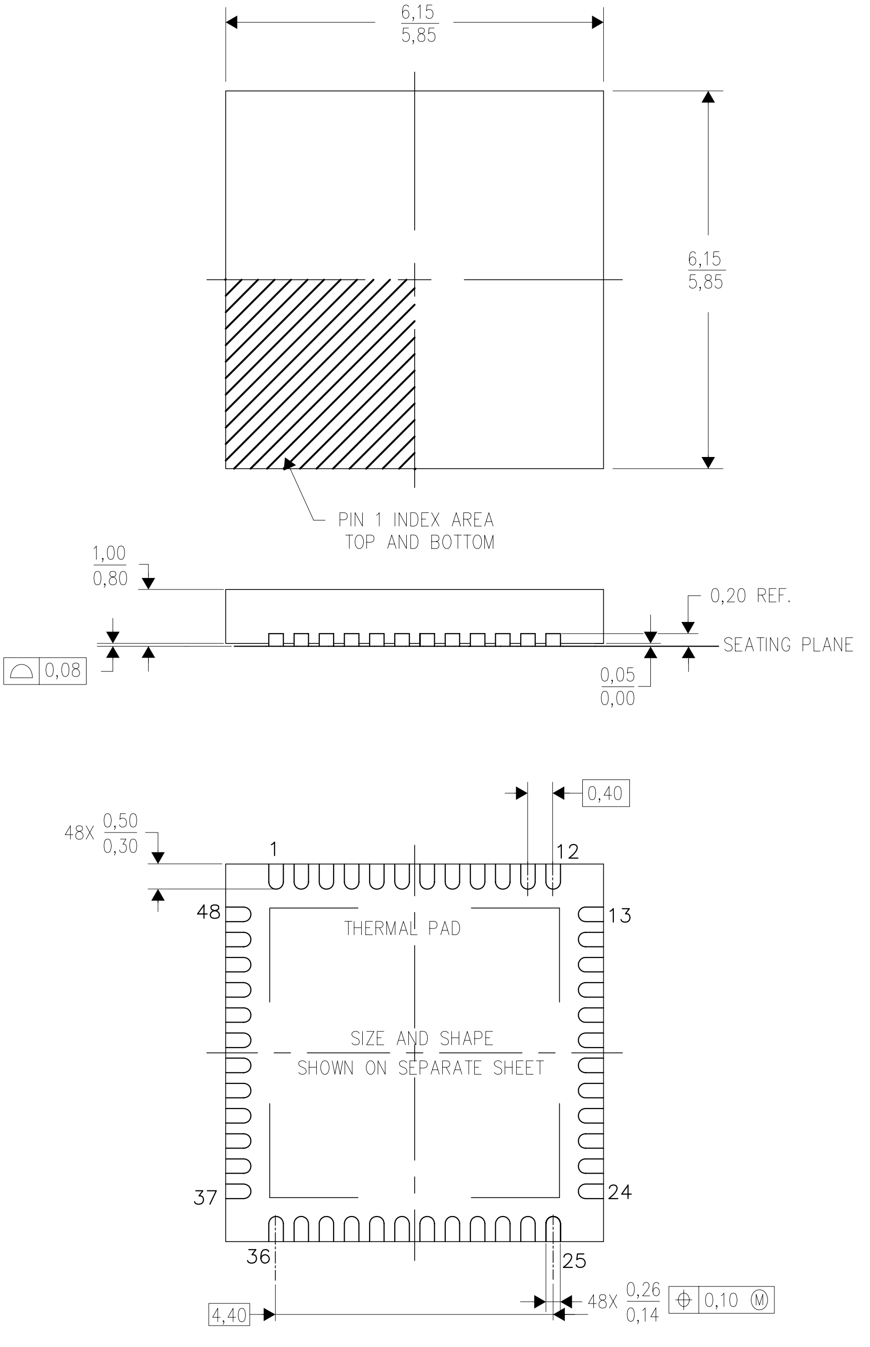
SOLDER PASTE EXAMPLE
SCALE:8X

4215157/A 03/2024

NOTES: (continued)

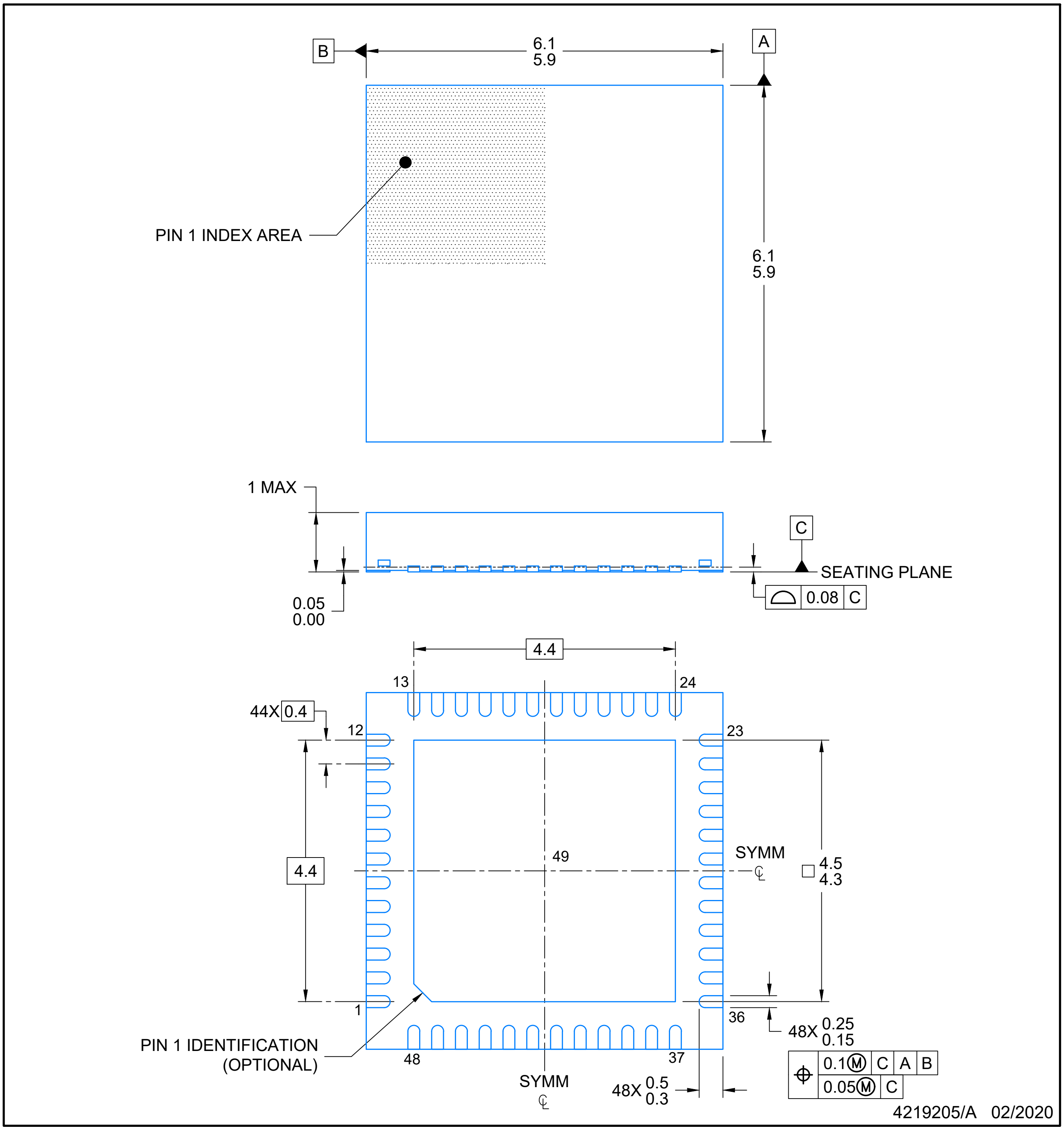
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

RSL (S-PVQFN-N48) PLASTIC QUAD FLATPACK NO-LEAD



4207548/B 06/11

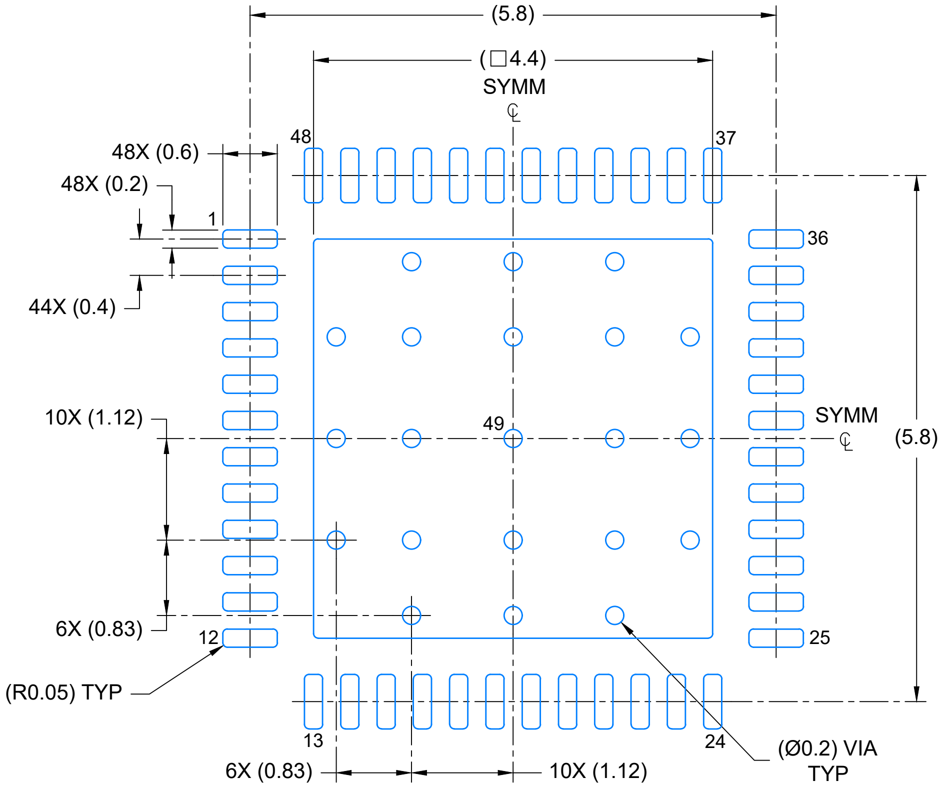
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No-leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.



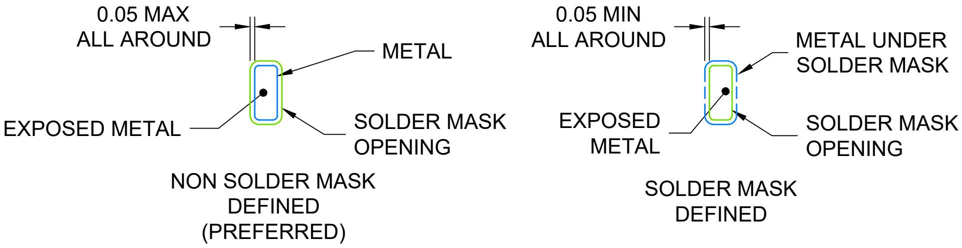
4219205/A 02/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X

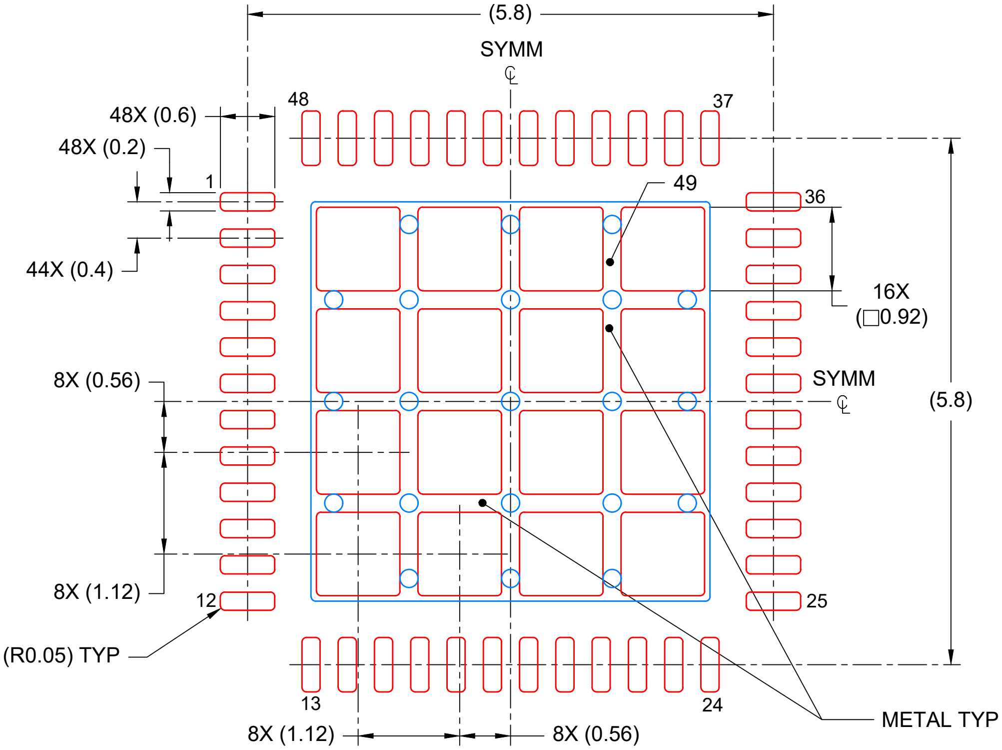


SOLDER MASK DETAILS

4219205/A 02/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
70% PRINTED COVERAGE BY AREA
SCALE: 12X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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