

DCPA1シリーズ1W、絶縁型、非レギュレートDC/DCコンバータ・モジュール

1 特長

- 2.0kVDC絶縁(動作時)
- ソフトスタートにより突入電流を低減
- 周波数同期
- EN55022 Class B EMC特性
- UL1950認定済みのコンポーネント
- 7ピンPDIPおよび7ピンSOPパッケージ

2 アプリケーション

- 信号パス絶縁
- グランド・ループの除去
- データ収集
- 産業用制御および計測機器
- 試験用機器

3 概要

DCPA1シリーズは、1W、絶縁型、非レギュレートのDC/DCコンバータ・モジュールのファミリーです。DCPA1シリーズのデバイスは必要な外付け部品が2つだけで、オンチップのデバイス保護が内蔵され、外部クロックと同期できます。

これらの機能に加え、サイズが小さいことから、DCPA1シリーズのデバイスは広範なアプリケーションに適しており、信号パスの絶縁が必要なアプリケーションで簡単に使用できるソリューションです。

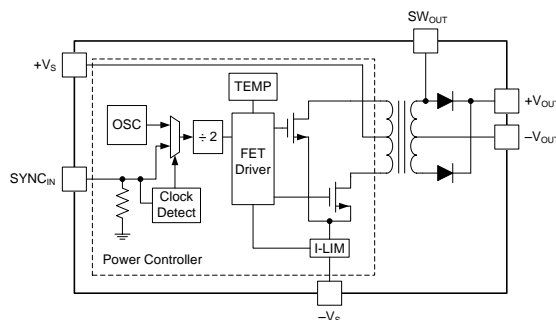
警告: この製品の動作絶縁は、信号の絶縁のみを目的としています。強化絶縁を必要とする安全用の絶縁回路の一部として使用してはいけません。[機能説明](#)セクションの定義を参照してください。

製品情報 (1)

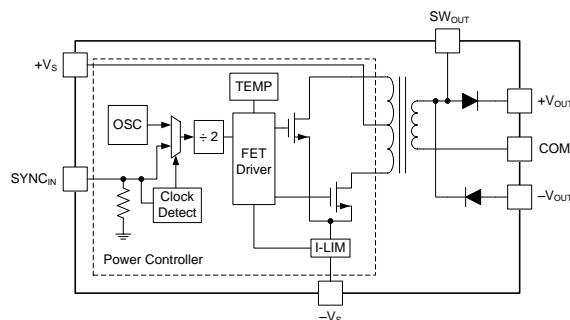
型番	パッケージ	本体サイズ(typ)
DCPA1xxxx	PDIP (7)	19.18mm×10.60mm
	SOP (7)	

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

単一出力のブロック図



デュアル出力のブロック図



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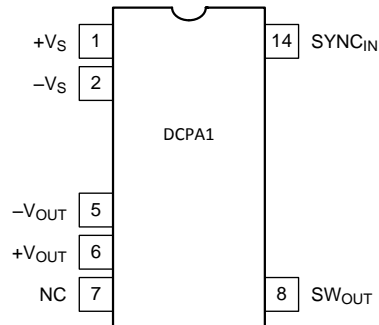
4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

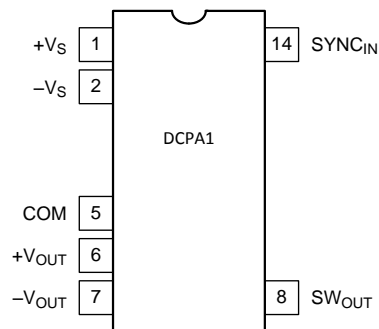
日付	改訂内容	注
2017年4月	*	初版

5 Pin Configuration and Functions

NVA and DUA Package
7-Pin PDIP and SOP (Single Output)
(Top View)



NVA and DUA Package
7-Pin PDIP and SOP (Dual Output)
(Top View)



Pin Functions

PIN NAME	PIN NUMBER		I/O ⁽¹⁾	Description
	SINGLE-OUTPUT	DUAL-OUTPUT		
COM	—	5	O	Output side common
NC	7	—	—	No connection
SYNC _{IN}	14	14	I	Synchronization. This pin is used to synchronize to an external clock. Internally it is pulled to GND. If valid clock is not detected on this pin, the SN6505 shifts automatically to internal clock.
SW _{OUT}	8	8	O	Unrectified transformer output.
+V _{OUT}	6	6	O	Positive output voltage
+V _S	1	1	I	Input voltage
-V _{OUT}	5	7	O	Negative output voltage
-V _S	2	2	I	Input side common

(1) I = Input, O = Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
Input voltage	+V _S	-0.5	6	V
	50ns transient	-1.0	7	V
	SYNC _{IN}	-0.5	+V _S	V
		50ns transient	-1.0	6
Lead temperature (soldering, 10 s)			260	°C
Storage temperature, T _{stg}		-60	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±1000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±250

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage		4.5	5	5.5	V
Output power		0.05		1	W
Operating ambient temperature range		-40		100	°C

6.4 Electrical Characteristics

T_A = 25°C, +V_S = nominal, C_{IN} = 2.2 μF, C_{OUT} = 1.0 μF, (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
P _{OUT}	Output power	Over +V _S range, I _{OUT} = 100% (full load)				1	W
I _{OUT}	Output current	DCPA10505				200	mA
		DCPA10505D				200 ⁽¹⁾	mA
		DCPA10512				83	mA
		DCPA10512D				83 ⁽¹⁾	mA
		DCPA10515				66	mA
		DCPA10515D				66 ⁽¹⁾	mA

(1) I_{OUT1} + I_{OUT2}

Electrical Characteristics (continued)

 $T_A = 25^\circ\text{C}$, $+V_S = \text{nominal}$, $C_{IN} = 2.2\ \mu\text{F}$, $C_{OUT} = 1.0\ \mu\text{F}$, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	Output voltage	$I_{OUT} = 100\% \text{ load }^{(2)}$	DCPA10505	5.0		V
			DCPA10505D	± 5.0		V
			DCPA10512	12.0		V
			DCPA10512D	± 12.0		V
			DCPA10515	15.0		V
			DCPA10515D	± 15.0		V
	Temperature variation	$-40^\circ\text{C} \leq T_A \leq 100^\circ\text{C}$, $I_{OUT} = 100\% \text{ load}$		0.02		%/ $^\circ\text{C}$
Line regulation		$+V_S(\text{MIN})$ to $+V_S(\text{TYP})$, $I_{OUT} = 10\% \text{ load}$		10%		
		$+V_S(\text{TYP})$ to $+V_S(\text{MAX})$, $I_{OUT} = 10\% \text{ load}$		10%		
Load regulation ⁽³⁾		10% to 100% load		5%		
V_{RIPPLE}	Output voltage ripple ⁽⁴⁾	$C_{OUT} = 1\ \mu\text{F}$, $I_{OUT} = 50\%$		20		mV _{PP}
INPUT						
$+V_S$	Input voltage range		4.5		5.5	V
UVLO	$+V_S$ Undervoltage lockout	$+V_S$ increasing threshold			2.25	V
		$+V_S$ decreasing threshold	1.7			V
I_Q	Quiescent current	$I_{OUT} = 0\% \text{ load}$	DCPA10505	35		mA
			DCPA10505D	25		mA
			DCPA10512	29		mA
			DCPA10512D	36		mA
			DCPA10515	31		mA
			DCPA10515D	38		mA

(2) See Load Regulation graphs in the Typical Characterization section for typical voltage at all load conditions.

(3) Load regulation = $(V_{OUT} \text{ at } 10\% \text{ load} - V_{OUT} \text{ at } 100\% \text{ load}) / V_{OUT} \text{ at } 75\% \text{ load}$

(4) Guaranteed by design. Not production tested.

Electrical Characteristics (continued)

$T_A = 25^\circ\text{C}$, $+V_S = \text{nominal}$, $C_{IN} = 2.2 \mu\text{F}$, $C_{OUT} = 1.0 \mu\text{F}$, (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
ISOLATION								
V_{ISO}	Isolation	1-second flash test, voltage	DC	2.0 ⁽⁵⁾⁽⁴⁾			kVDC	
			AC	1.5 ⁽⁵⁾			kVrms	
		1-second flash test, leakage current				30		μA
		Continuous working voltage across isolation barrier	DC			60		VDC
			AC			42.5		VAC
		dV/dt			50		V/ms	
C_{ISO}	Barrier capacitance	$V_{ISO} = 750 \text{ Vrms}$			28		pF	
PERFORMANCE								
Efficiency		$I_{OUT} = 100\%$	DCPA10505	85%				
			DCPA10505D	85%				
			DCPA10512	87%				
			DCPA10512D	88%				
			DCPA10515	86%				
			DCPA10515D	86%				
Transient response ⁽⁴⁾		50% to 100% load step	DCPA10505	3.0%				
			DCPA10512	1.9%				
			DCPA10515	2.0%				
		50% to 100% load step per output ⁽⁶⁾	DCPA10505D	2.7%				
			DCPA10512D	2.0%				
			DCPA10515D	1.6%				
RELIABILITY								
Demonstrated		$T_A = 55^\circ\text{C}$			55		FITS	
CAPACITANCE								
C_{IN}	External input capacitance	Ceramic		2.2			μF	
C_{OUT}	External output capacitance	Ceramic		0.1	1.0	200	μF	
THERMAL SHUTDOWN								
T_{SD}	Die temperature at shutdown			168			$^\circ\text{C}$	
I_{SD}	Shutdown current			3			mA	

(5) See [Isolation Voltage](#) section for more information.

(6) Transient testing for dual output devices are tested with one output loaded with a 50% static load and the other output loaded with a 50% to 100% dynamic load step.

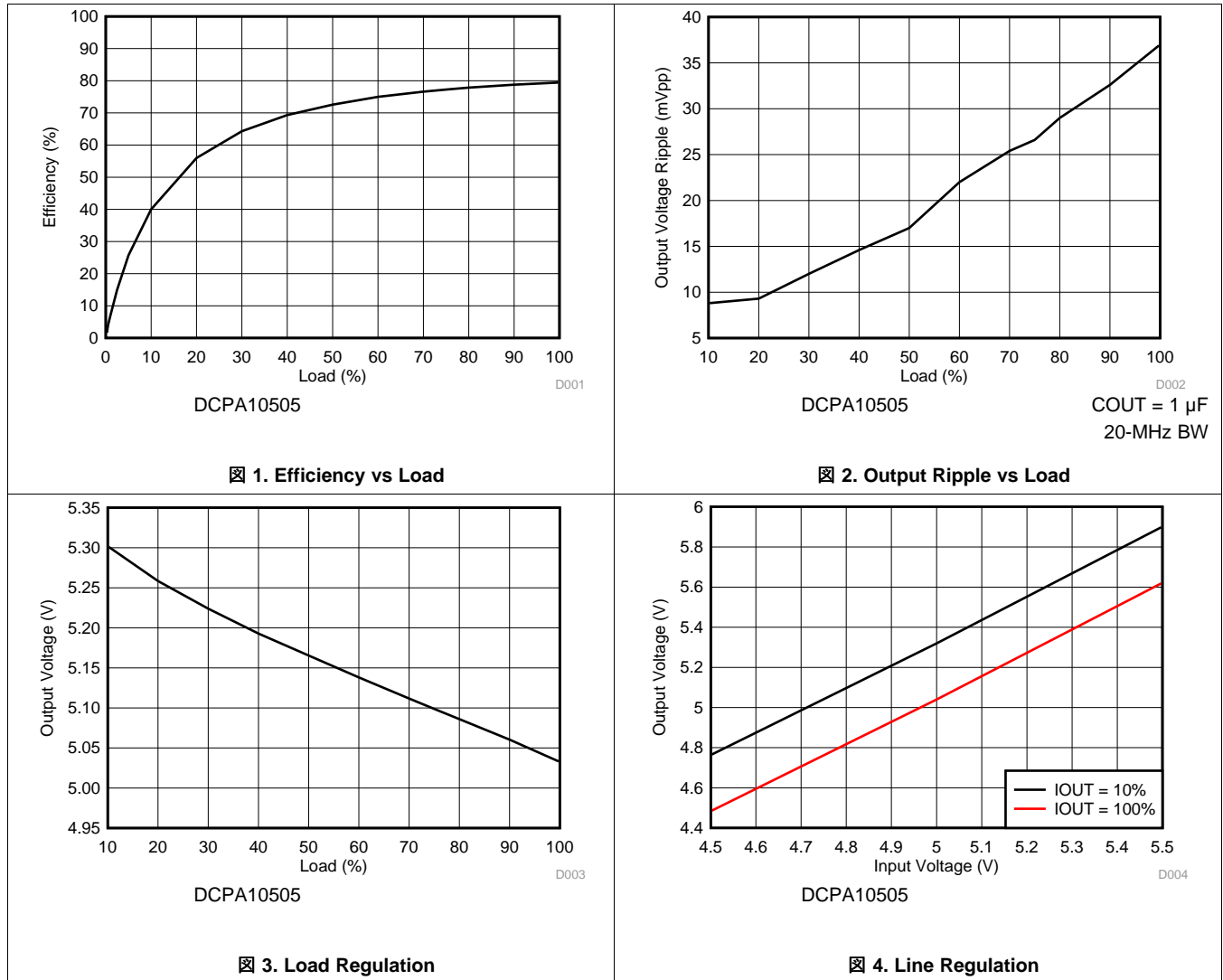
6.5 Switching Characteristics

at $T_A = +25^\circ\text{C}$, $+V_S = \text{nominal}$, $C_{IN} = 2.2 \mu\text{F}$, $C_{OUT} = 1.0 \mu\text{F}$, (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{OSC}	Oscillator frequency	$f_{SW} = f_{OSC}/2$		850			kHz
f_{SYNC}	Synchronization frequency range			750		1000	kHz
V_{IH}	High-level input threshold, $SYNC_{IN}$			0.7			V
V_{IL}	Low-level input threshold, $SYNC_{IN}$					0.3	V

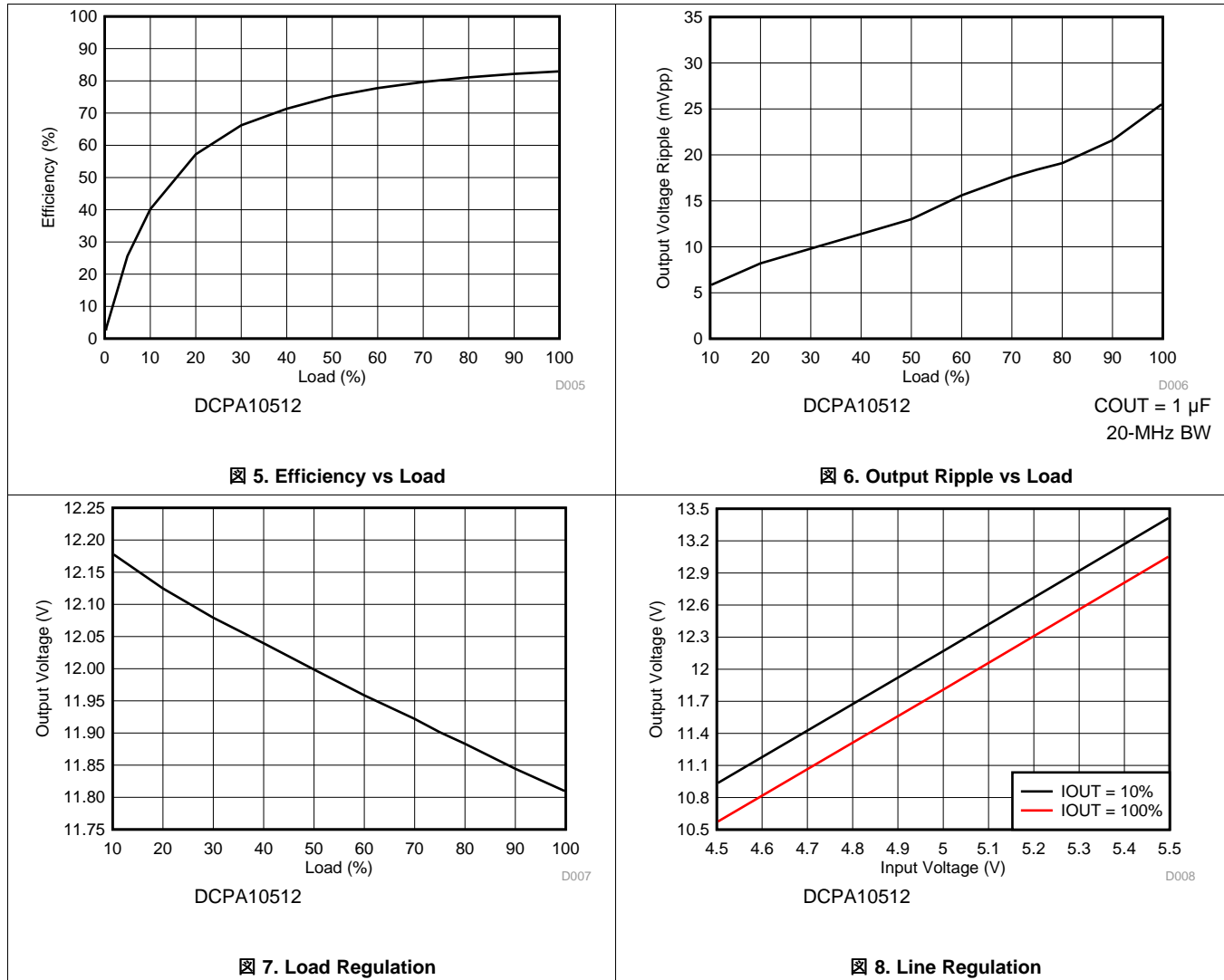
6.6 Typical Characteristics (DCPA10505)

At $T_A = 25^\circ\text{C}$, $+V_S = \text{nominal}$, (unless otherwise noted)



6.7 Typical Characteristics (DCPA10512)

At $T_A = 25^\circ\text{C}$, $+V_S = \text{nominal}$, (unless otherwise noted)



6.8 Typical Characteristics (DCPA10515)

At $T_A = 25^\circ\text{C}$, $+V_S = \text{nominal}$, (unless otherwise noted)

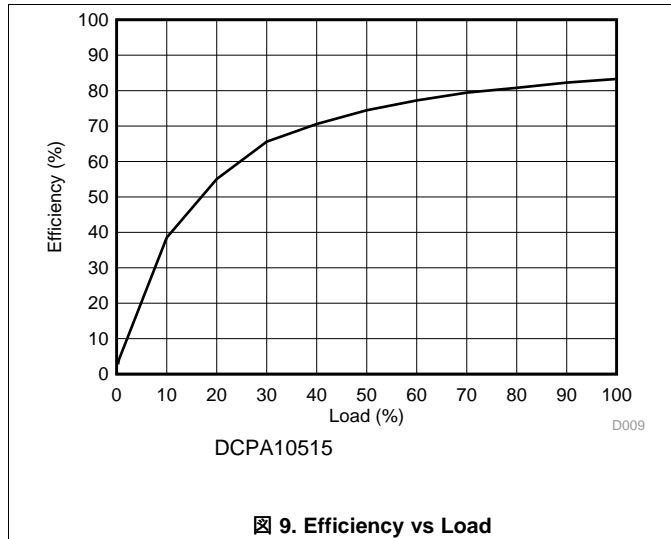


Figure 9. Efficiency vs Load

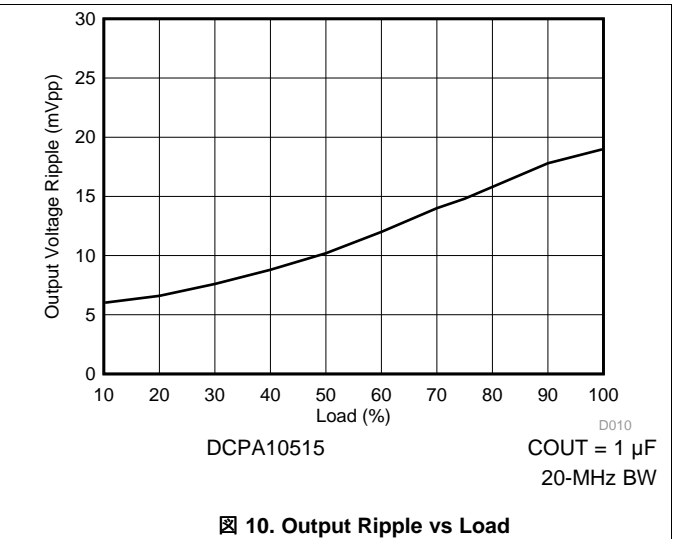


Figure 10. Output Ripple vs Load

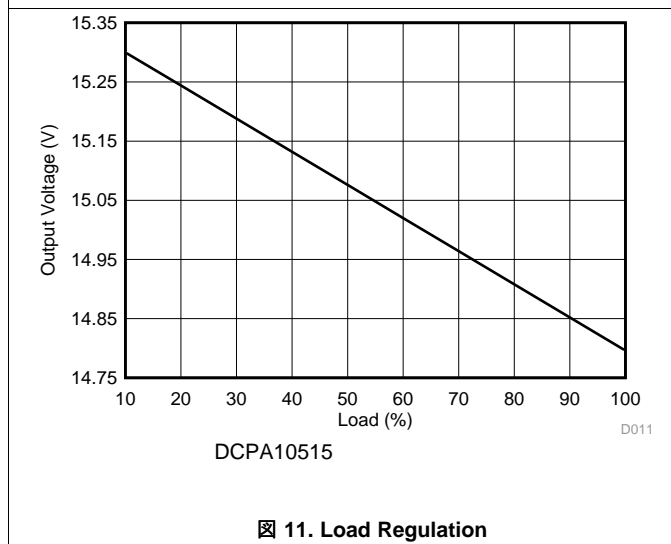


Figure 11. Load Regulation

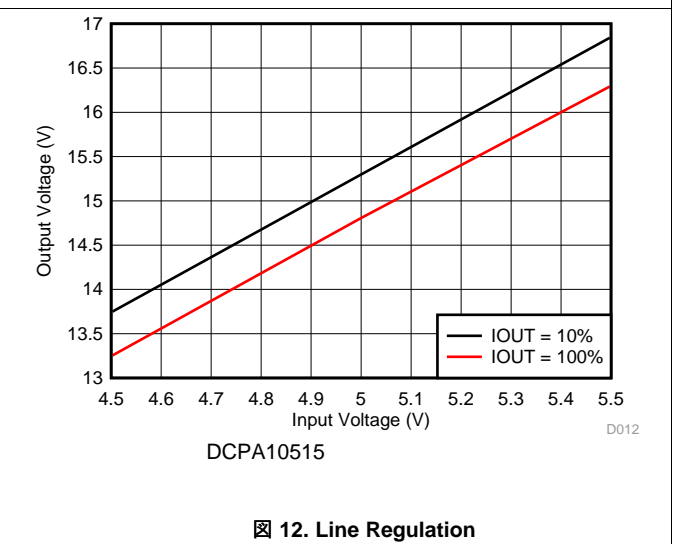
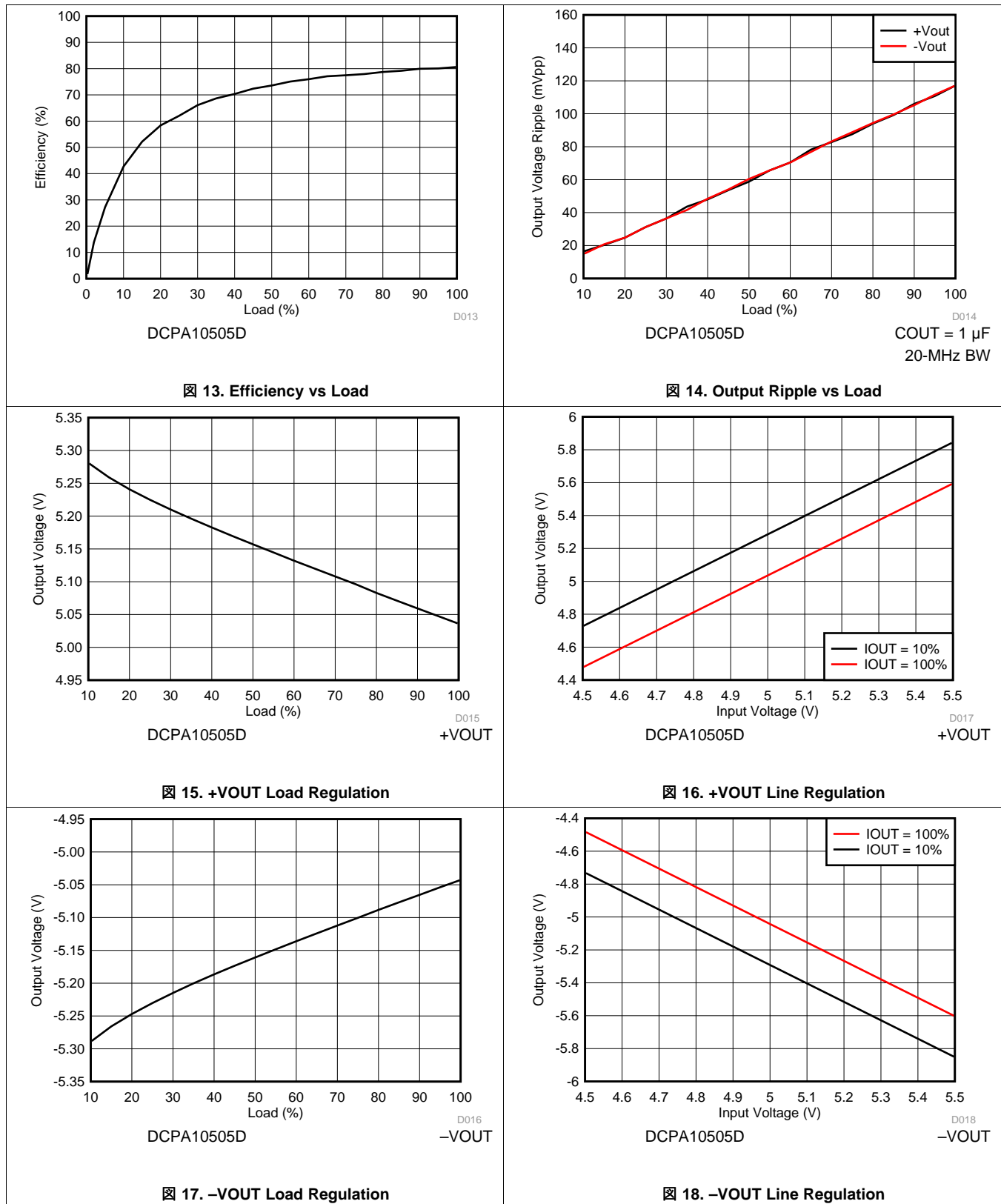


Figure 12. Line Regulation

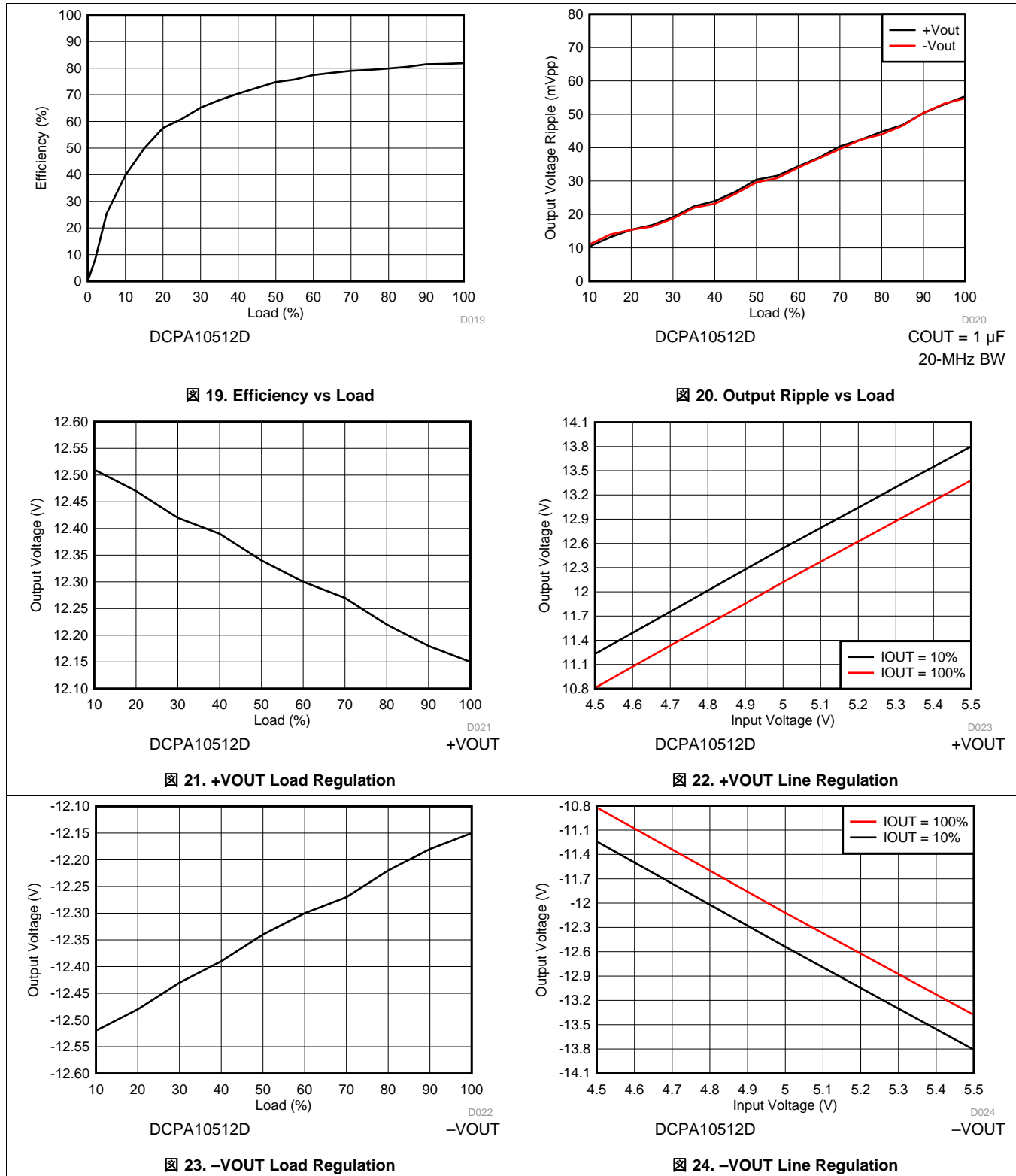
6.9 Typical Characteristics (DCPA10505D)

At $T_A = 25^\circ\text{C}$, $+V_S = \text{nominal}$, (unless otherwise noted)



6.10 Typical Characteristics (DCPA10512D)

At $T_A = 25^\circ\text{C}$, $+V_S = \text{nominal}$, (unless otherwise noted)



6.11 Typical Characteristics (DCPA10515D)

At $T_A = 25^\circ\text{C}$, $+V_S = \text{nominal}$, (unless otherwise noted)

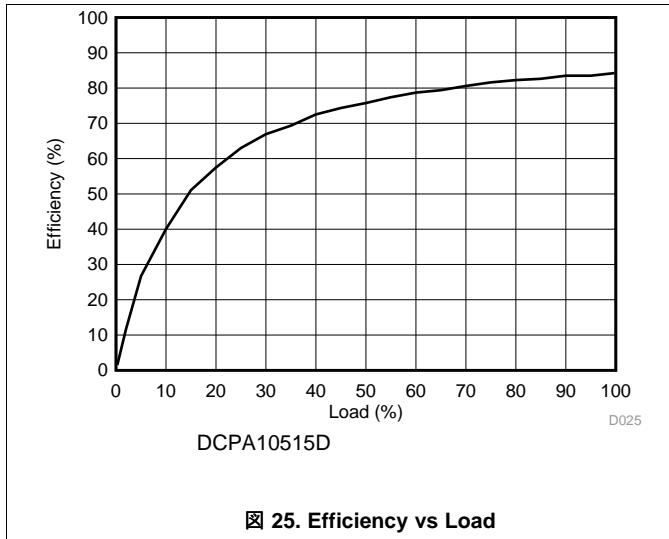


图 25. Efficiency vs Load

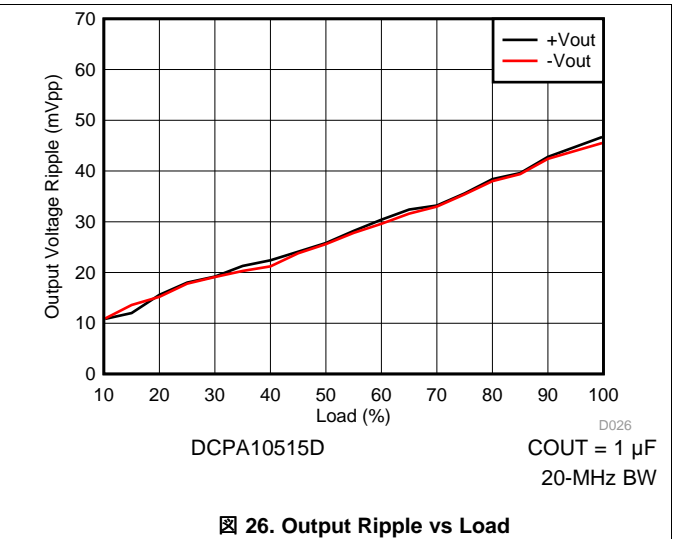


图 26. Output Ripple vs Load

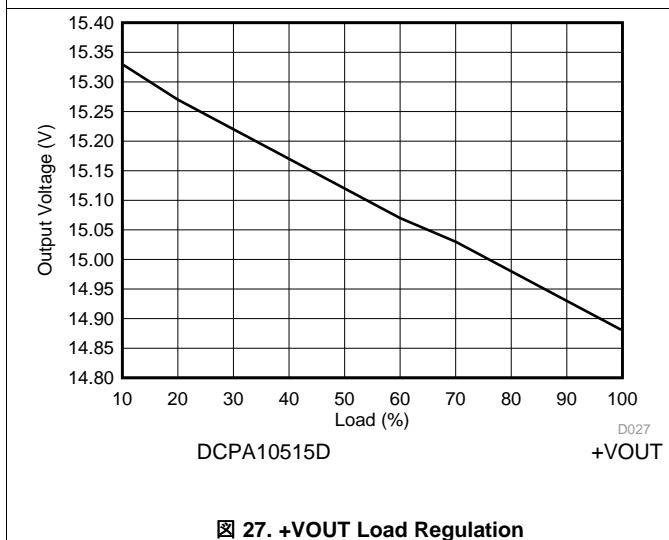


图 27. +VOUT Load Regulation

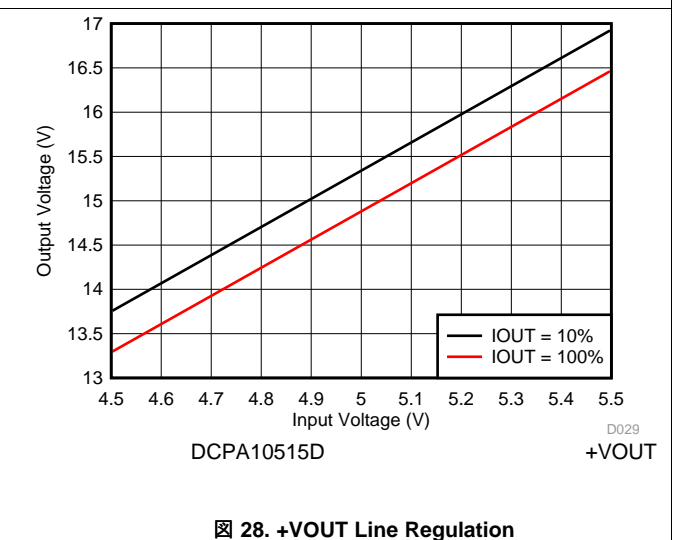


图 28. +VOUT Line Regulation

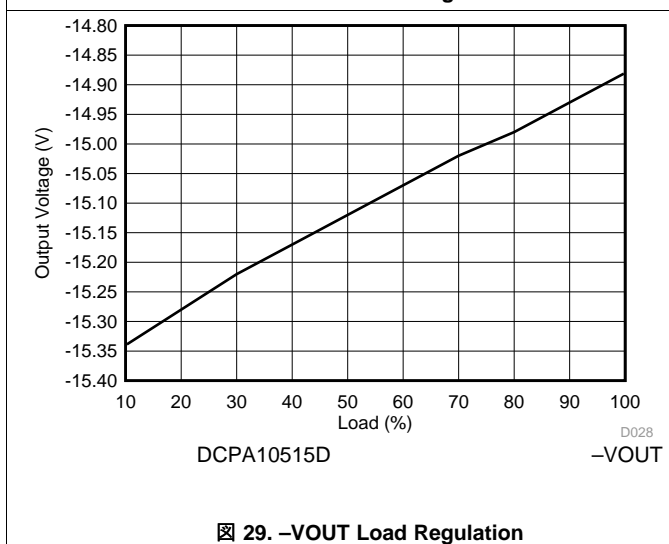


图 29. -VOUT Load Regulation

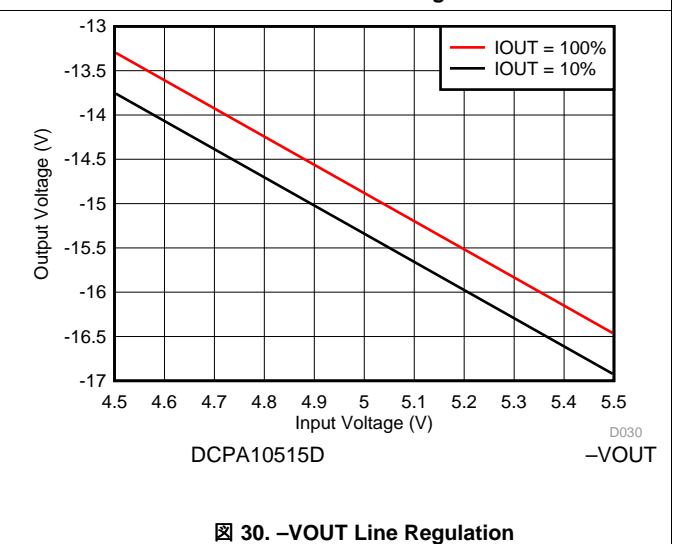


图 30. -VOUT Line Regulation

7 Detailed Description

7.1 Overview

The DCPA1 offers up to 1 W of isolated, unregulated output power from a 5-V input source with a typical efficiency of up to 87%. This efficiency is achieved through highly integrated packaging technology and the implementation of a custom power stage and control device. The DCPA1 devices are specified for operational isolation only. The circuit design uses an advanced BiCMOS and DMOS process.

7.2 Functional Block Diagrams

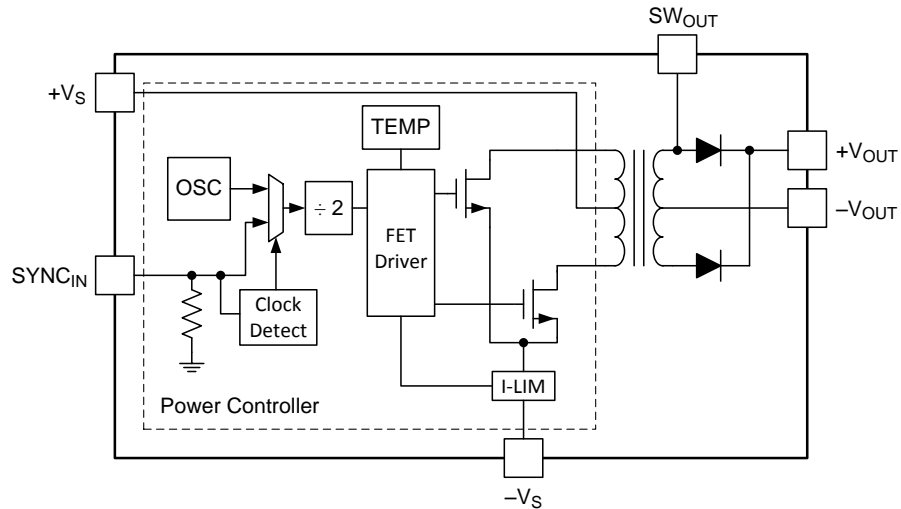


图 31. Single Output Device

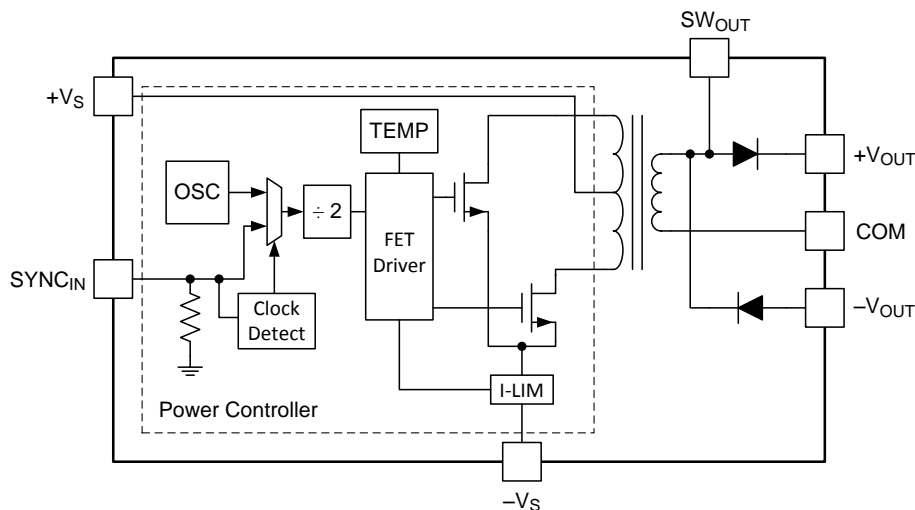


图 32. Dual Output Device

7.3 Feature Description

7.3.1 Isolation

Underwriters Laboratories, UL™ defines several classes of isolation that are used in modern power supplies.

Safety extra low voltage (SELV) is defined by UL (UL1950 E199929) as a secondary circuit which is so designated and protected that under normal and single fault conditions the voltage between any two accessible parts, or between an accessible part and the equipment earthing terminal for operational isolation does not exceed steady state 42 V peak or 60 V_{DC} for more than 1 second.

7.3.1.1 Operation or Functional Isolation

Operational or functional isolation is defined by the use of a high-potential (hipot) test only. Typically, this isolation is defined as the use of insulated wire in the construction of the transformer as the primary isolation barrier. The hipot one-second duration test (dielectric voltage, withstand test) is a production test used to verify that the isolation barrier is functioning. Products with operational isolation should never be used as an element in a safety-isolation system.

7.3.1.2 Basic or Enhanced Isolation

Basic or enhanced isolation is defined by specified creepage and clearance limits between the primary and secondary circuits of the power supply. Basic isolation is the use of an isolation barrier in addition to the insulated wire in the construction of the transformer. Input and output circuits must also be physically separated by specified distances.

7.3.1.3 Continuous Voltage

For a device that has no specific safety agency approvals (operational isolation), the continuous voltage that can be applied across the part in normal operation is less than 42.4 V_{RMS}, or 60 V_{DC}. Ensure that both input and output voltages maintain normal SELV limits. The isolation test voltage represents a measure of immunity to transient voltages.

警告

Do not use the device as an element of a safety isolation system that exceeds the SELV limit.

If the device is expected to function correctly with more than 42.4 V_{RMS} or 60 V_{DC} applied continuously across the isolation barrier, then the circuitry on both sides of the barrier must be regarded as operating at an unsafe voltage, and further isolation or insulation systems must form a barrier between these circuits and any user-accessible circuitry according to safety standard requirements.

7.3.1.4 Isolation Voltage

The terms *Hipot test*, *flash-tested*, *withstand voltage*, *proof voltage*, *dielectric withstand voltage*, and *isolation test voltage* all describe the same spec. The terms describe a test voltage applied for a specified time across a component designed to provide electrical isolation to verify the integrity of that isolation. TI's DCPA1 series of dc-dc converters are all 100% production tested at 1.5 kV_{AC} for one second.

7.3.1.5 Repeated High-Voltage Isolation Testing

Repeated high-voltage isolation testing of a barrier component can degrade the isolation capability, depending on materials, construction, and environment. The DCPA1 series of dc-dc converters have toroidal, enameled, wire isolation transformers with no additional insulation between the primary and secondary windings. While a device can be expected to withstand several times the stated test voltage, the isolation capability depends on the wire insulation. Any material, including this enamel (typically polyurethane), is susceptible to eventual chemical degradation when subject to very-high applied voltages. Therefore, strictly limit the number of high-voltage tests and repeated high-voltage isolation testing. However, if it is absolutely required, reduce the voltage by 20% from specified test voltage with a duration limit of one second per test.

Feature Description (continued)

7.3.2 Power Stage

The DCPA1 series of devices uses a push-pull, center-tapped topology. The DCPA1 devices switch at 425 kHz (divide-by-2 from an 850-kHz oscillator).

7.3.3 Input and Output Capacitors

For all DCPA1 designs, a minimum 2.2- μ F, low-ESR, ceramic input capacitor is required. Place the input capacitor as close as possible to the device input pins, $+V_S$ and $-V_S$, to ensure good startup performance.

The recommended typical output capacitance for each output of any DCPA1 device is 1.0- μ F of low-ESR, ceramic capacitance. Adding additional output capacitance will aid in ripple reduction, however, any additional capacitance will also require additional input current at start-up.

7.3.4 Oscillator And Watchdog Circuit

The onboard, 850-kHz oscillator generates the switching frequency via a divide-by-2 circuit. The oscillator can be synchronized to an external source, and is used to minimize system noise. A watchdog circuit checks the operation of the oscillator circuit.

7.3.5 Synchronization

When more than one DC/DC converter is needed onboard, beat frequencies and other electrical interference can be generated. This interference occurs because of the small variations in switching frequencies between the DC/DC converters.

The DCPA1 series of devices overcomes this interference by allowing devices to synchronize to an external clock. The $SYNC_{IN}$ pin responds to the rising edge of the external clock. If the external clock is removed, the DCPA1 will return to the frequency of the internal oscillator. If unused, it is recommended to connect this pin to the input side common, $-V_S$.

7.3.6 SW_{OUT}

The SW_{OUT} pin is directly connected to one winding of the transformer secondary prior to the output rectifier. It is not recommended to pull current from this pin. Do not connect capacitance directly to this pin as it will degrade performance. The SW_{OUT} pin is not compatible with the $SYNC_{IN}$ pin, therefore these two pins should not be connected together.

7.3.7 Soft Start

The DCPA1 series of devices includes a soft-start feature that prevents high in-rush current during power up. Once input power is applied, there is a delay of typically 10 ms before the output voltage begins to rise. Once the output voltage begins to rise, the soft start time is typically 5 ms.

7.3.8 Load Regulation

The load regulation of the DCPA1 series of devices is specified at 10% to 100% load. Operation below 10% load may cause the output voltage to increase up to 40% higher than the typical output voltage. Placing a minimum 10% load will ensure the output voltage is within the range specified in the [Electrical Characteristics](#) table.

Feature Description (continued)

7.3.9 Thermal Performance

The DCPA1 family of devices have been characterized to operate over an ambient temperature range of -40°C to $+100^{\circ}\text{C}$. The Safe Operating Area curve shown below in [Figure 33](#), represents the operating conditions of the DCPA1 devices where the maximum thermal ratings will not be exceeded. [Figure 33](#) shows that all DCPA1 devices can safely operate over the full ambient temperature range, without airflow, to the full current rating of the device.

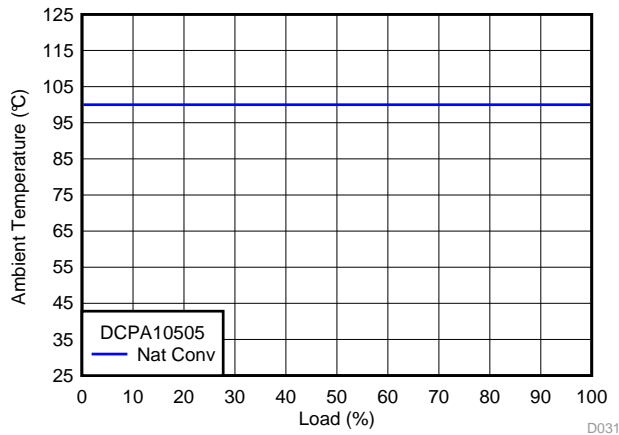


Figure 33. Thermal Safe Operating Area

7.3.9.1 Thermal Protection

The DCPA1 series of devices are protected by a thermal-shutdown circuit.

If the on-chip temperature rises above 150°C , the device shuts down. Normal operation resumes as soon as the temperature falls below 150°C . While the overtemperature condition continues, operation randomly cycles on and off. This cycling continues until the temperature is reduced.

7.3.10 Current Limit

For protection against a short circuit on the output, the DCPA1 series of devices have a built in current limit protection threshold of 1.75A (typical). These devices are not intended to be used at output currents greater than the device's output current rating as shown in the [Electrical Characteristics](#) table. Operating at currents greater than the device's current rating, but less than current limit threshold will cause excessive stress to the internal components. For protection against a partial short circuit condition, an input fuse or output fuse is recommended.

7.3.11 Construction

The basic construction of the DCPA1 series of devices is the same as standard integrated circuits. The molded package contains no substrate. The DCPA1 series of devices are constructed using an IC, rectifier diodes, and a wound magnetic toroid on a leadframe. Because the package contains no solder, the devices do not require any special printed circuit board (PCB) assembly processing. This architecture results in an isolated DC/DC converter with inherently high reliability.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Ripple Reduction

The high switching frequency of 425 kHz allows simple filtering. To reduce output voltage ripple, it is recommended that a minimum of 1- μ F capacitor be used on the +V_{OUT} pin. For dual output devices, decouple both of the outputs to the COM pin. The required 2.2- μ F, low ESR ceramic input capacitor also helps to reduce ripple and noise. See *DC-to-DC Converter Noise Reduction* (SBVA012).

8.1.2 Connecting the DCPA1 in Series

Multiple DCPA1 isolated 1-W DC/DC converters can be connected in series to provide non-standard voltage rails. This configuration is possible by using the floating outputs provided by the galvanic isolation of the DCPA1 devices by connecting the +V_{OUT} from one DCPA1 to the -V_{OUT} of another as shown in [Figure 34](#). The synchronization feature allows easy synchronization to prevent power-rail beat frequencies at no additional filtering cost.

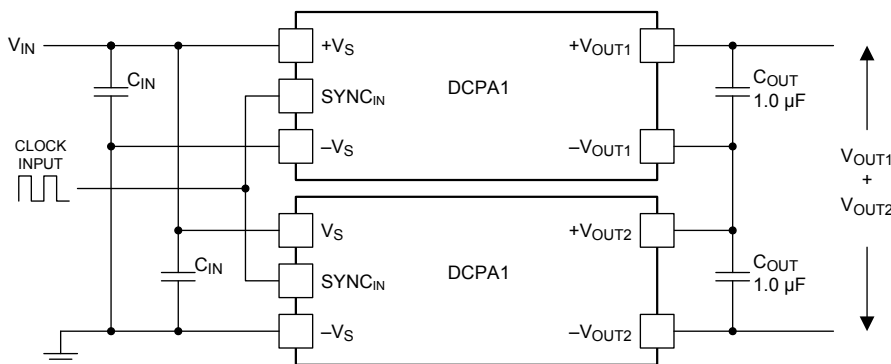


Figure 34. Multiple DCPA1 Devices Connected in Series

The outputs of a dual-output DCPA1 device can also be connected in series to provide two times the magnitude of +V_{OUT}, as shown in [Figure 35](#). For example, connect a dual-output, ± 15 -V, DCPA10515D device to provide a 30-V rail.

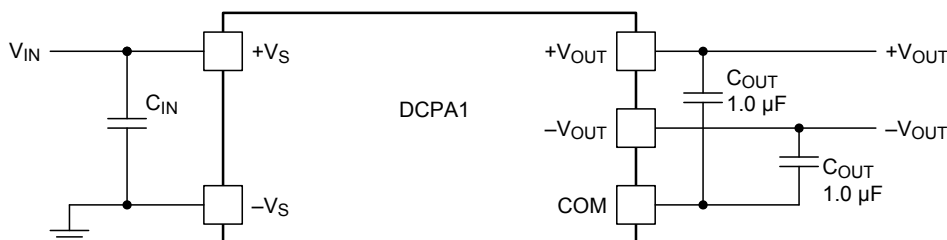


Figure 35. Dual Output Devices Connected in Series

8.1.3 Connecting the DCPA1 in Parallel

If the output power from one DCPA1 is not sufficient, it is possible to parallel the outputs of multiple DCPA1s, as shown in [Figure 36](#), (applies to single output devices only). The synchronization feature allows easy synchronization to prevent power-rail beat frequencies at no additional filtering cost.

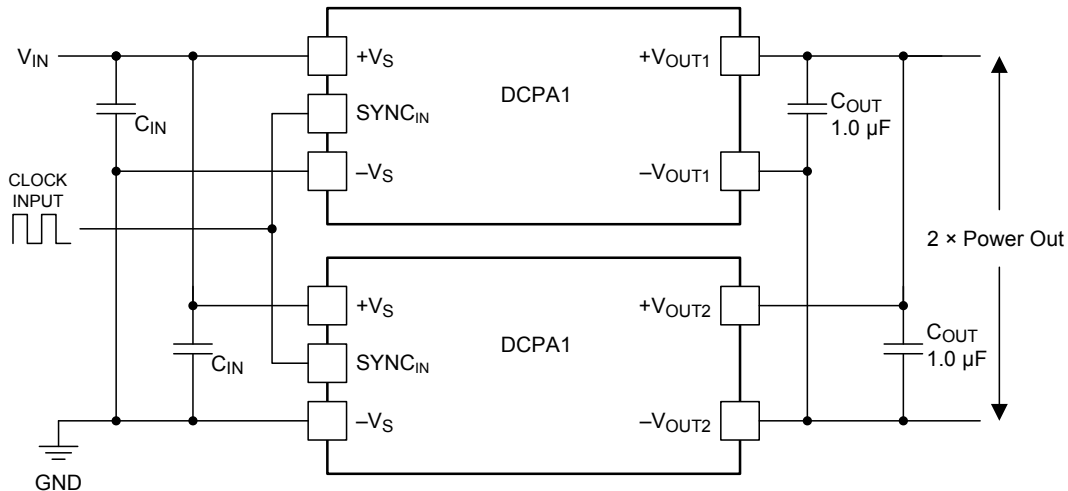


Figure 36. Multiple DCPA1 Devices Connected in Parallel

8.2 Typical Application

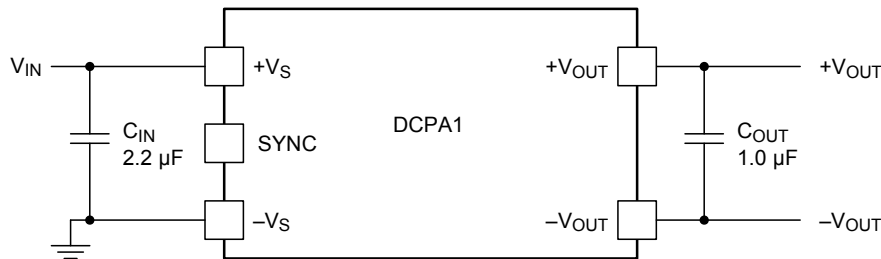


Figure 37. Typical DCPA10505 Application

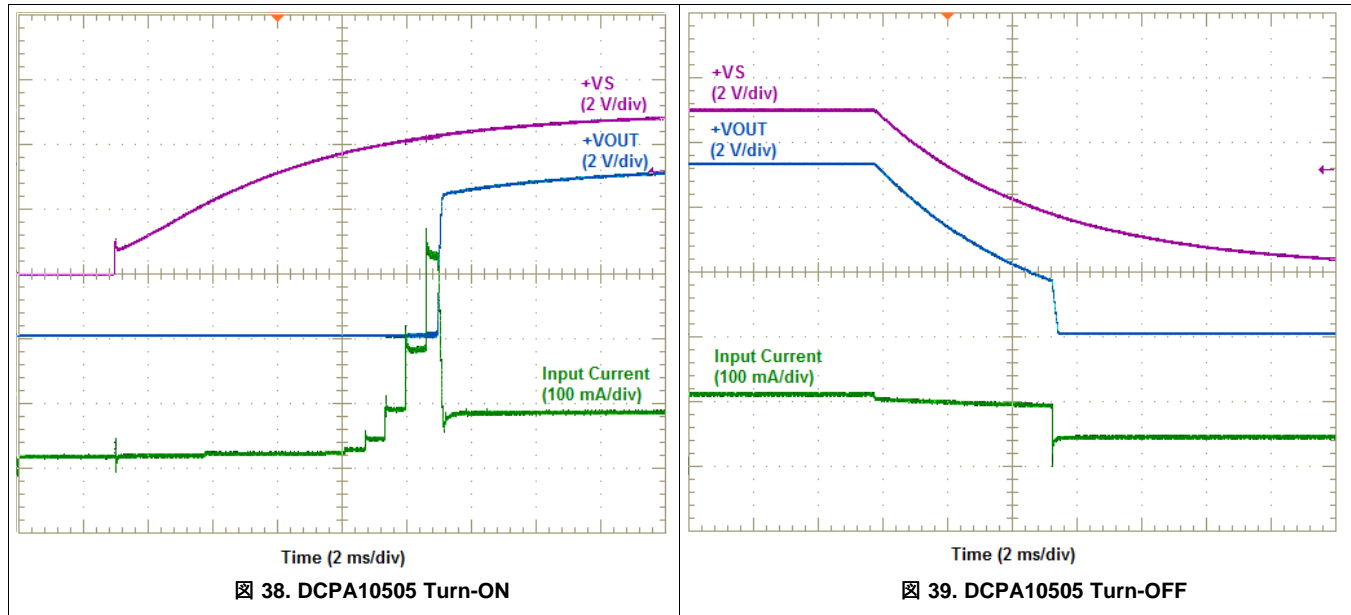
8.2.1 Design Requirements

For this design example, use the parameters listed in [Table 1](#) and follow the design procedures shown in [Detailed Design Procedure](#) section.

Table 1. Design Example Parameters

PARAMETER		VALUE	UNIT
$V_{(+VS)}$	Input voltage	5	V
$V_{(+VOUT)}$	Output voltage	5	V
I_{OUT}	Output current rating	200	mA
f_{SW}	Operating frequency	425	kHz

8.2.2 DCPA10505 Application Curves



8.2.3 Detailed Design Procedure

8.2.3.1 Input Capacitor

For all DCPA1, 5-V input voltage designs, select a 2.2- μ F low-ESR ceramic input capacitor to ensure a good startup performance.

8.2.3.2 Output Capacitor

For any DCPA1 design, select a 1.0- μ F low-ESR ceramic output capacitor to reduce output ripple.

8.2.3.3 SYNC_{IN} Pin

In a stand-alone application, it is recommended to connect this pin to the input side common, $-V_S$.

8.2.4 PCB Design

The copper losses (resistance and inductance) can be minimized by the use of mutual ground and power planes where possible. If that is not possible, use wide traces to reduce the losses. If several devices are being powered from a common power source, a star-connected system for the traces must be deployed. Do not connect the devices in series, because that type of connection cascades the resistive losses. The position of the decoupling capacitors is important. They must be as close to the devices as possible in order to reduce losses. See the [PCB Layout](#) section for more details.

9 Power Supply Recommendations

The DCPA1 is a switching power supply, and as such can place high peak current demands on the input supply. In order to avoid the supply falling momentarily during the fast switching pulses, ground and power planes should be used to connect the power to the input of DCPA1 device. If this connection is not possible, then the supplies must be connected in a star formation with the traces made as wide as possible.

10 Layout

10.1 Layout Guidelines

Due to the high power density of these devices, provide ground planes on the input and output rails.

Figure 40 shows the schematic for a single output DCPA1 device. Figure 40 illustrates a printed circuit board (PCB) layout for the schematics.

Including input power and ground planes provides a low-impedance path for the input power. For the output, the COM signal connects via a ground plane, while the connections for the positive and negative voltage outputs conduct via wide traces in order to minimize losses.

The output should be taken from the device using ground and power planes, thereby ensuring minimum losses.

The location of the decoupling capacitors in close proximity to their respective pins ensures low losses due to the effects of stray inductance, thus improving the ripple performance. This location is of particular importance to the input decoupling capacitor, because this capacitor supplies the transient current associated with the fast switching waveforms of the power drive circuits.

If the SYNC_{IN} pin is unused, it is recommended to connect this pin to the input side common, $-V_S$. Allow the SW_{OUT} pin, to remain configured as a floating pad.

10.2 Layout Example

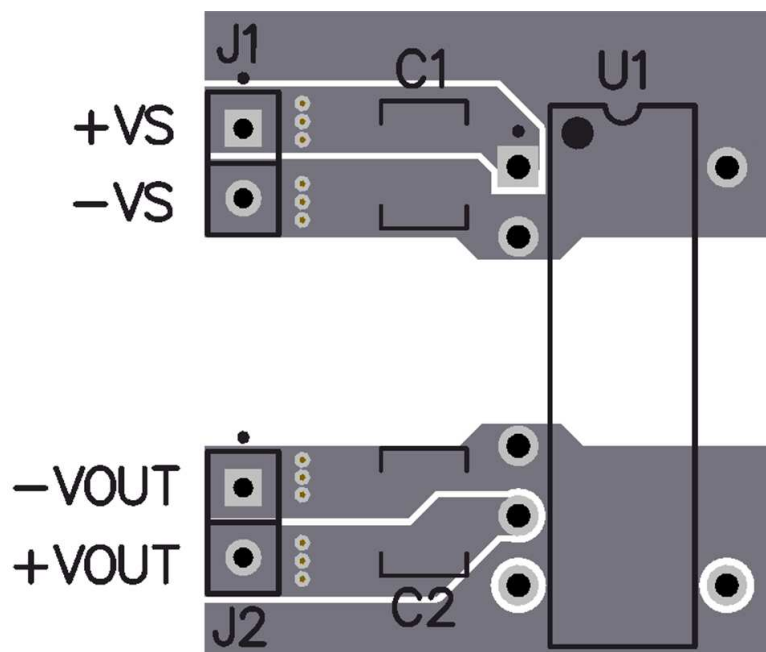


Figure 40. Typical Layout

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 デバイスの項目表記

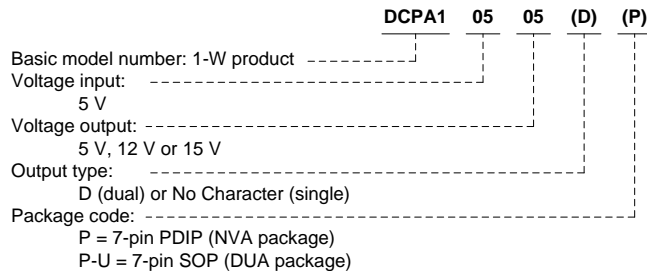


図 41. 製品情報の補足

11.2 ドキュメントのサポート

11.2.1 関連資料

『DC/DCコンバータのノイズ低減』(SBVA012)

『DCP01/02シリーズDC/DCコンバータの外部同期』(SBAA035)

『DCP01/02シリーズDC/DCコンバータの性能最適化』(SBVA013)

11.3 コミュニティ・リソース

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11.4 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 2. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
DCPA10505	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
DCPA10505D	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
DCPA10512	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
DCPA10512D	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
DCPA10515	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
DCPA10515D	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

11.5 商標

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11.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DCPA10505DP	ACTIVE	PDIP	NVA	7	25	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 100	DCPA10505DP	Samples
DCPA10505DP-U/700	ACTIVE	SOP	DUA	7	700	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 100	DCPA10505DP-U	Samples
DCPA10505P	ACTIVE	PDIP	NVA	7	25	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 100	DCPA10505P	Samples
DCPA10505P-U/700	ACTIVE	SOP	DUA	7	700	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 100	DCPA10505P-U	Samples
DCPA10512DP	ACTIVE	PDIP	NVA	7	25	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 100	DCPA10512DP	Samples
DCPA10512DP-U/700	ACTIVE	SOP	DUA	7	700	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 100	DCPA10512DP-U	Samples
DCPA10512P	ACTIVE	PDIP	NVA	7	25	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 100	DCPA10512P	Samples
DCPA10512P-U/700	ACTIVE	SOP	DUA	7	700	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 100	DCPA10512P-U	Samples
DCPA10515DP	ACTIVE	PDIP	NVA	7	25	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 100	DCPA10515DP	Samples
DCPA10515DP-U/700	ACTIVE	SOP	DUA	7	700	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 100	DCPA10515DP-U	Samples
DCPA10515P	ACTIVE	PDIP	NVA	7	25	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 100	DCPA10515P	Samples
DCPA10515P-U/700	ACTIVE	SOP	DUA	7	700	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 100	DCPA10515P-U	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

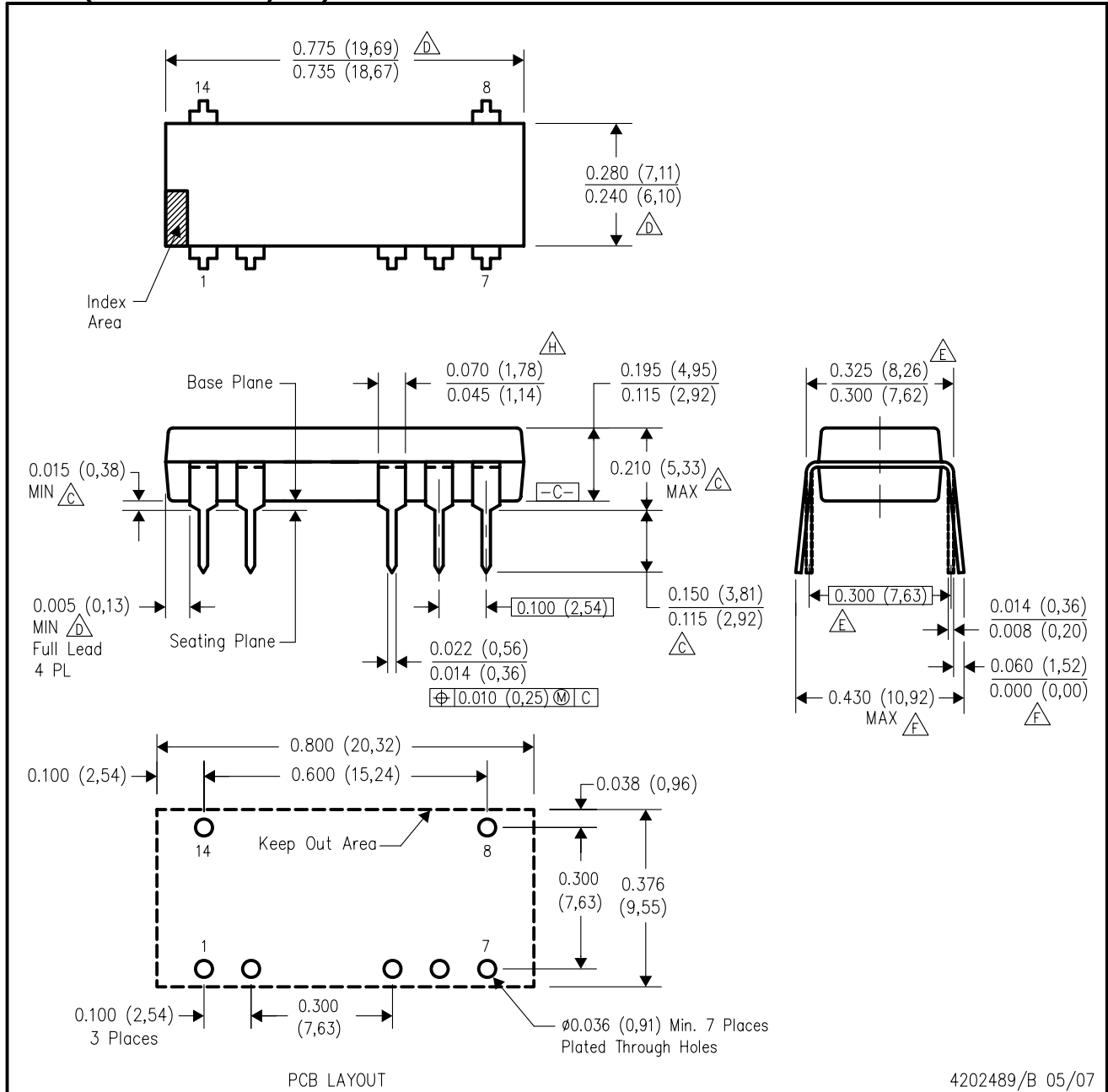
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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NVA (R-PDIP-T7/14)

PLASTIC DUAL-IN-LINE

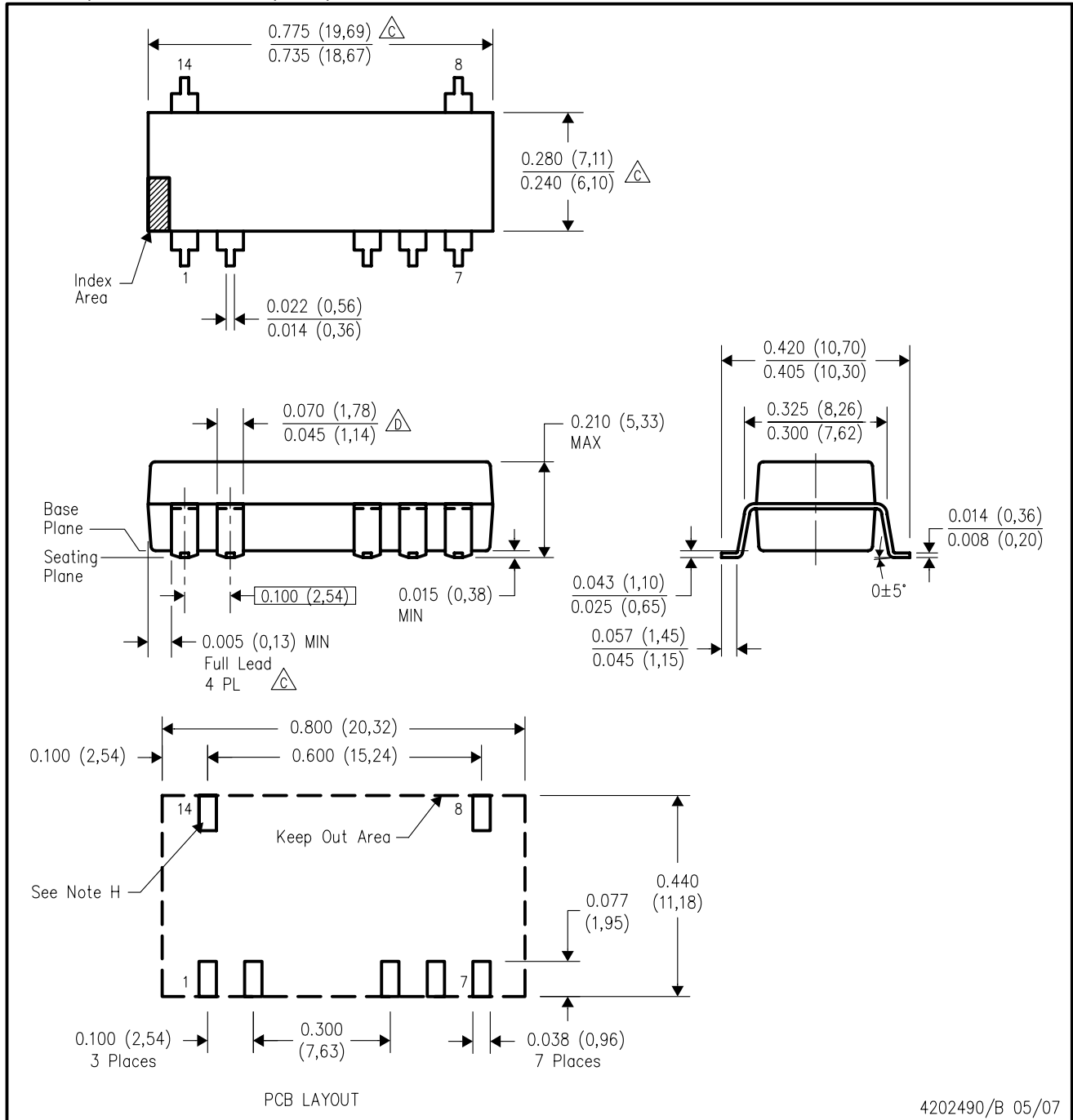


4202489/B 05/07

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Dimensions are measured with the package seated in JEDEC seating plane gauge GS-3.
 - D. Dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 (0,25).
 - E. Dimensions measured with the leads constrained to be perpendicular to Datum C.
 - F. Dimensions are measured at the lead tips with the leads unconstrained.
 - G. Pointed or rounded lead tips are preferred to ease insertion.
 - H. Lead shoulder maximum dimension does not include dambar protrusions. Dambar protrusions shall not exceed 0.010 (0,25).
 - I. Distance between leads including dambar protrusions to be 0.005 (0,13) minimum.
 - J. A visual index feature must be located within the cross-hatched area.
 - K. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.
 - L. Falls within JEDEC MS-001-AA.

DUA (R-PDSO-G7/14)

PLASTIC SMALL-OUTLINE



4202490/B 05/07

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 (0,25).
 - D. Lead shoulder maximum dimension does not include dambar protrusions. Dambar protrusions shall not exceed 0.010 (0,25).
 - E. Distance between leads including dambar protrusions to be 0.005 (0,13) minimum.
 - F. A visual index feature must be located within the cross-hatched area.
 - G. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.
 - H. Power pin connections should be two or more vias per input, ground and output pin.

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