DLP550JE 0.55 XGA デジタル・マイクロミラー・デバイス

1 特長

- 対角 0.55 インチ (16.5mm) のマイクロミラー・アレイ
  - XGA (1024 × 768)
  - 10.8 ミクロンのマイクロミラー・ピッチ
  - マイクロミラーの傾斜角 ±12° (フラット状態に対して)
  - コーナー照明
- 2×LVDS 入力データ・バス
- DLP550JE チップセットの構成部品:
  - DLP470TE DMD
  - DLPC4430 コントローラ
  - DLPA100 コントローラ・パワー・マネージメントおよびモーター・ドライバ IC
  - DLPA200

2 アプリケーション

- デジタル・サイネージ
- 教育機関向けプロジェクタ
- 企業向けプロジェクタ

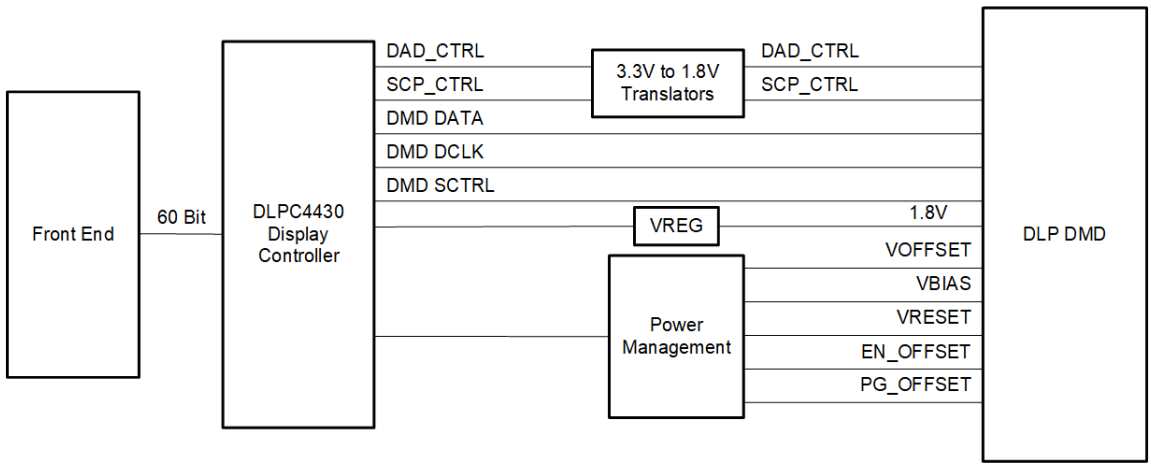
3 概要

TI DLP550JE デジタル・マイクロミラー・デバイス (DMD) は、デジタル制御型の MEMS (Micro-ElectroMechanical System) 空間光変調器 (SLM) で、色鮮やかな DLP® 0.55 XGA ディスプレイ・ソリューションを低コストで実現します。DLP550JE DMD を DLPC4430 ディスプレイ・コントローラ、DLPA100 電源およびモーター・ドライバ、DLPA200 DMD マイクロミラー・ドライバと組み合わせることで、高性能なシステムとなり、4:3 のアスペクト比、高輝度、システムの単純性を必要とするディスプレイ・アプリケーションに最適です。

製品情報

部品番号	パッケージ (1)	本体サイズ (公称)
DLP550JE	FYA (149)	32.20mm × 22.30mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



DLP550JE のアプリケーション概略図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (September 2022) to Revision B (February 2023) **Page**

- コントローラを DLPC4430 に更新、すべてのチップセット・コンポーネントへのリンクが正常に動作 ... 1
- コントローラを DLPC4430 に更新し、DMD をドキュメントにリンク ... 1
- Updated this section ... 25
- Updated controller to DLPC4430, updated the application diagram ... 25
- Updated controller to DLPC4430 ... 26
- Updated controller to DLPC4430 ... 28

Changes from Revision * (November 2017) to Revision A (September 2022) **Page**

- 文書全体にわたって表、図、相互参照の採番方法を更新 ... 1
- ドキュメントのステータスを「事前情報」から「量産データ」に変更 ... 1
- 用語を更新し、「MOEMS」を「MEMS」に置き換え ... 1
- 製品情報で、本体サイズ (公称値) を整理 ... 1
- Updated wording in "Input Voltages" in セクション 6.1 ... 7

5 Pin Configuration and Functions

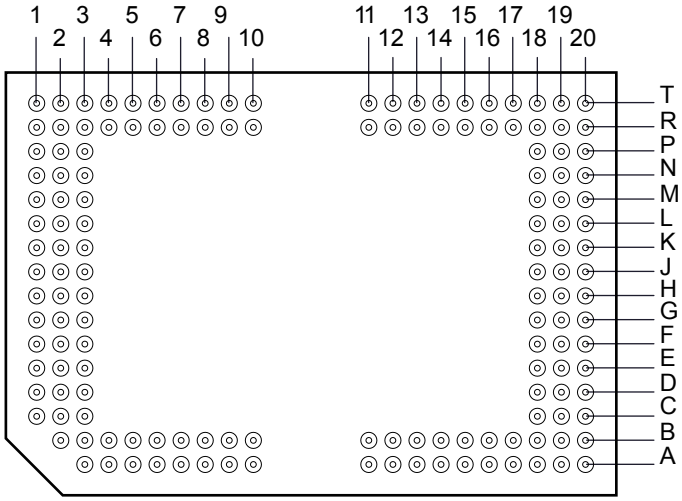


図 5-1. FYA Package 149-Pin Bottom View

表 5-1. Pin Functions

PIN[1]		TYPE (I/O/P)	SIGNAL	DATA RATE[2]	INTERNAL TERM[3]	CLOCK	DESCRIPTION	TRACE (mils)[4]
NAME	NO.							
DATA INPUTS								
D_AN1	G20	Input	LVCMOS	DDR	Differential	DCLK_A	Input data bus A (LVDS)	760.78
D_AP1	H20	Input	LVCMOS	DDR	Differential	DCLK_A		760.86
D_AN3	H19	Input	LVCMOS	DDR	Differential	DCLK_A		760.73
D_AP3	G19	Input	LVCMOS	DDR	Differential	DCLK_A		760.76
D_AN5	F18	Input	LVCMOS	DDR	Differential	DCLK_A		760.73
D_AP5	G18	Input	LVCMOS	DDR	Differential	DCLK_A		760.81
D_AN7	E18	Input	LVCMOS	DDR	Differential	DCLK_A		760.77
D_AP7	D18	Input	LVCMOS	DDR	Differential	DCLK_A		760.81
D_AN9	C20	Input	LVCMOS	DDR	Differential	DCLK_A		760.67
D_AP9	D20	Input	LVCMOS	DDR	Differential	DCLK_A		760.74
D_AN11	B18	Input	LVCMOS	DDR	Differential	DCLK_A		760.68
D_AP11	A18	Input	LVCMOS	DDR	Differential	DCLK_A		760.77
D_AN13	A20	Input	LVCMOS	DDR	Differential	DCLK_A		760.82
D_AP13	B20	Input	LVCMOS	DDR	Differential	DCLK_A		760.77
D_AN15	B19	Input	LVCMOS	DDR	Differential	DCLK_A		760.79
D_AP15	A19	Input	LVCMOS	DDR	Differential	DCLK_A		760.75

表 5-1. Pin Functions (continued)

PIN[1]		TYPE (I/O/P)	SIGNAL	DATA RATE[2]	INTERNAL TERM[3]	CLOCK	DESCRIPTION	TRACE (mils)[4]
NAME	NO.							
D_BN1	K20	Input	LVCMOS	DDR	Differential	DCLK_B	Input data bus B (LVDS)	760.72
D_BP1	J20	Input	LVCMOS	DDR	Differential	DCLK_B		760.80
D_BN3	J19	Input	LVCMOS	DDR	Differential	DCLK_B		760.79
D_BP3	K19	Input	LVCMOS	DDR	Differential	DCLK_B		760.82
D_BN5	L18	Input	LVCMOS	DDR	Differential	DCLK_B		760.77
D_BP5	K18	Input	LVCMOS	DDR	Differential	DCLK_B		760.85
D_BN7	M18	Input	LVCMOS	DDR	Differential	DCLK_B		760.78
D_BP7	N18	Input	LVCMOS	DDR	Differential	DCLK_B		760.81
D_BN9	P20	Input	LVCMOS	DDR	Differential	DCLK_B		760.76
D_BP9	N20	Input	LVCMOS	DDR	Differential	DCLK_B		760.83
D_BN11	R18	Input	LVCMOS	DDR	Differential	DCLK_B		760.78
D_BP11	T18	Input	LVCMOS	DDR	Differential	DCLK_B		760.80
D_BN13	T20	Input	LVCMOS	DDR	Differential	DCLK_B		760.78
D_BP13	R20	Input	LVCMOS	DDR	Differential	DCLK_B		760.72
D_BN15	R19	Input	LVCMOS	DDR	Differential	DCLK_B		760.80
D_BP15	T19	Input	LVCMOS	DDR	Differential	DCLK_B		760.77
DCLK_AN	D19	Input	LVCMOS	—	Differential	—	Input data bus A Clock (LVDS)	760.73
DCLK_AP	E19	Input	LVCMOS	—	Differential	—		760.80
DCLK_BN	N19	Input	LVCMOS	—	Differential	—	Input data bus B Clock (LVDS)	760.72
DCLK_BP	M19	Input	LVCMOS	—	Differential	—		760.80
DATA CONTROL INPUTS								
SCTRL_AN	F20	Input	LVCMOS	DDR	Differential	DCLK_A	Data Control (LVDS)	760.74
SCTRL_AP	E20	Input	LVCMOS	DDR	Differential	DCLK_A		760.70
SCTRL_BN	L20	Input	LVCMOS	DDR	Differential	DCLK_B		760.83
SCTRL_BP	M20	Input	LVCMOS	DDR	Differential	DCLK_B		760.78
SERIAL COMMUNICATION (SCP) AND CONFIGURATION								
SCP_CLK	A8	Input	LVCMOS	—	Pulldown	—		—
SCP_DO	A9	Output	LVCMOS	—	—	SCP_CLK		—
SCP_DI	A5	Input	LVCMOS	—	Pulldown	SCP_CLK		—
$\overline{\text{SCP\_EN}}$	B7	Input	LVCMOS	—	Pulldown	SCP_CLK		—
$\overline{\text{PWRDN}}$	B9	Input	LVCMOS	—	Pulldown	—		—
MICROMIRROR BIAS CLOCKING PULSE								
MODE_A	A4	Input	LVCMOS	—	Pulldown	—		—

表 5-1. Pin Functions (continued)

PIN[1]		TYPE (I/O/P)	SIGNAL	DATA RATE[2]	INTERNAL TERM[3]	CLOCK	DESCRIPTION	TRACE (mils)[4]
NAME	NO.							
MBRST0	C3	Input	Analog	—	—	—	Micromirror Bias Clocking Pulse "MBRST" signals "clock" micromirrors into state of LVCMOS memory cell associated with each mirror.	—
MBRST1	D2	Input	Analog	—	—	—		—
MBRST2	D3	Input	Analog	—	—	—		—
MBRST3	E2	Input	Analog	—	—	—		—
MBRST4	G3	Input	Analog	—	—	—		—
MBRST5	E1	Input	Analog	—	—	—		—
MBRST6	G2	Input	Analog	—	—	—		—
MBRST7	G1	Input	Analog	—	—	—		—
MBRST8	N3	Input	Analog	—	—	—		—
MBRST9	M2	Input	Analog	—	—	—		—
MBRST10	M3	Input	Analog	—	—	—		—
MBRST11	L2	Input	Analog	—	—	—		—
MBRST12	J3	Input	Analog	—	—	—		—
MBRST13	L1	Input	Analog	—	—	—		—
MBRST14	J2	Input	Analog	—	—	—		—
MBRST15	J1	Input	Analog	—	—	—		—

表 5-1. Pin Functions (continued)

PIN[1]		TYPE (I/O/P)	SIGNAL	DATA RATE[2]	INTERNAL TERM[3]	CLOCK	DESCRIPTION	TRACE (mils)[4]
NAME	NO.							
POWER								
V_{CC}	B11, B12, B13, B16, R12, R13, R16, R17	Power	Analog	—	—	—	Power for LVCMOS Logic	—
V_{CCI}	A12, A14, A16, T12, T14, T16	Power	Analog	—	—	—	Power supply for LVDS Interface	—
V_{OFFSET}	C1, D1, M1, N1	Power	Analog	—	—	—	Power for High Voltage CMOS Logic	—
V_{SS}	A6, A11, A13, A15, A17, B4, B5, B8, B14, B15, B17, C2, C18, C19, F1, F2, F19, H1, H2, H3, H18, J18, K1, K2, L19, N2, P18, P19, R4, R9, R14, R15, T7, T13, T15, T17	Power	Analog	—	—	—	Common return for all power inputs	—
RESERVED SIGNALS (Not for use in system)								
RESERVED_FC	R7	Input	LVCMOS	—	Pulldown	—	Pins should be connected to V_{SS}.	—
RESERVED_FD	R8	Input	LVCMOS	—	Pulldown	—		—
RESERVED_PFE	T8	Input	LVCMOS	—	Pulldown	—		—
RESERVED_STM	B6	Input	LVCMOS	—	Pulldown	—		—
NO_CONNECT	A3, A7, A10, B2, B3, B10, E3, F3, K3, L3, P1, P2, P3, R1, R2, R3, R5, R6, R10, R11, T1, T2, T3, T4, T5, T6, T9, T10, T11	—	—	—	—	—	Do not connect.	—

(1) The following power supplies are required to operate the DMD: V_{CC}, V_{CCI}, V_{OFFSET}. V_{SS} must also be connected.
(2) DDR = Double Data Rate. SDR = Single Data Rate. Refer to the *Timing Requirements* for specifications and relationships.
(3) Refer to *Electrical Characteristics* for differential termination specification.
(4) Internal Trace Length (mils) refers to the Package electrical trace length. See the *DLP 0.55 XGA Chip-Set Data Manual* for details regarding signal integrity considerations for end-equipment designs.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted).(7)

		MIN	MAX	UNIT
SUPPLY VOLTAGES				
V_{CC}	Supply voltage for LVCMOS core logic(1)	–0.5	4	V
V_{CCI}	Supply voltage for LVDS Interface(1)	–0.5	4	V
V_{OFFSET}	Micromirror Electrode and HVCMOS voltage(1) (2)	–0.5	9	V
V_{MBRST}	Voltage applied to MBRST[0:15] Input Pins	–28	28	V
$\lvert V_{CC} - V_{CCI} \rvert$	Supply voltage change(3)		0.3	V
INPUT VOLTAGES				
	Input voltage for all other input pins(1)	–0.5	V_{CC} + 0.3	V
$\lvert V_{ID} \rvert$	Input differential voltage (absolute value) (4)		700	mV
CLOCKS				
f_{clock}	Clock frequency for LVDS interface, DCLK_A		400	MHz
f_{clock}	Clock frequency for LVDS interface, DCLK_B		400	MHz
ENVIRONMENTAL				
T_{ARRAY} and T_{WINDOW}	Temperature, operating(5)	0	90	°C
	Temperature, non-operating (5)	–40	90	°C
$\lvert T_{DELTA} \rvert$	Absolute Temperature delta between any point on the window edge and the ceramic test point TP1(6)		30	°C
T_{DP}	Dew Point Temperature, operating and non-operating (non-condensing)		81	°C

(1) All voltages are referenced to common ground V_{SS}. Voltages V_{CC}, V_{CCI}, and V_{OFFSET} are required for proper DMD operation. V_{SS} must also be connected.
(2) V_{OFFSET} supply transients must fall within specified voltages.
(3) Exceeding the recommended allowable absolute voltage difference between V_{CC} and V_{CCI} may result in excess current draw.
(4) This maximum LVDS input voltage rating applies when each input of a differential pair is at the same voltage potential.
(5) The highest temperature of the active array (as calculated by the セクション 7.4) or of any point along the Window Edge as defined in 図 7-1. The locations of thermal test points TP2, TP3, TP4, and TP5 in 図 7-1 are intended to measure the highest window edge temperature. If a particular application causes another point on the window edge to be at a higher temperature, that point should be used.
(6) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in 図 7-1. The window test points TP2, TP3, TP4, and TP5 shown in 図 7-1 are intended to result in the worst-case delta. If a particular application causes another point on the window edge to result in a larger delta temperature, that point should be used.
(7) Stresses beyond those listed under セクション 6.1 may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under セクション 6.4. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 Storage Conditions

Applicable for the DMD as a component or non-operational in a system.

		MIN	MAX	UNIT
T_{DMD}	DMD storage temperature	–40	80	°C
T_{DP-AVG}	Average dew point temperature (non-condensing)(1)		28	°C
T_{DP-ELR}	Elevated dew point temperature range (non-condensing)(2)	28	36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range		24	Months

(1) The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.
(2) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of CT_{ELR}.

6.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins except MBRST(15:0)	±2000	V
		Pins MBRST(15:0)	<250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.4 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by this table. No level of performance is implied when operating the device above or below these limits.

		MIN	NOM	MAX	UNIT
VOLTAGE SUPPLY					
V_{CC}	Supply voltage for LVCMOS core logic(1)	3.0	3.3	3.6	V
V_{CCI}	Supply voltage for LVDS receivers(1)	3.0	3.3	3.6	V
V_{OFFSET}	Mirror Electrode and HVCMOS voltage(1) (2)	8.25	8.5	8.75	V
V_{MBRST}	Micromirror clocking pulse voltages(1)	–27		26.5	V
$\lvert V_{CCI}–V_{CC}\rvert$	Supply voltage delta (absolute value)(3)			0.3	V
LVCMOS INTERFACE					
V_{IH}	High level input voltage	1.7	2.5	VCC + 0.3	V
V_{IL}	Low level input voltage	–0.3		0.7	V
I_{OH}	High level output current at V_{OH} = 2.4 V			–20	mA
I_{OL}	Low level output current at V_{OL} = 0.4 V			15	mA
t_{PWRDNZ}	PWRDNZ pulse width(4)	10			ns
SCP INTERFACE					
f_{SCPCLK}	SCP clock frequency(5)	50		500	kHz
t_{SCP_PD}	Propagation delay, clock to Q, from rising-edge of SCPCLK to valid SCPDO(6)	0		900	ns
t_{SCP_DS}	SCPDI clock setup time (before SCPCLK falling-edge)(6)	800			ns
t_{SCP_DH}	SCPDI hold time (after SCPCLK falling-edge)(6)	900			
$t_{SCP\_NEG\_ENZ}$	Time between falling-edge of SCPENZ and the first rising-edge of SCPCLK	1			us
$t_{SCP\_POS\_ENZ}$	Time between falling-edge of SCPCLK and the rising-edge of SCPENZ	1			us
$t_{SCP\_PW\_ENZ}$	SCPENZ inactive pulse width (high level)	1			$1/f_{SCPCLK}$
t_{r_SCP}	Rise time for SCP signals			200	ns
t_{fP}	Fall time for SCP signals			200	ns
LVDS INTERFACE					
f_{CLOCK}	Clock frequency for LVDS interface (all channels), DCLK(7)		320	330	MHz
$\lvert V_{ID}\rvert$	Input differential voltage (absolute difference)(8)	100	400	600	mV
V_{CM}	Common mode voltage(8)		1200		mV
V_{LVDS}	LVDS voltage(8)	0		2000	mV
t_r	Rise time (20% to 80%)	100		400	ps
t_r	Fall time (80% to 20%)	100		400	ps
t_{LVDS_RSTZ}	Time required for LVDS receivers to recover from PWRDNZ			10	ns
Z_{IN}	Internal differential termination resistance	95		105	Ω
ENVIRONMENTAL					
T_{ARRAY}	Array temperature, long-term operational(9) (10) (11)	10		40 to 70(12)	°C
	Array temperature, short-term operational(10) (13)	0		10	°C

6.4 Recommended Operating Conditions (continued)

Over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by this table. No level of performance is implied when operating the device above or below these limits.

		MIN	NOM	MAX	UNIT
T_{WINDOW}	Window temperature – operational(14)			85	°C
$T_{\|DELTA\|}$	Absolute temperature delta between any point on the window edge and the ceramic test point TP1(15)			26	°C
T_{DP-AVG}	Average dew point temperature (non-condensing)(16)			28	°C
T_{DP-ELR}	Elevated dew point temperature range (non-condensing)(17)	28		36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range			24	Months
ILL_{UV}	Illumination wavelengths < 395 nm(9)		0.68	2.00	mW/cm^2
ILL_{VIS}	Illumination wavelengths between 395 nm and 800 nm		Thermally limited		mW/cm^2
ILL_{IR}	Illumination wavelengths > 800 nm			10	mW/cm^2

(1) All voltages are referenced to common ground V_{SS}. V_{BIAS}, V_{CC}, V_{OFFSET}, and V_{RESET} power supplies are all required for proper DMD operation. V_{SS} must also be connected.
(2) V_{OFFSET} supply transients must fall within specified max voltages.
(3) To prevent excess current, the supply voltage delta $|V_{CCI} – V_{CC}|$ must be less than specified limit. See セクション 9.
(4) PWRDNZ input pin resets the SCP and disables the LVDS receivers. PWRDNZ input pin overrides SCPENZ input pin and tristates the SCPDO output pin.
(5) The SCP clock is a gated clock. Duty cycle shall be 50% ± 10%. SCP parameter is related to the frequency of DCLK.
(6) See 図 6-2.
(7) See LVDS Timing Requirements in セクション 6.7 and 図 6-5.
(8) Refer to 図 6-7, 図 6-8, and 図 6-9.
(9) Simultaneous exposure of the DMD to the maximum セクション 6.4 for temperature and UV illumination reduces device lifetime.
(10) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point 1 (TP1) shown in 図 7-1 and the package thermal resistance using the calculation in セクション 7.4 .
(11) Long-term is defined as the average over the usable life.
(12) Per 図 6-1, the maximum operational array temperature should be derated based on the micromirror landed duty cycle that the DMD experiences in the end application. See セクション 7.5 for a definition of micromirror landed duty cycle.
(13) Array temperatures beyond those specified as long-term are recommended for short-term conditions only (for example, power-up). Short-term is defined as cumulative time over the usable life of the device and is less than 500 hours.
(14) The locations of thermal test points TP2, TP3, TP4, and TP5 in 図 7-1 are intended to measure the highest window edge temperature. For most applications, the locations shown are representative of the highest window edge temperature. If a particular application causes additional points on the window edge to be at a higher temperature, test points should be added to those locations.
(15) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in 図 7-1. The window test points TP2, TP3, TP4, and TP5 shown in 図 7-1 are intended to result in the worst-case delta temperature. If a particular application causes another point on the window edge to result in a larger delta in temperature, that point should be used.
(16) The average over time (including storage and operating) that the device is not in the "elevated dew point temperature range."
(17) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of CT_{ELR}.

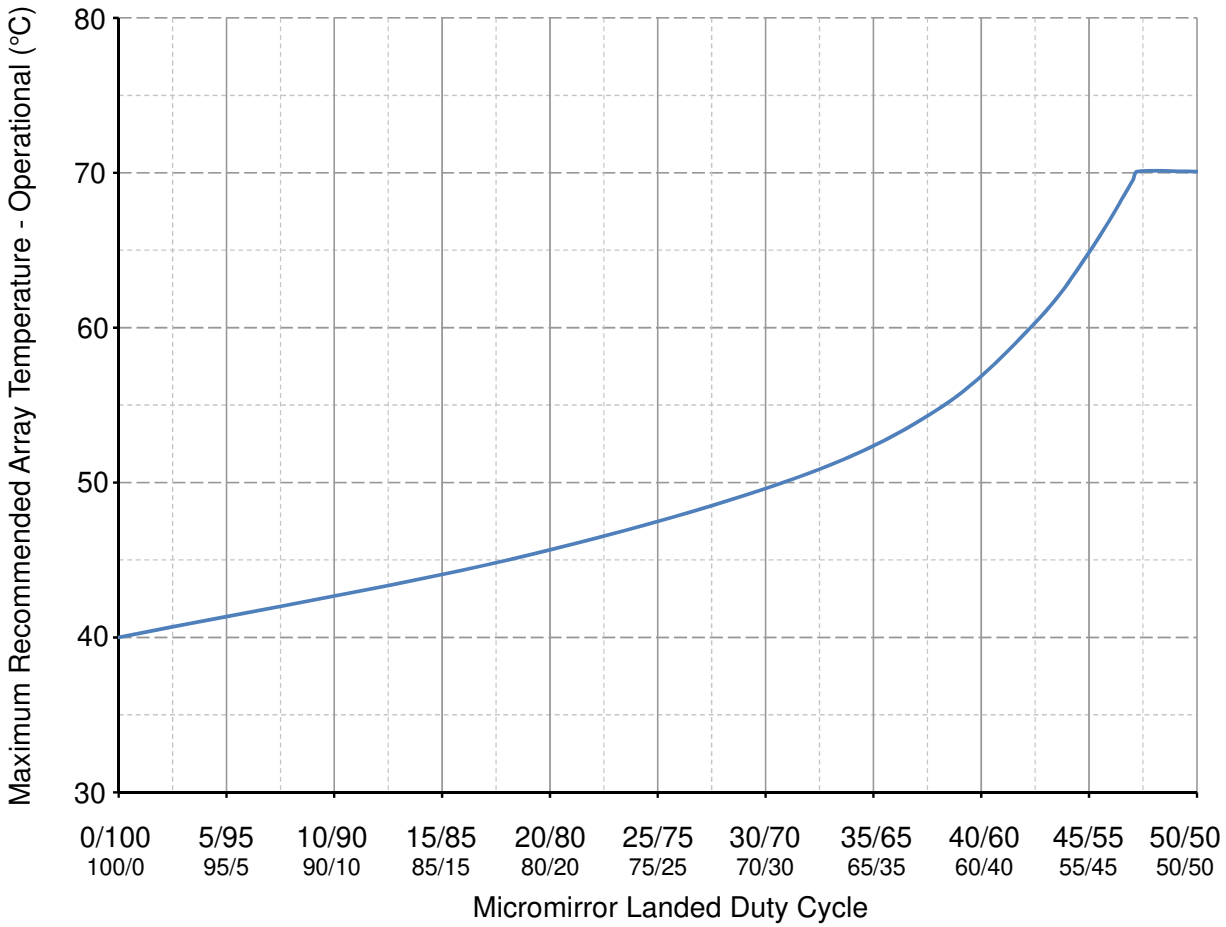


図 6-1. Maximum Recommended DMD Temperature—Derating Curve

6.5 Thermal Information

THERMAL METRIC	DLP550JE FYA PACKAGE 149 PINS	UNIT
Thermal resistance, active array to test point 1 (TP1)(1)	0.60	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the package within the temperature range specified in the セクション 6.4.
The total heat load on the DMD is largely driven by the incident light absorbed by the active area; although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array.
Optical systems should be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

6.6 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 3.0 V, I_{OH} = –20 mA	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = 3.6 V, I_{OL} = 15 mA			0.4	V
I_{OZ}	High impedance output current	V_{CC} = 3.6 V			10	µA
I_{IL}	Low-level input current	V_{CC} = 3.6 V, V_I = 0 V			–60	µA
I_{IH}	High-level input current(1)	V_{CC} = 3.6 V, V_I = V_{CC}			200	µA
I_{CC}	Current into V_{CC} pin	V_{CC} = 3.6 V			531	mA
I_{CCI}	Current into V_{CC1} pin(2)	V_{CCI} = 3.6 V			374	mA
I_{OFFSET}	Current into V_{OFFSET} pin(3)	V_{OFFSET} = 8.75 V			25	mA
Z_{IN}	Internal Differential Impedance		95		105	Ω
Z_{LINE}	Line Differential Impedance (PWB or Trace)		90	100	110	Ω
C_I	Input capacitance(1)	f = 1 MHz			10	pF
C_O	Output capacitance(1)	f = 1 MHz			10	pF
C_{IM}	Input capacitance for MBRST[0:15] pins	f = 1 MHz	160		210	pF

(1) Applies to LVCMOS pins only. Excludes LVDS pins and test pad pins
(2) To prevent excess current, the supply voltage change $|V_{CCI} – V_{CC}|$ must be less than specified limits listed in the セクション 6.4.
(3) To prevent excess current, the supply voltage delta $|V_{BIAS} – V_{OFFSET}|$ must be less than the specified limit in セクション 6.4.

6.7 Timing Requirements

Over operating free-air temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
LVDS (1)					
t_c	Clock Cycle for DLCK_A	3.03			ns
t_c	Clock Cycle for DCLKC_B	3.03			ns
t_w	Pulse Duration DCLK_A	1.36	1.52		ns
t_w	Pulse Duration for DCLK_B	1.36	1.52		ns
t_{SU}	Setup Time, D_A[0:15] before DCLK_A	0.35			ns
t_{SU}	Setup Time, D_B[0:15] before DCLK_B	0.35			ns
t_{SU}	Setup Time, SCTRL_A before DCLK_A	0.35			ns
t_{SU}	Setup Time, SCTRL_B before DCLK_B	0.35			ns
t_H	Hold Time, D_A[0:15] after DCLK_A	0.35			ns
t_H	Hold Time, D_B[0:15] after DCLK_B	0.35			ns
t_H	Hold Time, SCTRL_A after DCLK_A	0.35			ns
t_H	Hold Time, SCTRL_B after DCLK_B	0.35			ns
t_{skew}	Channel B relative to Channel A(2) (3)	–1.51		1.51	ns

(1) See 図 6-5 for timing requirements for LVDS.
(2) Channel A (Bus A) includes the following LVDS pairs: DCLK_AN and DCLK_AP, SCTRL_AN and SCTRL_AP, D_AN(15:0) and D_AP(15:0).
(3) Channel B (Bus B) includes the following LVDS pairs: DCLK_BN and DCLK_BP, SCTRL_BN and SCTRL_BP, D_BN(15:0) and D_BP(15:0).

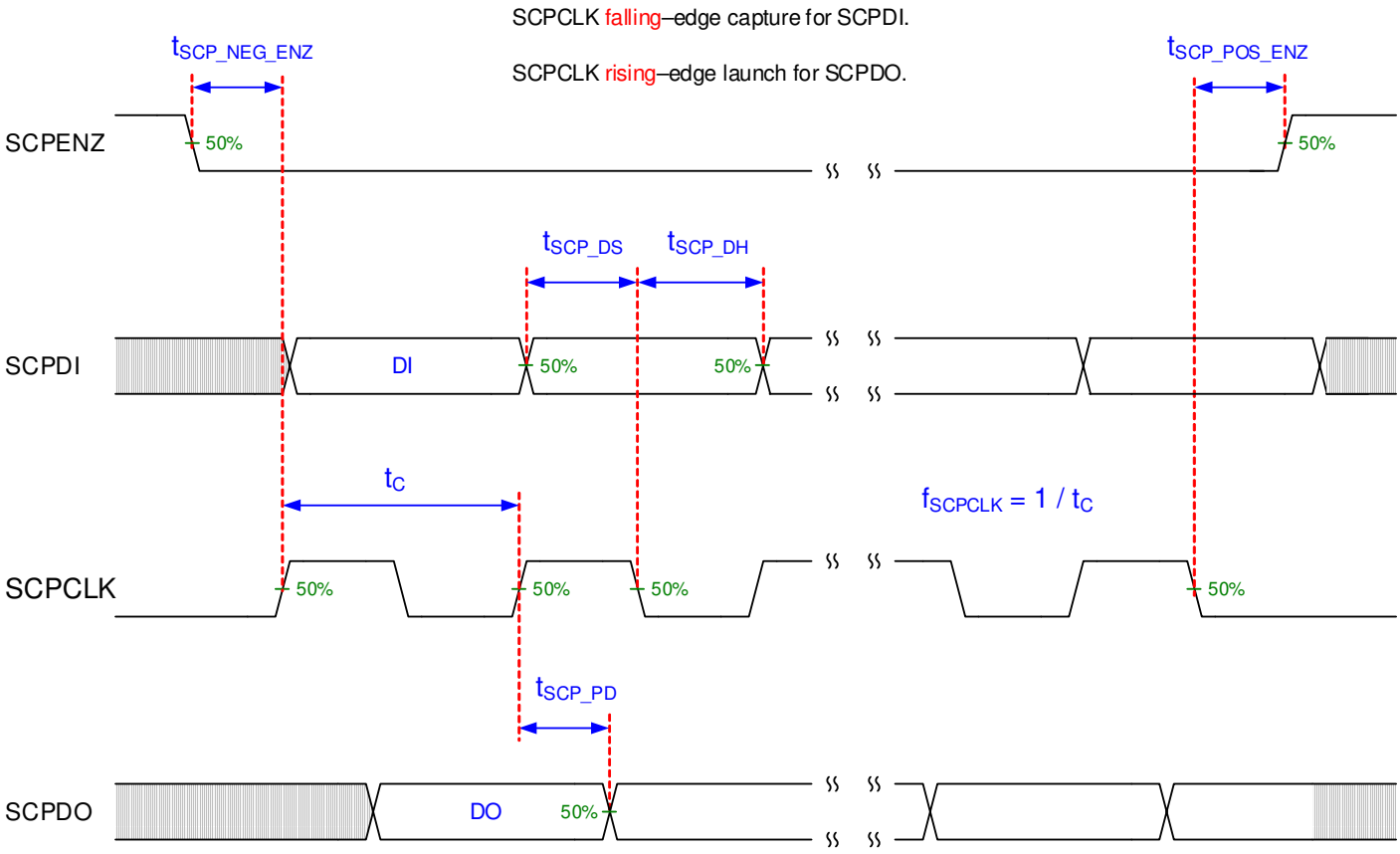
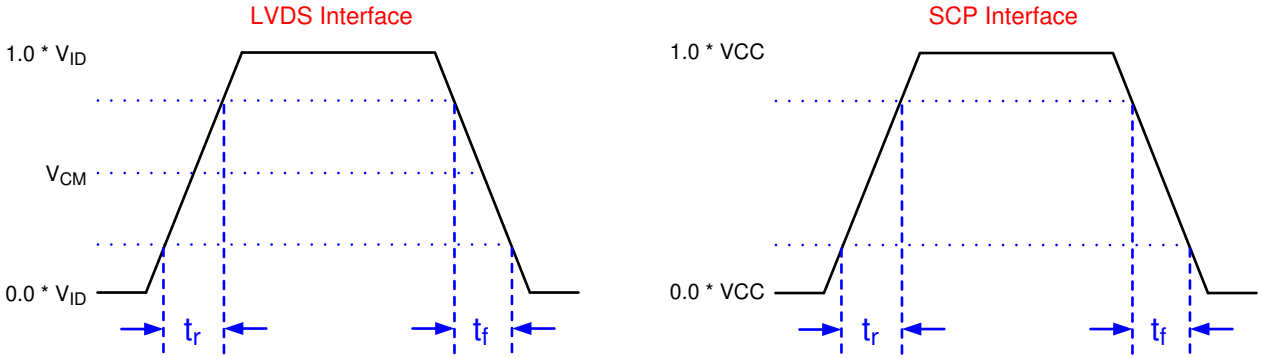


図 6-2. SCP Timing Parameters



Not to scale
Refer to セクション 6.7.
Refer to セクション 5 for list of LVDS pins and SCP pins.

図 6-3. Rise Time and Fall Time

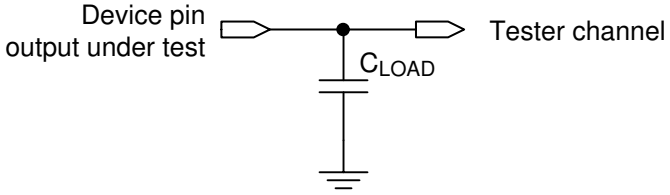


図 6-4. Test Load Circuit for Output Propagation Measurement

For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. System design should use IBIS or other simulation tools to correlate the timing reference load to a system environment. See 図 6-4.

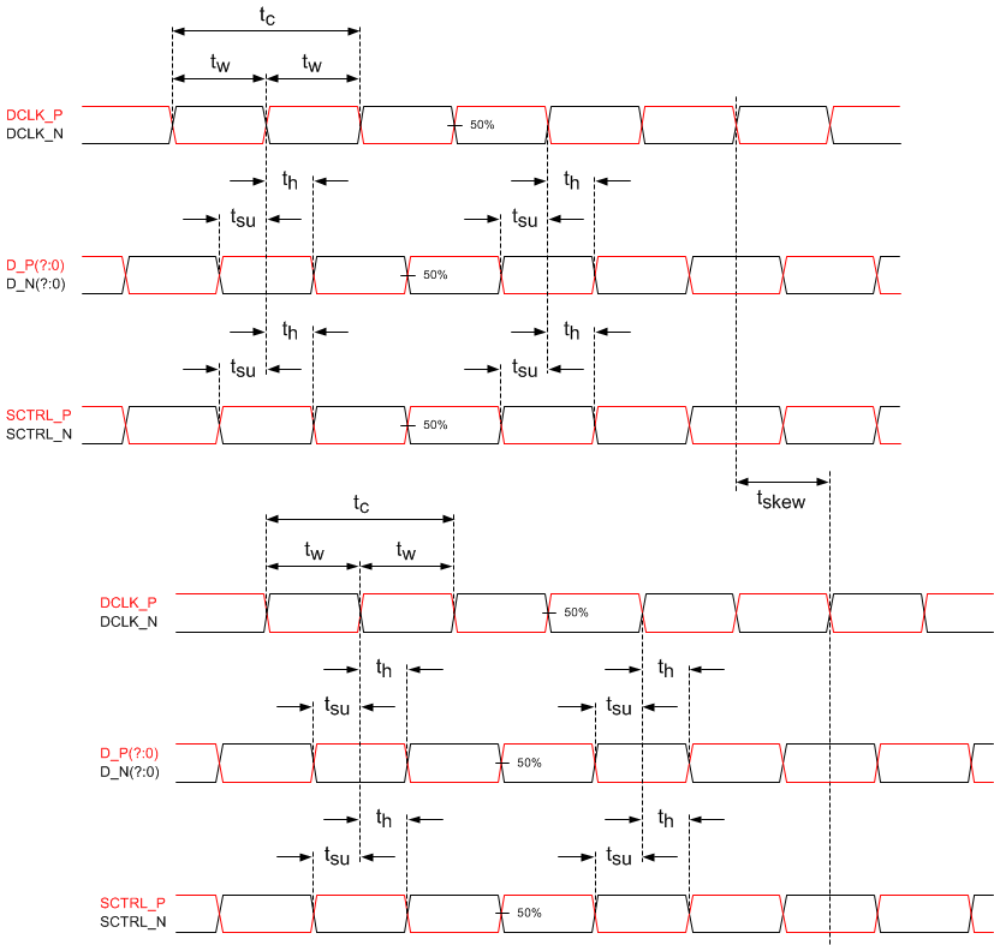


図 6-5. Timing Requirements

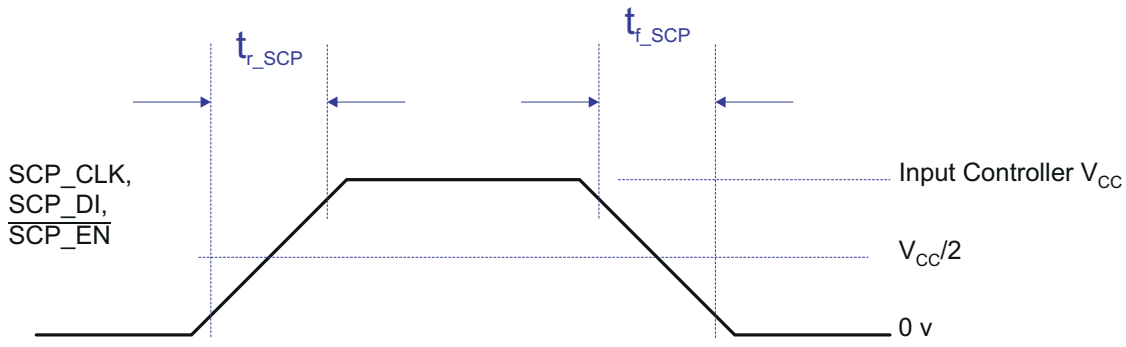
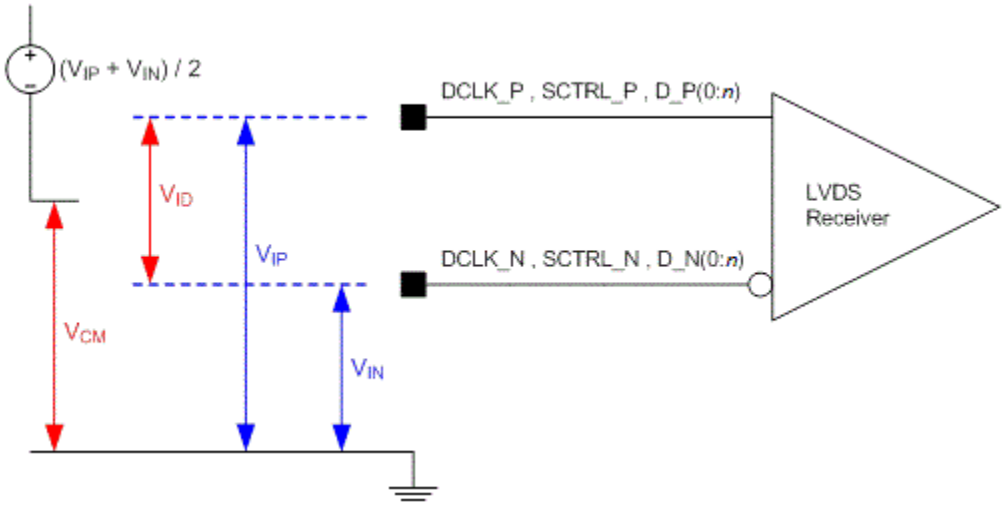


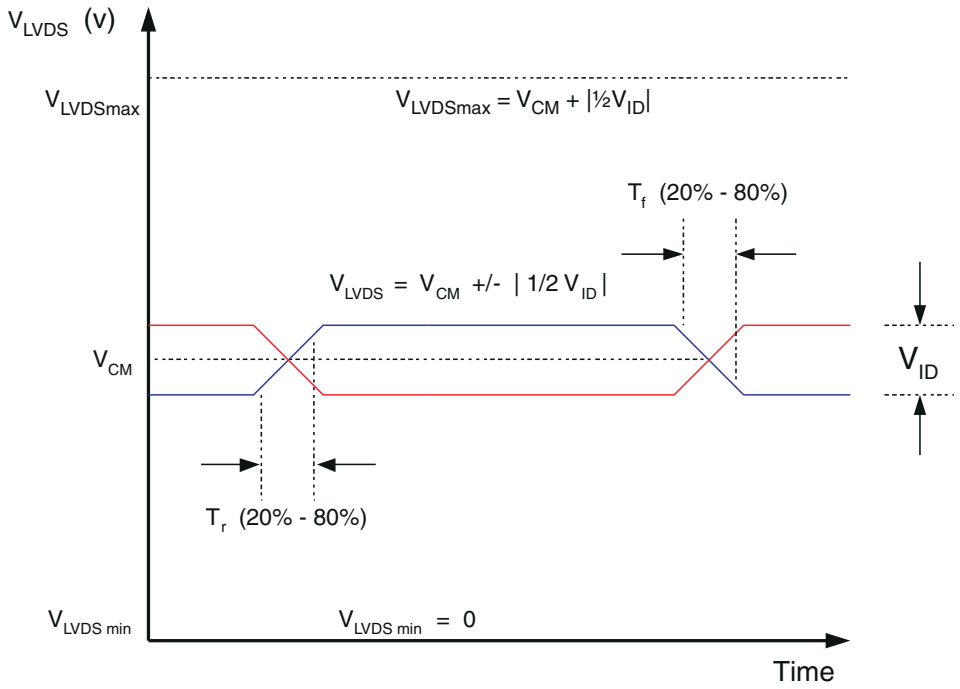
図 6-6. Serial Communications Bus Waveform Requirements



Refer to LVDS Interface section of セクション 6.4.

Refer to セクション 5 for list of LVDS pins.

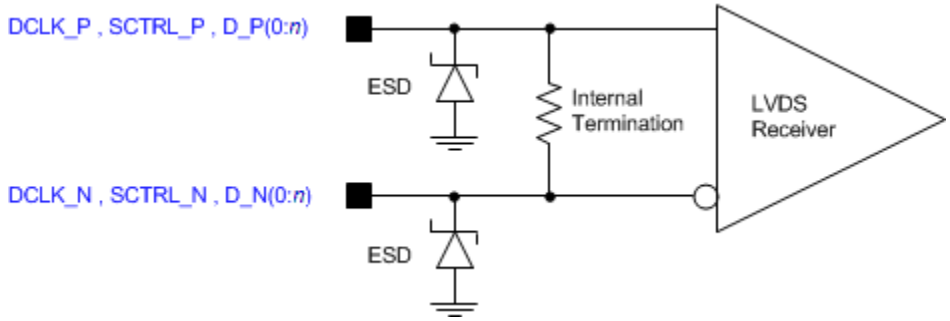
図 6-7. LVDS Voltage Definitions (References)



Not to scale

Refer to LVDS Interface section of the セクション 6.4.

図 6-8. LVDS Voltage Parameter



Refer to LVDS Interface section of the セクション 6.4.

Refer to セクション 5 for list of LVDS pins.

図 6-9. LVDS Equivalent Input Circuit

6.8 Window Characteristics

PARAMETER	MIN	NOM
Window material		Corning Eagle XG
Window refractive index at wavelength 546.1 nm		1.5119
Window Transmittance, minimum within the wavelength range 420–680 nm. Applies to all angles 0°–30° AOI. (1) (2)	97%	
Window Transmittance, average over the wavelength range 420–680 nm. Applies to all angles 30°–45° AOI. (1) (2)	97%	

(1) Single-pass through both surfaces and glass.
(2) Angle of incidence (AOI) is the angle between an incident ray and the normal to a reflecting or refracting surface.

6.9 System Mounting Interface Loads

PARAMETER	MIN	NOM	MAX	UNIT
Condition 1:				
• Thermal Interface area(1)			11.3	kg
• Electrical Interface area(1)			11.3	kg
Condition 2:				
• Thermal Interface area(1)			0	kg
• Electrical Interface area(1)			22.6	kg

(1) Uniformly distributed within the area shown in 図 6-10

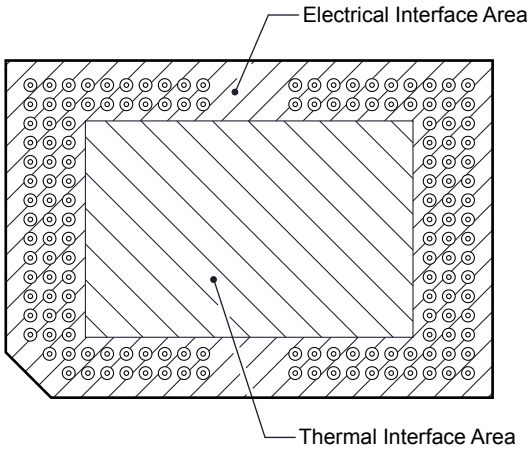
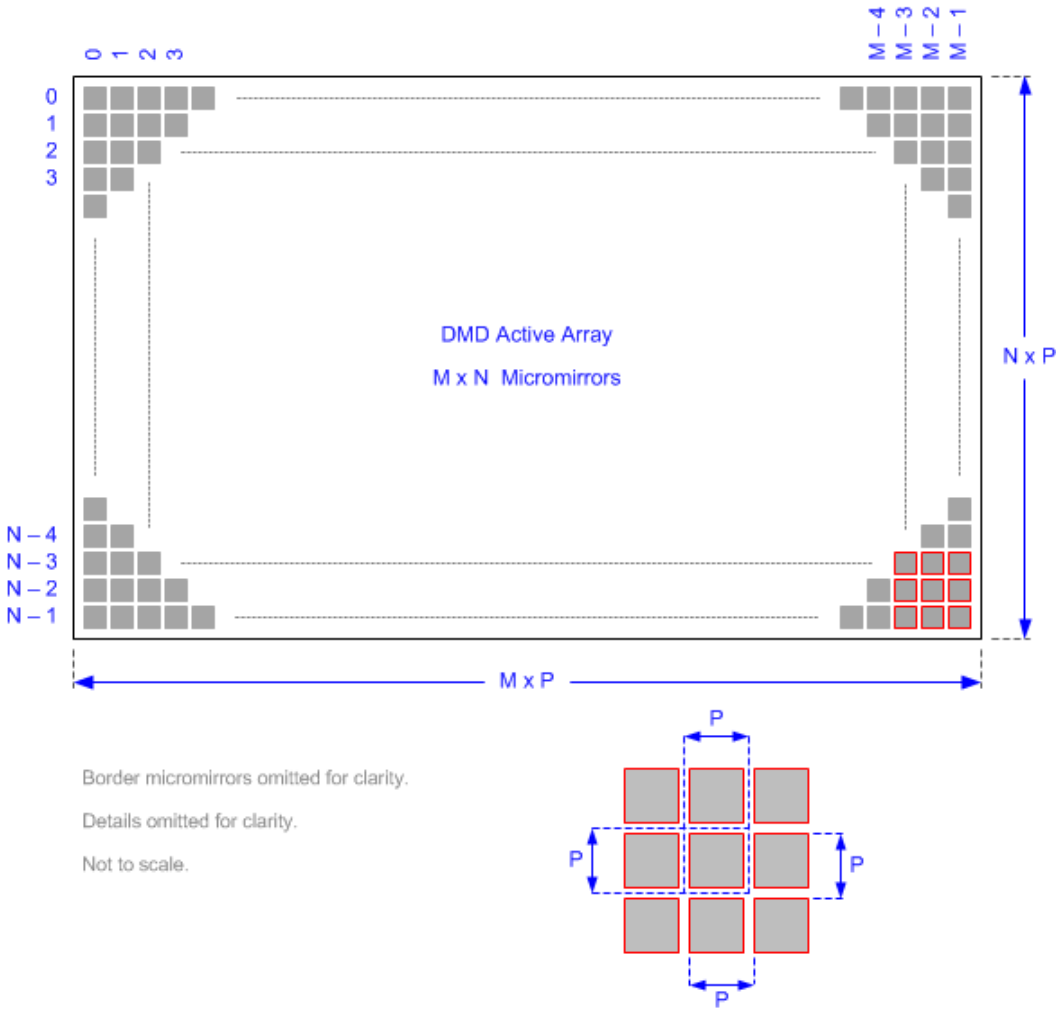


図 6-10. System Interface Loads

6.10 Micromirror Array Physical Characteristics

PARAMETER		VALUE	UNIT
Number of active columns(1)	M	1024	micromirrors
Number of active rows(1)	N	768	
Micromirror (pixel) pitch(1)	P	10.8	µm
Micromirror active array width(1)	Micromirror pitch × number of active columns	11.059	mm
Micromirror active array height (1)	Micromirror pitch × number of active columns	8.294	mm
Micromirror active array border(2)	Pond of Micromirror (POM)	10	micromirrors/side

(1) See 図 6-11.
(2) The structure and qualities of the border around the active array includes a band of partially functional micromirrors referred to as the Pond Of Mirrors (POM). These micromirrors are structurally and/or electrically prevented from tilting toward the bright or ON state, but still require an electrical bias to tilt toward OFF.



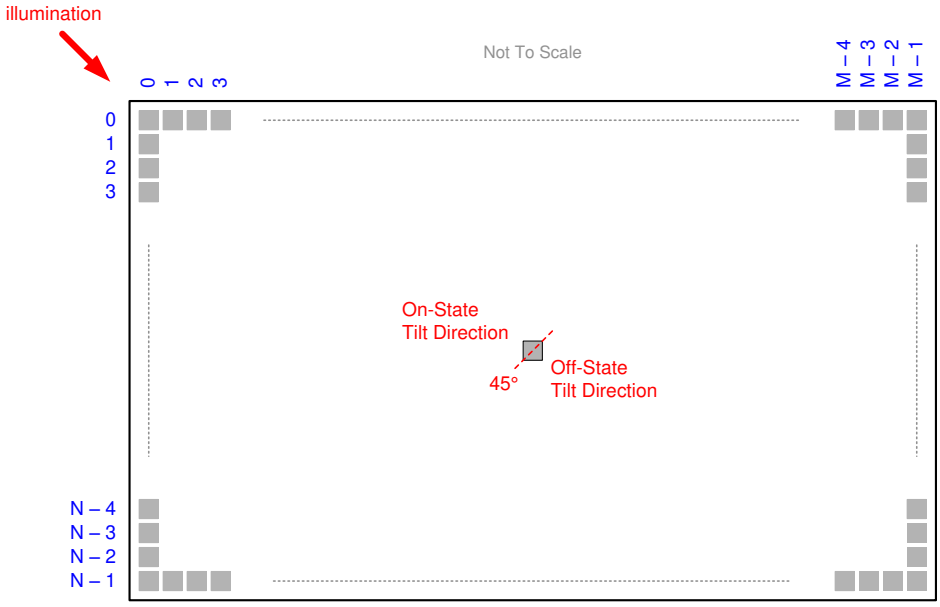
Refer to the *セクション 6.10* for M, N, and P specifications.

図 6-11. Micromirror Array Physical Characteristics

6.11 Micromirror Array Optical Characteristics

PARAMETER		MIN	NOM	MAX	UNIT
Micromirror tilt angle, variation device to device (1) (2) (3) (4)		11	12	13	degrees
Number of out-of-specification micromirrors (5)	Adjacent micromirrors			0	micromirrors
	Non-adjacent micromirrors			10	

(1) Measured relative to the plane formed by the overall micromirror array.
(2) Variation can occur between any two individual micromirrors located on the same device or located on different devices.
(3) Additional variation exists between the micromirror array and the package datums. See package drawing.
(4) See 図 6-12.
(5) An out-of-specification micromirror is defined as a micromirror that is unable to transition between the two landed states.



Refer to section *Micromirror Array Physical Characteristics* table for M, N, and P specifications.

図 6-12. Micromirror Landed Orientation and Tilt

6.12 Chipset Component Usage Specification

Reliable function and operation of the DLP550JE DMD requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology consists of the TI technology and devices used for operating or controlling a DLP DMD.

7 Detailed Description

7.1 Overview

The DLP550JE is a 0.55 inch diagonal spatial light modulator which consists of an array of highly reflective aluminum micromirrors. Pixel array size and square grid pixel arrangement are shown in 図 6-11.

The DMD is an electrical input, optical output micro-electrical-mechanical system (MEMS). The electrical interface is Low Voltage Differential Signaling (LVDS), Double Data Rate (DDR).

The DLP550JE DMD consists of a two-dimensional array of 1-bit CMOS memory cells. The array is organized in a grid of *M* memory cell columns by *N* memory cell rows.

The positive or negative deflection angle of the micromirrors can be individually controlled by changing the address voltage of underlying CMOS addressing circuitry and micromirror reset signals (MBRST).

Each cell of the *M* × *N* memory array drives its true and complement (‘Q’ and ‘QB’) data to two electrodes underlying one micromirror, one electrode on each side of the diagonal axis of rotation. The micromirrors are electrically tied to the micromirror reset signals (MBRST) and the micromirror array is divided into reset groups.

Electrostatic potentials between a micromirror and its memory data electrodes cause the micromirror to tilt toward the illumination source in a DLP projection system or away from it, thus reflecting its incident light into or out of an optical collection aperture. The positive (+) tilt angle state corresponds to an 'on' pixel, and the negative (–) tilt angle state corresponds to an 'off' pixel.

Refer to *Micromirror Array Optical Characteristics* for the ± tilt angle specifications. Refer to the *Pin Configuration and Functions* for more information on micromirror clocking pulse (reset) control.

7.2 Feature Description

7.2.1 Power Interface

The DMD requires 3 DC voltages: DMD_P3P3V, V_{OFFSET}, and MBRST. DMD_P3P3V is created by the DLPA100 power and motor driver and the DLPA200 DMD micromirror driver. Both the DLPA100 and DLPA200 create the main DMD voltages, as well as powering various peripherals (TMP411, I^2C, and TI level translators). DMD_P3P3V provides the V_{CC} voltage required by the DMD. V_{OFFSET} (8.5V) and MBRST are made by the DLPA200 and are supplied to the DMD to control the micromirrors.

7.2.2 Timing

The data sheet provides timing analysis as measured at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be considered. 図 6-4 shows an equivalent test load circuit for the output under test. Timing reference loads are not intended as a precise representation of any particular system environment or depiction of the actual load presented by a production test. TI suggests that system designers use IBIS or other simulation tools to correlate the timing reference load to a system environment. The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

7.3 Optical Interface and System Image Quality Considerations

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. System optical performance and image quality strongly relate to optical system design parameter trade offs. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in the following sections.

7.3.1 Numerical Aperture and Stray Light Control

The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area should be the same. This angle should not exceed the nominal device mirror tilt angle unless appropriate apertures are added in the illumination and/or projection pupils to block out flat-state and stray light from the projection lens. The mirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the mirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle (and vice versa), contrast degradation, and objectionable artifacts in the display's border and/or active area could occur.

7.3.2 Pupil Match

TI's optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display's border and/or active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

7.3.3 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD chip assembly from normal view, and is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. The illumination optical system should be designed to limit light flux incident anywhere on the window aperture from exceeding approximately 10% of the average flux level in the active area. Depending on the particular system's optical architecture, overfill light may have to be further reduced below the suggested 10% level in order to be acceptable.

7.4 Micromirror Array Temperature Calculation

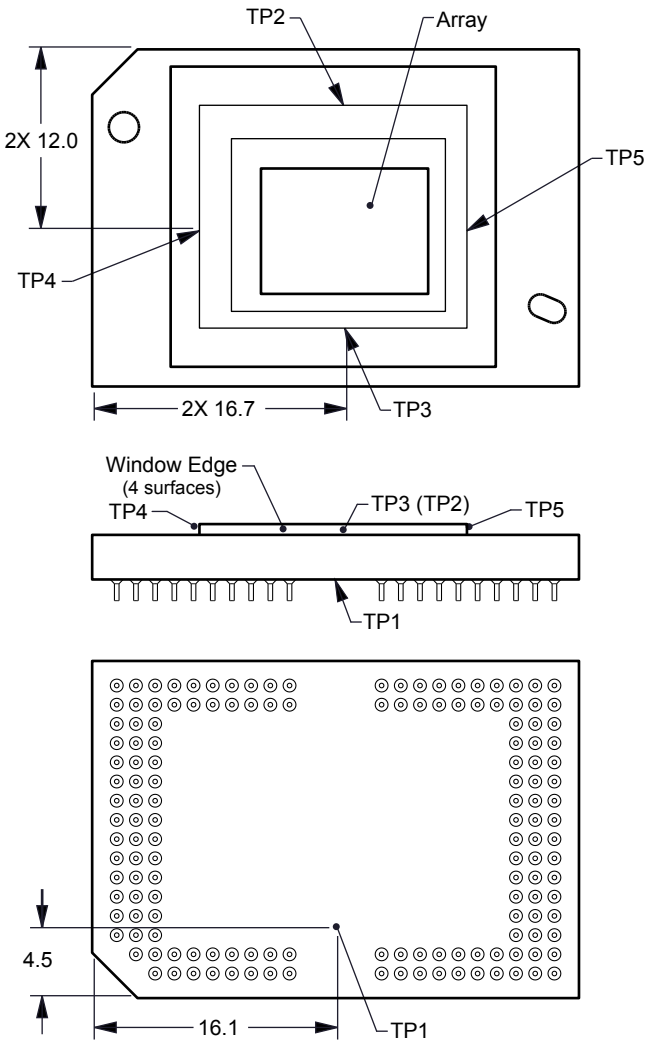


図 7-1. Thermal Test Point Location

7.4.1 Micromirror Array Temperature Calculation

Micromirror array temperature cannot be measured directly, therefore it must be computed analytically from measurement points on the outside of the package, the package thermal resistance, the electrical power, and the illumination heat load. The relationship between array temperature and the reference ceramic temperature (thermal test TP1 in 図 7-1) is provided by the following equations:

$$T_{ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{ARRAY-TO-CERAMIC})$$

$$Q_{ARRAY} = Q_{ELECTRICAL} + Q_{ILLUMINATION}$$

$$Q_{ILLUMINATION} = (C_{L2W} \times SL)$$

where

- T_{ARRAY} = Computed array temperature (°C)
- $T_{CERAMIC}$ = Measured ceramic temperature (°C), TP1 location in 図 7-1

- $R_{ARRAY–TO–CERAMIC}$ = Thermal resistance of package (specified in *Thermal Information*) from array to ceramic TP1(°C/Watts).
- Q_{ARRAY} = Total DMD Power (electrical + absorbed) on array (Watts).
- $Q_{ELECTRICAL}$ = Nominal electrical power
- C_{L2W} = Conversion constant for screen lumens to absorbed optical power on the DMD (W/lm) specified below
- SL = Measured ANSI screen lumens (lm)

The electrical power dissipation of the DMD is variable and depends on the voltages, data rates and operating frequencies. A nominal electrical power dissipation to use when calculating array temperature is 1.4 W. The absorbed optical power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. The equations shown above are valid for a 1-chip DMD system with total projection efficiency through the projection lens from DMD to the screen of 87%.

The conversion constant C_{L2W} is based on the DMD micromirror array characteristics. It assumes a spectral efficiency of 300 lm/W for the projected light and illumination distribution of 83.7% on the DMD active array, and 16.3% on the DMD array border and window aperture. The conversion constant is calculated to be 0.00274 W/lm.

Sample calculations:

$T_{CERAMIC}$ = 55°C

SL = 3000 lm

$Q_{ELECTRICAL}$ = 1.4 W

C_{L2W} = 0.00274 W/lm

Q_{ARRAY} = 1.4 W + (0.00274 × 3000) = 9.62 W

T_{ARRAY} = 55°C + (9.62 W × 0.6 C/W) = 60.8°C

7.5 Micromirror Landed-on/Landed-Off Duty Cycle

7.5.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the On–state versus the amount of time the same micromirror is landed in the Off–state.

As an example, a landed duty cycle of 100/0 indicates that the referenced pixel is in the On-state 100% of the time (and in the Off-state 0% of the time); whereas 0/100 would indicate that the pixel is in the Off-state 100% of the time. Likewise, 50/50 indicates that the pixel is On 50% of the time and Off 50% of the time.

Note that when assessing landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (On or Off), the two numbers (percentages) always add to 100.

7.5.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD's micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD's usable life.

Note that it is the symmetry/asymmetry of the landed duty cycle that is of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

7.5.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD Temperature and Landed Duty Cycle interact to affect the DMD's usable life, and this interaction can be exploited to reduce the impact that an asymmetrical Landed Duty Cycle has on the DMD's usable life. This is quantified in the de-rating curve shown in 図 6-1. The importance of this curve is that:

- All points along this curve represent the same usable life.
- All points above this curve represent lower usable life (and the further away from the curve, the lower the usable life).
- All points below this curve represent higher usable life (and the further away from the curve, the higher the usable life).

In practice, this curve specifies the maximum operating DMD Temperature at a given long-term average Landed Duty Cycle.

7.5.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the Landed Duty Cycle of a given pixel follows from the image content being displayed by that pixel.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel will experience a 100/0 Landed Duty Cycle during that time period. Likewise, when displaying pure-black, the pixel will experience a 0/100 Landed Duty Cycle.

Between the two extremes (ignoring for the moment color and any image processing that may be applied to an incoming image), the Landed Duty Cycle tracks one-to-one with the gray scale value, as shown in 表 7-1.

表 7-1. Grayscale Value and Landed Duty Cycle

GRAYSCALE VALUE	LANDED DUTY CYCLE
0%	0/100
10%	10/90
20%	20/80
30%	30/70
40%	40/60
50%	50/50
60%	60/40
70%	70/30
80%	80/20
90%	90/10
100%	100/0

Accounting for color rendition (but still ignoring image processing) requires knowing both the color intensity (from 0% to 100%) for each constituent primary color (red, green, and/or blue) for the given pixel as well as the color cycle time for each primary color, where “color cycle time” is the total percentage of the frame time that a given primary must be displayed in order to achieve the desired white point.

During a given period of time, the landed duty cycle of a given pixel can be calculated as follows:

$$\text{Landed Duty Cycle} = (\text{Red\_Cycle\_\%} \times \text{Red\_Scale\_Value}) + (\text{Green\_Cycle\_\%} \times \text{Green\_Scale\_Value}) + (\text{Blue\_Cycle\_\%} \times \text{Blue\_Scale\_Value}) \quad (1)$$

where

- Red_Cycle_%, Green_Cycle_%, and Blue_Cycle_%, represent the percentage of the frame time that Red, Green, and Blue are displayed (respectively) to achieve the desired white point.

For example, assume that the red, green, and blue color cycle times are 50%, 20%, and 30% respectively (in order to achieve the desired white point), then the Landed Duty Cycle for various combinations of red, green, and blue color intensities would be as shown in 表 7-2.

表 7-2. Example Landed Duty Cycle for Full-Color

Red Cycle Percentage 50%	Green Cycle Percentage 20%	Blue Cycle Percentage 30%	Landed Duty Cycle
Red Scale Value	Green Scale Value	Blue Scale Value	
0%	0%	0%	0/100
100%	0%	0%	50/50
0%	100%	0%	20/80
0%	0%	100%	30/70
12%	0%	0%	6/94
0%	35%	0%	7/93
0%	0%	60%	18/82
100%	100%	0%	70/30
0%	100%	100%	50/50
100%	0%	100%	80/20
12%	35%	0%	13/87
0%	35%	60%	25/75
12%	0%	60%	24/76
100%	100%	100%	100/0

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

Texas Instruments DLP technology is a micro-electromechanical system (MEMS) technology that modulates light using a digital micromirror device (DMD). The DMD is a spatial light modulator, which reflects incoming light from an illumination source to one of two directions, either towards the projection optics or the collection optics. The large micromirror array size and ceramic package provides great thermal performance for bright display applications. Typical applications using the DLP550JE include digital signage, educational projector, and business projector.

The following orderables have been replaced by the DLP650JE:

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)	MECHANICAL ICD
DLP550JET	FYA (149)	32.20 mm × 22.30 mm	2512194
1076-6434B	FYA (149)	32.20 mm × 22.30 mm	2512194
1076-6438B	FYA (149)	32.20 mm × 22.30 mm	2512194
1076-6439B	FYA (149)	32.20 mm × 22.30 mm	2512194
1076-643AB	FYA (149)	32.20 mm × 22.30 mm	2512194

8.2 Typical Application

The DLP550JE digital micromirror device (DMD), combined with a DLPC4430 digital controller and a DLPA100 power management or a DLPA200 power management device, provides XGA resolution for bright, colorful display applications. A typical display system using the DLP550JE and additional system components is shown in Typical DLPC4430 Application (LED Top, LPCW Bottom).

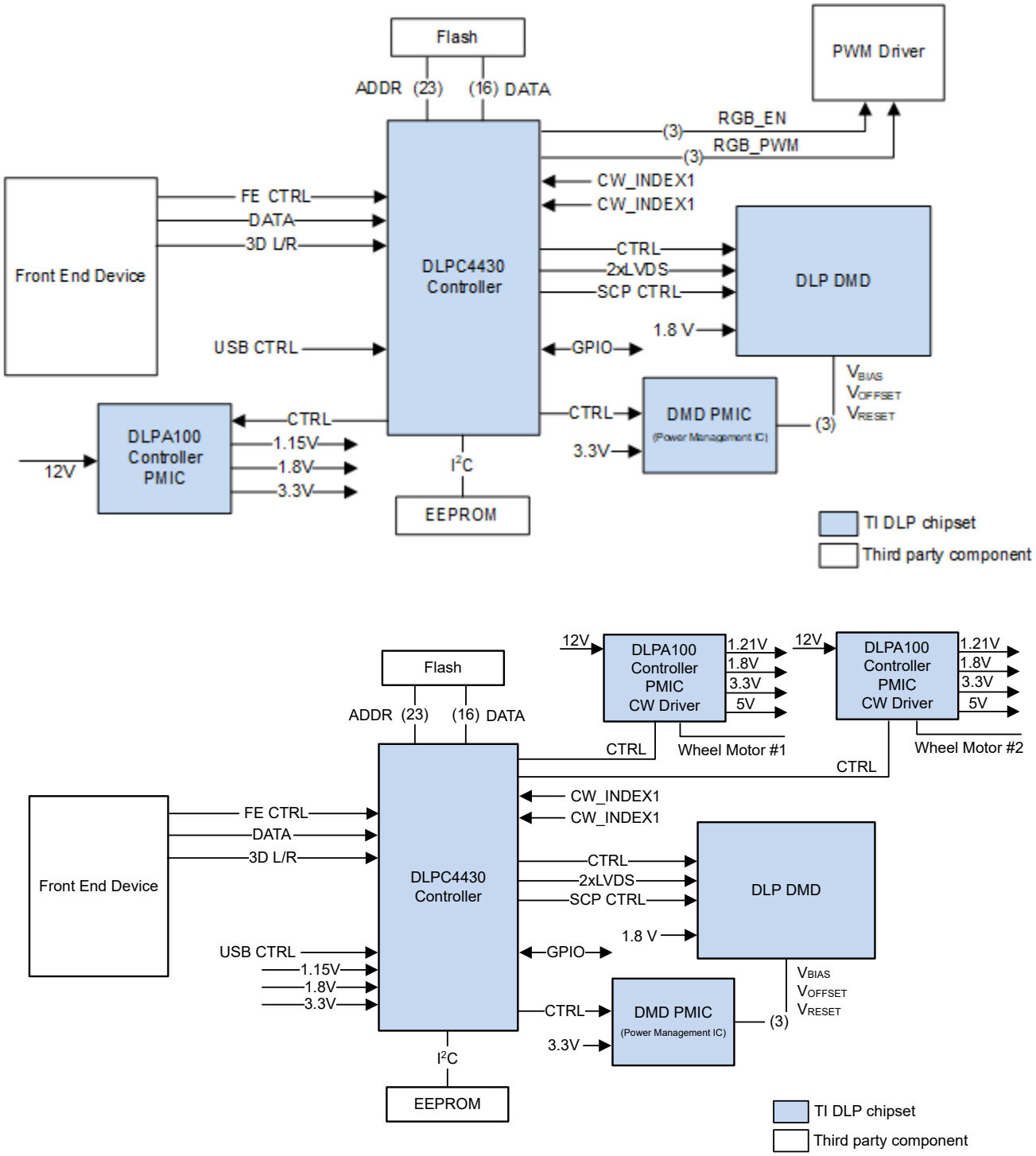


図 8-1. Typical DLPC4430 Application (LED Top, LPCW Bottom)

8.2.1 Design Requirements

The DLP550JE projection system is created by using the DMD chipset, including the DLP550JE, DLPC4430, DLPA100, and the DLPA200. The DLP550JE is used as the core imaging device in the display system and contains a 0.55-inch array of micromirrors. The DLPC4430 controller is the digital interface between the DMD and the rest of the system, taking digital input from front end receiver that converts the data from the source and using the converted data for driving the DMD over a high speed interface. The DLPA100 power management

device provides voltage regulators for the controller and illumination functionality. The DLPA200 provides the power and sequencing to drive the DLP550JE.

Other core components of the display system include an illumination source, an optical engine for the illumination and projection optics, other electrical and mechanical components, and software. The illumination source options include a lamp, LED, laser, or laser phosphor. The type of illumination used and desired brightness will have a major effect on the overall system design and size.

8.2.2 Detailed Design Procedure

For connecting the DLPC4430 display controller and the DLP550JE DMD, see the reference design schematic. For a complete DLP system, an optical module or light engine is required that contains the DLP550JE DMD, associated illumination sources, optical elements, and necessary mechanical components. The optical module is typically supplied by an OMM (optical module manufacturer) who specializes in designing optics for DLP projectors.

To ensure reliable operation, the DLP550JE DMD must always be used with the DLPC4430 display controller, a DLPA100 PMIC driver, and a DLPA200 DMD micromirror driver.

9 Power Supply Recommendations

9.1 DMD Power-Up and Power-Down Procedures

The DLP550JE power-up and power-down procedures are defined by the DLPC4430 data sheet. The power supply guidelines are defined in the *DLPA200 DMD Micromirror Driver Data Sheet*. These procedures must be followed to ensure reliable operation of the device.

注意

For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to the prescribed power-up and power-down procedures may affect device reliability. V_{CC}, V_{CCI}, V_{OFFSET}, and V_{MBRST} power supplies have to be coordinated during power-up and power-down operations. V_{SS} must also be connected. Failure to meet any of these requirements results in a significant reduction in the DMD's reliability and lifetime.

10 Device and Documentation Support

10.1 Device Support

10.1.1 サード・パーティ製品に関する免責事項

サード・パーティ製品またはサービスに関するテキサス・インスツルメンツの出版物は、単独またはテキサス・インスツルメンツの製品、サービスと一緒に提供される場合に関係なく、サード・パーティ製品またはサービスの適合性に関する是認、サード・パーティ製品またはサービスの是認の表明を意味するものではありません。

10.1.2 Device Nomenclature

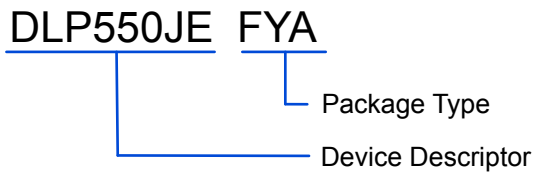


図 10-1. Device Number Description

10.1.3 Device Markings

The device marking includes both human-readable information and a 2-dimensional matrix code. The human readable information is described in 図 10-2. The 2-dimensional matrix code is an alpha-numeric character string that contains the DMD part number, Part 1 of Serial Number, and Part 2 of Serial Number. The first character of the DMD Serial Number (part 1) is the manufacturing year. The second character of the DMD Serial Number (part 1) is the manufacturing month. The last character of the DMD Serial Number (part 2) is the bias voltage bin letter.

Example: *1076-643AB GHXXXXX LLLLLLM

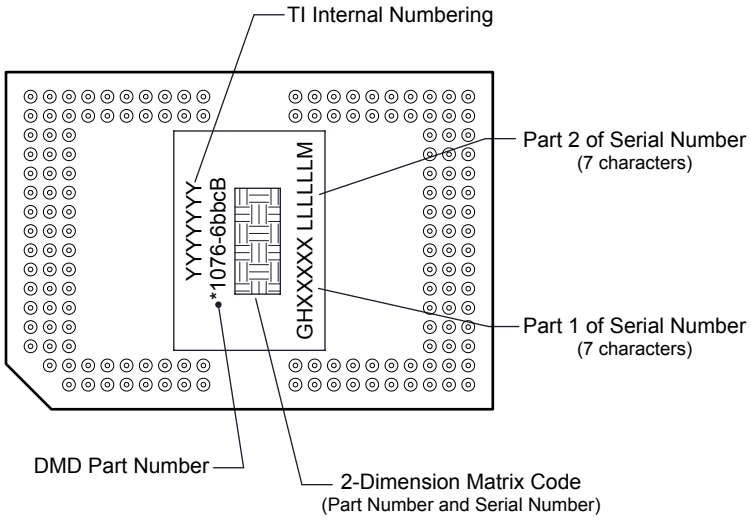


図 10-2. DMD Marking (Device Top View)

10.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

10.2.1 Related Documentation

The following documents contain additional information related to the chipset components used with the DLP470NE.

- *DLPC4430 Display Controller Data Sheet*
- *DLPA100 Power and Motor Driver Data Sheet*

10.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

10.4 Trademarks

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DLP® is a registered trademark of TI.
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10.5 静電気放電に関する注意事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLP550JEFYA	ACTIVE	CPGA	FYA	149	33	RoHS & Green	NI-AU	N / A for Pkg Type	0 to 70		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

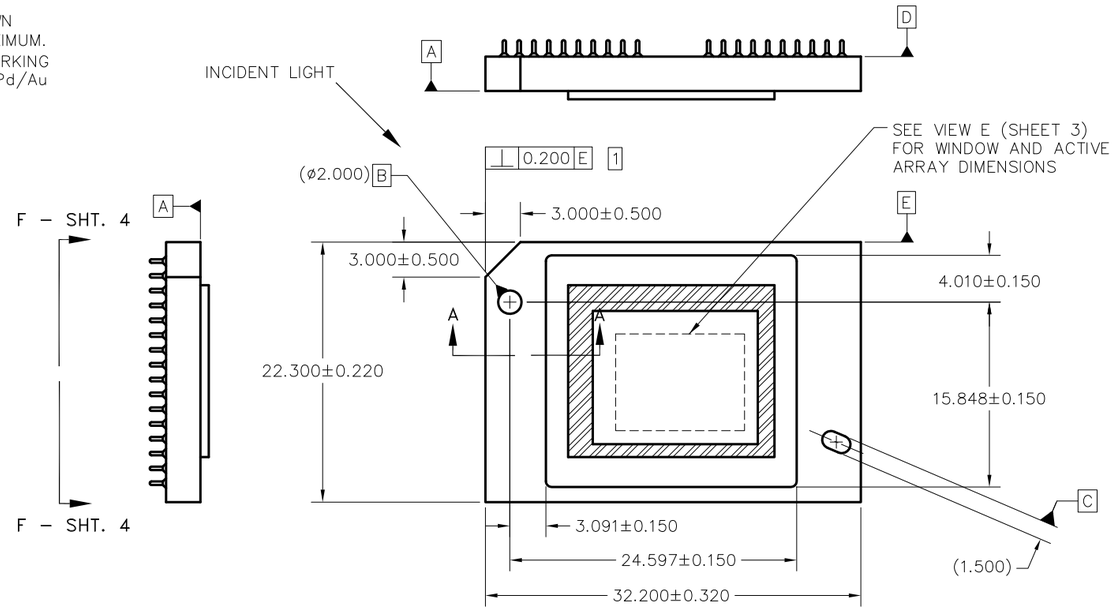
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

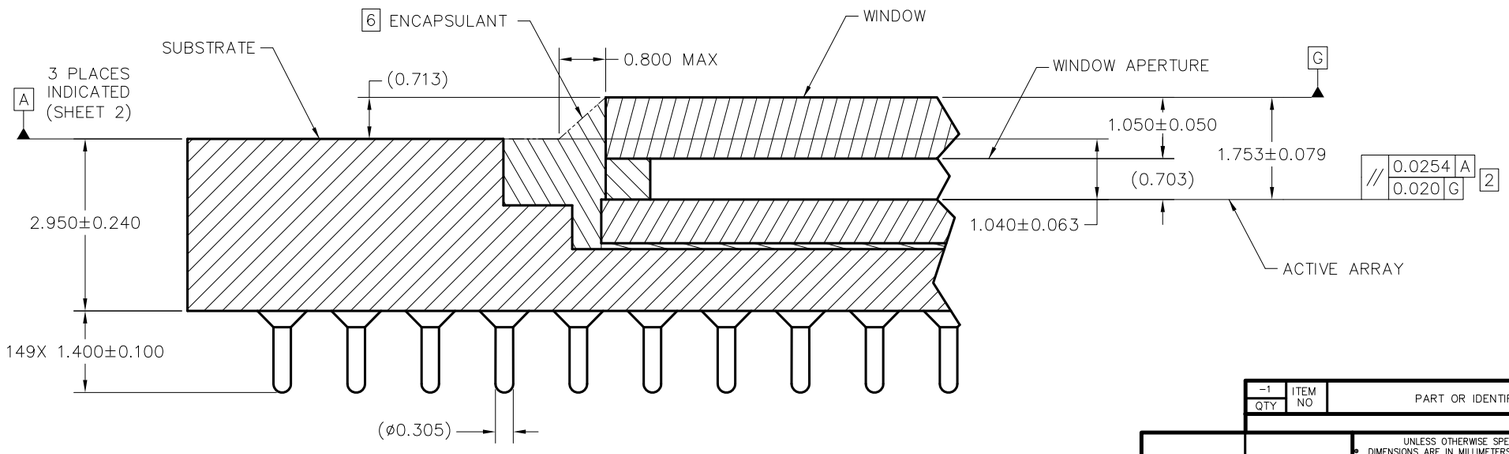
REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	ECO 2121693, INITIAL RELEASE	01/17/2012	F. ARMSTRONG
B	ECO 2123271, CHG TO LARGE SYMBOLIZATION PAD	03/16/2012	F. ARMSTRONG
C	ECO 2135103, ADD NOTE 8 TO SHEETS 1 & 4	08/02/2013	F. ARMSTRONG
D	ECO 2168422, ADD FYA PACKAGE TO TITLE	08/17/17	M. AVERY

NOTES: UNLESS OTHERWISE SPECIFIED:

1. SUBSTRATE EDGE PERPENDICULARITY TOLERANCE APPLIES TO ENTIRE SURFACE
2. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY
3. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.8 DEGREES
4. SUBSTRATE SYMBOLIZATION PAD, AND PLATING AT BOTTOM OF DATUMS B AND C HOLES TO BE ELECTRICALLY CONNECTED TO VSS PLANE WITHIN THE SUBSTRATE
5. BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE AREA
6. MAXIMUM ENCAPSULANT PROFILE SHOWN
7. ENCAPSULANT ALLOWED ON THE SURFACE OF THE CERAMIC IN THE AREA SHOWN IN VIEW B (SHEET 2). ENCAPSULANT SHALL NOT EXCEED 0.200 THICKNESS MAXIMUM.
8. SUBSTRATES PLATED WITH Ni/Au SHALL HAVE THE THREE-DIGIT NUMERICAL MARKING IN THE AREA ABOVE THE SYMBOLIZATION PAD. SUBSTRATES PLATED WITH Ni/Pd/Au SHALL HAVE THE MARKING IN THE AREA BELOW THE SYMBOLIZATION PAD.





SECTION A–A
SCALE 20/1

PARTS LIST

ITEM NO	QTY	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	NOTES
-1				

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- TOLERANCES: ANGLES ± 1°
  2 PLACE DECIMALS ±0.25
  3 PLACE DECIMALS ±0.50
- REMOVE ALL BURRS AND SHARP EDGES
- INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5-1994
- DIMENSIONAL LIMITS APPLY BEFORE PROCESSES
- PARENTHETICAL INFO FOR REF ONLY

		DATE
DWN F. ARMSTRONG		01/17/12
ENGR F. ARMSTRONG		01/17/12
QA P. KONRAD		01/19/12
CQE M. DORAK		01/19/12

THIRD ANGLE PROJECTION

NEXT ASSY	USED ON
NONE	0314DA

APPLICATION

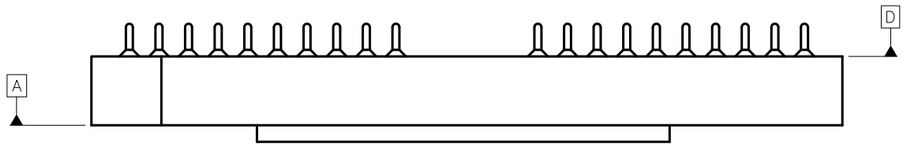
TEXAS INSTRUMENTS
Dallas, Texas

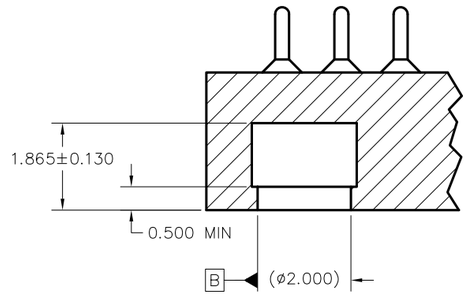
ICD, MECHANICAL, DMD
.55" XGA 2xLVDS V2 SERIES 450
(FYA PACKAGE)

SIZE	DRAWING NO	REV
B	2512194	D

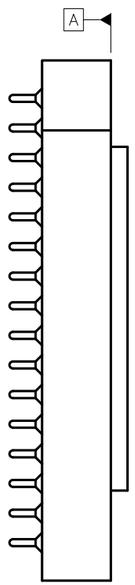
SCALE 4/1 SHEET 1 OF 4

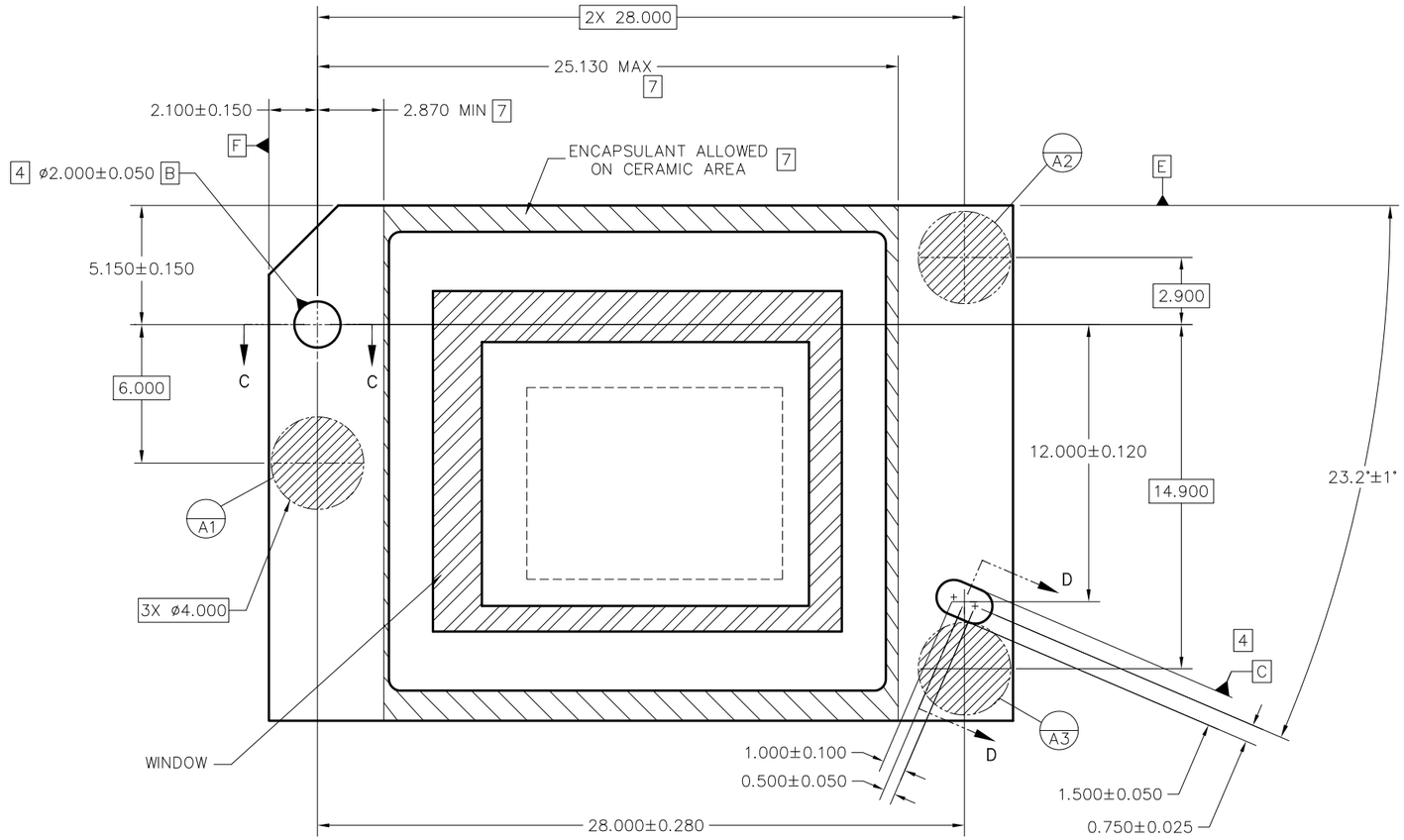
ACED1g



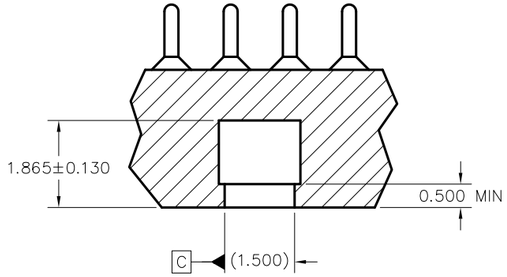


SECTION C–C
DATUM B
SCALE 16/1





VIEW B
DATUMS AND ENCAPSULANT ALLOWABLE AREA
SCALE 8/1



SECTION D–D
DATUM C
SCALE 16/1

TEXAS INSTRUMENTS Dallas, Texas	DWN DATE	SIZE B	DRAWING NO 2512194	REV D
	ISSUE DATE	SCALE 4/1	SHEET 2	

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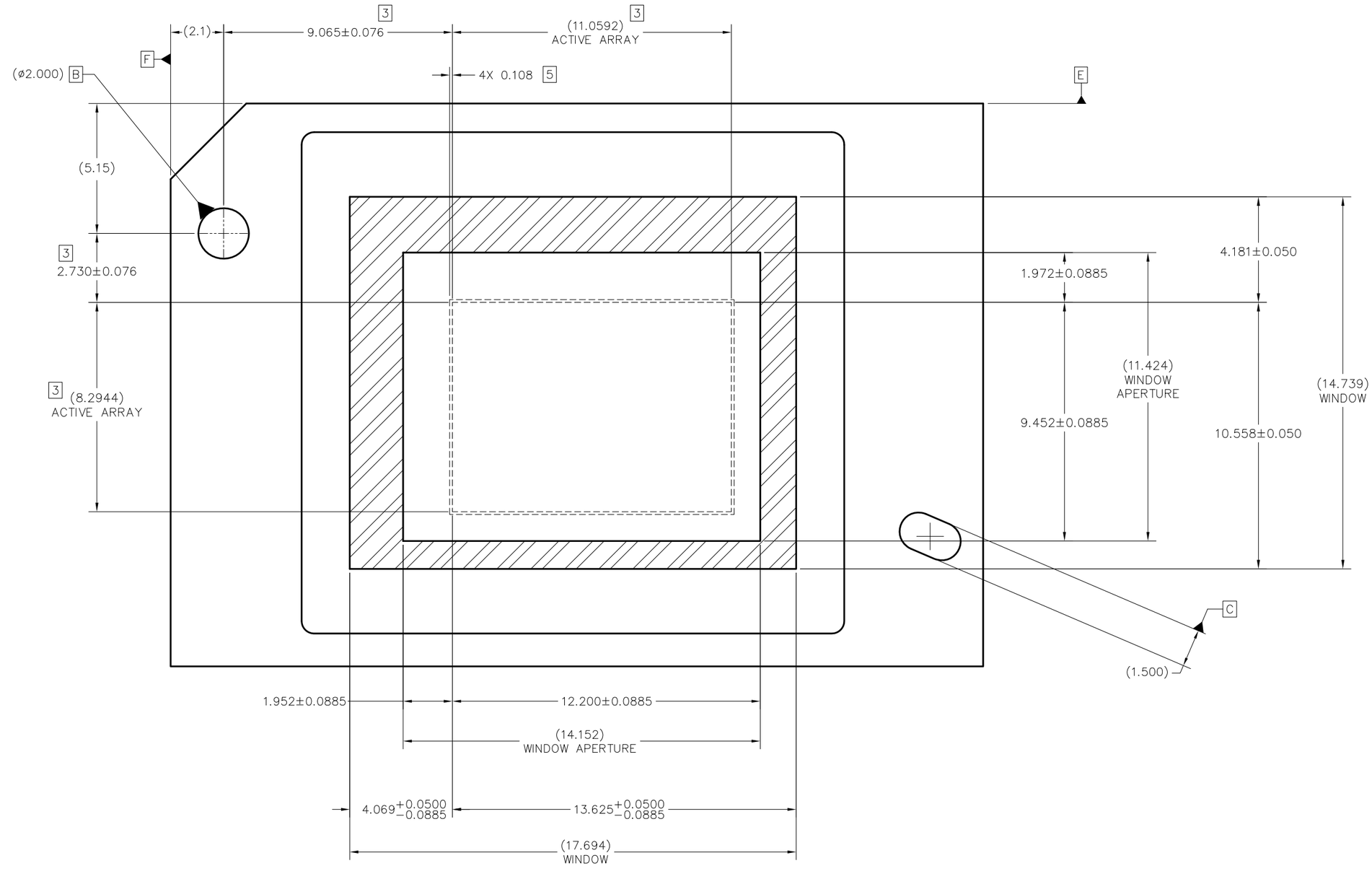

VIEW E (SHEET 1)
DMD WINDOW AND ACTIVE ARRAY
SCALE 12:1

Texas Instruments, Dallas, Texas	DWN DATE / ISSUE DATE	SIZE B	DRAWING NO 2512194	REV D
		SCALE 4/1	SHEET 3	

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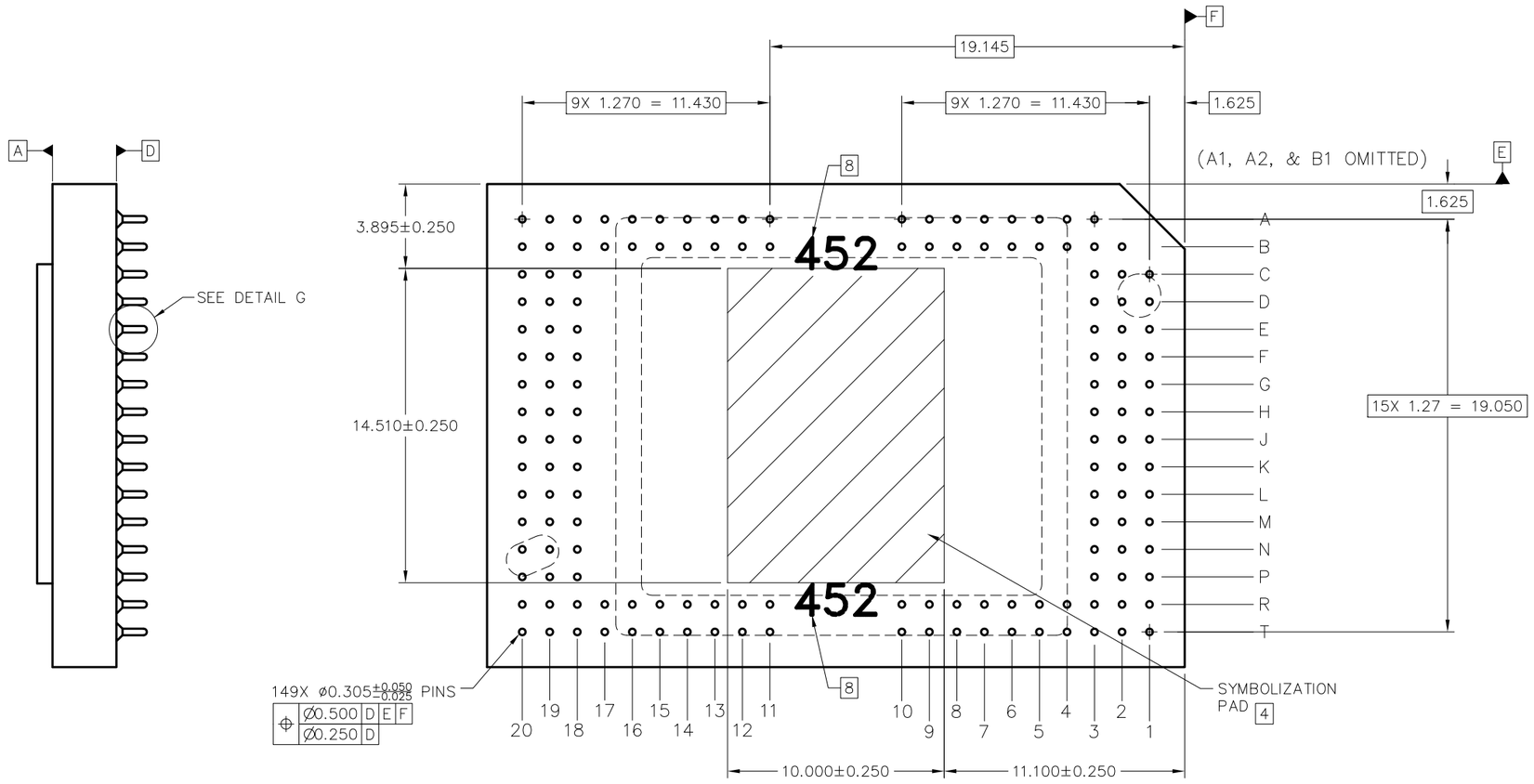
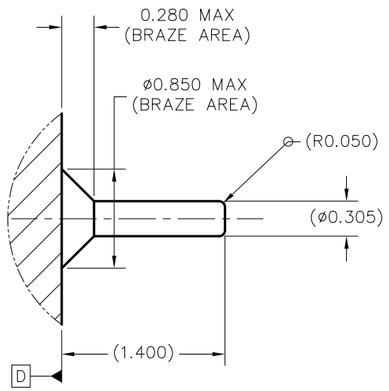


VIEW F–F (SHEET 1)
PINS AND SYMBOLIZATION PAD
SCALE 8/1



DETAIL G (149 PLACES)
PIN & BRAZE DIMENSIONS
SCALE 40/1

Texas Instruments, Dallas, Texas	DWN DATE	SIZE B	DRAWING NO 2512194	REV D
	ISSUE DATE	SCALE 4/1	SHEET 4	

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