TEXAS INSTRUMENTS
DLPA4000
JAJSFJ1 – MAY 2018

DLPA4000 PMICおよび大電流LEDドライバ

1 特長

- ハイサイド・ポンプ機能を搭載した高効率、大電流のRGB LEDドライバ
- 最大32Aの外部降圧FET用のドライバ
- 外部RGBスイッチ用のドライバ
- チャネルごとに10ビットのプログラム可能な電流
- カラー・シーケンシャルRGB LEDの選択用入力
- DMD高電圧電源の生成
- 2つの高効率降圧コンバータによりDLPC4422コントローラとDMDの電源を生成
- ファン・ドライバ・アプリケーションまたは汎用の、高効率な8ビットのプログラマブル降圧コンバータ(PWR6)
- 2つのLDOで補助電圧を供給
- アナログ・マルチプレクサで内部および外部のノードを測定
- 保護機能: サーマル・シャットダウン、ダイ過熱、バッテリ残量減少、低電圧誤動作防止(UVLO)

2 アプリケーション

スマートLEDプロジェクタ
スクリーンレスTV
デジタル・サイネージ
舞台照明

3 概要

DLPA4000デバイスは、高度に統合された電力管理ドライバです。このデバイスは、DLP® LEDプロジェクタ・システム用に最適化されています。DLPA4000はハイサイド・ポンプ機能により、LEDごとに最大32Aのプロジェクタをサポートします。内蔵の高効率降圧コントローラにより、デバイスに電力が供給されます。ドライバ制御スイッチは、R、G、BのLEDのシーケンシングに対応します。このデバイスには5つの降圧コンバータが内蔵され、そのうち2つはDLPC4422コントローラの低電圧電源専用です。別の専用のレギュレートされた電源が、DLPA200 DMDマイクロミラー・ドライバと、DMD用のタイミングが重要な3つのDC電源であるVBIAS、VRST、VOFSに電力を供給します。

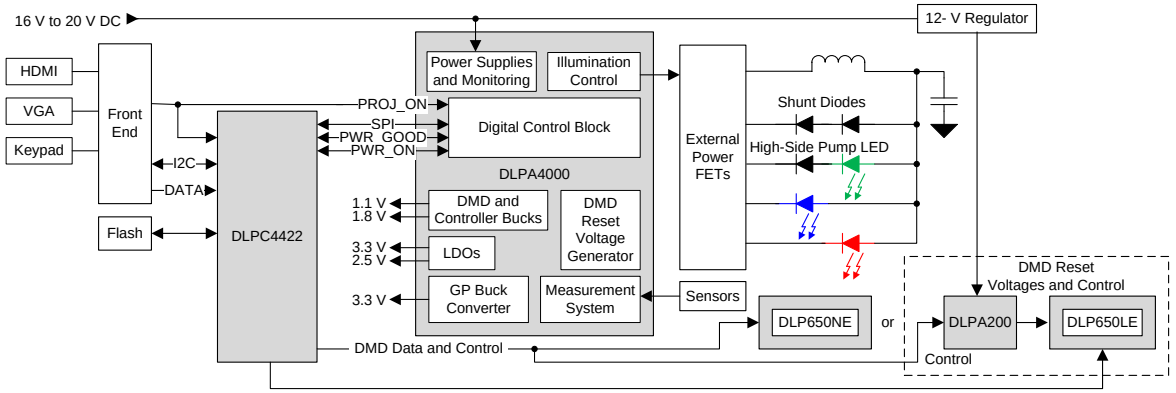
DLPA4000デバイスには、いくつかの補助ブロックが含まれています。これらのブロックにより、LEDプロジェクタのシステムを柔軟に設計できます。8ビットのプログラム可能な降圧コンバータは、RGBプロジェクタのファンを駆動するか、補助電源ラインを形成できます。2つのLDOは、最大200mAの低電流電源を生成できます。これらのLDOは、2.5V～3.3Vでの動作が規定されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
DLPA4000	HTQFP (100)	14.00mm×14.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

システム・ブロック図



目次

4 改訂履歴

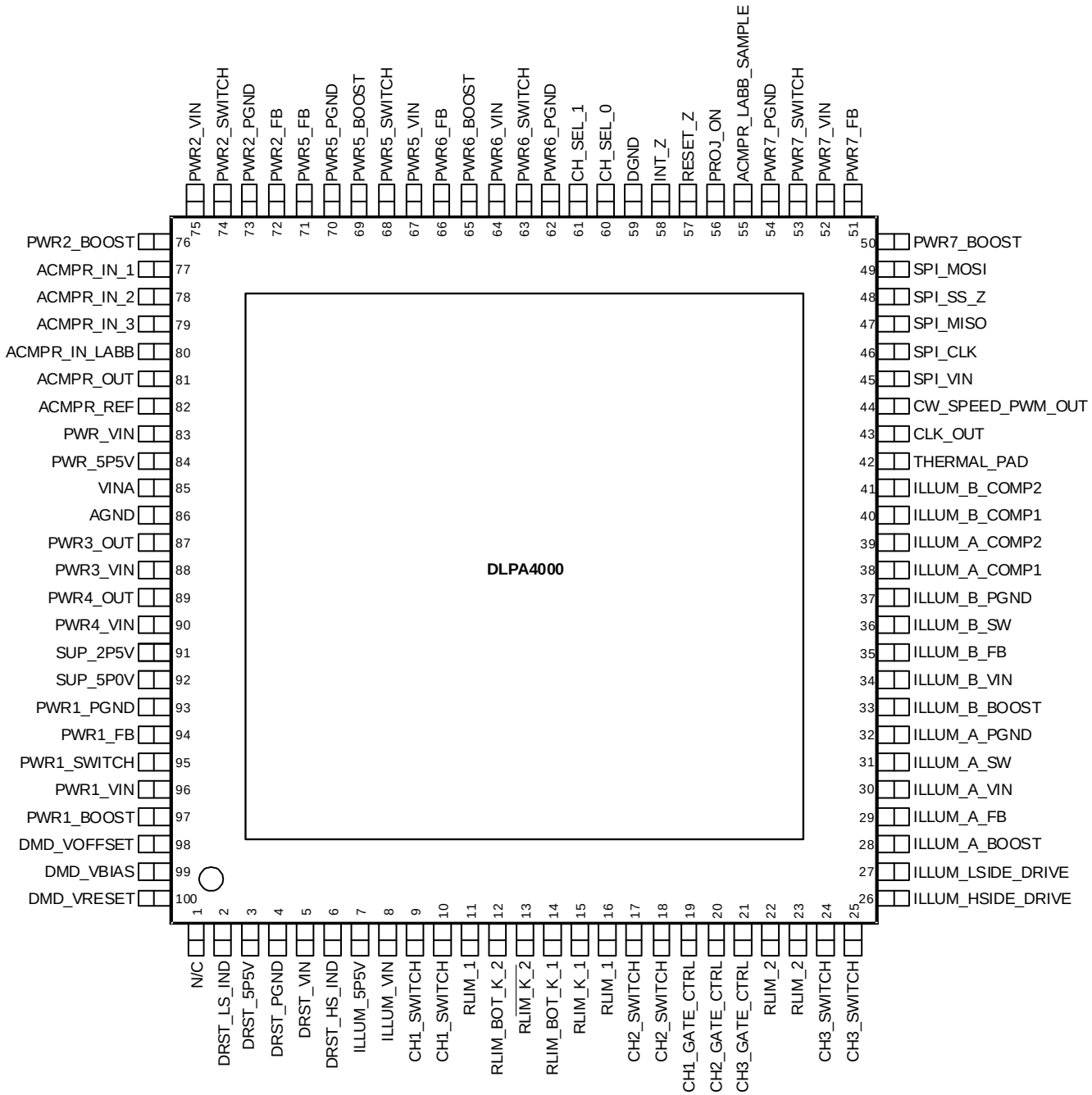
日付	リビジョン	注
2018年5月	*	初版

5 概要（続き)

シリアル・プロトコル・インターフェイス(SPI)により、DLPA4000デバイスのすべてのブロックをアドレス指定できます。このアドレス指定に対応した機能には、システムリセットの生成、電源シーケンシング、アクティブLEDを順に選択するための入力信号、ICの自己保護、および外部ADCにアナログ情報をルーティングするアナログ・マルチプレクサが含まれます。

6 Pin Configuration and Functions

PFD Package
100-Pin HTQFP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
N/C	1	—	No connect
DRST_LS_IND	2	I/O	Connection for the DMD SMPS-inductor (low-side switch).
DRST_5P5V	3	O	Filter pin for LDO DMD. Power supply for internal DMD reset regulator, typical 5.5 V.
DRST_PGND	4	GND	Power ground for DMD SMPS. Connect to ground plane.
DRST_VIN	5	P	Power supply input for LDO DMD. Connect to system power.
DRST_HS_IND	6	I/O	Connection for the DMD SMPS-inductor (high-side switch).
ILLUM_5P5 V	7	O	Filter pin for LDO ILLUM. Power supply for internal ILLUM block, typical 5.5 V.
ILLUM_VIN	8	P	Supply input of LDO ILLUM. Connect to system power.
CH1_SWITCH	9	I	Low-side MOSFET switch for LED Cathode. Connect to RGB LED assembly.
CH1_SWITCH	10	I	Low-side MOSFET switch for LED Cathode. Connect to RGB LED assembly.
RLIM_1	11	O	Connection to LED current sense resistor for CH1 and CH2.
RLIM_BOT_K_2	12	I	Kelvin sense connection to ground side of LED current sense resistor.
RLIM_K_2	13	I	Kelvin sense connection to top side of current sense resistor.
RLIM_BOT_K_1	14	I	Kelvin sense connection to ground side of LED current sense resistor.
RLIM_K_1	15	I	Kelvin sense connection to top side of current sense resistor.
RLIM_1	16	O	Connection to LED current sense resistor for CH1 and CH2.
CH2_SWITCH	17	I	Low-side MOSFET switch for LED cathode. Connect to RGB LED assembly.
CH2_SWITCH	18	I	Low-side MOSFET switch for LED cathode. Connect to RGB LED assembly.
CH1_GATE_CTRL	19	O	Gate control of CH1 external MOSFET switch for LED cathode.
CH2_GATE_CTRL	20	O	Gate control of CH2 external MOSFET switch for LED cathode.
CH3_GATE_CTRL	21	O	Gate control of CH3 external MOSFET switch for LED cathode.
RLIM_2	22	O	Connection to LED current sense resistor for CH3.
RLIM_2	23	O	Connection to LED current sense resistor for CH3.
CH3_SWITCH	24	I	Low-side MOSFET switch for LED Cathode. Connect to RGB LED assembly.
CH3_SWITCH	25	I	Low-side MOSFET switch for LED Cathode. Connect to RGB LED assembly.
ILLUM_HSIDE_DRIVE	26	O	Gate control for external high-side MOSFET for ILLUM Buck converter.
ILLUM_LSIDE_DRIVE	27	O	Gate control for external low-side MOSFET for ILLUM Buck converter.
ILLUM_A_BOOST	28	I	Supply voltage for high-side N-channel MOSFET gate driver. A 100 nF capacitor (typical) must be connected between this pin and ILLUM_A_SW.
ILLUM_A_FB	29	I	Input to the buck converter loop controlling I_{LED}.
ILLUM_A_VIN	30	P	Power input to the ILLUM Driver A.
ILLUM_A_SW	31	I/O	Switch node connection between high-side NFET and low-side NFET. Serves as common connection for the flying high side MOSFET driver.
ILLUM_A_PGND	32	GND	Ground connection to the ILLUM Driver A.
ILLUM_B_BOOST	33	I	Supply voltage for high-side N-channel MOSFET gate driver.
ILLUM_B_VIN	34	P	Power input to the ILLUM driver B.
ILLUM_B_FB	35	I	Input to the buck converter loop controlling I_{LED}.
ILLUM_B_SW	36	I/O	Switch node connection between high-side NFET and low-side NFET.
ILLUM_B_PGND	37	GND	Ground connection to the ILLUM driver B.
ILLUM_A_COMP1	38	I/O	Connection node for feedback loop components
ILLUM_A_COMP2	39	I/O	Connection node for feedback loop components
ILLUM_B_COMP1	40	I/O	Connection node for feedback loop components
ILLUM_B_COMP2	41	I/O	Connection node for feedback loop components
THERMAL_PAD	42	GND	Thermal pad. Connect to clean system ground.
CLK_OUT	43	O	Color wheel clock output
CW_SPEED_PWM_OUT	44	O	Color wheel PWM output
SPI_VIN	45	I	Supply for SPI interface
SPI_CLK	46	I	SPI clock input

Pin Functions (continued)

PIN		I/O	DESCRIPTION
SPI_MISO	47	O	SPI data output
SPI_SS_Z	48	I	SPI chip select (active low)
SPI_MOSI	49	I	SPI data input
PWR7_BOOST	50	I	Charge-pump-supply input for the high-side MOSFET gate drive circuit. Connect 100 nF capacitor between PWR7_BOOST and PWR7_SWITCH pins.
PWR7_FB	51	I	Converter feedback input. Connect to converter output voltage.
PWR7_VIN	52	P	Power supply input for converter.
PWR7_SWITCH	53	I/O	Switch node connection between high-side NFET and low-side NFET.
PWR7_PGND	54	GND	Ground pin. Power ground return for switching circuit.
ACMPR_LABB_SAMPLE	55	I	Control signal to sample voltage at ACMPR_IN_LABB.
PROJ_ON	56	I	Input signal to enable/disable the IC and DLP projector.
RESET_Z	57	O	Reset output to the DLP system (active low). Pin is held low to reset DLP system.
INT_Z	58	O	Interrupt output signal (open drain, active low). Connect to pull-up resistor.
DGND	59	GND	Digital ground. Connect to ground plane.
CH_SEL_0	60	I	Control signal to enable either of CH1,2,3.
CH_SEL_1	61	I	Control signal to enable either of CH1,2,3.
PWR6_PGND	62	GND	Ground pin. Power ground return for switching circuit.
PWR6_SWITCH	63	I/O	Switch node connection between high-side NFET and low-side NFET.
PWR6_VIN	64	P	Power supply input for converter.
PWR6_BOOST	65	I	Charge-pump-supply input for the high-side MOSFET gate drive circuit. Connect 100 nF capacitor between PWR6_BOOST and PWR6_SWITCH pins.
PWR6_FB	66	I	Converter feedback input. Connect to output voltage.
PWR5_VIN	67	P	Power supply input for converter.
PWR5_SWITCH	68	I/O	Switch node connection between high-side NFET and low-side NFET.
PWR5_BOOST	69	I	Charge-pump-supply input for the high-side MOSFET gate drive circuit. Connect 100nF capacitor between PWR5_BOOST and PWR5_SWITCH pins.
PWR5_PGND	70	GND	Ground pin. Power ground return for switching circuit.
PWR5_FB	71	I	Converter feedback input. Connect to output voltage.
PWR2_FB	72	I	Converter feedback input. Connect to output voltage.
PWR2_PGND	73	GND	Ground pin. Power ground return for switching circuit.
PWR2_SWITCH	74	I/O	Switch node connection between high-side NFET and low-side NFET.
PWR2_VIN	75	P	Power supply input for converter.
PWR2_BOOST	76	I	Charge-pump-supply input for the high-side MOSFET gate drive circuit. Connect 100 nF capacitor between PWR2_BOOST and PWR2_SWITCH pins.
ACMPR_IN_1	77	I	Input for analog sensor signal.
ACMPR_IN_2	78	I	Input for analog sensor signal.
ACMPR_IN_3	79	I	Input for analog sensor signal.
ACMPR_IN_LABB	80	I	Input for ambient light sensor, sampled input
ACMPR_OUT	81	O	Analog comparator out
ACMPR_REF	82	I	Reference voltage input for analog comparator
PWR_VIN	83	P	Power supply input for LDO_Bucks. Connect to system power.
PWR_5P5V	84	O	Filter pin for LDO_BUCKS. Internal analog supply for buck converters, typical 5.5 V.
VINA	85	P	Input voltage supply pin for Reference system.
AGND	86	GND	Analog ground pin.
PWR3_OUT	87	O	Filter pin for LDO_2 DMD/DLPC/AUX, typical 2.5 V.
PWR3_VIN	88	P	Power supply input for LDO_2. Connect to system power.
PWR4_OUT	89	O	Filter pin for LDO_1 DMD/DLPC/AUX, typical 3.3 V.
PWR4_VIN	90	P	Power supply input for LDO_1. Connect to system power.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
SUP_2P5V	91	O	Filter pin for LDO_V2V5. Internal supply voltage, typical 2.5 V.
SUP_5P0V	92	O	Filter pin for LDO_V5V. Internal supply voltage, typical 5 V.
PWR1_PGND	93	GND	Ground pin. Power ground return for switching circuit.
PWR1_FB	94	I	Converter feedback input. Connect to output voltage.
PWR1_SWITCH	95	I/O	Switch node connection between high-side NFET and low-side NFET.
PWR1_VIN	96	P	Power supply input for converter.
PWR1_BOOST	97	I	Charge-pump-supply input for the high-side MOSFET gate drive circuit. Connect 100nF capacitor between PWR1_BOOST and PWR1_SWITCH pins.
DMD_VOFFSET	98	O	VOFS output rail. Connect to ceramic capacitor.
DMD_VBIAS	99	O	VBIAS output rail. Connect to ceramic capacitor.
DMD_VRESET	100	O	VRESET output rail. Connect to ceramic capacitor.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature (unless otherwise noted).(1)

		MIN	MAX	UNIT
Voltage	ILLUM_A,B_BOOST	–0.3	28	V
	ILLUM_A,B_BOOST (10 ns transient)	–0.3	30	
	ILLUM_A,B_BOOST vs ILLUM_A,B_SWITCH	–0.3	7	
	ILLUM_LSIDE_DRIVE	–0.3	7	
	ILLUM_HSIDE_DRIVE	–2	28	
	ILLUM_A_BOOST vs ILLUM_HSIDE_DRIVE	-0.3	7	
	ILLUM_A,B_SW	–2	22	
	ILLUM_A,B_SW (10 ns transient)	–3	27	
	PWR_VIN, PWR1_VIN, PWR2_VIN, PWR3_VIN, PWR4_VIN, PWR5_VIN, PWR6_VIN, PWR7_VIN, VINA, ILLUM_VIN, ILLUM_A,B_VIN, DRST_VIN	–0.3	22	
	PWR1_BOOST, PWR2_BOOST, PWR5_BOOST, PWR6_BOOST, PWR7_BOOST	–0.3	28	
	PWR1_BOOST, PWR2_BOOST, PWR5_BOOST, PWR6_BOOST, PWR7_BOOST (10 ns transient)	–0.3	30	
	PWR1_SWITCH, PWR2_SWITCH, PWR5_SWITCH, PWR6_SWITCH, PWR7_SWITCH	–2	22	
	PWR1_SWITCH, PWR2_SWITCH, PWR5_SWITCH, PWR6_SWITCH, PWR7_SWITCH (10 ns transient)	–3	27	
	PWR1_FB, PWR2_FB, PWR5_FB, PWR6_FB, PWR7_FB	–0.3	6.5	
	PWR1_BOOST, PWR2_BOOST, PWR5_BOOST, PWR6_BOOST, PWR7_BOOST vs PWR1_SWITCH, PWR2_SWITCH, PWR5_SWITCH, PWR6_SWITCH, PWR7_SWITCH	–0.3	6.5	
	CH1_SWITCH, CH2_SWITCH, CH3_SWITCH, DRST_LS_IND, ILLUM_A,B_FB	–0.3	20	
	ILLUM_A,B_COMP1, ILLUM_A,B_COMP2, INT_Z, PROJ_ON	–0.3	7	
	DRST_HS_IND	–18	7	
	ACMPR_IN_1, ACMPR_IN_2, ACMPR_IN_3, ACMPR_REF, ACMPR_IN_LABB, ACMPR_LABB_SAMPLE, ACMPR_OUT	–0.3	3.6	
	SPI_VIN, SPI_CLK, SPI_MOSI, SPI_SS_Z, SPI_MISO, CH_SEL_0, CH_SEL_1, RESET_Z	–0.3	3.6	
	RLIM_K_1, RLIM_K_2, RLIM_1, RLIM_2	–0.3	3.6	
	DGND, AGND, DRST_PGND, ILLUM_A,B_PGND, PWR1_PGND, PWR2_PGND, PWR5_PGND, PWR6_PGND, PWR7_PGND, RLIM_BOT_K_1, RLIM_BOT_2	–0.3	0.3	
	DRST_5P5V, ILLUM_5P5V, PWR_5P5, PWR3_OUT, PWR4_OUT, SUP_5P0V	–0.3	7	
	CH1 _GATE_CTRL,CH2_GATE_CTRL, CH3_GATE_CTRL	–0.3	7	
	CLK_OUT	–0.3	3.6	
	CW_SPEED_PWM	–0.3	7	
	SUP_2P5V	–0.3	3.6	
	DMD_VOFFSET	–0.3	12	
	DMD_VBIAS	–0.3	20	
	DMD_VRESET	–18	7	
Source current	RESET_Z, ACMPR_OUT		1	mA
	SPI_DOUT		5.5	
Sink current	RESET_Z, ACMPR_OUT		1	mA
	SPI_DOUT, INT_Z		5.5	
T_{stg}	Storage temperature	–65	150	ºC

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ (1)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (2)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (3)	±500	

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

		MIN	MAX	UNIT
Input voltage range	PWR_VIN, PWR1_VIN, PWR2_VIN, PWR3_VIN, PWR4_VIN, PWR5_VIN, PWR6_VIN, PWR7_VIN, VINA, ILLUM_VIN, ILLUM_A_VIN,ILLUM_B_VIN, DRST_VIN	16	20	V
	CH1_SWITCH, CH2_SWITCH, CH3_SWITCH, ILLUM_A,B_FB,	–0.1	8.6	
	INT_Z, PROJ_ON	–0.1	6	
	PWR1_FB, PWR2_FB, PWR5_FB, PWR6_FB, PWR7_FB	–0.1	5	
	ACMPR_REF, CH_SEL_0, CH_SEL_01, SPI_CLK, SPI_MOSI, SPI_SS_Z	–0.1	3.6	
	RLIM_BOT_K_1, RLIM_BOT_K_2	–0.1	0.1	
	ACMPR_IN_1, ACMPR_IN_2, ACMPR_IN_3, LABB_IN_LABB	–0.1	1.5	
	SPI_VIN	1.7	3.6	
	RLIM_K_1, RLIM_K_2	–0.1	0.25	
	ILLUM_A,B_COMP1, ILLUM_A,B_COMP2	–0.1	5.7	
Ambient temperature range		0	70	°C
Operating junction temperature		0	120	°C

7.4 Thermal Information

THERMAL METRIC (1)		DLPA4000 PFD (HTQFP) 100 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)	7.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance (3)	0.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	N/A	°C/W
ψ_{JT}	Junction-to-top characterization parameter (4)	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter (5)	3.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, but because the device is intended to be cooled with a heatsink from the top case of the package, the simulation includes a fan and heatsink attached to the DLPA4000 device . The heatsink is a 22 mm × 22 mm × 12 mm aluminum pin fin heatsink with a 12 × 12 × 3 mm stud. Base thickness is 2 mm and pin diameter is 1.5 mm with an array of 6 × 6 pins. The heatsink is attached to the DLPA4000 device with 100 um thick thermal grease with 3 W/m-K thermal conductivity. The fan is 20 × 20 × 8 mm with 1.6 cfm open volume flow rate and 0.22 in. water pressure at stagnation.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7), but modified to include the fan and heatsink described in note 2.
(5) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7), but modified to include the fan and heatsink described in note 2.

7.5 Electrical Characteristics

Over operating free-air temperature range. V_{IN} = 19.5 V, T_A = 0 to +40°C, typical values are at T_A = 25°C, Configuration according to *Typical Application* (V_{IN} =19.5 V, I_{OUT} = 32 A, LED, external MOSFETs) (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLIES						
INPUT VOLTAGE						
V_{IN}	Input voltage range	VINA – pin	16(1)	19.5	20	V
V_{LOW_BAT}	Low battery warning threshold	VINA falling (via 5 bit trim function, 0.5 V steps)	3.9		18.4	V
	Hysteresis	VINA rising		90		mV
V_{UVLO}	UVLO threshold	VINA falling (via 5 bit trim function, 0.5 V steps)	3.9		18.4	V
	Hysteresis	VINA rising		90		mV
$V_{STARTUP}$	Startup voltage	DMD_VBIAS, DMD_VOFFSET, DMD_VRESET loaded with 10 mA	6			V
INPUT CURRENT						
I_{IDLE}	Idle current	IDLE mode, all VIN pins combined		15		µA
I_{STD}	Standby current	STANDBY mode, analog, internal supplies and LDOs enabled, DMD, ILLUMINATION and BUCK CONVERTERS disabled.		3.7		mA
I_{Q_DMD}	Quiescent current (DMD)	Quiescent current DMD block (in addtion to I_{STD}), VINA + DRST_VIN		0.49		mA
I_{Q_ILLUM}	Quiescent current (ILLUM)	Quiescent current ILLUM block (in addtion to I_{STD}), V_openloop= 3 V (0x18, ILLUM_OLV_SEL), VINA + ILLUM_VIN + ILLUM_A_VIN + ILLUM_B_VIN		21		mA
I_{Q_BUCK}	Quiescent current (per BUCK)	Quiescent current per BUCK converter (in addtion to I_{STD}), Normal mode, VINA + PWR_VIN + PWR1,2,5,6,7_VIN, PWR1,2,5,6,7_VOUT = 1 V		4.3		mA
		Quiescent current per BUCK converter (in addtion to I_{STD}), Normal mode, VINA + PWR_VIN + PWR1,2,5,6,7_VIN, PWR1,2,5,6,7_VOUT = 5 V		15		
		Quiescent current per BUCK converter (in addtion to I_{STD}), Cycle-skipping mode, VINA + PWR_VIN + PWR1,2,5,6,7_VIN = 1 V		0.41		
		Quiescent current per BUCK converter (in addtion to I_{STD}), Cycle-skipping mode, VINA + PWR_VIN + PWR1,2,5,6,7_VIN = 5 V		0.46		
I_{Q_TOTAL}	Quiescent current (Total)	Typical Application: ACTIVE mode, all VIN pins combined, DMD, ILLUMINATION and PWR1,2 enabled, PWR3,4,5,6,7 disabled.		38		mA
INTERNAL SUPPLIES						
V_{SUP_5P0V}	Internal supply, analog			5		V
V_{SUP_2P5V}	Internal supply, logic			2.5		V
DMD - LDO DMD						

(1) VIN must be higher than the UVLO voltage setting, including after accounting for AC noise on VIN, for the DLPA4000 device to fully operate. While 15.5 V is the min VIN voltage supported, TI recommends that the UVLO is never set below 16 V. 16 V gives margin above the minimum to protect against the case where someone suddenly removes VIN's power supply which causes the VIN voltage to drop rapidly. Failure to keep VIN above 16.0 V before the mirrors are parked and VOFS, VRST, and VBIAS supplies are properly shut down can result in permanent damage to the DMD. Because 16 V is 500 mV above 15.5 V, when UVLO trips there is time for the DLPA4000 device and DLPC343x to park the DMD mirrors and do a fast shut down of supplies VOFS, VRST, and VBIAS. Regardless of the UVLO setting, , include enough bulk capacitance on VIN inside the projector to maintain VIN above 15.5 V for at least 100 µs after VIN power supply is suddenly removed causing a UVLO fault.

Electrical Characteristics (continued)

Over operating free-air temperature range. V_{IN} = 19.5 V, T_A = 0 to +40°C, typical values are at T_A = 25°C, Configuration according to *Typical Application* (V_{IN} =19.5 V, I_{OUT} = 32 A, LED, external MOSFETs) (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DRST_VIN}			6	12	20	V
V_{DRST_5P5V}				5.5		V
PGOOD	Power good DRST_5P5V	Rising		80%		
		Faling		60%		
OVP	Overvoltage protection DRST_5P5V			7.2		V
	Regulator dropout	At 25 mA, VDRST_VIN= 5.5 V		56		mV
	Regulator current limit(2)		300	340	400	mA
DMD - BUCK CONVERTERS						
OUTPUT VOLTAGE						
$V_{PWR\_1\_VOUT}$	Output Voltage			1.1		V
$V_{PWR\_2\_VOUT}$	Output Voltage			1.8		V
	DC output voltage accuracy	I_{OUT}= 0 mA	–3%		3%	
MOSFET						
$R_{ON,H}$	High side switch resistance	25°C, $V_{PWR\_1,2\_Boost} – V_{PWR1,2\_SWITCH}$ = 5.5 V		150		mΩ
$R_{ON,L}$	Low side switch resistance(2)	25°C		85		mΩ
LOAD CURRENT						
	Allowed Load Current.				3	A
I_{OCL}	Current limit(2)	L_{OUT}= 3.3 µH	3.2	3.6	4.2	A
ON-TIME TIMER CONTROL						
t_{ON}	On time	V_{IN} = 12 V, V_O = 5 V		120		ns
$t_{OFF(MIN)}$	Minimum off time(2)	T_A = 25°C, V_{FB} = 0 V		270		ns
START-UP						
	Soft start		1	2.5	4	ms
PGOOD						
$Ratio_{OV}$	Overvoltage protection			120%		
$Ratio_{PG}$	Relative power good level	Low to High		72%		
ILLUMINATION - LDO ILLUM						
V_{ILLUM_VIN}			6	12	20	V
V_{ILLUM_5P5V}				5.5		V
PGOOD	Power good ILLUM_5P5V	Rising		80%		
		Falling		60%		
OVP	Overvoltage protection ILLUM_5P5V			7.2		V
	Regulator dropout	At 25 mA, V_{ILLUM_VIN} = 5.5 V		53		mV
	Regulator current limit(2)		300	340	400	mA
ILLUMINATION - DRIVER A,B						
V_{ILLUM_A,B_IN}	Input supply voltage range		6	12	20	V
PWM						
f_{SW}	Oscillator frequency	3 V < V_{IN} < 20 V		600		kHz
t_{DEAD}	Output driver dead time	HDRV off to LDRV on, TRDLY = 0		28		ns
		HDRV off to LDRV on, TRDLY = 1		40		
		LDRV off to HDRV on, TRDLY = 0		35		
OUTPUT DRIVERS						

(2) Not production tested.

Electrical Characteristics (continued)

Over operating free-air temperature range. V_{IN} = 19.5 V, T_A = 0 to +40°C, typical values are at T_A = 25°C, Configuration according to *Typical Application* (V_{IN} =19.5 V, I_{OUT} = 32 A, LED, external MOSFETs) (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{HDHI}	High-side driver pull-up resistance	$V_{ILLUM\_A,B\_BOOT} – V_{ILLUM\_A,B\_SW}$ = 5 V, I_{HDRV} = –100 mA		4.9		Ω
R_{HDLO}	High-side driver pull-down resistance	$V_{ILLUM\_A,B\_BOOT} – V_{ILLUM\_A,B\_SW}$ = 5 V, I_{HDRV} = 100 mA		3		Ω
R_{LDHI}	Low-side driver pull-up resistance	I_{LDRV} = –100 mA		3.1		Ω
R_{LDLO}	Low-side driver pull-down resistance	I_{LDRV} = 100 mA		2.4		Ω
t_{HRISE}	High-side driver rise time(2)	C_{LOAD} = 5 nF		23		ns
t_{HFALL}	High-side driver fall time(2)	C_{LOAD} = 5 nF		19		ns
t_{LRISE}	Low-side driver rise time(2)	C_{LOAD} = 5 nF		23		ns
t_{LFALL}	Low-side driver fall time(2)	C_{LOAD} = 5 nF		17		ns
OVERCURRENT PROTECTION						
HSD OC	High-Side Drive Over Current threshold	External switches, V_{DS} threshold(2).		185		mV
BOOT DIODE						
V_{DFWD}	Bootstrap diode forward voltage	I_{BOOT} = 5 mA		0.75		V
PGOOD						
RatioUV	Undervoltage protection			89%		
INTERNAL RGB STROBE CONTROLLER SWITCHES						
R_{ON}	ON-resistance	CH1,2,3_SWITCH		30	45	mΩ
I_{LEAK}	OFF-state leakage current	V_{DS}= 5.0 V			0.1	µA
I_{MAX}	Maximum current			6		A
DRIVERS EXTERNAL RGB STROBE CONTROLLER SWITCHES						
CHx_GATE_CNTR_HIGH	Gate control high level	ILLUM_SW_ILIM_EN[2:0] = 7, register 0x02, I_{SINK}= 400 µA		4.35		V
		ILLUM_SW_ILIM_EN[2:0] = 0, register 0x02, I_{SINK}= 400 µA		5.25		
CHx_GATE_CNTR_LOW	Gate control low level	ILLUM_SW_ILIM_EN[2:0] = 7, register 0x02, I_{SINK}= 400 µA		55		mV
		ILLUM_SW_ILIM_EN[2:0] = 0, register 0x02, I_{SINK}= 400 µA		55		
LED CURRENT CONTROL						
V_{LED_ANODE}	LED Anode voltage(2)	Ratio with respect to V_{ILLUM_A,B_VIN} (Duty cycle limitation).	0.85x			
					8.6	V
I_{LED}	LED currents	V_{ILLUM_A,B_VIN} ≥ 8 V. See register SWx_IDAC[9:0] for settings.	1		32	A
	DC current offset, CH1,2,3_SWITCH	R_{LIM} = 4 mΩ	–150	0	150	mA
	Transient LED current limit range (programmable)	20% higher than I_{LED}. Min-setting, R_{LIM}= 4 mΩ.		11%		
		20% higher than I_{LED}. Max-setting, R_{LIM}= 4 mΩ. Percentage of max current.		133%		
t_{RISE}	Current rise time	I_{LED} from 5% to 95%, I_{LED} = 600 mA, transient current limit disabled(2).			50	µs
BUCK CONVERTERS - LDO_BUCKS						
V_{PWR_VIN}	Input voltage range PWR1,2,5,6,7_VIN		16	19.5	20	V
V_{PWR_5P5V}	PWR_5P5V			5.5		V

Electrical Characteristics (continued)

Over operating free-air temperature range. V_{IN} = 19.5 V, T_A = 0 to +40°C, typical values are at T_A = 25°C, Configuration according to *Typical Application* (V_{IN} =19.5 V, I_{OUT} = 32 A, LED, external MOSFETs) (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PGOOD	Power good PWR_5P5V	Rising		80%		
		Falling		60%		
OVP	Overvoltage Protection PWR_5P5V			7.2		V
	Regulator dropout	At 25 mA, V_{PWR_VIN}= 5.5 V		41		mV
	Regulator current limit(2)		300	340	400	mA
BUCK CONVERTERS - GENERAL PURPOSE BUCK CONVERTERS (3)						
OUTPUT VOLTAGE						
$V_{PWR\_5,6,7\_VOUT}$	Output Voltage (General Purpose Buck1,2,3)	8-bit programmable	1		5	V
	DC output voltage accuracy	I_{OUT}= 0 mA	–3.5%		3.5%	
MOSFET						
$R_{ON,H}$	High-side switch resistance	25°C, $V_{PWR5,6,7\_Boost} – V_{PWR5,6,7\_SWITCH}$ = 5.5 V		150		mΩ
$R_{ON,L}$	Low-side switch resistance(2)	25°C		85		mΩ
LOAD CURRENT						
	Allowed load current PWR6.			2		A
	Allowed load current PWR5, PWR7.	Buck converters should not be used.				A
I_{OCL}	Current limit(2)	L_{OUT}= 3.3 µH	3.2	3.6	4.2	A
ON-TIME TIMER CONTROL						
t_{ON}	On time	V_{IN} = 12 V, V_O = 5 V		120		ns
$t_{OFF(min)}$	Minimum off time(2)	T_A = 25°C, V_{FB} = 0 V		270	310	ns
START-UP						
t_{SS}	Soft-start period		1	2.5	4	ms
PGOOD						
$Ratio_{OV}$	Overvoltage protection			120%		
$Ratio_{PG}$	Relative power good level	Low to High		72%		
AUXILIARY LDOs						
$V_{PWR3,4\_VIN}$	Input voltage range	LDO1 (PWR4), LDO2 (PWR3)	3.3	12	20	V
PGOOD	Power good PWR3_VOUT, PWR4_VOUT	PWR3_VOUT and PWR4_VOUT rising		80%		
		PWR3_VOUT and PWR4_VOUT falling		60%		
OVP	Overvoltage Protection PWR3_VOUT, PWR4_VOUT			7		V
	DC output voltage accuracy PWR3_VOUT, PWR4_VOUT	I_{OUT}= 0 mA	–3%		3%	
	Regulator current limit(2)		300	340	400	mA
t_{ON}	Turn-on time	to 80% of V_{OUT} = PWR3 and PWR4, C = 1 µF		40		µs
LDO2 (PWR3)						
V_{PWR3_VOUT}	Output Voltage PWR3_VOUT			2.5		V
	Load Current capability			200		mA
	DC Load regulation PWR3_VOUT	V_{OUT}= 2.5 V, 5 ≤ I_{OUT} ≤ 200 mA		–70		mV/A

(3) General Purpose Buck2 (PWR6) currently supported, others may be available in the future.

Electrical Characteristics (continued)

Over operating free-air temperature range. V_{IN} = 19.5 V, T_A = 0 to +40°C, typical values are at T_A = 25°C, Configuration according to *Typical Application* (V_{IN} =19.5 V, I_{OUT} = 32 A, LED, external MOSFETs) (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	DC Line regulation PWR3_VOUT	V_{OUT}= 2.5 V, I_{OUT}= 5 mA, 3.3 ≤ PWR3_VIN ≤ 20 V		30		µV/V
LDO1 (PWR4)						
V_{PWR4_VOUT}	Output Voltage PWR4_VOUT			3.3		V
	Load Current capability			200		mA
	DC Load regulation PWR4_VOUT	V_{OUT}= 3.3 V, 5 ≤ I_{OUT} ≤ 200 mA		–70		mV/A
	DC Line regulation PWR4_VOUT	V_{OUT}= 3.3 V, I_{OUT}= 5 mA, 4 ≤ PWR4_VIN ≤ 20 V		30		µV/V
	Regulator dropout	I_{OUT} = 25 mA, V_{OUT}= 3.3 V, V_{PWR4_VIN}= 3.3 V		48		mV
MEASUREMENT SYSTEM						
AFE						
G	Amplifier gain (PGA)	AFE_GAIN[1:0] = 01		1		V/V
		AFE_GAIN[1:0] = 10		9.5		
		AFE_GAIN[1:0] = 11		18		
V_{OFS}	Input referred offset voltage	PGA, AFE_CAL_DIS = 1 (2)	–1		1	mV
		Comparator (2)	–1.5		+1.5	
τ_{RC}	Settling time	To 1% of final value (2).		46	67	µs
		To 0.1% of final value (2).		69	100	
$V_{ACMPR\_IN\_1,2,3}$	Input voltage Range ACMPR_IN_1,2,3		0		1.5	V
LABB						
τ_{RC}	Settling time	To 1% of final value (2).		4.6	6.6	µs
		To 0.1% of final value (2).		7	10	
$V_{ACMPR\_IN\_LABB}$	Input voltage range ACMPR_IN_LABB		0		1.5	V
	Sampling window ACMPR_IN_LABB	Programmable per 7 µs	7		28	µs
COLOR WHEEL PWM						
CLK_OUT	Clock output frequency			2.25		MHz
$V_{CW\_SPEED\_PWM\_OUT}$	Voltage range CW_SPEED_PWM_OUT	Average value programmable in 16 bits	0		5	V
DIGITAL CONTROL - LOGIC LEVELS AND TIMING CHARACTERISTICS						
V_{SPI}	SPI supply voltage range	SPI_VIN	1.7		3.6	V
V_{OL}	Output low-level	RESETZ, CMP_OUT, CLK_OUT. I_O = 0.3 mA sink current	0		0.3	V
		SPI_DOUT. I_O = 5 mA sink current	0		0.3 × V_{SPI}	
		INTZ. I_O = 1.5 mA sink current	0		0.3 × V_{SPI}	
V_{OH}	Output high-level	RESETZ, CMP_OUT, CLK_OUT. I_O = 0.3 mA source current	1.3		2.5	V
		SPI_DOUT. I_O = 5 mA source current	0.7 × V_{SPI}		V_{SPI}	
V_{IL}	Input low-level	PROJ_ON, LED_SEL0, LED_SEL1	0		0.4	V
		SPI_CSZ, SPI_CLK, SPI_DIN	0		0.3 × V_{SPI}	
V_{IH}	Input high-level	PROJ_ON, LED_SEL0, LED_SEL1	1.2			V
		SPI_CSZ, SPI_CLK, SPI_DIN	0.7 × V_{SPI}		V_{SPI}	

Electrical Characteristics (continued)

Over operating free-air temperature range. V_{IN} = 19.5 V, T_A = 0 to +40°C, typical values are at T_A = 25°C, Configuration according to *Typical Application* (V_{IN} =19.5 V, I_{OUT} = 32 A, LED, external MOSFETs) (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{BIAS}	Input bias current	V_{IO}= 3.3 V, any digital input pin			0.1	µA
SPI_CLK	SPI clock frequency(4)	Normal SPI mode, DIG_SPI_FAST_SEL = 0, f_{OSC} = 9 MHz	0		36	MHz
		Fast SPI mode, DIG_SPI_FAST_SEL = 1, V_{SPI}> 2.3 V, f_{OSC} = 9 MHz	20		40	
$t_{DEGLITCH}$	Deglitch time	LED_SEL0, LED_SEL1(2).		300		ns
INTERNAL OSCILLATOR						
f_{OSC}	Oscillator frequency			9		MHz
	Frequency accuracy	T_A= 0 to 70°C	–5%		5%	
THERMAL SHUTDOWN						
T_{WARN}	Thermal warning (HOT threshold)			120		°C
	Hysteresis			10		
T_{SHTDWN}	Thermal shutdown (TSD threshold)			150		°C
	Hysteresis			15		

(4) Maximum depends linearly on oscillator frequency f_{OSC}.

7.6 SPI Timing Parameters

SPI_VIN = 3.6 V ± 5%, T_A = 0 to 40ºC, C_L = 10 pF (unless otherwise noted).

		MIN	NOM	MAX	UNIT
f_{CLK}	Serial clock frequency	0		40	MHz
t_{CLKL}	Pulse width low, SPI_CLK, 50% level	10			ns
t_{CLKH}	Pulse width high, SPI_CLK, 50% level	10			ns
t_t	Transition time, 20% to 80% level, all signals	0.2		4	ns
t_{CSCR}	SPI_SS_Z falling to SPI_CLK rising, 50% level	8			ns
t_{CFCS}	SPI_CLK falling to SPI_CSZ rising, 50% level			1	ns
t_{CDS}	SPI_MOSI data setup time, 50% level	7			ns
t_{CDH}	SPI_MOSI data hold time, 50% level	6			ns
t_{iS}	SPI_MISO data setup time, 50% level	10			ns
t_{iH}	SPI_MISO data hold time, 50% level	0			ns
t_{CFDO}	SPI_CLK falling to SPI_MISO data valid, 50% level		13		ns
t_{CSZ}	SPI_CSZ rising to SPI_MISO HiZ		6		ns

8 Detailed Description

8.1 Overview

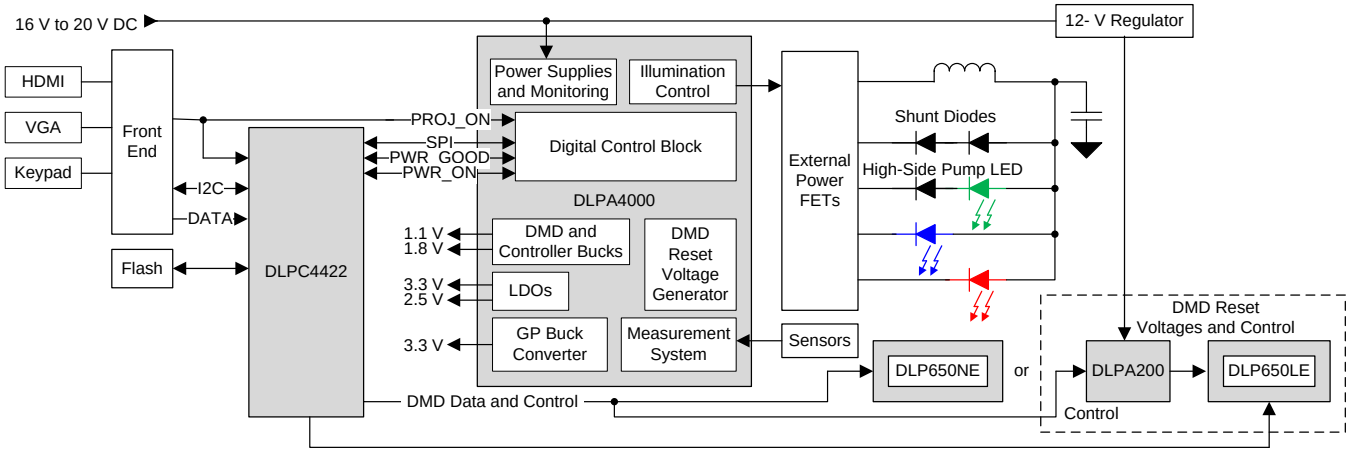
The DLPA4000 device is a highly integrated power management driver optimized for DLP 1500 to 3000 lumen LED projectors . It targets accessory applications up to several hundreds of lumen and is designed to support a wide variety of high-current LEDs. *Functional Block Description* shows a typical DLP high-side pumped LED 1500-3000 lumen projector implementation.

Part of the projector is the projector module, which is an optimized combination of components consisting of, for instance, LEDs, DMD, control chip, memory, and optional sensors and fans. The front-end chip controls the projector module. More information about the system and projector module configuration can be found in a separate application note.

The device blocks are listed below and discussed in detail in this data sheet:

- Supply and Monitoring: Creates internal supply and reference voltages and has functions such as thermal protection
- Illumination: Block to control the light. Contains drivers, strobe decoder for the LEDs and power conversion
- External Power FETs: Capable for 32 A and High-Side Pump
- DMD Supply: Generates voltages and their specific timing for the DMD. Contains regulators and DMD/DLPC buck converters
- Buck Converter: General purpose buck converter
- Auxiliary LDOs: Fixed voltage LDOs for customer usage
- Measurement System: Analog front end to measure internal and external signals
- Programming: SPI interface, digital control

8.2 Functional Block Description



8.3 Feature Description

8.3.1 Supply and Monitoring

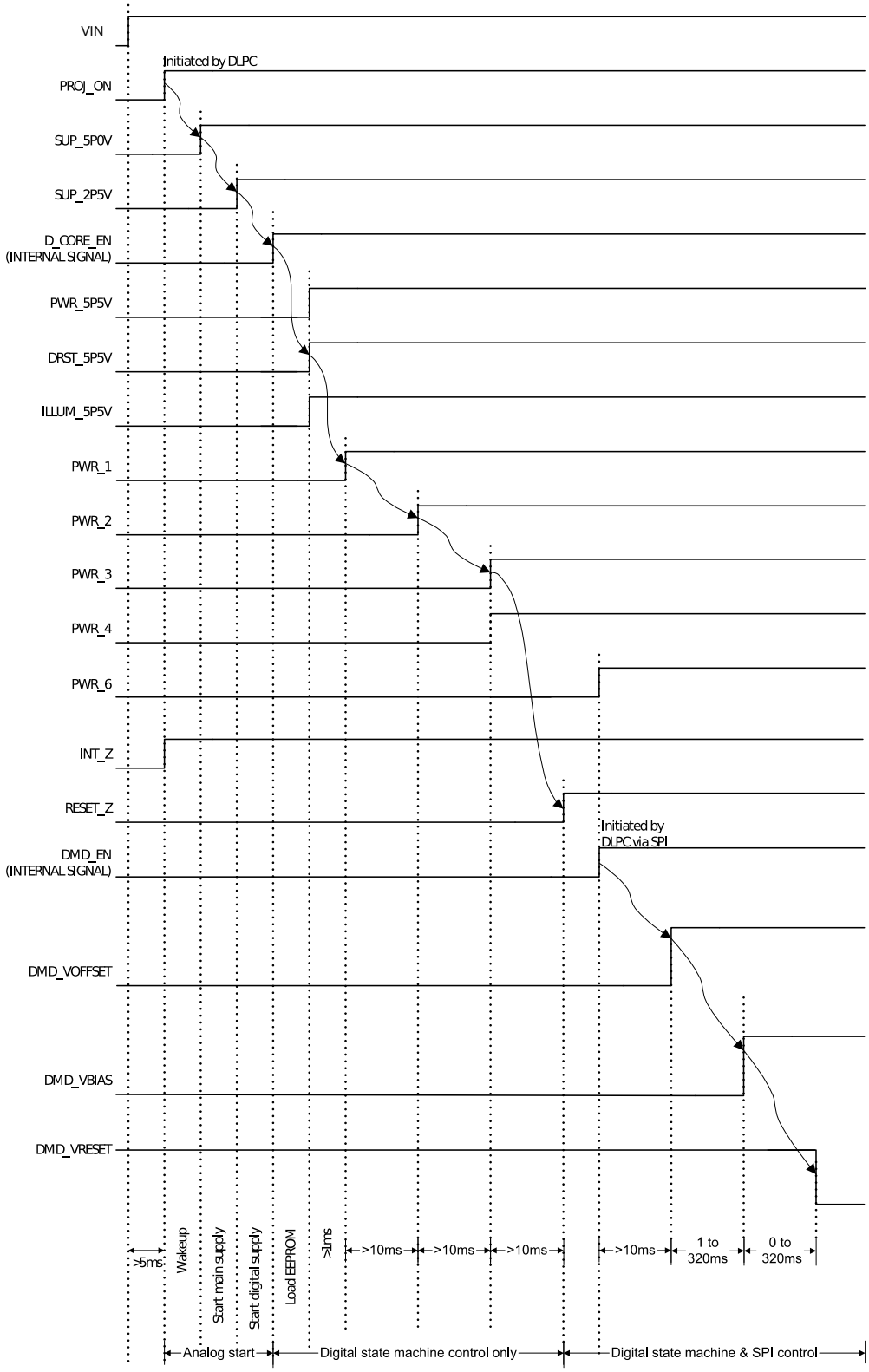
This block generates internal supply voltages and monitors device behavior.

8.3.1.1 Supply

The specified input supply voltage for main supply (VIN) is between 16 V and 20 V. The typical specification is 19.5 V. When the device energizes, several internal power supplies become energized sequentially.(Figure 1). A sequential startup ensures that all the different blocks start in a certain order and prevent excessive startup currents. The main control to start the device is the control pin *PROJ_ON*. Once set high the *basic* analog circuitry is started that is needed to operate the digital and SPI interface. This circuitry is supplied by two LDO regulators that generate 2.5 V (SUP_2P5V) and 5 V (SUP_5P0V). These regulator voltages internal only. Do not load these regulator voltages externally. Make sure the output capacitance is 2.2 µF for the 2.5-V LDO (pin 91) and 4.7 µF for the 5-V LDO, (pin 92). After the LDO voltages reach the regulator levels, the digital core starts, and the Digital State Machine (DSM) controls the device.

Subsequently, the 5.5-V LDOs for various blocks start: PWR_5V5V, DRST_5P5V and ILLUM_5P5V. Then the DLPC buck converters (PWR_1 & PWR_2) start and followed by the DMD LDOs (PWR_3 & PWR_4).The device enables and is controllable by the DLPC (indicated by RESET_Z going high). At this point the general purpose buck converter (PWR_6) can start. Lastly the regulator that supplies the DMD starts. The DMD regulator generates the timing critical VOFFSET, VBIAS, and VRESET supplies.

Feature Description (continued)



Note: Arrows indicate sequence of events automatically controlled by digital state machine. Other events are initiated under SPI control.

Figure 1. Powerup Timing

Feature Description (continued)

8.3.1.2 Monitoring

The DLPA4000 device monitors and reports faults occurrence and fault type. Register 0x0C stores the fault type .The device generates an interrupt signal whenever a fault occurs. The user can configure fault conditions in 0x0D.

8.3.1.2.1 Block Faults

The device can detect fault conditions for supplies such as the low voltage supplies (SUPPLY_FAULT). ILLUM_FAULT monitors correct supply and voltage levels in the illumination block. DMD_FAULT monitors a correctly functioning DMD block. The PROJ_ON_INT bit indicates when PROJ_ON asserts.

8.3.1.2.2 Low Battery and UVLO

The low voltage warning signal (BAT_LOW_WARN) and voltage low shutdown (BAT_LOW_SHUT) signal monitor the input voltage (VIN) (see Figure 2). These signals warn for a low VIN supply voltage or automatically shutdown the device when the VIN supply drops below a predefined level. The threshold levels for these fault conditions can be set from 3.9 V to 18.4 V by writing to registers 0x10<4:0> (LOWBATT) and 0x11<4:0> (BAT_LOW_SHUT_UVLO). Figure 3 shows the threshold level hysteresis and its dependence on the selected threshold voltage. Set the low voltage higher than the undervoltage lockout threshold to generate a warning before the device shuts down.

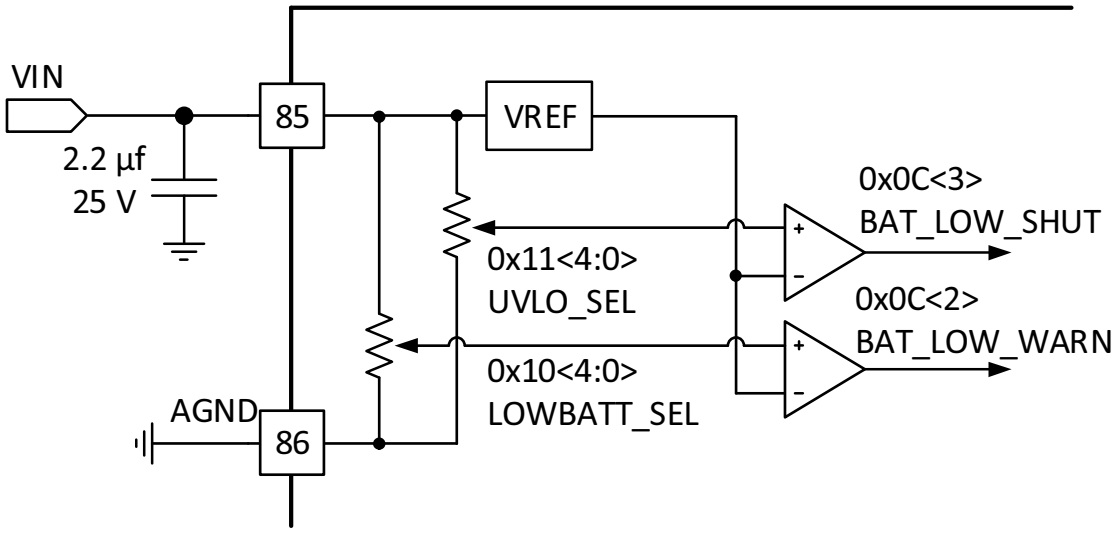


Figure 2. Voltage Monitoring

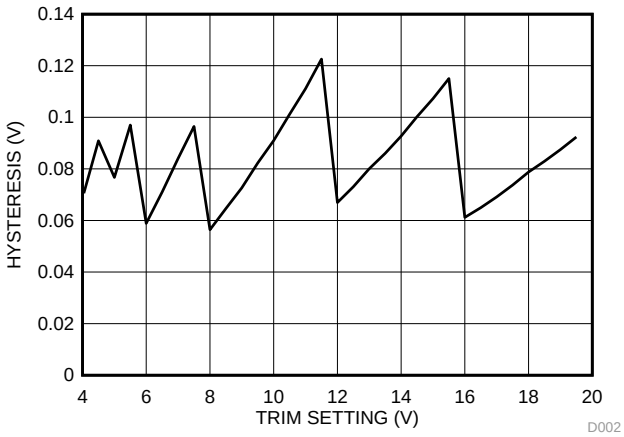


Figure 3. Hysteresis on V_{LOW_BAT} and V_{UVLO}

Feature Description (continued)

8.3.1.2.3 Thermal Protection

The device constantly monitors the chip temperature to prevent overheating. There are two levels of fault condition for register 0x0C. The first level is an overheat warning (TS_WARN). The overheat warning indicates when the chip reaches a critically high temperature. The second level (TS_SHUT) indicates when the chip reaches a higher temperature than the TS_WARN level. The device shuts down the device to prevent permanent damage when it reaches the TS_SHUT level. Both temperature faults have hysteresis levels to prevent rapid switching when the temperature is near the threshold.

8.3.2 Illumination

The illumination function includes all blocks needed to generate light for the DLP system. The device uses a control loop to accurately set the current through the LEDs (see Figure 4). Use IDAC[9:0] to set the intended LED current. The Illumination driver controls the LED anode voltage V_{LED} and as a result a current flows through one of the LEDs. The voltage across the sense resistor (R_{LIM}) measures the LED current. Based on the difference between the actual and intended current, the loop controls the output of the buck converter (V_{LED}) higher or lower. Switches P, Q, and R control the LED which conducts the current. The *Openloop feedback circuitry"* confirms that the control loop can be closed for cases when there is no path via the LED (for instance, when I_{LED}= 0 A).

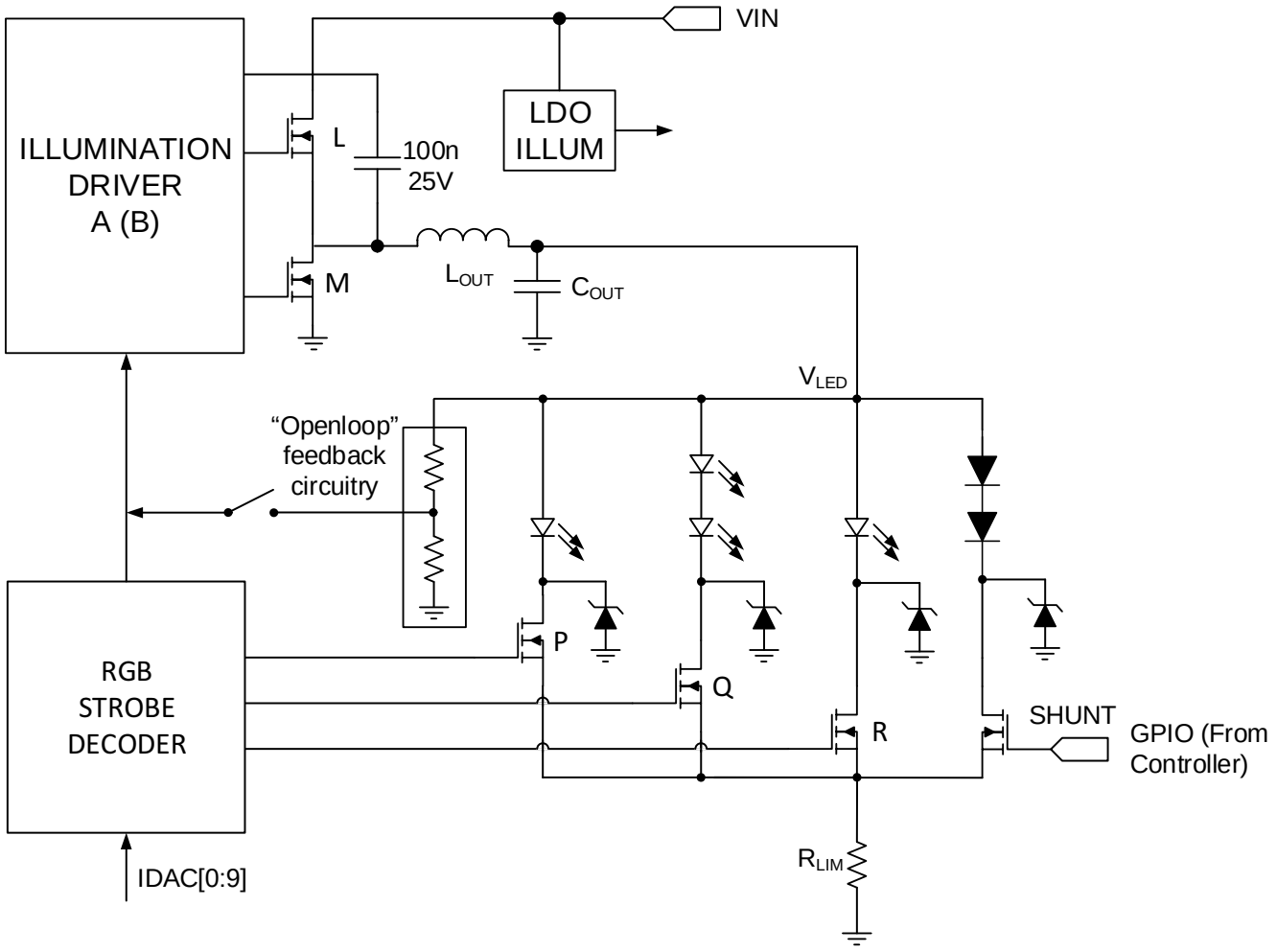


Figure 4. Illumination Control Loop

These blocks comprise the illumination control loop.

- Programmable gain block

Feature Description (continued)

- LDO illum, analog supply voltage for internal illumination blocks
- Illumination driver A, primary driver for the external FETs
- RGB strobe decoder, driver for external switches to control the on-off rhythm of the LEDs and measures the LED current

8.3.2.1 Programmable Gain Block

IDAC registers 0x03h to 0x08h determine the current through the LEDs, which is measured through the sense resistor R_{LIM}. The device compares the voltage across R_{LIM} with the current setting from the IDAC registers. The loop regulates the current to the set value.

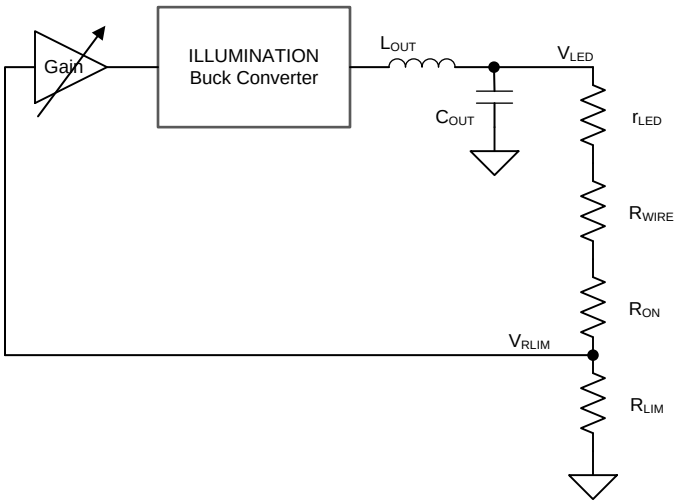


Figure 5. Programmable Gain Block in the Illumination Control Loop

When current flows through an LED, a forward voltage builds up across the LED. The LED acts as a (low) differential resistance that is part of the load circuit for V_{LED}. Together with the wire resistance (R_{WIRE}) and the on-resistance (R_{ON}) of the MOSFET switch, the device creates a voltage divider with the R_{LIM} resistor that is a factor in the loop gain of the I_{LED} control. During normal conditions, the loop produces a well-regulated LED current up to 32 A.

Because this voltage divider is a component of the control loop, make sure to consider issues such as resistance and attenuation. For instance, when the application includes two LEDs connected in series, or when the application has relatively high wiring resistance, the loop gain reduces due to the extra attenuation caused by the increased series resistance of r_{LED} + R_{WIRE} +R_{ON}. As a result, the loop response time lowers. To compensate for this increased attenuation, increase the loop gain by selecting a higher gain for the programmable gain block. Use register 0x25h [3:0] to set the gain increase.

During normal operation the default gain setting (00h) suffices. In case of two LEDs connected in series a gain setting 01h or 02h suffices.

Wiring resistance also impacts the control-loop performance. Avoid unnecessary large wire length in the loop. Maintain a wiring resistance as low as possible to yield the highest efficiency. When wiring resistance continues to impact the response time of the loop, select an appropriate setting of the gain block. Also be aware of connector resistance and PCB tracks. Every milli-ohm of resistance counts.

8.3.2.2 LDO Illumination

A dedicated regulator to the illumination block provides an analog power supply of 5.5 V to the internal circuitry. Add a 1-µF capacitor to the input of the LDO and to the output of the LDO.

Feature Description (continued)

8.3.2.3 Illumination Driver A

The illumination driver of the DLPA4000 comprises a buck controller for driving two external low-ohmic N-channel MOSFETs Figure 6). The application note *Understanding Buck Power Stages in Switchmode Power Supplies* (SLVA057) explains buck converter operation theory. Proper operation requires careful selection of the external components, especially the inductor L_{OUT} and the output capacitor C_{OUT}. For best efficiency and ripple performance, choose an inductor and capacitor with low equivalent series resistance (ESR).

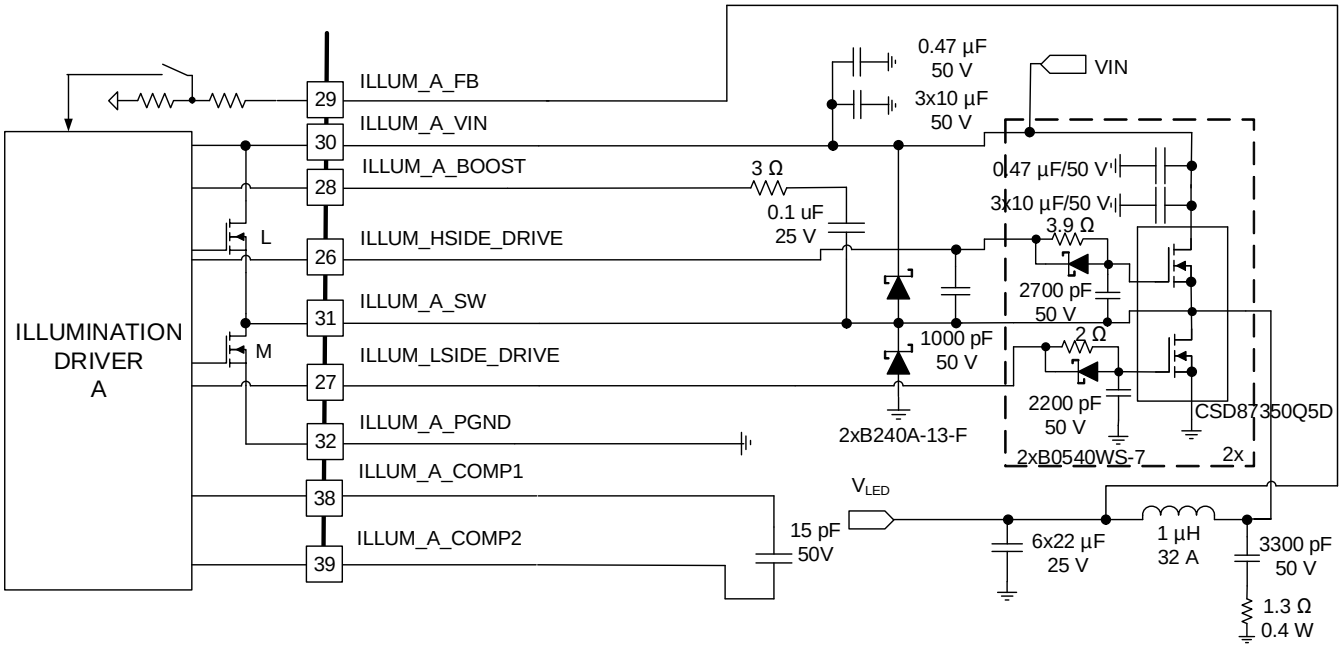


Figure 6. Typical Illumination Driver Configuration

Several factors determine the component selection of the buck converter, including input voltage (VIN), desired output voltage (V_{LED}) and the allowed output current ripple. The first step of the configuration is to select the inductor L_{OUT}.

Select the value of the inductance of a buck power stage so that the peak-to-peak ripple current flowing in the inductor remains within a certain range. Here, the target is set to have an inductor current ripple, k_{I_RIPPLE}, less than 0.174 (17.4%). The minimum inductor value can be calculated given the input and output voltage, output current, switching frequency of the buck converter (f_{SWITCH}= 600 kHz), and inductor ripple of 0.174 (17.4%):

$$L_{OUT} = \frac{\frac{V_{OUT}}{V_{IN}} \cdot (V_{IN} - V_{OUT})}{k_{I\_RIPPLE} \cdot I_{OUT} \cdot f_{SWITCH}} \quad (1)$$

Example: V_{IN}= 19.5 V, V_{OUT}= 4.3 V, I_{OUT}= 32 A results in an inductor value of L_{OUT}= 1µH

Determine the output capacitor, C_{OUT} after selecting the inductor. Calculate the value considering that the frequency compensation of the illumination loop is designed for an LC-tank resonance frequency of 13.8 kHz:

$$f_{RES} = \frac{1}{2 \cdot \pi \cdot \sqrt{L_{OUT} \cdot C_{OUT}}} \quad (2)$$

Example: C_{OUT}= 132 µF given that L_{OUT}= 1 µH. A practical value is 6 × 22 µF. Here, a parallel connection of two capacitors is chosen to lower the ESR even further.

The selected inductor and capacitor determine the output voltage ripple. The resulting output voltage ripple V_{LED_RIPPLE} is a function of the inductor ripple k_{I_RIPPLE}, output current I_{OUT}, switching frequency f_{SWITCH} and the capacitor value C_{OUT}:

Feature Description (continued)

$$V_{LED\_RIPPLE} = \frac{k_{I\_RIPPLE} \cdot I_{OUT}}{8 \cdot f_{SWITCH} \cdot C_{OUT}} \quad (3)$$

Example: K_{I_RIPPLE}= 0.174, I_{OUT}= 32 A, f_{SWITCH}= 600 kHz and C_{OUT}= 6 x 22 µF results with an appropriately small level of 8.8 mVpp.

It is strongly advised to keep the capacitance value low. The larger the capacitor value the more energy is stored. When the LED voltage falls, stored energy must dissipate. Current discharges when stored energy dissipates. Use Equation 4 to calculate the theoretical peak reverse current caused by a large voltage drop.

$$I_{2(max)} = \sqrt{\frac{C_{OUT}}{L_{OUT}} \times ((V_1)^2 - (V_2)^2) + (I_1)^2} \quad (4)$$

where

- V_1 is the starting V_{LED}
- V_2 is the ending V_{LED}
- I_1 is the LED current

8.3.2.4 External MOSFETs

Depending on the type of external MOSFETs selected, consider adding any or all of the components described in this section. TI recommends the user include placeholders for these components in the board design.

8.3.2.4.1 Gate series resistor (R_G)

Use gate series resistors to slow the turn-on transient of the power FET, if needed. Because the device switches large currents, a fast turn-on transient time potentially risks switch-node ringing. Slowing down the turn-on transient time reduces the edge steepness of the drain current waveform, The reduction of the edge steepness results in a reduction of the induced inductive ringing. A resistance of a few Ohms typically suffices.

8.3.2.4.2 Gate series diode (D_G)

The turn-off transient time of the power FET includes gate series resistance also. This resistance potentially affects on the non-overlap timing negatively. In order to maintain a fast turn-off transient time for the power FET, use a diode in parallel with the gate series resistance. The cathode of the diode shunts the current at the gate series resistor which results in a fast turn-off transient time. to the DLPA4000 device which results in a fast turn-off transient time.

8.3.2.4.3 Gate parallel capacitance (C_G)

Use gate parallel capacitance specifically for higher supply voltages. The gate of a disabled power MOSFET can be pulled high parasitically due to a large drain voltage swing and the drain-gate capacitance,

In the low-side MOSFET this voltage swing can happen at the end of the non-overlap time while the power converter supplies current. In this case the switch node is low at the end of the non-overlap time. The switch node pulls high when the high-side MOSFET starts. Due to the large and steep waveform edge of the switch node current, the drain-gate capacitance of the low-side MOSFET injects the charge into the gate of the low-side FET. This situation causes the low-side MOSFET to operate for a short period of time causing a shoot-through current.

A similar situation exists with high-side FET. While the power converter discharges the LED voltage (V_{LED}) the device directs the power converter current inward. At the end of the non-overlap time the switch node is high. If at that moment the low-side MOSFET is enabled, via the gate-drain capacitance of the high-side MOSFET charge is being injected into the gate of the high-side MOSFET potentially causing the device to switch on for a short amount of time. That switch-on behavior causes a shoot through current as well.

Add more gate-source filter capacitance to reduce the effect of the charge injection via the drain-source capacitance. In the case where a linear voltage division exists between gate-source capacitance and gate-drain capacitance, and for a 20-V supply voltage, maintain a ratio of gate-source capacitance and gate-drain capacitance to approximately 1:10 or larger. Make sure to test the gate-drive signals and the switch node for potential cross conduction.

Feature Description (continued)

Sometimes a design can include dual MOSFETs to dissipate power (heat). Consider the configurations shown in Figure 7 tp prevent parasitic gate-oscillation a structure. In this example, the device isolates each gate with a resistor (R_{ISO}) to dampen potential oscillations. A resistance of 1 Ω is typically sufficient.

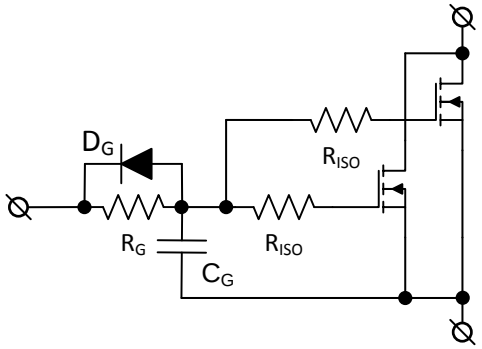


Figure 7. Using R_{ISO} to Prevent Gate Oscillations When Using Power MOSFETs in Parallel

A buck converter design requires at least two capacitors. Make sure that the value of the input-capacitor pin (ILLUM_A_VIN) is equal or greater than the selected output capacitance C_{OUT}, in this case ≥ 2 × 68 µF.

8.3.2.5 RGB Strobe Decoder

The DLPA4000 can sequentially control the three color-LEDs (red, green and blue). This circuitry consists of three drivers to control external switches, the actual strobe decoder and the LED current control (Figure 8). The N-channel MOSFET switches are connected to the cathode terminals of the external LED package. These switches start and stop the currents through the LEDs.

Feature Description (continued)

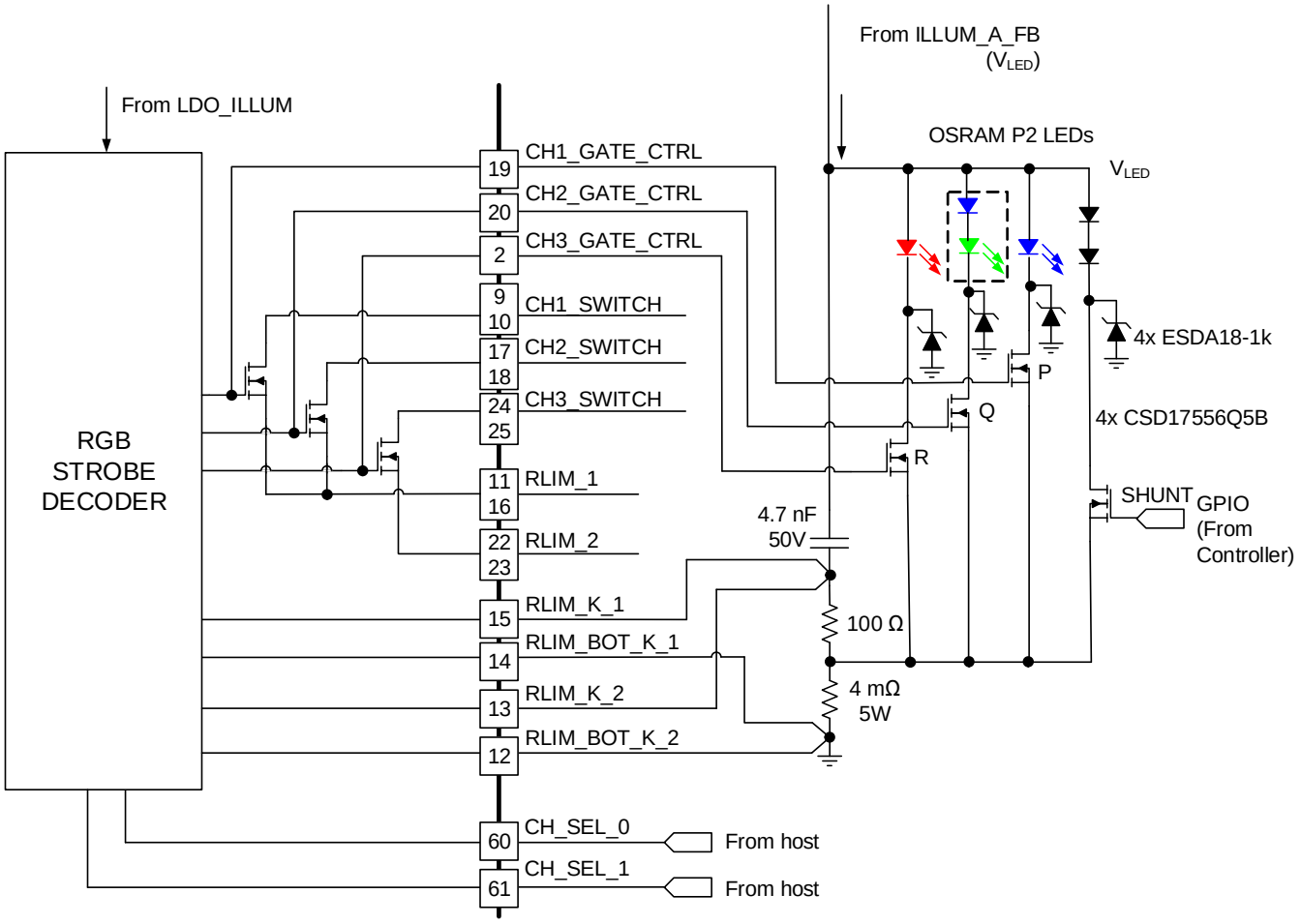


Figure 8. Switch Connection for a Common-Anode LED Assembly

The CH_SEL_0 and CH_SEL_1 pins control the N-channel MOSFET P, Q, and R signals. The CH_SEL[1:0] registers typically receive a rotating code switching from RED to GREEN to BLUE and then back to RED. Table 1 lists the relationship between CH_SEL[0:1] and the switch positions.

Table 1. Switch Positions for Common Anode RGB LEDs

PINS CH_SEL[1:0	SWITCH			IDAC REGISTER
	P	Q	R	
00	Open	Open	Open	N/A
01	Closed	Open	Open	0x03 and 0x04 SW1_IDAC[9:0]
10	Open	Closed	Open	0x05 and 0x06 SW2_IDAC[9:0]
11	Open	Open	Closed	0x07 and 0x08 SW3_IDAC[9:0]

CH_SEL[1:0] functions to start one of the switches, CH_SEL[1:0] but it also selects a 10-bit current setting for the control IDAC that is used as the set current for the LED. The device uses this set current in addition to the measured current through R_{LIM} to control the illumination driver to the appropriate V_{LED}. Registers 0x03 to 0x08 (Table 1). independently set the current through the three LEDs.

Each current level can be set from *off* to 150mV/R_{LIM} in 1023 steps:

$$I_{LED\,A} = \frac{\text{Bit Value} + 1}{1024} \times \frac{150\ \text{mV}}{R_{LIM}} \quad (5)$$

The maximum current for $R_{LIM}$is 4.7 mΩ, so the I_{LEDA} is 32 A. However, the reference design includes a more common 4-mΩ value with a less than maximum IDAC value for 32 A.

The device requires a minimum LED current of 5% of I_{LED_MAX} to operate correctly.

8.3.2.5.1 Break Before Make (BBM)

The operation of the three LED N-channel MOSFET switches (P, Q, R) follows a break-before-make control. The device returns a switch to the OPEN position first before the device sets the subsequent switch to the CLOSED position (BBM), Figure 9. The BBM register (0x0E) controls the dead-time between closing one swtich and opening another. Switches that are intended to remain closed do not opened during the BBM delay time.

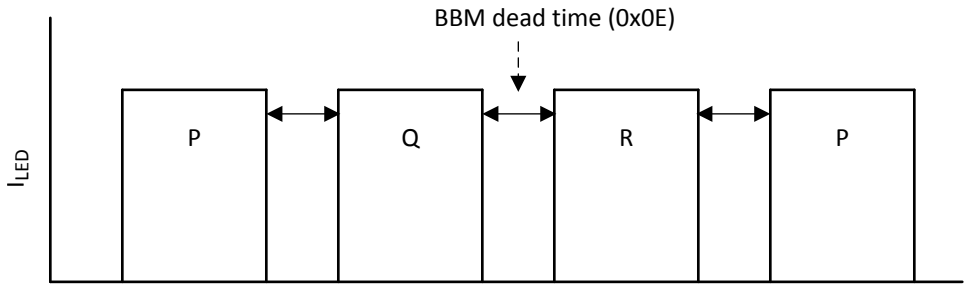


Figure 9. Break-Before-Make Timing

8.3.2.5.2 Openloop Voltage

in some case, there is no control loop for the buck converter through the LED. To prevent the output voltage of the buck converter to vary inconsistently, use an internal resistive divider to close the loop is closed as shown in Figure 4. Open loop voltage control is active:

- during the BBM period. Transitions from one LED to another implies that during the BBM time all LEDs are off.
- when the current setting for all three LEDs is 0.

It's important to set the open loop voltage to approximately equal the lowest LED forward voltage. Use register 0x18 to set the open loop voltage between 3 V and 18 V in steps of 1 V.

8.3.2.5.3 Transient Current Limit

Typically the forward voltages of the green diodes and the blue diodes are equivalent to each other (between 3 V and 5 V). However the forward voltage of the red diode is significantly lower (2 V to 4 V). This difference can lead to a current spike in the RED diode when the strobe controller switches from green or blue to red. The spike occurs because the LED voltage (V_{LED}) is initially higher than required to drive the red diode. DLPA4000 limits the transient current for each switch in the LEDs during the transition. Use register 0x02 (ILLUM_ILIM) to control the transient current limit. A typical application requires this limit for only for the RED diode. Set the value for ILLUM_ILIM to at least 20% higher than the DC regulation current. Use the three bits of register 0x02 (ILLUM_SW_ILIM_EN) to select which switch controls the transient current limiting feature. Figure 10 and Figure 11 show the effect of the transient current limit on the LED current.

For high-side pump applications, where there are two series stacked LEDs for green, sequence precautions are needed to avoid damaging the LEDS. Always transition from high-side pump green to blue, avoid following the green with red.

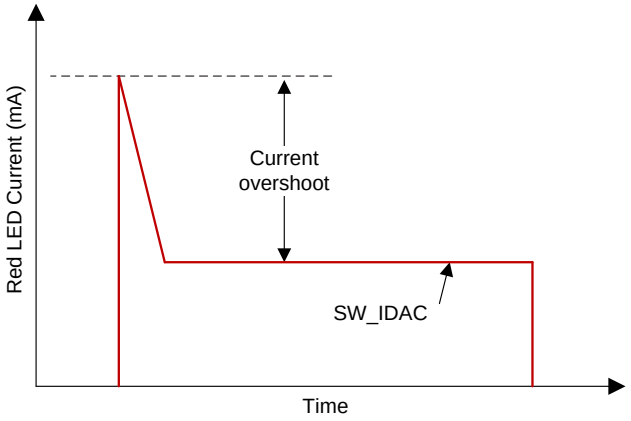


Figure 10. LED Current Without Transient Current Limit

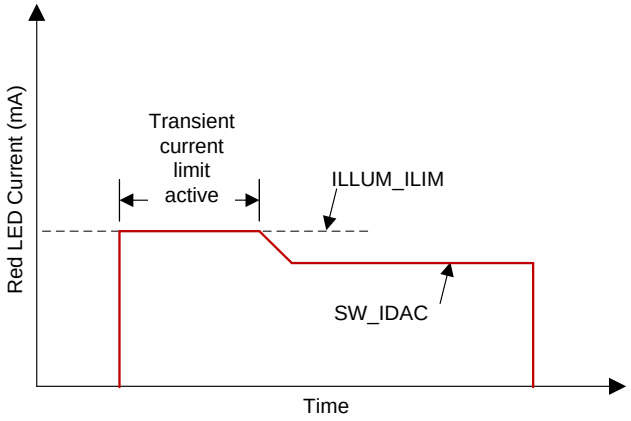


Figure 11. LED Current With Transient Current Limit

8.3.2.6 Illumination Monitoring

The device continuously monitors the illumination block for system failures to prevent damage to the system and the LEDs. The device protects from a broken control loop and a too high or too low output voltage V_{LED}. Register 0x0C (ILLUM_FAULT) controls the overall illumination fault bit. If the device report either ILLUM_BC1_PG_FAULT (powergood) or ILLUM_BC1_OV_FAULT (overvoltage), make sure the ILLUM_FAULT bit is not set too high:

8.3.2.6.1 Power Good

Both the Illumination driver and the Illumination LDO have a power good indication. The power good for the driver indicates if the output voltage (V_{LED}) is within a defined window indicating that the LED current has reached the set point. If for some reason the LED current cannot be controlled to the intended value, this fault occurs. Subsequently, the device sets bit ILLUM_BC1_PG_FAULT in register 0x27 to high. When the device energizes the power good of the LDO, it indicates that the LDO voltage is below a pre-defined minimum of 80% (for the rising edge) or 60% (for the falling edge). Register 0x27 stores the power good indication for the LDO (V5V5_LDO_ILLUM_PG_FAULT).

8.3.2.6.2 RatioMetric Overvoltage Protection

The DLPA4000 device protects the illumination driver LED outputs against open circuit use. When no LED is connected and the device receives a signal to set the LED current to a specific level, the LED voltage (ILLUM_A_FB) quickly rises and potentially saturates to VIN. The device triggers OVP protection circuit when V_{LED} crosses the specified threshold to prevent this dangerous situation. The OVP protection fault disables the DLPA4000 device.

The device triggers a fault when the supply voltage (VINA) falls too low. A comparator senses both the LED voltage and the V_{INA} supply voltage The fraction of the VINA is connected to the minus input of the comparator while the fraction of the V_{LED} voltage is connected to the plus input. The OVP fault occurs when the plus input rises above the minus input. Set the fraction of the VINA between 1 V and 4 V to ensure proper operation of the comparator.

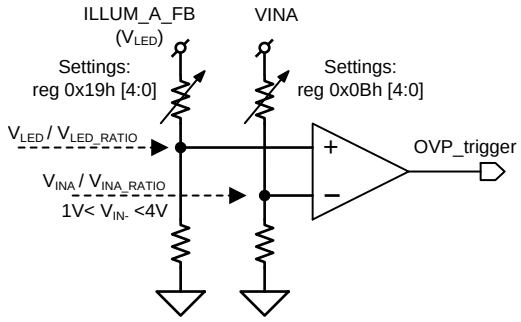


Figure 12. Ratio Metric OVP

Use register 0x19h bits [4:0] to set the fraction of the ILLUM_A_FB voltage. Use register 0x0Bh bits [4:0] to set the fraction of the VINA voltage. In general the device issues an OVP fault when either Equation 6 or Equation 6 occurs.

$$\frac{V_{LED}}{V_{LED\,RATIO}} \geq \frac{V_{INA}}{V_{INA\,RATIO}} \therefore V_{LED} \geq V_{INA} \times \frac{V_{LED\,RATIO}}{V_{INA\,RATIO}} \quad (6)$$

$$V_{LED} \geq V_{INA} \times \frac{V_{LED\,RATIO}}{V_{INA\,RATIO}} \geq V_{INA} \times \frac{4.98}{5.85} = 0.85 \times V_{INA} \quad (7)$$

Because the OVP level is ratio-metric it can be set to a fixed fraction of V_{INA}.

For example: to maintain a V_{LED} level below 85% of V_{INA}, use these settings:

reg 0x19h [4:0] = 01h (4.98)

reg 0x0Bh [4:0] = 07h (5.85)

Additionally for V_{IN_RATIO} = 5.85 the $V_{IN–}$ input voltage for the comparator is between 1 V and 3.4 V for a supply voltage between 6 V and 20 V.

8.3.3 External Power MOSFET Selection

The DLPA4000 requires five external N-type Power MOSFETs for proper operation. Two Power MOSFETs are required for the illumination buck converter section (FETs L_{EXT} and M_{EXT} 図 22) and three power MOSFETs are required for the LED selection switches (FETs P_{EXT}, Q_{EXT} and R_{EXT} in 図 22). This section discusses the selection criteria for these MOSFETs.

- Threshold voltage
- Gate charge
- Gate gate timing
- On-resistance, ($R_{DS(on)}$)

8.3.3.1 Threshold Voltage

The DLPA4000 has one drive output for each of the five power MOSFETs. Select MOSFETs that can be energized with a gate-source voltage of 5 V because signal swing at these outputs is approximately 5 V. For the three LED selection outputs (CHx_GATE_CTRL) and the low-side drive (ILLUM_LSIDE_DRIVE), the drive signal refers to ground. The signal swing of the ILLUM_HSIDE_DRIVE output refers to the switch node of the converter, ILLUM_A_SW. Use only N-channel MOSFETS.

8.3.3.2 Gate Charge and Gate Timing

Power MOSFETs typically specify the total gate charge required to energize and de-energize parameter. The total gate charge informs the gate-to-source rise times and fall times. Make sure the maximum gate-to-source rise times and fall times maximum are approximately between 20 ns and 30 ns. Because the typical high-side driver pull-up resistance is approximately 5 Ω, use a maximum gate capacitance between 4 nF and 6 nF . Design a maximum total gate charge between 20 nC and 30 nC.

Internal non-overlap timing prevents both the high-side and low-side MOSFET of the illumination buck converter from energizing simultaneously. Typical non-overlap timing of approximately 35 ns usually gives sufficient margins. The DLPA4000 device measures the gate-to-source voltage of the external MOSFETs to determine whether a MOSFET energized or not. This measurement is done at the pins of the DLPA4000. For the low-side MOSFET this measurement is done between ILLUM_LSIDE_DRIVE and ILLUM_A_GND. Similarly, for the high-side MOSFET the device measures the gate-to-source voltage between the ILLUM_HSIDE_DRIVE pin and the ILLUM_A_SW pin. Because of the location of these measurement nodes, do not insert any additional drivers or circuitry between the DLPA4000 and the external power MOSFETs of the buck converter. Delays can lead to incorrect on-off detection of the FETs and cause shoot-through currents if the user inserts additional circuitry. Shoot-through currents reduce efficiency, and more seriously damage the power MOSFETs.

LED selection switches require no specific criteria regarding the gate charge or gate timing. Timing of the LED selection signals is in the microsecond range rather than nanosecond range.

8.3.3.3 On-resistance $R_{DS(on)}$

Consider two issues relative to the drain-to-source on-resistance ($R_{DS(on)}$) to select a MOSFET. The first consideration is for the high-side MOSFET of the illumination buck-converter the $R_{DS(ON)}$ is a factor in the over-current detection. Secondly, for the other four MOSFETs the power dissipation drives the choice of the MOSFETs $R_{DS(on)}$.

The DLPA4000 measures the drain-to-source voltage drop of the high-side MOSFET when energized to detect an overcurrent situation. When the device detection circuit triggers, and de-energizes the high-side FET, the high-side drive over current threshold ($V_{DC\text{-}Th}$) is 185 mV . Use Equation 8 to calculate the actual current level, (I_{OC}) that trigger the overcurrent detection.

$$I_{OC} = \frac{V_{DC} - Th}{R_{DS(on)}} \times \frac{185\ mV}{R_{DS(on)}} \tag{8}$$

Use the on-resistance specification listed in the MOSFET datasheet for a high-temperature condition.For example, the CSD87350Q5D NexFET specifies the on-resistance of 5 mΩ at 125 °C. The overcurrent level for a design that uses this MOSFET is 37 A. This MOSFET is a good choice for a 32-A application.

Power dissipation due to conduction losses determines the on-resistance selection for the low-side MOSFET and the three LED selection MOSFETs. Use Equation 9 to calculate the power dissipated in these MOSFETs.

$$P_{DISS} = \int_{t} (I_{DS})^2 \times R_{DS(on)} \tag{9}$$

where

- I_{DS} is the FET current

The lower the on-resistance the lower the power dissipation. For example, the on-resistance specified for the CSD17556Q5B MOSFET is 1.2 mΩ. For a drain-to-source current of 32 A with a duty cycle of 25% (when the MOSFET is used as LED selection switch) the dissipation is approximately 0.3 W.

8.3.4 DMD Supplies

Figure 13 shows the supplies needed for the DMD and DLPC block.

- LDO_DMD: for internal supply
- DMD_HV: regulator generates high voltage supplies
- Two buck converters: for DLPC/DMD voltages

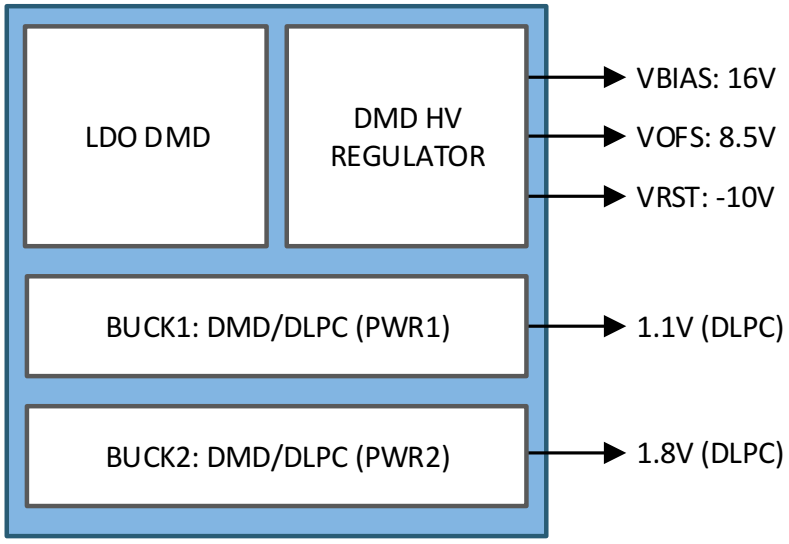


Figure 13. DMD Supplies Blocks

The DMD supplies block operates with the 0.65 DLP650NE DMD and the related DLPC4422. In addition to the three high voltage supplies to power the DLPA4000, the DMD and the related DLPC4422 each require a supply, Two buck converters provide the power.

The EEPROM of the DLPA4000 is factory programmed for a certain configuration, such as the type of buck converter used. Use register 0x26 to read the EEPROM configuration using these bits:

- DMD_BUCK1_USE
- DMD_BUCK2_USE

Table 8 describes the function of register 0x26.

8.3.4.1 LDO DMD

The LDO DMD is a regulator dedicated to the DMD supplies block. The LDO DMD provides an analog supply voltage of 5.5 V to the internal circuitry.

8.3.4.2 DMD HV Regulator

The DMD HV regulator generates three high voltage supplies: DMD_VRESET, DMD_VBIAS, and DMD_VOFFSET (see Figure 14). The DMD HV regulator uses a switching regulator (switch A through switch D), when the inductor shares time between all three supplies. The inductor charges to the current limit threshold and then discharged into one of the three supplies. The regulator distributes available charge time between those supplies that require a charge and when not all supplies require a charge.

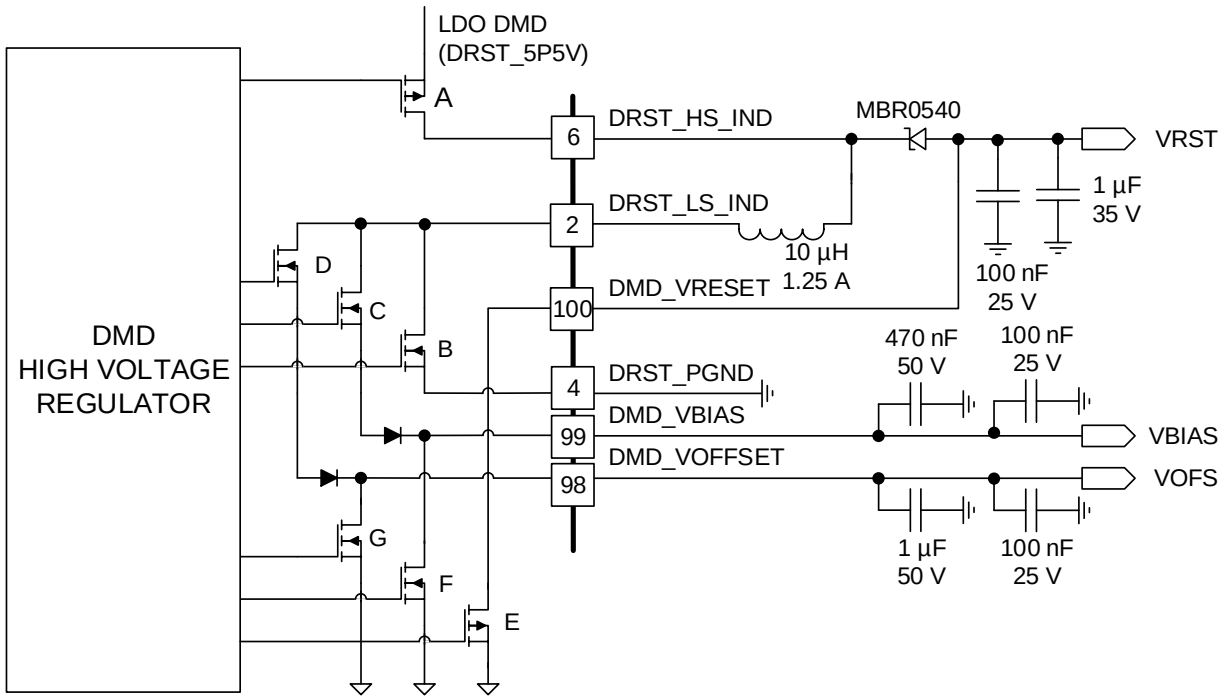


Figure 14. DMD High Voltage Regulator

8.3.4.3 DMD/DLPC Buck Converters

Each of the two DMD buck converters creates a supply voltage for the DLPC device. The values of the voltages for the DMD and DLPC used, for instance:

- DMD+DLPC4422: 1.1 V and 1.8 V

The topology of the buck converters is the same topology for the general purpose buck converters. See the *Buck Converters* section for inductor and capacitor configuration .

A typical configuration uses a value of 3.3 µH for the inductor and a value of 2 × 22 µF for the output capacitor.

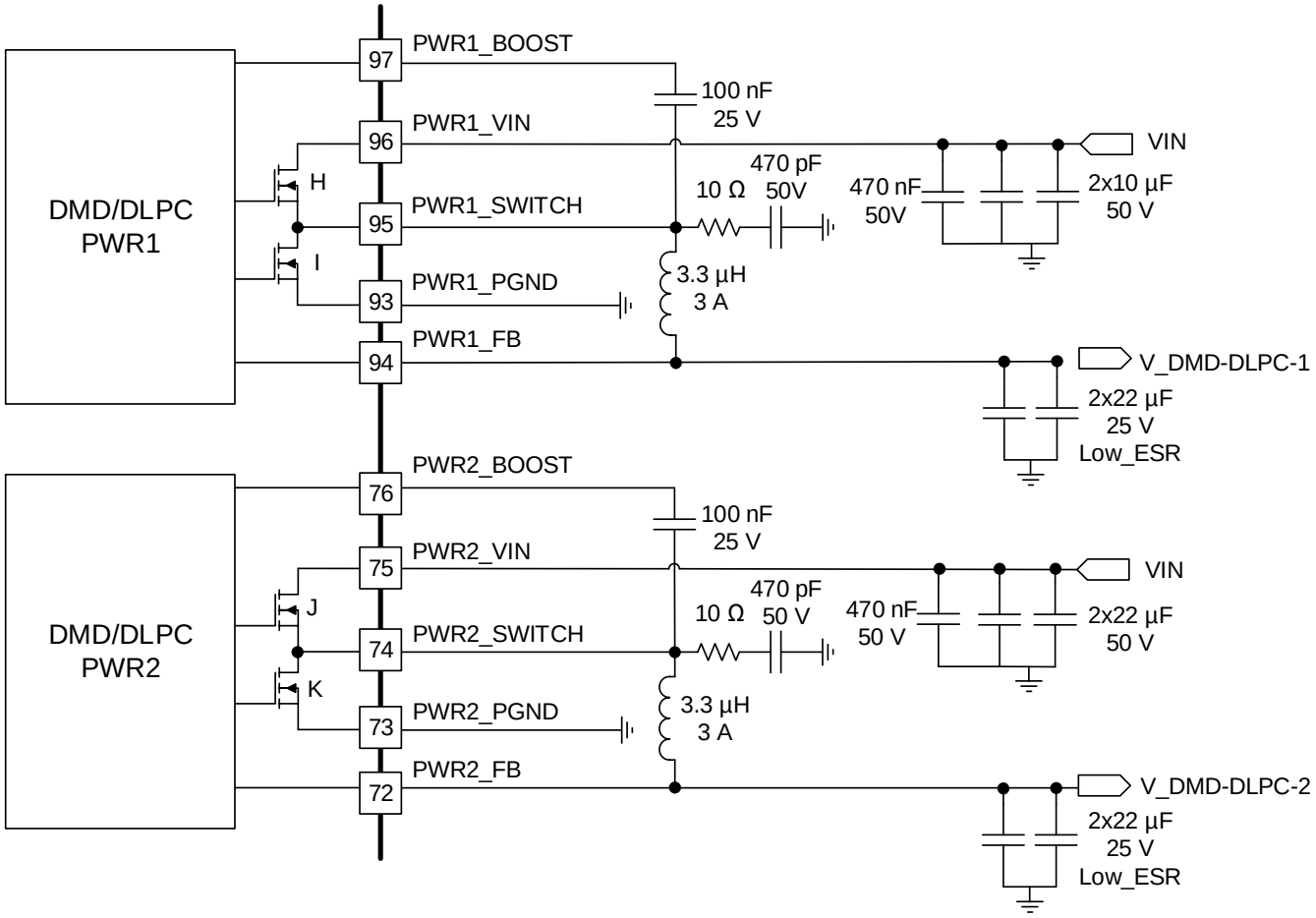


Figure 15. DMD and DLPC Buck Converters

8.3.4.4 DMD Monitoring

The device continuously monitors the DMD block for failures in order to prevent damage and to regulate the DMD voltages. Potential failures include but are not limited to a broken control loop or a too high or too low converter output voltage. Register 0x0C stores the overall DMD fault bit, DMD_FAULT. If any of the failures in Table 2 occur, the device sets the DMD_FAULT bit to high.

Table 2. DMD FAULT Indication

POWER GOOD (REGISTER 0x29)		
BLOCK	**REGISTER BIT**	**THRESHOLD**
HV Regulator	DMD_PG_FAULT	DMD_RESET: 90%, DMD_OFFSET and DMD_VBIAS: 86% rising, 66% falling
PWR1	BUCK_DMD1_PG_FAULT	Ratio: 72%
PWR2	BUCK_DMD2_PG_FAULT	Ratio: 72%
PWR3 (LDO_2)	LDO_GP2_PG_FAULT / LDO_DMD1_PG_ FAULT	80% rising, 60% falling
PWR4 (LDO_1)	LDO_GP1_PG_FAULT / LDO_DMD1_PG_ FAULT	80% rising, 60% falling
OVER-VOLTAGE (REGISTER 0x2A)		
BLOCK	**REGISTER BIT**	**THRESHOLD** (V)
PWR1	BUCK_DMD1_OV_FAULT	Ratio: 120%
PWR2	BUCK_DMD2_OV_FAULT	Ratio: 120%
PWR3 (LDO_2)	LDO_GP2_OV_FAULT / LDO_DMD1_OV_FAULT	7
PWR4 (LDO_1)	LDO_GP1_OV_FAULT / LDO_DMD1_OV_FAULT	7

8.3.4.4.1 Power Good

The DLPA4000 has power good indication for the DMD high-voltage (HV) regulator, DMD buck converters, DMD LDOs, and the LDO_DMD that supports the high-voltage regulator.

The DLPA4000 device continuously monitors the DMD HV regulator output rails DMD_RESET, DMD_VOFFSET and DMD_VBIAS. The DLP4000 device sets the DMD_ PG_FAULT bit in register 0x29 if either one of the output rails drops out of regulation. This situation can be due to a shorted output or an overload. The DMD_RESET threshold is 90%. The DMD_OFFSET and DMD_VBIAS thresholds are 86% (rising edge) and 66% (falling edge).

The power good signal for the two DMD buck converters indicate if each output voltage (PWR1_FB and PWR2_FB) maintains a specified range. The relative power good ratio is 72%, which indicates the level (output voltage falls below) at which the power good fault bit is asserted. The power good fault bits are in register 0x29, BUCK_DMD1_PG_FAULT and BUCK_DMD2_PG_FAULT.

The device monitors the output voltage of the DMD_LDO1 pin and the DMD_LDO2 pin. The power good fault of the LDO is asserted when the LDO voltage is below 80% (rising edge) or 60% (falling edge) of its intended value. The power good fault indication for the LDOs is in register 0x29, LDO_GP1_PG_FAULT, LDO_DMD1_PG_FAULT, LDO_GP2_PG_FAULT, LDO_DMD2_PG_FAULT.

The LDO_DMD pin regulates the DMD HV. The device asserts the power good fault of the LDO_DMD when the LDO voltage goes below 80% (rising edge) or 60% (falling edge) of its intended value. Register 0x29 stores the power good fault indication for this LDO as V5V5_LDO_DMD_PG_FAULT.

8.3.4.4.2 Overvoltage Fault

An overvoltage fault occurs when an output voltage rises above a specified threshold. The device indicates overvoltage faults for the DMD buck converters, DMD LDOs and the LDO_DMD that support the DMD HV regulator. The device does not include overvoltage fault of LDO1 and LDO2 in the overall DMD_FAULT when the LDOs are used as general purpose LDOs. Table 2 provides an overview of the DMD overvoltage faults and threshold levels.

8.3.5 Buck Converters

The DLPA4000 contains three general purpose buck converters and a supporting LDO (LDO_BUCKS). The three programmable 8-bit buck converters generate a voltage between 1 V and 5 V. The buck converters have an output current limit of 2 A. The device supports only General Purpose Buck2 (PWR6) types. Figure 16 shows one of the buck converters and the LDO_BUCKS.

The two DMD or DLPC buck converters discussed earlier in *DMD Supplies* have the same architecture as these three buck converters and can be configured in the same way.

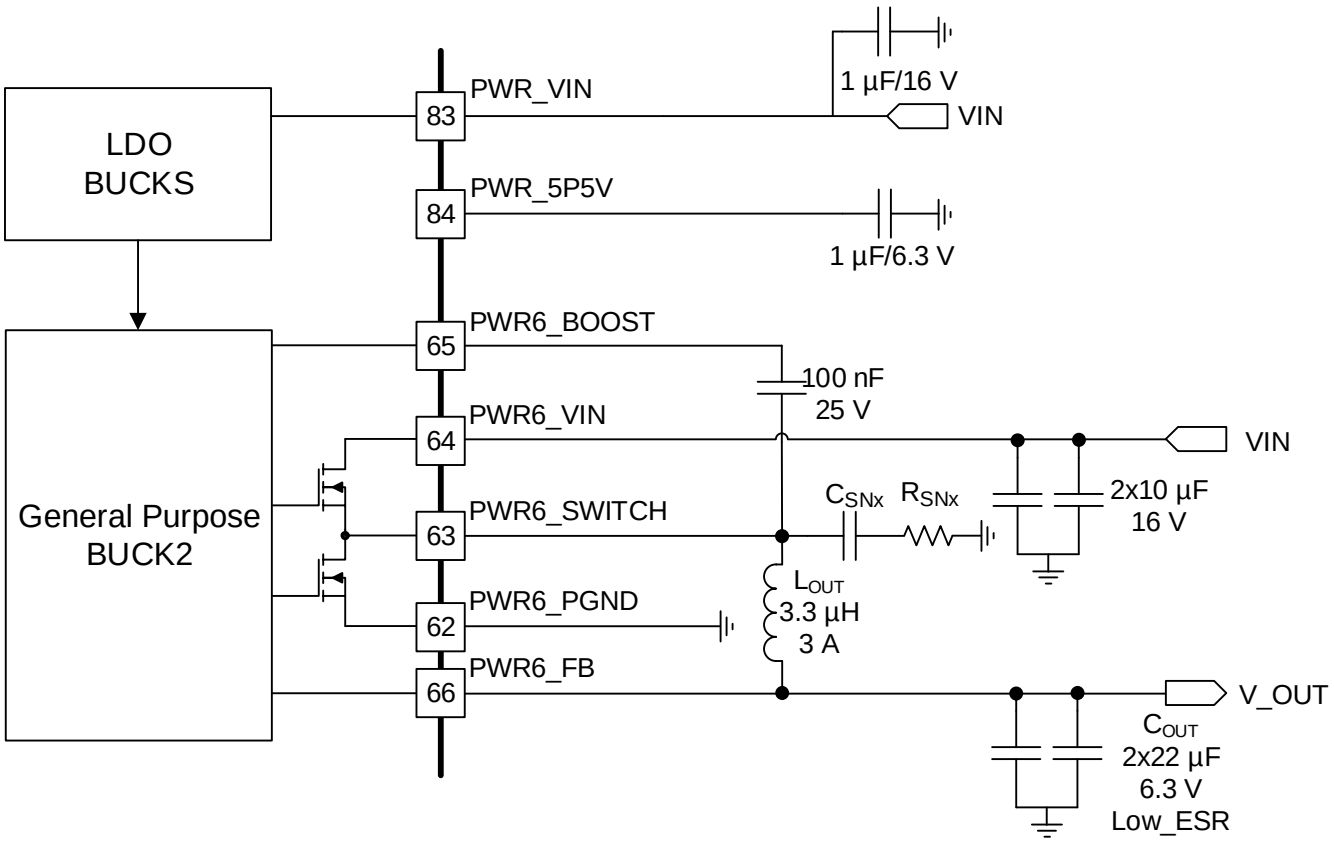


Figure 16. Buck Converter

8.3.5.1 LDO Bucks

This regulator supports the three general purpose buck converters and the 2 DMD or DLPC buck converters The regulator provides an analog voltage of 5.5 V to the internal circuitry.

8.3.5.2 General Purpose Buck Converters

Register 0x01 (BUCK_GP2_EN) controls the general purpose buck converters (GP2) (Figure 16).

Use register 0x14 to configure the converter outpout voltage between 1 V and 5 V with an 8-bit resolution.

The device supports only General Purpose Buck2 (PWR6) types. has a current capability of 2 A. The device does not support other buck converters such as PWR5 or PWR7.

The buck converter operates in one of two switching modes; Normal mode (600 kHz switching frequency), mode and skip mode. Applications operate with an increase in light-load efficiency in skip mode. As the output current decreases from a heavy-load condition, the inductor current decreases. The inductor current eventually decreases to a point where the ripple valley touches zero. Zero is the boundary between continuous conduction and discontinuous conduction modes. The device de-energizes the rectifying MOSFET when it detects zero inductor current. The converter transitions into discontinuous conduction mode as the load current further decreases. Because the device maintains the on-time, it takes longer to discharge the output capacitor with a smaller load current to the level of the reference voltage. Skip mode operation can toggle per buck converter in register 0x16.

8.3.5.3 Buck Converter Monitoring

The device continuously monitors the buck converter block to prevent damage to the DLPA4000 and peripherals. The device monitors several pin voltages. 表 3 summarizes the buck converter fault indications.

表 3. Buck Converter Fault Indication

POWER GOOD (REGISTER 0X27)		
BLOCK	**REGISTER BIT**	**THRESHOLD (RISING EDGE)**
Gen.Buck1	BUCK_GP1_PG_FAULT	Ratio 72%
Gen.Buck2	BUCK_GP2_PG_FAULT	Ratio 72%
Gen.Buck3	BUCK_GP3_PG_FAULT	Ratio 72%
OVERVOLTAGE (REGISTER 0X28)		
BLOCK	**REGISTER BIT**	**THRESHOLD (RISING EDGE)**
Gen.Buck1	BUCK_GP1_OV_FAULT	Ratio 120%
Gen.Buck2	BUCK_GP2_OV_FAULT	Ratio 120%
Gen.Buck3	BUCK_GP3_OV_FAULT	Ratio 120%

8.3.5.3.1 Power Good

The device has individual power good indication for each buck converter and the supporting LDO_BUCK pin.

The power good indication for the buck converter monitors the output voltage (PWR6_FB) is within a defined window. The relative power good ratio is 72%. This means that if the output voltage is below 72% of the set voltage the PG_fault bit is set high. The power good bits of the buck converter are in register 0x27 bit:

- BUCK_GP2_PG_FAULT for BUCK2 (PWR6)

The LDO_BUCKS that supports the buck converters has its own power good indication. The power good of the LDO_BUCKS is asserted if the LDO voltage is below 80% (rising edge) or 60% (falling edge) of its intended value. The power good indication for the LDO_BUCKS is in register 0x29, V5V5_LDO_BUCK_PG_FAULT.

8.3.5.3.2 Overvoltage Fault

An over-voltage fault occurs when an output voltage rises above the specified threshold. The device indicates overvoltage faults for the buck converters, and the LDO_BUCKS pin. The device asserts an overvoltage fault of the LDO_BUCKS pin when the LDO voltage goes abve 7.2 V. Use register 0x2A, V5V5_LDO_BUCK_OV_FAULT. The overvoltage of the general purpose buck converters is 120% of the set value. Register 0x28 stores the BUCK_GP1_OV_FAULT, BUCK_GP2_OV_FAULT, and BUCK_GP3_OV_FAULT faults.

8.3.6 Auxiliary LDOs

Use the two auxiliary LDOs (LDO_1 and LDO_2) for external applications. Use all other LDOs for internally only. Do not load these internal LDOs . LDO1 (PWR4) has a fixed voltage of 3.3 V. LDO2 (PWR3) has a fixed voltage of 2.5 V. Both LDOs deliver 200 mA of output current.

8.3.7 Measurement System

図 17 shows the circuitry that senses internal and external nodes. The implemented AFE comparator converts the nodes to digital signals. Use the 0x0A register to enable AFE_EN. The reference signal for this comparator, ACMPR_REF, is a low pass filtered PWM signal coming from the DLPC. A variable gain amplifier (VGA) is added with three gain settings (1x, 9.5x, and 18x) allows the device to receive a wide range of input signals . Use register 0x0A, to set the VGA gain (AFE_GAIN). The maximum input voltage of the VGA is 1.5 V. The device reduces some large internal voltage to accomodate the VGA function.

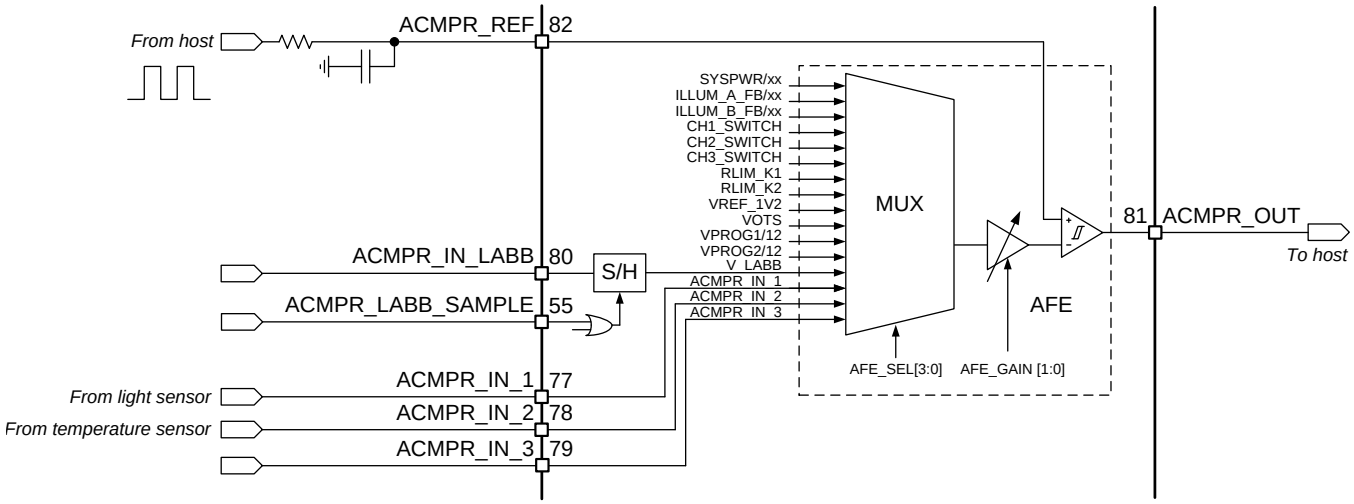


図 17. Measurement System Schematic

The device connects a multiplexer (MUX) to a wide range of nodes. Use egister 0X0A, to select the MUX input (AFE_SEL) . Choose settings from these options:

- System input voltage, SYSPWR
- LED anode cathode voltage, ILLUM_A_FB
- LED cathode voltage, CHx_SWITCH
- V_R_{LIM} to measure LED current
- Internal reference, VREF_1V2
- Die Temperature represented by voltage VOTS
- EEPROM programming voltage, VPROG1,2/12
- LABB sensor, V_LABB
- External sense pins, ACMPR_IN_1, ACMPR_IN_2, ACMPR_IN_3

The system input voltage VIN can be measured by selecting the SYSPWR/xx input of the MUX. the The device must divide the voltage before the device supplies system input voltage to the MUX. Applications require this process because the variable gain amplifier (VGA) handles voltages up-to 1.5 V but system voltages can be as high as 20 V. The device combines the division factor selection (VIN division factor) with the auto LED turn off functionality of the illumination driver . Use register 0x18 to ILLUM_LED_AUTO_OFF_SEL.

The device measures the LED voltages by monitoring the common anode of the LEDs and the cathode of each LED individually. The device senses the feedback pin of the illumination driver (ILLUM_A_FB) to measure the LED anode voltage (V_{LED}). The device must divide the LED anode voltage before the device supplies input voltage to the MUX. The device combines the division factor with the overvoltage fault level of the illumination driver. Use register 0x19 to set VLED_OVP_VLED_RATIO. The device feeds the cathode voltages for CH1_SWITCH, CH2_SWITCH,and CH3_SWITCH directly to the MUX without a division factor.

You can determine the LED current if you know the value of the sense resistor R_{LIM} and the voltage across the resistor. Measure the voltage at the high-side of the sense resistor can be measured by selecting MUX-input RLIM_K1. The bottom-side of the resistor connects to GND.

The VOTS pin connects to an on-chip temperature sensor. The VOTS voltage measures the device junction temperature:

$T_J = 300 \times V_{VOTS} – 270$ (10)

The DLPA4000 has two EEPROM blocks for storage of trim bits, 0x30 to 0x35). Use these bytes for USER EEPROM also. Use MUX input VPROG1/12 to measure the programming voltage of EEPROM block 1. Use VPROGR2/12 to measure the programming voltage of EEPROM block 2. The device divides the EEPROM programming voltage by 12 and then supplies the value to the MUX to prevent a too large voltage on the MUX input. The EEPROM programming voltage is approximately 12 V.

The local area brightness boost (LABB) function increases brightness while maintaining good contrast and saturation. Connect the sensor to pin ACMPR_IN_LABB. The device samples the light sensor signal. The device holds the sample value separate from the sensor timing. Make sure the application uses these setting for LABB oepration.

- The AFE block is enabled (0x0A, AFE_EN = 1)
- The LABB input is selected (0x0A, AFE_SEL<3:0>=3h)
- The AFE gain is set appropriately to have AFE_Gain x VLABB < 1.5 V (0x0A, AFE_GAIN<1:0>)

Use one of the following methods to sample the signal.

- Write to register 0x0B by specifying the sample time window (TSAMPLE_SEL) and set bit SAMPLE_LABB=1 to start sampling. The device automatically restes the SAMPLE_LABB bit in register 0x0B to 0 at the end of the sample period to prepare for a next sample request.
- Use the input ACMPR_LABB_SAMPLE-pin as a sample signal. The signal on ACMPR_IN_LABB is tracked while it is high. After the ACMP_LABB_SAMPLE goes lowm the value the device holds the value.

ACMPR_IN_1, ACMPR_IN_2,and ACMPR_IN_3 measure external signals from components such as a light sensor or a temperature sensor. Make sure that the voltage on the input doe not exceed 1.5 V.

8.4 Device Functional Modes

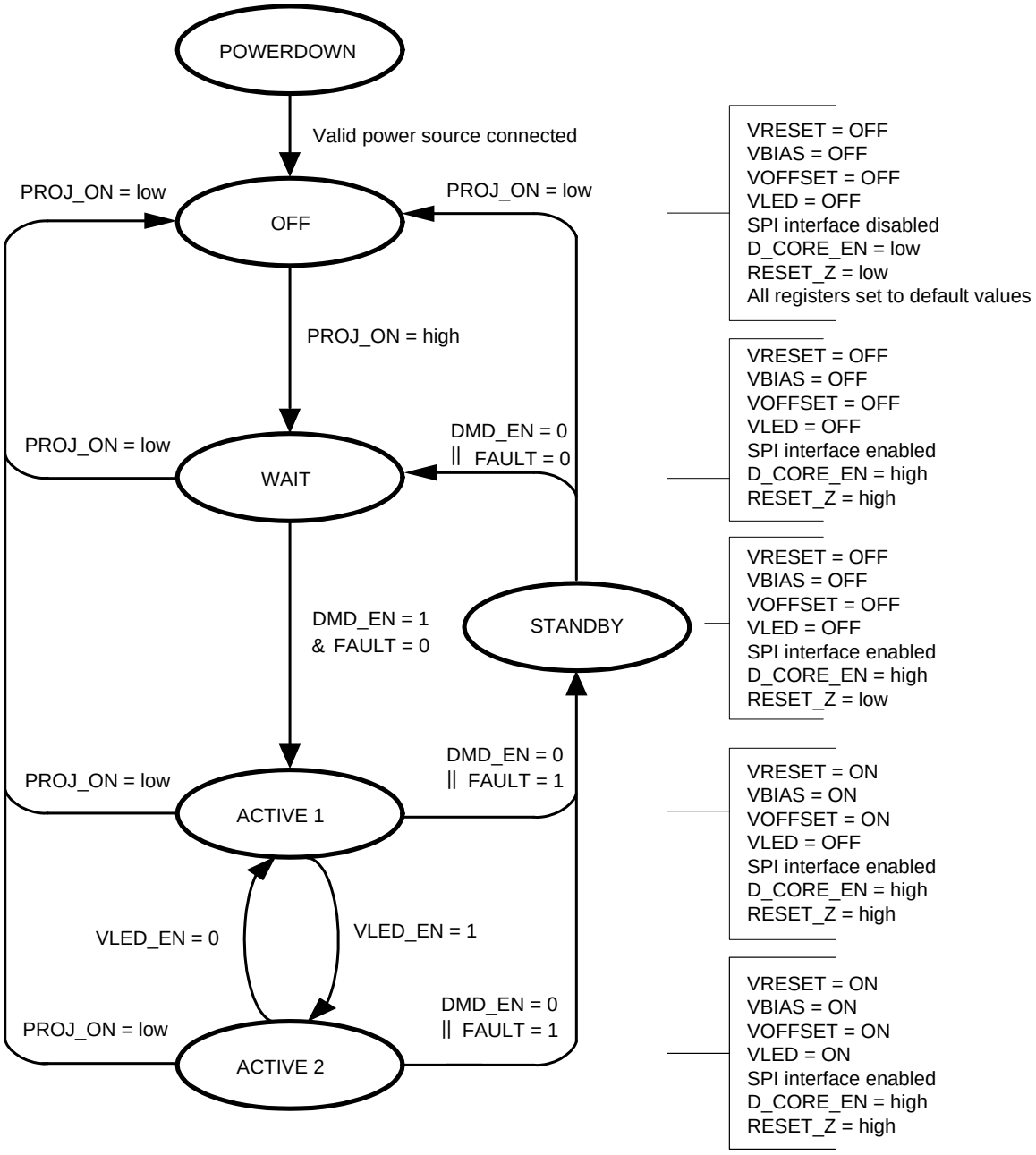
表 4. Modes of Operation

MODE	DESCRIPTION
OFF	This is the lowest-power mode of operation. All power functions are de-energized, registers are reset to their default values, and the IC does not respond to SPI commands. RESET_Z pin is pulled low. The IC enters OFF mode whenever the PROJ_ON pin is low.
WAIT	The DMD regulators and LED power (V_{LED}) are turned off, but the IC does respond to the SPI. The device enters WAIT mode whenever PROJ_ON is set high, DMD_EN(1) bit is set to 0 or a FAULT is resolved.
STANDBY	The device also enters STANDBY mode when a fault condition is detected(2). (See also section *Interrupt*). Once the fault condition is resolved, WAIT mode is entered.
ACTIVE1	The DMD supplies are enabled but LED power (V_{LED}) is disabled. PROJ_ON pin must be high, DMD_EN bit must be set to 1, and ILLUM_EN(3) bit is set to 0.
ACTIVE2	DMD supplies and LED power are enabled. PROJ_ON pin must be high and DMD_EN and ILLUM_EN bits must both be set to 1.

(1) Settings can be done through register 0x01
(2) Power-good faults, over-voltage, over-temperature shutdown, and undervoltage lockout
(3) Settings can be done through register 0x01, bit is named ILLUM_EN

表 5. Device State as a Function of Control-Pin Status

PROJ_ON Pin	STATE
LOW	OFF
HIGH	WAIT STANDBY ACTIVE1 ACTIVE2 (Device state depends on DMD_EN and ILLUM_EN bits and whether there are any fault conditions.)



A. || = OR, & = AND

B. FAULT = Undervoltage on any supply, thermal shutdown, or UVLO detection

C. UVLO detection, per the diagram, causes the DLPA4000 to go into the standby state. Standby state is not the lowest power state. If the application requires lower power, set PROJ_ON low.

D. DMD_EN register bit can be reset or set by SPI writes. DMD_EN defaults to 0 when PROJ_ON goes from low to high and then the DLPC4422 software automatically sets it to 1. Also, FAULT = 1 causes the DMD_EN register bit to be reset.

E. D_CORE_EN is a signal internal to the DLPA4000. This signal turns on the VCORE regulator.

図 18. State Diagram

8.5 Programming

This section discusses the serial protocol interface (SPI) of the DLPA4000 as well as the interrupt handling, device shutdown and register protection.

8.5.1 SPI

The DLPA4000 provides a 4-wire SPI port that supports two SPI clock frequency modes: 0 MHz to 36 MHz and 20 MHz to 40MHz. The clock frequency mode can be set in register 0x17, DIG_SPI_FAST_SEL. The interface supports both read and write operations. The SPI_SS_Z input serves as the active low chip select for the SPI port. The SPI_SS_Z input must be forced low for writing to or reading from registers. When SPI_SS_Z is forced high, the data at the SPI_MOSI input is ignored, and the SPI_MISO output is forced to a high-impedance state. The SPI_MOSI input serves as the serial data input for the port; the SPI_MISO output serves as the serial data output. The SPI_CLK input serves as the serial data clock for both the input and output data. Data at the SPI_MOSI input is latched on the rising edge of SPI_CLK, while data is clocked out of the SPI_MISO output on the falling edge of SPI_CLK. 図 19 illustrates the SPI port protocol. Byte 0 is referred to as the command byte, where the most significant bit is the write/not-read bit. For the W/nR bit, a 1 indicates a write operation, while a 0 indicates a read operation. The remaining seven bits of the command byte are the register address targeted by the write or read operation. The SPI port supports write and read operations for multiple sequential register addresses through the implementation of an auto-increment mode. As shown in 図 19, the auto-increment mode is invoked by simply holding the SPI_SS_Z input low for multiple data bytes. The register address is automatically incremented after each data byte transferred, starting with the address specified by the command byte. After reaching address 0x7Fh the address pointer jumps back to 0x00h.

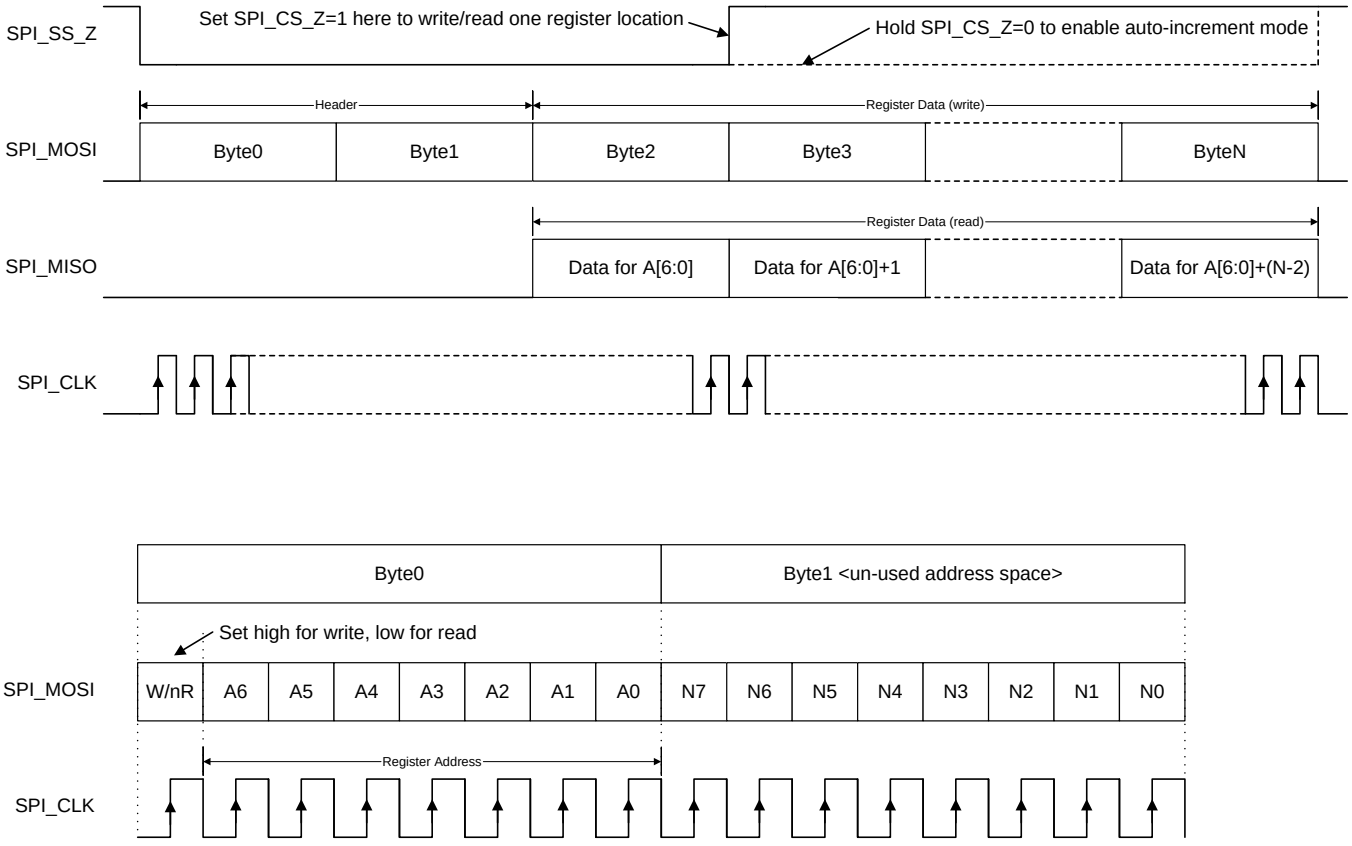


図 19. SPI Protocol

Programming (continued)

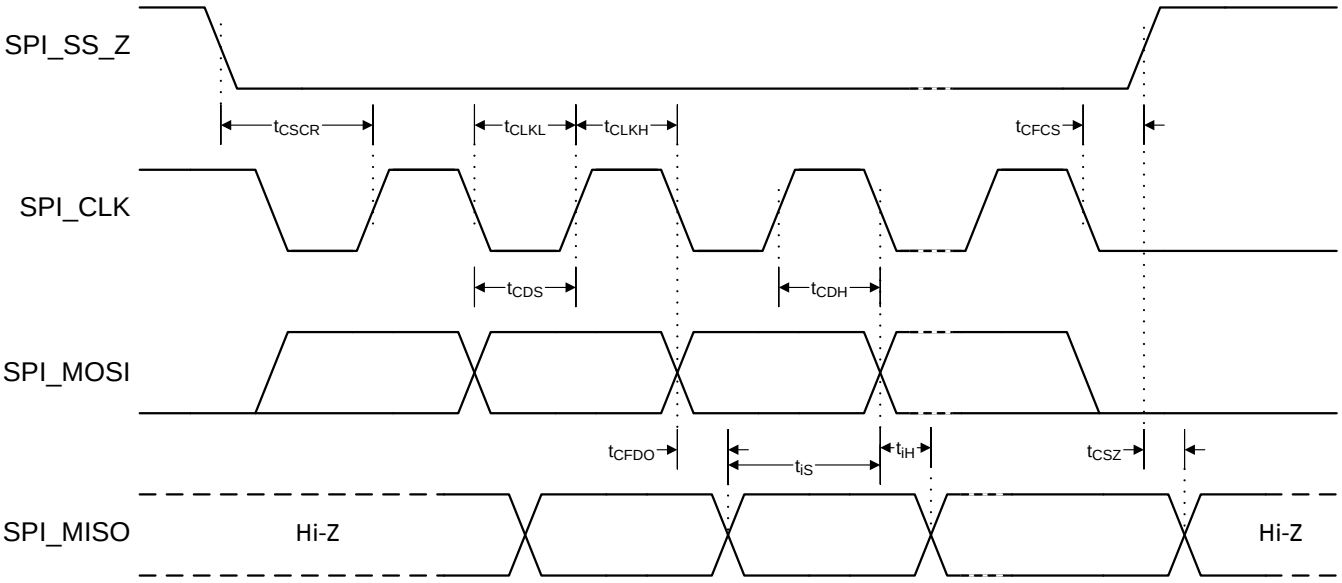


図 20. SPI Timing Diagram

8.5.2 Interrupt

The DLPA4000 has the capability to flag for several faults in the system, such as overheating, low battery, power good and over voltage faults. If a certain fault condition occurs one or more bits in the interrupt register (0x0C) gets set. The setting of a bit in register 0x0C triggers an interrupt event, which pulls down the INT_Z pin. Interrupts can be masked by setting the respective MASK bits in register 0x0D. Setting a MASK bit prevents the INT_Z from pulling low for the particular fault condition. Some high-level faults are composed of multiple low-level faults. The high-level faults can be read in register 0x0C, while the lower-level faults can be read in register 0x027 through 0x2A. An overview of the faults and how they are related is given in 表 6.

表 6. Interrupt Registers

HIGH-LEVEL	MID-LEVEL	LOW-LEVEL
SUPPLY_FAULT	DMD_FAULT	DMD_PG_FAULT
		BUCK_DMD1_PG_FAULT
		BUCK_DMD1_OV_FAULT
		BUCK_DMD2_PG_FAULT
		BUCK_DMD2_OV_FAULT
		LDO_GP1_PG_FAULT / LDO_DMD1_PG_FAULT
		LDO_GP1_OV_FAULT / LDO_DMD1_OV_FAULT
		LDO_GP2_PG_FAULT / LDO_DMD2_PG_FAULT
		LDO_GP2_OV_FAULT / LDO_DMD2_OV_FAULT
	BUCK_GP2_PG_FAULT	
	BUCK_GP2_OV_FAULT	
ILLUM_FAULT	ILLUM_BC1_PG_FAULT	
	ILLUM_BC1_OV_FAULT	
	ILLUM_BC2_PG_FAULT	
	ILLUM_BC2_OV_FAULT	
PROJ_ON_INT		
BAT_LOW_SHUT		
BAT_LOW_WARN		

Programming (continued)

表 6. Interrupt Registers (continued)

HIGH-LEVEL	MID-LEVEL	LOW-LEVEL
TS_SHUT		
TS_WARN		

8.5.3 Fast-Shutdown in Case of Fault

The DLPA4000 has 2 shutdown-down modes: a normal shutdown initiated after pulling PROJ_ON level low and a fast power-down mode. The fast shutdown feature can be enabled/disabled via register 0x01, FAST_SHUTDOWN_EN. By default the mode is enabled.

When the fast power-down feature is enabled, a fast shutdown is initiated for specific faults. This shutdown happens autonomously from the DLPC. The DLPA4000 enters the fast-shutdown mode only for specific faults, thus not for all the faults flagged by the DLPA4000. The faults for which the DLPA4000 goes into fast-shutdown are listed in 表 7.

表 7. Faults that Trigger a Fast-Shutdown

HIGH-LEVEL	LOW-LEVEL
BAT_LOW_SHUT	
TS_SHUT	
DMD_FAULT	DMD_PG_FAULT
	BUCK_DMD1_PG_FAULT
	BUCK_DMD1_OV_FAULT
	BUCK_DMD2_PG_FAULT
	BUCK_DMD2_OV_FAULT
	LDO_GP1_PG_FAULT / LDO_DMD1_PG_FAULT
	LDO_GP1_OV_FAULT / LDO_DMD1_OV_FAULT
	LDO_GP2_PG_FAULT / LDO_DMD2_PG_FAULT
	LDO_GP2_OV_FAULT / LDO_DMD2_OV_FAULT
ILLUM_FAULT	ILLUM_BC1_OV_FAULT
	ILLUM_BC2_OV_FAULT

8.5.4 Protected Registers

By default all regular USER registers are writable, except for the READ ONLY registers. Registers can be protected though to prevent accidental write operations. By enabling the protecting, only USER registers 0x02 through 0x09 are writable. Protection can be enabled/ disabled via register 0x2F, PROTECT_USER_REG.

8.5.5 Writing to EEPROM

The DLPA4000 has an EEPROM mainly intended for default settings and factory trimming parameters. Registers 0x30 through 0x35 can freely be used for customer convenience though, to write a serial number or version information for instance. Writing to EEPROM requires a couple of steps. First the EEPROM needs to be unlocked. Unlock the EEPROM by writing 0xBAh to register 0x2E followed by writing 0xBE to the same register. Both writes must be consecutive, that is, there must be no other read or write operation in between sending these two bytes. Once the password has been successfully written, register 0x30h through 0x35h are unlocked and can be write accessed using the regular SPI protocol. They remain unlocked until any byte other than 0xBABE is written to PASSWORD register 0x2E or the part is power cycled. To permanently store the written data in EEPROM write a 1 to register 0x2F, EEPROM_PROGRAM, > 250 ms later followed by writing a 0 to the same register.

To check if the registers are unlocked, read back the PASSWORD register 0x2E. If the data returned is 0x00h, the registers are locked. If the PASSWORD register returns 0x01h, the registers are unlocked.

8.6 Register Maps

Register Address, Default, R/W, Register name. **Boldface** settings are the hardwired defaults.

Table 8. Register Map

NAME	BITS	DESCRIPTION
0x00, E3, R/W, Chip Identification		
CHIPID	[7:4]	Chip identification number: E (hex)
REVID	[3:0]	Revision number, 3 (hex)
0x01, 82, R/W, Enable Register		
FAST_SHUTDOWN_EN	[7]	0: Fast shutdown disabled **1: Fast shutdown enabled**
CW_EN	[6]	**0: Color wheel circuitry disabled** 1: Color wheel circuitry enabled
Reserved	[5]	
BUCK_GP2_EN	[4]	**0: General purpose buck2 disabled** 1: General purpose buck2 enabled
Reserved	[3]	
ILLUM_LED_AUTO_OFF_EN	[2]	**0: Illum_led_auto_off_en disabled** 1: Illum_led_auto_off_en enabled
ILLUM_EN	[1]	0: Illum regulators disabled **1: Illum regulators enabled**
DMD_EN	[0]	**0: DMD regulators disabled** 1: DMD regulators enabled
0x02, 70, R/W, IREG Switch Control		
	[7]	Reserved, values don't care
ILLUM_ILIM	[6:3]	Rlim voltage top-side (mV). Illum current limit = Rlim voltage / Rlim 0000: 17 / 1000: 73 0001: 20 / 1001: 88 0010: 23 / 1010: 102 0011: 25 / 1011: 117 0100: 29 / 1100: 133 0101: 37 / 1101: 154 0110: 44 / **1110: 176** 0111: 59 / 1111: 197
ILLUM_SW_ILIM_EN	[2:0]	Bit2: CH3, MOSFET R transient current limit (**0:disabled**, 1:enabled) Bit1: CH2, MOSFET Q transient current limit (**0:disabled**, 1:enabled) Bit0: CH1, MOSFET P transient current limit (**0:disabled**, 1:enabled)
0x03, 00, R/W, SW1_IDAC(1)		
	[7:2]	Reserved, values don't care
SW1_IDAC<9:8>	[1:0]	Led current of CH1(A) = ((Bit value + 1)/1024) × (150 mV / Rlim), Most significant bits of 10 bits register (register 0x03 and 0x04). **00 0000 0000 [OFF]** 00 0011 0011 [(52/1024) × (150mV/Rlim)], Minimum code. …. 11 1111 1111 [150mV/Rlim]

Register Maps (continued)

Table 8. Register Map (continued)

NAME	BITS	DESCRIPTION
0x04, 00, R/W, SW1_IDAC(2)		
SW1_IDAC<7:0>	[7:0]	Led current of CH1(A) = ((Bit value + 1)/1024) × (150 mV / Rlim), Least significant bits of 10 bits register (register 0x03 and 0x04). **00 0000 0000 [OFF]** 00 0011 0011 [(52/1024) × (150mV/Rlim)], Minimum code. …. 11 1111 1111 [150mV/Rlim]
0x05, 00, R/W, SW2_IDAC(1)		
	[7:2]	Reserved, value don't care.
SW2_IDAC<9:8>	[1:0]	Led current of CH2(A) = ((Bit value + 1)/1024) × (150 mV / Rlim), Most significant bits of 10 bits register (register 0x05 and 0x06). **00 0000 0000 [OFF]** 00 0011 0011 [(52/1024) × (150mV/Rlim)], Minimum code. …. 11 1111 1111 [150mV/Rlim]
0x06, 00, R/W, SW2_IDAC(2)		
SW2_IDAC<7:0>	[7:0]	Led current of CH2(A) = ((Bit value + 1)/1024) × (150 mV / Rlim), Least significant bits of 10 bits register (register 0x05 and 0x06). **00 0000 0000 [OFF]** 00 0011 0011 [(52/1024) × (150mV/Rlim)], Minimum code. …. 11 1111 1111 [150mV/Rlim]
0x07, 00, R/W, SW3_IDAC(1)		
	[7:2]	Reserved, value don't care.
SW3_IDAC<9:8>	[1:0]	Led current of CH3(A) = ((Bit value + 1)/1024) × (150 mV / Rlim), Most significant bits of 10 bits register (register 0x07 and 0x08). **00 0000 0000 [OFF]** 00 0011 0011 [(52/1024) × (150mV/Rlim)], Minimum code. …. 11 1111 1111 [150mV/Rlim]
0x08, 00, R/W, SW3_IDAC(2)		
SW3_IDAC<7:0>	[7:0]	Led current of CH3(A) = ((Bit value + 1)/1024) × (150 mV / Rlim), Least significant bits of 10 bits register (register 0x07 and 0x08). **00 0000 0000 [OFF]** 00 0011 0011 [(52/1024) × (150mV/Rlim)], Minimum code. …. 11 1111 1111 [150mV/Rlim]
0x09, 00, R/W, Switch ON/OFF Control		
SW3	[7]	Only used if DIRECT MODE is enabled (see register 0x2F) **0: SW3 disabled** 1: SW3 enabled
SW2	[6]	Only used if DIRECT MODE is enabled (see register 0x2F) **0: SW2 disabled** 1: SW2 enabled
SW1	[5]	Only used if DIRECT MODE is enabled (see register 0x2F) **0: SW1 disabled** 1: SW1 enabled
	[4:0]	Reserved, value don't care.
0x0A, 00, R/W, Analog Front End (1)		
AFE_EN	[7]	**0: Analog front end disabled** 1: Analog front end enabled
AFE_CAL_DIS	[6]	**0: Calibrated 18x AFE_VGA** 1: Uncalibrated 18x AFE_VGA
AFE_GAIN	[5:4]	Gain analog front end gain **00: Off** 01: 1x 10: 9.5x 11: 18x

Register Maps (continued)

Table 8. Register Map (continued)

NAME	BITS	DESCRIPTION
AFE_SEL	[3:0]	Selected analog multiplexer input **0000: ILLUM_A_FB/xx, where xx is controlled by VLED_OVP_VLED_RATIO <4:0> (reg0x19)** 0001: ILLUM_B_FB/xx, where xx is controlled by VLED_OVP_VLED_RATIO <4:0> (reg0x19) 0010: VIN/xx, where xx is controlled by ILLUM_LED_AUTO_OFF_SEL <3:0> (reg0x18) 0011: V_LABB 0100: RLIM_K1 0101: RLIM_K2 0110: CH1_SWITCH 0111: CH2_SWITCH 1000: CH3_SWITCH 1001: VREF_1V2 1010: VOTS (Main temperature sense block output voltage) 1011: VPROG1/12 (EEPROM block1 programming voltage divided by 12) 1100: VPROG2/12 (EEPROM block2 programming voltage divided by 12) 1101: ACMPR_IN_1 1110: ACMPR_IN_2 1111: ACMPR_IN_3
0x0B, 00, R/W, Analog Front End (2)		
TSAMPLE_SEL	[7:6]	Samples time LABB Sensor (µs) **00: 7** 01: 14 10: 21 11: 28
SAMPLE_LABB	[5]	**0: LABB SAMPLING disabled** 1: START LABB SAMPLING (auto reset to 0 after TSAMPLE_SEL time).
VLED_OVP_VIN_RATIO	[4:0]	OVP_VIN Division factor.
		00000: 3.33 / 01000: 6.10 / 10000: 9.16 / 11000: 12.51
		00001: 4.98 / 01001: 6.23 / 10001: 9.60 / 11001: 12.94
		00010: 5.23 / 01010: 6.67 / 10010: 9.99 / 11010: 13.31
		00011: 5.32 / 01011: 7.11 / 10011: 10.41 / 11011: 13.70
		00100: 5.42 / 01100: 7.50 / 10100: 10.88 / 11100: 14.11
		00101: 5.52 / 01101: 7.96 / 10101: 11.26 / 11101: 14.56
		00110: 5.62 / 01110: 8.34 / 10110: 11.67 / 11110: 15.04
		00111: 5.85 / 01111: 8.77 / 10111: 12.11 / 11111: 15.41
0x0C, 00, R, Main Status Register		
SUPPLY_FAULT	[7]	**0: No PG or OV failures for any of the LV Supplies** 1: PG failures for a LV Supplies
ILLUM_FAULT	[6]	**0: ILLUM_FAULT = LOW** 1: ILLUM_FAULT = HIGH
PROJ_ON_INT	[5]	**0: PROJ_ON = HIGH** 1: PROJ_ON = LOW
DMD_FAULT	[4]	**0: DMD_FAULT = LOW** 1: DMD_FAULT = HIGH
BAT_LOW_SHUT	[3]	**0: VIN > UVLO_SEL<4:0>** 1: VIN < UVLO_SEL<4:0>
BAT_LOW_WARN	[2]	**0: VIN > LOWBATT_SEL<4:0>** 1: VIN < LOWBATT_SEL<4:0>
TS_SHUT	[1]	**0: Chip temperature < 132.5°C and no violation in V5V0** 1: Chip temperature > 156.5°C, or violation in V5V0
TS_WARN	[0]	**0: Chip temperature < 121.4°C** 1: Chip temperature > 123.4°C
0x0D, F5, Interrupt Mask Register		
SUPPLY_FAULT_MASK	[7]	0: Not masked for SUPPLY_FAULT interrupt **1: Masked for SUPPLY_FAULT interrupt**

Register Maps (continued)

Table 8. Register Map (continued)

NAME	BITS	DESCRIPTION
ILLUM_FAULT_MASK	[6]	0: Not masked for ILLUM_FAULT interrupt **1: Masked for ILLUM_FAULT interrupt**
PROJ_ON_INT_MASK	[5]	0: Not masked for PROJ_ON_INT interrupt **1: Masked for PROJ_ON_INT interrupt**
DMD_FAULT_MASK	[4]	0: Not masked for DMD_FAULT interrupt **1: Masked for DMD_FAULT interrupt**
BAT_LOW_SHUT_MASK	[3]	**0: Not masked for BAT_LOW_SHUT interrupt** 1: Masked for BAT_LOW_SHUT interrupt
BAT_LOW_WARN_MASK	[2]	0: Not masked for BAT_LOW_WARN interrupt **1: Masked for BAT_LOW_WARN interrupt**
TS_SHUT_MASK	[1]	**0: Not masked for TS_SHUT interrupt** 1: Masked for TS_SHUT interrupt
TS_WARN_MASK	[0]	0: Not masked for TS_WARN interrupt **1: Masked for TS_WARN interrupt**
0x0E, 00, R/W, Break-Before-Make Delay		
BBM_DELAY	[7:0]	Break before make delay register (ns), step size is 111 ns **0000 0000: 0** 0000 0001: 333 0000 0010: 444 0000 0011: 555 …. 1111 1101: 28305 1111 1110: 28416 **1111 1111: 28527**
0x0F, 07, R/W, Fast Shutdown Timing		
VOFS/RESETZ_DELAY	[7:4]	VOFS/RESETZ_DELAY (µs) / (blank) **0000: 4.000 – 4.445** / 1000: 6.230 – 7.120 0001: 8.010 – 8.900 / 1001: 12.46 – 14.24 0010: 16.02 – 17.80 / 1010: 24.89 – 28.44 0011: 32.00 – 35.55 / 1011: 49.77 – 56.88 0100: 63.99 – 71.10 / 1100: 99.5 – 113.8 0101: 128.0 – 142.2 / 1101: 199.1 – 227.6 0110: 256.0 – 284.5 / 1110: 398.3 – 455.2 0111: 512.1 – 569.0 / 1111: 1024.2 – 1138.0
VBIAS/VRST_DELAY	[3:0]	VBIAS/VRST_DELAY (µs) / (blank) 0000: 4.000 – 4.445 / 1000: 6.230 – 7.120 0001: 8.010 – 8.900 / 1001: 12.46 – 14.24 0010: 16.02 – 17.80 / 1010: 24.89 – 28.44 0011: 32.00 – 35.55 / 1011: 49.77 – 56.88 0100: 63.99 – 71.10 / 1100: 99.5 – 113.8 0101: 128.0 – 142.2 / 1101: 199.1 – 227.6 0110: 256.0 – 284.5 / 1110: 398.3 – 455.2 **0111: 512.1 – 569.0** / 1111: 1024.2 – 1138.0
0x10, C0, R/W, VOFS State Duration		

Register Maps (continued)

Table 8. Register Map (continued)

NAME	BITS	DESCRIPTION			
VOFS_STATE_DURATION	[7:5]	Duration of VOFS state (ms) 000: 1 001: 5 010: 10 011: 20 100: 40 101: 80 **110: 160** 111: 320			
LOWBATT_SEL	[4:0]	Low Battery level Selection			
		00000: 3.93	01000: 7.27	10000: 10.94	11000: 14.96
		00001: 5.92	01001: 7.43	10001: 11.46	11001: 15.47
		00010: 6.21	01010: 7.95	10010: 11.92	11010: 15.91
		00011: 6.32	01011: 8.46	10011: 12.42	11011: 16.37
		00100: 6.43	01100: 8.93	10100: 12.97	11100: 16.87
		00101: 6.55	01101: 9.47	10101: 13.42	11101: 17.40
		00110: 6.67	01110: 9.92	10110: 13.91	11110: 17.96
		00111: 6.93	01111: 10.42	10111: 14.43	11111: 18.41
0x11, 00, R/W, VBIAS State Duration					
VBIAS_STATE_DURATION	[7:5]	Duration of VBIAS state (ms) **000: bypass** 001: 5 010: 10 011: 20 100: 40 101: 80 110: 160 111: 320			
UVLO_SEL	[4:0]	Under Voltage Lockout level Selection			
		00000: 3.93	01000: 7.27	10000: 10.94	11000: 14.96
		00001: 5.92	01001: 7.43	10001: 11.46	11001: 15.47
		00010: 6.21	01010: 7.95	10010: 11.92	11010: 15.91
		00011: 6.32	01011: 8.46	10011: 12.42	11011: 16.37
		00100: 6.43	01100: 8.93	10100: 12.97	11100: 16.87
		00101: 6.55	01101: 9.47	10101: 13.42	11101: 17.40
		00110: 6.67	01110: 9.92	10110: 13.91	11110: 17.96
		00111: 6.93	01111: 10.42	10111: 14.43	11111: 18.41

Register Maps (continued)

Table 8. Register Map (continued)

NAME	BITS	DESCRIPTION
0x14, 00, R/W, GP2 Buck Converter voltage Selection		
BUCK_GP2_TRIM	[7:0]	General purpose2 buck output voltage = 1+ bit value * 15.69 (stepsize = 15.69 mV) **00000000 1 V** …. 11111111 5 V
0x16, 00, R/W, Buck Skip Mode		
	[7:5]	Reserved, value don't care.
BUCK_SKIP_ON	[4:0]	Skip Mode: Bit4: Buck_GP3 (**0:disabled**, 1:enabled) Bit3: Buck_GP1 (**0:disabled**, 1:enabled) Bit2: Buck_GP2 (**0:disabled**, 1:enabled) Bit1: Buck_DMD1 (**0:disabled**, 1:enabled) Bit0: Buck_DMD2 (**0:disabled**, 1:enabled)
0x17, 02, R/W, User Configuration Selection Register		
DIG_SPI_FAST_SEL	[7]	**0: SPI Clock from 0 to 36 MHz** 1: SPI Clock from 20 to 40 MHz
	[6]	Reserved, value don't care.
ILLUM_EXT_LSD_CUR_LIM_EN	[5]	**0: Current limiting disabled (External FETs mode)** 1: Current limiting enabled (External FETs mode)
Reserved	[4]	
ILLUM_3A_INT_SWITCH_SEL	[3]	Illum Configuration: most significant bit is ILLUM_EXT_SWITCH_CAP<6> (Reg0x26). Other 4 bits are <3:0> of this register. "x" is don't care. x xx00: Off x x110: 2 x 3 A Internal FETs **x 0010: 1 x 6 A Internal FETs** x 1010: 1 x 3 A Internal FETs 0 xx0x: Off 0 x11x: 2 x 3 A Internal FETs 0 001x: 1 x 6 A Internal FETs 0 101x: 1 x 3 A Internal FETs 0 xxx1: External FETs
ILLUM_DUAL_OUTPUT_CNTR_SEL	[2]	
ILLUM_INT_SWITCH_SEL	[1]	
ILLUM_EXT_SWITCH_SEL	[0]	
0x18, 00, R/W, OLV -ILLUM_LED_AUTO_OFF_SEL		
ILLUM_OLV_SEL	[7:4]	Illum openloop voltage (V) = 3 + bit value * 1 (stepsize = 1 V) **0000: 3 V** 0001: 4 V ... 1110: 17 V 1111: 18 V

Register Maps (continued)

Table 8. Register Map (continued)

NAME	BITS	DESCRIPTION			
ILLUM_LED_AUTO_OFF_SEL	[3:0]	Bit value	Led Auto Off Level (V)	VIN division factor	
		0000	**3.93**	**3.33**	
		0001	5.92	4.98	
		0010	6.21	5.23	
		0011	6.32	5.32	
		0100	6.43	5.42	
		0101	6.55	5.52	
		0110	6.67	5.62	
		0111	6.93	5.85	
		1000	7.27	6.10	
		1001	7.95	6.67	
		1010	8.93	7.50	
		1011	9.92	8.34	
		1100	10.94	9.16	
		1101	11.92	9.99	
		1110	12.97	10.88	
		1111	13.91	11.67	
0x19, 1F, R/W, Illumination Buck Converter Overvoltage Fault Level					
Reserved	[7:5]				
VLED_OVP_VLED_RATIO	[4:0]	Bit value / OVP VLED Division factor			
		00000: 3.33	01000: 6.10	10000: 9.16	11000: 12.51
		00001: 4.98	01001: 6.23	10001: 9.60	11001: 12.94
		00010: 5.23	01010: 6.67	10010: 9.99	11010: 13.31
		00011: 5.32	01011: 7.11	10011: 10.41	11011: 13.70
		00100: 5.42	01100: 7.50	10100: 10.88	11100: 14.11
		00101: 5.52	01101: 7.96	10101: 11.26	11101: 14.56
		00110: 5.62	01110: 8.34	10110: 11.67	11110: 15.04
		00111: 5.85	01111: 8.77	10111: 12.11	**11111: 15.41**
0x1B, 00, R/W, Color Wheel PWM Voltage(1)					
CW_PWM <7:0>	[7:0]	Least significant 8 bits of 16 bits register (register 0x1B and 0x1C) Average color wheel PWM voltage (V), step size = 76.294 µV **0x0000 0 V** .... 0xFFFF 5 V			

Register Maps (continued)

Table 8. Register Map (continued)

NAME	BITS	DESCRIPTION
0x1C, 00, R/W, Color Wheel PWM Voltage(2)		
CW_PWM <15:8>	[7:0]	Most significant 8 bits of 16 bits register (register 0x1B and 0x1C) Average color wheel PWM voltage (V), step size = 76.294 µV **0x0000 0 V** .... 0xFFFF 5 V
0x25, 00, R/W, ILLUM BUCK CONVERTER BANDWIDTH SELECTION		
reserved	[7:4]	
ILLUM_BW_BC1	[3,2]	ILED CONTROL LOOP BANDWIDTH INCREASE (dB)
		00: 0
		01: 1.9
		10: 4.7
		11: 9.3
ILLUM_BW_BC2	[1,0]	ILED CONTROL LOOP BANDWIDTH INCREASE (dB)
		00: 0
		01: 1.9
		10: 4.7
		11: 9.3
0x26, DF, R, Capability register		
LED_AUTO_TURN_OFF_CAP	[7]	0: LED_AUTO_TURN_OFF_CAP disabled **1: LED_AUTO_TURN_OFF_CAP enabled**
ILLUM_EXT_SWITCH_CAP	[6]	0: No external switch control capability **1: External switch control capability included**
CW_CAP	[5]	**0: No color wheel capability** 1: Color wheel capability included
Reserved	[4]	
DMD_LDO1_USE	[3]	0: LDO1 not used for DMD, voltage set by user register **1: LDO1 used for DMD, voltage set by EEPROM**
DMD_LDO2 _USE	[2]	0: LDO2 not used for DMD, voltage set by user register **1: LDO2 used for DMD, voltage set by EEPROM**
DMD_BUCK1 _USE	[1]	0: DMD Buck1 disabled **1: DMD Buck1 used**
DMD_BUCK2 _USE	[0]	0: DMD Buck2 disabled **1: DMD Buck2 used**
0x27, 00, R, Detailed status register1 (Power good failures for general purpose and illumination blocks)		
BUCK_GP3_PG_FAULT	[7]	**0: No fault** 1: Focus motor buck power good failure. Does not initiate a fast shutdown.
BUCK_GP1_PG_FAULT	[6]	**0: No fault** 1: General purpose buck1 power good failure. Does not initiate a fast shutdown.
BUCK_GP2_PG_FAULT	[5]	**0: No fault** 1: General purpose buck2 power good failure. Does not initiate a fast shutdown.
Reserved	[4]	
ILLUM_BC1_PG_FAULT	[3]	**0: No fault** 1: Illum buck converter1 power good failure. Does not initiate a fast shutdown.
ILLUM_BC2_PG_FAULT	[2]	**0: No fault** 1: Illum buck converter2 power good failure. Does not initiate a fast shutdown.
	[1]	**Reserved, value always 0**
	[0]	**Reserved, value always 0**
0x28, 00, R, Detailed status register2 (Overvoltage failures for general purpose and illum blocks)		
BUCK_GP3_OV_FAULT	[7]	**0: No fault** 1: Focus motor buck overvoltage failure. Does not initiate a fast shutdown.

Register Maps (continued)

Table 8. Register Map (continued)

NAME	BITS	DESCRIPTION
BUCK_GP1_OV_FAULT	[6]	**0: No fault** 1: General purpose buck1 overvoltage failure. Does not initiate a fast shutdown.
BUCK_GP2_OV_FAULT	[5]	**0: No fault** 1: General purpose buck2 overvoltage failure. Does not initiate a fast shutdown.
	[4]	**Reserved, value always 0**
ILLUM_BC1_OV_FAULT	[3]	**0: No fault** 1: Illum buck converter1 overvoltage failure. Does not initiate a fast shutdown.
ILLUM_BC2_OV_FAULT	[2]	**0: No fault** 1: Illum buck converter2 overvoltage failure. Does not initiate a fast shutdown.
	[1]	**Reserved, value always 0**
	[0]	**Reserved, value always 0**
0x29, 00, R, Detailed status register3 (Power good failure for DMD related blocks)		
	[7]	**Reserved, value always 0**
DMD_PG_FAULT	[6]	**0: No fault** 1: VBIAS, VOFS and/or VRST power good failure. Initiates a fast shutdown.
BUCK_DMD1_PG_FAULT	[5]	**0: No fault** 1: Buck1 (used to create DMD voltages) power good failure. Initiates a fast shutdown.
BUCK_DMD2_PG_FAULT	[4]	**0: No fault** 1: Buck2 (used to create DMD voltages) power good failure. Initiates a fast shutdown.
	[3]	**Reserved, value always 0**
	[2]	**Reserved, value always 0**
LDO_GP1_PG_FAULT / LDO_DMD1_PG_FAULT	[1]	**0: No fault** 1: LDO1 (used as general purpose or DMD specific LDO) power good failure. Initiates a fast shutdown.
LDO_GP2_PG_FAULT / LDO_DMD2_PG_FAULT	[0]	**0: No fault** 1: LDO2 (used as general purpose or DMD specific LDO) power good failure. Initiates a fast shutdown.

Register Maps (continued)

Table 8. Register Map (continued)

NAME	BITS	DESCRIPTION			
0x2A, 00, R, Detailed status register4 (Overvoltage failures for DMD related blocks and Color Wheel)					
	[7]	**Reserved, value always 0**			
	[6]	**Reserved, value always 0**			
BUCK_DMD1_OV_FAULT	[5]	**0: No fault** 1: Buck1 (used to create DMD voltage) overvoltage failure			
BUCK_DMD2_OV_FAULT	[4]	**0: No fault** 1: Buck2 (used to create DMD voltage) overvoltage failure			
	[3]	**Reserved, value always 0**			
	[2]	**Reserved, value always 0**			
LDO_GP1_OV_FAULT / LDO_DMD1_OV_FAULT	[1]	**0: No fault** 1: LDO1 (used as general purpose or DMD specific LDO) overvoltage failure			
LDO_GP2_OV_FAULT / LDO_DMD2_OV_FAULT	[0]	**0: No fault** 1: LDO2 (used as general purpose or DMD specific LDO) overvoltage failure			
0x2B, 01, R, Chip ID extension					
CHIP_ID_EXTENTION	[7:0]	ID extension to distinguish between various configuration options.			
0x2C, 00, R/W, ILLUM_LED_AUTO_TURN_OFF_DELAY SETTINGS					
Reserved	[7:4]	TBD			
ILLUM_LED_AUTO_TURN_OFF_DELAY	[3:0]	ILLUM_LED_AUTO_TURN_OFF_DELAY (µsec)			
		0000: 4.000-4.445	0100: 63.99-71.10	1000: 6.230-7.120	1100: 99.5-113.8
		0001: 8.010-8.900	0101: 128.0-142.2	1001: 12.46-14.24	1101: 199.1-227.6
		0010: 16.02-17.80	0110: 256.0-284.5	1010: 24.89-28.44	1110: 398.3-455.2
		0011: 32.00-35.55	0111: 512.1-569.0	1011: 49.77-56.88	1111: 1024.2-1138.0
0x2E, 00, R/W, User Password					
USER PASSWORD (0xBABE)	[7:0]	Write Consecutively 0xBA and 0xBE to unlock.			
0x2F, 00, R/W, User Protection Register					
	[7:3]	Reserved, value don't care.			
EEPROM_PROGRAM	[2]	**0: EEPROM programming disabled** 1: Shadow register values programmed to EEPROM			
DIRECT_MODE	[1]	**0: Direct mode disabled** 1: Direct mode enabled (register 0x09 to control switched)			
PROTECT_USER_REG	[0]	**0: ALL regular USER registers are WRITABLE, except for READ ONLY registers** 1: ONLY USER registers 0x02, 0x03, 0x04, 0x05, 0x06, 0x07, 0x08, and 0x09 are WRITABLE			
0x30, 00, R/W, User EEPROM Register					
USER_REGISTER1	[7:0]	User EEPROM Register1			
0x31, 00, R/W, User EEPROM Register					
USER_REGISTER2	[7:0]	User EEPROM Register2			
0x32, 00, R/W, User EEPROM Register					
USER_REGISTER3	[7:0]	User EEPROM Register3			
0x33, 00, R/W, User EEPROM Register					
USER_REGISTER4	[7:0]	User EEPROM Register4			
0x34, 00, R/W, User EEPROM Register					
USER_REGISTER5	[7:0]	User EEPROM Register5			
0x35, 00, R/W, User EEPROM Register					
USER_REGISTER6	[7:0]	User EEPROM Register6			

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

In display applications, using the DLPA4000 provides all needed analog functions including all analog power supplies and the RGB LED driver (up to 32A per LED) with high-side Pump functionality to provide a robust and efficient display solution. Each DLP application is derived primarily from the optical architecture of the system and the format of the data coming into the DLPC4422 controller.

9.2 Typical Application

A common application combines the DLPA4000 with the 0.65 WXGA DMD (DLP650LE) or a 0.65 1080P DMD (DLP650NE) and a DLPC4422 controller to create a high resolution, LED projector. The DLPC4422 in the projector typically receives images from a PC or video player using HDMI or VGA analog as shown in 図 21. Card readers and Wi-Fi can receive images when the application includes the appropriate peripheral components. The DLPA4000 sequences the power-supply and controls the RGB LED currents in this application.

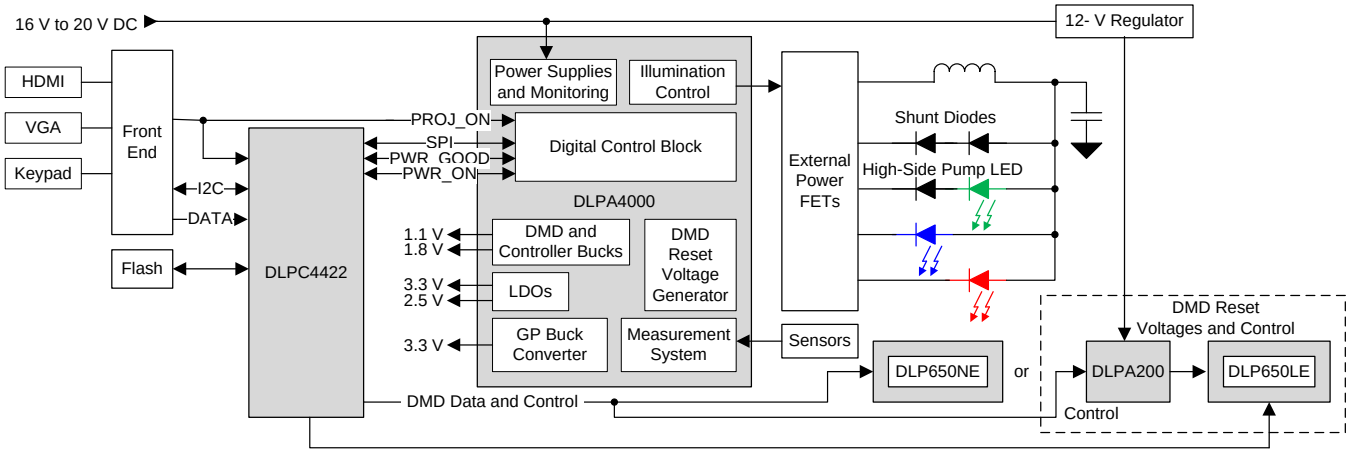


図 21. Typical Setup Using DLPA4000

9.2.1 Design Requirements

A high resolution LED projector can be created by using a DLP chip set comprised of a 0.65 WXGA DMD (DLP650LE) or a 0.65 1080p DMD (DLP650NE), a DLPC4422 controller, and the DLPA4000 PMIC/LED Driver. The DLPC4422 does the digital image processing, the DLPA4000 provides the needed analog functions for the projector, and the DMD is the display device for producing the projected image. In addition to the three DLP chips in the chip set, other components is required. At a minimum a Flash part is needed to store the software and firmware to control the DLPC4422. The illumination light that is applied to the DMD is typically from red, green, and blue LEDs. These are often contained in three separate packages, but sometimes more than one color of LED die may be in the same package to reduce the overall size of the projector. Power MOSFETs are needed external to the DLPA4000 so that high LED currents can be supported. For connecting the DLPC4422 to the front end chip for receiving images, the parallel interface is typically used. Connect the front end chip to the parallel interface, I^2C to input commands to the DLPC4422.

Typical Application (continued)

The DLPA4000 has three built-in buck switching regulators to serve as projector system power supplies. Two of the regulators are fixed to 1.1 V and 1.8 V for powering the DLP chip set. The remaining buck regulator is available for general purpose use and its voltages are programmable. The regulators can be used to a drive variable-speed fans or to power other projector chips such as the front-end chip. The only power supply needed at the DLPA4000 input is SYSPWR from an external DC power supply or internal battery. The entire projector can be turned on and off by using a single signal called PROJ_ON. When PROJ_ON is high, the projector turns on and begins displaying images. When PROJ_ON is set low, the projector turns off and draws just microamps of current on SYSPWR.

9.2.2 Detailed Design Procedure

To connect the 0.65 WXGA DMD (DLP650LE) or 0.65 1080p DMD (DLP650NE), DLPC4422 controller and DLPA4000, see the reference design schematic. When a circuit board layout is created from this schematic a very small circuit board is possible. An example small board layout is included in the reference design data base. Comply with the layout guidelines to achieve reliable projector operation. The optical engine that has the LED packages and the DMD mounted to it is typically supplied by an optical OEM who specializes in designing optics for DLP projectors.

The component selection of the buck converter is mainly determined by the output voltage. 表 9 shows the recommended value for inductor L_{OUT} and capacitor C_{OUT} for a given output voltage.

表 9. Recommended Buck Converter L_{OUT} and C_{OUT}

V_{OUT} (V)	L_{OUT} (µH)			C_{OUT} (µF)	
	MIN	TYP	MAX	MIN	MAX
1 - 1.5	1.5	2.2	4.7	22	68
1.5 - 3.3	2.2	3.3	4.7	22	68
3.3 - 5	3.3		4.7	22	68

Use 式 11 to calculate the inductor peak-to-peak ripple current. Use 式 12 the peak current. Use 式 13to calculate teh RMS current. The inductor saturation current rating must be greater than the calculated peak current. The RMS or heating current rating of the inductor must be greater than the calculated RMS current.

$$I_{L_{OUT\ RIPPLE\ P-P}} = \frac{\frac{V_{OUT}}{V_{IN(max)}} \times \left(V_{IN(max)} - V_{OUT}\right)}{L_{OUT} \times f_{SW}} \tag{11}$$

where

- the switching frequency of the buck converter is approximately 600 kHz

$$I_{L_{OUT\ PEAK}} = I_{L_{OUT}} + \frac{I_{L_{OUT\ RIPPLE\ P}-P}}{2} \tag{12}$$

$$I_{L_{OUT\ RMS}} = \sqrt{\left(I_{L_{OUT}}\right)^2 + \frac{1}{12} \times \left(I_{L_{OUT\ RIPPLE\ P}-P}\right)^2} \tag{13}$$

The capacitor value and ESR determines the level of output voltage ripple. Use ceramic or other low ESR capacitors. Recommended values range from 22 to 68 µF. Use 式 14 to determine the required RMS current rating for the output capacitor.

$$I_{C_{OUT\ (rms)}} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_{OUT} \times f_{SW}} \tag{14}$$

One other component for the buck converter configuration is needed. Use a charge pump capacitor between PWRx_SWITCH and PWRx_BOOST to drive the high-side MOSFET. The recommended value for the charge pump capacitor is 100 nF.

Because the switching edges of the buck converter are relatively fast, voltage overshoot and ringing can become a problem. To overcome this problem a snubber network is used. The snubber circuit consists of a resistor and capacitor that are connected in series from the switch node to ground. The snubber circuit is used to damp the parasitic inductances and capacitances during the switching transitions. This circuit reduces the ringing voltage and also reduces the number of ringing cycles. The snubber network is formed by RSNx and CSNx. More information on controlling switch-node ringing in synchronous buck converters and configuring the snubber can be found in *Analog Applications Journal*.

9.2.2.1 Component Selection for General-Purpose Buck Converters

The theory of operation of a buck converter is explained in application note, *Understanding Buck Power Stages in Switchmode Power Supplies*, SLVA057. This section is limited to the component selection. For proper operation, selection of the external components is very important, especially the inductor L_{OUT} and the output capacitor C_{OUT}. Choose inductor and capacitors with low equivalent series resistance (ESR) specifications to ensure the best efficiency and ripple performance.

9.3 System Example With DLPA4000 Internal Block Diagram

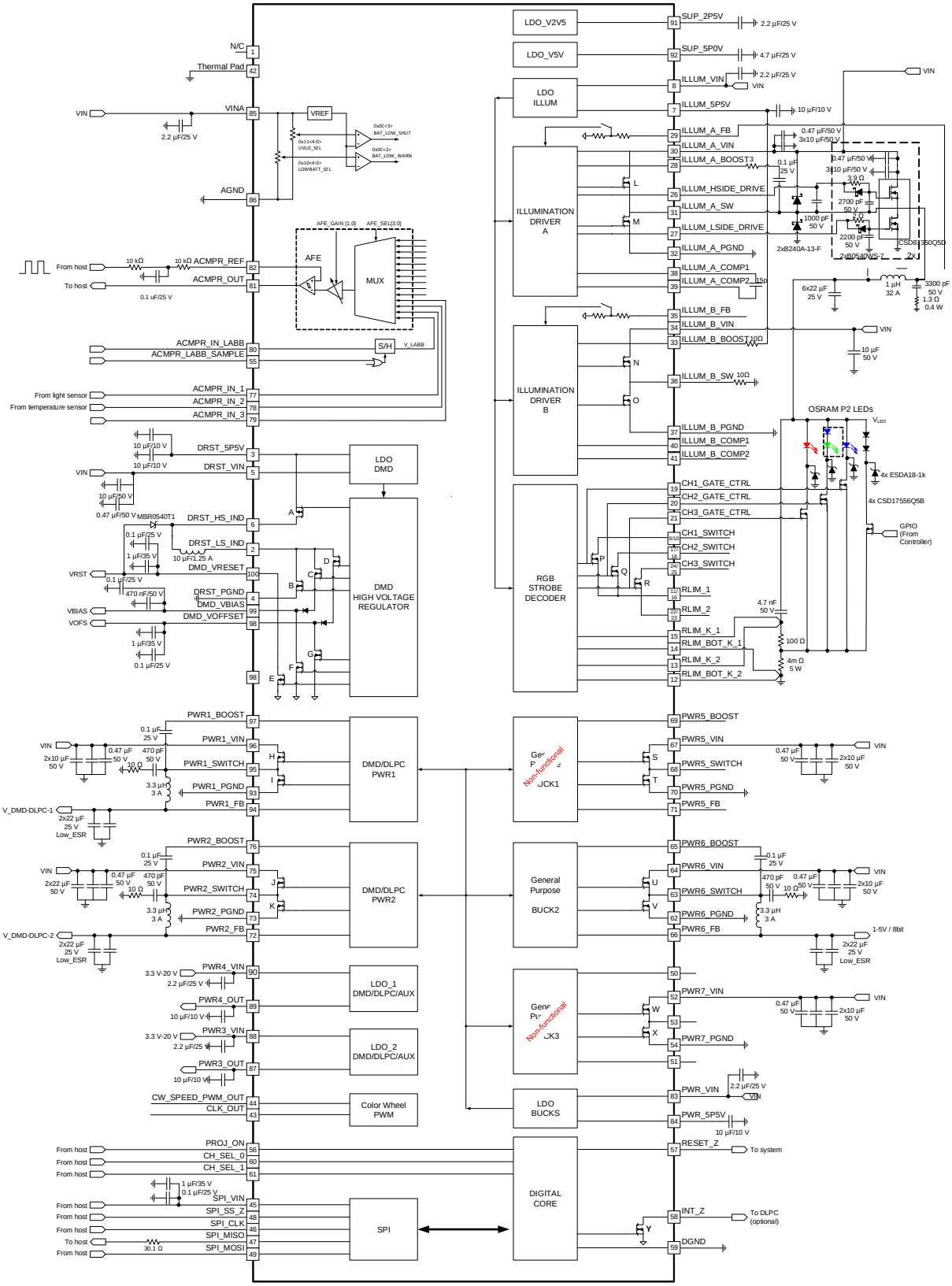


図 22. Typical Application: V_{IN} = 19.5 V, I_{OUT} = 32 A, LED, External MOSFETs

10 Power Supply Recommendations

The DLPA4000 operates over a range of 16 V to 20 V input voltage supply or battery. The power supply design may require additional bulk capacitance. Additional bulk capacitance helps avoid insufficient supply current due to line drop, ringing due to trace inductance at the VIN terminals, or supply peak current limitations, When the interaction of the ceramic input capacitors causes ringing, an electrolytic or tantalum type capacitor may be needed for damping.

Evaluate the bulk capacitance required so that the input voltage remains within the specified range long enough for a proper fast shutdown to occur for the VOFFSET, VRESET, and VBIAS supplies. The shutdown period begins when the input voltage goes below the programmable UVLO threshold. Shutdown occurs when the external power suddenly discontinues.

10.1 Power-Up and Power-Down Timing

The power-up and power-down sequence ensures a correct operation of the DLPA4000 and to prevent damage to the DMD. The DLPA4000 controls the correct sequencing of the DMD_VRESET, DMD_VBIAS, and DMD_VOFFSET to ensure a reliable operation of the DMD.

The general startup sequence of the supplies is described earlier in *Supply and Monitoring*. The power-up sequence of the high voltage DMD lines is especially important in order not to damage the DMD. A too large delta voltage between DMD_VBIAS and DMD_VOFFSET could cause the damage and should therefore be prevented.

After the device pulls PROJ_ON high, the DMD buck converters and LDOs energize (PWR1, PWR2, PWR3, PWR4) the DMD high voltage lines (HV) sequentially enable. At the end of this sequence, the DLPA4000 becomes fully powered and ready for projection.

1. DMD_VOFFSET
2. delay
3. VOFS_STATE_DURATION (register 0x10) DMD_VBIAS
4. delay
5. VBIAS_STATE_DURATION (register 0x11) DMD_VRESET

For shutdown there are two sequences, normal shutdown (図 23) and a fault fast shutdown used in case a fault occurs (図 24).

This is the shutdown sequence during normal mode operation

1. 25-ms delay
2. PROJ_ON pin goes low
3. DMD_VBIAS and DMD_VRESET stop regulating
4. 10 ms delay
5. DMD_OFFSET stops regulating
6. RESET_Z goes low
7. 1 ms delay
8. all three voltages discharge
9. all other supplies de-energized
10. INT_Z remains high

INT_Z remains high during the shutdown sequence because no fault occurred. During the power-down sequence the device makes sure the HV levels do not violate the DMD specifications on these three lines. For this it is important to select the capacitors such that $C_{VOFFSET}$ is equal to C_{VRESET} and C_{VBIAS} is ≤ $C_{VOFFSET}$, C_{VBIAS}.

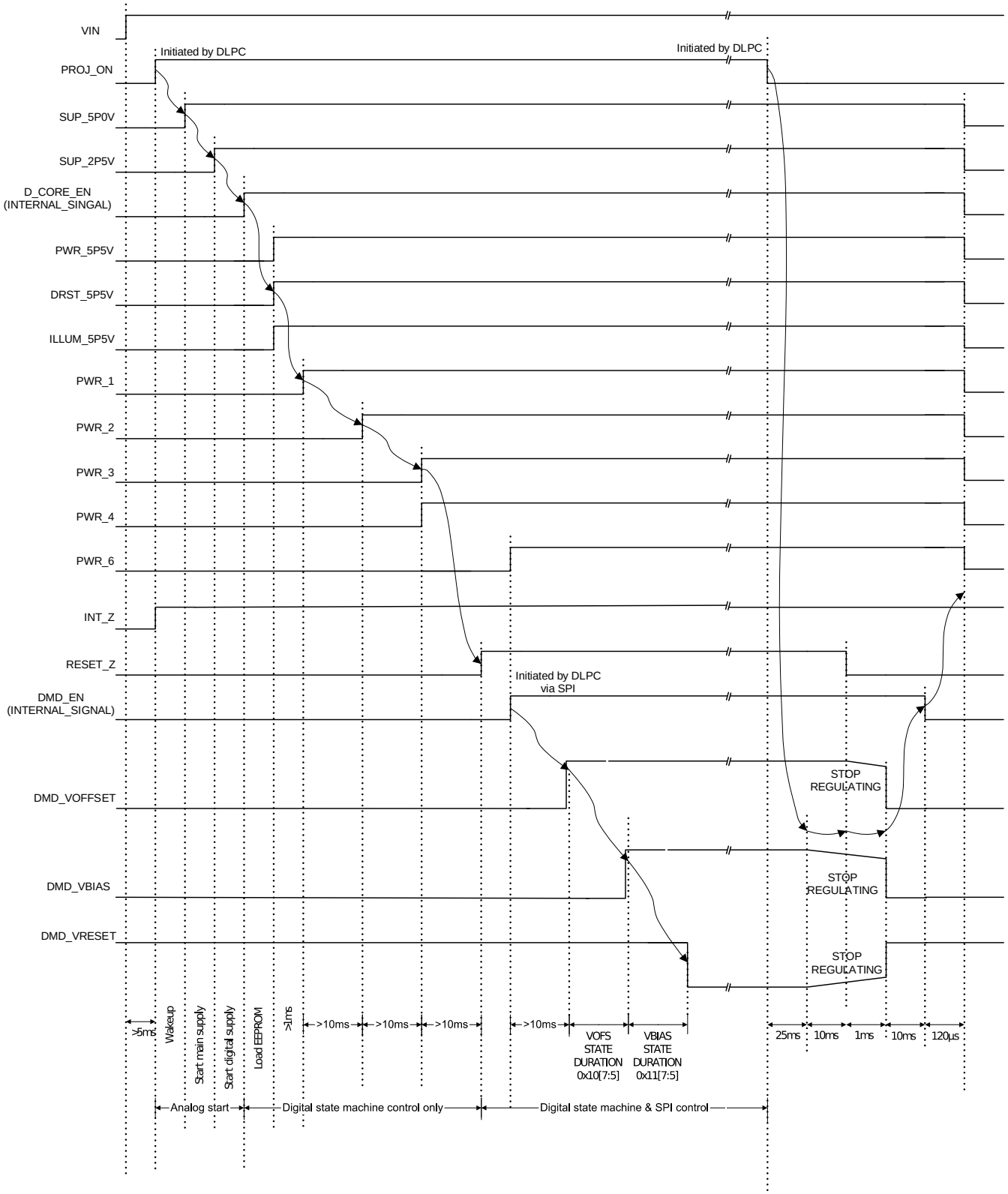
The fast shutdown mode (図 24) sequence starts in case a fault occurs (INT_Z is pulled low), for instance due to overheating.

Power-Up and Power-Down Timing (continued)

Use register 0x01 to enable and disable fast shutdown mode (FAST_SHUTDOWN_EN). Fast shutdown mode is the default mode. After the fault occurs, regulation of DMD_VBIAS and DMD_VRESET is stopped. The time (delay) between fault and stop of regulation can be controlled via register 0x0F (VBIAS/VRST_DELAY). The delay can be selected between 4 µs and approximately 1.1 ms, where the default is approximately 540 µs. A defined delay-time after the regulation stopped, all three high voltages lines are discharged and RESET_Z is pulled low. The delay can be controlled via register 0x0F (VOFS/VRESETZ_DELAY). Delay can be selected between 4 µs and approximately1.1ms. The default is ~4 µs. Finally the internal DMD_EN signal is pulled low.

The DLPA4000 device remains in standby state until the fault resolves. The device restarts then the fault resolves. The restart sequence begins when the device energizes the PWR_3 pin and follows the same steps as the regular startup sequence (see 図 24). select capacitors so that $C_{VOFFSET}$ is equal to C_{VRESET} and C_{VBIAS} is ≤ $C_{VOFFSET}$, C_{VBIAS}. This selection criteria ensures proper discharge timing and discharge levels.

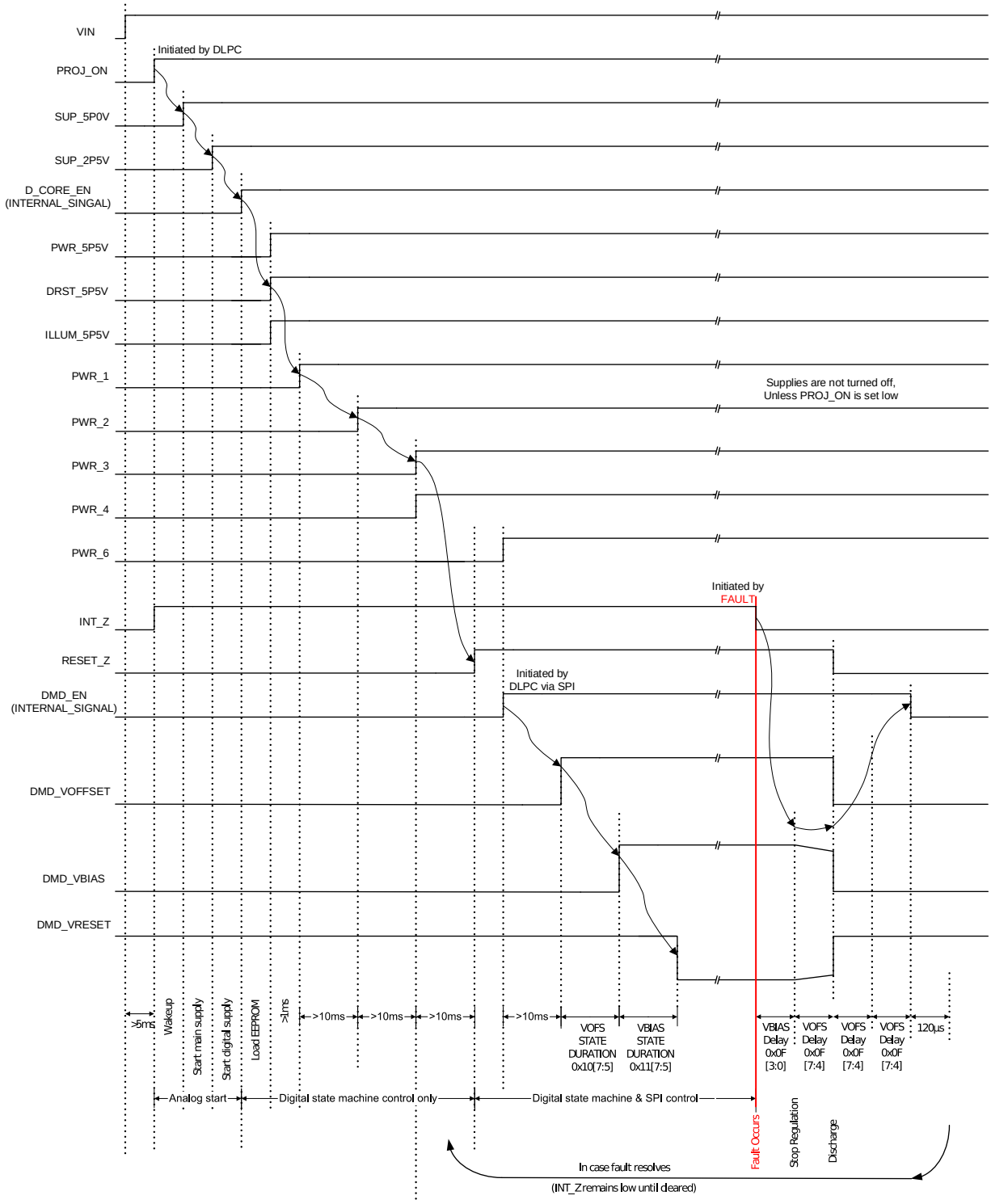
Power-Up and Power-Down Timing (continued)



Note: Arrows indicate sequence of events automatically controlled by digital state machine. Other events are initiated under SPI control.

図 23. Power Sequence Normal Shutdown Mode

Power-Up and Power-Down Timing (continued)



Note: Arrows indicate sequence of events automatically controlled by digital state machine. Other events are initiated under SPI control.

図 24. Power Sequence Fault Fast Shutdown Mode

11 Layout

11.1 Layout Guidelines

Make sure to consider high peak currents and high switching frequencies when designing the layout to avoid instability and EMI problems.

- Use wide and short traces for high-current paths and for high-current return power ground paths.
- Place, the input capacitor, output capacitor, and the inductor of the DMD HV regulator as close as possible to the DLPA4000 device.
- Separate the ground traces and connect them together at a central point underneath the device package. This design minimizes ground noise coupling between different buck converters
- The recommended value for the DMD capacitors is 1 µF for VRST and VOFS, 470 nF for VBIAS. The inductor value is 10 µH.

The currents of the buck converters are highest near pins VIN, SWITCH and PGND (). The voltage at the pins VIN, PGND and FB are DC voltages. the SWITCH pin voltage a value betweent eh value of the VIN viltage and teh PGND voltage. The red line in 図 25 indicates the current flow when the MOSFET between pin 52 and pin 53 is closed. The blue line indicates the current flow when the MOSFET between pin 53 and pin 54 is closed.

The buck converter paths carry the highest currents. Make sure the buck converter paths are as short as possible.

For the LDO DMD, it is recommended to use a 1-µF, 16-V capacitor on the input and a 10-µF, 6.3-V capacitor on the output of the LDO assuming a battery voltage of 12 V.

For LDO bucks, it is recommended to use a 1-µF, 16-V capacitor on the input and a 1-µF, 6.3-V capacitor on the output of the LDO.

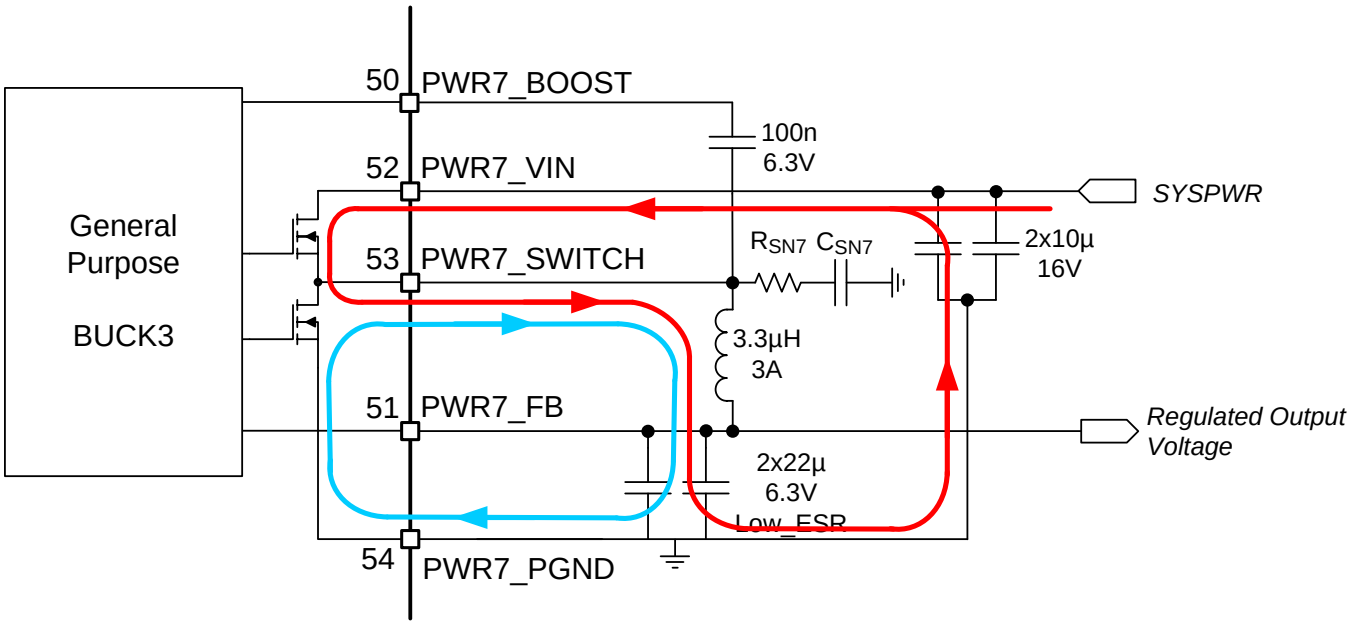


図 25. High AC Current Paths in a Buck Converter

The trace to the VIN pin in this design has high AC currents that prevents voltage drop across the trace. Make sure the trace to the VIN pin has low resistance.

Place the decoupling capacitors as close to the VIN pin as possible.

The SWITCH pin alternates connection to the VIN pin or GND. The SWITCH pin voltage waveform is square with an amplitude equal to VIN. The SWITCH pin voltage containing high frequencies. This situation causes EMI problems unless properly mitigated. Reduce EMI by creating a snubber network (R_{SN7} and C_{SN7}) Place the resistor and capacitor at the SWITCH pin to prevent or suppress unwanted high-frequency ringing during switching.

Layout Guidelines (continued)

The PGND pin sinks high current. Connect the PGND pin to a star ground point so that it does not interfere with other ground connections.

The FB pin is the sense connection for the regulated DC output voltage. No current flows through the FB pin. The device compares the voltage on the FB pin with the internal reference voltage. This comparison controls the loop. Make the FB connection at the load so that the I-R drop does not affect the sensed voltage.

11.1.1 LED Driver

The layout of the LED driver area of the PCB affects the performance of the DLPA4000 as an LED driver. Incorrect layout can cause high-current voltage ringing. High-current rining damages electronics and causes visible effects on the illumination.

11.1.1.1 PowerBlock Gate Control Isolation

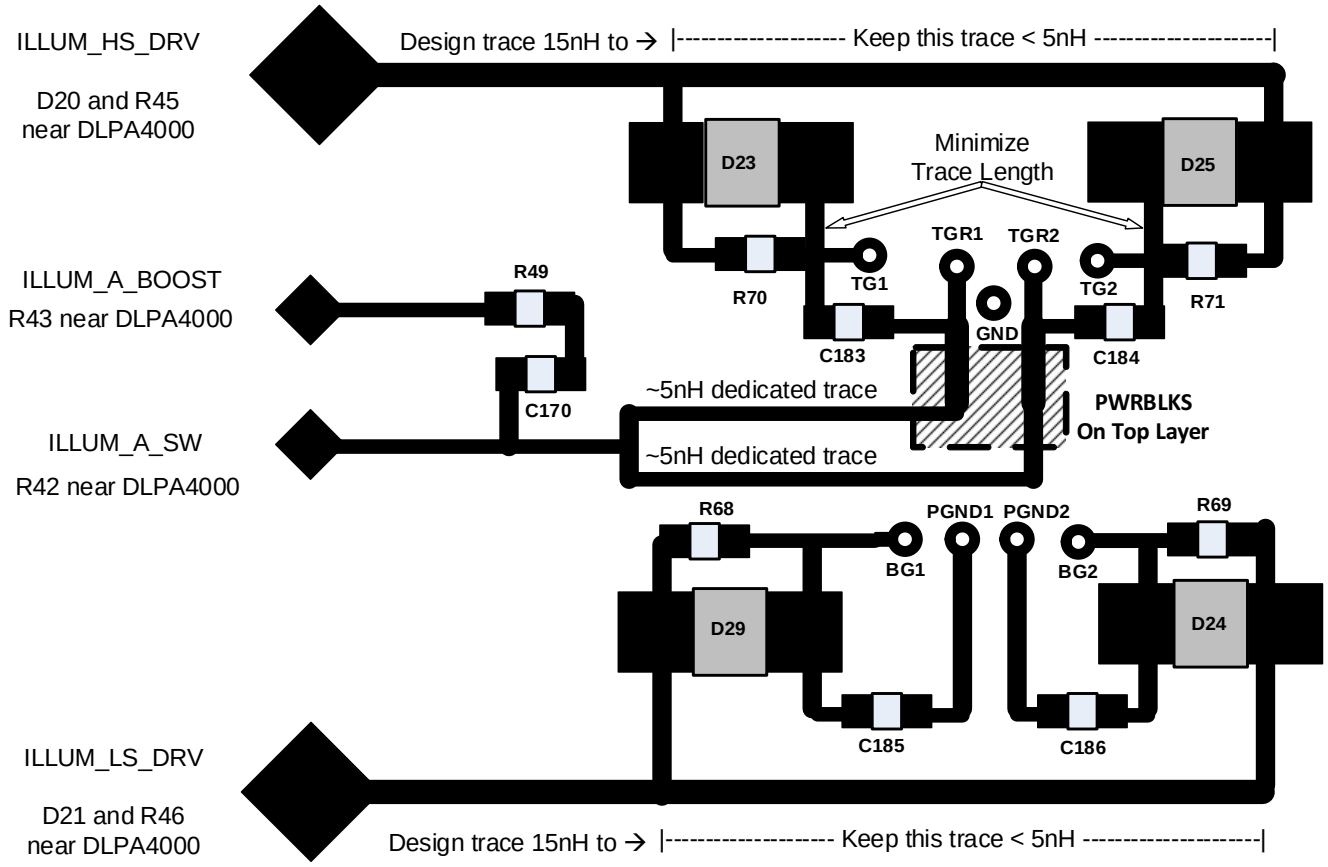


図 26. DLPA4000 Illumination Bottom Layout

The two power blocks *Synchronous Buck NexFET™ Power Block MOSFET Pair* in the reference design connects Q11 and Q12 in parallel. This design feature reduces current loss and power loss in the application. Place the two power blocks close to each other. Implement the gate control isolation topologies in the reference design to prevent feedback and ringing on the gate control line from the DLPA4000.

Place a single-shared ILLUM_HS_DRV trace from the PMIC to the two separate gate filtering and isolation component sets (D23, R70, and C183) and (D25, R71, and C184). Place each set close to the the power block high-side MOSFET pins. Minimize the ILLUM_HS_DRV route length. Minimize coupling to other routes. Terminate the ILLUM_HS_DRV from the PMIC in a T-junction. Make sure this termination is very close to the power blocks. Minimize the route beyond the T-junction that goes between the two filter and isolation component sets. Make sure the routing inductance is 5 nH or less on the trace between the filter and isolation sets.

Layout Guidelines (continued)

Place D23, R70, and C183 very close together and underneath Q11 with the goal of minimizing the net connecting D23, R70, C183, and the high-side MOSFET pin (Q11 Pin 3). The high-side MOSFET return pin (Q11 Pin 4) requires an independent 5-nH trace before merging with the Top Gate Return of Q12. Make sure that the merged Top Gate Return trace has an inductance of 15 nH on the return to the R-C filter (C170 and R49) near the DLPA4000 device. The isolation components near the Top Gate pin of Q12 (D25, R71, and C184) must follow the same requirements as those isolating Q11 (D23, R70, and C183). The inductance of the high-side illumination driver net connecting D25 to D23 must maintain a value below 5 nH. The high-side MOSFET return pin (Q12 pin 4) requires a 5-nH independent trace before merging with the Q11 Top Gate Return path back to the RC filter.

Route a single-shared ILLUM_LS_DRV trace from the PMIC to the two separate gate filtering and isolation component sets (D29, R68, and C185) and (D24, R69, and C186). Place each component set close to the power block low-side MOSSFET pins. Minimize the ILLUM_LS_DRV route length. Minimize coupling the ILLUM_LS_DRV route to other routes. Terminate the ILLUM_LS_DRV from the PMIC in a T-junction. Make sure this termination is very close to the power blocks. Minimize the route beyond the T-junction that goes between the two filter and isolation component sets. Make sure the routing inductance is 5 nH or less on the trace between the filter and isolation sets)

Make sure the inductance of the trace from D21 and R46 to D29 is as close to 15 nH as possible. Place D29, C185, and R68 directly underneath Q11 to minimize trace impedance. Similarly, place D24, C186, and R69 underneath and as close as possible to Q12. Make sure the inductance of the trace connecting D24 to D29 is less than 15 nH.

11.1.1.2 VIN to PowerBlocks

Create a dedicated VIN path (in addition to an internal VIN plane) directly to the power blocks (Q11 and Q12) on the top layer of the board. Use 2 oz. (7 mm or larger) copper in the layout for VIN, the dedicated VIN return (bottom layer), and all other high-power nets. Tie the two planes at the input power connector only. This connection significantly reduces the 32-A switching noise from the power blocks on the internal VIN plane for the rest of the DLPA4000 integrated switching power supplies.

Layout Guidelines (continued)

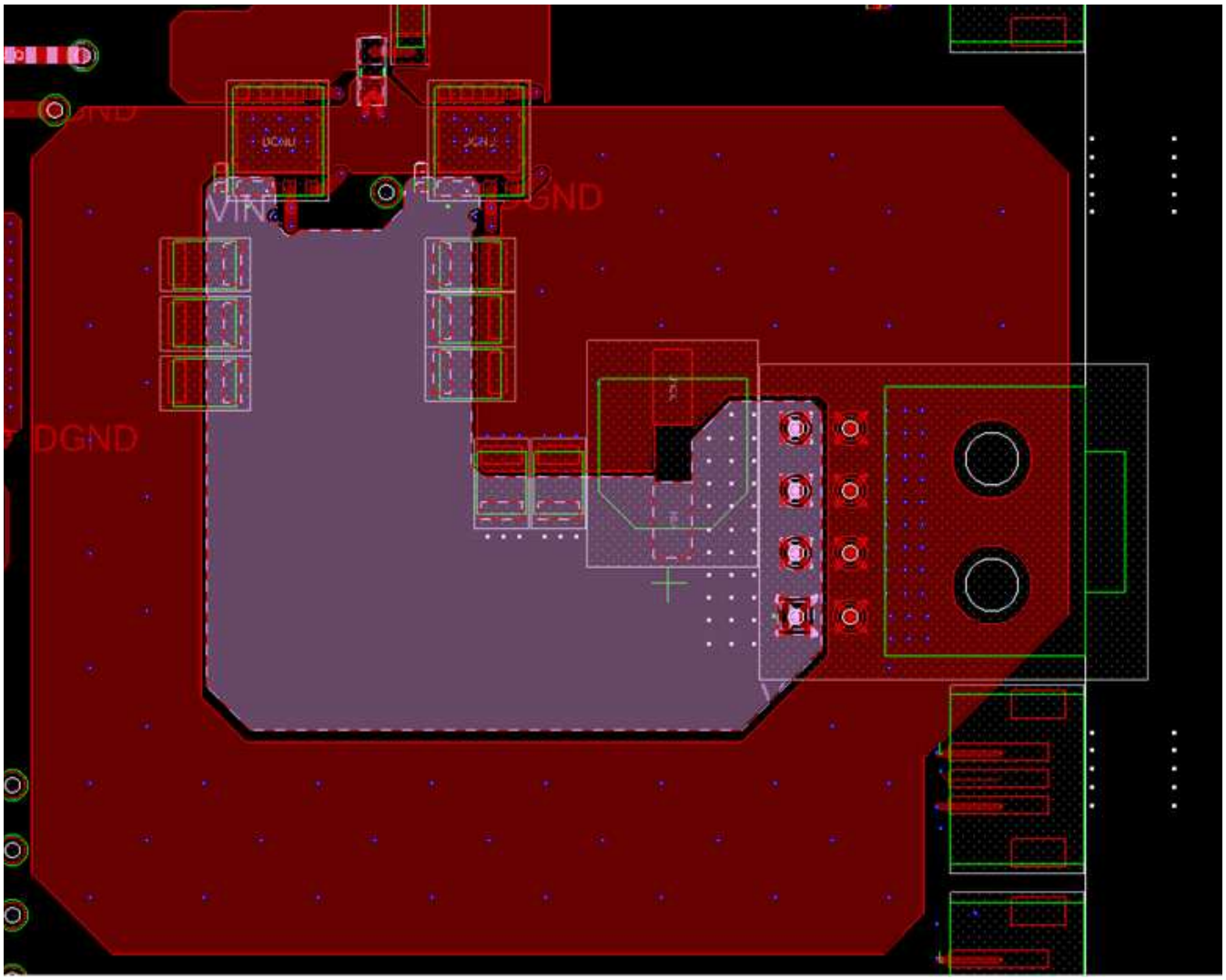


図 27. Dedicated VIN Path

11.1.1.3 Return Current from LEDs and RSense

The R_{SENSE} resistor (R72) senses the LED current. Connect the RLIM_K_1 and RLIM_K_2 lines close to the top side of the measurement resistor to accurately measure the LED current. Connect the RLIM_BOT_K_1 and RLIM_BOT_K_2 lines close to the bottom side of the measurement resistor to accurately measure the LED current.

The switched LED current flows through the R_{LIM} resistor and the R_{SENSE} resistor. Design a low-ohmic ground connection from the R_{SENSE} resistor that retuns to the input voltage connector. Make sure the PGND return has a dedicated plane on the top layer that returns to the connector. However, the PGND top layer must have vias placed from inside the top layer to the internal PGND plane. Make sure the PGND vias underneath the power block are compliant with the power block layout thermal guidelines. See CSD87350Q5D data sheet for guidelines..

Make sure the designer considers the entire return path for current from the LED connector through the R_{LIM} resistor plane and the R_{SENSE} resistor (R72) during layout. Any obstacles between the LED connectors and the PGND on the input power connector can cause power reduction. Similar obstacles can cause possible image artifacts due to slow LED turn-on times. See the reference design for a suggested placement and plane sizes.

Layout Guidelines (continued)

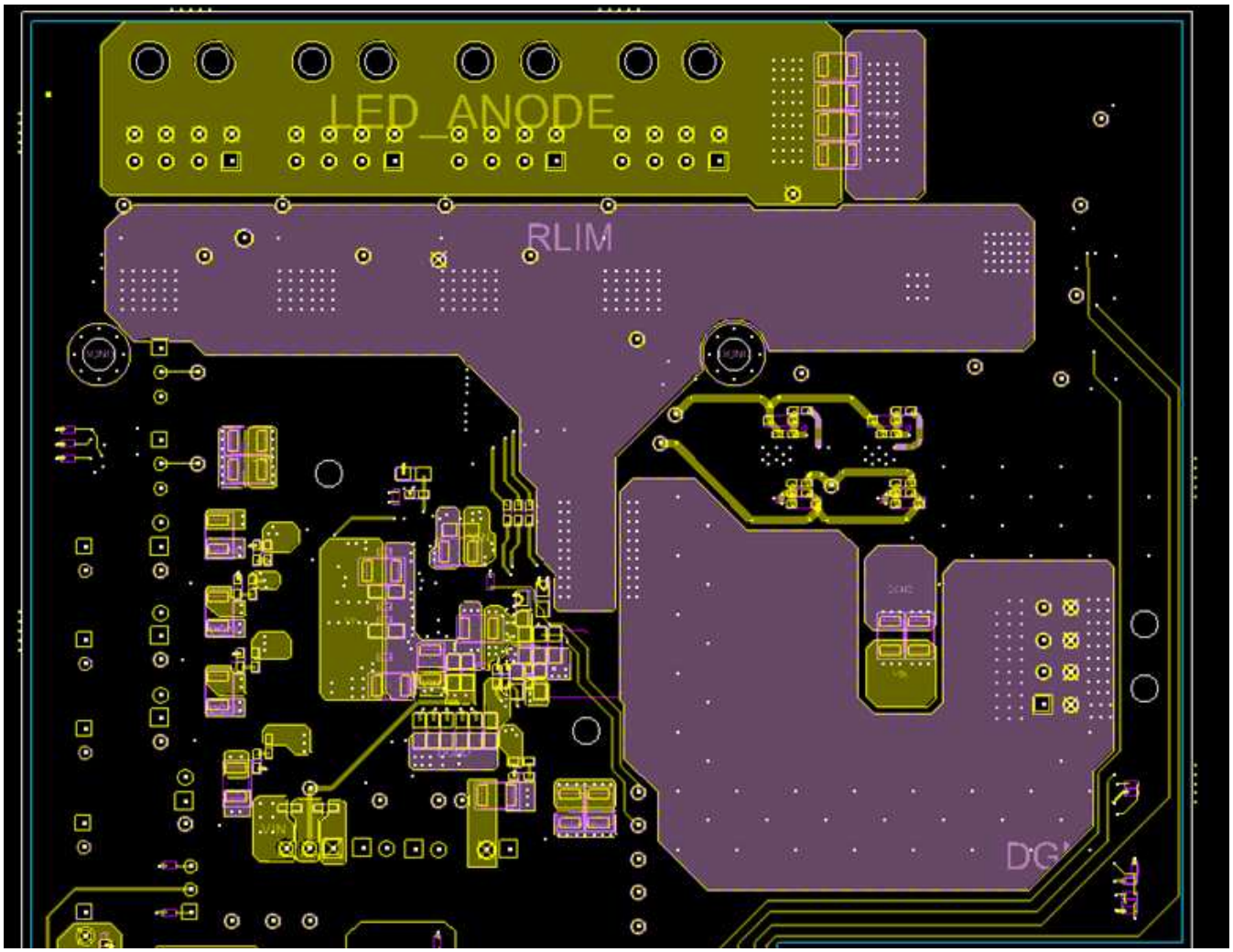


図 28. Current Return Path

11.1.1.4 RC Snubber

Proper operation requires snubber networks. The switching frequency can vary from several hundreds of kHz to frequencies in the MHz range. To switch currents from zero to several amperes requires only nanoseconds, equivalent to even much higher frequencies. EMI can occur when ringing occurs on the edges. This ringing can have higher amplitude and frequency than the switching voltage. All DLP4000 buck converters require a snubber network to prevent ringing. The snubber network comprises a resistor and a capacitor in series.

Place an R-C snubber network (C32 and R56) to reduce ringing on the switching node. Place the capacitor on top of a large plane for the switching node directly next to the PGND plane. This resistor placement eliminates the gap between the switching node and the PGND plane used by the PowerBlocks.

Layout Guidelines (continued)

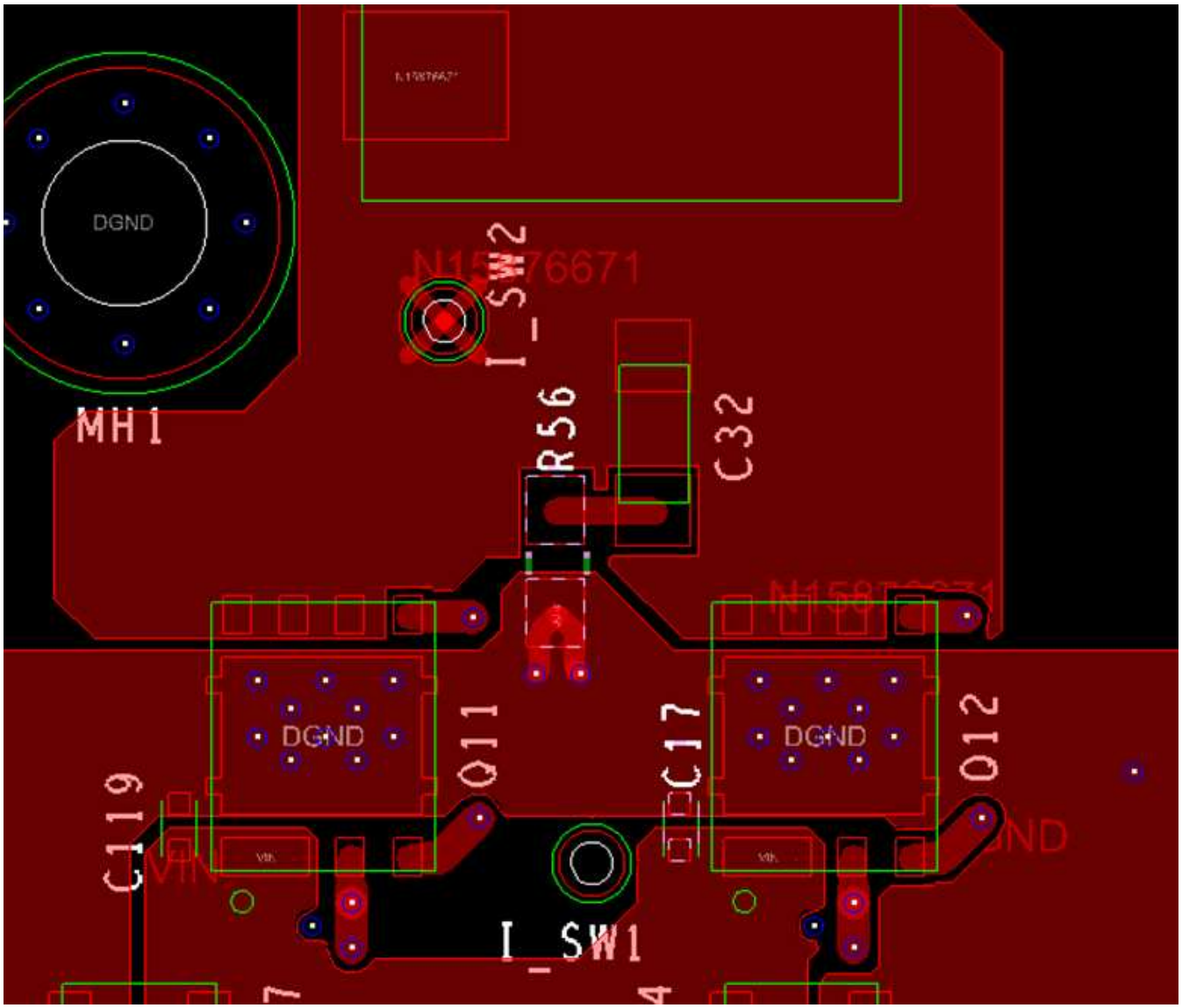


図 29. RC Snubber Layout

11.1.1.5 Capacitor Choice

Be aware of the voltage coefficient of the decoupling capacitors. Physically undersized ceramic capacitors (with respect to the capacitance value to physical size ratio) experiences a large reduction in capacitance. Depending on the VIN voltage chosen and the voltage rating of the capacitors, physically undersized capacitors can experience up to a 90% reduction in capacitance, leading to insufficient decoupling.

Choose decoupling capacitors (C17 and C119) with a value of 0.1 µF and a size of 0402. Place the decoupling capacitors as close as possible to the power block VIN pins. Even an increased distance as small as 1 mm in compared to the reference design can cause a large increase in voltage ringing amplitude. Because the parasitic inductance of the route combined with the effective inductance of the capacitor affects the switching node, select capacitors with a higher SRF rating. Place the VIN decoupling capacitors on the top layer very close to the power blocks to minimize parasitic inductance. Place the 10-µF decoupling capacitors (C18, C114, C115, C116, C117, and C118) near the power blocks, They do not need to be as close as the 0.1-µF capacitors.

Layout Guidelines (continued)

11.1.2 General Purpose Buck 2

Use short traces. Separate individual power grounds to avoid ground shift problems. Ground shift problems occur when ground currents of different buck converters interfere. High currents flow through the inductor (L7) and the output capacitors (C130, C131).Make the traces to and from inductor and capacitors as short as possible to avoid losses due to trace resistance. Use high-quality capacitors with a low ESR value to minimize losses in the capacitors and to maintain an acceptable amount of voltage ripple.

The next paragraph explains how to place and connect components near PWR6 Buck converter which are those component connected to pins 62, 63, 64, 65, and 66.

Connect the supply voltage i to pin 64 with sufficient copper to make it stable and of low resistance. Use multiple vias to the ground layer to connect pin 62 to ground. Use multiple layers create low resistive paths. Make sure the ground connection of the output capacitors and the ground connection of the DLPA4000 (pin 62) are close together. Connect both points using a wide trace. All buck converters in the layout use a separated ground trace to their respective ground connection on the DLPA4000. All these ground connections are connected together on the ground plane below the DLPA4000 package.

図 30 shows the position of the converter inductor and the accompanying capacitors (L7, C130, and C131) positioned as close as possible to pin 62 and pin 64 using the thickest traces that are feasible. Make these ground connections by using multiple vias to the ground layer to ensure a low-resistance path.

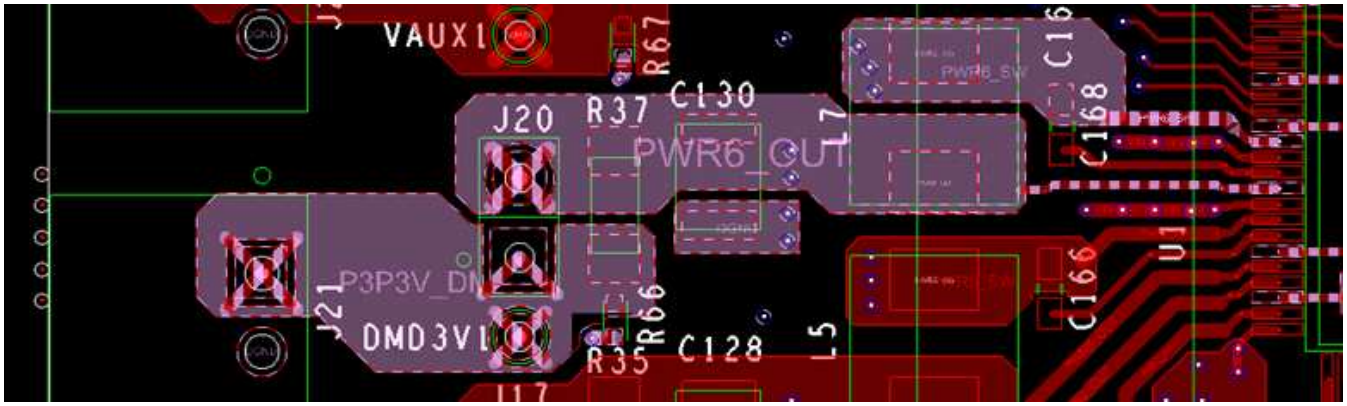


図 30. General Purpose Buck Layout

11.1.3 SPI Connections

The SPI interface comprises several digital lines and the SPI supply. Communication errors can occur if interface lines are not routed properly. Prevent interference on the SPI lines by placing noisy and interfering sources away from the interface.

Prevent noise by routing the SPI ground line with the digital lines to the respective pins as much as possible. Connect the SPI interface with a separate ground connection to the DGND pin of the DLPA4000 device. This design style prevents ground noise between SPI ground references of DLPA4000 and DLPC due to the high current in the system.

Layout Guidelines (continued)

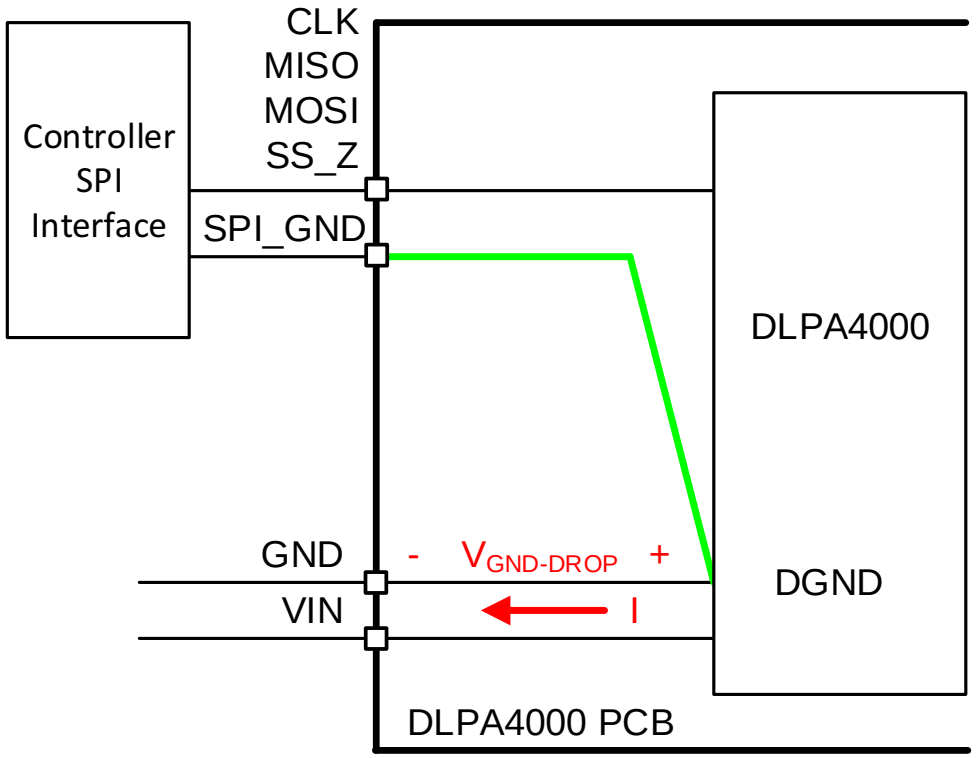


図 31. SPI Connections

Separate interfering sources from the interface lines. For example, high-current lines such as those near the PWR_7 pin and the SPI_CLK pin are too close, false clock pulses and communication errors can occur.

11.1.4 R_{LIM} Routing

The resistor R_{LIM} senses the LED current. Connect the RLIM _K_1 and RLIM _K_2 lines close to the high-side of measurement resistor R_{LIM} to accurately measure the LED current. Connect the RLIM_BOT_K_1 pin and the RLIM_BOT_K_2 pin close to the high-side of measurement resistor R_{LIM}.

The switched LED current flows through the R_{LIM} resistor. Use a low-ohmic ground connection for R_{LIM} .

11.1.5 LED Connection

Large switched currents flow through the wiring from the external RGB switches to the LEDs. Consider these two specifications to optimize the LED-to-RGB switches wiring layout:

1. wiring resistancce, R_{SERIES}
2. wiring inductance, L_{SERIES}

図 32 shows the parasitic series impedances.

Layout Guidelines (continued)

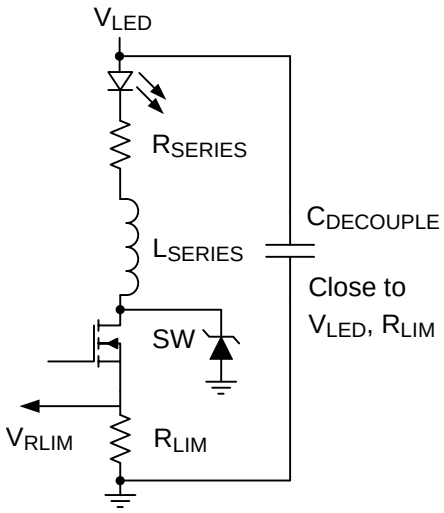


図 32. Parasitic Inductance (L_{Series}) and Resistance (R_{series}) in Series with LED

Currents up to 32 A can flow through the wires connecting the LEDs to the RGB switches. The layout can cause noticeable dissipation. Every 10 mΩ of series resistances implies a parasitic power dissipation of 5 W for a 32 A (avg) LED current . This dissipation can cause an increase in PCB temperature, and more importantly, deterioration of overall system efficiency.

The wiring resistance may impact the control dynamics of the LED current. The LED current control loop includes the routing resistance. The LED voltage (V_{LED}) controlls the LED current. Use 式 15 to calculate the total differential resistance of a path R_{SERIES}.

$$\Delta I_{LED} = \frac{\Delta V_{LED}}{r_{LED} + R_{series} + R_{ON_{SW\,P},Q,R} + R_{LIM}} \quad (15)$$

where

- ΔI_{LED} is the LED current variation
- ΔV_{LED} is a small change in V_{LED}
- r_{LED} is the differential resistance of the LED
- $R_{on\_SW\_P,Q,R}$ the on-resistance of the strobe decoder switch
- L_{SERIES} is ignored

式 15 ignores L_{SERIES} because realistic values are usually sufficiently low to cause any noticeable impact on the dynamics

All differential resistance values range from about 4 mΩ to several hundreds of mΩ. Applications can yield a series resistance of 100 mΩ if the layout guidelines are not followed. Make sure the application series resistance is <10 mΩ.

The series inductance plays an important role when considering the switched nature of the LED current. the current switches through R,G and B LEDs quickly. The turn-off time is significantly fast. A current of 32 A goes to 0 A in 50 ns. This speed causes a voltage spike of approximately 1 V for every 5 nH of parasitic inductance. Minimize the series inductance of the LED wiring by designing an application that has these features:

- Short wires
- Thick wires or multiple parallel wires
- Small enclosed area of the forward and return current path

Layout Guidelines (continued)

Use a diode when the application cannot be designed to yield a sufficiently low inductance. Use a Zener diode to clamp the drain voltage of the RGB switch so that it remains below the absolute maximum rating. Choose a clamping voltage between the maximum expected V_{LED} and the absolute maximum rating. Make sure the clamping voltage has sufficient margin relative to the minimum and maximum voltage.

11.2 Layout Example

図 33 shows an example of a proper buck converter layout. It shows the routing and placing of the components near the DLPA4000 for optimal performance. A register sets the output voltage of the converters used by the DLPA4000. The DLPA4000 uses the feedback pin to compare the output voltage with an internal setpoint.

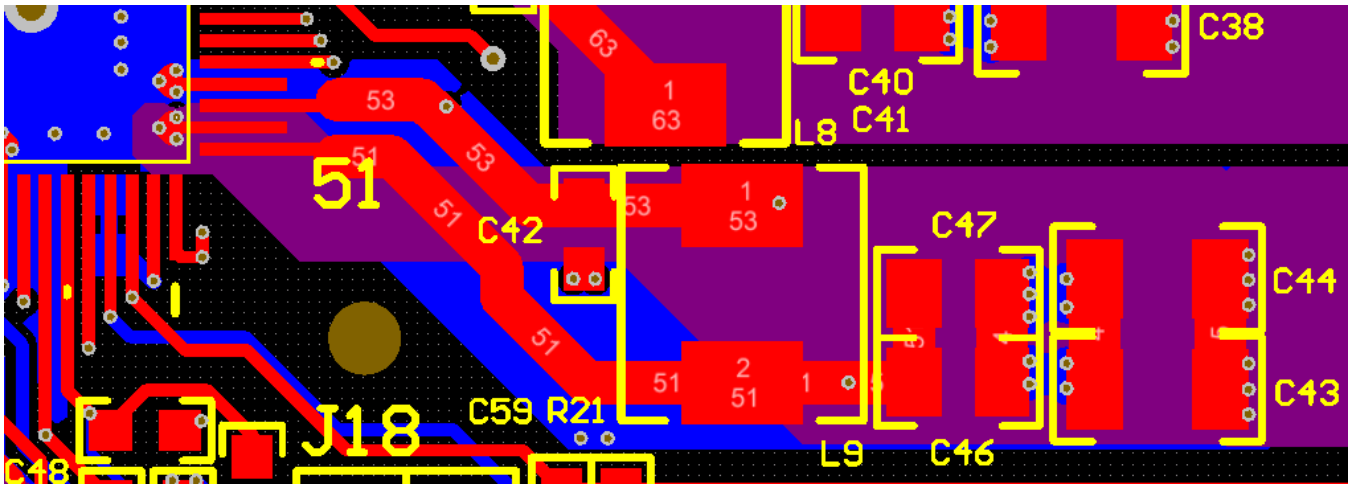


図 33. Practical Layout Example

Use short traces. Separate individual power grounds to avoid ground shift problems. Ground shift problems occur when ground currents of different buck converters interfere. High currents flow through the inductor (L7) and the output capacitors (C130, C131).Make the traces to and from inductor and capacitors as short as possible to avoid losses due to trace resistance. Use high-quality capacitors with a low ESR value to minimize losses in the capacitors and to maintain an acceptable amount of voltage ripple.

In order to prevent problems with switching high currents at high frequencies the layout is very critical and snubber networks are advisable. The switching frequency can vary from several hundreds of kHz to frequencies in the MHz range. Keep in mind that it takes only nanoseconds to switch currents from zero to several amperes which is equivalent to even much higher frequencies. Those switching moments causes EMI problems if not properly handled, especially when ringing occurs on the edges, which can have higher amplitude and frequency as the switching voltage itself. To prevent this ringing the DLPA4000 buck converters all need a snubber network, consisting of a resistor and a capacitor in series implemented on the board to reduce this unwanted behavior. The snubber network is in this case placed on the bottom-side of the PCB (thus not visible here) connected to the trace of L9 routing to the switch node.

In order to make more clear what plays a role when laying out a buck converter, this paragraph explains the connections and placing of the parts around the buck converter connected to the pins 50-54. The supply voltage is connected to pin 52 which is laid out on a mid layer (purple colored) and is connected to this pin using 3 via's to make sure a stable and low resistance connection is made. The decoupling is done by capacitor C43 & C44 visible on the bottom right of 図 33 and the connection to the supply and the ground layer is done using multiple vias. The ground connection on pin 54 is also done using multiple vias to the ground layer which is visible as the blue areas in 図 33. By using different layers it is possible to create low resistive paths. Ideally the ground connection of the output capacitors and the ground connection of the part (pin54) should be close together. The layout connects both points together using a wide trace on the bottom layer (blue colored area) which is also suitable to bring both connections together. All buck converters in the layout have the same layout structure and

Layout Example (continued)

use a separated ground trace to their respective ground connection on the part. All these ground connections are connected together on the ground plane below the DLPA4000 itself. shows the position of the converter inductor and its accompanying capacitors (L9 & C46, C47) as close as possible positioned to the pins 51 and 53 using traces as thick as possible. The ground connections of these capacitors is done using multiple via's to the ground layer to ensure a low resistance path.

11.3 Thermal Considerations

Integrated circuits in low-profile and fine-pitch surface-mount packages typically require special attention to power dissipation. Many different system-dependent issues affect the power dissipation limits of individual component. These issues include

- thermal coupling
- airflow
- added heat sinks
- added convection surfaces
- other heat-generating components

These three basic approaches enhance thermal performance.

- Improve the heat sinking capability of the PCB
- Increase heat sink capability on top of the package
- Increase airflow in the system

The DLPA4000 device has efficient power converters. But because the power delivered to the LEDs can be quite large (more than 50 W in some case) the power dissipation in the DLPA4000 device can be high. Use proper temperature calculation to minimize power dissipation in the application.

It is important to maintain the junction temperature below the maximum recommended value of 120°C during operation. Calculate P_{DISS}, to determine the junction temperature of the DLPA4000. P_{DISS} is a summation of all power dissipation. Use 式 16 to calculate T_J.

$$T_J = T_A + P_{DISS} \times R_{\theta JA}$$

where

- T_A is the ambient temperature
- $R_{\theta JA}$ is the thermal resistance from junction-to-ambient (16)

The total power dissipation varies depending on the application specifications. The main variances in the DLPA4000 circuitry are:

- Buck converters
- LDOs

Use 式 17 to calculate the dissipation for the buck converter.

$$P_{diss\_buck} = P_{in} - P_{out} = P_{out}\left(\frac{1}{\eta_{buck}} - 1\right)$$

where

- η_{BUCK} is the efficiency of the buck converter
- P_{IN} the power delivered at the input of the buck converter
- P_{OUT} the power delivered to the load of the buck converter (17)

shows efficiency for buck converters PWR1, PWR2, PWR5, PWR6, and PWR7.

Buck converters require high power efficiency because they typically handle the highest power levels. Linear regulators,(for example, LDOs) handle lower power levels. Because the efficiency of an LDO can be relative low, the related power dissipation can be significant.

Use 式 18 to calculate the power dissipation of an LDO, $P_{DISS(ldo)}$.

$$P_{DISS\,(ldo)} = (V_{IN} - V_{OUT}) \times I_{LOAD}$$

Thermal Considerations (continued)

where

- V_{IN} is the input supply voltage
- V_{OUT} is the output voltage of the LDO
- I_{LOAD} is the load current of the LDO

(18)

Because the voltage decrease over the LDO ($V_{IN} – V_{OUT}$) can be relative large, a relatively small load current can yield significant power dissipation in the DLPA4000 device. In this case, consider using one of the general purpose bucks to have a more power-efficient solition (in other words, a less dissipation solution).

It is important to consider the power dissipation of the LDO that supplies the boost power converter (the LDO DMD). The boost converter supplies high voltages for the DMD. This voltages are V_{BIAS}, V_{OFS}, V_{RST}.The maximum simultaneous load current $I_{LOAD(max)}$ for these lines is 10 mA . So, the maximum related power level is moderate. Use 式 19 An efficiency rate of 80% for the boost converter, η_{BOOST}, implies a maximum boost converter dissipation, $P_{DISS\ (DMD\_boost,MAX)}$.

$$P_{DISS\left(DMD_{boost\ MAX}\right)} = I_{LOAD\ (max)} \times (V_{BIAS} + V_{OFS} + |V_{RST}|) \times \left(\frac{1}{\eta_{BOOST}} - 1\right) \cong 0.1\ W \quad (19)$$

The level of power dissipation of the illumination buck converter this is likely negligible. The term that might count to the total power dissipation is $P_{diss\_LDO\_DMD}$. The input current of the DMD boost converter is supplied by this LDO. In case of an high supply voltage, a non negligible dissipation term is obtained. The worst case load current for the LDO is given by:

$$I_{LOAD\ LDO\ (max)} = \frac{1}{\eta_{BOOST}} \times \frac{(V_{BIAS} + V_{OFS} + |V_{RST}|)}{V_{DRST\ 5P5V}} \times I_{LOAD\ (max)} \cong 100\ mA \quad (20)$$

where

- the output voltage of the LDO is V_{DRST_5P5V} is 5.5 V

Dissipation of power in the LDO can be up to 1.5 W for an input supply voltage of 19.5 V. Power dissipation of 1.5 W is a worst case scenario. In most cases the load current of the LDO DMD is significantly less. Make sure to confirm the LDO current level for the specific application.

The DLPA4000 draws a quiescent current. The power supply voltage does not affect this quiescent current. For the buck converters the quiescent current is comprised in the efficiency numbers. For the LDOs a quiescent current on the order of 0.5 mA can be used. For the rest of the DLPA4000 circuitry, not included in the buck converters or LDOs, a quiescent current on the order of 3 mA applies. Use 式 21 to estimate dissipation, $P_{diss\_DLPA4000}$ in the DLPA4000 device.

$$P_{DISS\ (DLPS4000\ )} = \sum P_{BUCK} + \sum P_{LDO} \quad (21)$$

Use to calculate the maximum ambient temperature,

$$T_A = T_{J(max)} - P_{DISS} \times R_{\theta JA} = 120°C - 2.5\ W \times 7°C/W = 102.5°C \quad (22)$$

Use to calculate the junction temperature of the DLPA4000 device after you know the dissipated power and the ambient temperature.

Use Thermal Information to calculate the junction temperature for heat sink configuration and airflow.

$$T_J = T_A + P_{DISS} \times R_{\theta JA} = 50°C + 4\ W \times 7°C/W = 78°C \quad (23)$$

Use one of these three design features if the combination of ambient temperature and DLPA4000 power dissipation does not yield an acceptable junction temperature (<120°C).

1. Use a larger heat sink, which increases airflow, to reduced $R_{\theta JA}$,
2. Use lower load current through the internal general purpose buck converters..
3. Use an external general purpose buck converter instead of an internal one. This design reduces power dissipation in the DLPA4000 device

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 デバイスの項目表記

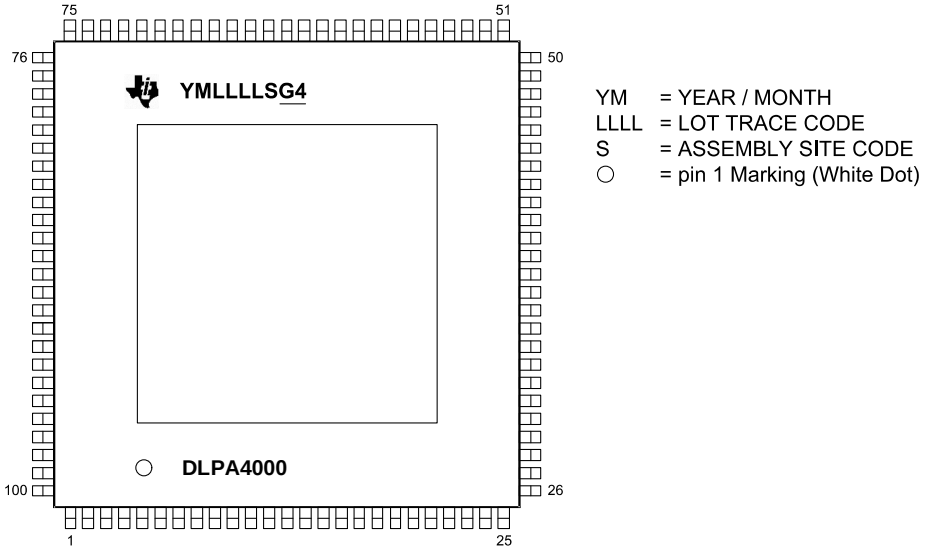


図 34. パッケージ・マーキングDLPA4000 (上面図)

12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E (Engineer-to-Engineer) コミュニティ。*** エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。

設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

12.4 商標

E2E is a trademark of Texas Instruments.
DLP is a registered trademark of Texas Instruments.

12.5 静電気放電に関する注意事項

これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

13.1 Package Option Addendum

13.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking(4)(5)
DLPA4000DPFD	ACTIVE	HTQFP	PFD	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	DLPA4000
DLPA4000DPFDR	ACTIVE	HTQFP	PFD	100	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	DLPA4000

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(5) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLPA4000PFD	ACTIVE	HTQFP	PFD	100	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	DLPA4000	Samples
DLPA4000PFDR	PREVIEW	HTQFP	PFD	100	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	DLPA4000	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

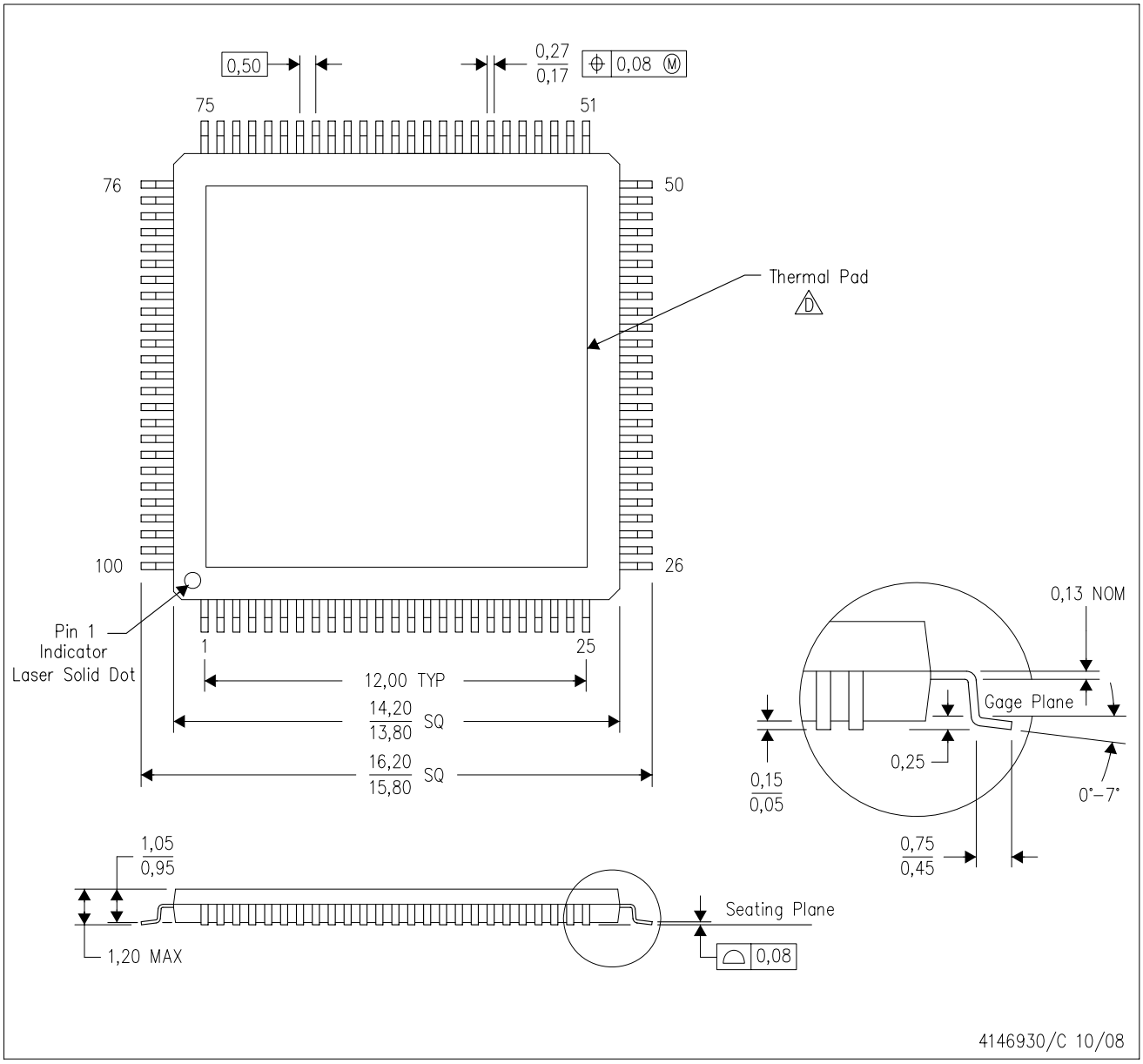
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PFD (S–PQFP–G100) PowerPAD™ PLASTIC QUAD FLATPACK (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be attached directly to an external heatsink. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>. See the product data sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

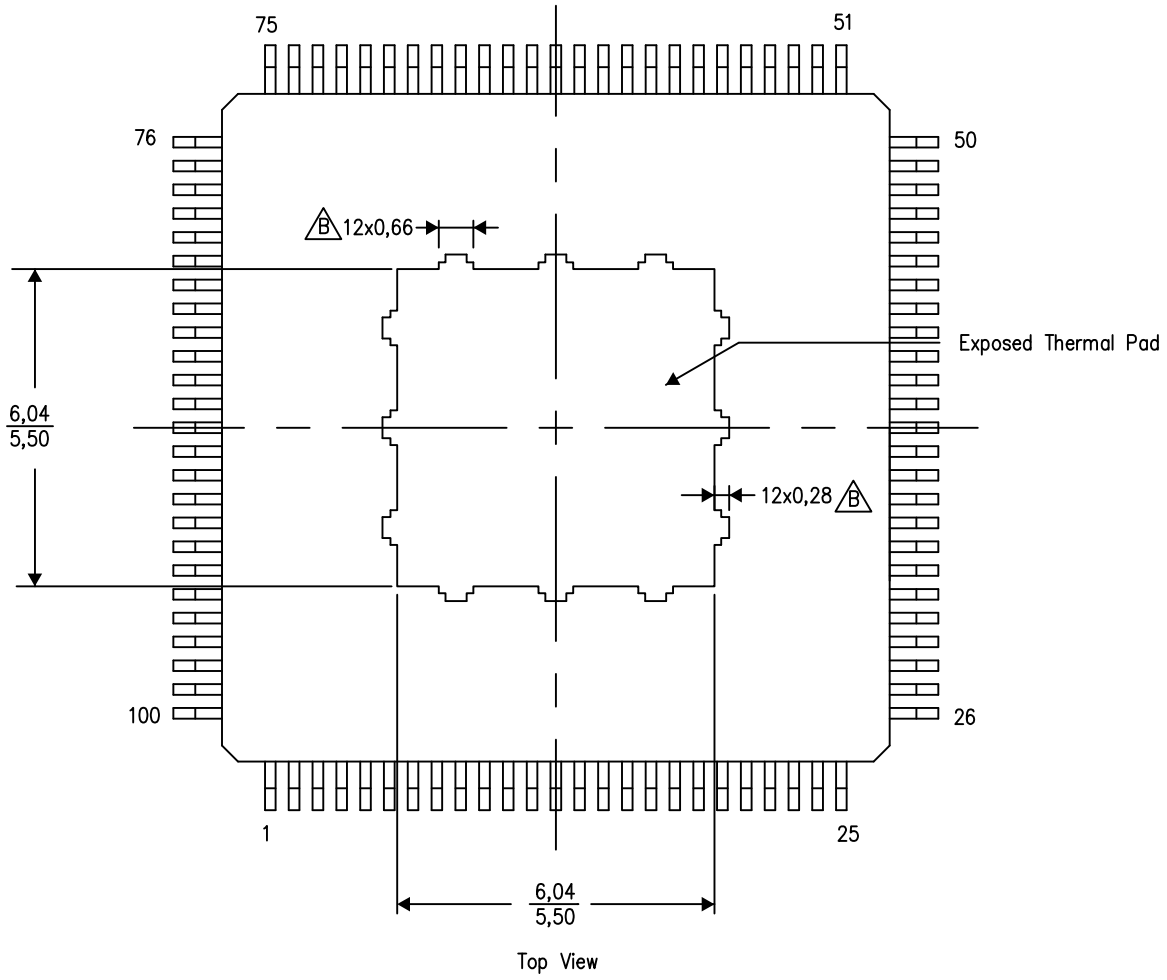
PFD (S–PQFP–G100) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

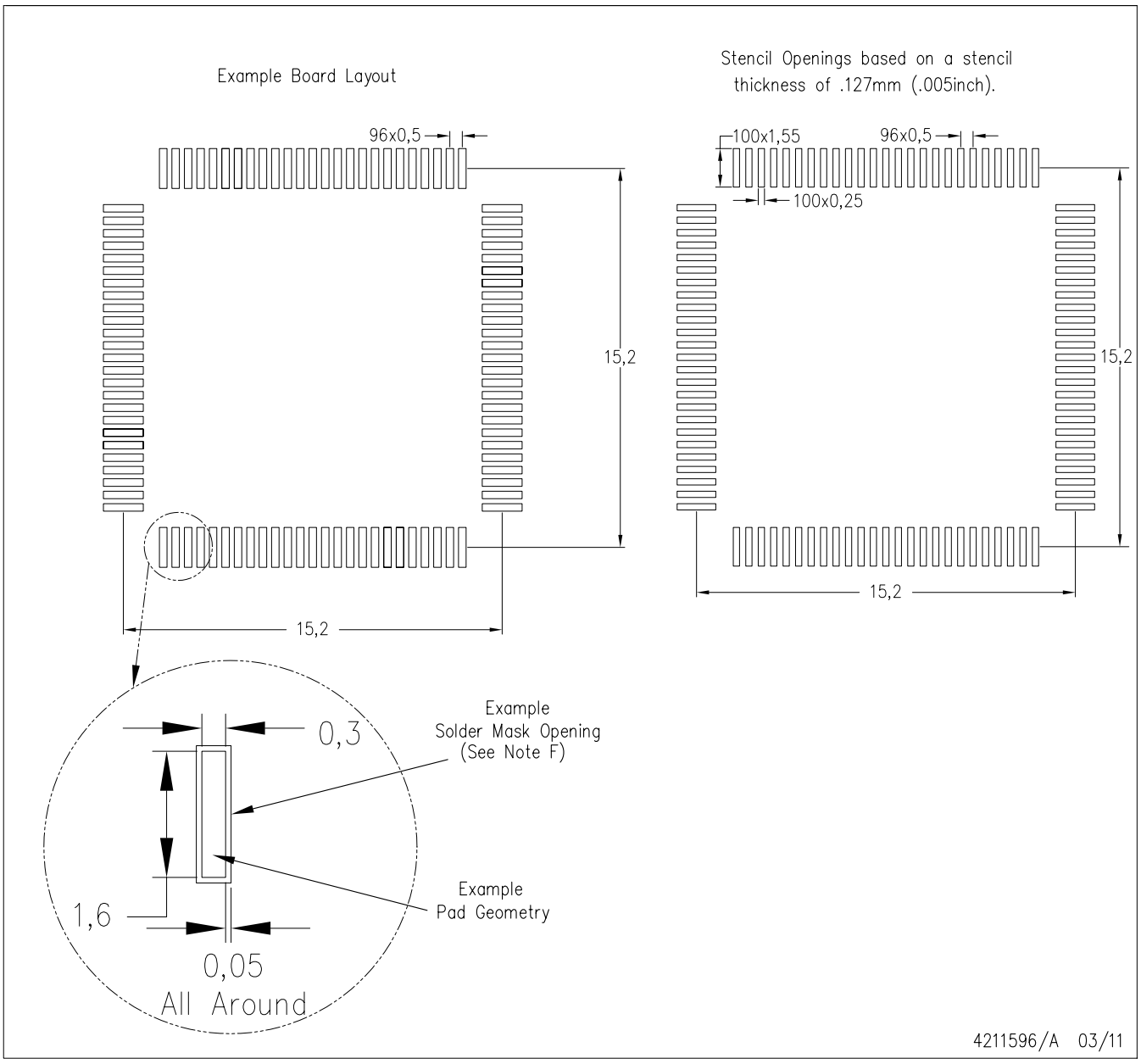
4211595–3/B 06/14

NOTE: A. All linear dimensions are in millimeters

B Tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PFD (S–PQFP–G100) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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