DLPC150 高度な照明制御用の DLP®デジタル・コントローラ

1 特長

- DLP2010 および DLP2010NIR DMD の確実な動作に必要なディスプレイ・コントローラ
- 高速のパターン・シーケンス・モード
  - 1 ビット・バイナリで最高 2880Hz のパターン速度
  - マイクロミラーへの 1 対 1 の入力マッピング
- カメラやセンサと簡単に同期
  - 1 つの入力トリガ
  - 2 つの出力トリガ
- I^2C 構成インターフェイス
- 入力ピクセル・インターフェイスのサポート
  - 24 ビットのパラレル RGB888 インターフェイス・プロトコル
  - 16 ビットのパラレル RGB565 インターフェイス・プロトコル
  - 最高 75MHz のピクセル・クロック
- マイクロミラー・ドライバ内蔵
- クロック生成機能内蔵
- 電源オフ時の自動 DMD パーキング
- 201 ピン、13mm × 13mm、0.8mm ピッチの VFBGA パッケージ

2 アプリケーション

- 分光計 (化学分析)
  - 携帯型プロセス・アナライザ
  - 携帯機器
- 圧縮センシング (単一ピクセルの NIR カメラ)
- 3D 生体認証
- マシン・ビジョン
- 赤外線シーン投影
- 顕微鏡
- レーザー・マーキング
- 光学チョッパー
- 光ネットワーク

3 概要

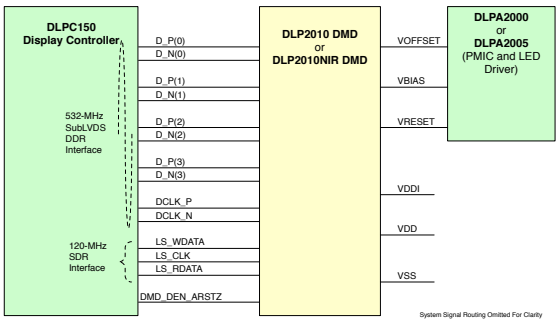
DLPC150 コントローラは、高速、高精度、高効率で光を操作しパターンを作成するための、ユーザー回路と、DLP2010 (可視光) または DLP2010NIR (近赤外線 (NIR)) デジタル・マイクロミラー・デバイス (DMD) との間の、使いやすく信頼性が高い多機能インターフェイスとして機能します。DLPC150 コントローラは高速パターン・レート、LED 制御、複数の入力形式へのデータのフォーマット化を実現します。DLPC150 コントローラは、カメラ、センサ、その他のペリフェラルと表示パターンを同期させるための入力および出力トリガ信号も生成します。DLPC150 コントローラは、DLP2010 または DLP2010NIR DMD と、DLPA2000 または DLPA2005 パワー・マネージメント IC (PMIC) を含む 0.2 WVGA チップセットの一部です。DLPC150 コントローラを使用すると、DLP® 0.2 WVGA 可視光または NIR チップセットを、スペクトルと波長をプログラマブル制御するための小フォーム・ファクタ、低消費電力、低コストのアプリケーション (例:3D スキャンまたは計測システム、分光計、対話型ディスプレイ、化学アナライザ、医療機器、皮膚分析、材料識別、化学検出) に組み込むことができます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
DLPC150	VFBGA (201)	13.00×13.00mm^2

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

DLP 0.2 インチ WVGA チップセット



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision B (March 2018) から Revision C に変更 **Page**

- Changed normal park time from 500 µs to 20 ms ... 3
- Deleted mention of bit weight for parallel data input ... 4

Revision A (March 2015) から Revision B に変更 **Page**

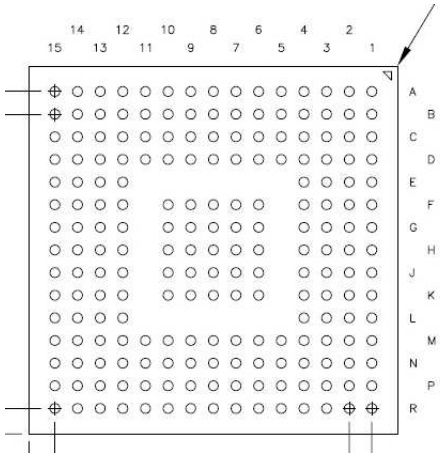
- Changed maximum binary pattern rate to 2880 Hz in Table 4 ... 27
- 「デバイスのマーキング」の図を更新 ... 47
- 「コミュニティ・リソース」セクションを追加 ... 48
- Added MSL Peak Temp and Op Temp to Packaging Option Addendum ... 49

2015年3月発行のものから更新 **Page**

- Consolidated the Pin Functions table ... 3
- Moved Storage temperature to Absolute Maximum Ratings ... 13
- Changed Handling Ratings to ESD Ratings ... 13

5 Pin Configuration and Functions

ZEZ Package
201-Pin VFBGA
Bottom View



Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
CONTROL AND INITIALIZATION			
RESETZ	C11	I_6	DLPC150 power-on reset (active low input) (hysteresis buffer). Self-configuration starts when a low-to-high transition is detected on RESETZ. All DLPC150 controller power and clocks must be stable before this reset is de-asserted. Connect to the reset output pin (RESETZ) of the DLPA2000 or DLPA2005 PMIC. Note that the following signals will be tri-stated while RESETZ is asserted: SPI0_CLK, SPI0_DOUT, SPI0_CSZ0, SPI0_CSZ1, PMIC_SPI_CLK, PMIC_SPI_CSZ, PMIC_SPI_DIN, PMIC_SPI_DOUT, TRIG_OUT_1, TRIG_OUT_2, and GPIO[19:05] External pullups or downs (as appropriate) should be added to all tri-stated output signals listed (including bidirectional signals to be configured as outputs) to avoid floating DLPC150 controller outputs during reset if connected to devices on the PCB that can malfunction. For SPI, at a minimum, any chip selects connected to the devices should have a pullup. Unused bidirectional signals can be functionally configured as outputs to avoid floating DLPC150 controller inputs after RESETZ is set high. The following signals are forced to a logic low state while RESETZ is asserted and corresponding I/O power is applied: LED_SEL_0, LED_SEL_1 and DMD_DEN_ARSTZ No signals will be in their active state while RESETZ is asserted. Note that no I^2C activity is permitted for a minimum of 500 ms after RESETZ (and PARKZ) are set high.
PARKZ	C13	I_6	DMD fast PARK control (active low Input) (hysteresis buffer). PARKZ must be set high to enable normal operation. PARKZ should be set high prior to releasing RESETZ (that is, prior to the low-to-high transition on the RESETZ input). PARKZ should be set low for a minimum of 40 µs before any power is removed from the DLPC150 such that the fast DMD PARK operation can be completed. Note for PARKZ, fast PARK control should only be used when loss of power is eminent and beyond the control of the host processor (for example, when the external power source has been disconnected or the battery has dropped below a minimum level). The longest lifetime of the DMD may not be achieved with the fast PARK operation. The longest lifetime is achieved with a normal PARK operation. Because of this, PARKZ is typically used in conjunction with a normal PARK request control input through PROJ_ON. The difference being that when the host sets PROJ_ON low, which connects to both DLPC150 and the DLPA200x PMIC chip, the DLPC150 takes much longer than 40 µs to park the mirrors. The DLPA200x holds on all power supplies, and keep RESETZ high, until the longer mirror parking has completed. This longer mirror parking time, of up to 20 ms, ensures the longest DMD lifetime and reliability. The DLPA2000 or DLPA2005 monitors power to the DLPC150 and detects an eminent power loss condition and drives the PARKZ signal accordingly. Connect to the interrupt output pin of the DLPA2000 or DLPA2005 PMIC.

(1) Refer to Table 1.

Pin Functions (continued)

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
PROJ_ON	G14	B_1	Normal mirror parking request (active low): To be driven by the PROJ_ON output of the host. A logic low on this signal will cause the DLPC150 to PARK the DMD, but it will not power down the DMD (the DLPA2000 or DLPA2005 controls the power down). The minimum high time is 200 ms. The minimum low time is also 200 ms.
HOST_IRQ(2)	N8	O_9	Host interrupt (output) This signal has two primary uses. The first use is to indicate when DLPC150 auto-initialization is in progress and most importantly when it completes. The second is to indicate when service is requested (that is an interrupt request). The DLPC150 tri-states this output during reset and requires an external pullup to drive this signal to its inactive state.
IIC0_SCL	N10	B_7	I^2C slave (port 0) SCL A bidirectional, open-drain signal with input hysteresis that requires an external pullup. The slave I^2C I/Os are 3.6-V tolerant (high-volt-input tolerant) and are powered by VCC_INTF (which can be 1.8, 2.5, or 3.3 V). External I^2C pullups must be connected to an equal or higher supply voltage, up to a maximum of 3.6 V (a lower pullup supply voltage would not likely satisfy the VIH specification of the slave I^2C input buffers).
IIC0_SDA	N9	B_7	I^2C slave (port 0) SDA. A bidirectional, open-drain signal with input hysteresis that requires an external pullup. The slave I^2C I/Os are 3.6-V tolerant (high-volt-input tolerant) and are powered by VCC_INTF (which can be 1.8, 2.5, or 3.3 V). External I^2C pullups must be connected to an equal or higher supply voltage, up to a maximum of 3.6 V (a lower pullup supply voltage would not likely satisfy the VIH specification of the slave I^2C input buffers).
PARALLEL PORT INPUT DATA AND CONTROL			
PCLK	P3	I_{11}	Pixel clock(3)
PDM_CVS_TE	N4	B_5	Parallel data mask(4)
VSYNC_WE	P1	I_{11}	Vsync(5)
HSYNC_CS	N5	I_{11}	Hsync(5)
DATAEN_CMD	P2	I_{11}	Data valid active high framing signal.(5) DLPC150 also offers a manual data framing mode through a software command. Refer to the DLPC150 Programmer's Guide for more information on the manual data framing command.
			(TYPICAL RGB 888)
PDATA_0 PDATA_1 PDATA_2 PDATA_3 PDATA_4 PDATA_5 PDATA_6 PDATA_7	K2 K1 L2 L1 M2 M1 N2 N1	I_{11}	Blue Blue Blue Blue Blue Blue Blue Blue
			(TYPICAL RGB 888)
PDATA_8 PDATA_9 PDATA_10 PDATA_11 PDATA_12 PDATA_13 PDATA_14 PDATA_15	R1 R2 R3 P4 R4 P5 R5 P6	I_{11}	Green Green Green Green Green Green Green Green

(2) For more information about usage, see *Host_irq Usage Model*.
(3) Pixel clock capture edge is software programmable.
(4) The parallel data mask signal input is optional for parallel interface operations. If unused, inputs should be grounded or pulled down to ground through an external resistor (8 kΩ or less).
(5) VSYNC, HSYNC, and DATAEN polarity is software programmable.

Pin Functions (continued)

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
			(TYPICAL RGB 888)
PDATA_16 PDATA_17 PDATA_18 PDATA_19 PDATA_20 PDATA_21 PDATA_22 PDATA_23	R6 P7 R7 P8 R8 P9 R9 P10	I_{11}	Red Red Red Red Red Red Red Red
DMD RESET AND BIAS CONTROL			
DMD_DEN_ARSTZ	B1	O_2	DMD driver enable (active high)/ DMD reset (active low). Assuming the corresponding I/O power is supplied, this signal will be driven low after the DMD is parked and before power is removed from the DMD. If the 1.8-V power to the DLPC150 is independent of the 1.8-V power to the DMD, then TI recommends a weak, external pulldown resistor to hold the signal low in the event DLPC150 power is inactive while DMD power is applied.
DMD_LS_CLK	A1	O_3	DMD, low speed interface clock
DMD_LS_WDATA	A2	O_3	DMD, low speed serial write data
DMD_LS_RDATA	B2	I_6	DMD, low speed serial read data
DMD SUB-LVDS INTERFACE			
DMD_HS_CLK_P DMD_HS_CLK_N	A7 B7	O_4	DMD high speed interface
DMD_HS_WDATA_H_P DMD_HS_WDATA_H_N DMD_HS_WDATA_G_P DMD_HS_WDATA_G_N DMD_HS_WDATA_F_P DMD_HS_WDATA_F_N DMD_HS_WDATA_E_P DMD_HS_WDATA_E_N DMD_HS_WDATA_D_P DMD_HS_WDATA_D_N DMD_HS_WDATA_C_P DMD_HS_WDATA_C_N DMD_HS_WDATA_B_P DMD_HS_WDATA_B_N DMD_HS_WDATA_A_P DMD_HS_WDATA_A_N	A3 B3 A4 B4 A5 B5 A6 B6 A8 B8 A9 B9 A10 B10 A11 B11	O_4	DMD high speed interface lanes, write data bits: (The true numbering and application of the DMD_HS_DATA pins are software configuration dependent)

Pin Functions (continued)

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
SERIAL FLASH MEMORY INTERFACE			
SPI0_CLK	A13	O_{13}	Synchronous serial port 0, clock output. Connect to clock input pin of the serial Flash memory device.
SPI0_CSZ0	A14	O_{13}	Synchronous serial port 0, chip select 0 output. Active low output. Connect to chip select pin of the serial Flash memory device. TI recommends an external pullup resistor to avoid floating inputs to the external SPI device during DLPC150 controller reset assertion.
SPI0_CSZ1	C12	O_{13}	Synchronous serial port 0, chip select 1 output. Active low output. Connect to chip select pin of a second serial Flash memory device. TI recommends an external pullup resistor to avoid floating inputs to the external SPI device during DLPC150 controller reset assertion.
SPI0_DIN	B12	I_{12}	Synchronous serial port 0, receive data input. Connect to the data output of the serial Flash memory device.
SPI0_DOUT	B13	O_{13}	Synchronous serial port 0, transmit data output. Connect to the data input of the serial Flash memory device.
DLPA2000 OR DLPA2005 PMIC INTERFACE			
PMIC_SPI_CLK	C15	B_1	Synchronous PMIC serial port, clock output. Connect to the clock input (SPI_CLK) of the DLPA2000 or DLPA2005 PMIC.
PMIC_SPI_CSZ	D15	B_1	Synchronous PMIC serial port, chip select output. Active low output. Connect to the chip select input (SPI_CSZ) of the DLPA2000 or DLPA2005 PMIC. TI recommends an external pullup resistor to avoid floating inputs to the external SPI device during DLPC150 controller reset assertion.
PMIC_SPI_DIN	C14	B_1	Synchronous PMIC serial port, receive data input. Connect to the data output (SPI_DOUT) of the DLPA2000 or DLPA2005 PMIC.
PMIC_SPI_DOUT	D14	B_1	Synchronous PMIC serial port, receive data output. Connect to the data input (SPI_DIN) of the DLPA2000 or DLPA2005 PMIC.
PMIC_CMP_IN	A12	I_6	Successive approximation ADC comparator input. Assumes a successive approximation ADC is implemented with a WPC light sensor and/or a thermistor feeding one input of an external comparator and the other side of the comparator is driven from the DLPC150 controller's CMP_PWM pin. Connect to the analog comparator output (CMP_OUT) of the DLPA2000 or DLPA2005 PMIC. If this function is not used, pulled-down to ground.
PMIC_CMP_PWM	A15	O_1	Successive approximation comparator pulse-duration modulation output. Supplies a PWM signal to drive the successive approximation ADC comparator used in WPC light-to-voltage sensor applications. Connect to the reference voltage input for analog comparator (PWM_IN) of the DLPA2000 or DLPA2005. If this function is not used, leave this pin unconnected.
PMIC_LED_SEL_0	B15	O_1	LED enable select. Controlled by programmable DMD sequence
LED_SEL(1:0)			Enabled LED Timing DLPA2000 or DLPA2005 application 00 = None 01 = Red 10 = Green 11 = Blue
PMIC_LED_SEL_1	B14	O_1	These signals will be driven low when RESETZ is asserted and the corresponding I/O power is supplied. They will continue to be driven low throughout the auto-initialization process. A weak, external pulldown resistor is still recommended to ensure that the LEDs are disabled when I/O power is not applied.
TRIGGER CONTROL			
TRIG_IN_1	N6	I_{11}	Input Trigger mode 1. Active high input signal that display the next pattern in the pattern sequence. Pull-down this signal with an external resistor.
TRIG_OUT_1	L14	B_1	Output Trigger mode 1. Active high output signal during pattern exposure
TRIG_OUT_2	E14	B_1	Output Trigger mode 2. Active high output signal that indicates the first pattern in a sequence.

Pin Functions (continued)

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
GPIO PERIPHERAL INTERFACE			
GPIO_19	M15	B_1	General purpose I/O 19 (hysteresis buffer). Options: 1. Optional GPIO. Should be configured as a logic zero GPIO output and left unconnected if not used (otherwise it will require an external pullup or pulldown to avoid a floating GPIO input). 2. KEYPAD_4 (input): keypad applications
GPIO_18	M14	B_1	General purpose I/O 18 (hysteresis buffer). Options: 1. Optional GPIO. Should be configured as a logic zero GPIO output and left unconnected if not used (otherwise it will require an external pullup or pulldown to avoid a floating GPIO input). 2. KEYPAD_3 (input): keypad applications
GPIO_17	L15	B_1	General purpose I/O 17 (hysteresis buffer). Options: 1. Optional GPIO. Configured as a logic zero GPIO output and left unconnected if not used.
GPIO_15	K15	B_1	General purpose I/O 15 (hysteresis buffer). Options: 1. Optional GPIO. Should be configured as a logic zero GPIO output and left unconnected if not used (otherwise it will require an external pullup or pulldown to avoid a floating GPIO input). 2. KEYPAD_0 (input): keypad applications
GPIO_14	K14	B_1	General purpose I/O 14 (hysteresis buffer). Option: 1. Optional GPIO. Should be configured as a logic zero GPIO output and left unconnected if not used (otherwise it will require an external pullup or pulldown to avoid a floating GPIO input).
GPIO_13	J15	B_1	General purpose I/O 13 (hysteresis buffer). Options: 1. CAL_PWR (output): Intended to feed the calibration control of the successive approximation ADC light sensor. 2. Optional GPIO. Should be configured as a logic zero GPIO output and left unconnected if not used (otherwise it will require an external pullup or pulldown to avoid a floating GPIO input).
GPIO_12	J14	B_1	General purpose I/O 12 (hysteresis buffer). Option: 1. Optional GPIO. Should be configured as a logic zero GPIO output and left unconnected if not used (otherwise it will require an external pullup or pulldown to avoid a floating GPIO input).
GPIO_11	H15	B_1	General purpose I/O 11 (hysteresis buffer). Options: 1. (Output): thermistor power enable. 2. Optional GPIO. Should be configured as a logic zero GPIO output and left unconnected if not used (otherwise it will require an external pullup or pulldown to avoid a floating GPIO input).
GPIO_10	H14	B_1	General Purpose I/O 10 (hysteresis buffer). Options: 1. RC_CHARGE (output): Intended to feed the RC charge circuit of the successive approximation ADC used to control the light sensor comparator. 2. Optional GPIO. Should be configured as a logic zero GPIO output and left unconnected if not used (otherwise it will require an external pullup or pulldown to avoid a floating GPIO input).
GPIO_09	G15	B_1	General purpose I/O 09 (hysteresis buffer). Options: 1. LS_PWR (active high output): Intended to feed the power control signal of the successive approximation ADC light sensor. 2. Optional GPIO. Should be configured as a logic zero GPIO output and left unconnected if not used (otherwise it will require an external pullup or pulldown to avoid a floating GPIO input).
GPIO_07	F15	B_1	General purpose I/O 07 (hysteresis buffer). Options: 1. (All) LED_ENABLE (active high input). This signal can be used as an optional shutdown interlock for the LED driver. Specifically, when so configured, setting LED_ENABLE = 0 (disabled), will cause LDEDRV_ON to be forced to 0 and LED_SEL(2:0) to be forced to b000. Otherwise when LED_ENABLE = 1 (enabled), the DLPC150 controller is free to control the LED SEL signals as it desires. There is however a 100-ms delay after LED_ENABLE transitions from low-to-high before the interlock is released. 2. (Output): LABB output sample and hold sensor control signal. 3. (All) GPIO (bidirectional): Optional GPIO. Should be configured as a logic zero GPIO output and left unconnected if not used (otherwise it will require an external pullup or pulldown to avoid a floating GPIO input).
GPIO_06	F14	B_1	General purpose I/O 06 (hysteresis buffer). Option: 1. Optional GPIO. Should be configured as a logic zero GPIO output and left unconnected if not used. An external pulldown resistor is required to deactivate this signal during reset and auto-initialization processes.

Pin Functions (continued)

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
GPIO_05	E15	B_1	General purpose I/O 05 (hysteresis buffer). Option: 1. Optional GPIO. Should be configured as a logic zero GPIO output and left unconnected if not used (otherwise it will require an external pullup or pulldown to avoid a floating GPIO input).
CLOCK AND PLL SUPPORT			
PLL_REFCLK_I	H1	I_{11}	Reference clock crystal input. If an external oscillator is used in place of a crystal, then this pin serves as the oscillator input.
PLL_REFCLK_O	J1	O_5	Reference clock crystal return. If an external oscillator is used in place of a crystal, then leave this pin unconnected with no capacitive load.
BOARD LEVEL TEST AND DEBUG			
HWTEST_EN	C10	I_6	Reserved Manufacturing test enable pin. For proper device operation, connect this signal directly to ground.
Reserved	P12	I_6	Reserved pin. For proper device operation, leave this pin unconnected.
Reserved	P13	I_6	Reserved pin. For proper device operation, leave this pin unconnected.
Reserved	N13(6)	O_1	Reserved pin. For proper device operation, leave this pin unconnected.
Reserved	N12(6)	O_1	Reserved pin. For proper device operation, leave this pin unconnected.
Reserved	R10	B_8	Reserved pin. For proper device operation, pull high to V_{cc18} with external pullup resistor.
Reserved	R11	B_8	Reserved pin. For proper device operation, pull high to V_{cc18} with external pullup resistor.
Reserved	M13	I_6	Reserved pin. For proper device operation, leave this pin unconnected.
Reserved	N11	I_6	Reserved pin. For proper device operation, leave this pin unconnected.
Reserved	P11	I_6	Reserved pin. For proper device operation, this pin must be tied to ground, through an external 8-kΩ, or less, resistor. Failure to tie this pin low will cause startup and initialization problems.
Reserved	E1		Reserved pin. For proper device operation, leave this pin unconnected.
Reserved	E2		Reserved pin. For proper device operation, leave this pin unconnected.
Reserved	F1		Reserved pin. For proper device operation, leave this pin unconnected.
Reserved	F2		Reserved pin. For proper device operation, leave this pin unconnected.
Reserved	F3		Reserved pin. For proper device operation, leave this pin unconnected.
Reserved	G1		Reserved pin. For proper device operation, leave this pin unconnected.
Reserved	G2		Reserved pin. For proper device operation, leave this pin unconnected.
Reserved	D1		Reserved pin. For proper device operation, leave this pin unconnected.
Reserved	D2		Reserved pin. For proper device operation, leave this pin unconnected.
Reserved	C1		Reserved pin. For proper device operation, leave this pin unconnected.
Reserved	C2		Reserved pin. For proper device operation, leave this pin unconnected.
TSTPT_0	R12	B_1	Reserved Test pin 0. For proper device operation, leave this pin unconnected (includes weak internal pulldown).Tri-stated while RESETZ is asserted low. Sampled as an input test mode selection control approximately 1.5 µs after de-assertion of RESETZ, and then driven as an output. Note: An external pullup should not be applied to this pin to avoid putting the DLPC150 in a test mode.
TSTPT_1	R13	B_1	Reserved Test pin 1. For proper device operation, leave this pin unconnected (includes weak internal pulldown). Tri-stated while RESETZ is asserted low. Sampled as an input test mode selection control approximately 1.5 µs after de-assertion of RESETZ and then driven as an output. Note: An external pullup should not be applied to this pin to avoid putting the DLPC150 in a test mode.
TSTPT_2	R14	B_1	Reserved Test pin 2. For proper device operation, leave this pin unconnected (includes weak internal pulldown). Tri-stated while RESETZ is asserted low. Sampled as an input test mode selection control approximately 1.5 µs after de-assertion of RESETZ and then driven as an output. Note: An external pullup should not be applied to this pin to avoid putting the DLPC150 in a test mode.

(6) If operation does not call for an external pullup and there is no external logic that might overcome the weak internal pulldown resistor, then this I/O can be left open or unconnected for normal operation. If operation does not call for an external pullup, but there is external logic that might overcome the weak internal pulldown resistor, then an external pulldown resistor is recommended to ensure a logic low.

Pin Functions (continued)

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
TSTPT_3	R15	B_1	Reserved Test pin 3. For proper device operation, leave this pin unconnected (includes weak internal pulldown).Tri-stated while RESETZ is asserted low. Sampled as an input test mode selection control approximately 1.5 µs after de-assertion of RESETZ and then driven as an output.
TSTPT_4	P14	B_1	Reserved Test pin 4. For proper device operation, leave this pin unconnected (includes weak internal pulldown).Tri-stated while RESETZ is asserted low. Sampled as an input test mode selection control approximately 1.5 µs after de-assertion of RESETZ and then driven as an output.
TSTPT_5	P15	B_1	Reserved Test pin 5. For proper device operation, leave this pin unconnected (includes weak internal pulldown). Tri-stated while RESETZ is asserted low. Sampled as an input test mode selection control approximately 1.5 µs after de-assertion of RESETZ and then driven as an output.
TSTPT_6	N14	B_1	Reserved Test pin 6. For proper device operation, leave this pin unconnected (includes weak internal pulldown). Tri-stated while RESETZ is asserted low. Sampled as an input test mode selection control approximately 1.5 µs after de-assertion of RESETZ and then driven as an output.
TSTPT_7	N15	B_1	Reserved Test pin 7. For proper device operation, leave this pin unconnected (includes weak internal pulldown). Tri-stated while RESETZ is asserted low. Sampled as an input test mode selection control approximately 1.5 µs after de-assertion of RESETZ and then driven as an output.
POWER AND GROUND			
VDD	C5, D5, D7, D12, J4, J12, K3, L4, L12, M6, M9, D9, D13, F13, H13, L13, M10, D3, E3	PWR	Core power 1.1 V (main 1.1 V)
VDDLP12	C3	PWR	Core power 1.1 V
VSS	C4, D6, D8, D10, E4, E13, F4, G4, G12, H4, H12, J3, J13, K4, K12, L3, M4, M5, M8, M12, G13, C6, C8, F6, F7, F8, F9, F10, G6, G7, G8, G9, G10, H6, H7, H8, H9, H10, J6, J7, J8, J9, J10, K6, K7, K8, K9, K10	GND	Core ground (eDRAM, I/O ground, thermal ground)

Pin Functions (continued)

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
VCC18	C7, C9, D4, E12, F12, K13, M11	PWR	All 1.8-V I/O power: (1.8-V power supply for all I/O other than the host or parallel interface and the SPI flash interface. This includes RESETZ, PARKZ LED_SEL, CMP, GPIO, IIC1, TSTPT, and JTAG pins)
VCC_INTF	M3, M7, N3, N7	PWR	Host or parallel interface I/O power: 1.8 to 3.3 V (Includes IIC0, PDATA, video syncs, and HOST_IRQ pins)
VCC_FLSH	D11	PWR	Flash interface I/O power:1.8 to 3.3 V (Dedicated SPI0 power pin)
VDD_PLLM	H2	PWR	MCG PLL 1.1-V power
VSS_PLLM	G3	RTN	MCG PLL return
VDD_PLLD	J2	PWR	DCG PLL 1.1-V power
VSS_PLLD	H3	RTN	DCG PLL return

5.1 DLPC150 Mechanical Data

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	DMD_LS_CLK	DMD_LS_WDATA	DMD_HS_WDATA_H_P	DMD_HS_WDATA_G_P	DMD_HS_WDATA_F_P	DMD_HS_WDATA_E_P	DMD_HS_CLK_P	DMD_HS_WDATA_D_P	DMD_HS_WDATA_C_P	DMD_HS_WDATA_B_P	DMD_HS_WDATA_A_P	PMIC_CMP_IN	SPI0_CLK	SPI0_CSZ0	PMIC_CMP_PWM
B	DMD_DEN_ARSTZ	DMD_LS_RDATA	DMD_HS_WDATA_H_N	DMD_HS_WDATA_G_N	DMD_HS_WDATA_F_N	DMD_HS_WDATA_E_N	DMD_HS_CLK_N	DMD_HS_WDATA_D_N	DMD_HS_WDATA_C_N	DMD_HS_WDATA_B_N	DMD_HS_WDATA_A_N	SPI0_DIN	SPI0_DOUT	PMIC_LED_SEL_1	PMIC_LED_SEL_0
C	Reserved	Reserved	VDDLP12	VSS	VDD	VSS	VCC18	VSS	VCC18	HWTEST_EN	RESETZ	SPI0_CSZ1	PARKZ	PMIC_SPI_DIN	PMIC_SPI_CLK
D	Reserved	Reserved	VDD	VCC18	VDD	VSS	VDD	VSS	VDD	VSS	VCC_FLSH	VDD	VDD	PMIC_SPI_DOUT	PMIC_SPI_CSZ
E	Reserved	Reserved	VDD	VSS								VCC18	VSS	TRIG_OUT_2	GPIO_05
F	Reserved	Reserved	Reserved	VSS		VSS	VSS	VSS	VSS	VSS		VCC18	VDD	GPIO_06	GPIO_07
G	Reserved	Reserved	VSS_PLLM	VSS		VSS	VSS	VSS	VSS	VSS		VSS	VSS	PROJ_ON	GPIO_09
H	PLL_REFCLK_I	VDD_PLLM	VSS_PLLD	VSS		VSS	VSS	VSS	VSS	VSS		VSS	VDD	GPIO_10	GPIO_11
J	PLL_REFCLK_O	VDD_PLLD	VSS	VDD		VSS	VSS	VSS	VSS	VSS		VDD	VSS	GPIO_12	GPIO_13
K	PDATA_1	PDATA_0	VDD	VSS		VSS	VSS	VSS	VSS	VSS		VSS	VCC18	GPIO_14	GPIO_15
L	PDATA_3	PDATA_2	VSS	VDD								VDD	VDD	GPIO_16	GPIO_17
M	PDATA_5	PDATA_4	VCC_INTF	VSS	VSS	VDD	VCC_INTF	VSS	VDD	VDD	VCC18	VSS	Reserved	TRIG_OUT_1	GPIO_19
N	PDATA_7	PDATA_6	VCC_INTF	PDM_CVS_TE	HSYNC_CS	TRIG_IN_1	VCC_INTF	HOST_IRQ	IIC0_SDA	IIC0_SCL	Reserved	Reserved	Reserved	TSTPT_6	TSTPT_7
P	VSYNC_WE	DATEN_CMD	PCLK	PDATA_11	PDATA_13	PDATA_15	PDATA_17	PDATA_19	PDATA_21	PDATA_23	Reserved	Reserved	Reserved	TSTPT_4	TSTPT_5
R	PDATA_8	PDATA_9	PDATA_10	PDATA_12	PDATA_14	PDATA_16	PDATA_18	PDATA_20	PDATA_22	Reserved	Reserved	TSTPT_0	TSTPT_1	TSTPT_2	TSTPT_3

Figure 1. 13- × 13-mm Package – VF Ball Grid Array

DLPC150 Mechanical Data (continued)

Table 1. I/O Type Subscript Definition

I/O TYPE		SUPPLY REFERENCE	ESD STRUCTURE
SUBSCRIPT	DESCRIPTION		
1	1.8 LVCMOS I/O buffer with 8-mA drive	V_{cc18}	ESD diode to GND and supply rail
2	1.8 LVCMOS I/O buffer with 4-mA drive	V_{cc18}	ESD diode to GND and supply rail
3	1.8 LVCMOS I/O buffer with 24-mA drive	V_{cc18}	ESD diode to GND and supply rail
4	1.8 sub-LVDS output with 4-mA drive	V_{cc18}	ESD diode to GND and supply rail
5	1.8, 2.5, 3.3 LVCMOS with 4-mA drive	V_{cc_INTF}	ESD diode to GND and supply rail
6	1.8 LVCMOS input	V_{cc18}	ESD diode to GND and supply rail
7	1.8-, 2.5-, 3.3-V I^2C with 3-mA drive	V_{cc_INTF}	ESD diode to GND and supply rail
8	1.8-V I^2C with 3-mA drive	V_{cc18}	ESD diode to GND and supply rail
9	1.8-, 2.5-, 3.3-V LVCMOS with 8-mA drive	V_{cc_INTF}	ESD diode to GND and supply rail
11	1.8, 2.5, 3.3 LVCMOS input	V_{cc_INTF}	ESD diode to GND and supply rail
12	1.8-, 2.5-, 3.3-V LVCMOS input	V_{cc_FLSH}	ESD diode to GND and supply rail
13	1.8-, 2.5-, 3.3-V LVCMOS with 8-mA drive	V_{cc_FLSH}	ESD diode to GND and supply rail

Table 2. Internal Pullup and Pulldown Characteristics(1)(2)

INTERNAL PULLUP AND PULLDOWN RESISTOR CHARACTERISTICS	V_{CCIO}	MIN	MAX	UNIT
Weak pullup resistance	3.3 V	29	63	kΩ
	2.5 V	38	90	kΩ
	1.8 V	56	148	kΩ
Weak pulldown resistance	3.3 V	30	72	kΩ
	2.5 V	36	101	kΩ
	1.8 V	52	167	kΩ

(1) The resistance is dependent on the supply voltage level applied to the I/O.
(2) An external 8-kΩ pullup or pulldown (if needed) would work for any voltage condition to correctly pull enough to override any associated internal pullups or pulldowns.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) (see (1))

		MIN	MAX	UNIT
SUPPLY VOLTAGE(2)(3)				
$V_{(VDD)}$ (core)		–0.3	1.21	V
$V_{(VDDLP12)}$ (core)		–0.3	1.32	V
Power + sub-LVDS		–0.3	1.96	V
$V_{(VCC\_INTF)}$	Host I/O power	–0.3	3.60	V
	If 1.8-V power used	–0.3	1.99	
	If 2.5-V power used	–0.3	2.75	
	If 3.3-V power used	–0.3	3.60	
$V_{(VCC\_FLSH)}$	Flash I/O power	–0.3	3.60	V
	If 1.8-V power used	–0.3	1.96	
	If 2.5-V power used	–0.3	2.72	
	If 3.3-V power used	–0.3	3.58	
$V_{(VDD\_PLLM)}$ (MCG PLL)		–0.3	1.21	V
$V_{(VDD\_PLLD)}$ (DCG PLL)		–0.3	1.21	V
GENERAL				
T_J	Operating junction temperature	–30	125	°C
T_{stg}	Storage temperature	–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) Overlap currents, if allowed to continue flowing unchecked, not only increase total power dissipation in a circuit, but degrade the circuit reliability, thus shortening its usual operating life.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(1)	±500	

(1) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$V_{(VDD)}$	Core power 1.1 V (main 1.1 V)	±5% tolerance	1.045	1.1	1.155	V
$V_{(VDDLP12)}$	Core power 1.1 V	±5% tolerance See (1)	1.02	1.1	1.18	V
			1.12	1.2	1.28	
$V_{(VCC18)}$	All 1.8-V I/O power: (1.8-V power supply for all I/O other than the host or parallel interface and the SPI flash interface. This includes RESETZ, PARKZ, LED_SEL, CMP, GPIO, TSTPT, and Reserved pins.)	±8.5% tolerance	1.64	1.8	1.96	V
$V_{(VCC\_INTF)}$	Host or parallel interface I/O power: 1.8 to 3.3 V (includes IIC0, PDATA, video syncs, and HOST_IRQ pins)	±8.5% tolerance See (1)	1.64	1.8	1.96	V
			2.28	2.5	2.72	
			3.02	3.3	3.58	
$V_{(VCC\_FLSH)}$	Flash interface I/O power:1.8 to 3.3 V	±8.5% tolerance See (1)	1.64	1.8	1.96	V
			2.28	2.5	2.72	
			3.02	3.3	3.58	
$V_{(VDD\_PLLM)}$	MCG PLL 1.1-V power	±9.1% tolerance See (2)	1.025	1.1	1.155	V
$V_{(VDD\_PLLD)}$	DCG PLL 1.1-V power	±9.1% tolerance See (2)	1.025	1.1	1.155	V
T_A	Operating ambient temperature range(3)		–30		85	°C

(1) These supplies have multiple valid ranges.
(2) These I/O supply ranges are wider to facilitate additional filtering.
(3) The operating ambient temperature range assumes 0 forced air flow, a JEDEC JESD51 junction-to-ambient thermal resistance value at 0 forced air flow ($R_{\theta JA}$ at 0 m/s), a JEDEC JESD51 standard test card and environment, along with min and max estimated power dissipation across process, voltage, and temperature. Thermal conditions vary by application, which will impact $R_{\theta JA}$. Thus, maximum operating ambient temperature varies by application.
(a) $T_{a\_min} = T_{j\_min} – (P_{d\_min} \times R_{\theta JA}) = –30°C – (0.0W \times 30.3°C/W) = –30°C$
(b) $T_{a\_max} = T_{j\_max} – (P_{d\_max} \times R_{\theta JA}) = +105°C – (0.348W \times 30.3°C/W) = +94.4°C$

6.4 Thermal Information

THERMAL METRIC(1)			DLPC150 ZEZ (VFBGA) 176 PINS	DLPC150 ZEZ (VFBGA) 201 PINS	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance		11.2	10.1	°C/W
$R_{\theta JA}$	Junction-to-air thermal resistance	at 0 m/s of forced airflow(2)	30.3	28.8	°C/W
		at 1 m/s of forced airflow(2)	27.4	25.3	
		at 2 m/s of forced airflow(2)	26.6	24.4	
ψ_{JT}(3)	Temperature variance from junction to package top center temperature, per unit power dissipation		.27	.23	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).
(2) Thermal coefficients abide by JEDEC Standard 51. $R_{\theta JA}$ is the thermal resistance of the package as measured using a JEDEC defined standard test PCB. This JEDEC test PCB is not necessarily representative of the DLPC150 PCB and thus the reported thermal resistance may not be accurate in the actual product application. Although the actual thermal resistance may be different , it is the best information available during the design phase to estimate thermal performance.
(3) Example: (0.5 W) × (0.2 C/W) ≈ 1.00°C temperature rise.

6.5 Electrical Characteristics Over Recommended Operating Conditions

(see (1)(2)(3)(4)(5)(6))

PARAMETER		TEST CONDITIONS(7)	MIN	TYP(8)	MAX(9)	UNIT
I_{CC11}	Supply voltage, 1.1-V Main core power	IDLE disabled, WVGA, 60 Hz		112	232.2	mA
		IDLE enabled, WVGA, 60 Hz		85		
I_{CC_PLLM}	Supply voltage, 1.1-V MCG PLL power	IDLE disabled, WVGA, 60 Hz		112		mA
		IDLE enabled, WVGA, 60 Hz		85		
I_{CC_PLLD}	Supply voltage, 1.1-V DCG PLL power	IDLE disabled, WVGA, 60 Hz		112		mA
		IDLE enabled, WVGA, 60 Hz		85		
I_{CC18}	Supply voltage, 1.8-V I/O power: (1.8-V power supply for all I/O other than the host or parallel interface and the SPI flash interface. This includes sub-LVDS DMD I/O, RESETZ, PARKZ LED_SEL, CMP, GPIO, IIC1, TSTPT, and JTAG pins)	IDLE disabled, WVGA, 60 Hz		13		mA
		IDLE enabled, WVGA, 60 Hz		13		
I_{CC_INTF}	Supply voltage, 1.8-V Host or parallel interface I/O power: (includes IIC0, PDATA, video syncs, and HOST_IRQ pins)	IDLE disabled, WVGA, 60 Hz, V_{VCC_INTF} = 1.8V			1.5	mA
I_{CC_FLSH}	Supply voltage, 1.8-V Flash interface I/O power	IDLE disabled, WVGA, 60 Hz, V_{VCC_FLSH} = 1.8V			1.01	mA

(1) Assumes 12.5% activity factor, 30% clock gating on appropriate domains, and mixed SVT or HVT cells.
(2) Programmable host and flash I/O are at minimum voltage (that is 1.8 V) for this typical scenario.
(3) Max currents column use typical motion video as the input. The typical currents column uses SMPTE color bars as the input.
(4) Some applications (that is, high-resolution 3D) may be forced to use 1-oz copper to manage DLPC150 controller package heat.
(5) For the typical cases, all pins using 1.8 V are tied together as are 1.1-V pins, and the current specified is for the collective 1.8-V and 1.1-V current.
(6) Input image is 854 × 480 (WVGA) 24-bits on the parallel interface at the frame rate shown with DLP2010 or DLP2010NIR.
(7) In normal mode.
(8) Assumes typical case power PVT condition = nominal process, typical voltage, typical temperature (55°C junction). WVGA resolution.
(9) Assumes worse case power PVT condition = corner process, high voltage, high temperature (105°C junction), WVGA resolution .

6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted) (see (1)(2))

PARAMETER(3)			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input threshold voltage	I^2C buffer (I/O type 7)		0.7 × VCC_INTF		(1)	V
		1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)		1.17		3.6	
		1.8-V LVTTL (I/O type 1, 6) identified below: (2) CMP_OUT; PARKZ; RESETZ; GPIO[19:05]; TRIG_OUT_1; TRIG_OUT_2		1.3		3.6	
		2.5-V LVTTL (I/O type 5, 9, 11, 12, 13)		1.7		3.6	
		3.3-V LVTTL (I/O type 5, 9, 11, 12, 13)		2		3.6	
V_{IL}	Low-level input threshold voltage	I^2C buffer (I/O type 7)		–0.5		0.3 × VCC_INTF	V
		1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)		–0.3		0.63	
		1.8-V LVTTL (I/O type 1, 6) identified below: (2) CMP_OUT; PARKZ; RESETZ; GPIO[19:05]; TRIG_OUT_1; TRIG_OUT_2		–0.3		0.5	
		2.5-V LVTTL (I/O type 5, 9, 11, 12, 13)		–0.3		0.7	
		3.3-V LVTTL (I/O type 5, 9, 11, 12, 13)		–0.3		0.8	
V_{CM}	Steady-state common mode voltage	1.8 sub-LVDS (DMD high speed) (I/O type 4)		800	900	1000	mV
$\lvert V_{OD} \rvert$	Differential output magnitude	1.8 sub-LVDS (DMD high speed) (I/O type 4)			200		mV
V_{OH}	High-level output voltage	1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)		1.35			V
		2.5-V LVTTL (I/O type 5, 9, 11, 12, 13)		1.7			
		3.3-V LVTTL (I/O type 5, 9, 11, 12, 13)		2.4			
		1.8 sub-LVDS – DMD high speed (I/O type 4)			1		
V_{OL}	Low-level output voltage	I^2C buffer (I/O type 7)	VCC_INTF > 2 V			0.4	V
		I^2C buffer (I/O type 7)	VCC_INTF < 2 V			0.2 × VCC_INTF	
		1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)				0.45	
		2.5 V LVTTL (I/O type 5, 9, 11, 12, 13)				0.7	
		3.3 V LVTTL (I/O type 5, 9, 11, 12, 13)				0.4	
		1.8 sub-LVDS – DMD high speed (I/O type 4)			0.8		

(1) I/O is high voltage tolerant; that is, if VCC = 1.8 V, the input is 3.3-V tolerant, and if VCC = 3.3 V, the input is 5-V tolerant.
(2) DLPC150 controller pins: CMP_OUT; PARKZ; RESETZ; GPIO[19:05]; TRIG_OUT_1; TRIG_OUT_2 have slightly varied V_{IH} and V_{IL} range from other 1.8-V I/O.
(3) The number inside each parenthesis for the I/O refers to the type defined in Table 1.

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted) (see [1][2])

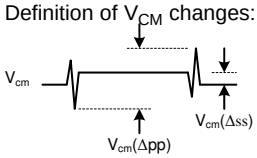
PARAMETER[3]			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OH}	High-level output current	1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)	4 mA	2			mA
		1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)	8 mA	3.5			
		1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)	24 mA	10.6			
		2.5-V LVTTL (I/O type 5)	4 mA	5.4			
		2.5-V LVTTL (I/O type 9, 13)	8 mA	10.8			
		2.5-V LVTTL (I/O type 5, 9, 11, 12, 13)	24 mA	28.7			
		3.3-V LVTTL (I/O type 5)	4 mA	7.8			
		3.3-V LVTTL (I/O type 9, 13)	8 mA	15			
I_{OL}	Low-level output current	I^2C buffer (I/O type 7)		3			mA
		1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)	4 mA	2.3			
		1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)	8 mA	4.6			
		1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)	24 mA	13.9			
		2.5-V LVTTL (I/O type 5)	4 mA	5.2			
		2.5-V LVTTL (I/O type 9, 13)	8 mA	10.4			
		2.5-V LVTTL (I/O type 5, 9, 11, 12, 13)	24 mA	31.1			
		3.3-V LVTTL (I/O type 5)	4 mA	4.4			
		3.3-V LVTTL (I/O type 9, 13)	8 mA	8.9			
I_{OZ}	High-impedance leakage current	I^2C buffer (I/O type 7)	0.1 × VCC_INTF < VI < 0.9 × VCC_INTF	–10		10	µA
		1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)		–10		10	
		2.5-V LVTTL (I/O type 5, 9, 11, 12, 13)		–10		10	
		3.3-V LVTTL (I/O type 5, 9, 11, 12, 13)		–10		10	
C_I	Input capacitance (including package)	I^2C buffer (I/O type 7)				5	pF
		1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)		2.6		3.5	
		2.5-V LVTTL (I/O type 5, 9, 11, 12, 13)		2.6		3.5	
		3.3-V LVTTL (I/O type 5, 9, 11, 12, 13)		2.6		3.5	
		1.8 sub-LVDS – DMD high speed (I/O type 4)				3	

6.7 High-Speed Sub-LVDS Electrical Characteristics

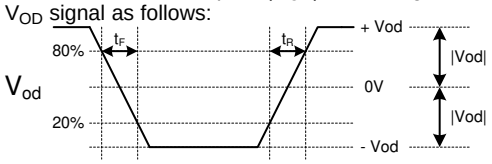
over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
V_{CM}	Steady-state common mode voltage	0.8	0.9	1	V
V_{CM} (Δpp)(1)	V_{CM} change peak-to-peak (during switching)			75	mV
V_{CM} (Δss)(1)	V_{CM} change steady state	–10		10	mV
$\|V_{OD}\|$(2)	Differential output voltage magnitude		200		mV
V_{OD} (Δ)	V_{OD} change (between logic states)	–10		10	mV
V_{OH}	Single-ended output voltage high		1		V
V_{OL}	Single-ended output voltage low		0.8		V
t_R(2)	Differential output rise time			250	ps
t_F(2)	Differential output fall time			250	ps
t_{MAX}	Max switching rate			1064	Mbps
DCout	Output duty cycle	45%	50%	55%	
Tx_{term}(1)	Internal differential termination	80	100	120	Ω
Tx_{load}	100-Ω differential PCB trace (50-Ω transmission lines)	0.5		6	inches

(1) Definition of V_{CM} changes:



(2) Note that V_{OD} is the differential voltage swing measured across a 100-Ω termination resistance connected directly between the transmitter differential pins. $|V_{OD}|$ is the magnitude of this voltage swing relative to 0. Rise and fall times are defined for the differential V_{OD} signal as follows:



Differential Output Signal
(Note Vcm is removed when the signals are viewed differentially)

6.8 Low-Speed SDR Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	ID	TEST CONDITIONS	MIN	MAX	UNIT
Operating voltage	VCC18 (all signal groups)		1.64	1.96	V
DC input high voltage	VIHD(DC) Signal group 1	All	0.7 × VCC18	VCC18 + 0.5	V
DC input low voltage (1)	VILD(DC) Signal group 1	All	–0.5	0.3 × VCC18	V
AC input high voltage (2)	VIHD(AC) Signal group 1	All	0.8 × VCC18	VCC18 + 0.5	V
AC input low voltage	VILD(AC) Signal group 1	All	–0.5	0.2 × VCC18	V
Slew rate (3)(4)(5)(6)	Signal group 1		1	3	V/ns
	Signal group 2		0.25		
	Signal group 3		0.5		

(1) VILD(AC) min applies to undershoot.
(2) VIHD(AC) max applies to overshoot.
(3) Signal group 1 output slew rate for rising edge is measured between VILD(DC) to VIHD(AC).
(4) Signal group 1 output slew rate for falling edge is measured between VIHD(DC) to VILD(AC).
(5) Signal group 1: See Figure 2.
(6) Signal groups 2 and 3 output slew rate for rising edge is measured between VILD(AC) to VIHD(AC).

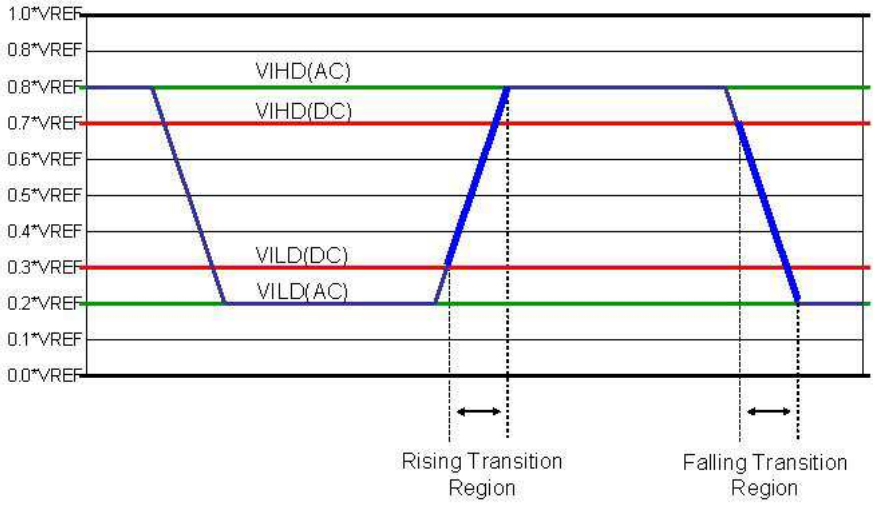


Figure 2. Low Speed (Ls) I/O Input Thresholds

6.9 System Oscillators Timing Requirements(1)

NUMBER				MIN	MAX	UNIT
1a	f_{clock}	Clock frequency, MOSC(2)	Option 1: 24-MHz oscillator	23.998	24.002	MHz
1a	t_c	Cycle time, MOSC(2)	Option 1: 24-MHz oscillator	41.67	41.663	ns
1b	f_{clock}	Clock frequency, MOSC(2)	Option 2: 16-MHz oscillator	15.998	16.002	MHz
1b	t_c	Cycle time, MOSC(2)	Option 2: 16-MHz oscillator	62.508	62.492	ns
2	$t_{w(H)}$	Pulse duration(3), MOSC, high	50% to 50% reference points (signal)		40 t_c%	
3	$t_{w(L)}$	Pulse duration(3), MOSC, low	50% to 50% reference points (signal)		40 t_c%	
4	t_t	Transition time(3), MOSC, $t_t = t_f / t_r$	20% to 80% reference points (signal)		10	ns
5	t_{jp}	Long-term, peak-to-peak, period jitter(3), MOSC (that is the deviation in period from ideal period due solely to high frequency jitter)			2%	

(1) The I/O pin TSTPT_6 enables the DLPC150 controller to use two different oscillator frequencies through a pullup control at initial DLPC150 controller power-up. If a pullup is applied to this pin then a 16.0-MHz oscillator option must be used instead of the 24-MHz option shown.
(2) The frequency accuracy for MOSC is ±200 PPM. (This includes impact to accuracy due to aging, temperature, and trim sensitivity.) The MOSC input cannot support spread spectrum clock spreading.
(3) Applies only when driven through an external digital oscillator.

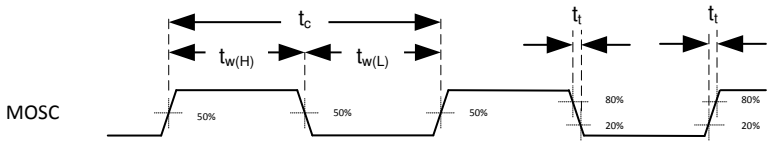


Figure 3. System Oscillators

6.10 Power-Up and Reset Timing Requirements

NUMBER				MIN	MAX	UNIT
1	$t_{w(L)}$	Pulse duration, inactive low, RESETZ	50% to 50% reference points (signal)	1.25		µs
2	t_t	Transition time, RESETZ(1), $t_t = t_f / t_r$	20% to 80% reference points (signal)		0.5	µs

(1) For more information on RESETZ, see *Pin Configuration and Functions*.

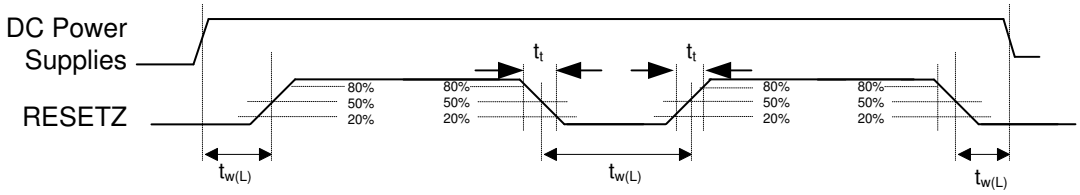


Figure 4. Power-Up and Power-Down RESETZ Timing

6.11 Parallel Interface Frame Timing Requirements

			MIN	MAX	UNIT
t_{p_vsw}	Pulse duration – VSYNC_WE high	50% reference points	1		lines
t_{p_vbp}	Vertical back porch (VBP) – time from the leading edge of VSYNC_WE to the leading edge HSYNC_CS for the first active line (see (1))	50% reference points	2		lines
t_{p_vfp}	Vertical front porch (VFP) – time from the leading edge of the HSYNC_CS following the last active line in a frame to the leading edge of VSYNC_WE (see (1))	50% reference points	1		lines
t_{p_tvb}	Total vertical blanking – time from the leading edge of HSYNC_CS following the last active line of one frame to the leading edge of HSYNC_CS for the first active line in the next frame. (This is equal to the sum of VBP (t_{p_vbp}) + VFP (t_{p_vfp}).)	50% reference points	See (1)		lines
t_{p_hsw}	Pulse duration – HSYNC_CS high	50% reference points	4	128	PCLKs
t_{p_hbp}	Horizontal back porch – time from rising edge of HSYNC_CS to rising edge of DATAEN_CMD	50% reference points	4		PCLKs
t_{p_hfp}	Horizontal front porch – time from falling edge of DATAEN_CMD to rising edge of HSYNC_CS	50% reference points	8		PCLKs
t_{p_thb}	Total horizontal blanking – sum of horizontal front and back porches	50% reference points	See (2)		PCLKs

(1) The minimum total vertical blanking is defined by the following equation: $t_{p\_tvb}(min) = 6 + [6 \times Max(1, Source\_ALPF/ DMD\_ALPF)]$ lines
where:
(a) SOURCE_ALPF = Input source active lines per frame
(b) DMD_ALPF = Actual DMD used lines per frame supported

(2) Total horizontal blanking is driven by the max line rate for a given source which will be a function of resolution and orientation. The following equation can be applied for this: $t_{p\_thb} = Roundup[(1000 \times f_{clock})/ LR] – APPL$
where:
(a) f_{clock} = Pixel clock rate in MHz
(b) LR = Line rate in kHz
(c) APPL is the number of active pixels per (horizontal) line.
(d) If t_{p_thb} is calculated to be less than $t_{p\_hbp} + t_{p\_hfp}$ then the pixel clock rate is too low or the line rate is too high, and one or both must be adjusted.

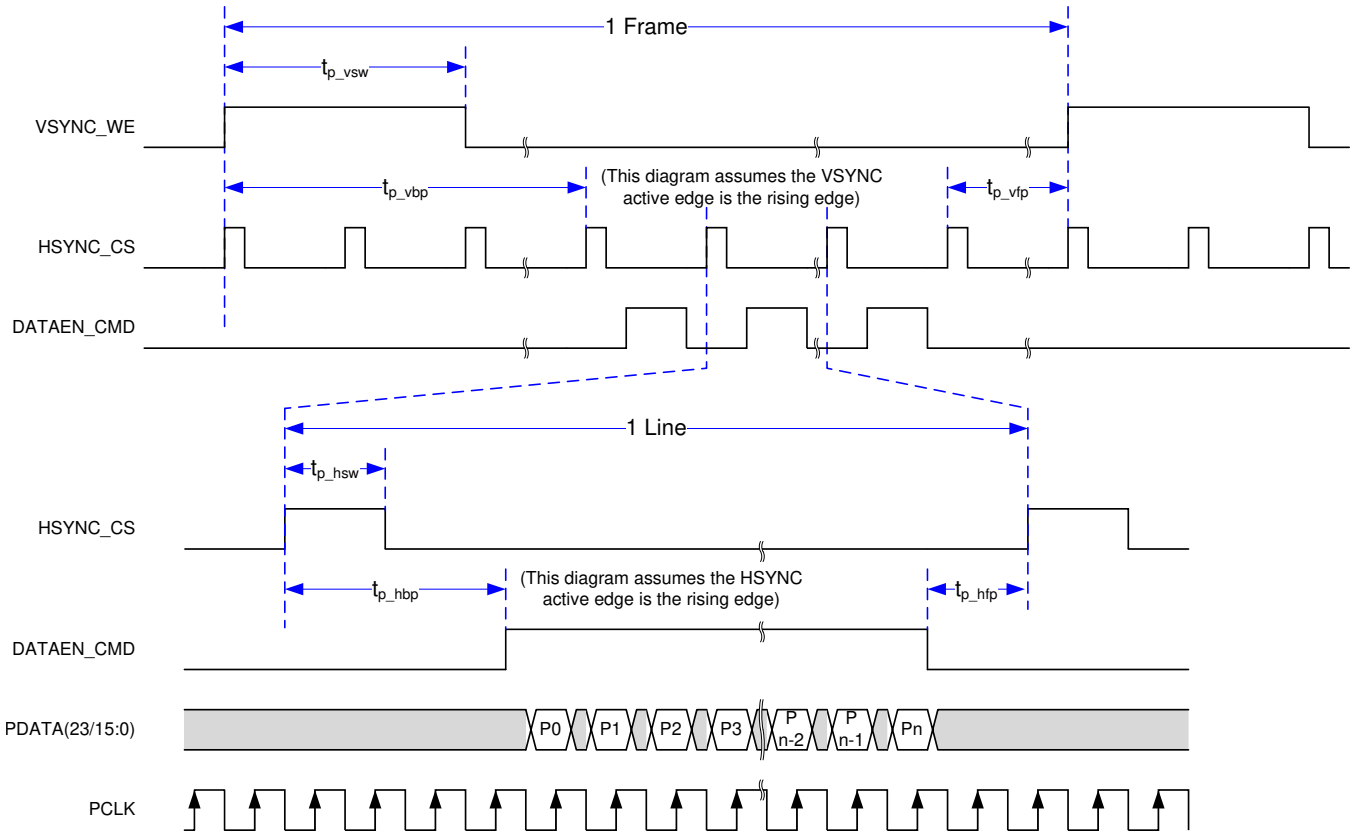


Figure 5. Parallel Interface Frame Timing

6.12 Parallel Interface General Timing Requirements(1)

			MIN	MAX	UNIT
f_{clock}	Clock frequency, PCLK		1	75	MHz
t_{p_clkper}	Clock period, PCLK	50% reference points	6.66	1000	ns
t_{p_clkjit}	Clock jitter, PCLK	Max f_{clock}	see (2)	see (2)	
t_{p_wh}	Pulse duration low, PCLK	50% reference points	2.43		ns
t_{p_wl}	Pulse duration high, PCLK	50% reference points	2.43		ns
t_{p_su}	Setup time – HSYNC_CS, DATEN_CMD, PDATA(23:0) valid before the active edge of PCLK	50% reference points	0.9		ns
t_{p_h}	Hold time – HSYNC_CS, DATEN_CMD, PDATA(23:0) valid after the active edge of PCLK	50% reference points	0.9		ns
t_t	Transition time – all signals	20% to 80% reference points	0.2	2	ns

(1) The active (capture) edge of PCLK for HSYNC_CS, DATEN_CMD and PDATA(23:0) is software programmable, but defaults to the rising edge.
(2) Clock jitter (in ns) should be calculated using this formula: Jitter = [1 / f_{clock} – 5.76 ns]. Setup and hold times must be met during clock jitter.

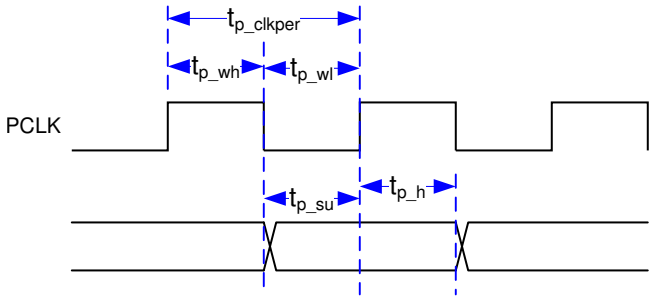


Figure 6. Parallel Interface General Timing

6.13 Flash Interface Timing Requirements

The DLPC150 controller flash memory interface consists of a SPI flash serial interface with a programmable clock rate. The DLPC150 controller can support 1- to 16-Mb flash memories. (see (1)(2))

			MIN	MAX	UNIT
f_{clock}	Clock frequency, SPI_CLK	See (3)	1.42	36	MHz
t_{p_clkper}	Clock period, SPI_CLK	50% reference points	704	27.7	ns
t_{p_wh}	Pulse duration low, SPI_CLK	50% reference points	352		ns
t_{p_wl}	Pulse duration high, SPI_CLK	50% reference points	352		ns
t_t	Transition time – all signals	20% to 80% reference points	0.2	3	ns
t_{p_su}	Setup time – SPI_DIN valid before SPI_CLK falling edge	50% reference points	10		ns
t_{p_h}	Hold time – SPI_DIN valid after SPI_CLK falling edge	50% reference points	0		ns
t_{p_clqv}	SPI_CLK clock falling edge to output valid time – SPI_DOUT and SPI_CSZ	50% reference points		1	ns
t_{p_clqx}	SPI_CLK clock falling edge output hold time – SPI_DOUT and SPI_CSZ	50% reference points	–3	3	ns

(1) Standard SPI protocol is to transmit data on the falling edge of SPI_CLK and capture data on the rising edge. The DLPC150 controller does transmit data on the falling edge, but it also captures data on the falling edge rather than the rising edge. This provides support for SPI devices with long clock-to-Q timing. DLPC150 controller hold capture timing has been set to facilitate reliable operation with standard external SPI protocol devices.
(2) With the above output timing, the DLPC150 controller provides the external SPI device 8.2-ns input set-up and 8.2-ns input hold, relative to the rising edge of SPI_CLK.
(3) This range include the 200 ppm of the external oscillator (but no jitter).

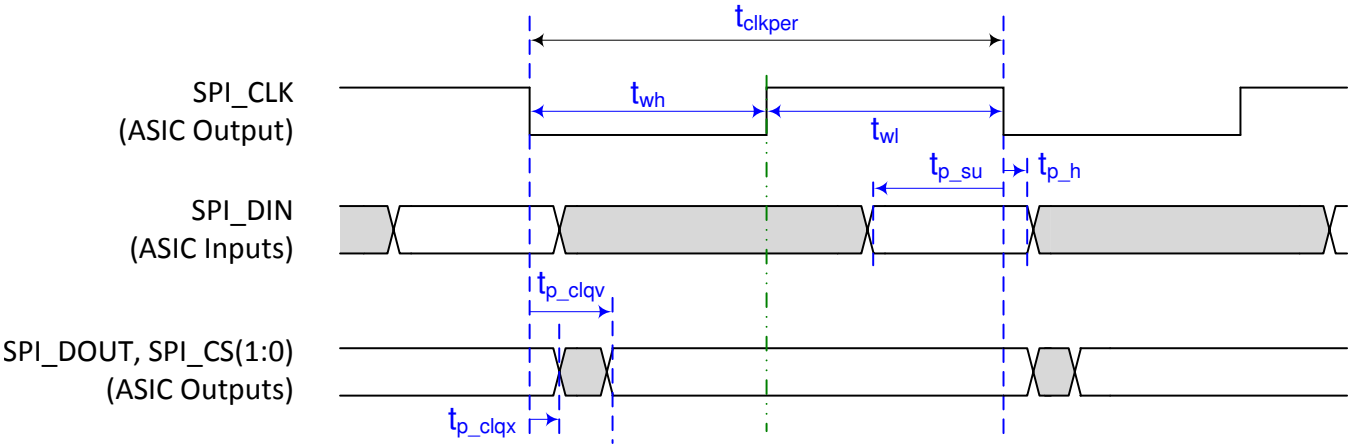


Figure 7. Flash Interface Timing

7 Parameter Measurement Information

7.1 Host_irq Usage Model

- While reset is applied, HOST_IRQ will reset to tri-state (an external pullup pulls the line high).
- HOST_IRQ will remain tri-state (pulled high externally) until the microprocessor boot completes. While the signal is pulled high, this indicates that the DLPC150 controller is performing boot-up and auto-initialization.
- As soon as possible after boot-up, the microprocessor will drive HOST_IRQ to a logic high state to indicate that the DLPC150 controller is continuing to perform auto-initialization (no real state change occurs on the external signal).
- Upon completion of auto-initialization, software will set HOST_IRQ to a logic low state to indicate the completion of auto-initialization. At the falling edge, the system is said to enter the INIT_DONE state.
- After auto-initialization completes, HOST_IRQ is used to generate a logic high interrupt pulse to the host through software control. This interrupt indicates that the DLPC150 controller has detected an error condition or otherwise requires service.

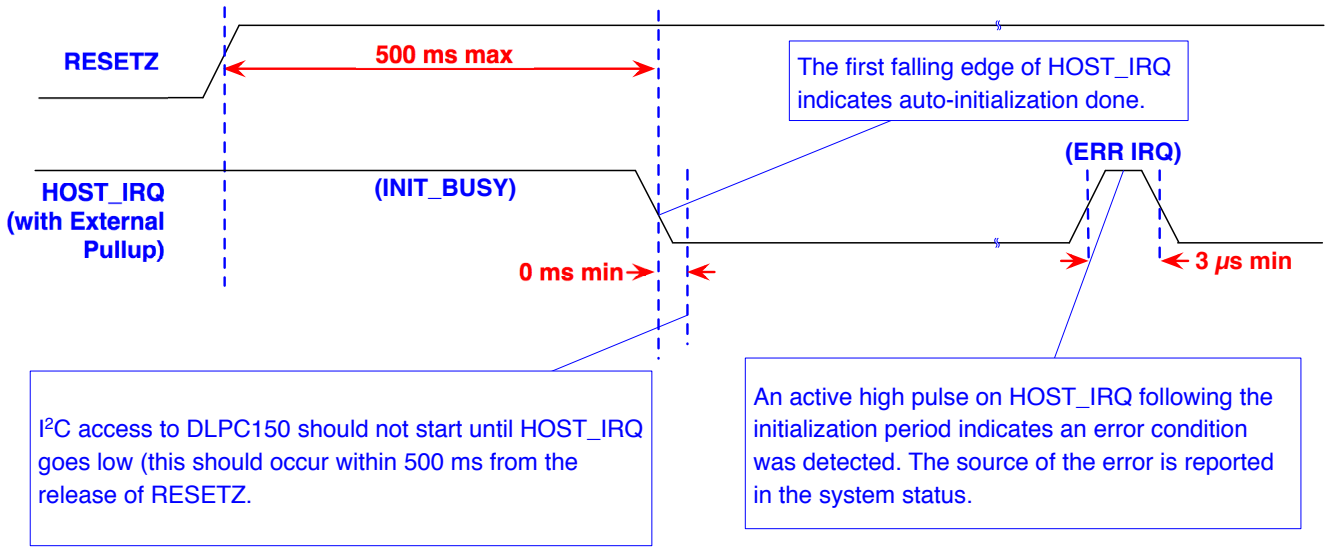


Figure 8. Host Irq Timing

7.2 Input Source

Table 3. Supported Input Source Ranges(1)(2)(3)(4)

INTERFACE	BITS / PIXEL (5)	SOURCE RESOLUTION RANGE		FRAME RATE RANGE
		HORIZONTAL	VERTICAL	
Parallel	16 or 24-bit	320 to 1280	200 to 800	47 to 63 Hz
SPI Flash	16-bit	320 to 1280	200 to 800	60 Hz

(1) The user must stay within specifications for all source interface parameters such as max clock rate and max line rate.
(2) The max DMD size for all rows in the table is 854 × 480.
(3) To achieve the ranges stated, the composer-created firmware used must be defined to support the source parameters used.
(4) These interfaces are supported with the DMD sequencer sync mode command (3Bh) set to auto.
(5) Bits / Pixel does not necessarily equal the number of data pins used on the DLPC150 controller. Fewer pins are used if multiple clocks are used per pixel transfer.

7.2.1 Parallel Interface Supports Two Data Transfer Formats

- 24-bit RGB888 on a 24 data wire interface
- 16-bit RGB565 on a 16 data wire interface

Pdata Bus – Parallel Interface Bit Mapping Modes shows the required PDATA(23:0) bus mapping for these two data transfer formats.

7.2.1.1 Pdata Bus – Parallel Interface Bit Mapping Modes

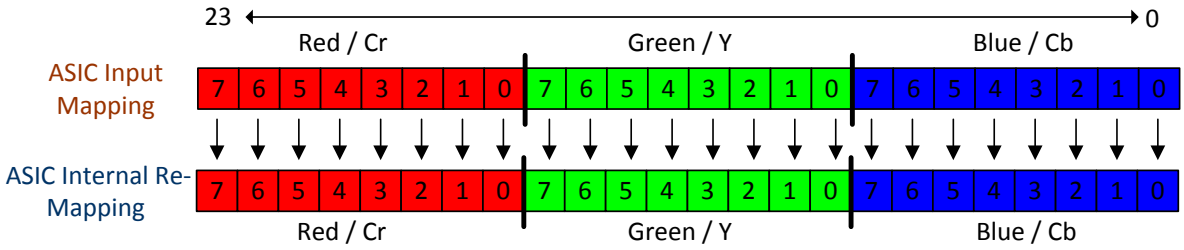


Figure 9. 24-Bit Rgb-888 I/O Mapping

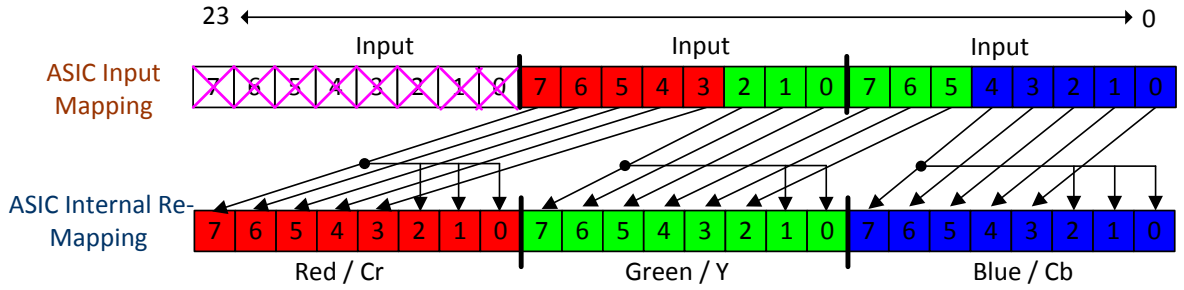


Figure 10. 16-Bit Rgb-565 I/O Mapping

8 Detailed Description

8.1 Overview

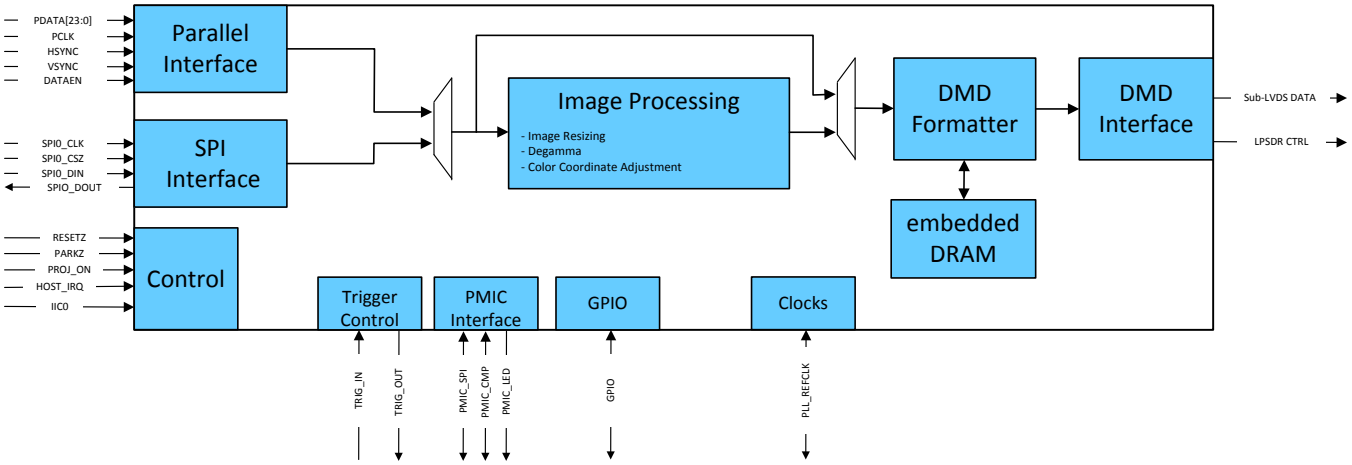
In DLP-based solutions, image data is 100% digital from the DLPC150 controller input port to the image on the DMD. The image stays in digital form and is not converted into an analog signal. The DLPC150 controller processes the digital input image and converts the data into a format needed by the DMD. The DMD steers light by using binary pulse-duration modulation (PWM) for each micromirror. For further details, refer to DMD data sheet (DLPS046 for the DLP2010 and DLPS059 for the DLP2010NIR).

As shown in *Functional Block Diagram*, the DLPC150 controller takes input data from the Parallel or SPI interface, optionally performs image processing, and formats the data for the DMD. The DLPC150 controller offers a Pattern Generation Mode of operation. In Pattern Generation Mode, the DLPC150 bypasses the video processing functions for accurate pattern display with one-to-one association with the corresponding micromirror on the DMD. The pattern generation mode supports inputs and speeds shown in Table 4. This high speed pattern display is well-suited for wavelength selection and control techniques used in spectroscopy, compressive sensing, machine vision, or laser marking.

Table 4. Pattern Generation Mode Supported Inputs And Speeds

INPUT	FORMAT	MAXIMUM PATTERN RATE
SPI Flash memory	Binary pattern sequence encoded as a 16-bit RGB565 image	960 Hz
24-bit parallel input	Binary pattern sequence encoded as a 16-bit RGB565 image	1008 Hz
	Binary pattern sequence encoded as a 24-bit RGB888 image	2880 Hz

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Interface Timing Requirements

This section defines the timing requirements for the external interfaces for the DLPC150 controller.

8.3.1.1 Parallel Interface

The parallel interface complies with standard graphics interface protocol, which includes a vertical sync signal (VSYNC_WE), horizontal sync signal (HSYNC_CS), optional data valid signal (DATAEN_CMD), a 24-bit data bus (PDATA), and a pixel clock (PCLK). The polarity of both syncs and the active edge of the clock are programmable. Figure 5 shows the relationship of these signals. The data valid signal (DATAEN_CMD) is optional in that the DLPC150 provides auto-framing parameters that can be programmed to define the data valid window based on pixel and line counting relative to the horizontal and vertical syncs.

Feature Description (continued)

In addition to these standard signals, an optional side-band signal (PDM_CVS_TE) is available, which allows periodic frame updates to be stopped without losing the displayed image. When PDM_CVS_TE is active, it acts as a data mask and does not allow the source image to be propagated to the display. A programmable PDM polarity parameter determines if it is active high or active low. This parameter defaults to make PDM_CVS_TE active high; if this function is not desired, then it should be tied to a logic low on the PCB. PDM_CVS_TE is restricted to change only during vertical blanking.

NOTE

VSYNC_WE must remain active at all times (in lock-to-VSYNC mode) or the display sequencer will stop and cause the LEDs to be turned off.

8.3.2 Serial Flash Interface

DLPC150 uses an external SPI serial flash memory device for configuration support. The minimum required size is dependent on the desired minimum number of sequences, CMT tables, and splash options while the maximum supported is 16 Mb.

For access to flash, the DLPC150 uses a single SPI interface operating at a programmable frequency complying to industry standard SPI flash protocol. The programmable SPI frequency is defined to be equal to 180 MHz/N, where N is a programmable value between 5 to 127 providing a range from 36.0 to 1.41732 MHz. Note that this results in a relatively large frequency step size in the upper range (for example, 36 MHz, 30 MHz, 25.7 MHz, 22.5 MHz, and so forth) and thus this must be taken into account when choosing a flash device.

The DLPC150 supports two independent SPI chip selects; however, the flash must be connected to SPI chip select zero (SPI0_CSZ0) because the boot routine is only executed from the device connected to chip select zero (SPI0_CSZ0). The boot routine uploads program code from flash to program memory, then transfers control to an auto-initialization routine within program memory. The DLPC150 asserts the HOST_IRQ output signal high while auto-initialization is in progress, then drives it low to signal its completion to the host processor. Only after auto-initialization is complete will the DLPC150 be ready to receive commands through I^2C.

The DLPC150 should support any flash device that is compatible with the modes of operation, features, and performance as defined in Table 5 and Table 6.

Table 5. SPI Flash Required Features or Modes of Operation

FEATURE	DLPC150 REQUIREMENT
SPI interface width	Single
SPI protocol	SPI mode 0
Fast READ addressing	Auto-incrementing
Programming mode	Page mode
Page size	256 B
Sector size	4 KB sector
Block size	any
Block protection bits	0 = Disabled
Status register bit(0)	Write in progress (WIP) {also called flash busy}
Status register bit(1)	Write enable latch (WEN)
Status register bits(6:2)	A value of 0 disables programming protection
Status register bit(7)	Status register write protect (SRWP)
Status register bits(15:8) (that is expansion status byte)	The DLPC150 only supports single-byte status register R/W command execution, and thus may not be compatible with flash devices that contain an expansion status byte. However, as long as expansion status byte is considered optional in the byte 3 position and any write protection control in this expansion status byte defaults to unprotected, then the device should be compatible with DLPC150.

To support flash devices with program protection defaults of either enabled or disabled, the DLPC150 always assumes the device default is enabled and goes through the process of disabling protection as part of the boot-up process. This process consists of:

- A write enable (WREN) instruction executed to request write enable, followed by
- A read status register (RDSR) instruction is then executed (repeatedly as needed) to poll the write enable latch (WEL) bit
- After the write enable latch (WEL) bit is set, a write status register (WRSR) instruction is executed that writes 0 to all 8-bits (this disables all programming protection)

Prior to each program or erase instruction, the DLPC150 issues:

- A write enable (WREN) instruction to request write enable, followed by
- A read status register (RDSR) instruction (repeated as needed) to poll the write enable latch (WEL) bit
- After the write enable latch (WEL) bit is set, the program or erase instruction is executed
- Note the flash automatically clears the write enable status after each program and erase instruction

The specific instruction OpCode and timing compatibility requirements are listed in Table 8 and Table 7. Note however that DLPC150 does not read the flash's electronic signature ID and thus cannot automatically adapt protocol and clock rate based on the ID.

Table 6. SPI Flash Instruction Opcode and Access Profile Compatibility Requirements

SPI FLASH COMMAND	FIRST BYTE (OPCODE)	SECOND BYTE	THIRD BYTE	FOURTH BYTE	FIFTH BYTE	SIXTH BYTE
Fast READ (1 Output)	0x0B	ADDRS(0)	ADDRS(1)	ADDRS(2)	dummy	DATA(0)(1)
Read status	0x05	n/a	n/a	STATUS(0)		
Write status	0x01	STATUS(0)	(2)			
Write enable	0x06					
Page program	0x02	ADDRS(0)	ADDRS(1)	ADDRS(2)	DATA(0)(1)	
Sector erase (4KB)	0x20	ADDRS(0)	ADDRS(1)	ADDRS(2)		
Chip erase	0xC7					

(1) Only the first data byte is show, data continues for the duration of the read.
(2) DLPC150 does not support access to a second/ expansion Write Status byte.

The specific and timing compatibility requirements for a DLPC150 compatible flash are listed in Table 7 and Table 8.

Table 7. SPI Flash Key Timing Parameter Compatibility Requirements(1)(2)

SPI FLASH TIMING PARAMETER	SYMBOL	ALTERNATE SYMBOL	MIN	MAX	UNIT
Access frequency (all commands)	FR	f_C	≤1.42		MHz
Chip select high time (also called chip select deselect time)	t_{SHSL}	t_{CSH}	≤200		ns
Output hold time	t_{CLQX}	t_{HO}	≥0		ns
Clock low to output valid time	t_{CLQV}	t_V		≤ 11	ns
Data in set-up time	t_{DVCH}	t_{DSU}	≤5		ns
Data in hold time	t_{CHDX}	t_{DH}	≤5		ns

(1) The timing values are related to the specification of the flash device itself, not the DLPC150.
(2) The DLPC150 does not drive the $\overline{HOLD}$ or $\overline{WP}$ (active low write protect) pins on the flash device, and thus these pins should be tied to a logic high on the PCB through an external pullup.

The DLPC150 supports 1.8-, 2.5-, or 3.3-V serial flash devices. To do so, VCC_FLSH must be supplied with the corresponding voltage. Table 8 contains a list of 1.8-, 2.5-, and 3.3-V compatible SPI serial flash devices supported by DLPC150.

Table 8. DLPC150 Verified Compatible SPI Flash Device Options(1) (2)

DENSITY (M-BITS)	VENDOR	PART NUMBER	PACKAGE SIZE
1.8-V Compatible Devices			
4 Mb	Winbond	W25Q40BWUXIG	2 × 3 mm USON
4 Mb	Macronix	MX25U4033EBAI-12G	1.43 × 1.94 mm WLCSP
4 Mb	Macronix	MX25U4033EBAI-12G	1.68 × 1.99 mm WLCSP
2.5- or 3.3-V Compatible Devices			
16 Mb	Winbond	W25Q16CLZPIG	5 × 6 mm WSON
64 Mb	Winbond	W25Q64FVZPIG	5 × 6 mm WSON

8.3.3 Serial Flash Programming

Note that the flash can be programmed through the DLPC150 over I^2C or by driving the SPI pins of the flash directly while the DLPC150 I/O are tri-stated. SPI0_CLK, SPI0_DOUT, and SPI0_CSZ0 I/O can be tri-stated by holding RESETZ in a logic low state while power is applied to the DLPC150. Note that SPI0_CSZ1 is not tri-stated by this same action.

8.3.4 I^2C Control Interface

DLPC150 supports I2C commands through the control interface. The control interface allows another master processor to send commands to the DLPC150 chipset to query system status or perform realtime operations. The DLPC150 I^2C interface ports support 100-kHz baud rate at the 7-bit address 0x1B. By definition, I^2C transactions operate at the speed of the slowest device on the bus, thus there is no requirement to match the speed grade of all devices in the system.

8.3.5 DMD (Sub-LVDS) Interface

The DLPC150 controller DMD interface consists of a high speed 1.8-V sub-LVDS output only interface with a maximum clock speed of 532-MHz DDR and a low speed SDR (1.8-V LVCMOS) interface with a fixed clock speed of 120 MHz. The DLPC150 sub-LVDS interface supports a number of DMD display sizes, and as a function of resolution, not all output data lanes are needed as DMD display resolutions decrease in size. With internal software selection, the DLPC150 also supports a limited number of DMD interface swap configurations that can help board layout by remapping specific combinations of DMD interface lines to other DMD interface lines as needed. Table 9 shows the four options available for the DLP2010 or DLP2010NIR (0.2-inch WVGA) DMD. Any unused DMD signal pairs should be left unconnected on the final board design.

Table 9. DLP2010 or DLP2010NIR (0.2-Inch WVGA) DMD – Controller to 4-Lane DMD Pin Mapping Options

DLPC150 CONTROLLER 4 LANE DMD ROUTING OPTIONS				DMD PINS
OPTION 1 SWAP CONTROL = x0	OPTION 2 SWAP CONTROI = x2	OPTION 3 SWAP CONTROL = x1	OPTION 4 SWAP CONTROL = x3	
HS_WDATA_D_P HS_WDATA_D_N	HS_WDATA_E_P HS_WDATA_E_N	HS_WDATA_H_P HS_WDATA_H_N	HS_WDATA_A_P HS_WDATA_A_N	Input DATA_p_0 Input DATA_n_0
HS_WDATA_C_P HS_WDATA_C_N	HS_WDATA_F_P HS_WDATA_F_N	HS_WDATA_G_P HS_WDATA_G_N	HS_WDATA_B_P HS_WDATA_B_N	Input DATA_p_1 Input DATA_n_1
HS_WDATA_F_P HS_WDATA_F_N	HS_WDATA_C_P HS_WDATA_C_N	HS_WDATA_B_P HS_WDATA_B_N	HS_WDATA_G_P HS_WDATA_G_N	Input DATA_p_2 Input DATA_n_2
HS_WDATA_E_P HS_WDATA_E_N	HS_WDATA_D_P HS_WDATA_D_N	HS_WDATA_A_P HS_WDATA_A_N	HS_WDATA_H_P HS_WDATA_H_N	Input DATA_p_3 Input DATA_n_3

(1) The flash supply voltage must match VCC_FLSH on the DLPC150. Special attention needs to be paid when ordering devices to be sure the desired supply voltage is attained as multiple voltage options are often available under the same base part number.
(2) Beware when considering Numonyx (Micron) serial flash devices as they typically do not have the 4KB sector size needed to be DLPC150 compatible.

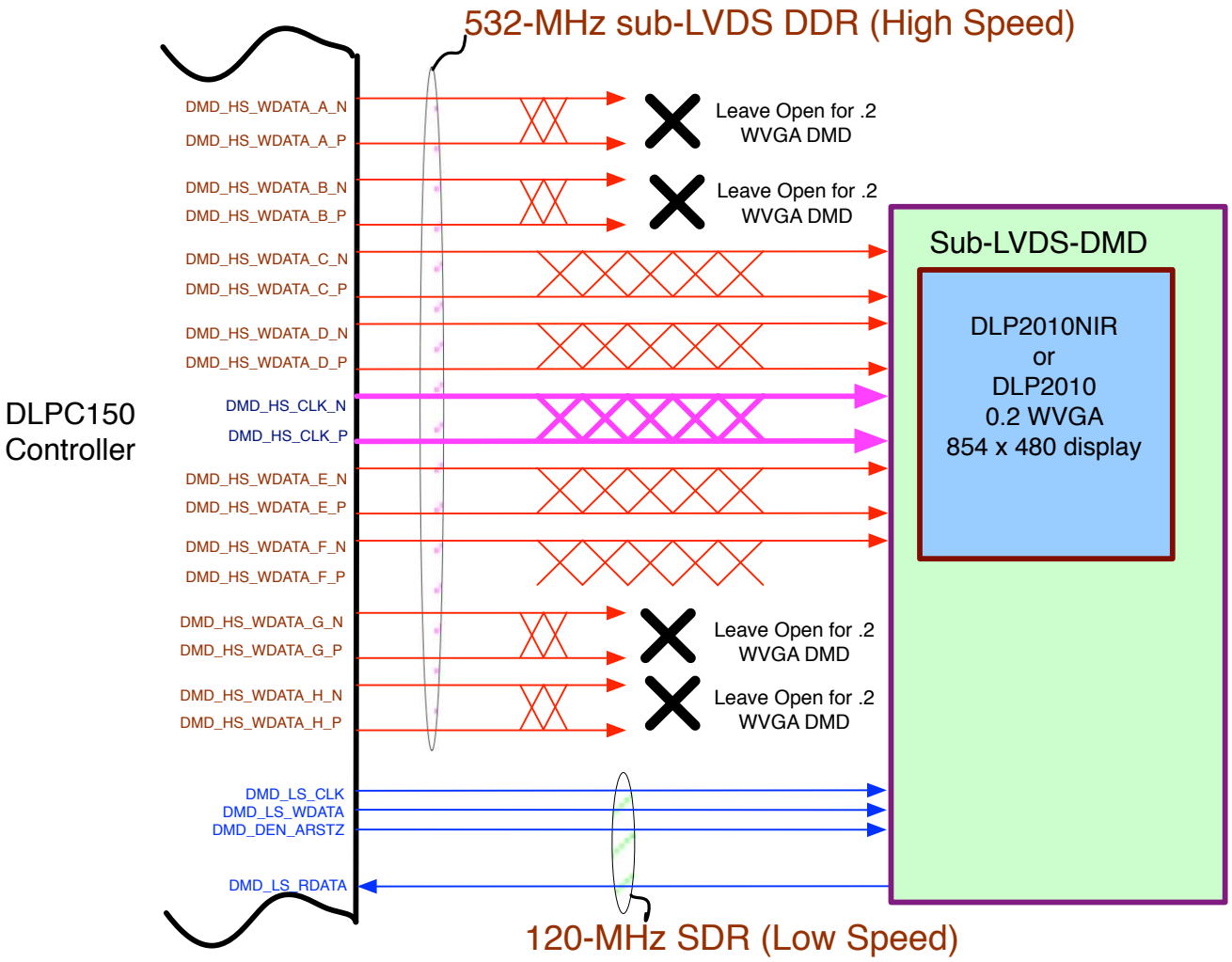


Figure 11. DLP2010 Or DLP2010NIR (0.2-Inch WVGA) DMD Interface Example (Mapping Option 1 Shown)

8.3.6 Calibration And Debug Support

The DLPC150 contains a test point output port, TSTPT_(7:0), which provides selected system calibration support as well as controller debug support. These test points are inputs while reset is applied and switch to outputs when reset is released. The state of these signals is sampled upon the release of system reset and the captured value configures the test mode until the next time reset is applied. Each test point includes an internal pulldown resistor, thus external pullups must be used to modify the default test configuration. The default configuration (x000) corresponds to the TSTPT_(7:0) outputs remaining tri-stated to reduce switching activity during normal operation. For maximum flexibility, an option to jumper to an external pullup is recommended for TSTPT_(2:0). Pullups on TSTPT_(6:3) are used to configure the controller for a specific mode or option. TI does not recommend adding pullups to TSTPT_(7:3) because this has adverse affects for normal operation. This external pullup is only sampled upon a 0-to-1 transition on the RESETZ input, thus changing their configuration after reset is released will not have any effect until the next time reset is asserted and released. Table 10 defines the test mode selection for one programmable scenario defined by TSTPT(2:0).

Table 10. Test Mode Selection Scenario Defined By Tstpt(2:0)(1)

TSTPT(2:0) CAPTURE VALUE	NO SWITCHING ACTIVITY	CLOCK DEBUG OUTPUT
	x000	x010
TSTPT(0)	HI-Z	60 MHz
TSTPT(1)	HI-Z	30 MHz
TSTPT(2)	HI-Z	0.7 to 22.5MHz
TSTPT(3)	HI-Z	HIGH
TSTPT(4)	HI-Z	LOW
TSTPT(5)	HI-Z	HIGH
TSTPT(6)	HI-Z	HIGH
TSTPT(7)	HI-Z	7.5 MHz

(1) These are only the default output selections. Software can reprogram the selection at any time.

8.3.7 DMD Interface Considerations

The sub-LVDS HS interface waveform quality and timing on the DLPC150 controller is dependent on the total length of the interconnect system, the spacing between traces, the characteristic impedance, etch losses, and how well matched the lengths are across the interface. Thus, ensuring positive timing margin requires attention to many factors.

As an example, DMD interface system timing margin can be calculated as follows:

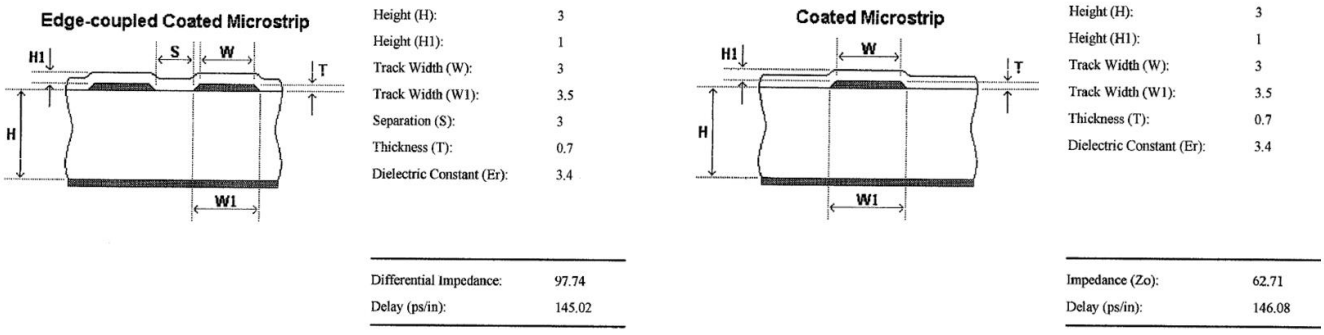
Setup Margin = (DLPC150 output setup) – (DMD input setup) – (PCB routing mismatch) – (PCB SI degradation) (1)

Hold-time Margin = (DLPC150 output hold) – (DMD input hold) – (PCB routing mismatch) – (PCB SI degradation)

where PCB SI degradation is signal integrity degradation due to PCB affects which includes such things as Simultaneously Switching Output (SSO) noise, cross-talk and Inter-symbol Interference (ISI) noise. (2)

DLPC150 I/O timing parameters as well as DMD I/O timing parameters can be found in their corresponding data sheets. Similarly, PCB routing mismatch can be budgeted and met through controlled PCB routing. However, PCB SI degradation is a more complicated adjustment.

In an attempt to minimize the signal integrity analysis that would otherwise be required, the following PCB design guidelines are provided as a reference of an interconnect system that will satisfy both waveform quality and timing requirements (accounting for both PCB routing mismatch and PCB SI degradation). Variation from these recommendations may also work, but should be confirmed with PCB signal integrity analysis or lab measurements.



DMD_HS Differential Signals DMD_LS Signals

Figure 12. DMD Interface Board Stack-Up Details

8.4 Device Functional Modes

DLPC150 has two functional modes (ON/OFF) controlled by a single pin PROJ_ON:

- When pin PROJ_ON is set high, the DLPA2000 or DLPA2005 applies power to the DMD and the DLPC150.
- When pin PROJ_ON is set low, the DLPA2000 or DLPA2005 powers down and only microwatts of power are consumed.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DLPC150 controller couples with DLP2010 or DLP2010NIR DMD to provide a reliable solution for many data and video display applications. The DMDs are spatial light modulators which reflect incoming light from an illumination source to one of two positions, with the primary position being into a projection or collection optic. Each specific application typically requires a system-level optical architecture that integrates the DMD, as well as, a particular data format to the DLPC150. For example, in a spectroscopy application, the DLP2010NIR DMD is often combined with a single element detector to replace expensive InGaAs array-based detector designs. In this application, the DMD acts as a wavelength selector diverting specific wavelengths of light through the collection optics into the single point detector by setting specific columns of pixel in the "on" position. All other DMD columns that are "off" divert the unselected wavelengths away from the detector's optical path so as to not interfere with the selected wavelength measurement. The DLPC150 controls the set of patterns that sequentially turns columns of pixels "on" or "off" to scan the desired wavelenght spectrum.

Other applications of interest include machine vision systems, spectrometers, skin analysis, medical systems, material identification, chemical sensing, infrared projection, and compressive sensing.

9.1.1 DLPC150 System Design Consideration – Application Notes

System power regulation: It is acceptable for VDD_PLLD and VDD_PLLM to be derived from the same regulator as the core VDD, but to minimize the AC noise component they should be filtered as recommended in the *PCB Layout Guidelines For Internal Controller PLL Power*.

9.2 Typical Application

A typical embedded system application using the DLPC150 controller and the DLPC2010NIR is shown in Figure 13. In this configuration, the DLPC150 controller supports a 24-bit parallel RGB input, typical of LCD interfaces, from an external source or processor. The DLPC150 controller processes the digital input image and converts the data into the format needed by the DLP2010NIR. The DLP2010NIR steers light by setting specific micromirrors to the "on" position, directing light to the detector, while unwanted micromirrors are set to "off" position, directing light away from the detector. The microprocessor sends binary images to the DLP2010NIR to steer specific wavelengths of light into the detector. The microprocessor uses an analog-to-digital converter to sample the signal received by the detector into a digital value. By sequentially selecting different wavelengths of light and capturing the values at the detector, the microprocessor can then plot a spectral response to the light.

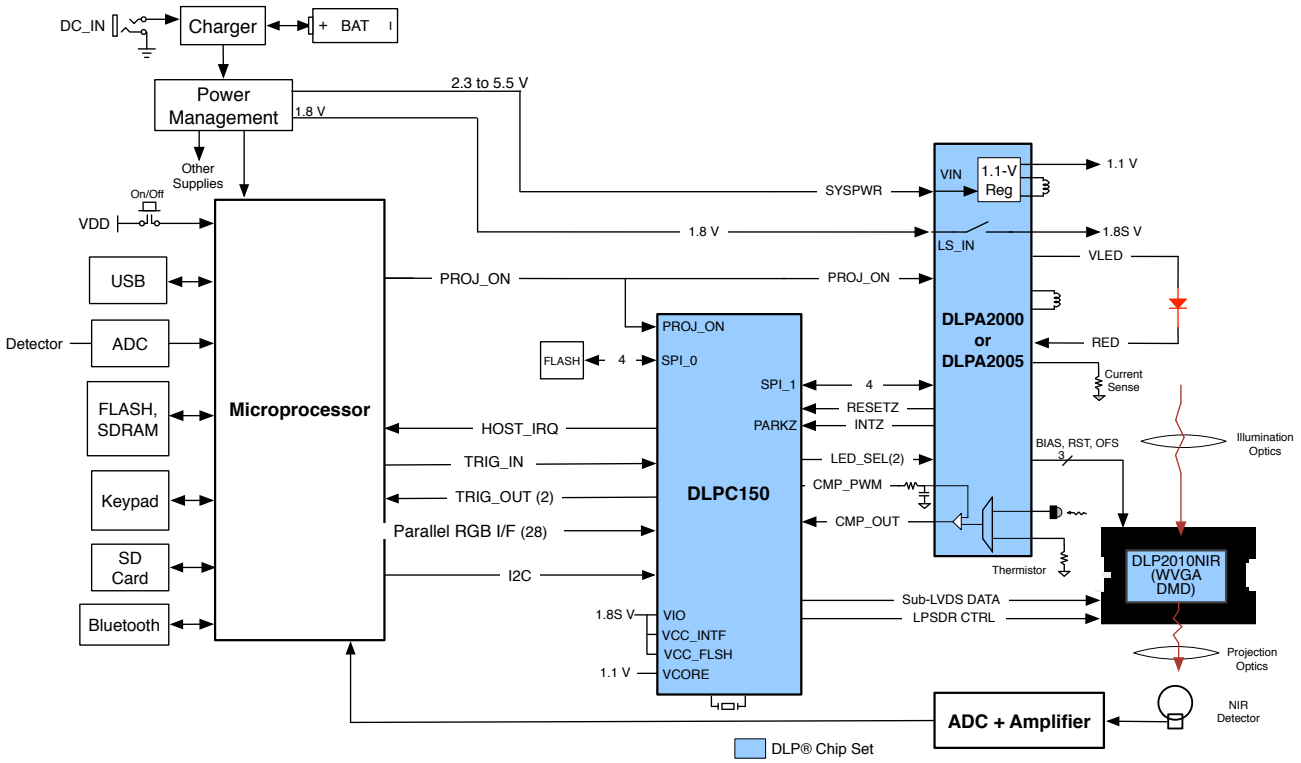


Figure 13. Typical Application Diagram

9.2.1 Design Requirements

All applications using the DLP 0.2-inch WVGA chipset require the:

- DLPC150 controller, and
- DLPA2000 or DLPA2005 PMIC, and
- DLP2010 or DLP2010NIR DMD

components for operation. The system also requires an external parallel flash memory device loaded with the DLPC150 configuration and support firmware. DLPC150 does the digital image processing and formats the data for the DMD. DLPA2000 or DLPA2005 PMIC provides the needed analog functions for the DLPC150 and DLP2010 or DLP2010NIR. The chipset has several system interfaces and requires some support circuitry. The following interfaces and support circuitry are required:

- DLPC150 system interfaces:
  - Control interface
  - Trigger interface
  - Input data interface
  - Illumination interface

Typical Application (continued)

- DLPC150 support circuitry and interfaces:
  - Reference clock
  - PLL
  - Program memory flash interface
- DMD interfaces:
  - DLPC150 to DMD digital data
  - DLPC150 to DMD control interface
  - DLPC150 to DMD micromirror reset control interface

9.2.2 Detailed Design Procedure

9.2.2.1 DLPC150 System Interfaces

The 0.2-inch WVGA chipset supports a16-bit or 24-bit parallel RGB interface for image data transfers from another device. There are two primary output interfaces: illumination driver control interface and sync outputs.

9.2.2.1.1 Control Interface

The 0.2-inch WVGA chipset supports I2C commands through the control interface. The control interface allows another master processor to send commands to the DLPC150 controller to query system status or perform realtime operations such as LED driver current settings.

9.2.3 Application Curve

In a reflective spectroscopy application, a broadband light source illuminates a sample and the reflected light spectrum is dispersed onto the DLP2010NIR. A microprocessor in conjunction with the DLPC150 controls individual DLP2010NIR micromirrors to reflect specific wavelengths of light to a single point detector. The microprocessor uses an analog-to-digital converter to sample the signal received by the detector into a digital value. By sequentially selecting different wavelengths of light and capturing the values at the detector, the microprocessor can then plot a spectral response to the light. This systems allows the measurement of the collected light and derive the wavelengths absorbed by the sample. This process leads to the absorption spectrum shown in Figure 14.

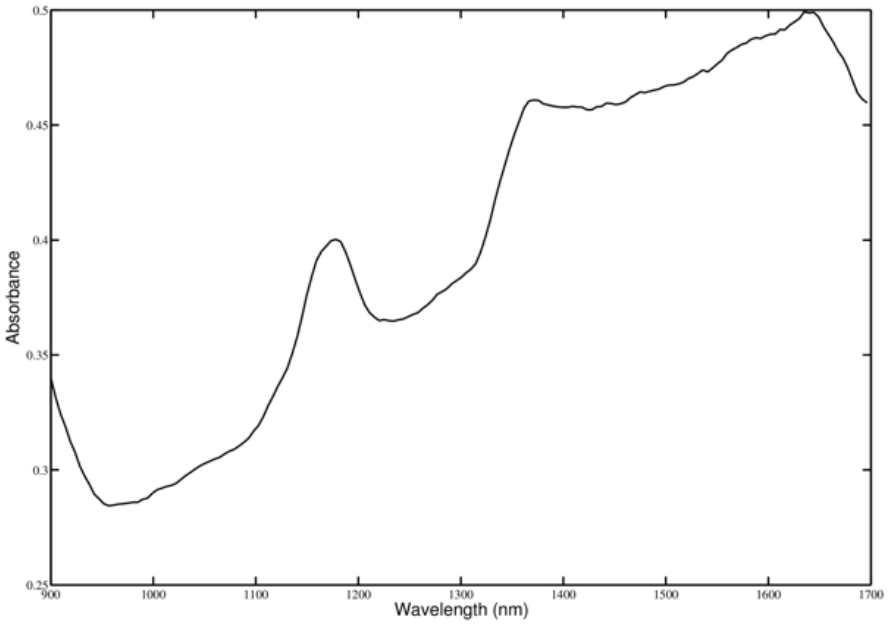


Figure 14. Sample DLPC150-Based Spectrometer Output

10 Power Supply Recommendations

10.1 System Power-Up and Power-Down Sequence

Although the DLPC150 requires an array of power supply voltages, (for example, VDD, VDDLP12, VDD_PLLM/D, VCC18, VCC_FLSH, VCC_INTF), if VDDLP12 is tied to the 1.1-V VDD supply (which is assumed to be the typical configuration), then there are no restrictions regarding the relative order of power supply sequencing to avoid damaging the DLPC150. This is true for both power-up and power-down scenarios. Similarly, there is no minimum time between powering-up or powering-down the different supplies if VDDLP12 is tied to the 1.1-V VDD supply.

If however VDDLP12 is not tied to the VDD supply, then VDDLP12 must be powered-on after the VDD supply is powered-on, and powered-off before the VDD supply is powered-off. In addition, if VDDLP12 is not tied to VDD, then VDDLP12 and VDD supplies must be powered on or powered off within 100 ms of each other.

Although there is no risk of damaging the DLPC150 if the above power sequencing rules are followed, the following additional power sequencing recommendations must be considered to ensure proper system operation.

- To ensure that DLPC150 output signal states behave as expected, all DLPC150 I/O supplies must remain applied while VDD core power is applied. If VDD core power is removed while the I/O supply (VCC_INTF) is applied, then the output signal state associated with the inactive I/O supply will go to a high impedance state.
- Additional power sequencing rules may exist for devices that share the supplies with the DLPC150, and thus these devices may force additional system power sequencing requirements.

Note that when VDD core power is applied, but I/O power is not applied, additional leakage current may be drawn. This added leakage does not affect normal DLPC150 operation or reliability.

Figure 15 and Figure 16 show the DLPC150 power-up and power-down sequence for both the normal PARK and fast PARK operations of the DLPC150 controller.

System Power-Up and Power-Down Sequence (continued)

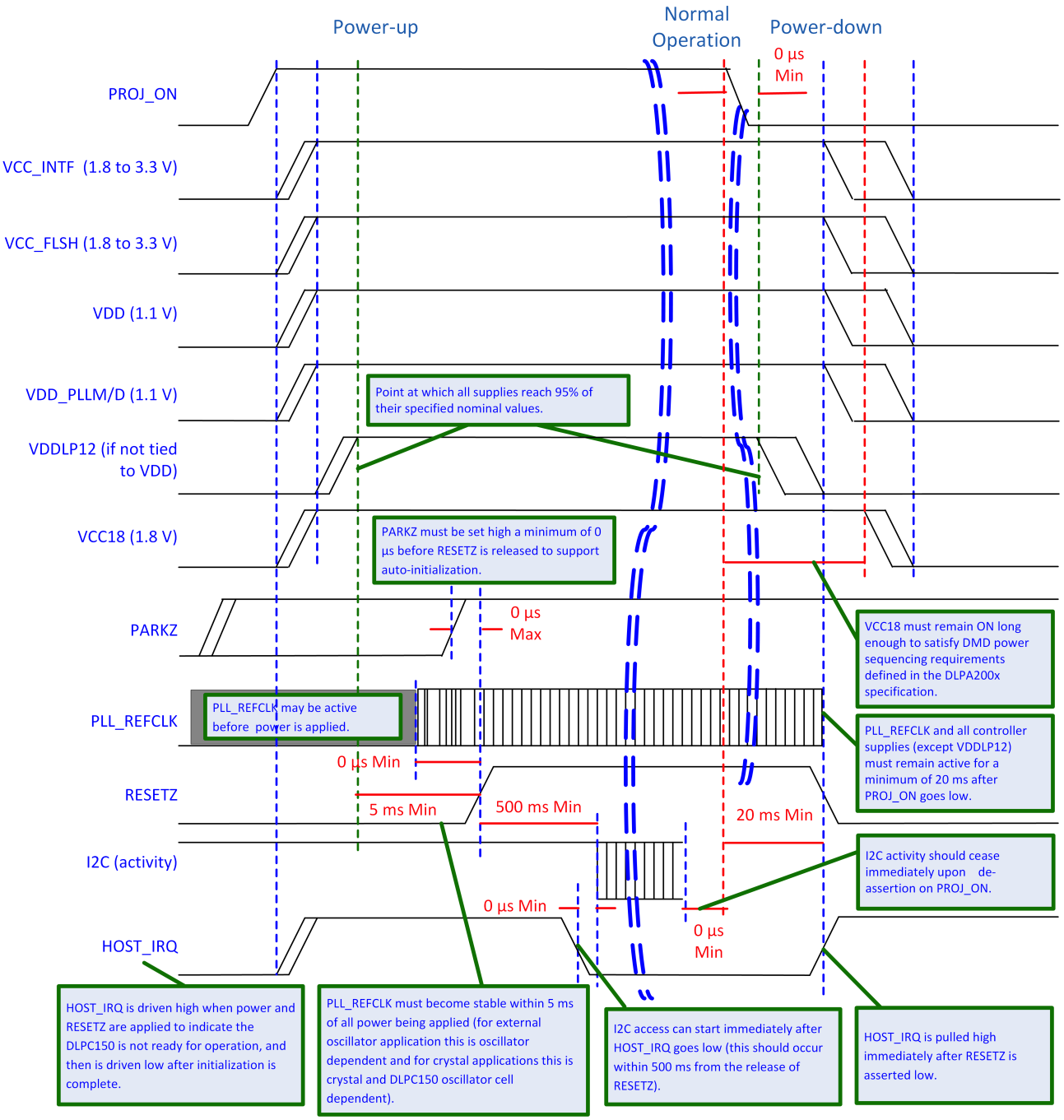


Figure 15. DLPC150 Power-Up / Proj_on = 0 Initiated Normal Park and Power-Down

System Power-Up and Power-Down Sequence (continued)

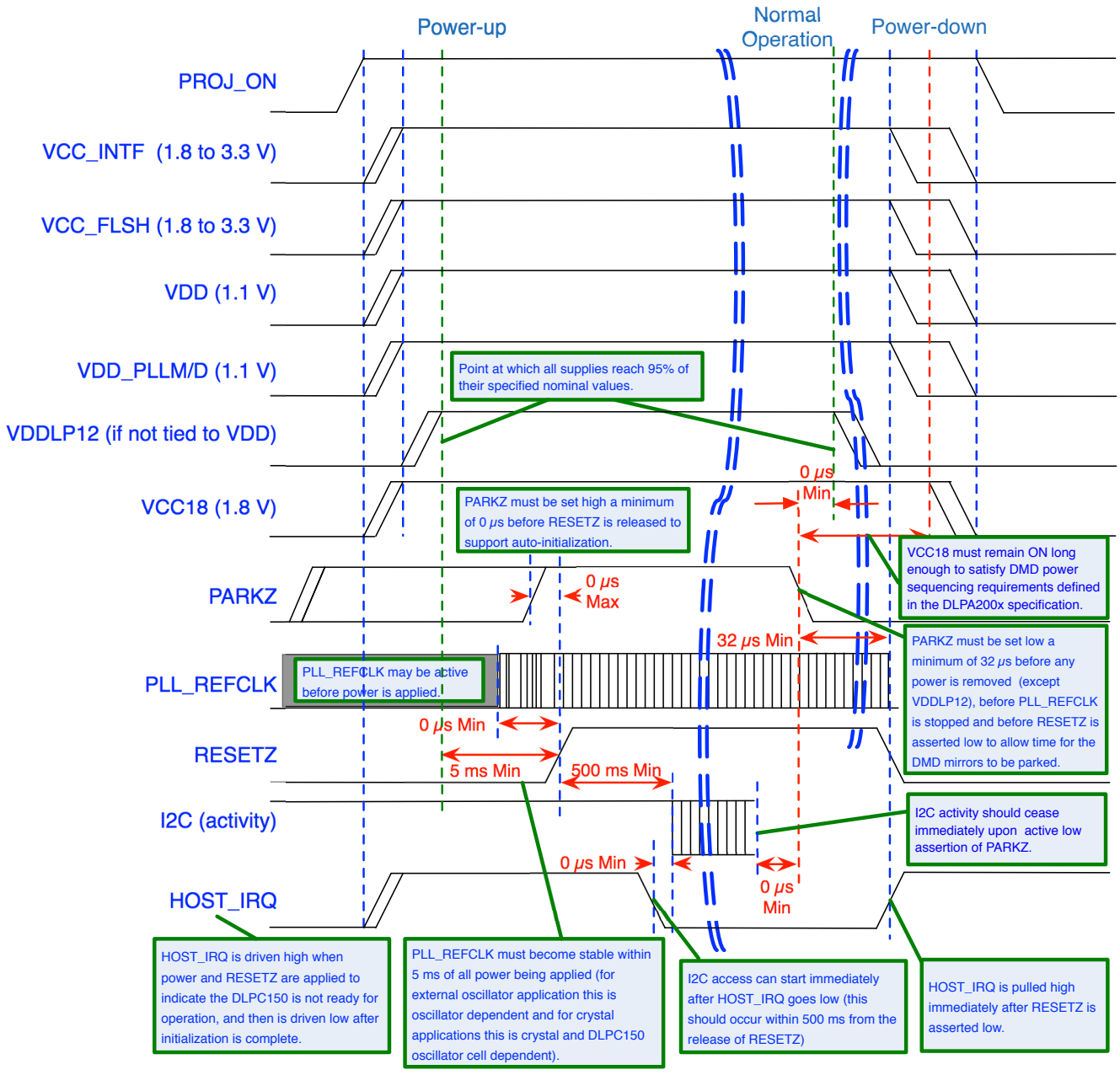


Figure 16. DLPC150 Power-Up / PARKZ = 0 Initiated Fast Park and Power-Down

10.2 DLPC150 Power-Up Initialization Sequence

It is assumed that an external power monitor will hold the DLPC150 in system reset during power-up. It must do this by driving RESETZ to a logic low state. It should continue to assert system reset until all controller voltages have reached minimum specified voltage levels, PARKZ is asserted high, and input clocks are stable. During this time, most controller outputs will be driven to an inactive state and all bidirectional signals will be configured as inputs to avoid contention. controller outputs that are not driven to an inactive state are tri-stated. These include LED_SEL_0, LED_SEL_1, SPICLK, SPIDOUT, and SPICSZ0 (see RESETZ pin description for full signal descriptions in *Pin Configuration and Functions*). After power is stable and the PLL_REFCLK_I clock input to the DLPC150 is stable, then RESETZ should be deactivated (set to a logic high). The DLPC150 then performs a

DLPC150 Power-Up Initialization Sequence (continued)

power-up initialization routine that first locks its PLL followed by loading self configuration data from the external flash. Upon release of RESETZ all DLPC150 I/Os will become active. Immediately following the release of RESETZ, the HOST_IRQ signal will be driven high to indicate that the auto initialization routine is in progress. However, since a pullup resistor is connected to signal HOST_IRQ, this signal will have already gone high before the DLPC150 actively drives it high. Upon completion of the auto-initialization routine, the DLPC150 will drive HOST_IRQ low to indicate the initialization done state of the DLPC150 has been reached.

Note that the host processor can start sending I^2C commands after HOST_IRQ goes low.

10.3 DMD Fast Park Control (PARKZ)

The PARKZ signal is defined to be an early warning signal that should alert the controller 40 µs before DC supply voltages have dropped below specifications in fast PARK operation. This allows the controller time to park the DMD, ensuring the integrity of future operation. Note that the reference clock should continue to run and RESETZ should remain deactivated for at least 40 µs after PARKZ has been deactivated (set to a logic low) to allow the park operation to complete.

10.4 Hot Plug Usage

The DLPC150 provides fail-safe I/O on all host interface signals (signals powered by VCC_INTF). This allows these inputs to be driven high even when no I/O power is applied. Under this condition, the DLPC150 will not load the input signal nor draw excessive current that could degrade controller reliability. For example, the I^2C bus from the host to other components would not be affected by powering off VCC_INTF to the DLPC150. TI recommends weak pullups or pulldowns on signals feeding back to the host to avoid floating inputs.

If the I/O supply (VCC_INTF) is powered off, but the core supply (VDD) is powered on, then the corresponding input buffer may experience added leakage current, but this does not damage the DLPC150.

10.5 Maximum Signal Transition Time

Unless otherwise noted, 10 ns is the maximum recommended 20 to 80% rise or fall time to avoid input buffer oscillation. This applies to all DLPC150 input signals. However, the PARKZ input signal includes an additional small digital filter that ignores any input buffer transitions caused by a slower rise or fall time for up to 150 ns.

11 Layout

11.1 Layout Guidelines

11.1.1 PCB Layout Guidelines For Internal Controller PLL Power

The following guidelines are recommended to achieve desired controller performance relative to the internal PLL. The DLPC150 contains 2 internal PLLs which have dedicated analog supplies (VDD_PLLM , VSS_PLLM, VDD_PLLD, VSS_PLLD). As a minimum, VDD_PLLx power and VSS_PLLx ground pins should be isolated using a simple passive filter consisting of two series Ferrites and two shunt capacitors (to widen the spectrum of noise absorption). It's recommended that one capacitor be a 0.1µF capacitor and the other be a 0.01µF capacitor. All four components should be placed as close to the controller as possible but it's especially important to keep the leads of the high frequency capacitors as short as possible. Note that both capacitors should be connected across VDD_PLLM and VSS_PLLM / VDD_PLLD and VSS_PLLD respectfully on the controller side of the Ferrites.

For the ferrite beads used, their respective characteristics should be as follows:

- DC resistance less than 0.40 Ω
- Impedance at 10 MHz equal to or greater than 180 Ω
- Impedance at 100 MHz equal to or greater than 600 Ω

The PCB layout is critical to PLL performance. It is vital that the quiet ground and power are treated like analog signals. Therefore, VDD_PLLM and VDD_PLLD must be a single trace from the DLPC150 to both capacitors and then through the series ferrites to the power source. The power and ground traces should be as short as possible, parallel to each other, and as close as possible to each other.

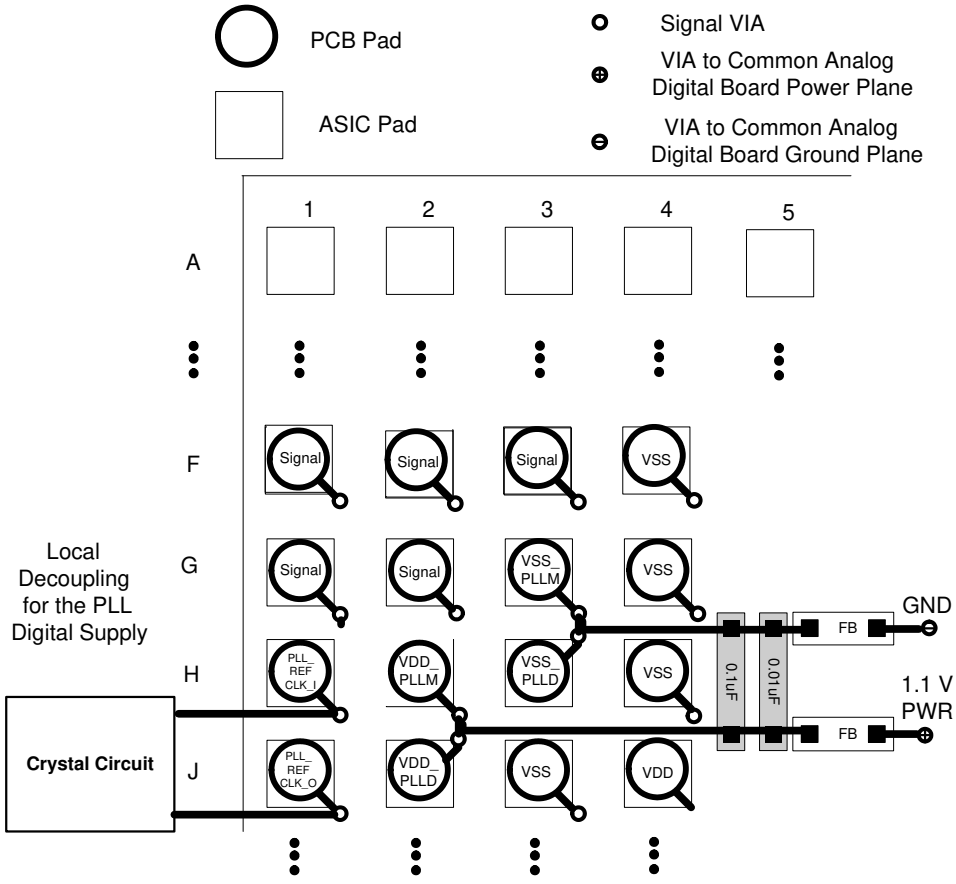
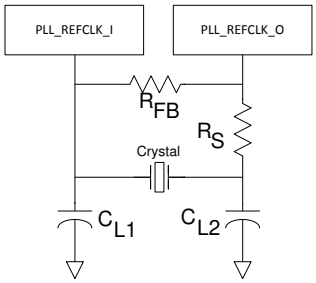


Figure 17. PLL Filter Layout

Layout Guidelines (continued)

11.1.2 DLPC150 Reference Clock

The DLPC150 requires an external reference clock to feed its internal PLL. A crystal or oscillator can supply this reference. For flexibility, the DLPC150 accepts either of two reference clock frequencies (see Table 12), but both must have a maximum frequency variation of ±200 ppm (including aging, temperature, and trim component variation). When a crystal is used, several discrete components are also required as shown in Figure 18.



A. CL = Crystal load capacitance (farads)

B. CL1 = 2 × (CL – Cstray_pll_refclk_i)

C. CL2 = 2 × (CL – Cstray_pll_refclk_o)

D. Where: Cstray_pll_refclk_i = Sum of package and PCB stray capacitance at the crystal pin associated with the controller pin pll_refclk_i. Cstray_pll_refclk_o = Sum of package and PCB stray capacitance at the crystal pin associated with the controller pin pll_refclk_o.

Figure 18. Recommended Crystal Oscillator Configuration

11.1.2.1 Recommended Crystal Oscillator Configuration

Table 11. Crystal Port Characteristics

PARAMETER	NOMINAL	UNIT
PLL_REFCLK_I TO GND capacitance	1.5	pF
PLL_REFCLK_O TO GND capacitance	1.5	pF

Table 12. Recommended Crystal Configuration(1)(2)

PARAMETER	RECOMMENDED	UNIT
Crystal circuit configuration	Parallel resonant	
Crystal type	Fundamental (first harmonic)	
Crystal nominal frequency	24 or 16	MHz
Crystal frequency tolerance (including accuracy, temperature, aging and trim sensitivity)	±200	PPM
Maximum startup time	1.0	ms
Crystal equivalent series resistance (ESR)	120 max	Ω
Crystal load	6	pF
RS drive resistor (nominal)	100	Ω
RFB feedback resistor (nominal)	1Meg	Ω
CL1 external crystal load capacitor	See equation in Figure 18 notes	pF
CL2 external crystal load capacitor	See equation in Figure 18 notes	pF
PCB layout	A ground isolation ring around the crystal is recommended	

(1) Temperature range of –30°C to +85°C.
(2) The crystal bias is determined by the controller's VCC_INTF voltage rail, which is variable (not the VCC18 rail).

If an external oscillator is used, then the oscillator output must drive the PLL_REFCLK_I pin on the DLPC150 DLPC150 controller and the PLL_REFCLK_O pins should be left unconnected.

Table 13. DLPC150 Recommended Crystal Parts(1)(2)

MANUFACTURER	PART NUMBER	SPEED	TEMPERATURE AND AGING	ESR	LOAD CAPACITANCE
KDS	DSX211G-24.000M-8pF-50-50	24 MHz	±50 ppm	120-Ω max	8 pF

(1) Crystal package sizes: 2.0 × 1.6 mm for both crystals.
(2) Operating temperature range: –30°C to +85°C for all crystals.

11.1.3 General PCB Recommendations

TI recommends 1-oz. copper planes in the PCB design to achieve needed thermal connectivity.

11.1.4 General Handling Guidelines for Unused CMOS-Type Pins

To avoid potentially damaging current caused by floating CMOS input-only pins, TI recommends that unused DLPC150 controller input pins be tied through a pullup resistor to its associated power supply or a pulldown to ground. For DLPC150 controller inputs with an internal pullup or pulldown resistors, it is unnecessary to add an external pullup or pulldown unless specifically recommended. Note that internal pullup and pulldown resistors are weak and should not be expected to drive the external line. The DLPC150 implements very few internal resistors and these are noted in the pin list. When external pullup or pulldown resistors are needed for pins that have built-in weak pullups or pulldowns, use the value 8 kΩ (max).

Unused output-only pins should never be tied directly to power or ground, but can be left open.

When possible, TI recommends that unused bidirectional I/O pins be configured to their output state such that the pin can be left open. If this control is not available and the pins may become an input, then they should be pulled-up (or pulled-down) using an appropriate, dedicated resistor.

11.1.5 Maximum Pin-to-Pin, PCB Interconnects Etch Lengths

Table 14. Max Pin-to-Pin PCB Interconnect Recommendations(1)(2)

DMD BUS SIGNAL	SIGNAL INTERCONNECT TOPOLOGY		UNIT
	SINGLE BOARD SIGNAL ROUTING LENGTH	MULTI-BOARD SIGNAL ROUTING LENGTH	
DMD_HS_CLK_P DMD_HS_CLK_N	6.0 152.4	See (3)	inch (mm)
DMD_HS_WDATA_A_P DMD_HS_WDATA_A_N	6.0 152.4	See (3)	inch (mm)
DMD_HS_WDATA_B_P DMD_HS_WDATA_B_N			
DMD_HS_WDATA_C_P DMD_HS_WDATA_C_N			
DMD_HS_WDATA_D_P DMD_HS_WDATA_D_N			
DMD_HS_WDATA_E_P DMD_HS_WDATA_E_N			
DMD_HS_WDATA_F_P DMD_HS_WDATA_F_N			
DMD_HS_WDATA_G_P DMD_HS_WDATA_G_N			
DMD_HS_WDATA_H_P DMD_HS_WDATA_H_N			
DMD_LS_CLK	6.5 165.1	See (3)	inch (mm)
DMD_LS_WDATA	6.5 165.1	See (3)	inch (mm)
DMD_LS_RDATA	6.5 165.1	See (3)	inch (mm)
DMD_DEN_ARSTZ	7.0 177.8	See (3)	inch (mm)

(1) Max signal routing length includes escape routing.
(2) Multi-board DMD routing length is more restricted due to the impact of the connector.
(3) Due to board variations, these are impossible to define. Any board designs should SPICE simulate with the DLPC150 controller IBIS models to ensure single routing lengths do not exceed requirements.

Table 15. High Speed PCB Signal Routing Matching Requirements (1)(2)(3)(4)

SIGNAL GROUP LENGTH MATCHING				
INTERFACE	**SIGNAL GROUP**	**REFERENCE SIGNAL**	**MAX MISMATCH (5)**	**UNIT**
DMD	DMD_HS_WDATA_A_P DMD_HS_WDATA_A_N	DMD_HS_CLK_P DMD_HS_CLK_N	±0.1 (±25.4)	inch (mm)
	DMD_HS_WDATA_B_P DMD_HS_WDATA_B_N			
	DMD_HS_WDATA_C_P DMD_HS_WDATA_C_N			
	DMD_HS_WDATA_D_P DMD_HS_WDATA_D_N			
	DMD_HS_WDATA_E_P DMD_HS_WDATA_E_N			
	DMD_HS_WDATA_F_P DMD_HS_WDATA_F_N			
	DMD_HS_WDATA_G_P DMD_HS_WDATA_G_N			
	DMD_HS_WDATA_H_P DMD_HS_WDATA_H_N			
DMD	DMD_LS_WDATA DMD_LS_RDATA	DMD_LS_CLK	±0.2 (±5.08)	inch (mm)
DMD	DMD_DEN_ARSTZ	N/A	N/A	inch (mm)

(1) These values apply to PCB routing only. They do not include any internal package routing mismatch associated with the DLPC150, the DMD.
(2) DMD HS data lines are differential, thus these specifications are pair-to-pair.
(3) Training is applied to DMD HS data lines, so defined matching requirements are slightly relaxed.
(4) DMD LS signals are single ended.
(5) Mismatch variance applies to high-speed data pairs. For all high-speed data pairs, the maximum mismatch between pairs should be 1 mm or less.

11.1.6 Number of Layer Changes

- Single-ended signals: Minimize the number of layer changes.
- Differential signals: Individual differential pairs can be routed on different layers, but the signals of a given pair should not change layers.

11.1.7 Stubs

- Stubs should be avoided.

11.1.8 Terminations

- No external termination resistors are required on DMD_HS differential signals.
- The DMD_LS_CLK and DMD_LS_WDATA signal paths should include a 43-Ω series termination resistor located as close as possible to the corresponding DLPC150 controller pins.
- The DMD_LS_RDATA signal path should include a 43-Ω series termination resistor located as close as possible to the corresponding DMD pin.
- DMD_DEN_ARSTZ does not require a series resistor.

11.1.9 Routing Vias

- The number of vias on DMD_HS signals should be minimized and should not exceed two.
- Any and all vias on DMD_HS signals should be located as close to the DLPC150 controller as possible.
- The number of vias on the DMD_LS_CLK and DMD_LS_WDATA signals should be minimized and not exceed two.
- Any and all vias on the DMD_LS_CLK and DMD_LS_WDATA signals should be located as close to the DLPC150 controller as possible.

11.2 Layout Example

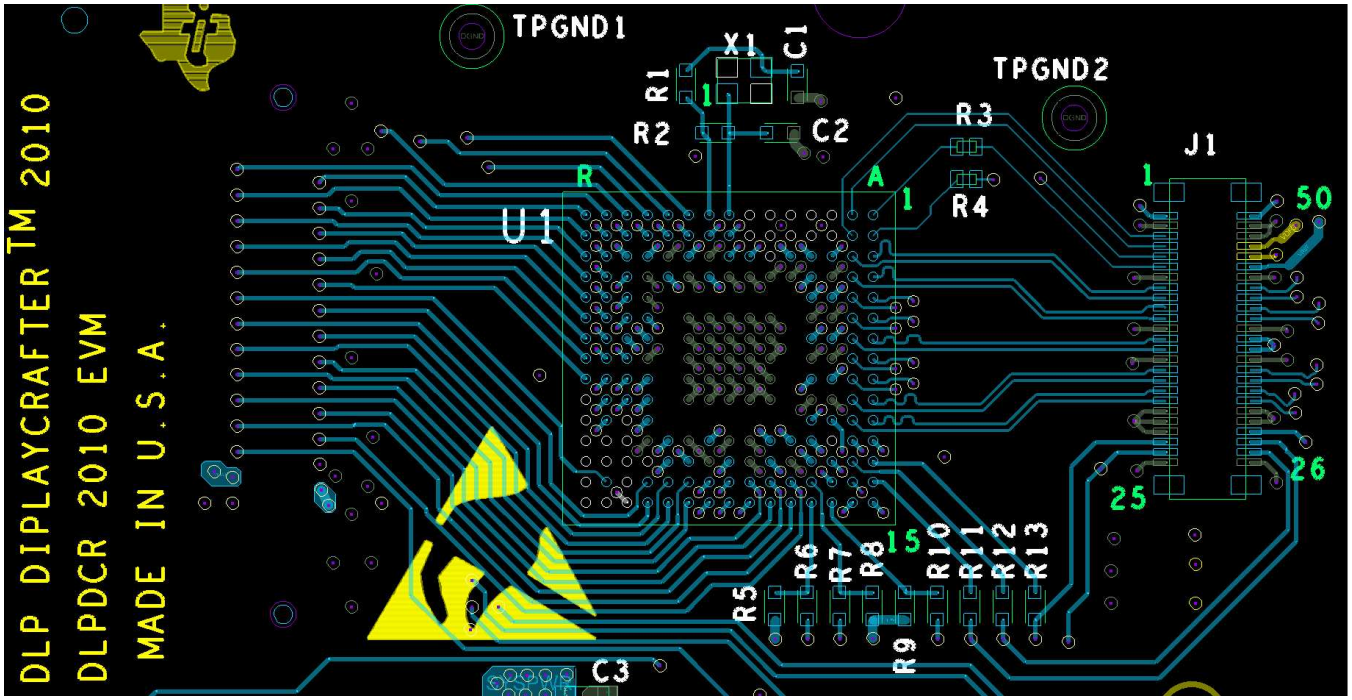


Figure 19. Board Layout Example

11.3 Thermal Considerations

The underlying thermal limitation for the DLPC150 is that the maximum operating junction temperature (T_J) not be exceeded (this is defined in the *Recommended Operating Conditions*). This temperature is dependent on operating ambient temperature, airflow, PCB design (including the component layout density and the amount of copper used), power dissipation of the DLPC150, and power dissipation of surrounding components. The DLPC150's package is designed primarily to extract heat through the power and ground planes of the PCB. Thus, copper content and airflow over the PCB are important factors.

The recommended maximum operating ambient temperature (T_A) is provided primarily as a design target and is based on maximum DLPC150 power dissipation and $R_{\theta JA}$ at 0 m/s of forced airflow, where $R_{\theta JA}$ is the thermal resistance of the package as measured using a glater test PCB with two, 1-oz power planes. This JEDEC test PCB is not necessarily representative of the DLPC150 PCB; the reported thermal resistance may not be accurate in the actual product application. Although the actual thermal resistance may be different, it is the best information available during the design phase to estimate thermal performance. However, after the PCB is designed and the product is built, TI highly recommends that thermal performance be measured and validated.

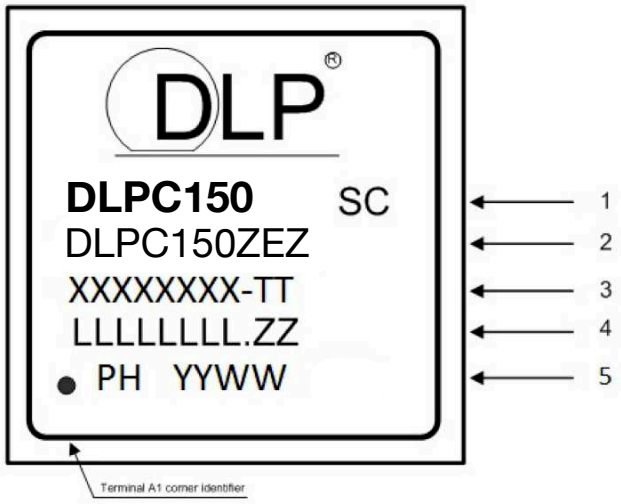
To do this, measure the top center case temperature under the worse case product scenario (max power dissipation, max voltage, max ambient temperature) and validated not to exceed the maximum recommended case temperature (T_C). This specification is based on the measured φ_{JT} for the DLPC150 package and provides a relatively accurate correlation to junction temperature. Take care when measuring this case temperature to prevent accidental cooling of the package surface. TI recommends a small (approximately 40 gauge) thermocouple. The bead and thermocouple wire should contact the top of the package and be covered with a minimal amount of thermally conductive epoxy. The wires should be routed closely along the package and the board surface to avoid cooling the bead through the wires.

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 デバイスの項目表記

12.1.1.1 デバイスのマーキング



マーキングの定義:

1行目:	DLP デバイス名 : DLPC150 SC: ハンダ・ボール組成 e1: SnAgCuからなる鉛フリー・ハンダ・ボールを示しています。 G8: 錫・銀・銅(SnAgCu)からなり、銀の含有量が1.5%以下で、モールド化合物がTIのグリーン規定を満たしている鉛フリー・ハンダ・ボールを示しています。
2 行目:	TI 型番
3 行目:	XXXXXXXX-TT : 製造元の型番
4 行目:	LLLLLLLL.ZZ : 半導体ウエハーの工場ロット・コードと鉛フリー・半田ボール・マーキング
5行目:	PH YYWW : パッケージ組み立て情報

12.2 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 16. 関連リンク

製品	プロダクト・フォルダ	サンプルと購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
DLP2010NIR	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
DLP2010	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
DLPA2000	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
DLPA2005	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

12.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 商標

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DLP is a registered trademark of Texas Instruments.
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12.5 静電気放電に関する注意事項

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12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

13.1 Package Option Addendum

13.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking(4)(5)
DLPC150ZEZ	DLPC150ZEZ	NFBGA	ZEZ	201	1	TBD	Call TI	Level-3-260C-168 HRS	–30 to 85	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(5) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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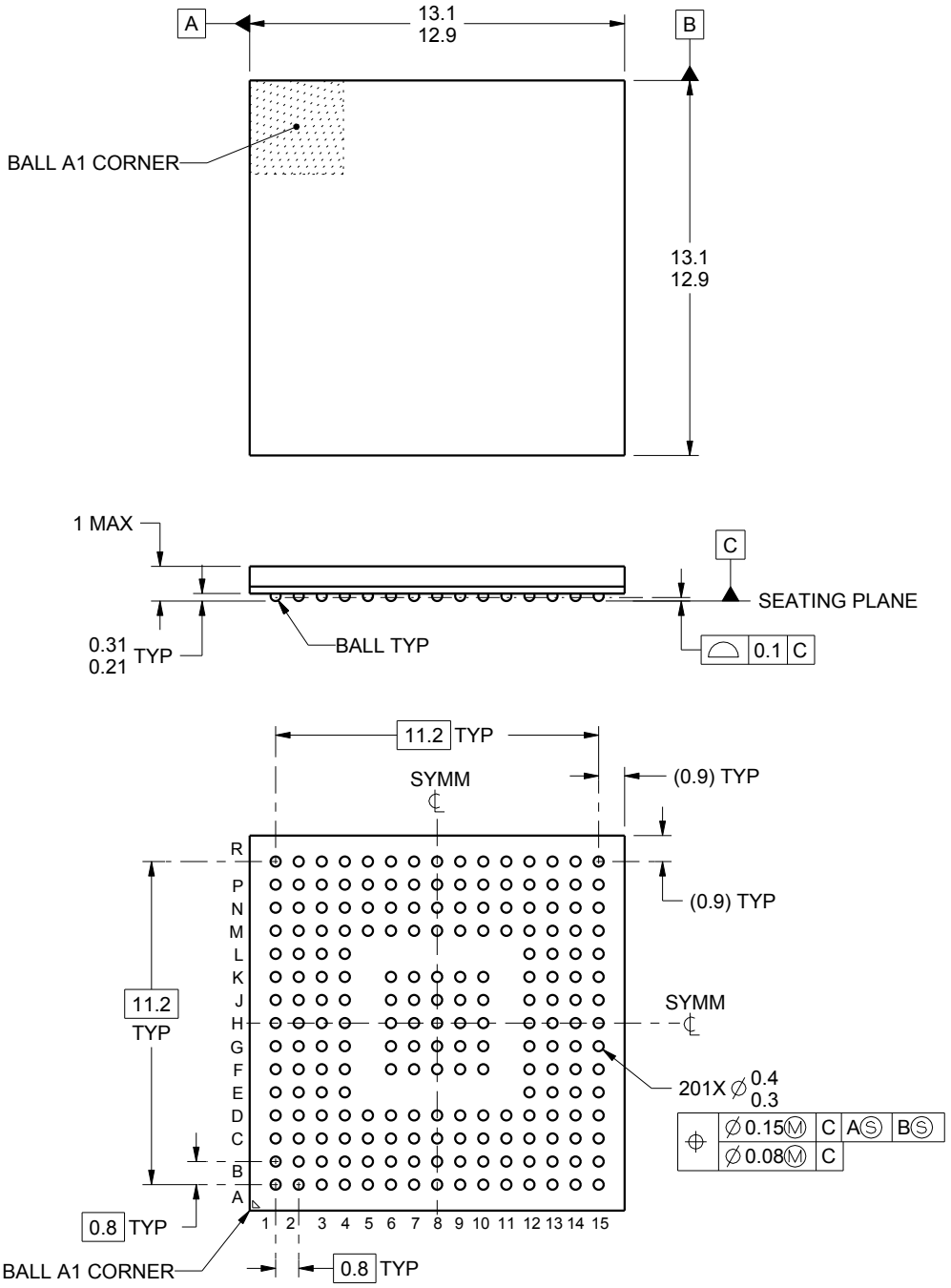
PACKAGE OUTLINE

ZEZ0201A

NFBGA - 1 mm max height

PLASTIC BALL GRID ARRAY



4221521/A 03/2015

NOTES:

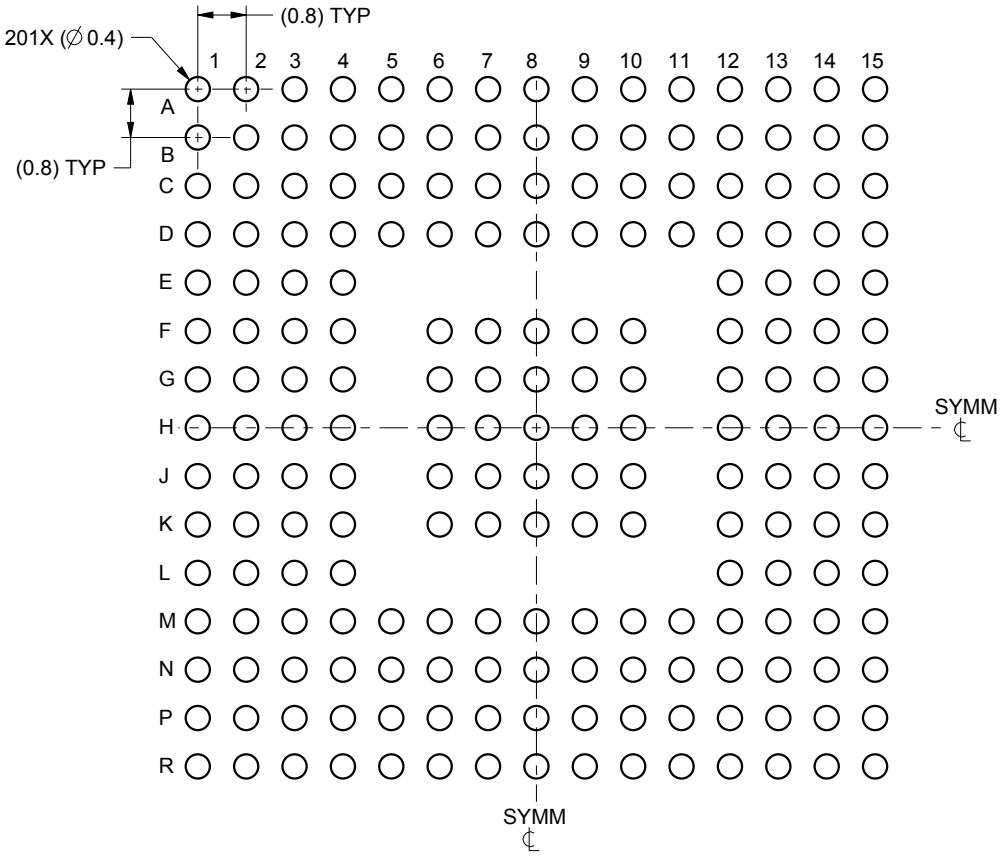
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

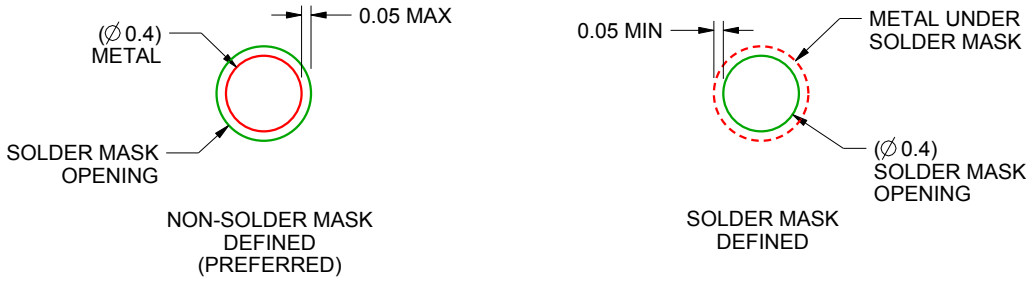
ZEZ0201A

NFBGA - 1 mm max height

PLASTIC BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:8X

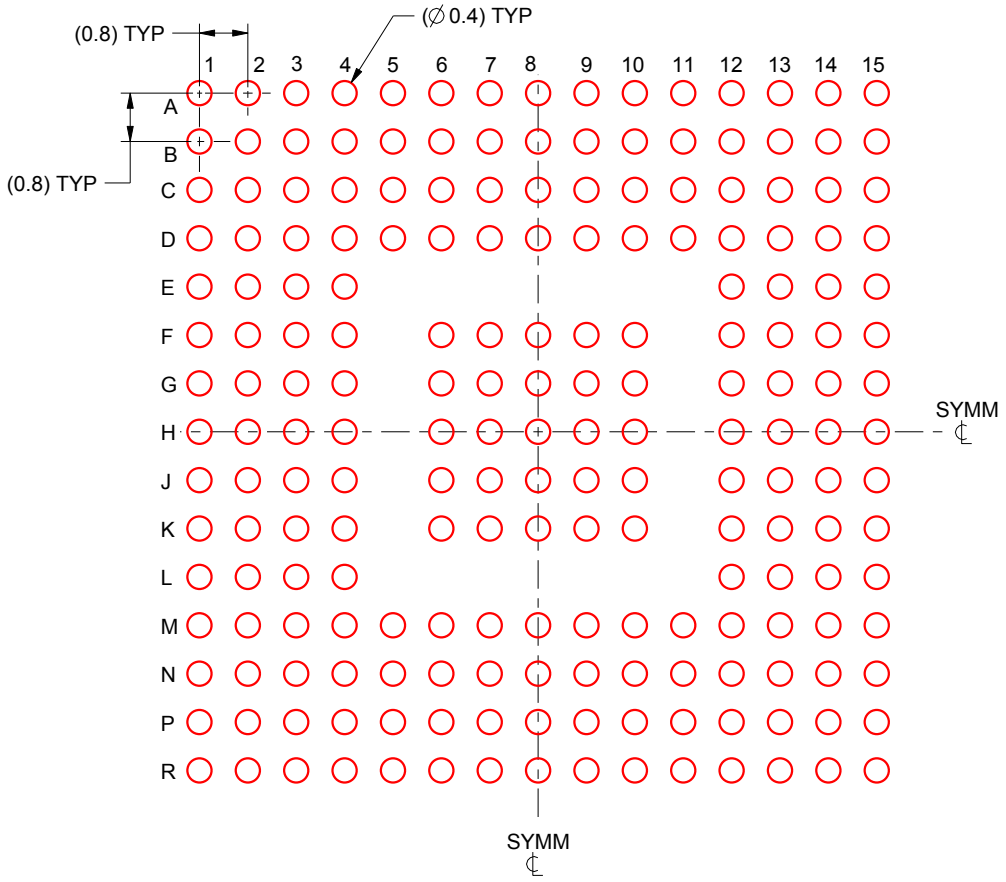


SOLDER MASK DETAILS
NOT TO SCALE

4221521/A 03/2015

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:8X

4221521/A 03/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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